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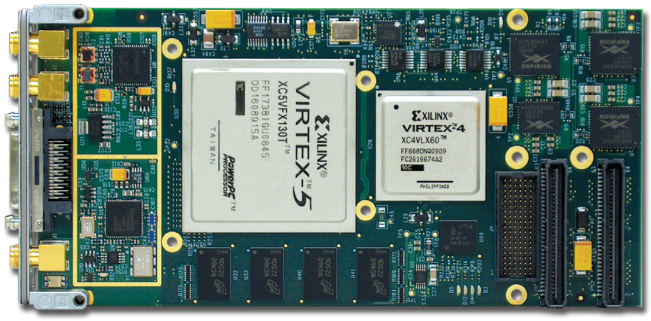
Find the *Vecima / Spectrum Signal Processing XMC-1131* at our website: ***Click HERE***

Dual 14-bit High-Speed ADC and Xilinx Virtex-5 Processing Engine

XMC-1131

Product Overview

The XMC-1131 is a key component in Spectrum's series of software-defined digital radio modules from the *flex*Comm™ wireless communications product line. The XMC-1131 has one dual channel 14-bit A/D converter running at up to 250 MSPS in a single-width VITA 42.0 XMC form factor. The ADC is integrated with a single user programmable Xilinx® Virtex-5™ FPGA device for wide bandwidth signal processing and filtering in the digital domain. The module can also be used as an Enhanced PMC (ePMC) module. The ePMC standard is fully compatible with IEEE P1386.1 PMC standard but offers the additional benefit of dedicated rapid Solano links between ePMC compliant carrier and mezzanine modules. Data can also be transferred over PCI, which provides the control path.



Features

- One dual channel 14-bit A/D converter sampling up to 250 MSPS
- Onboard clock provided for sample rate of 200 MSPS. Alternate VCXO may be provided for other sample rates as a future option*.
- XMC and Parallel RapidIO™* compatible module
- Can function as an enhanced PMC (ePMC) module using Solano Technology high-speed, low latency, deterministic data paths to processing engines
- A single user programmable Xilinx® Virtex-5™ FPGA device for wideband processing
- Total available bandwidth greater than 400 MB/s full duplex communication
- Two banks of 256 MB of DDR2 additional SDRAM memory available to the user FPGA
- 32-bit/33 MHz PCI host bus interface for control and data transfer. 66 MHz available as a future option*.
- JTAG connector compatible with Xilinx's ChipScope™ debugger
- 34-pin front panel digital I/O

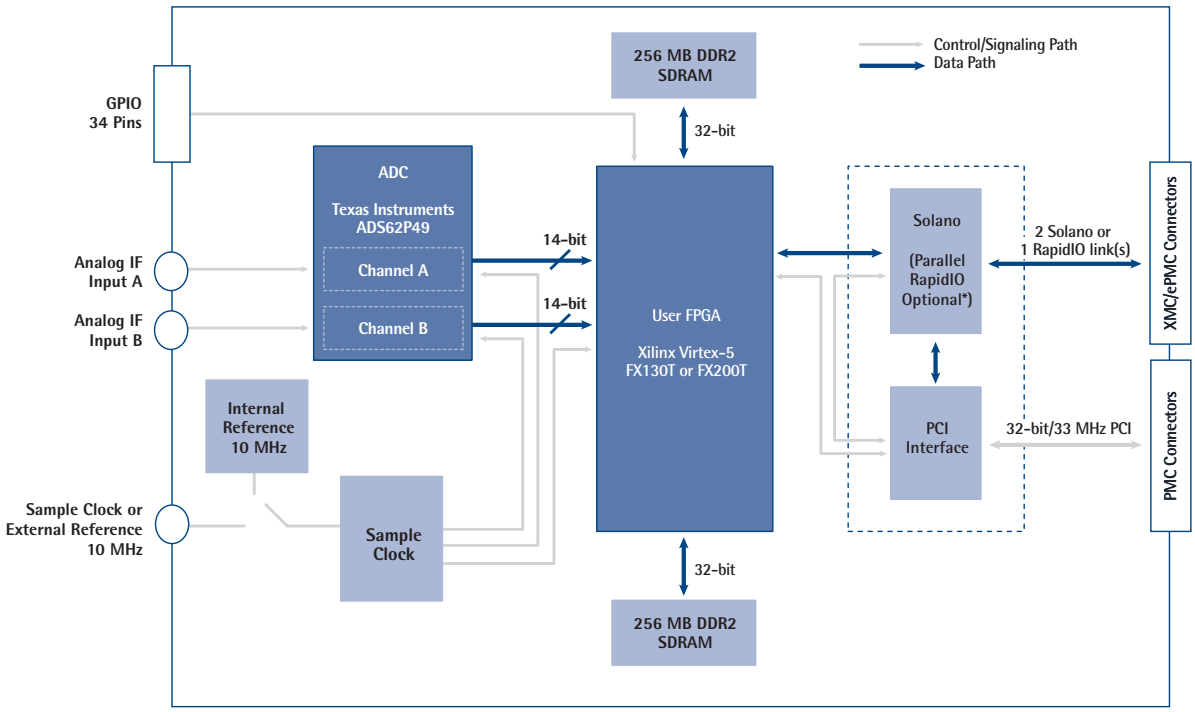
Benefits

- Allows conversion and processing of 160 MHz IF signals at 80 MHz bandwidth
- Enables coherent sampling over multiple boards, with GPS-based time synchronization
- Flexible platform that enables modular architecture design
- High-speed, low latency, deterministic data paths to carrier board

Applications

- Signals Intelligence (Wideband Spectral Analysis, Multichannel Direction Finding)
- Electronic Support Measures
- Electronic Countermeasures
- Phased Array Surveillance RADAR
- Military Communications/Military Satellite Communications including wireless gateways and satellite earth stations

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XMC-1131 Block Diagram

Architecture

[XMC and Parallel RapidIO*]

The XMC-1131 is a VITA 42.0 XMC compliant module. The VITA 42.0 XMC Mezzanine Card standard defines physical features that enable switched communications between a standard mezzanine card and its carrier. These features include the addition of two connectors carrying the additional electrical signals necessary for such communications.

As a future option*, the XMC-1131 may be made compliant with the VITA 42.1 Parallel RapidIO standard that uses a point-to-point scalable switched-fabric for its transport layer. The standard uses LVDS signaling with a double-data-rate clocking methodology, and supports both 8 and 16-bit link widths. The XMC-1131 module may support two 8-bit link widths (one per XMC connector) at 500 MB/s per link.

[ePMC - Solano Communications Technology]

The XMC-1131 is an ePMC module, employing Solano Communications technology that provides high bandwidth data paths between ePMC mezzanine modules and ePMC carriers. Each Solano high-speed link is capable of greater than 200 MB/s full-duplex communications. A data network implemented using this Solano Communications technology provides system throughput that can be many times higher than that offered by conventional bused or serial link architectures. The XMC-1131 Solano Communication fabric enables the module to simultaneously transmit and receive data streams to/from other processing units at a sustained 400 MB/s per channel.

[A/D Converters]

The XMC-1131 uses one ADS62P49 14-bit ADC, sampling at rates from 40 to 250 MHz. AC coupled SFDR is a minimum of 70 dB at 10.7 MHz, 21.4 MHz, 70 MHz, and 160 MHz when inputs are used independently. The input includes a transformer coupling circuit, which has a passband of 0.25 MHz to 300 MHz. DC coupled analog inputs are available as a future option*.

* See future options section of this datasheet.

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[Sample Clock]

The sample clock may be supplied from an external source for sampling rates of 40 to 250 MSPS. An onboard 200 MHz VCXO is included, which can be referenced to either an external reference input or an internal onboard 10 MHz reference.

[Front Panel GPIO]

A General Purpose I/O (GPIO) connector is available on the front panel. This connector allows access to 15 differential input/output LVDS pairs, 2 LVTTL data and 2 LVTTL global clock bi-directional pins for synchronization, triggering, timestamping and RF receivers/transmitters control. Multiple XMC-1131 modules can be synchronized to each other via the GPIO connector. This connector also allow the synchronization with frequency references, IRIG-B time stamp and software initiated events.

Software

[*quic*Comm™ Software Development Kit (SDK)]

*quic*Comm software equips users with basic link level access and control of Spectrum's *flex*Comm products. *quic*Comm significantly accelerates user application development. It is also standard across all *flex*Comm products, allowing code portability. This software includes a board support package for control and data handling which:

- Allows configuration and control of the Solano links between the processors and the ePMC modules
- Initiates and manages data transfers
- Manages interrupts
- Enables dynamic loading on a processor without affecting other processors

As a part of Spectrum's *quic*Comm package, an FPGA wrapper is provided to abstract all board level interfaces on the Virtex-5 user FPGA, including the interfaces to the analog converters, communication fabrics and control. The wrapper is designed so users can expedite the integration of third party or custom FPGA IP cores into the XMC-1131 module.

[Xilinx's ISE Foundation]

ISE Foundation is an integrated programmable logic design environment. It includes: schematic capture, power analysis tools, physical synthesis for FPGAs, advanced Place and Route Algorithms, HDL Advisors, and Timing Cross-Probing. ISE Foundation also contains COREgenerator, a graphical interactive design entry tool that is used to create high-level modules. COREgenerator gives access to a library of hundreds of FPGA IP cores, many of them free, from Xilinx and third-party vendors. This library includes DSP applications such as digital down converters (DDC), direct digital synthesizers (DDS), FIR filters, FFT, numerically controlled oscillator (NCO), memory controller, and much more.

[RF Engines]

Spectrum has partnered with RF Engines Ltd. (www.rfel.com) to offer integrated IP cores and turnkey designs for digital RF signal processing in FPGAs to speed development. RF Engines' IP cores are highly optimized in terms of speed, power and size compared to cores available from the major FPGA vendors. As an option, Spectrum can integrate the following RF Engines FPGA IP cores: dual 16K point FFT, 32K point FFT, tunable multi-channel receiver, distributed half band filter, and fixed point to floating point converter core.

For application specific requirements, Spectrum can develop custom cores for clients when these are otherwise unavailable. If you have such a requirement, please contact Spectrum Sales.

* See future options section of this datasheet.

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Specifications

[general]	FPGA Device	A single user-programmable Xilinx Virtex-5 FX130T or FX200T
	External Sampling Clock	40 to 250 MHz, 0.75 - 1.6 Vpp
[analog input]	A/D Converter	One Texas Instruments dual channel ADS62P49 14-bit @ 200 MHz @ up to 250 MHz
	ADC Input	AC coupled, full scale 2 Vpp into a 50 ohm load, single ended 3dB input bandwidth: 250 kHz – 190 MHz
	ADC SFDR	@ 200 MSPS, -1dBFS input: 10.7 MHz IF (10 MHz BW) > 85 dB typical 21.4 MHz IF (20 MHz BW) > 85 dB typical 70 MHz IF (30 MHz BW) > 70 dB typical 160 MHz IF (70 MHz BW) > 70 dB typical
[external interfaces]	Analog IF Input/Output, External Sampling Clock	SMA Socket 50 ohms
	or 10 MHz Reference	SMA Socket 50 ohms, 40 to 250 MHz, 0.75 to 1.6 Vpp
	PMC host PCI bus	32-bit/33 MHz PCI interface following IEEE P1386.1 specification
	JTAG Connection	JTAG connector for Virtex-4/5 FPGA, Xilinx ChipScope™ debugger compatible
	ePMC Interface	Two Spectrum Solano links, each providing greater than 200 MB/s (full-duplex)
[compatibility]	Carrier	PRO-1900/PRO-1901 Intelligent ePMC Carrier Board and I/O Expansion Daughter Board PRO-2900 PCI/PCI-X to ePMC/XMC Carrier PRO-2910 PCIe to XMC Carrier PRO-4600 3U CompactPCI Processing Engine
	Operating System	Refer to carrier specifications
[development software]	Application Libraries	*quic*Comm Software Development Kit
	FPGA Code Development	ISE Foundation tools from Xilinx and ModelSim® PE from Model Technology are required, Synplify Synthesis® from Synplicity is recommended
	HDL coding language	VHDL
[electrical]	Supply Voltage (DC)	Supply Voltage +5V, 3.3V +5%/-3% (supplied by PMC connector)
	Power Consumption	20 W typical
[environmental]	Temperature	Air-cooling operating temperature range of 0 to 50 degrees C, forced air @ 600 LFM
	RoHS	5 of 6 compliant (Pb solder exemption). For RoHS ordering information, other RoHS compliance options or certificates of compliance, please contact Spectrum Sales.
[ordering information]	650-00594	XMC-1131 for PRO-1900-Commercial Air Cooled-V5FX130T
	650-00600	XMC-1131 for PRO-1900-Commercial Air Cooled-V5FX200T
	650-00601	XMC-1131 for PRO-2910-Commercial Air Cooled-V5FX130T
	650-00604	XMC-1131 for PRO-2910-Commercial Air Cooled-V5FX200T
	650-00610	XMC-1131 for PRO-4600-Commercial Air Cooled-V5FX200T
	650-00612	XMC-1131 for PRO-4600-Commercial Air Cooled-V5FX130T
	650-00614	XMC-1131 for PRO-4600-Commercial Conduction Cooled-V5FX200T
[compatible modules]	ePMC-8120	Xilinx Virtex-II Processing Engine
	ePMC-PPC	PowerPC Processing Module
	XMC-2131	Dual 14b 300 MSPS DAC with Xilinx Virtex-5 Processing Engine
[future options]		Future options may be implemented at the discretion of Vecima Networks Inc. or its subsidiaries based on market demand.**
	Alternate PMC Host PCI Bus	66 MHz PCI interface
	XMC Interface	Two 8-bit Parallel RapidIO links
	Sample Clock	Alternate VCXO frequencies
	Alternate I/O	DC coupled analog inputs
	Additional Modules	XMC-8131 FPGA Processing Engine XMC Module

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