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Instruction Bulletin

Subject: **SY/MAX®**

CLASS 8030 TYPE RIM-131,
HIGH SPEED COUNTER MODULE

DESCRIPTION:

The Class 8030 Type RIM-131 SY/MAX High Speed Counter Module provides SY/MAX Programmable Controllers with the ability to receive high speed inputs in any of three standard modes. This instruction bulletin describes the installation, programming, operation, and troubleshooting of the High Speed Counter Module.



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1.0 DESCRIPTION OF CLASS 8030 TYPE RIM-131 MODULE

1.1 Introduction

1.1.1 WHAT DOES IT DO?

The Class 8030 Type RIM-131 high speed counter module can count pulses up to a speed of 100,000 cycles per second (100 KHz). It features three outputs, two of which can be individually energized at a predetermined count between +8,388,607 and −8,388,608, and a third to indicate counter underflow or overflow.

The high speed counter module (HSCM) can also communicate with a SY/MAX Class 8020 Programmable Controller (PC). By means of appropriate ladder diagram program, the PC can read and write HSCM data. This data can be the latest count value, new decode values, or other HSCM status.

Three different counting modes are usable with the module.

1. Rotary pulse generator (quadrature pulses).
2. Single count pulse train with direction signal.
3. Separate count-up and count-down pulse trains.

Typical input devices are proximity switches and incremental encoders.

The high speed counter module also has an overflow/underflow output which energizes should either condition occur. Error lights and self checking are incorporated.

Typical applications for the HSCM include cut-to-length, flow monitoring, injection molding, woodworking, and machining.

1.1.2 SUMMARY OF OPERATION

The HSCM uses medium scale integrated circuits for counting. An Intel 8031 microprocessor is used. All inputs and outputs are optically isolated from the logic of the microprocessor bus.

For more information, see Section 2, Specifications or Section 7, Theory of Operation.

1.2 Front View of Module



Figure 1.1 - Front View of High Speed Counter Module

1.2.1 DESCRIPTION OF FRONT OF MODULE

Figure 1.1 depicts the front of the high speed counter module. At the top front of the module is the nameplate. Below the nameplate are seven light emitting diodes (LED's). These LED's are fully described in Section 1.2.2.

Below the LED's are three front accessible fuses, one for each of the three outputs. Starting from the top, the fuses are for the Decode 1, Decode 2 and Overflow outputs.

Beneath the fuses are the terminals for connecting field wiring to the HSCM. The terminals are divided into two groups, outputs and inputs.

Outputs are, from the top terminal down, V+, DEC 1, DEC 2, overflow, and COM.

Inputs are V+, CHA, CHB, CNT EN, RES, and COM.

Detailed specifications on I/O are given in Section 2.1.

1.2.2 LED DESCRIPTION

There are seven LED's on the high speed counter module.

Number	LED Label	Color	Function
1	Count enable	Green	Illuminated when count is enabled unless counter is overflowed.
2	Reset	Red	Illuminated when the Reset Input has been energized
3	Decode 1	Red	Illuminated when Decode 1 Output is energized
4	Decode 2	Red	Illuminated when Decode 2 Output is energized
5	Overflow	Red	Illuminated when data overflows or underflows
6	Data Error	Red	Illuminated when processor has furnished bad data during Decode 1, Decode 2, or preset down-load.
7	Module Error	Red	Illuminated when the module self-diagnostics has detected an error.

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1.3 Rear view of module



Figure 1.2 - Rear View of High Speed Counter Module

1.3.1 DESCRIPTION OF REAR OF MODULE

Figure 1.2 depicts the rear of the high speed counter module. Access to the DIP switches for module setup is from the rear of the module.

1.3.2 DIP SWITCH DESCRIPTION

DIP switches are described in the following tables:

Switch Number	"ON" Function
1	See mode table
2	See mode table
3	Debounce for Channel A Input
4	Debounce for Channel B Input
5	Debounce for Count Enable Input
6	Debounce for Reset Input
7	Upon energization of the Reset Input, load preset value
8	Not used

Mode Table

Mode	Switch 1	Switch 2
Rotary Pulse (quadrature)	off	off
A=COUNT; B=DIRECTION	off	on
A=UP COUNT; B=DOWN COUNT	on	on
ILLEGAL MODE—DO NOT USE	on	off

This table appears on the side of the High Speed Counter Module.

2.0 SPECIFICATIONS

2.1 Electrical Specification

2.1.1 NUMBER OF INPUTS AND OUTPUTS

The HSCM has four 5 VDC to 24VDC inputs. There are three 5 VDC to 24 VDC outputs.

2.1.2 SY/MAX REGISTER USAGE

The HSCM uses 16 SY/MAX registers for Rack Addressing. These registers allow the user program to access status and data of the HSCM. They also allow the programmable controller to control the HSCM.

2.1.3 DETAILED SPECIFICATIONS

Detailed input specifications:

Inputs per module. 4
Type and rated isolation between
input terminal and logic: . . . . . optical, 2000 VRMS

Parameters	Logic 0	Logic 1
Signal	Low	High
User current sink required (per input)	16mA	N.A.
User current source required (per input)	N.A.	0*
User supply voltage required	5 to 24 VDC	

*Cable capacitance may require some current source.

All inputs share a common ground

Input signals must be 0 to 100 KHz square waves. The minimum time between state changes is five microseconds. (50% duty cycle at 100 HKz). Notice that input devices must be current sinking. See section 3.4.1 to determine the suitability of a particular input device.

Detailed output specifications:

Outputs per module: 3
Type and rated isolation between
output terminal and logic: . . . . . optical, 2000 VRMS

Parameters	Logic 0	Logic 1
Decode	True	False
Signal from processor	Off	On
Output voltage	5 to 24 VDC	0
Module current Sink Capability	250mA	N.A.
Module current Source capability	N.A.	0
Leakage current	N.A.	1.0mA at V= 5 to 24 VDC
User supply voltage *Requirements*	5 to 24 VDC	

All outputs share a common ground

Module draw on SY/MAX power supply = 1.2 A

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2.2 Physical Specifications

2.2.1 WEIGHT (UNPACKAGED)

LB/KG 2.75/1.25

2.2.2 DIMENSIONS

13.0 x 6.6 x 1.5 (HxDxW) inches
29.1 x 14.8 x 3.4 (HxDxW) cm
Mounting attitude must be vertical

2.3 Environmental Specifications

2.3.1 AMBIENT TEMPERATURE RATING

Minimum	Maximum
32°F/0°C	140°F/60°C

2.3.2 HUMIDITY RATING

95% non-condensing

2.4 Compatibility with Racks

The HSCM is compatible with the following SY/MAX racks:

Class 8030 Type CRK-210
Class 8030 Type CRK-300
Class 8030 Type DRK-210
Class 8030 Type DRK-300
Class 8030 Type GRK-110
Class 8030 Type GRK-210
Class 8030 Type HRK-100
Class 8030 Type HRK-200
Class 8030 Type RRK-100
Class 8030 Type RRK-200

2.5 Compatibility with other Modules

Class 8030 Type ROM-131 Stepper Motor Controller Module.

2.6 Compatibility with SY/MAX Processors

The HSCM is compatible with the following SY/MAX processors:

Class 8020 Type SCP-311 Series E or Later
Class 8020 Type SCP-312 Series E or Later
Class 8020 Type SCP-313 Series D or Later
Class 8020 Type SCP-321 Series D or Later
Class 8020 Type SCP-322 Series D or Later
Class 8020 Type SCP-323 Series C or Later
Class 8020 Type SCP-332 Series D or Later
Class 8020 Type SCP-333 Series D or Later
Class 8020 Type SCP-344 Series C or Later

Class 8020 Type SCP-521
Class 8020 Type SCP-522
Class 8020 Type SCP-523

Class 8020 Type SCP-7XX
Class 8020 Type SCP-7XX
Class 8020 Type SCP-7XX
Class 8020 Type SCP-7XX

3.0 INSTALLATION

3.1 Physical Inspection

Square D Company tests, burns in and packs each module with great care. However, it is wise to give each module a quick visual inspection before installation. Check for any shipping damage that may have occurred.

Inspect the seven LED's to ensure they are visible through the module cut-out. Examine the field wiring terminals for damage. Inspect the hold-down screw on the lower portion of the HSCM to verify the screw is securely attached to the module. Examine the upper rear of the module to ensure the mounting plate is secure. Inspect the printed circuit edge connector for damage.

3.1.1 INSTALLING A NEW MODULE

When installing a new HSCM verify the socket into which it is being installed is either unkeyed or keyed to receive a HSCM. Do not attempt to force the module into place if the socket has been keyed for another module. Refer to Section 3.2, Module Keying.

The reset and data error lights will illuminate after power is applied to the rack. Rungs described in Section 3.7.1 must be executed to enable the module.

3.1.2 REPLACING AN EXISTING MODULE

When replacing an existing Class 8030 Type RIM-131, first remove all power from the Class 8030 Type PS Power Supply connected to the rack assembly in which the original HSCM is installed.

Remove power to all input and output devices wired to the HSCM. Next, remove the original HSCM, noting which slot the module was removed from. Compare DIP switch settings, and set DIP switches on the new module to match the old if this is the intended operation.

The terminal strip on the HSCM is removable to facilitate module replacement. Attach the original terminal strip to the new module if desired.

For details on DIP switch setting, see Section 3.3.

Install the new module, as described in 3.1.1.

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3.2 Module Keying

Each SY/MAX register rack slot and digital rack register socket may be keyed to accept only one type of SY/MAX register module. An optional keying pin kit, Class 8030 Type CBP-104, is available for this purpose. The correct position of the keying pin for the HSCM is between pins 12 and 14 as described in the register rack Instruction Bulletin #30598-265. See Figure 3.1, HSCM Keying Pin Location. The keying pin is simply inserted manually into the slot in the rack connector using the keying pin insertion tool provided with the kit. See Figure 3.2, Inserting Keying Pin.

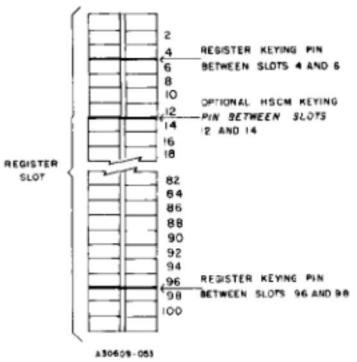


Figure 3.1 - HSCM Keying Pin Location

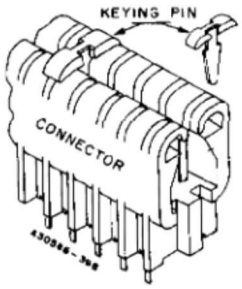


Figure 3.2 - Inserting Keying Pin

3.3 DIP Switch Settings

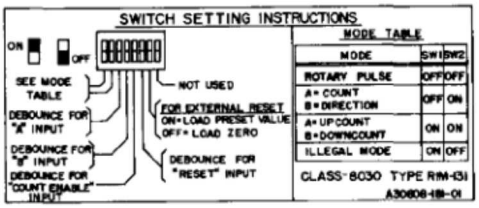


Figure 3.3 - DIP Switch Settings

Switch Number	"ON" Function
1	See mode table
2	See mode table
3	Debounce for Channel A Input
4	Debounce for Channel B Input
5	Debounce for Count Enable Input
6	Debounce for Reset Input
7	On hardware reset load preset value
8	Not used

Mode Table

Mode	Switch 1	Switch 2
Rotary Pulse (quadrature)	off	off
A=COUNT; B=DIRECTION	off	on
A=UP COUNT; B=DOWN COUNT	on	on
ILLEGAL MODE—DO NOT USE	on	off

3.4 Field Wiring Terminations

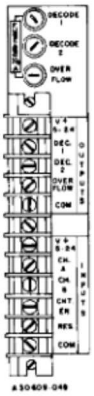


Figure 3.4 - Terminal Block

Field wiring is connected to the removable terminal strip on the front of the module. All terminations are self-lifting captive pressure terminals, for wire sizes AWG 18 to AWG 12 (0.8 mm² to 3 mm²).

Additional terminal blocks, Class 8030 Type CBP-110, may be purchased if desired.

The top 5 terminals are outputs.

> For safest operation, output devices controlled by the HSCM should be designed so that they are actuated only when HSCM outputs are switched ON, LOW Z to COM.

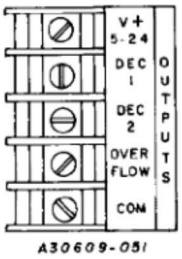


Figure 3.5 - Output Terminals

Terminal	Module Label	Description
1	V+ 5-24	User supplied voltage
2	DEC 1	Decode 1 Low-Z to COM when decode 1 true
3	DEC 2	Decode 2 Low-Z to COM when decode 2 true
4	OVER FLOW	Overflow Low-Z to COM when overflow true
5	COM	Common to V+, DEC 1, DEC 2, OVERFLOW.

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The lower 6 terminals are inputs.

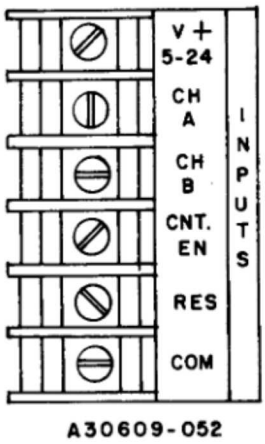


Figure 3.6 - Input Terminals

Terminal	Module Label	Description
6	V+ 5-24	User supplied voltage
7	CH A	Channel A input (Low = True)
8	CH B	Channel B input (Low = True)
9	CNT EN	Count enable input (Low = Enable)
10	RES	Reset input (Low = Reset)
11	COM	Common to V+, CH A, CH B, CNT EN, RES.

Notice that the function of the Channel A and Channel B inputs depends upon the mode for which the HSCM has been set. Section 3.3 explains DIP switch setting.

Wiring diagrams for the three modes of operation are shown in the next three figures.

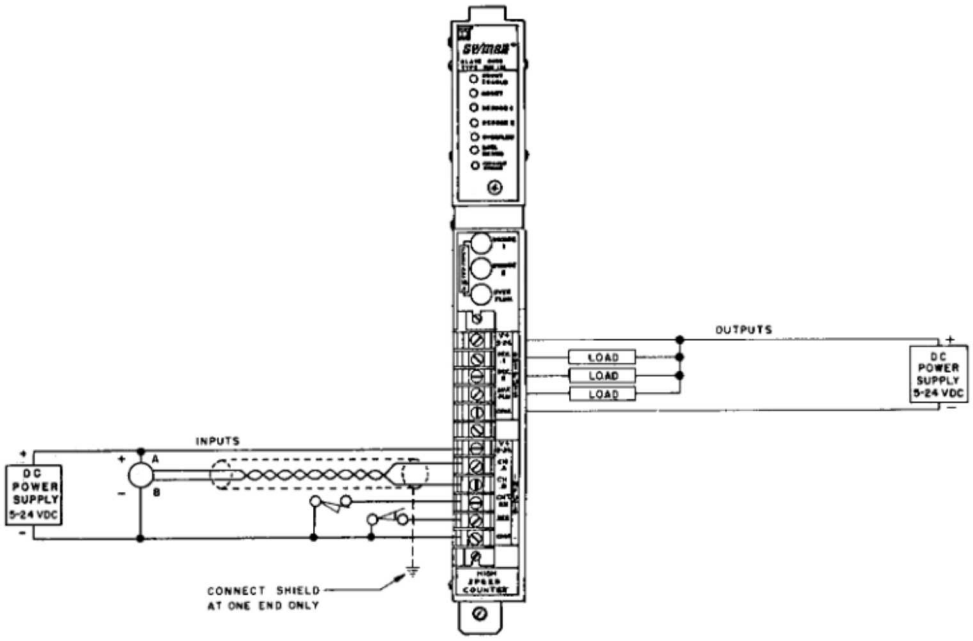


Figure 3.7 - Quadrature Encoder Wiring

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In this mode, Input A is always the count input. Input B, if open, will cause the count to increment. Input B, if switched to COM, will cause the count to decrement.

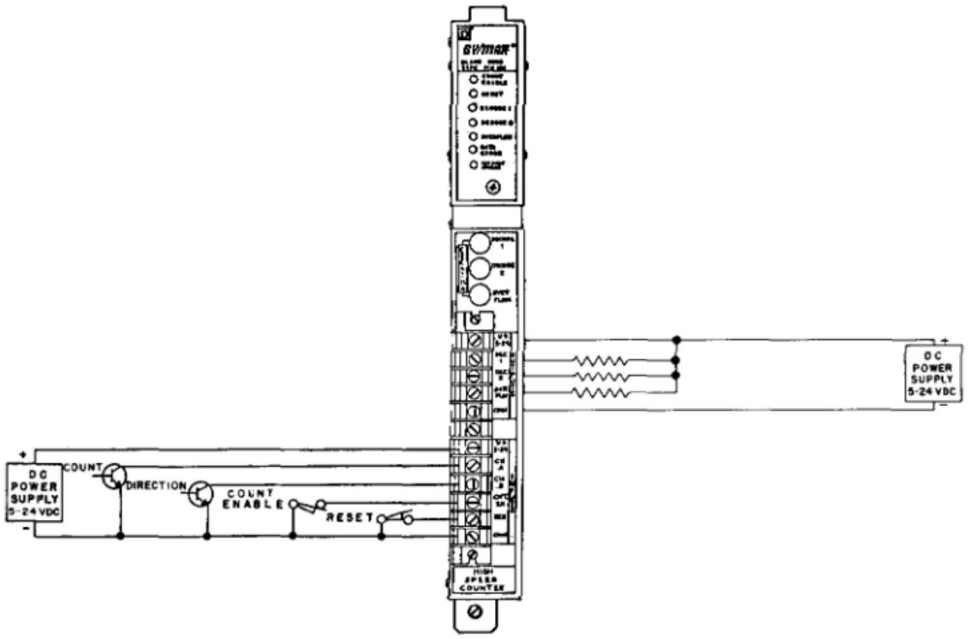


Figure 3.8 - Count-Up/Down Wiring

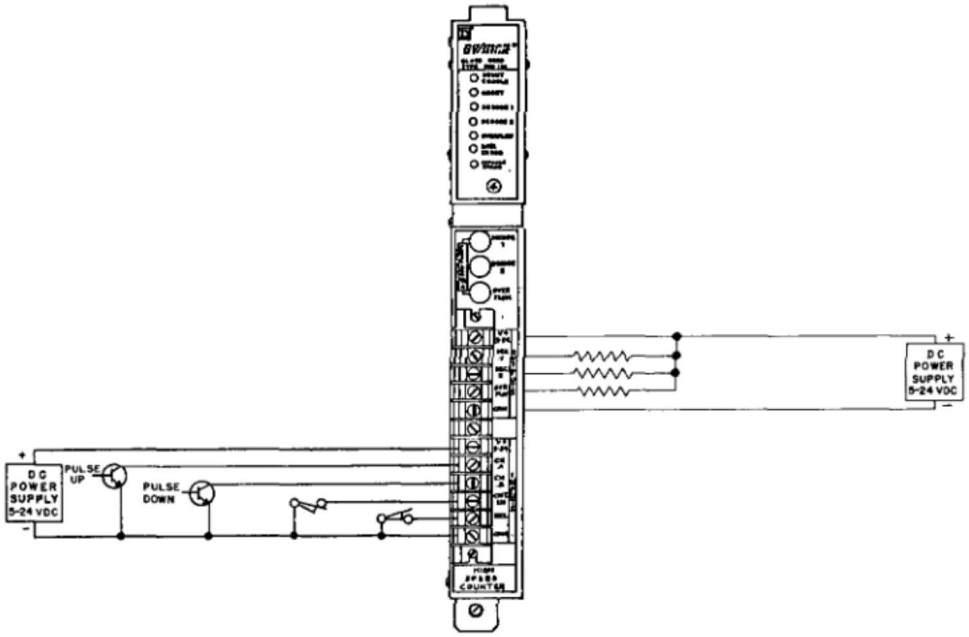


Figure 3.9 - Count Up/Count Down Wiring

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3.4.1 DETERMINING INPUT DEVICE SUITABILITY

The high speed counter module has versatile input circuitry, designed to work with current sinking devices. Figures 3.7, 3.8 and 3.9 all show current sinking inputs.

Current sinking inputs have a number of advantages over current sourcing inputs. These advantages are:

1) Compatibility with TTL integrated circuits.
2) Ability to work with open-collector transistor outputs.
3) Good noise immunity.

In order for the switching device to pull the input line low, the switching device must be able to change and discharge the cable capacitance and sink the current from the *constant current generator (8 mA) plus the current from* any pull-up resistor added.

Examples of pull-up resistor selection follow.

$$R_{PULL\text{-}UP} = \frac{1}{(10)\ (F_{HIGH})\ (l)\ (C/Length)} \quad \text{(equation 3.1)}$$

Where:

F_{HIGH} = Maximum operating frequency (Hertz)

= length of cable (units should be consistent with measurement of cable capacitance per length).

C/Length = Capacitance per unit length, where the unit of length is consistent with the length (l) measurement.

$R_{PULL\text{-}UP}$ = Maximum value of pull up resistor to satisfy operation.

This equation has a safety factor built in. It is based on the time necessary to charge the cable to the user V_{CC}.

Since many devices that are inputs to the high speed counter module may not be rated in terms of pull-up resistance, the following equation relates the minimum value of pull-up current to $R_{Pull\text{-}up}$:

$$I_{PULL\text{-}UP} = \frac{V_{CC}}{R_{PULL\text{-}UP}} \quad \text{(equation 3.2)}$$

If the input device cannot furnish sufficient pull-up current, an external pull-up resistor must be added. The resistor value may be calculated from the following equation:

$$R_{ADDED} = \frac{V_{CC}}{I_{PULL\text{-}UP} - I_{SOURCE}} \quad \text{(equation 3.3)}$$

Where:

V_{CC} = Value of user voltage

$I_{PULL\text{-}UP}$ = Required value of pull-up current from equation 3.2.

I_{SOURCE} = Maximum pull-up current user's switch is capable of sourcing (may be 0).

R_{ADDED} = Value of external pull-up resistor required.

In order for the switching device to pull the count line low, the switching device must be able to discharge the cable capacitance and sink the current from the constant current generator plus the current from any pull-up resistor added.

Since the constant current is typically 8 ma, the following equation may be used:

$$I_{SINK} \leq (40)(F_{MAX})(l)(c/ft) + \frac{V_{CC}}{R_{ADDED}} + .008 + \frac{V_{CC}}{3300}$$

(equation 3.4)

Where:

I_{SINK} = Required minimum sink current

F_{MAX} = Maximum frequency

l = *Cable length*

c/ft. = Cable capacitance/length

V_{CC} = User power supply voltage

R_{ADDED} = Any external pull-up resistors

Under conditions of high noise, it may be desirable to increase the energy required to produce a count pulse.

This may be done by decreasing the value of the pull-up resistor. The minimum value is given by the following equation:

$$R_{PULL\text{-}UP\ MIN} = \frac{V_{CC}}{(I_{OL} - I_{SINK})} \quad \text{(equation 3.5)}$$

Where:

V_{CC} = Value of user voltage

I_{OL} = Maximum current the user switch is capable of sinking

I_{SINK} = Sink current required from equation 3.4

$R_{PULL\text{-}UP\ MIN}$ =
Minimum value of pull-up resistor. If a resistor was specified in equation 3.3, a resistor equivalent to R_{ADDED} in parallel with $R_{PULL\text{-}UP\ MIN}$ may be used as the pull up resistor.

The following examples illustrate how these equations are used:

Example 1:

CABLE: Belden 9184 @ 8.8pf/ft.
50 ft. total

SWITCH: 74LS125
I_{OH} = 2.6 ma
I_{OL} = 24.0 ma

USER VOLTAGE: 5 VDC

MAX. FREQ: 50 KHz

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From equation 3.1:

$$R_{PULL\text{-}UP} = \frac{1}{(10)\,(50\text{x}10^{3})\,(50)\,(8.8\text{x}10^{-12})}$$

$$= 4.545\text{k}$$

Using equation 3.2, the minimum pull-up current is:

$$I_{PULL\text{-}UP} = \frac{5}{4.545\text{k}}$$

$$= 1.1 \text{ ma}$$

The 74LS125 gate will furnish 2.6 ma so no pull-up resistor is required.

Using equation 3.4:

$$I_{SINK} = (40)\,(50\text{x}10^{3})\,(50)\,(8.8\text{x}10^{-12}) + 0 + .008 + \frac{5}{3300}$$

$$= 10.4 \text{ ma}$$

The 74LS125 gate is able to sink more than 10.4 ma. so the circuit design will operate as intended.

Example 2:

CABLE: Belden 9406 @ 95 pf/ft.
30 ft. total

SWITCH: 74LS125
I_{OH} = 2.6 ma
I_{OL} = 24.0 ma

USER VOLTAGE: 5 VDC

MAX. FREQ: 50 KHz

From equation 3.1:

$$R_{PULL\text{-}UP} = \frac{1}{(10)\,(50\text{x}10^{3})\,(30)\,(95\text{x}10^{-12})}$$

$$= 702 \text{ ohm}$$

Using equation 3.2 for minimum pull-up current:

$$I_{PULL\text{-}UP} = \frac{5}{702}$$

$$= 7.1 \text{ ma}$$

Since the 74LS125 switch will only supply 2.6 ma, an external pull-up resistor is required.

$$R_{ADDED} = \frac{5}{(7.1 - 2.56)\text{ x } 10^{-3}}$$

$$= 1101 \text{ ohm}$$

A 1000 ohm resistor is practical to use.

To see if there is sufficient sink current, use equation 3.4:

$$I_{SINK} = (40)\,(50\text{x}10^{3})\,(30)\,(95\text{x}10^{-12}) + \frac{5}{1000} + .008 + \frac{5}{3300}$$

$$= 20 \text{ ma}$$

Since the 74LS125 switch can sink 24 ma, this design will work.

Example 3: Same as example 2 except 50 feet of cable.

$$R_{PULL\text{-}UP} = \frac{1}{(10)\,(50\text{x}10^{3})\,(50)\,(95\text{x}10^{-12})}$$

$$= 421 \text{ ohm}$$

Solving equation 3.2 for minimum pull-up current:

$$I_{PULL\text{-}UP} = \frac{5}{421}$$

$$= 12 \text{ ma}$$

$$I_{SINK} = (40)\,(50\text{x}10^{3})\,(50)\,(95\text{x}10^{-12}) + \frac{5}{421} + .008 + \frac{5}{3300}$$

$$= 31 \text{ ma}$$

The 74LS125 switch can only handle 24 ma, so this design will not work. A cable with lower capacitance per unit length, or a shorter cable will fix the problem.

Example 4:

CABLE: Belden 9184 @ 8.8 pf/ft.
200 ft. total

SWITCH: GEMCO "ROTO-PROX"
I_{OH} = 0 mA
I_{OL} = 200 mA

USER VOLTAGE: 24 VDC

MAX. FREQ: 400 Hz

Since the GEMCO switch will source no current, a pull-up resistor is required.

Using equation 3.1:

$$R_{PULL\text{-}UP} = \frac{1}{(10)\,(400)\,(200)\,(8.8\text{x}10^{-12})}$$

$$= 142\text{K ohm}$$

Using equation 3.4 to find the minimum sink current:

$$I_{SINK} = (40)\,(400)\,(200)\,(8.8\text{x}10^{-12}) + \frac{24}{142{,}000} + .008 + \frac{24}{3300}$$

$$= 16 \text{ ma}$$

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Since the switch can sink 200ma, there is sufficient margin. To find the smallest pull-up resistor possible, use *equation 3.5:*

$$R_{PULL\text{-}UP\ MIN} = \frac{24}{(200\text{-}16) \times 10^{3}}$$

$$= 130 \text{ ohm}$$

A pull-up resistor between 130 ohm and 142 K ohm will work. The smaller the value, the more energy is necessary to switch the circuit.

3.5 Compatibility with Racks

The HSCM is compatible with the following SY/MAX racks.

Class 8030 Type CRK-210
Class 8030 Type CRK-300
Class 8030 Type DRK-210
Class 8030 Type DRK-300
Class 8030 Type GRK-110
Class 8030 Type GRK-210
Class 8030 Type HRK-100
Class 8030 Type HRK-200
Class 8030 Type RRK-100
Class 8030 Type RRK-200

3.6 Security

Security is provided by proper keying of the rack in which the high speed counter module is located.

Fencing of registers assigned to the HSCM will also increase security.

Additionally, both the hardware enable and the software enable must be true in order to enable the count. This will prevent counting and potential hazards until two deliberate steps are taken to enable the counter.

Both the hardware reset and the software reset must not be true in order to count.

3.7 Start-up

A successful start-up of the HSCM will occur more easily if a few steps are followed. Ensure that the previous sections of this instruction bulletin, such as field wiring, Section 3.4, and DIP switch settings, Section 3.3, are understood before proceeding with this section.

The user must verify that the signals being supplied to the HSCM are suitable. Are the voltage, frequency, duty cycle, and current within specification? Encoder manufacturers are a source for this information.

If a proximity switch or other high speed input is being used, it may be necessary to examine the waveform by using an oscilloscope.

A very common problem in start-up is improperly set DIP switches. Be *absolutely* sure DIP switches are correctly set. See Section 3.3 for DIP switch settings.

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3.7.1 NECESSARY PROCESSOR INSTRUCTIONS

Figure 3.10 shows the 4 rungs necessary for high speed counter module start-up. Notice that the I/O addresses and register addresses used are for example only. For any given application, all I/O addressing will depend upon the rack addressing scheme for the SY/MAX Processor working with the high speed counter module.

Immediately following rack power-up, the reset and data error lights of the HSCM will illuminate. This is normal, until the following "load all start" rungs are executed.

IMPORTANT: Using the data enter mode of SY/MAX Programmable Controller programming equipment will not load data into the HSCM module registers. Data loaded using the data enter mode will appear to be in the registers assigned to the high speed counter module. The data is *not* transferred from the SY/MAX Processor to the HSCM until the proper loading rungs are executed.

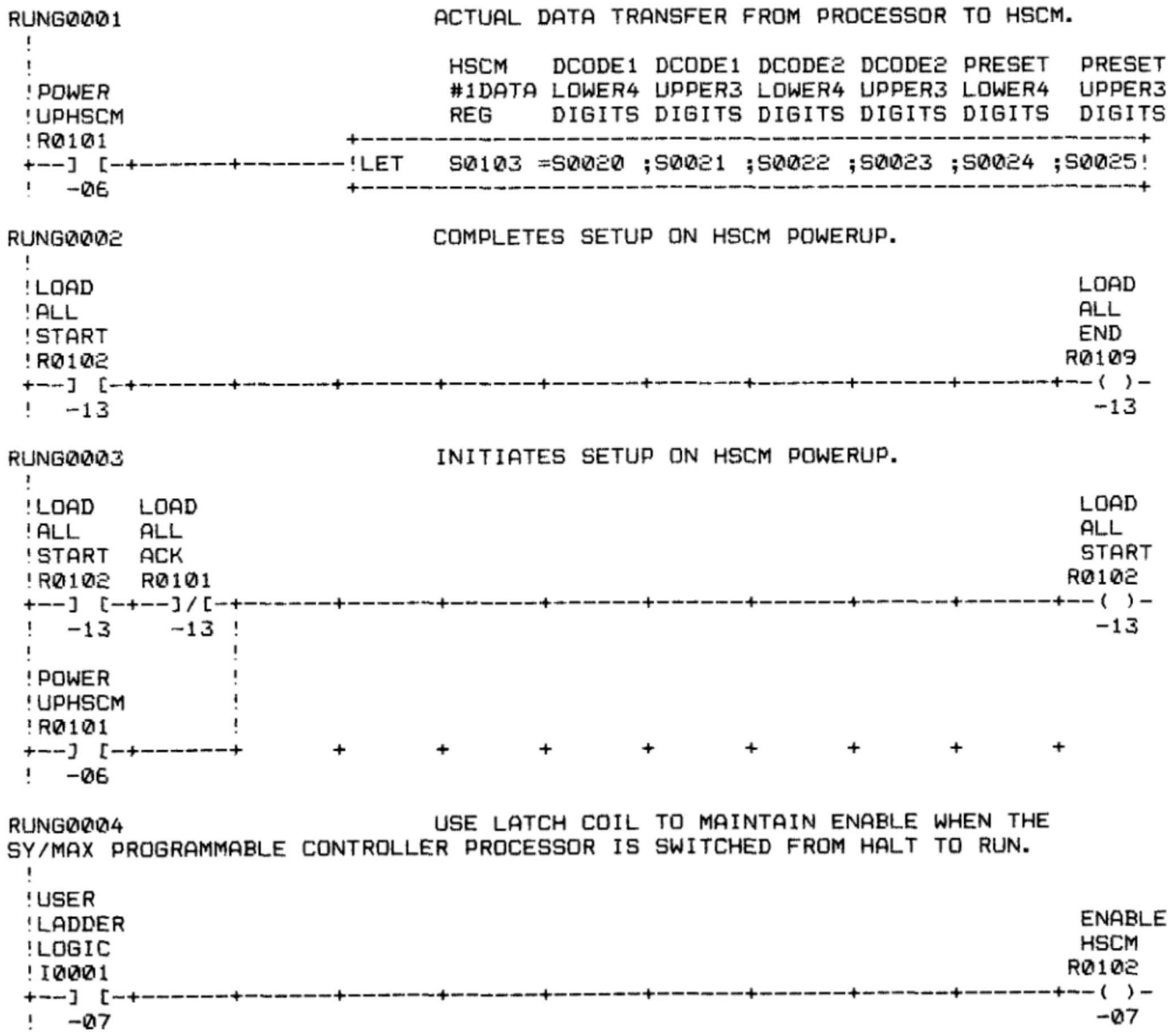


Figure 3.10 - "Load All Start" Rungs

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Rung 1 is the actual data transfer from the SY/MAX Processor to the HSCM. Data is loaded into the third through the eighth HSCM registers from processor registers 20 through 25.

HSCM* Register	Processor Register	Function
103 ←—	20	Decode 1 least significant register
104 ←—	21	Decode 1 most significant register
105 ←—	22	Decode 2 least significant register
106 ←—	23	Decode 2 most significant register
107 ←—	24	Preset least significant register
108 ←—	25	Preset most significant register

* Register addresses typical, actual address may differ, depending on the Rack Addressing scheme.

Rung 2 completes the load all sequence.

Rung 3 initiates the load all sequence.

Rung 4 enables the high speed counter module following the load all sequence.

The four start-up rungs *must* be programmed in this order.

If it is desired to perform a "load all start" operation under manual or program control, a *transitional* contact may be placed in parallel with HSCM contact 1-6, in Rung 3, the power up HSCM contact (101-6 for this example).

If it is necessary to have the HSCM count while the SY/MAX Processor is switched from HALT to RUN, the rung enabling HSCM register 2, bit 7 must use a latching coil.

If the hardware enable is also true and the HSCM is not in RESET, the green "COUNT ENABLE" LED will be illuminated.

Summary of start-up steps.

1. SY/MAX Processor in RUN.
2. External wiring correct.
3. "Load all start" rungs executed.
4. Hardware enable true.
5. Software enable true HSCM register 2 bit 7.
6. Module not in reset.

3.7.2 NORMAL STATE OF INDICATING LIGHTS

During normal operation, the green "COUNT ENABLE" LED will be on whenever the count is enabled (both hardware *and* software enables are required).

If the counter is in reset, the RESET LED will be on. The RESET light will cause all other non-error LEDs to turn off, unless DEC 1 and DEC 2 outputs have been programmed to turn on at count = zero.

The DECODE 1 LED will be illuminated whenever the count value is logically true in comparison to the DECODE 1 value.

If the comparison is not logically true, the DECODE 1 LED will not be illuminated.

The DECODE 2 LED behaves the same way. The DECODE 2 LED will be illuminated whenever the count value is logically true in comparison to the DECODE 2 value.

If the comparison is not logically true, the DECODE 2 LED will not be illuminated.

DECODE 1 and DECODE 2 are programmed independently, and therefore, their states (on or off) are independent.

At any particular time, depending on count value, the DECODE 1 LED and the DECODE 2 LED may be in any of 4 possible states.

STATE TABLE

Logical Comparison	Decode 1 LED	Decode 2 LED
Decode 1 True	On	X
Decode 1 Not True	Off	X
Decode 2 True	X	On
Decode 2 Not True	X	Off

If the high speed counter module is reset, both the DEC 1 output and the DEC 2 output will be turned off.

Halting the SY/MAX Processor will turn off both the DECODE 1 and DECODE 2 LEDs and the DEC 1 and DEC 2 outputs. The count value is *not* reset by halting the Processor. The counter will continue to count input pulses even if the SY/MAX processor is halted.

It is possible to test all LED's with the test routine described in Section 6.2. This "confidence" test is a self check that tests the HSCM thoroughly.

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4.0 PROGRAMMING

4.1 Register Usage for Rack Addressing

As mentioned in Section 2.1.2, the High Speed Counter Module requires 16 SY/MAX registers.

Register*	Read By: Processor	Read By: HSCM	Written By: Processor	Written By: HSCM	Function
1	Yes	No	No	Yes	HSCM status
2	Yes	Yes	Yes	No	Processor to HSCM control
3	Yes	Yes	Yes	No	Least significant 4 digits Decode 1 set point
4	Yes	Yes	Yes	No	Most significant 3 digits Decode 1 set point
5	Yes	Yes	Yes	No	Least significant 4 digits Decode 2 set point
6	Yes	Yes	Yes	No	Most significant 3 digits Decode 2 set point
7	Yes	Yes	Yes	No	Least significant 4 digits Preset count value
8	Yes	Yes	Yes	No	Most significant 3 digits Preset count value
9	Yes	Yes	Yes	No	Processor to HSCM control
10	Yes	Yes	No	Yes	Least significant 4 digits of Count value
11	Yes	Yes	No	Yes	Most significant 3 digits of Count value
12	Yes	No	No	Yes	Count pulses per second
13	Yes	No	Yes	No	Reserved for future expansion
14	Yes	No	Yes	No	Reserved for future expansion
15	Yes	No	Yes	No	Reserved for future expansion
16	Yes	No	Yes	No	Reserved for future expansion

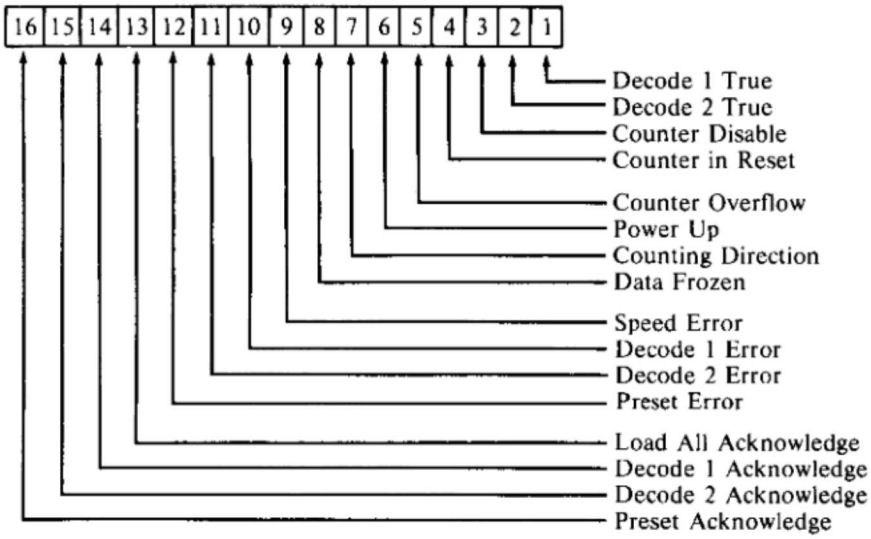
*NOTE: These registers are not necessarily the actual register addresses assigned to the HSCM. They simply indicate the function of the first to the sixteenth register assigned to the HSCM.

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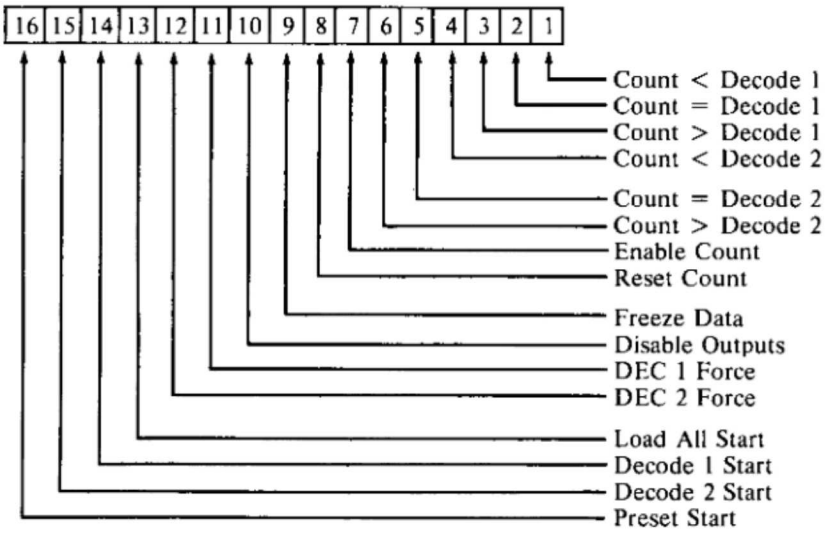
4.1.1 REGISTER DETAILS

The following table details the use of the 16 HSCM registers.

Register 1: Read Only (HSCM to CPU)



Register 2: (CPU to HSCM Control Word #1)



Register 3

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Least Significant 4 Digits of Decode 1 Set Point															

Register 4

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Most Significant 3 Digits of Decode 1 Set Point															

Register 5

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Least Significant 4 Digits of Decode 2 Set Point															

Register 6

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Most Significant 3 Digits of Decode 2 Set Point															

Register 7

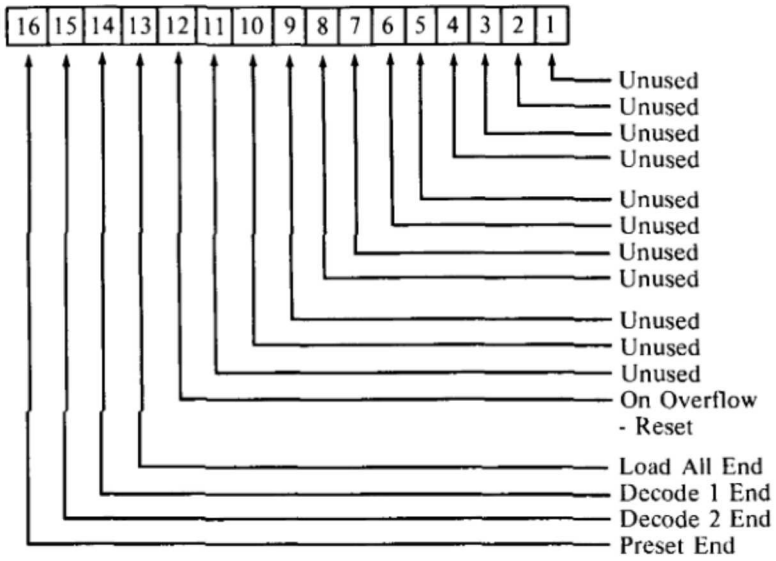
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Least Significant 4 Digits of Preset Count Value															

Register 8

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Most Signifcant 3 Digits of Preset Count Value															

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Register 9: (CPU to - HSCM Control Word #2)



Register 10

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Least Significant 4 Digits of Count Value															

Register 11

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Most Significant 3 Digits of Count															

Register 12

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Count Rate, Pulses Per Second															

Register 13

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Spare															

Register 14

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Spare															

Register 15

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Spare															

Register 16

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Spare															

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A. Register 1: Read Only (HSCM - to CPU)

This register is read by the user program and indicates the status of the High Speed Counter. The bits are defined as follows:

NOTE: Set = 1 Reset = 0

BIT	NAME	DESCRIPTION
1	Decode 1 True	When set, indicates logical conditions for Decode 1 "on" have been met, the DEC 1 output may however be off, due to disabled outputs. Initialized to 0.
2	Decode 2 True	When set, indicates logical conditions for Decode 2 "on" has been met, the DEC 2 output may however be off, due to disabled outputs. Initialized to 0.
3	Counter Disable	When set, indicates counter has been disabled by any signal or process that controls count enable. Initialized to 1.
4	Counter in Reset	When set, indicates a reset condition exists from any reset source. Initialized to 1.
5	Counter Overflow	When set, indicates counter has under or overflowed. The DEC 1 and DEC 2 outputs are forced off. Cleared by user program reset, or preset or hardware reset. Initialized to 0.
6	Power Up	Set on power-up, restart or detected error condition, indicating data is required from user ladder program. Counter is held in reset while this bit is set. This bit is reset when all three data error flags are reset (Preset Error, Decode 1 Error, Decode 2 Error)..
7	Counting Direction	If the difference between the last 2 counts read is positive, set to 1. If the difference is negative, reset to 0. If the difference is 0, no change. Initialized to 0 on power-up or reset.
8	Data Frozen	When set, indicates that the data in the output count register is not being updated. Cleared when the user ladder program clears the "FREEZE DATA" bit. NOTE: This is a display control, and does not affect the counter. Initialized to 0.
9	Speed Error	When set, indicates that the data in Register 12 (Rate) is in error. This may be caused by a rate that is too fast, counter over or under flow, counter held in reset, or any time the counter is disabled. Reset when valid speed data is placed in register 12. Initialized to 1.
10	*Decode 1 Error*	*When set, indicates that Decode 1 value sent from the user ladder program* cannot be processed. When set, Decode 1 output is forced off (HI-Z), and DATA ERROR LED is illuminated. Reset when valid Decode 1 data is received. Initialized to 1.
11	Decode 2 Error	When set, indicates that Decode 2 value sent from the user ladder program cannot be processed. When set, *Decode 2 output is forced off (HI-Z), and* DATA ERROR LED is illuminated. Reset when valid Decode 2 data is received. Initialized to 1.
12	Preset Error	When set, indicates that the preset value sent from user ladder program cannot be processed. When set, both Decodes are forced off (HI-Z), and the DATA ERROR LED is illuminated. Reset when a valid preset is received. Initialized to 1.
13	Load All ACK	When set, indicates that all double precision registers have been loaded regardless of error conditions. Data loaded is the last data written into the appropriate registers, or if no data has ever been written into the register all date registers will default to zero. Reset when the user ladder program opens Load All Start and Load All End contacts. Initialized to 0.
14	Decode 1 ACK	When set, indicates the Decode 1 input has been processed and loaded, regardless of error condition. Reset when the user ladder program opens Decode 1 start and end contacts. Initialized to 0.
15	Decode 2 ACK	When set, indicates the Decode 2 input has been processed and loaded, regardless of error condition. Reset when the user ladder program opens Decode 2 start and end contacts. Initialized to 0.
16	Preset ACK	When set, indicates a Preset input has been processed and loaded, regardless of error condition. Reset when the user ladder program opens Decode 2 start and end contacts. Initialized to 0.

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B. Register 2: *(CPU - to - HSCM CONTROL WORD #1)*

This register is written to by the user program and controls the High Speed Counter Module using the bits as defined below.

NOTE: Set = 1 Reset = 0

BIT	NAME	DESCRIPTION
1	< Decode 1	When set will enable the Count < Decode 1 comparison. Output 1 will be on whenever the Count value < Decode 1 value.
2	= Decode 1	When set will enable the Count = Decode 1 comparison. Output 1 will be on whenever the Count value = Decode 1 value.
3	> Decode 1	When set will enable the Count > Decode 1 comparison. Output 1 will be on whenever the Count value > Decode 1 value.
4	< Decode 2	When set will enable the Count < Decode 2 comparison. Output 2 will be on whenever the Count value < Decode 2 value.
5	= Decode 2	When set will enable the Count = Decode 2 comparison. Output 2 will be on whenever the Count value = Decode 2 value.
6	> Decode 2	When set will enable the Count > Decode 2 comparison. Output 2 will be on whenever the Count value > Decode 2 value.
7	Enable Count	When set the counter is enabled, unless disabled by hardware count enable, or overflow or any reset. When the enable count bit = 0, the counter does not follow input pulses, the outputs may be active depending on state of output control signals.
8	Reset Count	When bit 2-8 is first set, the counter is reset to 0,000,000. During the time the Reset Count bit is set, outputs are disabled (HI-Z), counting is disabled, speed is set to zero and the reset LED is on.
9	Freeze Data	When this bit is reset, the value in the HSCM "ACCUMULATED COUNT" register is continually updated. When the bit is set, the register value is frozen, but the counter continues to update. *This allows the user ladder program to read the accumulated count most significant* register and least significant register without the danger that one register has been updated while the other is being read.
10	Disable Outputs	When set, outputs are disabled (HI-Z).
11	Decode 1 Force	When set, the DEC 1 output is forced on. Over ridden by any module Reset.
12	Decode 2 Force	When set, the DEC 2 output is forced on. Over ridden by any module reset.
13	Load All Start	When set, indicates that a download of all double precision data from the SY/MAX Processor has started.
14	Decode 1 Start	When set, indicates that a download of Decode 1 data from the SY/MAX Processor has started.
15	Decode 2 Start	When set, indicates that a download of Decode 2 data from the SY/MAX Processor has started.
16	Preset Start	When set, indicates that a download of Preset data from the SY/MAX Processor has started.

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Additional Information About Register 2

Register 2 allows the user to have considerable control of the High Speed Counter Module. This control can be through the user ladder diagram program or by directly controlling bits with programming equipment or another SY/MAX Processor.

> Care should be taken when writing to these bits because output actuation and subsequent danger to personnel and machinery can result.

Bits 1 through 3 define the logical comparison between the 2 register Count Value and the 2 register Decode 1 value.

These three Decode 1 bits may be set separately or in pairs, or all three bits may be set.

HSCM REGISTER 2			DECODE 1 LOGIC Count Value vs. Decode 1 Value	REMARKS
Bit 3	Bit 2	Bit 1		
0	0	0		Output 1 disabled
0	0	1	<	Less than
0	1	0	=	Equal to
0	1	1	< =	Less than or equal to
1	0	0	>	Greater than
1	0	1	> < ≠	Not equal to
1	1	0	> =	Greater than or equal to
1	1	1	> = <	Output 1 on regardless of Decode 1 value

Table 4.1 - Decode 1 Logic

HSCM register 2, bits 1, 2 and 3 are reset each time the SY/MAX Processor keyswitch is placed in the HALT position. Following return of the SY/MAX Processor keyswitch to the RUN position, HSCM register 2, bits 1, 2 and 3 must be set to their intended states.

These three bits can be set by the user ladder diagram program or by direct use of SY/MAX programming equipment.

Bit 4 through 6 define the logical comparison between the 2 register Count Value and the 2 register Decode 2 value.

These three Decode 2 bits may be set separately, or in pairs or all three bits may be set.

HSCM REGISTER 2			DECODE 2 LOGIC Count Value vs. Decode 2 Value	REMARKS
Bit 6	Bit 5	Bit 4		
0	0	0		Output 2 disabled
0	0	1	<	Less than
0	1	0	=	Equal to
0	1	1	< =	Less than or equal to
1	0	0	>	Greater than
1	0	1	> < ≠	Not equal to
1	1	0	> =	Greater than or equal to
1	1	1	> = <	Output 2 on regardless of Decode 1 value

Table 4.2 - Decode 2 Logic

HSCM register 2, bits 4, 5 and 6 are reset each time the SY/MAX Processor keyswitch is placed in the HALT position. Following return of the SY/MAX Processor keyswitch to the RUN position, HSCM register 2, bits 4, 5 and 6 must be set to their intended states.

These 3 bits can be set by the user ladder diagram program or by direct use of SY/MAX programming equipment.

Register 2, bit 7, the enable count bit, must be set to allow the module to count. This bit is logically anded with the hardware count enable (CNT EN) input. Therefore, both HSCM bit 2-7 and the CNT EN input must be set in order to count.

HSCM CNT EN Input	HSCM Bit 2-7	Count Enable LED	HSCM Bit 1-3	Remarks
0	0	0	1	HSCM will not count
0	1	0	1	HSCM will not count
1	0	0	1	HSCM will not count
1	1	1	0	Counting enabled

Table 4.3 - Enable Logic

If it is necessary to have the HSCM count while the SY/MAX Processor is switched from halt to run, the rung that sets HSCM register 2, bit 7 must use a latch coil.

Register 2, bit 8, the reset count bit, will reset the counter to 0,000,000. This bit is logically or'ed with the external reset (RES) input. Therefore, either HSCM bit 2-8 or the RES input or both will reset the HSCM.

HSCM RES Input	HSCM Bit 2-8	Reset LED	HSCM Bit 1-4	Remarks
0	0	0	0	Counter not reset
0	1	1	1	Counter is reset
1	0	1	1	Counter is reset
1	1	1	1	Counter is reset

Table 4.4 - Reset Logic

It should be noted that the external RES input will load the counter either with 0,000,000 or with the last preset value loaded. DIP switch number 7 controls this function as described in Section 3.3.

Register 2, bit 10, the disable outputs bit, will disable (turn off) both the DEC 1 output and the DEC 2 output. The DECODE 1 and DECODE 2 LEDs will also turn off.

Notice this behavior is slightly different from the SY/MAX Processor keyswitch DISABLE OUTPUTS position. If HSCM outputs are disabled by use of the SY/MAX Processor keyswitch, the HSCM LED indicators will remain illuminated even though the actual DEC 1 output and DEC 2 outputs are off.

The module will continue to count while the outputs are disabled.

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Processor Keyswitch Disable	HSCM Bit 2-10	Output Disable	Remarks
0	0	0	Outputs controlled by Decode logic
0	1	1	LEDs off; outputs off
1	0	1	LEDs on; outputs off
1	1	1	LEDs off; outputs off

Table 4.5 - Disable Outputs Logic

HSCM register 2, bit 11, the Decode 1 force bit, will force on the DEC 1 output. A HSCM reset or Decode 1 data error will override the HSCM bit 2-11 force. The HSCM bit 2-11 force will override disabled outputs, and outputs turned off by module overflow.

CAUTION: Use extreme care when forcing outputs. Output actuation and danger to personnel and machinery can result.

HSCM register 2, bit 12, the Decode 2 force bit will force on the DEC 2 output. A HSCM reset or Decode 2 data error will override the HSCM bit 2-12 force. The HSCM bit 2-12 force will override disabled outputs, and outputs turned off by module overflow.

CAUTION: Use extreme care when forcing outputs. Output actuation and danger to personnel and machinery can result.

C. Register 3:

This register is the least significant 4 digit portion of the Decode 1 set point value. Values will range from +9999 to −9999.*

D. Register 4:

This register is the most significant 3 digit portion of the Decode 1 set point value. Values will range from +838 to −838*.

E. Register 5:

This register is the least significant 4 digit portion of the Decode 2 set point value. Values will range from +9999 to −9999.*

F. Register 6:

This register is the most significant 3 digit portion of the Decode 2 set point value. Values will range from +838 to −838.*

G. Register 7:

This register is the least significant 4 digit portion of the Preset count value. Values will range from +9999 to −9999.*

* The algebraic sum of the least significant and most significant register data must be within the range +8,388,607 to −8,388,608, or a "DATA ERROR" will be generated.

H. Register 8:

This register is the most significant 3 digit portion of the Preset count value. Values will range from +838 to −838.*

I. Register 9 (CPU - to - HSCM CONTROL WORD #2)

This register is written to by the user program and controls the HSCM using bits as defined below.

BIT	NAME	DESCRIPTION
1		Spare
2		Spare
3		Spare
4		Spare
5		Spare
6		Spare
7		Spare
8		Spare
9		Spare
10		Spare
11		Spare
12	On Overflow-Reset	When the user ladder program sets this bit, the counter will be automatically reset to zero when a counter over-flow or under-flow condition occurs. This is to allow continual updating of the rate register. If this bit is reset, the counter is not automatically reset on overflow, and the external hardware reset, or the user ladder program reset must be used to reset the counter.
13	Load All End	When set, indicates that new double precision data has been loaded into both decodes and the counter preset.
14	Decode 1 End	When set, indicates Decode 1 download completed.
15	Decode 2 End	When set, indicates Decode 2 download completed.
16	Preset End	When set, indicates preset download completed.

J. Register 10: Read Only

This register is the least significant 4 digit portion of the count value. Values will range from +9999 to −9999.

* The algebraic sum of the least significant and most significant register data must be within the range +8,388,607 to −8,388,608, or a "DATA ERROR" will be generated.

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K. Register 11: Read Only

This register is the most significant 3 digit portion of the count value. Values will range from +838 to −838.

L. Register 12: Read Only

This register is the rate of the count input signal in pulses per second (PPS). Values range from −32768 to +32767 PPS. Data is integrated for a time greater than 1 second, but less than 1.5 seconds. Accuracy is 3% of value ± one count. If under-flow or over-flow occurs, the "Speed Error" bit is set. The value of this register will be 32767 for an overflow, and −32766 for underflow. Any time new data is loaded into the counter, the rate program is reset.

M. Registers 13 through 16.

Spare registers for future expansion. User ladder program can read and write to these registers. The HSCM does not read, or write any data to these registers except for the status field.

4.2 Types of Programming Equipment

The following SY/MAX programmers may be used to program a SY/MAX Processor for HSCM operation.

Class 8010 Type SPR 100 Series D and later.
Class 8010 Type SPR 200 Series D and later.
Class 8010 Type SPR 201 Series D and later.
Class 8010 Type SPR 210 Series D and later.
Class 8010 Type SPR 211 Series D and later.

Class 8010 Type SPR 250 Series A and later.
Class 8010 Type SPR 260 Series A and later.

Class 8010 Type SPR-300 Series A and later.

Programming equipment must have rack addressing (or system addressing) capability.

4.3 Programming Equipment Connection

The CRT Programmer, described in Section 4.2, may be connected in either of two ways:

1. Directly to the PC
2. To the PC via the SY/NET network, if present.

Consult the appropriate programming instruction bulletin for CRT Programmer connection details.

4.4 Program Steps

The actual programming steps for rack addressing and ladder programming equipment are described in the respective instruction bulletin for each type of programming equipment.

4.5 Program Examples

The following example programs are used for initializing, changing, and reading the HSCM. All example programs assume Rack Addressing has assigned registers 101 through 116 to the high speed counter module. If the user's Rack Addressing scheme differs from the examples, the user's addressing of the HSCM must vary accordingly.

The same programs may be used regardless of which of the three count modes the HSCM has been set for.

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4.5.1 LOAD ALL START

The following four rungs *must* be executed to initialize and enable the high speed counter module.

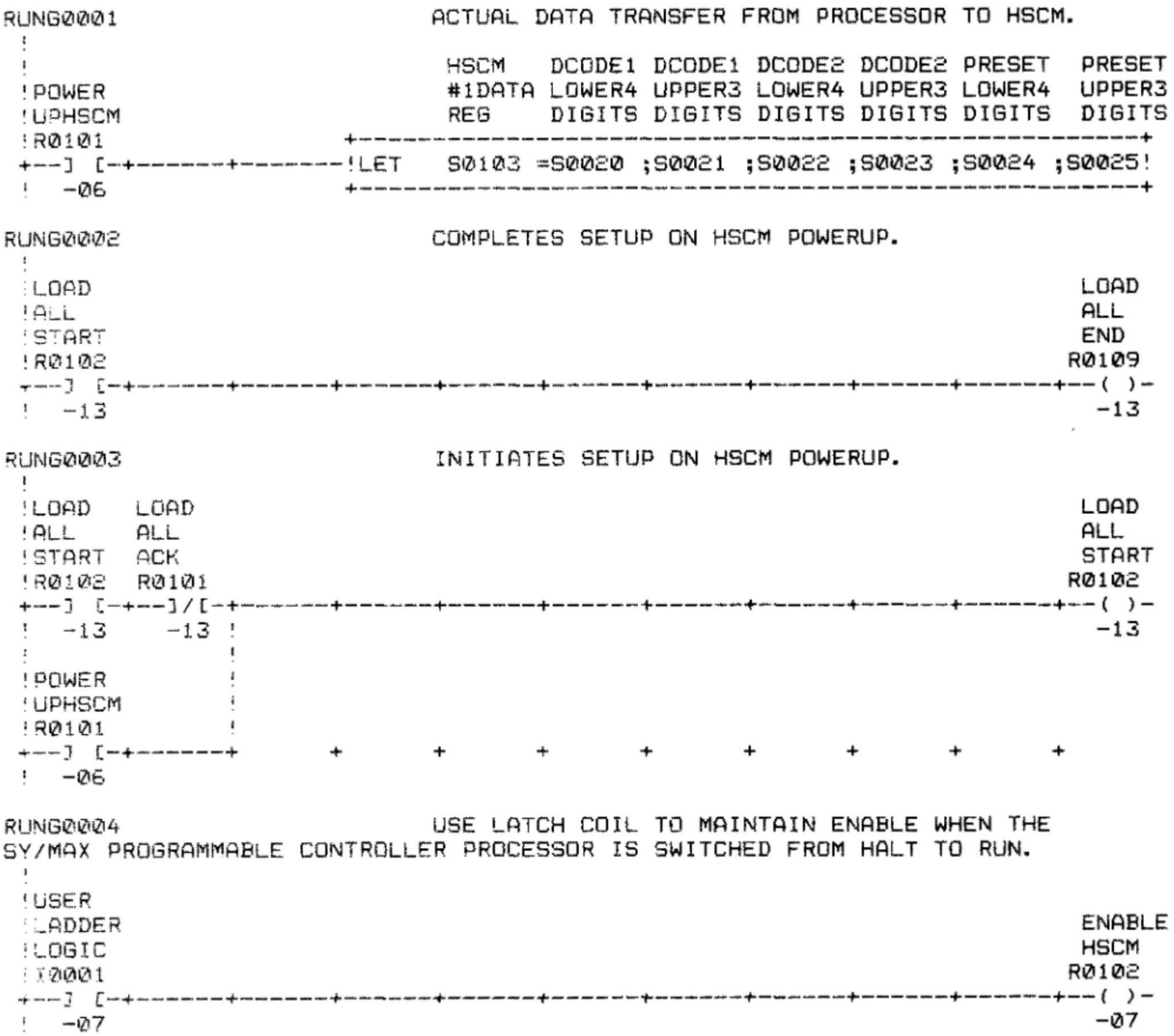


Figure 4.1 - Load All Start Rungs

For a complete explanation of these rungs, see Section 3.7, "Start-Up".

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4.5.2 CHANGING DECODE 1

The following three rungs are used to change Decode 1 data under control of the SY/MAX CPU.

IMPORTANT: Using the DATA ENTER mode of SY/MAX Programmable Controller programming equipment will not load data into the HSCM module registers. Data loaded using the DATA ENTER mode will appear to be in the registers assigned to the high speed counter module. The data is *not* transferred from the SY/MAX Processor to the HSCM until the proper loading rungs are executed.

NOTE: These rungs *must* be used to change Decode 1 values.

Rung 1 accomplishes the actual data transfer from CPU to high speed counter module.

Rung 2 indicates that the data transfer has been completed.

Rung 3 initializes the Decode 1 data change, with the closure of the user ladder contact.

If desired, the user SY/MAX program could monitor the *Decode 1 error bit in the HSCM* (HSCM register 1, bit 10) and also read back the Decode 1 value.

```
RUNG0001                        ACTUAL DATA TRANSFER FROM PROCESSOR TO HSCM.
 !
 !USER                                                    HSCM    DCODE1   DCODE1
 !LADDER                                                  #1DATA  LOWER4   UPPER3
 !LOGIC                                                   REG     DIGITS   DIGITS
 !R0002                                                +-------------------------+
 +--] [-+------+------+------+------+------+-------!LET    S0103 =S0020 ;S0021!
 !   -01                                               +-------------------------+

RUNG0002                        COMPLETES DECODE1 CHANGE SEQUENCE.
 !
 !DCODE1                                                                   DCODE1
 !START                                                                   END
 !R0102                                                                  R0109
 +--] [-+------+------+------+------+------+------+------+------+-------+--( )-
 !   -14                                                                   -14

RUNG0003                        INITIATES DECODE1 CHANGE SEQUENCE.
 !
 !DCODE1  DCODE1                                                          DCODE1
 !START   ACK                                                             START
 !R0102   R0101                                                         R0102
 +--] [-+--]/[-+------+------+------+------+------+------+------+-------+--( )-
 !   -14     -14 !                                                         -14
 !               !
 !USER           !
 !LADDER         !
 !LOGIC          !
 !R0002          !
 +--] [-+-------+       +       +       +       +       +       +       +       +
 !   -01
```

Figure 4.2 - Changing Decode 1

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4.5.3 CHANGING DECODE 2

The following three rungs are used to change Decode 2 data under control of the SY/MAX CPU.

IMPORTANT: Using the DATA ENTER mode of SY/MAX Programmable Controller programming equipment will not load data into the HSCM module registers. Data loaded using the DATA ENTER mode will appear to be in the registers assigned to the high speed counter module. The data is *not* transferred from the SY/MAX Processor to the HSCM until the proper loading rungs are executed.

NOTE: These rungs *must* be used to change Decode 2 values.

Rung 1 accomplishes the actual data transfer from the CPU to high speed counter module.

Rung 2 indicates that the data transfer has been completed.

Rung 3 initiates the Decode 2 data change, with the closure of the user ladder contact.

If desired, the user SY/MAX program could monitor the Decode 2 error bit in the HSCM (HSCM register 1, bit 11) and also read back the Decode 2 value.

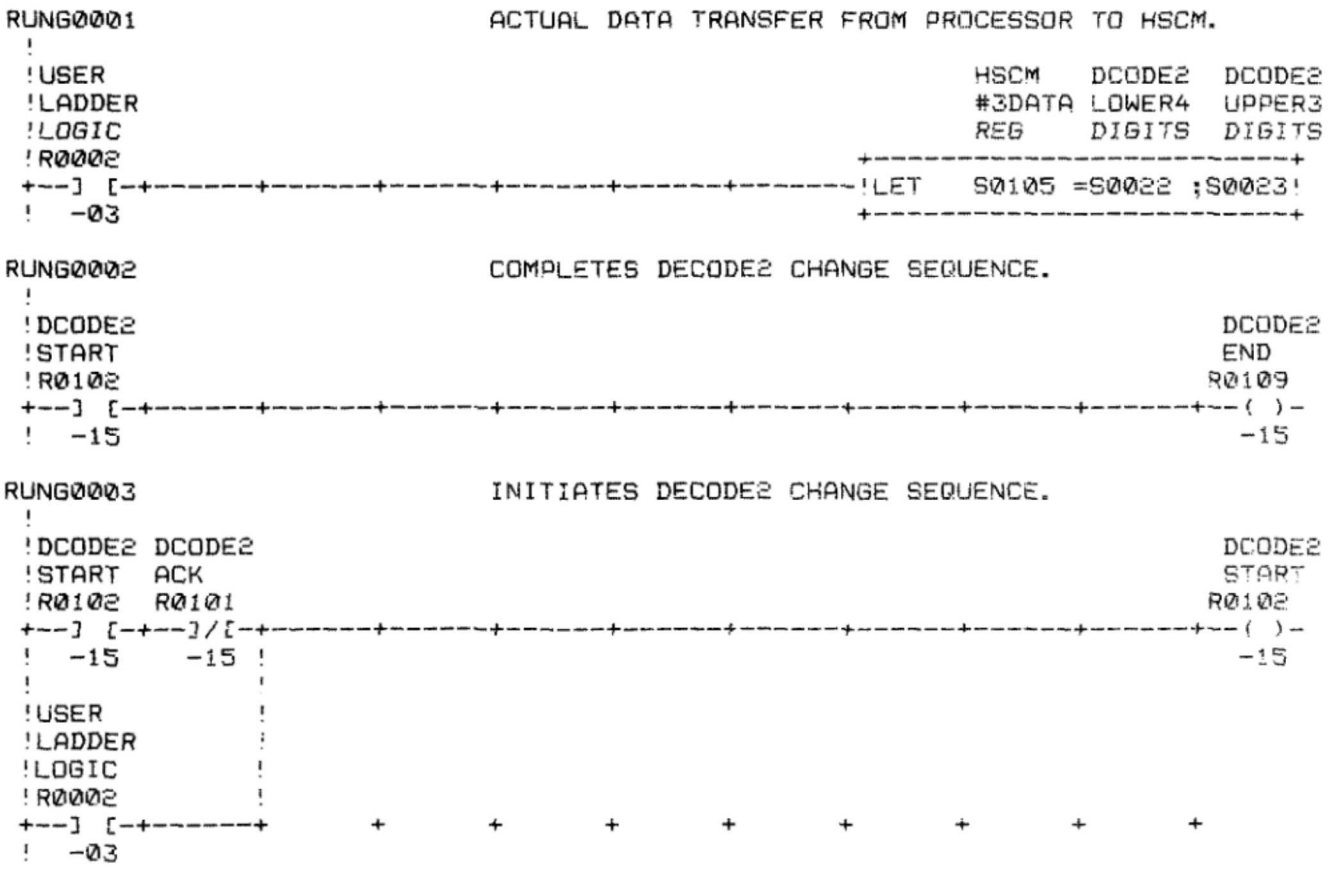


Figure 4.3 - Changing Decode 2

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4.5.4 CHANGING PRESET VALUE

The following 3 rungs are used to change Preset data under control of the SY/MAX CPU.

IMPORTANT: Using the DATA ENTER mode of SY/MAX Programmable Controller programming equipment will not load data into the HSCM module registers. Data loaded using the DATA ENTER mode will appear to be in the registers assigned to the high speed counter module. The data is *not* transferred from the SY/MAX Processor to the HSCM until the proper loading rungs are executed.

Rung 1 accomplishes the actual data transfer from the CPU to the high speed counter module.

Rung 2 indicates that the data transfer has been completed.

Rung 3 initiates the Preset data transfer with the closure of the user ladder contact.

If desired, the user SY/MAX program could monitor the Preset error bit in the HSCM (HSCM register 1, bit 12) and also read back the new Preset value.

NOTE: DIP switch 7 controls loading the preset value into the count registers whenever the module is reset by the hardware RES input.

If switch 7 is on, the preset value is loaded into the count registers following module external reset.

If switch 7 is on, the software reset, (HSCM register 2, bit 8) when set will load 0000 into both count registers.

If switch 7 is off, zero is loaded into the count registers following module reset from either source regardless of the preset value.

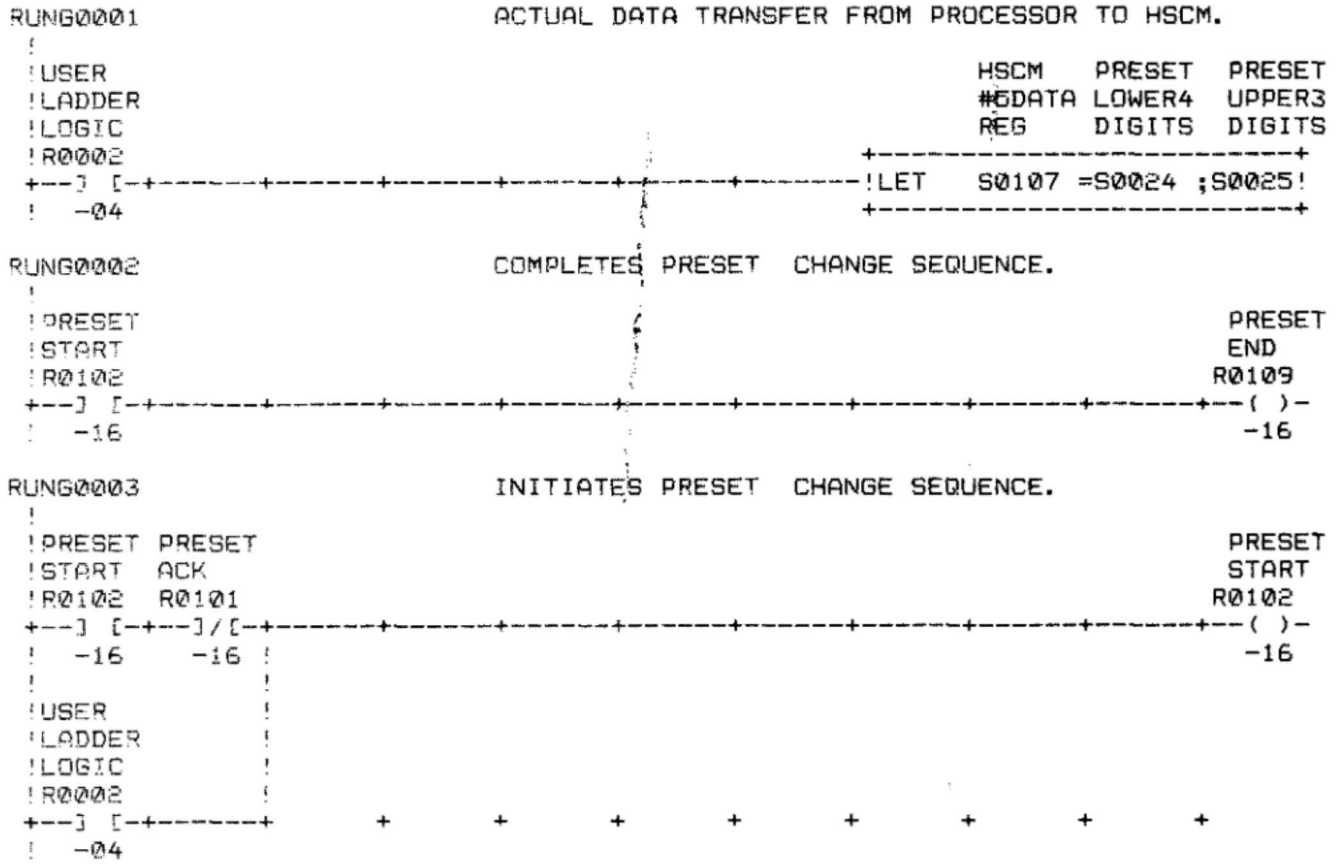


Figure 4.4 - Changing Preset Value

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4.5.5 READING COUNT VALUE

It may be desired to program the SY/MAX Processor to read the count value. However, it should be realized that the SY/MAX Processor cannot read the count and activate an output with great speed or precision.

It may be appropriate to have the SY/MAX Processor read the count if it is desired to display the count, write the count value to another SY/MAX device, or monitor the count.

The following technique is suitable for reading a slow or halted count value.

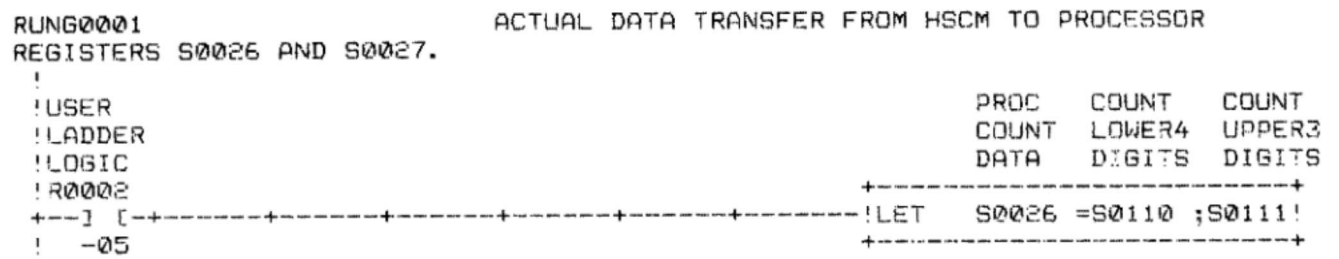


Figure 4.5 - Reading Count Value

This is a simple data transfer from the HSCM count registers to SY/MAX Processor registers.

In some cases, it may be desired to "freeze" the HSCM count data before it is read by the processor.

The following 3 rungs are used to freeze the count data.

NOTE: The high speed counter module continues to count and update its own internal registers even though data appears frozen to the SY/MAX CPU.

Rung 1 indicates that data has been frozen.

Rung 2 is the actual count data transfer from HSCM to SY/MAX CPU.

Rung 3 is the command rung from the SY/MAX CPU to HSCM to freeze data.

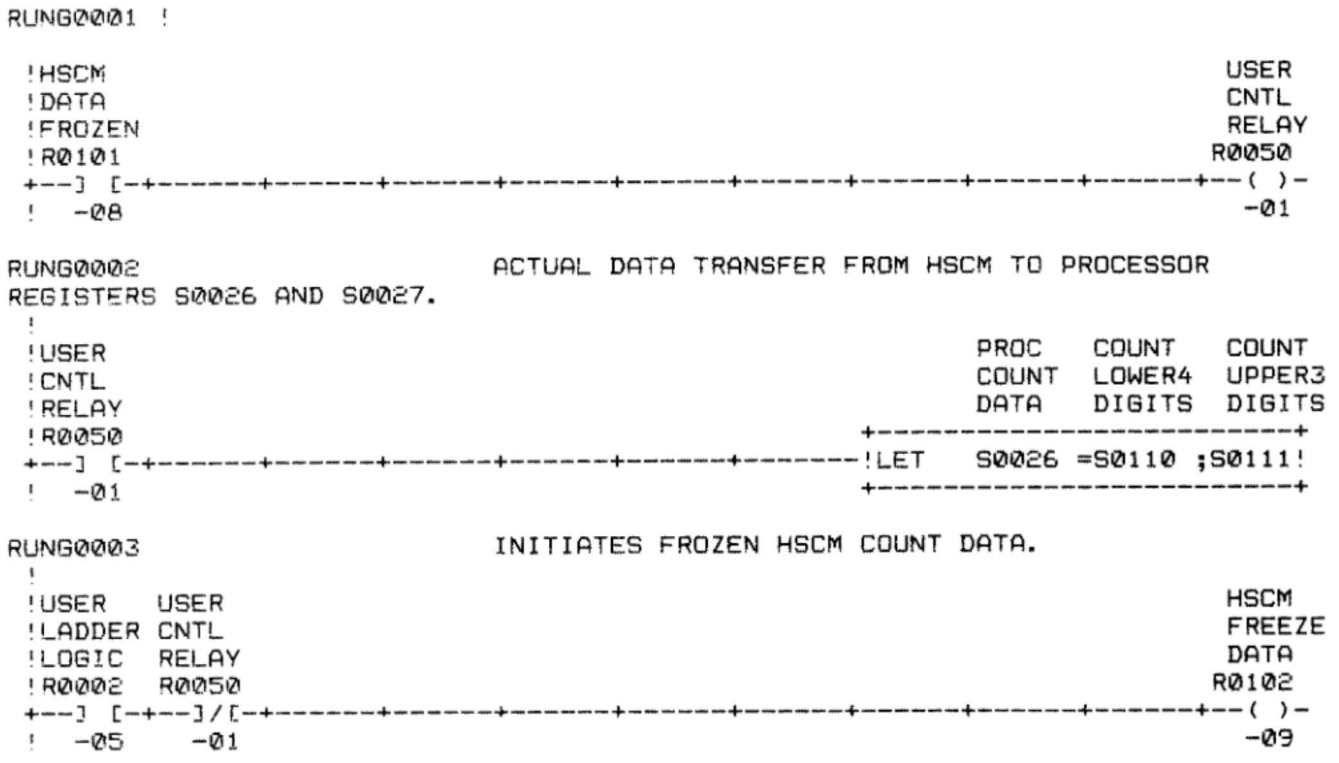


Figure 4.6 - Freezing Count Data

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4.5.6 READING SPEED

The SY/MAX Processor can be programmed to read the HSCM speed register.

A one rung program is used to read speed. Speed data is in units of Hertz.

One SY/MAX register is used to store the speed data. If HSCM register 1 bit 9 is set, the data in the speed register should be considered erroneous.

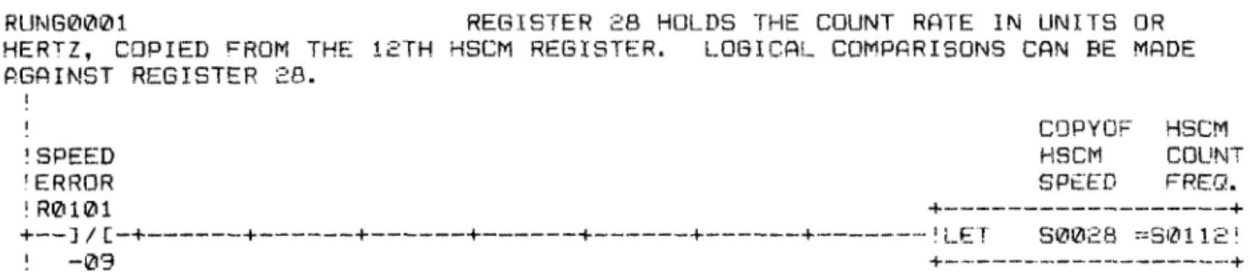


Figure 4.7 - Reading Speed

5.0 APPLICATIONS CONSIDERATIONS

5.1 General

The high speed counter module is capable of versatile high speed counting. It must be realized that electrical behavior at high switching speeds (which implies high frequencies) is not necessarily the same electrical behavior as at low switching speeds and frequencies.

For example, in a 120 VAC 60Hz or a 120 VDC system it is reasonable to assume that after contacts close, a potential difference appears almost instantaneously at the wire ends attached to the switch load. Typically, no delay is assumed from the time when limit switch contacts close (or open) and potential is measured at the ends of the wires attached to the load energized by the limit switch.

This instantaneous response cannot be assumed at higher frequencies, especially since most high speed signals operate at lower voltages. (5-24 volts typical.) All wire pairs possess capacitance, and it takes a finite time to charge or discharge the capacitance of these wires. If the time required to charge or discharge the wires is greater than 1/F, the count signals may never appear at the wire ends, the counter module inputs.

In order to minimize capacitive effects, input signal wires should be:

1. Low capacitance
2. As short as possible

Recommended input signal wires should be shielded, twisted pair such as Belden 9184. Wire length should be less than 50 feet, although high frequencies may require shorter lengths.

After the Decode 1 or Decode 2 value is reached by the counter, it will take 20 micro seconds to turn the DEC 1 and DEC 2 output MOSFET on or off. Therefore, at input frequencies greater than 50 KHz, an output will not turn on if the decode comparison is for equality.

All outputs are fused for 250mA (1/4A), therefore, all load resistances should be greater than:

$$R_{\text{load min.}} = V/0.250 = (4)(V). \text{ (Ohms)} \qquad \text{Equation 5.1}$$

At 5 VDC, $R_{\text{load min}} = (4)(5) = 20$ ohms
At 24 VDC, $R_{\text{load min}} = (4)(24) = 96$ ohms

Fuses will blow with lower load resistances.

Outputs are protected against inductive loads. Diodes are provided on each output to allow a discharge path for the inductors. Large inductive loads may require additional discharge paths.

The users machine must be designed such that the actual machine activators will respond as desired when receiving a Decode output signal from the HSCM. For example, solenoids must be fast enough to respond during the DEC 1 output or DEC 2 output "on time".

User inputs should preferably not be from mechanical contacts. These mechanical contacts usually bounce upon closing. The high speed counter will count these contact bounces, leading to erroneous, unintended count values.

All inputs have DIP switch selectable low-pass filters, but these limit maximum count frequency to 300 Hz. Use of the low pass filters largely defeats the purpose of the HSCM. For this reason, it is preferable to use open-collector type transistor inputs to the HSCM. Typical inputs are metal sensing proximity switches and photo sensitive limit switches.

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5.2 Quadrature Inputs

Quadrature incremental encoders are available from a number of sources such as:

MANUFACTURER	ADDRESS	PRODUCT LINE
BEI Electronics Inc.	7230 Hollister Avenue Goleta, CA 93117-2891	Type H25
Datametrics	340 Fordham Road Wilmington, MA 01887	TRU-Mite®
Dynapar	1675 Delany Road Gurnee, IL 60031	Series 40 Series 60
Teledyne Gurley	514 Fulton Street Troy, NY 12181-0088	Series 825

The listed suppliers can provide a wide variety of encoders. The choice of a specific encoder is influenced by the requirements of each encoder application.

If count doubling or quadrupling is desired, external circuitry must be added by the user.

5.3 Count - Up/Down

Typical inputs to the HSCM for count and up/down direction operation are photo switches, metal detecting proximity switches, or incremental encoders.

Square D Company Class 9007 Type PS DC operating proximity switches may be used as the count and the up/down direction inputs. Operation of these switches is limited to 200 Hz and lower.

Mechanical limit switches should not be used due to contact bounce, which may lead to erroneous counts.

5.4 Count Up - Count Down

Typical inputs to the HSCM for count up - count down operation are photo switches, metal detecting proximity switches, or incremental encoders.

Square D Company Class 9007 Type PS DC operating proximity switches may be used as the count up and the count down inputs. Operation of these switches is limited to 200 Hz and lower.

Mechanical limit switches should not be used due to contact bounce, which may lead to erroneous counts.

Anti-coincidence circuitry is provided on the HSCM to ensure a proper count, even if both count up and count down signals occur simultaneously (in phase). In this case, the count will be correct, it will be both incremented and decremented for no net change.

6.0 TROUBLESHOOTING

6.1 Diagnostic Lights

During normal operation, the green COUNT ENABLE light will be on if count is enabled. DECODE 1 and DECODE 2 will be in any of 4 possible states, depending on the decode logic and the count value.

The DATA ERROR light, if illuminated, indicates invalid data has been received from the PC. This may have been caused by an improper user ladder program.

The MODULE ERROR LED indicates the HSCM is inoperable. This may be due to a module hardware error.

If the SY/MAX CPU is unprogrammed or does not contain a suitable program, the RESET and DATA ERROR lights of the high speed counter module will be illuminated.

See Section 3.7 for the required ladder diagram program.

6.2 With Programming Equipment

If it is necessary to use programming equipment for examining the ladder diagram or for monitoring registers, verify that the programmer is suitable as described in Section 4.2.

Examine the ladder diagram program to verify the proper program is present to allow the HSCM to operate. The necessary ladder program, as described in Section 3.7.1 must be present to allow the high speed counter module to operate.

With the Class 8010 CRT in the monitor mode (SPR 2XX types) or data mode (SPR 3XX types), display the 16 SY/MAX registers which have been assigned to the high speed counter module.

With the CRT in the monitor mode (SPR 2XX types) or data mode (SPR 3XX types), display the 16 SY/MAX registers which have been assigned to the high speed counter module.

Verify that the software enable bit, HSCM register 2 bit 7, is set and that the software reset bit, HSCM register 2 bit 8 is reset.

If a high speed counter module error has occurred (MODULE ERROR LED illuminated), the HSCM will contain an error code that can be read by the programming equipment or by the SY/MAX Processor. These codes will appear in both the data and the status fields, in both the high byte and the low byte.

The error codes are as follows:

Code	Condition
60H	PROM Checksum Error
61H	RAM Error
62H	Count or Decode Error
40H	General Fault

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If desired, the user's ladder diagram program can be designed to recognize these error codes. The SY/MAX Processor can then initiate control action based upon the error codes.

6.2.1 USE OF THE SELF-TEST CAPABILITY

The high speed counter module has additional self-test software built in. To run this self-test, a jumper must be removed from the HSCM circuit board. The HSCM must be removed from the rack to provide access to the jumper.

NOTE: The HSCM will not operate normally with the test jumper removed.

The test jumper is located on the component side of the printed circuit board, above the DIP switches.

All user wiring must be removed from the module and special test wiring installed.

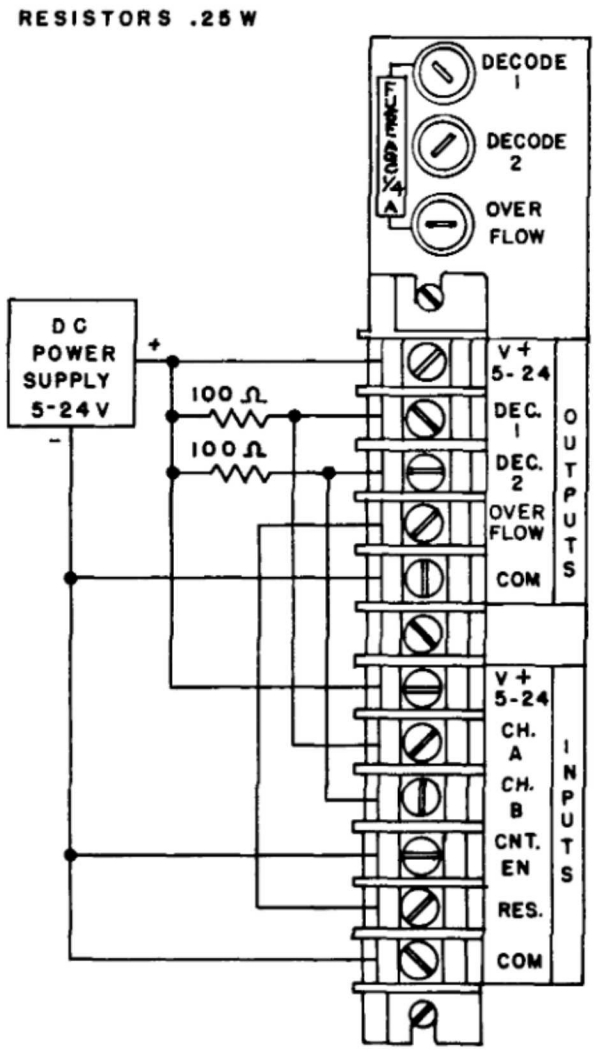


Figure 6.1 - Special Test Wiring

If an error is detected, and the self-test jumper is out, the DATA ERROR LED flashes in a particular sequence. The sequence of flashes is as follows:

1) A synch flash.
2) A number of flashes as given in the table below.
3) Approximately 1 second delay with LED off.
4) Repeat at step 1.

NUMBER OF FLASHES	
	WATCHDOG TEST
01	WATCHDOG WILL NOT GO LOW
02	WATCHDOG DID NOT DISABLE COUNTER
03	WATCHDOG DID NOT TURN RESET ON
04	WATCHDOG DID NOT CAUSE RESET
05	WATCHDOG WILL NOT PULSE
06	WATCHDOG PULSE TOO SHORT
	RAM TEST
07	RAM BAD
	WATCHDOG TIMED OUT
08	WATCHDOG DETECTED IN TIMED OUT MODE
09	SELF TEST, COUNT NOT ENABLED, (PERHAPS NO USER VCC, NO JUMPER/ HARDWARE FAULT)
	COUNTER VALUE TEST
10	LSB OF COUNTER IN ERROR
11	NSB OF COUNTER IN ERROR
12	MSB OF COUNTER IN ERROR
	EQUAL TEST
13	DEC1 NOT SHOWING =
14	DEC2 NOT SHOWING =
15	DEC1 SHOWING < OR >
16	DEC2 SHOWING < OR >
	GREATER THAN TEST
17	DEC1 NOT SHOWING >
18	DEC2 NOT SHOWING >
19	DEC1 SHOWING < OR =
20	DEC2 SHOWING < OR =
	LESS THAN TEST
21	DEC1 NOT SHOWING <
22	DEC2 NOT SHOWING <
23	DEC1 SHOWING = OR >
24	DEC2 SHOWING = OR >
	NUMBER CONVERSION TESTS
25	FAILED NUMBER CONVERSION
	CLR FOUND HIGH DURING TEST
26	WHEN PULSING OUTPUT, CLR WAS HIGH
27	NOT USED
28	NOT USED
	WARM RAM TEST FAIL
29	FAILED "CLR" RAM TEST
	COUNT DIRECTION ERROR
30	COUNT DIRECTION IN ERROR

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NUMBER OF FLASHES	
	RUN TIME TEST
31	FAILED BACKGROUND RAM TEST
	OVERFLOW AND RESET INPUT TEST
32	RESET INTERRUPT FLAG SET, SHOULD BE CLEAR
33	OVERFLOW FLAG DID NOT SET
34	CNT IS ENABLED WITH OVERFLOW ON
35	RESET INTERRUPT DID NOT HAPPEN
36	NO UNDERFLOW FLAG WHEN UNDERFLOW FORCED
37	OVERFLOW NOT CLEARED WHEN MSB LOADED

6.3 With DVM

If the user ladder program is correct, a Digital Volt Meter (DVM) may be used to check the high speed counter module I/O terminals.

Verify that 5 to 24 VDC from the external power supplies is present at the module terminals.

6.4 With Oscilloscope

If the user ladder program is correct, and the module hardware can be shown to work through forcing, it may be necessary to examine the incoming count signal. A dual trace oscilloscope will allow both A and B inputs to be examined simultaneously.

Measure between common and the input terminals. Verify that the signal is present, and that voltage and frequency are within high speed counter module specifications. In particular, check the oscilloscope display for any extra undesirable signals from noise sources or from contact bounce of mechanical contact inputs.

If noise is found to exist on the input signal wires, the noise source should be identified. Noise coupling through the field wiring is a potential source of noise at the high speed counter module inputs.

Coupled noise can be reduced by eliminating the noise source, re-routing the input signal wire, installing additional shielding around the input leads or by a combination of these methods.

6.5 If Module Isn't Working

If the ladder program, the external signals and power are proper, it may be necessary to replace the high speed counter module.

Remove all power from the Class 8030 Type PS Power Supply connected to the rack in which the high speed counter module is located. Remove the suspect module and replace with the new high speed counter module. Refer to Section 3.1.2 "Replacing an Existing Module".

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7.0 THEORY OF OPERATION

7.1 Block Diagram

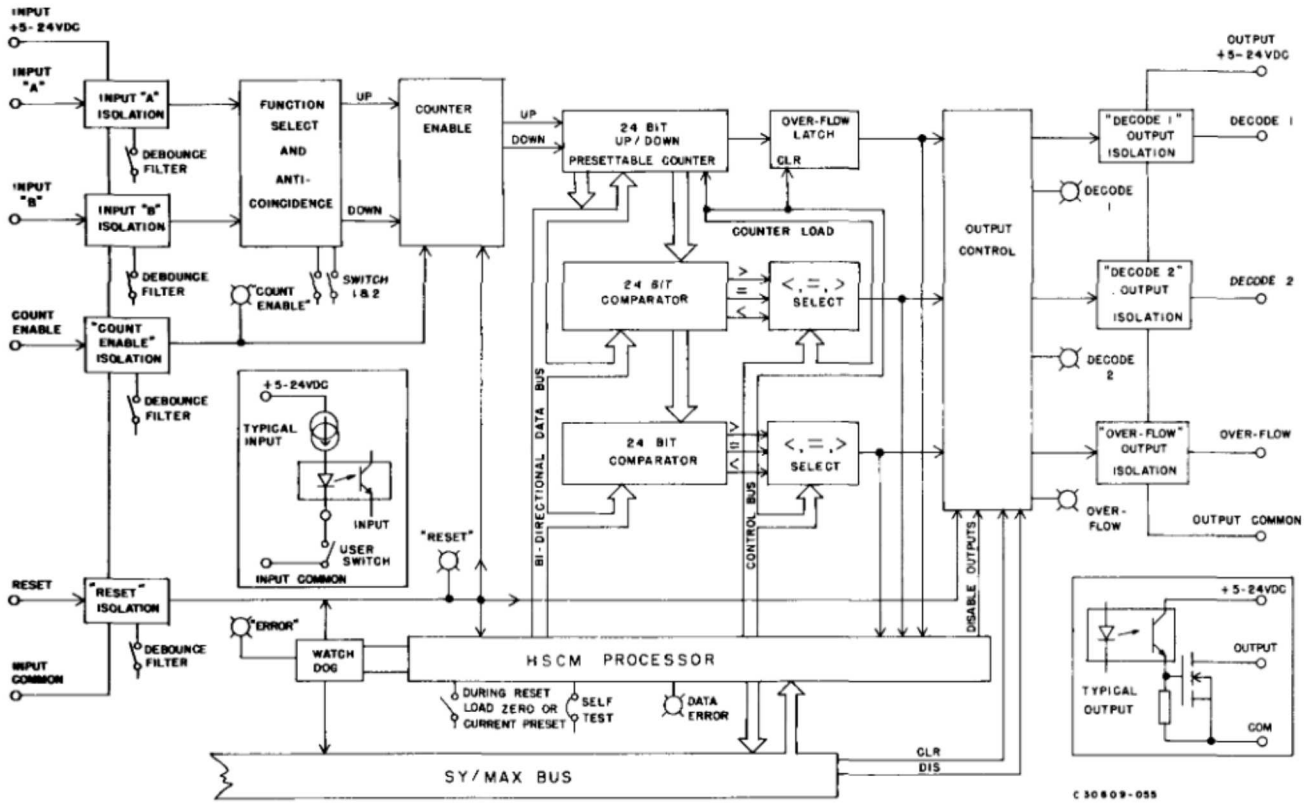


Figure 7.1 - HSCM Block Diagram

Figure 7.1 "HSCM Block Diagram" shows the major features of the HSCM. Inputs are at the left of the diagram, counting and logic in the middle, and outputs at the right. The microprocessor and SY/MAX Bus are shown towards the bottom of the diagram.

7.2 Detailed Description of Operation

Input signals are used to switch a current source, on or off. Each input current source then controls an optical isolator. See Inset A of Figure 7.1 for typical input detail. Debounce filters can be enabled at the optical isolator output.

Count signals are next routed to function select and counter enable circuitry. Count enable is controlled by the count enable input and by the reset input circuitry.

If the counter is enabled and not reset, count signals are fed to the 24 bit up/down presettable counter. This counter is a hardware counter made of 74LS193 integrated circuits.

The count value is compared against the established decodes by two 24 bit comparators. Comparator outputs greater than, equal to and less than are used to drive the output decode selectors. Any combination of greater than, equal to, and less than may be enabled by the user program.

Decode 1, Decode 2 and Overflow drive the output control circuit. The output control circuit drives the output optical isolators. Each optical isolator switches a MOSFET which controls the "external field" loads connected to the output terminals by the user. See Inset B of Figure 7.1 for typical output circuitry detail.

The HSCM processor, an Intel 8031, allows the HSCM to communicate with the SY/MAX Bus. Because counting and decoding is done in hardware, the 8031 operates almost independently of the count. Major functions performed by the 8031 are reading the count, loading decode values and decode types. The 8031 also performs the divide function for the HSCM rate register. Additionally, the Intel 8031 performs module diagnostics and self test.

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GLOSSARY

DEC 1	The first of 2 programmable outputs on the high speed counter module.
DEC 2	The second of 2 programmable outputs on the high speed counter module.
DIP	Dual Inline Package. A commonly used method for packaging integrated circuits.
DIP SWITCH	Small switches mounted in a dual inline package. Commonly used for user-selectable options on electronic equipment.
Hertz	Units of frequency, formerly cycles-per-second (CPS)
HI-Z	High Impedance
HSCM	High Speed Counter Module
LED	Light Emitting Diode
LO-Z	Low Impedance
PRESET	The value that can be loaded into the high speed counter module's 10th and 11th registers. This allows counting to begin at any user determined value between +8,388,607 and -8,388,608.

Quadrature Encoder — An incremental encoder with a 2 channel output of 2 square waves separated in phase by 90°

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