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FS725 Rubidium Frequency Standard
Operation and Service Manual



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Addendum: PRS10 Manual

Specifications

Standard outputs	Two 10 MHz sine waves, one 5 MHz sine wave, one 1 pps with 10 µs width
Optional outputs	Up to 3 distribution modules, each with four 10 MHz, one 5 MHz, and one 1 pps
1 pps output	2.5 V into 50 Ω , 5 V into high impedance, 10 µs pulse width
Sine outputs	0.5 V_{rms}, ±10% (1.41 V_{pp} or +7 dBm)
Phase noise (5 MHz & 10 MHz)	<-130 dBc/Hz @ 10 Hz <-140 dBc/Hz @ 100 Hz <-150 dBc/Hz @ 1 kHz <-155 dBc/Hz @ 10 kHz
Spurious	<-100 dBc (within 100 kHz)
Harmonics	<-60 dBc
Return loss	>25 dB @ 10 MHz
Accuracy	$\pm 5 \times 10^{-11}$
Aging	$<5 \times 10^{-11}$ (monthly, after 1st month) $<5 \times 10^{-10}$ (yearly, after first year)
Allan variance	$<2 \times 10^{-11}$ (1 s) $<1 \times 10^{-11}$ (10 s) $<2 \times 10^{-12}$ (100 s)
Holdover	72 hour Stratum 1 (1×10^{-11})
Frequency retrace	$\pm 5 \times 10^{-11}$ (72 hrs off then 72 hrs on)
Settability	$<5 \times 10^{-12}$
Trim range	$\pm 2 \times 10^{-9}$ (pot or by 0-5 VDC input) ±0.5 ppm (via RS-232)
Warm-up time	<6 minutes (time to lock) <7 minutes (time to 1×10^{-9})

Front Panel Indicators

Power "On" when AC power is applied

Locked "On" when frequency is locked to rubidium hyperfine transition

1 PPS input Blinks with each 1 pps reference input applied to rear panel

1 PPS sync "On" when 1 pps output is synchronized to within ±1µs of 1 pps input

Receive Blinks "on" when RS-232 characters are received by FS725

Send Blinks "on" when RS-232 characters are sent by FS725

Rear Panel Connections

FREQ ADJ 0-5 VDC to adjust frequency by +/- 0.002 ppm (normally unconnected)

1 PPS Input One 100 kΩ input. Requires CMOS level pulses (0-5 VDC.) If an external 1 pps input is applied, lock is maintained between the 1 pps input and 1 pps output with computer adjustable natural time constant from 8 minutes to 18 hours. (Default is 2.25 hours.)

10 MHz Out Two isolated 50 Ω 10 MHz sine outputs

5 MHz Out One 50 Ω 5 MHz sine output

1 PPS Out One 50 Ω pulse output.

Optional Each option board provides four 10 MHz, one 5 MHz and one 1 pps outputs. Up to 3 boards may be installed at the time of order.

Relays Max current, 3A. SPDT, normally-open or normally-closed. May be wired in parallel with other relays to "wire-or" a single alarm.

Rb Lock Relay status matches front panel "Locked" LED.

1 PPS Relay status matches front panel "1 pps sync" LED

RS-232 9 pin connector configured as DCE, 9600 baud. A Windows® Control program is provided.

Environmental

Operating temperature	+10 °C to +40 °C
Storage temperature	-55 °C to +85 °C
Temperature stability	$\Delta f/f <= \pm 1 \times 10^{-10}$ (+10 °C to +40 °C)
Magnetic field	$\Delta f/f < \pm 2 \times 10^{-10}$ for 1 Gauss field reversal
Relative humidity	95% (non-condensing)

General

AC Power	90 to 132 VAC or 175 to 264 VAC, 47 to 63 Hz, 50 VA
Dimensions	8.5” x 3.5” x 13” (WHL)
Weight	9 lbs
Warranty	One year parts and labor on materials and workmanship

Overview

The FS725 is a stand-alone 10 MHz frequency standard with an estimated 20-year aging of less than 0.005 ppm. The unit integrates an SRS PRS10 Rubidium Frequency Standard, a universal AC input power supply, and distribution amplifiers in a half-width 2U chassis (3.5" height). The unit's low aging eliminates the need for an external frequency reference in many applications; however units can phase-lock to an external 1 pps GPS signal for ageless performance or periodic calibration as required.

The FS725 provides exceptionally low phase noise 5 MHz & 10 MHz sine outputs as well as a low-jitter 1 pps output. The 10 MHz outputs have a phase noise of <-130 dBc/Hz at 10Hz offset from carrier, dropping to <–155 dBc/Hz at 10 kHz offset. The Allan Variance is less than $2x10^{-11}$ at one second and 2×10^{-12} at 100 seconds. The 1 PPS TTL output has less than 1ns of jitter and may be set with 1ns resolution.

The standard FS725 has two 10 MHz outputs, one 5 MHz output, and one 1 PPS output. Up to three distribution modules can be added to the unit. Each module provides six additional outputs: four 10 MHz outputs, one 5 MHz output, and one 1 PPS output. With three modules installed the FS725 will provide fourteen 10 MHz outputs, four 5 MHz outputs, and four 1 PPS outputs, each with the same low phase noise, harmonic distortion and jitter.

An RS-232 interface allows for direct communication with the PRS10 Rubidium frequency standard. This interface is used for frequency calibration, 1 PPS timing, status determination, and to assist in the evaluation of the PRS10 rubidium frequency standard as a component for OEM applications. A Windows application program is provided.

FS725 will time-tag the rising edge of a user supplied 1 pps input, which usually comes from a GPS receiver. The unit can phase-lock to this input to cancel long-term aging. The time-tag results may be read back via the RS-232 interface. Timing is referenced to the leading edge of the 1 pps output pulse. The 1 pps output pulse will be moved into coincidence with the user supplied 1 pps input after 256 input pulses. Thereafter, the PRS10 will adjust its frequency to maintain the phase lock between the 1 pps input and the 1 pps output. The phase lock algorithm uses an adjustable natural time constant (from a 8 minutes to 18 hours) which may be adjusted via the RS-232.

Two alarm relays are provided to signal the status of the PRS10 rubidium frequency standard and its synchronization to an external 1 pps input. Both relays are SPDT providing both normally-open and normally-closed operation. Several thousand PRS10s have been operating in various OEM applications with a demonstrated MTBF several hundred thousand hours and so a malfunction of the PRS10 is very unlikely. In the event of a failure the alarm relay will activate but the 10 MHz output will be provided by the unit's ovenized SC-cut 10 MHz crystal oscillator with typical aging of 0.05 ppm/year.

The FS725 will find application as an autonomous frequency standard in virtually any calibration and R&D laboratories where precision time or frequency measurements are made, or in any other facility requiring an accurate frequency standard. The low cost of the unit,

together with its extremely low aging, will allow customers to deploy precision frequency references throughout a facility without the need to install cables or antennas.

Operational Description

Power

The unit is powered from the AC mains. The universal input power supply accommodates any voltage in the ranges 90 to 132VAC or 175 to 264VAC with a frequency in the range of 47 to 63Hz. There is no power switch as the unit should be left "on" all the time. The rubidium frequency standard is operating and outputs are available whenever AC power is applied.

Warm-up

The front panel "POWER" LED should be on whenever power is applied to the unit. The front panel "LOCKED" LED should come on within six minutes after power is applied if the unit is started from room temperature. Warm-up and locking will take longer if the unit is started from a lower temperature. Operation of the "LOCKED" LED corresponds to the state of the rear panel "RB LOCK" alarm relay. When power is first applied, the "LOCKED" LED will be off and the "RB LOCKED" relay will be in the "alarm" position. Once the unit warms up and locks its crystal oscillator to the rubidium physics package, the "LOCKED" LED will turn on and the "RB LOCK" relay will move to the non-alarm state.

The output frequency will be about 200 ppm below nominal when power is first applied to a cold unit. The frequency will gradually converge on 10 MHz as the unit warms up. After about 4 minutes (typically) the unit will reach operating temperature and lock the crystal oscillator to the rubidium hyperfine transition. Within seven minutes, the unit will be locked to with 0.001ppm of 10 MHz.

Connection to other instruments

All of the outputs on the rear of the FS725 have a source impedance of 50 Ω and are intended to drive 50 Ω loads. Since the outputs have a source impedance of 50 Ω, termination into a 50 Ω load is not critical in most applications. Generally, the amplitude will approximately double if the output is not terminated into a 50 Ω load. Properly terminating into a 50 Ω load will reduce channel-to-channel cross-talk and will reduce the probably of multiple triggering on the 1 pps output.

If a single 5 MHz or 10 MHz output is "daisy-chained" to several instruments it will be important that all of the instruments have a high-impedance input (>1 kΩ) and that a 50 Ω terminator be placed at the far end of the line. Generally, it is better practice to use a separate output to each instrument to avoid cross-talk and amplitude variations due to uncertain loading and standing waves along the line.

Many instruments which generate or measure precise frequencies or time-intervals have a 10 MHz input, usually located on the rear of the instrument. Most of these instruments accept a sine input with the amplitude provided by the FS725. Sometimes a rear panel switch or front panel configuration menu is required to "tell" the instrument to use the 10 MHz input as a

reference instead of using the instrument's own time base. Improved accuracy can be achieved by using the FS725 as an external time base to all of the instruments in a particular laboratory. In addition, all errors associated with the calibration of an individual instrument's time base are eliminated.

Connection to SRS Instruments

SR620 Time Interval Counter. This instrument is "told" to use the external 10 MHz input via the front panel CONFIG menu. To configure the SR620 to use an external time base press the SEL key in the CONFIG section once to display CONFIG menus, then press SEL one more time to select the "cAL" menu, which will flash when selected. Press the SET key twice to access the "cLoc SourcE" submenu. Press the arrow keys immediately to the left of the CONFIG menu (in the SCOPE AND CHART section) to select "rEAr", which is the rear panel time base input. Press the SET key in the CONFIG section once more to verify the expected time base frequency (5 MHz or 10 MHz). Press the arrow keys to select the frequency of the time base which you will be using.

DS345 Synthesized Function Generator.

The DS345 automatically detects the application of an external time base and phase locks to it. After applying a 5 MHz or 10 MHz sine to the rear panel time base input, a front panel indicator will turn "on".

DG535 Digital Delay Generator

A rear panel switch is used to specify an external 10 MHz time base input. Some revisions of the DG535 required a 10 MHz square wave input, and may not operate properly with the 10 MHz sine wave output from the FS725. The user should verify proper operation of the DG535 when locked to an external time base with an SR620 Time Interval Counter.

Direct Frequency Control of the FS725

The frequency of the rubidium hyperfine transition is adjusted via a small magnetic field in the physics package. The magnitude of the magnetic field is set by the microcontroller in the PRS10. The frequency offset is quadratic in the magnetic field but firmware in the PRS10 linearizes the adjustment. The microcontroller reads the position of a calibration potentiometer (accessible on the side panel of the instrument), or responds to software commands via the RS-232, to set the magnetic field which controls the operating frequency.

The operating frequency may be directly controlled over the range of ±0.002ppm in four ways:

1. By the adjustment of a 15 turn potentiometer accessible on the side of the instrument. Turning the potentiometer clockwise will increase the frequency by about 0.0025Hz per turn. The adjustment procedure is detailed in the calibration section.

2. By applying a voltage in the range of 0 to 5 VDC to the rear panel FREQ ADJ BNC. The nominal voltage is 2.50 VDC. The voltage on this BNC corresponds to the position of the 15 turn potentiometer described above. The voltage may be overridden by a user input. The tuning rate at 10 MHz is 0.008 Hz/volt. The input/source impedance is between 10 kΩ and 35 kΩ depending on the potentiometer position.

3. By software command via the RS-232. The SF (Set Frequency) parameter allows the user to set the frequency with a resolution of $1:10^{-12}$. The parameter has a range of ±2000 which allows frequency control over the range of ±0.002 ppm. The position of the frequency adjustment potentiometer is used to set the SF parameter until a SF command is received via the RS-232 or until phase locking to an external source is activated by the application of 1 pps inputs to the rear panel BNC. Control is returned to the potentiometer when the power is cycled. Details are available in the PRS10 operation and service manual.

4. By software calibration via the MO (Magnetic Offset) parameter. The MO parameter is summed in quadrature with the SF parameter to control the frequency of operation. At the factory, the MO parameter is calibrated so that the unit will operate at 10 MHz with an SF value of 0. The SF parameter is set by either the potentiometer or via RS-232 commands, and will be zero when the potentiometer is centered. The MO parameter may be adjusted and retained in the PRS10 EEPROM, allowing frequency calibration via the RS-232. Details are available in the PRS10 operation and service manual.

Using an External 1 pps Reference.

The FS725 has sufficient accuracy (0.005 ppm estimated over 20 years) that most users will not need to use an external timing reference. However, for critical applications requiring a frequency accuracy which is better than 1×10^{-9}, or to provide continuous traceablity, the FS725 may be locked to an external 1 pps reference.

When a precise 1 pps signal is applied to the 1 pps input on the rear panel of the FS725, the rubidium frequency standard will phase-lock to the signal. The 1 pps signal usually comes from a GPS receiver which can have a long-term accuracy of a few parts in 10^{12}. Because the stability of the 1 pps reference in the short term can be much worse than that of the PRS10, the PRS10 phase-locks to the 1 pps with an adjustable time constant of from 8 minutes to 18 hours, which reduces the noise of the reference 1 pps by averaging.

The rear-panel 1 pps input to the FS725 is a high impedance input that is discriminated by a CMOS Schmitt trigger, with a threshold of about 2.5VDC. It is important to provide a 1 pps input with CMOS levels (0-5VDC.) The 1 pps input may not work reliably with a TTL input or the 1 pps output from another instrument (such as another FS725) if the signal is terminated into 50 Ω. (The 1 pps from another FS725 will work fine, providing it is not terminated into 50 Ω.)

A classical 2nd order phase-lock control loop is implemented in firmware. The "phase comparator" is a time-tagging circuit which measures the timing of the 1 pps input with nanosecond resolution. A proportional-integral phase-lock algorithm controls the frequency of the rubidium frequency standard via the parameter SF (Set Frequency). Normally, the SF parameter is set by the firmware reading the calibration potentiometer. However, when a 1 pps signal is seen, the phase-lock algorithm 'hijacks' the SF parameter to phase-lock the rubidium frequency standard to the 1 pps input.

The locking algorithm of the PRS10 proceeds as follows:

- The 1 pps PLL is enabled when the unit is turned-on or restarted if the PL parameter stored in the unit's EEPROM is "1". (This is the default value.)

- The PLL will begin to control the frequency of the rubidium frequency standard when 256 consecutive "good" 1 pps inputs (i.e., 1 pps inputs which are within ±2048 ns of the first time-tag result, modulo 1 s) are received.

- After receiving 256 consecutive "good" 1 pps inputs, the 1 pps output pulse is moved to coincide with the last of the 256 time-tag values. The front panel "1 pps synchronized" LED will turn on, as the 1 pps input and the 1 pps output are now within ±1μs of each other.

- The unit will lock the frequency of the PRS10 to the "good" 1 pps input pulses. "Bad" 1 pps inputs (1 pps inputs with time-tags greater than 1,024 ns from the last "good" 1 pps input) will be rejected. A digital filter is used to implement the classical 2nd order

proportional/integral phase lock loop. The output of the digital filter controls the frequency of operation via the SF (set frequency) command, which is updated once a second.

• The PLL will be aborted and restarted if there are 256 consecutive "bad" 1 pps inputs. (This could happen if the 1 pps input is moved suddenly by more than 1,024 ns.)

The time constant of the PLL is set with the PT command. The default value is 8, providing a 'natural time constant' of about 2.25 hours. The PT value should be set to a smaller number if the 1 pps reference is very clean, for example, if the 1 pps reference is provided by another FS725. Using a smaller PT value will reduce the peak-to-peak variations ('swimming') between the 1 pps input and the unit's 1 pps output. With a clean reference and a short time constant, the 1 pps output typically tracks the 1 pps input within a ±1ns window.

The default time-constant of 2.25 hours is appropriate for locking to the typical GPS receiver. However, if there is a rapid change in the ambient temperature which causes the PRS10 to change frequency by 1×10^{-11}, the change will not be appreciably effected by the PLL during the first hour, and one would expect to see a drift between the 1 pps input and the 1 pps output on the order of 3600×10^{-11}, or 36 ns.

The FS725 indicates that it is synchronized to the 1 pps input by a front panel LED and a rear panel alarm relay. The unit will indicate that it is synchronized when the 1 pps input is present and if it occurs within ±1 μs of the 1 pps output. (A single dropped pulse on the 1 pps input will cause the unit to indicate that it is not synchronized, but there is no detrimental effect from missing a small number of 1 pps inputs.)

It is quite common for a unit to indicate that it has acquired, and then lost, synchronization depending on the initial frequency offset between the FS725 and the 1 pps reference. Suppose that a FS725 is out of calibration by 1×10^{-9} and a 1 pps input is applied while using the default PLL time constant of "PT8" or 2.25 hours. With this time-constant, the PLL algorithm has little effect on the FS725's frequency of operation during the first hour of phase locking, and the 1 pps output will stray from the 1 pps input by about 3600×10^{-9}, or 3.6 μs. This is larger than the ±1 μs synchronization window, and so the unit will indicate that it is not synchronized. With the default time constant, the unit will pull its 1 pps output to within the ±1 μs synchronization window within a few hours, and will thereafter indicate that it is properly synchronized.

The table below shows the PLL parameters for the allowed values of the PT parameter. The right-most column, "Natural Time Constant", is the best measure of the PLL response characteristics. (The values shown are for the default stability parameter, ζ=1.)

PT Parameter Parameter set by PT command	Integrator Time-Constant (hours)	Integral Gain (SF bits per hour per ns of time-tag)	Proportional Gain (SF bits per ns of time-tag)	Natural Time-Constant Characterizes PLL response (hours)
0	0.07	-14.063	-3.95	0.14
1	0.14	-7.031	-2.80	0.20
2	0.28	-3.516	-1.98	0.28
3	0.57	-1.758	-1.40	0.40
4	1.14	-0.879	-0.99	0.56
5	2.28	-0.439	-0.70	0.80
6	4.55	-0.220	-0.49	1.12
7	9.10	-0.110	-0.35	1.59
8	18.20	-0.055	-0.25	2.25
9	36.41	-0.027	-0.17	3.18
10	72.82	-0.014	-0.12	4.50
11	145.64	-0.007	-0.09	6.36
12	291.27	-0.003	-0.06	8.99
13	582.54	-0.002	-0.04	12.72
14	1,165.08	-0.001	-0.03	17.99

Further details of the phase-locking algorithm are provided in the PRS10 Rubidium Frequency Standard manual.

Monitoring and Control via the RS-232

A Windows® based program, RbMon, is provided on a 3½" floppy disc. The program may also be downloaded from the SRS web site at www.thinkSRS.com. The program facilitates monitoring, control, and calibration of the FS725 Rubidium Frequency Standard via the computer's COM port over a serial RS-232 interface.

Running the Install program will place the RbMon icon on the Desktop and in the Start Programs list and place the program components in the folder "RbMon". The (provided) Uninstall utility should be used to remove the program and its icons from your computer. System requirements include ≥150MHz Pentium or comparable, Windows® 95 or later, and an available COM port.

The default COM port is COM1. If your computer uses COM1 as a mouse port, you will need to change the COM port to COM2.

The FS725 uses the PRS10 rubidium frequency standard, also manufactured by Stanford Research Systems. All commands sent to the FS725 are passed directly to the PRS10. All commands received from the FS725 come directly from the PRS10. No buffering or filtering of commands is performed by the FS725. The PRS10 operation and service manual, which is an addendum to this document, serves as a programming reference for the FS725.

Setting up Communications

The PRS10 frequency standard can communicate operating and calibration settings, such as lock indicators, signal levels, heater control status, 1 pps time tags, status flags, and calibration parameters. This provides the systems' integrator with the ability to monitor and control the operation of the PRS10.

Communicating with the PRS10 is not required in most applications. The PRS10 comes from the factory calibrated to $\pm 5 \times 10^{-11}$, and the FS725 provides front panel LEDs to indicate power, lock, and 1 pps synchronization.

You may want to communicate with the PRS10 to access advanced features or for evaluation of the PRS10 in an OEM application. For instance, when locking the PRS10 to an external 1 pps reference you may want to optimize the time constant and lock mode of the digital PLL to match the stability characteristics of your reference.

Getting Connected

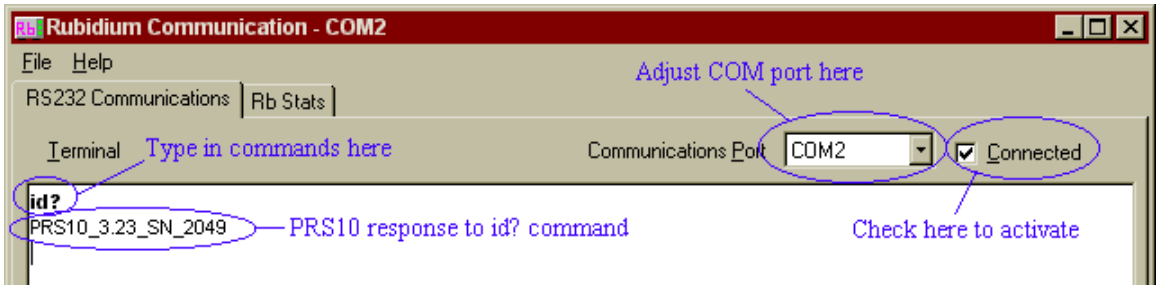
The PRS10 uses the RS-232 protocol for communication. Most computers have one or more communications ports for this purpose. To establish communication with the PRS10 you will need a standard, straight-through 9-pin RS-232 cable connected between your computer's communications port and the DB9 connector on the back of the FS725.

Once the cable is in place, you need to tell the software which COM port you will be using to communicate with the FS725. This is done with the pull down list box located in the upper

right portion of the main window. Use the pull down list box to select the COM port. For most computers this will be either COM1 or COM2. Make sure that the "Connected" box is checked. This will activate the communications port.

Testing the Connection

Test the connection by sending a command to the PRS10 to see that it responds properly. Type the command ID? and press <ENTER>. The PRS10 should respond with its identifier string. A typical screen shot with all the pertinent elements pointed out is shown below.



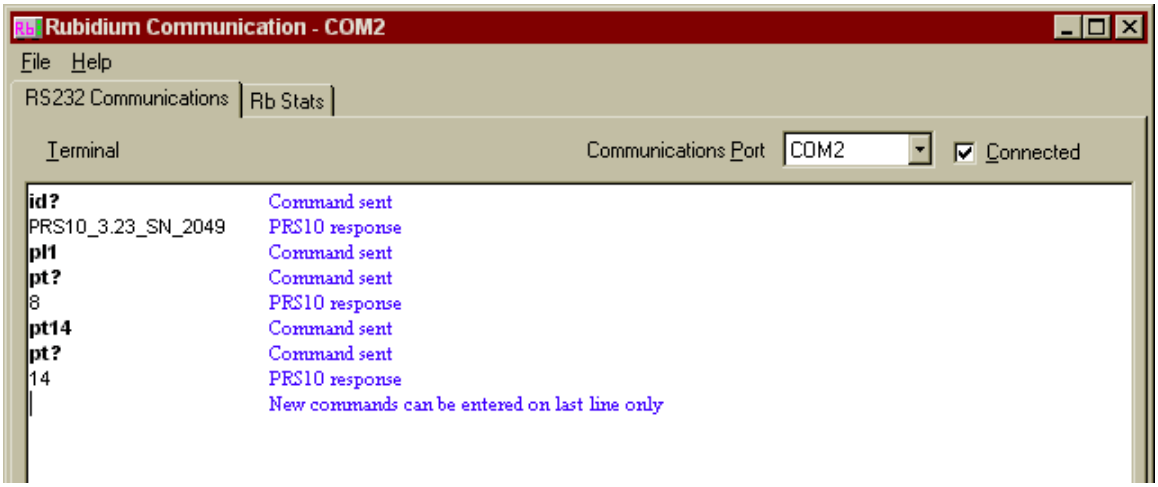
RS-232 Communications

Use the tab labeled RS-232 Communications to send commands to the PRS10 manually. This tab is meant to provide the user with an easy method for manually typing commands to the PRS10. To use it, make sure that the proper communications port is selected, and that the "Connected" box is checked. Once that is complete, sending a command to the PRS10 is as simple as typing it in and pressing <ENTER>.

For ease of interpretation, commands that you type will be formatted in **bold**. Responses from the PRS10 will have normal formatting. Keep in mind that the PRS10 will not respond to all commands. It only responds to query commands—ones ending with a question mark (?).

One important point to keep in mind is that commands can only be entered on the last line. Lines above the last line show the previous commands sent and responses received. These lines can not be overwritten. Only the last line is available for typing in new commands.

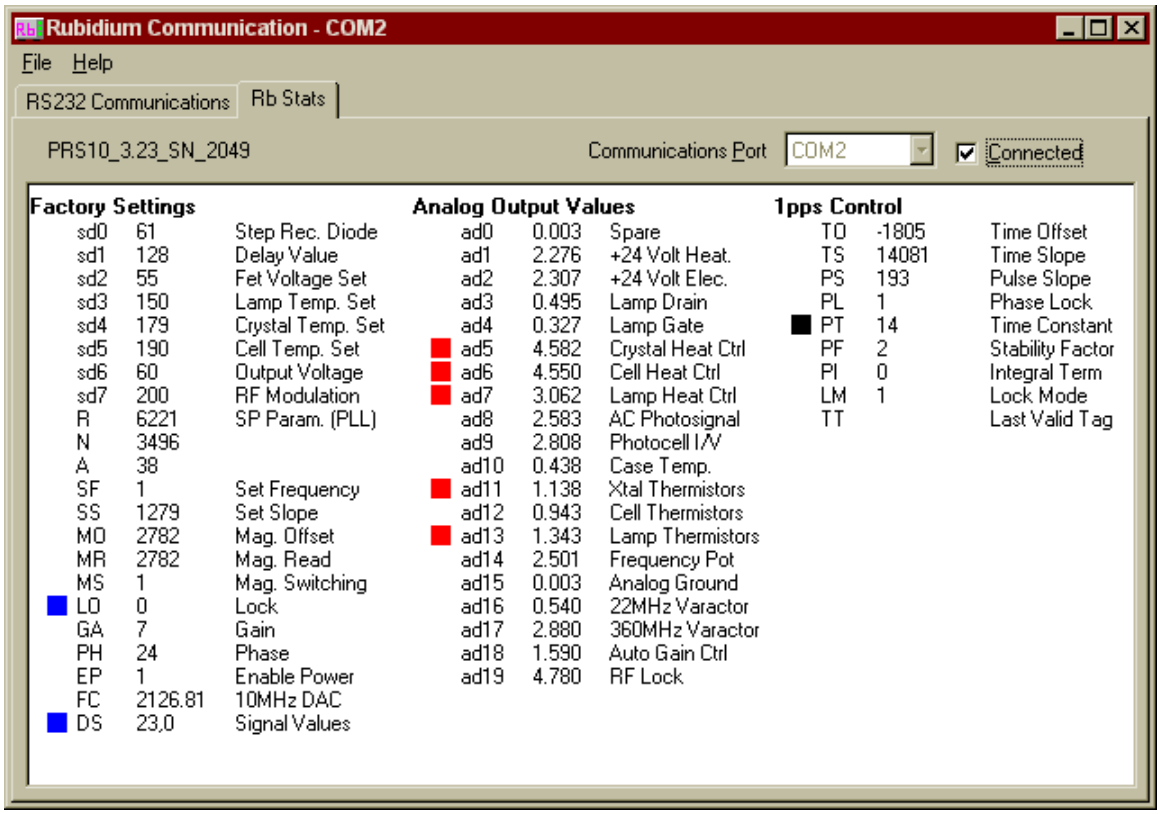
Here is a sample screen shot pointing out the pertinent items of interest.



Rb Stats

The tab labeled Rb Stats is used to monitor virtually all of the PRS10's settings. To view the current PRS10 settings, click on the Rb Stats tab, make sure that the selected communications port is correct, and click the "Connected" check box to enable the connection. The screen should fill in with the current PRS10 settings. The settings will be continuously updated until you disconnect from the communications port by clicking on the "Connected" check box a second time to uncheck it.

A sample screen shot, taken while the PRS10 was warming up, is shown below.



The screen is divided into three main sections labeled Factory Settings, Analog Output Values, and 1 pps Control. Each section has three columns. The first column contains the command name, the second contains the current value of that parameter, and the third contains a brief description of the parameter. Colored boxes highlight various parameters that are out of the normal operating range. The three sections and the meanings of the colored boxes are briefly described below. For detailed descriptions of each of the commands, consult the PRS10 manual.

Factory Settings

This section includes calibration values and parameters for controlling the frequency of the PRS10. The most important parameter here is “LO”, which indicates whether the PRS10 has locked to the Rb atomic hyperfine transition. In the screen shot, the value of LO is zero, indicating that the unit has not yet locked to the atomic transition. It is highlighted with a blue box to indicate that this value is lower than normal.

Analog Output Values

This section contains the current values of 20 internal voltage test points within the PRS10. These values allow you to monitor the heaters, temperatures, power supplies, phase lock loops, and lamp characteristics of the PRS10. In the example screen shot, the values AD5, AD6, and AD7 are highlighted with red boxes to indicate that the heaters are at maximum power. Values AD11, AD12, and AD13 indicate the current voltages on the temperature sensitive thermistors. Values AD11 and AD13 are highlighted with red boxes to indicate that these voltages are above normal. In the above screen shot, AD12 is not highlighted because the cell has almost reached the correct operating temperature. Highlighted boxes are a normal occurrence during the warm-up of the PRS10.

1 pps Control

This section contains calibration parameters that control the PRS10's behavior when locking to an external 1 pps reference. In the example screen shot, PT is highlighted with a black box. This is meant to indicate that its current value, 14, is different from the value stored in EEPROM, which is the value it will have at start up. In this particular case, the command PT14 was entered manually in the RS-232 Communications tab to change the current value of PT from 8 to 14. The value for TT, the last valid time tag, is blank because the unit has not yet received a pulse on its 1 pps input. When a pulse is received, the TT command will report the time difference in nanoseconds between the input pulse and the 1 pps output.

Colored Boxes

The colored boxes are visual cues to let the user know that a given parameter is outside the normal operating range. This most commonly occurs at start up, while the unit is warming up. After about 15 minutes of operation, the unit should be fully warmed up, and all red and blue boxes should disappear. After the initial warmup, the appearance of a colored box typically signals something unusual that should be looked into. If the unit was being operated in an oven, for example, the unit may not be able to properly regulate the temperatures of the crystal, cell, and lamp. Under these circumstances, one would expect blue boxes to appear next to AD5, AD6, and AD7, as the heaters are shut off.

The interpretation of the boxes is as follows:

(Red) Value is higher than normal.
(Blue) Value is lower than normal.
(Black)Value is different from the value stored in EEPROM

File Menu

Print

The program can print out the current settings shown in the Rb Stats tab. To do this, make sure that the Rb Stats tab is visible and then select Print from the File menu. The current values displayed in Rb Stats will be sent to the printer. The formatting of the printed output is intended for standard 8 ½ by 11 inch, Letter size paper. Printing on paper of other sizes is not supported, but not prevented.

Print Setup

Print Setup enables you to configure your printer for printing. You should choose Letter size paper (8 ½ by 11 inch) and the Portrait orientation. Landscape orientation is not supported.

Exit

The Exit menu item will close the program.

Help Menu

Contents

Choose this menu item to display help infromation.

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Communicating with Other Devices

RbMon was designed to communicate with the PRS10, however many people have used the RS-232 Communications tab as a general purpose dumb terminal for communicating with other instruments and devices. If you wish to do this, keep in mind the following technical limitations:

- The communications port configuration is fixed at 9600 baud, 8 bits per byte, no parity, and 1 stop bit.
- A carriage return, <CR>, is appended to each command sent.
- Commands are sent on a line by line basis. Nothing is sent until the user hits the <ENTER> key, after which the entire line is sent with a <CR> appended to the end.
- Responses to commands from the device are expected to be terminated by a carriage return, <CR>.
- Unprintable characters will not be displayed
- The program does not provide any facility for customizing the COM port settings for communication with other devices.

Calibration

There is a 15-turn potentiometer in the PRS10 rubidium frequency standard which adjusts the operating frequency. The potentiometer is accessible beneath a calibration sticker on the left side of the instrument. The total adjustment range using the potentiometer is ±0.002 ppm or ±0.02 Hz at 10 MHz. Turning the potentiometer clockwise will increase the 10 MHz output by about 0.0025 Hz per turn.

The position of the potentiometer may be determined by measuring the dc voltage on the center pin of the rear panel FREQ ADJ BNC. The voltage will read 0 VDC at the counter-clockwise extreme, +5 VDC at the clockwise extreme, and +2.50 VDC when the potentiometer is centered. This voltage should be recorded before any calibration is attempted. This will allow you to return to the previous calibration if necessary and serves as a record of the frequency aging of the unit.

When the FS725 is shipped from the factory, the potentiometer is set to its center position and the frequency is calibrated via the RS-232. The user can return the potentiometer to the center position by adjusting the potentiometer until the dc voltage on the center pin of the rear panel FREQ ADJ BNC measures +2.50VDC.

The procedure is to adjust the calibration potentiometer so that the FS725 produces 10 MHz to within $\pm 1 \times 10^{-11}$ or 10 MHz ± 0.0001Hz. Important details are list below:

1. Be certain that the FS725 has been operated continuously for at least 24 hours.
2. If the FS725 has been off for more than one week, it should be operated continuously for at least 72 hours before the adjustment is made.
3. Be certain that nothing is connected to the rear-panel FREQ ADJ input.
4. Be certain that nothing is connected to the rear-panel 1 pps input.
5. Measure and record the dc voltage on the center pin of the FREQ ADJ BNC.
6. Power cycle the FS725 by unplugging it for at least three seconds. This will make certain that the unit will track the calibration potentiometer (which can be ignored if the unit was phase-locked to a 1 pps input or the frequency had been previously set via the SF command.) The unit should lock in less than a minute as it is warm from previous operation. Wait for at least one hour before proceeding with the calibration.
7. The frequency standard used in the calibration must have an accuracy of better than $\pm 1 \times 10^{-11}$ or 10 MHz ± 0.0001 Hz. A cesium standard or a well characterized rubidium or quartz standard referenced to GPS may be used.
8. The frequency counter must have sufficient resolution and accuracy to perform the measurement. This may require long gate times in the frequency measurement mode of operation. A 100s gate is recommended when using an SR620 Time Interval Counter in the frequency mode.
9. Usually, the measurement can be done more quickly and accurately by comparing the phase of a 10 MHz reference to the phase of the FS725 10 MHz output. A time-interval counter may be used for this purpose. In this case, the 10 MHz reference is used as a timebase for the time-interval counter. The inputs to the time-interval counter will be two 10 MHz signals; one from the 10 MHz reference and one from the FS725. The time-

interval counter should be set-up to report the average of 1000 measurements. The reported time-interval measurements will be between 0 and 100 ns (the period of a 10 MHz signal.) Using the SR620, the resolution and jitter of the average of 1000 time-interval measurements will be less than 1 ps rms, and values will be reported about once a second. Observe how the average time-interval measurement changes with time. If the reported time-intervals are changing by 1ns per second then the two 10 MHz source are "off" by 1×10^{-9} or 0.001 ppm. Adjust the calibration potentiometer until the drift between time-interval measurements slows to less than 1×10^{-11} or 10 ps per second.

10. Measure and record the dc voltage on the center pin of the FREQ ADJ BNC.

Calibration using a 1 pps signal (such as from a GPS receiver)

The FS725 may also be calibrated by phase-locking the unit to the 1 pps signal from a GPS receiver. The calibration potentiometer will be adjusted so that the frequency control parameter, SF, matches the value determined by the phase-locking algorithm.

When a precise 1 pps signal is applied to the 1 pps input on the rear panel of the FS725, the rubidium frequency standard will phase-lock to the signal. The 1 pps signal usually comes from a GPS receiver which can have a long-term accuracy of a few parts in 10^{12}. Because the stability of the 1 pps reference in the short term can be much worse than that of the PRS10, the PRS10 phase-locks to the 1 pps with a very long time constant of several hours or more.

A classical 2nd order phase-lock control loop is implemented in firmware. The "phase comparator" is a time-tagging circuit which measures the timing of the 1 pps input with nanosecond resolution. A proportional-integral phase-lock algorithm controls the frequency of the rubidium frequency standard with the SF parameter (Set Frequency). Normally, the SF parameter is set by the firmware reading the calibration potentiometer. However, when a 1 pps signal is seen, the phase-lock algorithm 'hijacks' the SF parameter to phase-lock the rubidium frequency standard to the 1 pps input.

To calibrate with a precise 1 pps input, the FS725 will be phase-locked to the 1 pps input and the SF parameter will be read via the RS-232 interface. Then, the 1 pps input will be removed, the unit will be power cycled (so that the SF is again set by the calibration potentiometer), and the potentiometer will be adjusted to provide the same SF value as was seen when the FS725 was phase locked to the 1 pps.

To use this procedure you will need a source of a precise 1 pps signal, such as a GPS timing receiver. You will also need a way to communicate with the FS725 via the RS-232, such as a PC or laptop computer with a serial port operating at 9600 baud. Any Windows computer together with the FS725 application program, RbMon, will work well.

Procedure for frequency calibration using a precise 1 pps input

1 Be certain that nothing is connected to the rear-panel FREQ ADJ input.
2 Be certain that nothing is connected to the rear-panel 1 pps input.
3 Power cycle the FS725 by unplugging it for at least three seconds. This will make certain that the unit will track the calibration potentiometer (which can be ignored if the unit was phase-locked to a 1 pps input or the frequency had been previously set via the SF command.) The unit should lock in less than a minute as it is warm from previous operation.
4 The position of the calibration potentiometer may be determined by measuring the dc voltage on the center pin of the rear panel FREQ ADJ BNC. The voltage will read 0V at the counter-clockwise extreme or +5 VDC at the clockwise extreme and will read +2.50VDC when the potentiometer is centered. This voltage should be recorded before any calibration is attempted. This will allow you to return to the previous calibration if necessary and serves as a record of the frequency aging of the unit.
5 Connect the RS-232 serial cable between the FS725 and the PC or laptop computer and verify that you can "talk" to the FS725.
6 Be certain that the FS725 has been operated continuously for at least 24 hours (excluding the brief power-cycling.)
7 Send the command: **LM1**. This enables the 1 pps input digital pre-filter to reduce the noise of the 1 pps reference. (LM1 is the default value.)
8 Send the command: **PT8**. This sets the 'natural time-constant' of the PLL to about 2.25 hours, which reduces the noise of the 1 pps reference by averaging. (PT8 is the default value.)
9 If the FS725 has been off for more than one week, it should be operated continuously for at least 72 hours before the adjustment is made.
10 Apply the 1 pps signal to the rear panel of the FS725. The front panel "1 pps input" LED should blink at 1 pps, and the "1 pps sync" LED should light in about 5 minutes.
11 THE FS725 SHOULD BE PHASE-LOCKED FOR AT LEAST 24 HOURS BEFORE PROCEDING TO THE NEXT STEP.
12 Query the SF parameter via the RS-232. (**SF?** The response will be a number between ±2000). Write the number down. The SF parameter is being controlled by the phase-lock loop algorithm and has a resolution of $1:10^{12}$, so ±2000 corresponds to ±0.002ppm. To set the FS725 to $1:10^{11}$, you want to determine the correct value of SF to ±10, so check back in a few hours to determine if the SF parameter has settled. Repeat as necessary.
13 When you have a satisfactory SF value, unplug the 1 pps input and power cycle the FS725 to return control of the SF parameter to the potentiometer. While monitoring the SF parameter via the RS-232, adjust the calibration potentiometer to set the SF value to the value seen when the unit was phase locked to the 1 pps reference. Now, each time the unit turns "on", it will be operating at the same frequency as when it did when it was phase-locked to the 1 pps reference.

Calibration of the time-tag offset parameter

The FS725 can time-tag the leading edge of a rear-panel 1 pps input. Results of the time-tag are returned over the RS-232, in response to the TT? command, in integer nanoseconds with respect to the 1 pps output. If the 1 pps input arrives 5ns after the 1 pps output, the TT? should return a value of 5. If the 1 pps input arrives 5ns before the 1 pps output, the TT? should return a value of 999999995. If no input was applied, and so no time-tag result is available, the TT? will return a value of -1.

There is a calibration parameter, "TO", which is added to the measured time-tag before the result is returned over the RS-232. Offsets in time-tag results can be eliminated by adjusting the TO parameter.

Few users will need to perform this calibration, as fixed offsets of a few nanoseconds in the reported time-tags will have little consequence. Substantial offsets are usually caused by low or slow pulses provided to the 1 pps input: The 1 pps input should make a clean transition from 0 to 5VDC with a rise time of less than 10ns.

To calibrate the TO parameter:

1. Connect to the FS725's serial port using the RbMon program.
2. Select the RS-232 Communications tab.
3. Verify the connection by typing the ID? command.
4. Send the PL0 to disable phase locking to the 1 pps input.
5. Verify that the PL0 command was received by typing the PL? command, which should return a "0", indicating that 1 pps phase locking is disabled.
6. Connect the 1 pps output directly to the 1 pps input with a 3' RG58 coax cable. Do not use any 50 Ω terminators.
7. Query the time-tag with the TT? command. If the result is 5ns, which is the time delay of 3' of RG58 coax cable, then you are done.
8. If the result of the TT? is not 5ns, then query the TO parameter with a TO? A typical value of the TO parameter is -1700ns. This value is added to the time-tag measurement before is it returned via RS-232.
9. If the result of the TT? was greater than 5ns, then increase the magnitude of the TO parameter (making it more negative.) For example, if TT? returned 15ns, and TO? returned -1700, then send TO-1710.
10. If the result of the TT? less greater than 5ns, then decrease the magnitude of the TO parameter (making it less negative.) For example, if TT? returned 1ns, and TO? returned -1700, then send TO-1696.
11. Iterate as necessary, adjusting TO, until the TT? returns 5ns.
12. Save the TO parameter to EEPROM by sending the command TO!
13. Verify that the TO was saved to EEPROM by reading it back from EEPROM with the TO!? command.

FS725 Circuit Description

The FS725 provides an operating environment for the PRS10 Rubidium Frequency Standard. The PRS10 operation and service manual details operation, circuits, and software interface for the rubidium frequency standard as an addendum to this manual.

Rubidium Logic Interface (Sheet 1 of 2)

J100 is the connector to the PRS10 rubidium frequency standard. The pin-out for J100 is detailed in the table below:

Pin No.	Name	Function
1	LOCK/1 pps OUT	TTL HIGH=UNLOCK. PULSES HIGH AT 1 pps
2	POT WIPER	0-5VDC ANALOG FREQUENCY ADJUST
3	POT (-)	ANALOG GROUND VOLTAGE REFERENCE
4	TXD	RS-232 TRANSMIT OUTPUT (CMOS LEVELS)
5	1 pps IN	1 pps TIME-TAG INPUT FOR PHASE-LOCKING
6	+24V HEATER	+24VDC SUPPLY FOR HEATERS
7	RXD	RS-232 RECEIVER INPUT (CMOS LEVELS)
8	POT (+)	+5.00VDC ANALOG REFERENCE
9	+24 ELECTRONICS	+24VDC SUPPLY FOR ELECTRONICS
10	GROUND	POWER SUPPLY CURRENT RETURN

In addition, there is an RF connector which is part of J100, which is used for the 10 MHz sine output from the unit. The connector shell of J100 is also grounded.

1 pps Input

The rear panel 1 pps input is connected directly to the 1 pps input to the PRS10. The PRS10 can time-tag the rising edge of this input and report the time-tag values via the RS-232 with 1ns resolution. The PRS10 can also phase-lock to the external 1 pps input by adjusting its frequency of operation.

The rear panel 1 pps input also triggers a 1µs one-shot (U102B) to detect the synchronization of the 1 pps input to the 1 pps output to within a 1µs window. (The 1 pps output also triggers a 1µs one-shot (U102A). If the two 1 pps pulses have rising edges within 1µs of each other the NAND gate (U101B) will re-trigger the 1.6s one-shot (U103A) which holds the 1 pps SYNC relay (U107) “on.”)

The 1µs one-shot triggered by the 1 pps input also triggers a 70ms one-shot (U103B) which is used to blink the front panel “1 pps input” LED. The 70ms one-shot also holds off additional triggers of the 1µs one-shot until it times-out, reducing the probability of false sync detection in the case that the user’s 1 pps input is running much faster than 1 pps.

Lock and 1 pps output

The PRS10 outputs lock status and 1 pps on Pin 1. This output will have a CMOS high level (5V) until the unit locks its crystal oscillator to the rubidium physics package. When the unit locks, Pin 1 will go to a CMOS low level (0V) and pulse high for 10µs at 1 pps.

An RC filter (R100 & C100) together with the Schmitt trigger (U104A) recovers the lock status and gates the 1 pps output "off" when the unit is unlocked. The Schmitt trigger output holds the LOCK relay "on" when the unit is locked.

The 1 pps output from the PRS10 is gated by U101A and buffered by the octal driver U100. The gated 1 pps is also passed to the optional output modules. The 8 outputs of U100 are ganged together through two 100Ω resistors (R101 & R102) to drive the rear panel 1 pps OUT via a balun (T100). The 1 pps output is intended to drive 50 Ω loads to 2.5VDC requiring 50mA of current during the 10µs pulse. Care was taken to confine this large current pulse to the immediate area around the 1 pps driver: there is an isolated ground plane which is locally bypassed by a 330µF capacitor (C102) and a .1µF capacitor (C101), the system's +5VDC supply is isolated by a 47Ω resistor (R112), and the balun (T100) "requires" that all of the output current returns to the local ground.

RS-232 Interface

The PRS10 can receive serial data on Pin 7 and transmit serial data on Pin 4. The CMOS levels from the PRS10 are level shifted by an RS-232 interface (U105) which has a charge pump to generate the ±10VDC required by the RS-232. Activity on the RS-232 lines is detected by diodes (D100 and D101) and RC networks (R108, C107 & R109, and C108) which drive the front panel LEDs (RS-232 Receive and Send) via Schmitt trigger (U104D and U104E). The charge pump RS-232 interface has a separate ground plane and is locally bypassed and isolated from the system's +5VDC supply.

Front Panel LEDs

A small PCB mounted on the front panel can hold up to 9 LEDs and their current limiting resistors (only six are used in this product.) An LED is lit when the corresponding line is pulled low via a 10 conductor ribbon cable.

Rubidium Power Supplies and RF Amplifiers (Sheet 2 of 2)

Power Supplies

A universal input, +24VDC/55W output, switching supply powers the FS725. After warm-up the FS725 draws only about 1/3rd of the rated power from the supply which improves reliability and reduces ripple. The output of the power supply is further filtered by passive LC networks (L1, L2, C200, L200 and C201) before being applied to the PRS10 rubidium frequency standard.

Three-terminal regulators (U200, U201 and U203) are used to generate systems voltages of +20VDC, +10VDC and +5VDC. A very quiet +5.00VDC reference is provided by U202. A transistor (Q200) is used as a current boost for the +5.00VDC reference.

10 MHz Outputs

The PRS10 provides a 10 MHz sine wave output on an RF connector. The output has a source impedance of 50 Ω and amplitude of 1.41V_{pp} with very low phase noise. The FS725's 10 MHz output drivers were designed to maintain the low phase noise of the PRS10's outputs and to reduce the harmonic distortion with high output-to-output isolation.

The output amplifiers (LM7171's U204 & U206) have high bandwidth, low distortion, low current noise, but rather high voltage noise (14nV/√Hz). A tuned transformer (T200) is used to increase the voltage (and source impedance) of the PRS10's 10 MHz output to avoid degrading the output noise. The 10.7MHz transformer is tuned down to 10 MHz by an additional capacitor on the primary side of the transformer. (The transformers have a 47pF capacitor internally.) The 3.5:1 transformer increases the 10 MHz amplitude to about 5Vpp, the source impedance to about 600Ω, and reduces harmonic distortion. A 10VDC bias (from U205) is added to the transformer secondary so that the 5Vpp output is centered in the common mode input range of the op amps (which are operated from +20VDC.)

The op amps (U204 and U206) are operated with a nominal gain of 2.4. The gain can be adjusted with P200 or P201 to calibrate the amplitude of the rear panel 10 MHz outputs. The op amps drive 50 Ω loads via a tuned output transformer and a 3rd degree Cauer low pass filter. The transformer impedance matches the user load to the amplifier, reduces voltage noise, and insures that all of the output current will return to the isolated ground. Passive LC filters on each power supply also improves channel-to-channel isolation. The output filter reduces the harmonic distortion by an additional 15 dB.

Another amplifier (U208) provides a buffered 10 MHz sine wave to the optional output modules. This amplifier is operated with nominal gain of 2.4 which is adjusted to provide 5 Vpp to the optional output modules. The source impedance of the line is 250 Ω and it has an offset of 10 VDC.

5 MHz Output

A 5 MHz output is created by converting the 10 MHz sine into a square wave, clocking a D-type flip-flop to divide the frequency by two, and filtering the 5 MHz square wave to produce a low distortion 5 MHz sine wave output.

It is necessary to increase the slew rate of the 10 MHz clock signal to the flip-flop so that the noise at the clock input does not produce jitter and so degrade the phase noise. A low-noise, high bandwidth, linear clamping amplifier is used to condition the 10 MHz clock (instead of a comparator.) The clamp amplifier is operated with a gain of 7x, so that the slew rate of its 10 MHz output will be about 1V/ns. The clamping operation restricts the output to an amplitude of 4.5 Vpp with a DC offset of 5.00VDC. This signal is AC coupled into the clock of the D-type flip-flop with a bias of Vcc/2. The clock input of the flip-flop has a nominal threshold of Vcc/2. The flip-flop is powered from the quiet +5.00V reference for two reasons: to reduce the noise of the clock threshold and to reduce amplitude modulation of the output. (The outputs of the flip-flop swing between 0 and Vcc and so any noise on Vcc translates directly into amplitude noise, thereby degrading the phase noise of the output.)

Two flip-flops are clocked with the output of the clamping amplifier. One of the flip-flops drives the rear panel 5 MHz output via R231 & R232, a tuned transformer (T203), and a 5^{th} order Cauer low-pass filter (C241-248 & L209-210). A standard 10.7 MHz transformer is tuned down to 5 MHz by additional capacitance on the primary of the transformer. The tuned transformer and filter attenuate harmonics of the 5 MHz square wave by more than 60dB producing a low distortion 5 MHz sine wave at the rear panel output. The other 5 MHz square wave is used as a clock reference for the optional output modules.

Signals to the Optional Output Modules

A 10-line bus connects signals from the main board to each of optional output modules. Signals and ground planes on this bus are arranged to reduce cross talk. Three power supplies (+20V, +5V and the +5.00V reference), three grounds (all in common), and four signals (10 MHz sine, 5 MHz and its compliment, and the gated 1 pps signal) are passed to all the option modules.

Optional Output Modules

Up to three optional output modules can be installed in the FS725. Each module provides four 10 MHz sine outputs, one 5 MHz sine output, and one 1 pps TTL output. All of the outputs are intended to drive 50 Ω loads and all have the same drive levels, phase noise, and distortion as the standard outputs.

Signals passed from the main board are buffered on each option module. The 10 MHz sine wave is buffered by U300 which operates with a gain of 2 to overcome the attenuation of the input divider used on each channel. To improve distortion, biases are arranged so that none of the 10 MHz amplifiers has any dc current at their output.

The 5 MHz square waves are buffered by U305. The 1 pps signal is buffered by U306. To reduce channel-to-channel cross talk, all channels are placed on separate ground planes and operate from locally bypassed power supplies.

FS725 Component Parts List

FS725 (REV B) MAIN BOARD PARTS LIST

Item	Quantity	Reference	Part	SRS P/N
1	5	C100,C103,C104,C256,C257	.001U	5-387
2	30	C101,C106,C107,C108,C109, C110,C111,C113,C114,C115, C116,C117,C211,C212,C213, C214,C221,C222,C229,C231, C232,C234,C235,C236,C237, C238,C239,C250,C253,C254	.1U	5-299
3	3	C102,C200,C201	330UF	5-516
4	10	C105,C112,C202,C203,C204, C205,C206,C207,C208,C249	2.2U-35V	5-318
5	6	C210,C217,C225,C242,C243, C245	27P	5-368
6	3	C215,C223,C230	.01U	5-298
7	4	C216,C219,C224,C227	100P	5-375
8	4	C218,C220,C226,C228	220P	5-379
9	1	C240	180P	5-378
10	1	C241	390P	5-382
11	1	C244	820P	5-386
12	1	C246	68P	5-373
13	1	C247	330P	5-381
14	1	C248, C255	39P	5-370
15	2	C251,C252	4.7P	5-359
16				
17	3	C258,C260,C262	1P	5-351
18	3	C259,C261,C263	2.2P	5-355
19	2	D100,D101	MBAV70L	3-544
20	6	D150,D151,D152,D153,D154, D155	LED	3-010
21	1	J100	DAM11W1SD	1-1027
22	1	COAX PART OF J100	DM121073-202	1-1028
23	6	J101,J102,J108,J202,J203, J204	BNC_RT	1-579
24	1	J103	BLOCK6	1-1029
25	1	EXTERNAL PART OF J103		1-1030
26	1	J104	DB9F318	1-1031
27	1	J205	HEAD10F-RT	1-1032
28	4	J250,J251,J252,J253	HEAD10M	1-1033
29	4	J254,J255,J256,J257	FUSE_CLIP	0-1044
30	4	L102,L206,L208,L211	BEAD	6-236
31	1	L200	100UH-H	6-594
32	2	L202,L204	.56UH	6-595
33	1	L209	1.8UH	6-596
34	1	L210	1.5UH	6-597
35	3	P200,P201,P202	100	4-353
36	4	R209,R217,R234,R240	100	4-1455
37	2	Q100,Q101	MMBT3904	3-601
38	1	Q200	MMBT3906	3-580
39	1	R100	100K	4-1527
40	6	R101,R102,R204,R206,R222, R225	100/1%	4-1021

Item	Quantity	Reference	Part	SRS P/N
41	7	R103,R104,R107,R205,R207, R213,R214	1K	4-1479
42	4	R105,R106,R108,R109	1M	4-1551
43	2	R110,R111	10K	4-1503
44	6	R112,R229,R230,R241,R242, R243	47	4-1447
45	9	R150,R151,R152,R153,R154, R155,R156,R157,R158	330	4-1467
46	4	R200,R202,R231,R232	249	4-1059
47	1	R201	3.74K	4-1172
48	1	R203	1.74K	4-1140
49	3	R208,R212,R220	604	4-1096
50	3	R210,R218,R235	715	4-1103
51	5	R211,R219,R236,R237,R238	499	4-1088
52	4	R215,R216,R227,R228	1.00K	4-1117
53	2	R221,R226	1.50K	4-1134
54	1	R223	49.9	4-992
55	1	R224	301	4-1067
56	1	T100	T1-1	6-0009
57	4	T200,T201,T202,T203	TOKO7P	6-195
58	1	U100	74HC540	3-748
59	1	U101	74AC00	3-1405
60	2	U102,U103	74HC4538	3-1467
61	1	U104	74HC14	3-662
62	1	U105	MAX232ACSE	3-1468
63	2	U106,U107	HS-212	3-196
64	2	U200,U201	LM317	3-149
65	1	U202	MAX6250BCSA	3-1469
66	1	U203	LM340-5	3-112
67	3	U204,U206,U208	LM7171	3-819
68	1	U205	OP27	3-660
69	1	U207	AD8037	3-897
70	1	U209	74HC74	3-742
71	1	PCB REV-B		7-1337

FS725 OPTION BOARD PARTS LIST (REV-B)

Item	Quantity	Reference	Part	SRS P/N
1	1	C300	2.2U-35V	5-318
2	8	C301,C302,C304,C312,C320, C328,C336,C346	.1U	5-299
3	9	C303,C305,C308,C313,C315, C321,C323,C329,C332	.01U	5-298
4	8	C306,C310,C314,C318,C322, C326,C330,C334	100P	5-375
5	7	C307,C316,C324,C331,C339, C340,C342	27P	5-368
6	8	C309,C311,C317,C319,C325, C327,C333,C335	220P	5-379
7	1	C337	180P	5-378
8	1	C338	390P	5-382
9	1	C341	820P	5-386
10	1	C343	68P	5-373

Item	Quantity	Reference	Part	SRS P/N
11	1	C344	330P	5-381
12	1	C345	39P	5-370
13	1	C347	330UF	5-516
14	2	C348,C349	.001U	5-387
15	5	C350,C352,C354,C356,C358	1P	5-313
16	5	C351,C353,C355,C357,C359	2.2P	5-355
17	1	J300	HEAD10	1-1032
18	6	J301,J302,J303,J304,J305, J306	BNC_RT	1-579
19	2	J307,J308	STANDOFFS	0-293
20	4	L305,L306,L307,L308	.56UH	6-595
21	1	L309	BEAD	6-236
22	1	L310	1.8UH	6-596
23	1	L311	1.5UH	6-597
24	10	R300,R301,R305,R307,R310, R312,R315,R317,R320,R322	499	4-1088
25	8	R303,R304,R308,R309,R313, R314,R318,R319	2.00K	4-1146
26	4	R306,R311,R316,R321	604	4-1096
27	2	R323,R325	249	4-1059
28	2	R326,R327	100/1%	4-1021
29	1	R328	100	4-1455
30	6	R329,R330,R331,R332,R333, R334	47	4-1447
31	5	T301,T302,T303,T304,T305	TOKO7P	6-195
32	1	T306	T1-1	6-009
33	5	U300,U301,U302,U303,U304	LM7171	3-819
34	1	U305	74HC04	3-741
35	1	U306	74HC540	3-748
36	1	PCB	REV B	7-1338

FS725 (REV B) HARDWARE PART LIST

Item	Qnt	Description	SRS P/N
1	2	STANDOFF FOR P/S	0-550
2	1	TOP SKIN	7-260
3	1	BOTTOM SKIN	7-259
4	2	6-32 FLAT HEAD FOR P/S	0-195
5	2	6-32 PAN HEAD FOR P/S	0-185
6	2	WASHER FOR P/S MOUNTING	0-97, 0-99
7	1	RIGHT FRONT FOOT	0-179
8	1	LEFT FRONT FOOT	0-180
9	2	REAR FEET	0-204
10	1	BAIL WIRE	7-122
11	4	BIG SKIN SCREWS	0-248
12	4	LITTLE SKIN SCREWS	
13	2	REAR FOOT SCREWS	0-167
14	4	FRONT FOOT SCREWS	0-185
15	4	BEZEL SCREWS	0-150
16	1	BEZEL	7-217
17	12	BNC WASHERS	
18	12	BNC NUTS	

Item	Qnt	Description	SRS P/N
19	1	INSIDE FRONT CHASSIS (REV-B)	7-1320
20	1	INSIDE REAR CHASSIS (REV-B)	7-1321
21	1	CORCOM 3EEA1, DIGIKEY CCM1622-ND	0-1045
22	1	3" BLACK	0-548
23	1	3" WHITE	0-549
24	2	3" GREEN/YELLOW	0-521
25	1	17" BLACK (THREE TURNS THROUGH FERRITE)	0-225
26	1	17" RED (THREE TURNS THROUGH FERRITE)	0-227
27	2	BIG FERRITE BEADS FOR POWER LEADS	6-598
28	1	ADHESIVE CLIP	0-418
29	1	CHASSIS BINDING POST	0-517
30	1	LUG FOR BINDING POST	
31	8	4-40 PAN X 1/4" PCBs AND ROUND STANDOFFS	0-187
32	7	4-40 FLATHEAD PHILLIPS X 1/4"	0-149
33	4	6-32X1/4" FLAT HEAD CHASSIS SCREWS	0-181
34	2	DB-9 CHASSIS HARDWARE	0-79?
35	5	4-40 KEP NUTS	0-43
36	4	4-40 ROUND THREADED STANDOFF	0-293
37	2	4-40 FLAT HEAD BLACK SCREWS FOR PEM	0-240, 0-401
38	1	MAP55-1024 +24VDC POWER SUPPLY	6-182
39	1	LINE CORD	1-053
40	1	RS-232 SERIAL CABLE	1-277
41	1	12", 10 CONDUCTOR, CABLE WITH 0.1" PITCH	
42	2	4-40 NYLON SHOULDER WASHER	0-231
43	2	TO-220 INSULATOR PADS	0-243
44	2	HOLE COVERING BRACKET (NEW FAB)	7-1345
45	1	FRONT PANEL LEXAN	7-1366
46	1	PRS10 FROM SRS FINISHED GOODS	PRS10

Model PRS10
Rubidium Frequency Standard

Operation and Service Manual



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Version 1.5 (Dec. 21, 2015)

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PRS10 Rubidium Frequency Standard Introduction

The PRS10 is a ultra-low noise 10 MHz frequency standard which disciplines an SC-cut ovenized oscillator to a hyperfine transition in the ground state of rubidium.

The PRS10 was designed to fill a variety of communication, synchronization, and instrumentation requirements. The phase noise of the 10 MHz output is low enough to be used as the reference source for cellular synthesizers. The unit's short-term stability and low environmental coefficients make it an ideal component in network synchronization systems. Also, the low aging rate makes it an excellent choice as a timebase for precision frequency measurements.

The unit is compatible in fit, form, and function to the Efratom FRS frequency standards, with improvements in features and performance. The PRS10 allows closed case diagnostics and calibration via an RS-232 interface, its digital synchronous detection and filtering eliminate spurs on the 10 MHz output, and the PRS10 has 1000x less phase noise than the Efratom unit (-130 dBc vs. –90 dBc at 10 Hz).

The PRS10 can time-tag an external 1pps input with very high resolution. These values may be reported back via RS-232 and/or used to phase lock the unit to an external reference (such as GPS) with a time-constant of several hours. This feature can provide Stratum 1 performance at a very low cost.

In addition to reading time-tag results, the RS-232 interface allows the user to set the frequency, adjust the phase of the 1pps output, read the value of virtually every parameter (lamp drive level, rf level, temperature set point of the crystal, lamp, and resonance cell, and 10 MHz output level) and measure many "test-points" (lamp light level, heater currents, power supply voltages, and case temperature.)

The PRS10 establishes a new level of features and performance in atomic frequency standards. Its design provides for the lowest phase noise and easiest path to system integration of any rubidium frequency standard available.

		Units
Output		
Frequency	10 (Sine wave into 50Ω)	MHz
Amplitude	0.5 ± 10% (about 1.41V_{pp} or +7 dBm)	V_{rms}
Accuracy	$\pm 5 \times 10^{-11}$ (at shipment)	Δf/f
Allan variance	$< 2 \times 10^{-11}$(1s), $< 1 \times 10^{-11}$(10s), $< 2 \times 10^{-12}$(100s)	Δf/f
SSB phase noise	<-130 (10Hz), <-140 (100Hz), <-150 (1kHz)	dBc/Hz
Spurious	<-130 (100kHz B.W.)	dBc
Harmonics	<-25	dBc
Aging (after 30 days)	$<5 \times 10^{-11}$ (monthly) $<5 \times 10^{-10}$ (yearly)	Δf/f Δf/f
Return loss	> 25 (at 10MHz)	dB
Temperature	$\pm 1 \times 10^{-10}$ over -20°C to +65°C baseplate	Δf/f
Voltage	$< 2 \times 10^{-11}$ for a 1V_{dc} supply change	Δf/f
Magnetic field	$< 2 \times 10^{-10}$ for 1 Gauss field reversal	Δf/f
Retrace	$\pm 5 \times 10^{-11}$ (72 hr off then 72 hr on)	Δf/f
Settability	$< 5 \times 10^{-12}$	Δf/f
Trim Range	$\pm 2 \times 10^{-9}$	Δf/f
Time to lock	< 6 (starting at 25°C)	minutes
Time to 1×10^{-9}	< 7 (starting at 25°C)	minutes
Other Electrical		
Power supply	+24.0 (nom), +22 (min), +30 (max)	Vdc
Supply current	2.2 (warmup) , 0.6 (steady-state at 25°C)	A
Protection	± 30 (to any pin except rf output)	V_{dc}
RF protection	100 (stable with any termination)	mA
Ext calibration	0-5.00	V_{dc}
Cal reference out	5.00 ± 0.05	V_{dc}
RS-232	9600 (8 bits, no parity, 1 stop bit, 0V/5V levels with x on/x off protocol)	baud
1pps measurement	±10 (accuracy), 1 (resolution)	ns
1pps output set	±10 (accuracy), 1 (resolution)	ns
Miscellaneous		
Temperature	-20 to +65 (baseplate)	°C
Storage	-55 to +85	°C
Size	2.00 x 3.00 x 4.00	inches
Weight	1.32	lbs
Warranty	1	year
Baseplate threads	4-40 (4 places)	
Connector	Mates with ITT/Cannon DAM11W1S series	

Abridged Command List

Commands consist of two-letter ASCII mnemonics. A command may be followed one or more numeric values, and punctuation. Command sequences end with a carriage return (ASCII 13_{10}). All commands are case insensitive. Spaces (ASCII 32_{10}) and linefeeds (ASCII 10_{10}) are ignored.

A command followed by a value is used to set a parameter to the value. A command followed by an exclamation point (! or ASCII 33_{10}) indicates that the current value should be saved to EEPROM to be used as the initial value after the next reset. A command followed by a question mark (? or ASCII 63_{10}) is used to request that the current value be returned. A command followed by an exclamation point and a question mark is used to return the EEPROM value.

For example, the gain parameter determines the time constant used to lock the 10MHz oscillator to the rubidium hyperfine transition. Examples of the four forms of the gain parameter command are:

```
GA?     ;returns the current value of the frequency lock loop gain parameter.
GA7     ;sets the frequency lock loop gain parameter to 7.
GA!     ;writes the value of the gain parameter to EEPROM for use after reset.
GA!?    ;returns the value of the gain parameter which is stored in EEPROM.
```

All strings returned by the unit are terminated with a carriage return (ASCII 13_{10}). In the verbose mode, strings are preceded with a linefeed (ASCII 10_{10}) and terminated with a carriage return and a linefeed. If more than one value is returned by a command the values will be separated by a comma (ASCII 44_{10}).

When a unit is first turned “on”, it will send the string “PRS_10” (without the quotes) followed by a carriage return.

Only commands in **bold type** are available to the end-user. The other commands are “factory only” commands which disabled at the factory.

Query Value	Set Value or Activate	Write EEPROM	Query EEPROM	Description
Initialize				
RS?	**RS 1**			Restart
VB?	**VB *value***			Verbose mode
ID?				Read ID string
SN?	SN *value*	SN!	**SN!?**	Read unit serial number
ST?				Read six status values
LM?	**LM *value***	**LM!**	**LM!?**	Lock pin mode
	RC 1	RC!		Recall factory calibration
Freq. Lock				
LO?	**LO *value***			Frequency lock loop status
FC?	**FC *high,low***	**FC!**	**FC!?**	Frequency control values
DS?				Read detected signals (ω and 2ω)
SF?	**SF *value***			Set frequency offset
SS?	SS *value*	SS!	**SS!?**	Set Slope (SF calibration)
GA?	**GA *value***	**GA!**	**GA!?**	FLL Gain parameter
PH?	PH *value*	PH!	**PH!?**	Phase angle parameter
SP?	**SP *r,n,a***	**SP!**	**SP!?**	Set synthesizer parameters
Magnetic Tuning				
MS?	**MS *value***			Magnetic switching
MO?	**MO *value***	**MO!**	**MO!?**	Magnetic Offset
MR?				Magnet read
1PPS Lock				
TT?				Time-tag (1pps input)
TS?	TS *value*	TS!	**TS!?**	Time slope cal. (1pps input)
TO?	**TO *value***	**TO!**	**TO!?**	Time-tag offset
	PP *value*			Place pulse (1pps output)
PS?	PS *value*	PS!	**PS!?**	Pulse slope cal. (1pps output)
PL?	**PL *value***	**PL!**	**PL!?**	Phase lock (to 1pps input)
PT?	**PT *value***	**PT!**	**PT!?**	Phase lock time constant
PF?	**PF *value***	**PF!**	**PF!?**	Phase lock stability factor
PI?	**PI *value***			Phase lock integral term

Query Value	Set Value	Write EEPROM	Query EEPROM	Description
D/A Control				
SD0?	SD0,*value*	SD0!	**SD0!?**	Set DAC (RF amplitude)
SD1?	SD1,*value*	SD1!	**SD1!?**	Set DAC (1pps delay)
SD2?	SD2,*value*	SD2!	**SD2!?**	Set DAC (lamp intensity)
SD3?	SD3,*value*	SD3!	**SD3!?**	Set DAC (lamp temperature)
SD4?	SD4,*value*	SD4!	**SD4!?**	Set DAC (crystal temperature)
SD5?	SD5,*value*	SD5!	**SD5!?**	Set DAC (cell temperature)
SD6?	SD6,*value*	SD6!	**SD6!?**	Set DAC (10 MHz amplitude)
SD7?	SD7,*value*	SD7!	**SD7!?**	Set DAC (RF deviation)
Analog Test	(12-bit values)			
AD0?				Spare (J204)
AD1?				+24V(heater supply) / 10.
AD2?				+24V(electronics supply) /10
AD3?				Drain voltage to lamp FET / 10
AD4?				Gate voltage to lamp FET / 10
AD5?				Crystal heater control voltage
AD6?				Resonance cell heater control
AD7?				Discharge lamp heater control
AD8?				Amplified ac photosignal
AD9?				Photocell's I/V converter / 4
AD10?				Case temperature (10 mV/°C)
AD11?				Crystal thermistors
AD12?				Cell thermistors
AD13?				Lamp thermistors
AD14?				Frequency calibration pot
AD15?				Analog ground
Analog Test	(8bit values)			
AD16?				VCXO varactor voltage
AD17?				VCO varactor voltage
AD18?				AGC for RF
AD19?				RF PLL lock signal

Theoretical Overview of Rubidium Frequency Standards

Rubidium is an alkali metal (like lithium, sodium, potassium and cesium). There are two naturally occurring isotopes of rubidium, Rb85 and Rb87, which have relative abundances of 72% and 28% respectively. The metal has a melting point of 39°C.

The alkali metals behave similarly: they have one electron outside an inert core. Most of the chemical, electronic and spectroscopic properties of these elements are determined by this outer electron. The deep red glow of a low power rubidium discharge lamp is due to the resonance line transitions of the outer electron as it emits a red photon and drops back to the ground state.

The ground state of Rb87 is split by a very small energy due to the relative orientation of the magnetic spins of the electron and the nucleus. The split corresponds to the energy of a photon with a (microwave) frequency of 6.834,682,612,8 GHz. It is this hyperfine transition frequency which will be used to stabilize the 10 MHz output of the PRS10.

To see how this is might be done, Figure 1 shows a typical physics package which uses a discharge lamp, an isotopic filter, and a resonance cell. We will see that the amount of light which passes through the resonance cell to the photodetector can be reduced when the resonance cell is exposed to microwaves at the hyperfine transition frequency.

To simplify the discussion, we will assume that the light from the Rb87 discharge lamp consists of just two lines corresponding to transitions from a single excited state to the split ground state. The filter cell contains Rb85 vapor which also has a split ground state and an isotopic shift (relative to Rb87) as well. An important coincidence exists: one of the lines from the Rb87 discharge corresponds one of the transitions in Rb85. This will allow us to reduce the intensity of this line by passing the Rb87 discharge light through the Rb85 vapor.

Normally, atoms in the ground state will be equally distributed between the split states, as the splitting is much less than the thermal energy of the atoms in the vapor. This distribution is modified by the filtered light from the discharge, by a process called “optical pumping”.

Suppose that the filter can completely remove one of the two discharge lines. The remaining light can be absorbed by Rb87 atoms in the resonance cell which are in the lower ground state, moving them to the upper state. When they decay from the upper state, they fall with equal probability into either ground state. As this continues, population will be moved from the lower ground state to the upper ground state, circulating through the upper state. As the population in the lower ground state is decreased, the amount of light which reaches the photodetector will increase, as the number of atoms which can absorb the radiation is reduced.

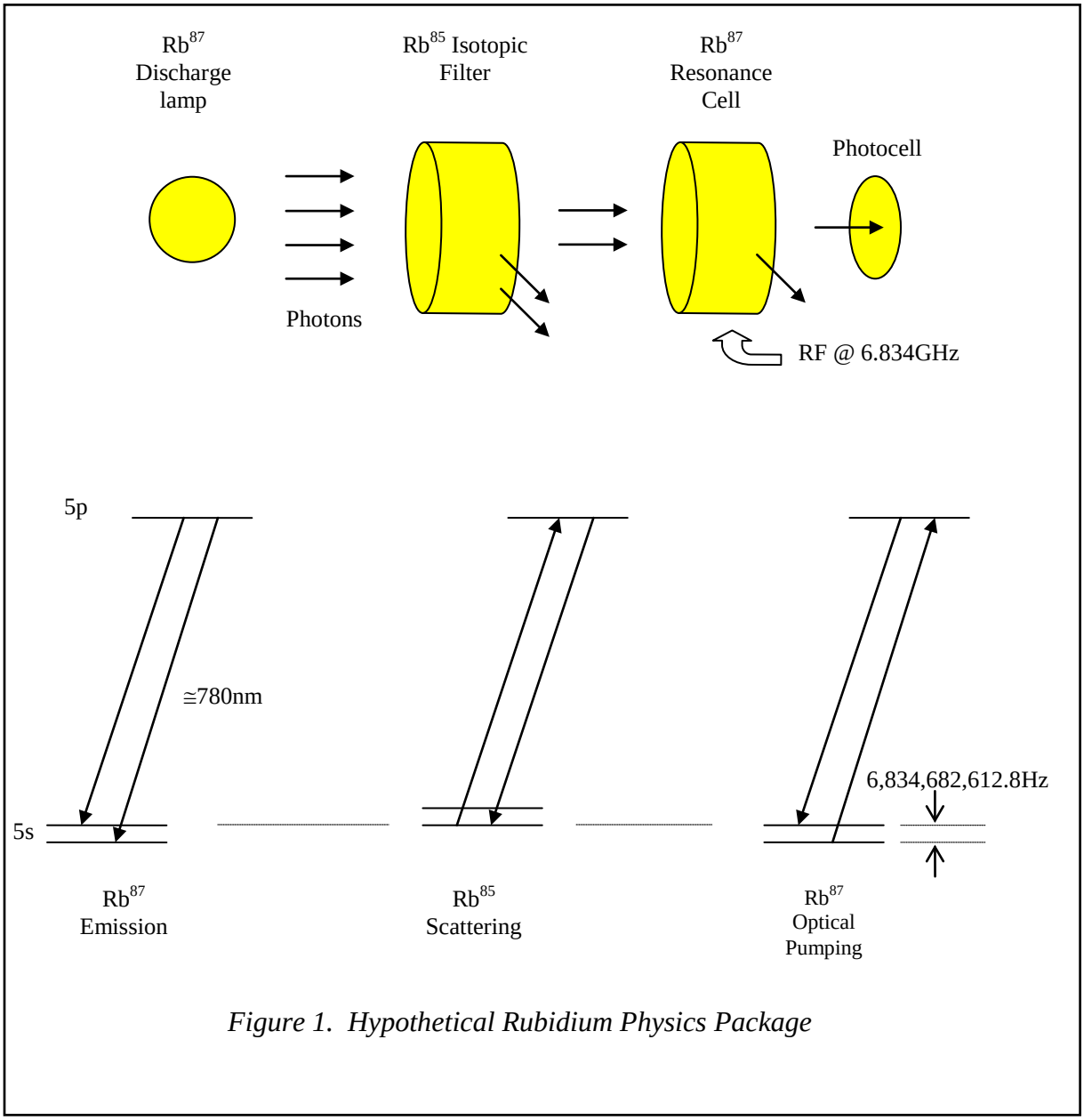


Figure 1. Hypothetical Rubidium Physics Package

Now, if we apply a microwave field at the frequency corresponding to the hyperfine transition frequency (6.834,682,612,8 GHz), the populations in the ground state will mix, and the amount of light reaching the photodetector will decrease.

The PRS10 uses the “integrated filter” topology: rather than a separate filter cell, the resonance cell contains a mixture of the two rubidium isotopes, along with a buffer gas. The lamp also contains a mixture of isotopes. The isotopic mixtures, buffer gases, and operating conditions are chosen so as to minimize temperature coefficients and intensity shifts of the apparent hyperfine transition frequency.

The apparent transition frequency will be shifted by about 3 kHz from the natural transition frequency by the buffer gas and discharge lamp spectral profile. The transition frequency differs slightly for each unit, depending on the fill pressure, etc. The transition frequency is also tuned over a few Hertz by a magnetic field which may be varied.

In the PRS10, the rubidium physics package acts as a very stable frequency detector for a frequency around 6.834 GHz. By using a microwave frequency synthesizer which is referenced to the 10 MHz OCXO, the 10 MHz may be stabilized to the rubidium hyperfine transition frequency.

PRS10 Overview

All compact rubidium frequency standards discipline a crystal oscillator to the hyperfine transition frequency in the ground state of rubidium. Several different topologies have been developed. A major difference in these designs is the method chosen to lock a standard output frequency (usually 10 MHz) to the (essentially arbitrary) hyperfine transition frequency at about 6.834 GHz.

Block Diagram

Figure 2 shows a block diagram for the PRS10 Rubidium Frequency Standard. The design of the PRS10 is quite different from other rubidium frequency standards leading to several feature and performance benefits.

Ovenized Oscillator

The output from PRS10 comes directly from a 10 MHz oven stabilized, 3rd overtone, varactor tuned, SC-cut crystal oscillator. The varactor is tuned by a 22bit digital-to-analog converter which provides a full scale tuning range of ±2 ppm. The very fine step size ($\approx 1{:}10^{-12}$) maintains the low noise inherent to the SC-cut resonator, yet the full-scale range is sufficient to compensate for crystal aging over the lifetime of the unit. This approach provides a 10 MHz output with extremely low phase noise which is virtually free of spurs.

Frequency Synthesizer

The 10 MHz also serves as the reference source to the frequency synthesizer which generates RF at about 359.72 MHz. The RF is multiplied by a factor of 19x in a step recovery diode to provide the microwave frequency (at about 6.834 GHz) which is used to interrogate the physics package. (The apparent hyperfine transition frequency varies with each physic package due to variations in buffer gas fill pressure, etc.)

The frequency synthesizer has two important characteristics: a step size of about $1{:}10^{-9}$ and very low phase noise output. The small step size is required so that only small magnetic fields will be needed to tune the apparent hyperfine transition frequency between the steps of the synthesizer. The low phase noise is required so as not to degrade the signal from the physics package, which would lead to a noisy frequency lock, and degraded output stability.

These two characteristics require a dual loop design for the frequency synthesizer. The inner loop consists of the 359.72 MHz VCO which is directly phase locked to a 3rd overtone 22.48252 MHz crystal oscillator. This loop has a large natural frequency of about 400,000r/s. The VCO's phase noise at 359.72 MHz is very close to the phase noise of the crystal (plus 24 dB for the multiplication factor of 16).

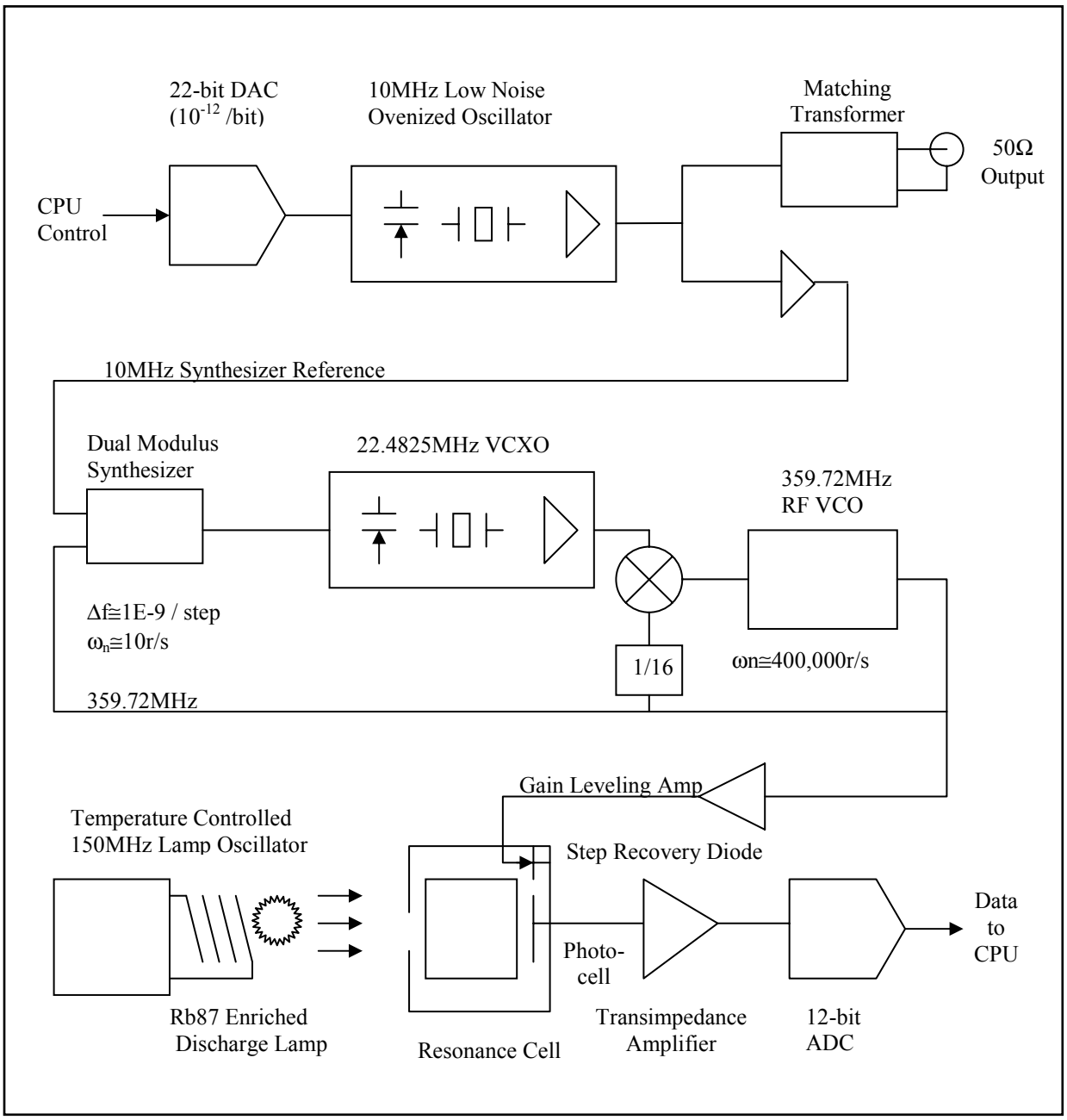


Figure 2. Rubidium Frequency Standard Block Diagram

The outer loop compares the RF frequency to the 10 MHz. This loop provides high resolution by dividing the RF and 10 MHz by large numbers, and consequently operates at a low comparison rate (typically 4 kHz). This loop has a low natural frequency (about 10 r/s) so the phase noise of the RF more than a few Hz from carrier will be determined by the inner loop. The outer loop slowly disciplines the frequency of the inner loop's crystal, keeping it locked to the 10 MHz reference.

The frequency synthesizer is set to the nearest frequency above the apparent hyperfine transition for the unit's physics package. A magnetic field is used to tune the physics package's apparent hyperfine transition frequency up to the synthesizer frequency. A 70 Hz digitally synthesized sine wave is used to phase modulate the inner loop. (The outer loop bandwidth is too small to suppress this modulation.) This generates an RF output, which when multiplied to 6.834 GHz, sweeps by about 300 Hz around the apparent hyperfine transition frequency. By sweeping through the transition at 70 Hz, the output from the photocell will have an ac component at 140 Hz, when centered on the transition. There will be an ac component at 70 Hz if we are off to one side of the transition: the phase of the 70 Hz component is used to determine if the RF is above or below the transition.

Physics Package

The physics package consists of a discharge lamp (enriched with Rb87) and an integrated filter and resonance cell. The discharge lamp operates at about 150 MHz. The lamp oscillator can provide up to 300 V_{pp} to start the lamp, which drops to about 100 V_{pp} during normal operation. The lamp oscillator voltage and current are carefully regulated to provide a consistent intensity and low noise.

The resonance cell is inside a mu-metal shell to reduce the frequency pulling effects of external magnetic fields. The apparent hyperfine transition frequency may be quadratically tuned over a range of about $\pm 2 \times 10^{-9}$ by the magnetic field coil. (The frequency shift is always positive, regardless of the direction of the magnetic field.)

To further reduce the effects of external magnetic fields, the current in the field coil is switched at 5 Hz. An external field which adds to the coil's field will increase the apparent transition frequency, and an external field which opposes the coil's field will decrease it. By alternating the coil's field and averaging, the effect of an external field can be reduced.

Control Algorithm

The microcontroller is responsible for (1) generating the 70 Hz phase modulation of the RF to probe the physics package, (2) synchronously detecting the amplitude and phase of the photosignals at 70 Hz and 140 Hz, and (3) digitally filtering the error signal to lock the 10 MHz SC-cut ovenized oscillator to the rubidium hyperfine transition.

The 70 Hz digitally synthesized phase modulation waveform is generated via a 12-bit DAC in 32 discrete steps. A low pass filter is used to remove image frequencies from the modulation waveform. The microcontroller's hardware timers are used synchronize updating of the DAC so as to eliminate sample jitter. The modulation waveform has very little distortion, noise or spurs, and is precisely 70 Hz.

The photosignal is amplified and bandpass filtered before being converted by a 12-bit ADC. The microcontroller multiplies the ADC samples by table data corresponding to sines and cosines at 70 Hz and 140 Hz. The products are summed over a frame of 14 modulation cycles

which completely eliminates signal components at 5 Hz, (and at any integer multiple of 5 Hz including 50 Hz, 60 Hz, 70 Hz and 140 Hz) from the error signal, so that there will be no spurs at the modulation frequency in the 10 MHz output.

The summed product corresponding to the detected signal at 70 Hz and 0° is used to frequency lock the 10 MHz oscillator to the Rb hyperfine transition frequency. This value is filtered in a simple, first order, IIR digital filter. The filter coefficient determines the frequency lock loop time constant. Time constants from 1 s to 128 s are available to optimize the output stability of the 10 MHz.

Initial Locking

When power is first applied to the unit, the EFC (the electronic frequency control, or, the voltage applied to the varactor in the 10 MHz SC-cut oscillator) is set to the last value for which the unit was locked. As the 10 MHz oscillator heats to its operating temperature, the output frequency will increase smoothly to converge on 10 MHz. In most cases, the output frequency will be within 0.1 Hz of 10 MHz even before the lock to rubidium is achieved.

After the lamp starts, and the physics package settles to its operating temperature, a resonance signal will be detected by the processor, and used to lock the crystal oscillator to rubidium. In the case that no signal is detected, or if the signal is lost during normal operation, the processor will suspend the frequency lock loop, and maintain the varactor voltage to the 10 MHz ovenized oscillator at a fixed level. Any of the following conditions would cause the CPU to suspend lock:

1) The detected signal at 140Hz is very low.
2) The discharge lamp light level is outside an acceptable range.
3) The RF synthesizer is unlocked.
4) The RF AGC level is pinned high or low.
5) The VXCO varactor voltage is outside the acceptable range.

Suspending lock will prevent a radical change in output frequency in the case of a physics package failure. So, in the case of most failures which cause loss of the lock to rubidium, the 10 MHz will maintain a stable output, with an aging of a few parts in 10^{10} per day.

Locking to External 1pps

The PRS10 may be locked to an external 1pps source (from a GPS or LORAN receiver, for example) by applying a 1pps pulse to the 1pps input (pin 5 on the main connector). A second order digital phase lock loop (PLL) is used to adjust the frequency of the PRS10 to match the frequency of the 1pps source over long time intervals.

The block diagram of this PLL is shown in Figure 3. The “phase detector” is the time-tagging circuit and firmware, which has a gain of K_{det} = 1bit/ns. The loop filter is a digital filter consisting of an optional pre-filter and a standard proportional-integral controller

(PI controller) with programmable proportional and integral gains. The VCO is the rubidium frequency standard, whose frequency, f, is tuned by the magnetic field via the SF command parameter with a sensitivity for its 1pps output of K_{vco} = 0.001 ns / bit-s, or (1 part in 10^{12}) / bit. The response function for each of the elements of the digital PLL is also indicated in the figure in terms of the standard Laplace variable *s*.

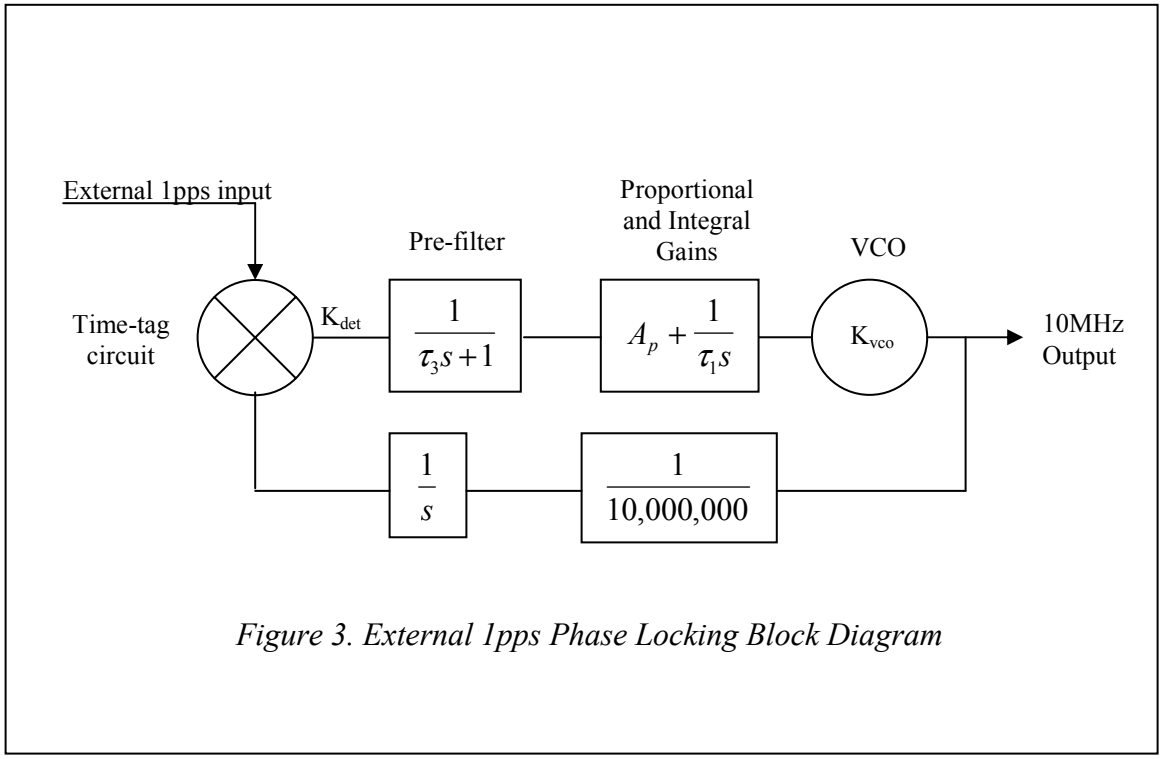


Figure 3. External 1pps Phase Locking Block Diagram

The PI controller is programmed by choosing an appropriate integrator time constant, τ_1, and a stability factor, ζ. τ_1 determines the natural time constant, τ_n, of the PLL for following a step in phase of the reference, while ζ determines the relative rise time and ringing of the PLL in response to the step. The value of ζ also represents the tradeoff in the equivalent noise bandwidth verses peaking in the passband near the natural frequency of the response function.

The PRS10 accepts integrator time constants, τ_1, ranging from 2^8 to 2^{22} seconds in powers of 2. The natural time constant is given by $\tau_n = \sqrt{\tau_1 / K_{\det} K_{vco}} = \sqrt{(1000\text{s})\tau_1}$. Thus, the PRS10 provides natural time constants ranging from 506 seconds to 18.0 hours. While the integrator time constant (τ_1) determines the natural time constant (τ_n), it is the natural time constant which characterizes the loop response.

The PRS10 accepts stability factors ranging from 0.25 to 4.0 in powers of 2. The default value of ζ = 1.0 corresponds to a critically damped response; $\zeta < 1.0$ and $\zeta > 1.0$ correspond to under-damped and over-damped responses respectively.

With τ_1 and ζ specified, the proportional gain, A_p, of the controller is given by the equation $A_p = 2\zeta / \sqrt{K_{\text{det}} K_{vco} \tau_1} = 2\zeta / \sqrt{(0.001 \text{s}^{-1})\tau_1}$. With the default time constant, τ_1, of 65,536 seconds and a stability factor, ζ, of 1.0, the proportional gain will be about 0.25. In this case the instantaneous frequency of the rubidium source will be adjusted by about 0.25 parts in 10^{12} per nanosecond of time-tag measured.

The PRS10 also provides an optional pre-filter. The pre-filter is enabled by default, but it can be disabled by sending the command **LM0**, which puts the PRS10 into lock mode 0. When the pre-filter is enabled, the PRS10 will exponentially average the time tags output by the "phase detector" before passing the result to the PI controller. The time constant of the pre-filter, τ_3, is hard coded to be $\tau_n/6.0$ in order to obtain the maximum benefits of the averaging while simultaneously insuring that the PLL will be stable

Use of the pre-filter is recommended when locking to references that have poorer short term stability than the PRS10, but better long term stability. Locking to the 1pps output by GPS is a prime example of such a case. Use of the pre-filter dramatically reduces the digital PLL's sensitivity to the sort term jitter of 50 to 300 ns present on the GPS reference 1pps. The GPS reference also has a significant amount of 1/f noise associated with it. Very long time constants are therefore required to prevent the PRS10 from following this noise too closely. The PRS10 provides natural time constants of up to 18.0 hours, which will allow the PRS10 to follow GPS over time scales on the order of a day, but retain the superior short term stability of the rubidium clock. When locking to a reference that has short term stability comparable to the PRS10, disabling the pre-filter is recommended because it will allow the PRS10 to better track the phase of the reference.

In lock mode 0, the PRS10's digital PLL will approximate one of the following three equations depending on the value of ζ:

$$\Delta T(t) = \frac{F_0 - \zeta \Delta T(0) / \tau_n}{\sqrt{1-\zeta^2} / \tau_n} e^{\frac{-\zeta t}{\tau_n}} \sin(\sqrt{1-\zeta^2}\, t / \tau_n) + \Delta T(0) e^{\frac{-\zeta t}{\tau_n}} \cos(\sqrt{1-\zeta^2}\, t / \tau_n) \qquad \text{for } \zeta < 1$$

$$\Delta T(t) = t[F_0 - \Delta T(0) / \tau_n] e^{\frac{-t}{\tau_n}} + \Delta T(0) e^{\frac{-t}{\tau_n}} \qquad \text{for } \zeta = 1$$

$$\Delta T(t) = \frac{-\left[F_0 - (\zeta + \sqrt{\zeta^2 - 1}) \Delta T(0) / \tau_n\right]}{2\sqrt{\zeta^2 - 1} / \tau_n} e^{\frac{-(\zeta + \sqrt{\zeta^2-1})t}{\tau_n}} + \frac{\left[F_0 - (\zeta - \sqrt{\zeta^2 - 1}) \Delta T(0) / \tau_n\right]}{2\sqrt{\zeta^2 - 1} / \tau_n} e^{\frac{-(\zeta - \sqrt{\zeta^2-1})t}{\tau_n}} \qquad \text{for } \zeta > 1$$

ΔT(0) is the initial offset in phase of the PRS10 from the reference. F_0 is the initial offset in frequency of the PRS10 from the reference before the digital PLL is enabled. *ΔT(t)* details how the PRS10 approaches the phase of the reference as a function of time. With the default

time constant, τ_1 = 65,536s, and stability factor, ζ = 1, the PRS10's 1pps output will exponentially approach the phase of the reference 1pps input with a time constant τ_n = 8,095 seconds or approximately 2¼ hours. In lock mode 1, the equations describing *ΔT(t)* are qualitatively similar to those presented above, but generally can only be solved numerically.

The locking algorithm of the PRS10 proceeds as follows:

• The 1pps PLL is enabled when the unit is turned-on or restarted if the PL parameter stored in the unit's EEPROM is "1".

• The PLL will begin to control the frequency of the rubidium frequency standard when 256 consecutive "good" 1pps inputs (i.e., 1pps inputs which are within ±2048 ns of the first time-tag result, modulo 1 s) are received.

• After receiving 256 consecutive "good" 1pps inputs, the 1pps pulse delay is set to the last of the 256 time-tag values. (For example, if the last of the 256 "good" time tag values is 123,456,789 ns then the program will set the 1pps output delay to 123,456,789 ns, which moves the 1pps output by 123,456,789 ns, so that new time-tag values will be about zero.) Also, the current value of the SF parameter (which adjusts the frequency of the rubidium frequency standard over the range of ± 2000 parts in 10^{12}) is used to initialize the integrator, Int(0). (The current value of the SF parameter may be from the internal calibration pot position, an external calibration voltage, the value from a previously received SF command, or the value left over from a previous PLL lock.) If the pre-filter is enabled, the exponential filter for the time tags is zeroed.

• The unit will lock the frequency of the PRS10 to the "good" 1pps input pulses. "Bad" 1pps inputs (1pps inputs with time-tags greater than 1,024 ns from the last "good" 1pps input) will be rejected. The frequency parameter, f, to the SF command will be updated with each "good" time-tag result, ΔT(n), as follows:

The pre-filter : if **LM0** $\overline{\Delta T}(n+1) = \Delta T(n)$

The pre-filter : if **LM1** $\overline{\Delta T}(n+1) = (1.0 - \Delta t/\tau_3)\,\overline{\Delta T}(n) + (\Delta t / \tau_3)\,\Delta T(n)$

The integral term: $Int(n+1) = Int(n) - (\overline{\Delta T}(n+1) / \tau_1) K_{det} \Delta t$

The proportional term: $Pro(n+1) = -A_p\,\overline{\Delta T}(n+1) K_{det}$

The frequency setting: $f(n+1) = Pro(n+1) + Int(n+1)$

In the above equations, Δt is the time between phase comparisons, which is one second for the PRS10. The frequency control value, f, ranges over ±2000 bits. If the new f value exceeds 2000, it is set to 2000. If the new f value is less than -2000, it is set to -2000.

If the new integral term exceeds 2000, it is set to 2000. If the new integral term is less than -2000, it is set to -2000. This will prevent "integrator wind-up" in the case that the f-value is pinned for a long time to slew the 1pps output in line with the 1pps input.

The output of the digital filter, f, is used as the frequency control parameter for the SF (set frequency) command, which is updated once a second.

• The PLL will be aborted and restarted if there are 256 consecutive "bad" 1pps inputs. (This could happen if the 1pps input is moved suddenly by more than 1,024 ns.) The PLL will also be aborted and restarted if the measured time-tag value for a "good" 1pps input exceeds ±4 ns/s * τ_1. (For τ_1's default value of 65,536 seconds, the PLL will restart if the absolute value of a "good" time-tag is greater than 262,144 ns. This could happen if the 1pps input is more than a few parts in 10^{-9} off the correct frequency for a long time.)

CPU Tasks

In addition to the frequency lock loop control, the microprocessor is responsible for a variety of other tasks. The CPU sets D/A values which control the microwave amplitude, the lamp intensity, the 10 MHz output amplitude, and set the temperature of the crystal, lamp and resonance cell. The CPU will also controls peripheral electronics to output a 1pps pulse (with 1ns placement) and measure the time for a 1pps input pulse (with 1 ns resolution).

There is an RS-232 interface which allows closed-case calibration of the PRS10. This capability may also be used to servo the 10 MHz or 1pps outputs to another frequency or time source in a system. For example, this would allow the PRS10 to be locked to the 1pps from a GPS receiver with a long time constant to eliminate aging.

PRS10 Applications

In virtually all cases, the PRS10 may be "dropped into" applications which use the Efratom FRS-C-1A8A4C (10 MHz sine output, -5°C to +65°C) or the FRS-N-1A8A4B (10 MHz sine output, -55°C to +65°C).

Some customers may wish to evaluate the PRS10 on the bench. To facilitate this, SRS can provide a connector adapter, power supply and RS-232 cable. The adapter breaks-out the Cannon plug on the PRS10 to a power connector (2.1 mm with +24 V to center pin), three BNCs (10 MHz and 1pps output and 1pps input), and a DB9 (for the RS-232). The adapter also has status indicators for power, lock and RS-232 activity. This kit allows the PRS10 to be operated from 110-240 Vac (50/60 Hz), provides for a direct connection to a PC via a serial port (typically COM2:), and allows the use of standard BNC cables.

The PRS10 may also be operated with a customer supplied connector (Cannon series DAM11W1S with coaxial insert DM53740-5008 for RG178 cable) from a bench dc power supply. The power supply should be able to supply 2.2 A at +24 Vdc.

Interface Connector

Pin	Name	Description
1	LOCK/1PPS	Lock indication and 1pps output. (See LM command)
2	POT WIPER	Ext. freq. calibration. Nom:+2.50 V. 0-5 V for $\pm 2 \times 10^{-9}$
3	POT -	Ground reference for external frequency calibration.
4	TXD/PHOTO	RS-232 data output or photo I/V monitor output
5	1PPS_IN/PHOTO	1pps input for time-tagging or photo-amp output
6	+24(HEAT)	+24 Vdc supply for discharge lamp and heaters
7	RXD/EFC	RS-232 data input or EFC monitor output
8	POT +	+5.00 Vdc reference output for external freq. cal. pot.
9	+24(CLEAN)	+24 Vdc supply for electronics (not heaters or lamp)
10	GROUND	Case ground and power supply return
coax	10MHz	10 MHz sine output on center conductor

Configuration Notes

The functions of three pins (4, 5 and 7) on the interface connector may be modified by internal hardware jumpers. The function of the LOCK output may be modified via RS-232.

Pin 1: LOCK/1PPS output. The default configuration is: +5 V indicates that the unit is not locked to rubidium (as during warm-up), 0 V indicates a successful lock of the 10 MHz oscillator to rubidium, pulsing high for 10 µs at a 1pps rate. The 1pps output may be moved earlier by any interval from 1ns to 999,999,999 ns via RS-232 command. The unit may be configured to omit the 1pps output via the LM command (via RS-232).

Pin 4: TXD/PHOTO The default configuration uses this pin as an output for RS-232 data. Many system parameters (including the lamp intensity) may be monitored via the RS-232 interface. The function of this pin may be changed to an analog monitor for the lamp intensity by removing one resistor (R347) and installing a 10 kΩ resistor for another (R348) on the microcontroller PCB.

Pin 7: RXD/EFC The default configuration uses this pin as an input for RS-232 data. Many system parameters (including the EFC, electronic frequency control) may be monitored via the RS-232 interface. The function of this pin may be changed to an analog monitor for the EFC by removing one resistor (R354) and installing a 10 kΩ resistor for another (R353) on the microcontroller PCB.

Pin 5: 1PPS_IN/PHOTO The default configuration uses this pin as a 1pps input to allow time-tagging or phase locking to an external 1pps source. The function of this pin may be changed to allow monitoring of the amplified photo-signal. When configured as a 1PPS_IN, R241 will be omitted on the top PCB, and a 1 kΩ resistor will be installed for R242. When configured for PHOTO_AMP output, R242 will be omitted on the top PCB, and a 1 kΩ resistor will be installed for R241.

10 MHz coax shield The default configuration floats the shield of the 10 MHz coaxial connector with respect to ground. The 10 MHz output is transformer coupled, and the shield may be ground referenced by installing the jumper between J101 and J102 (located near the connector on the 10 MHz oscillator PCB.)

Hardware Notes

All of the pins on the interface connector are protected against continuous connection to any potential up to 24 V_{dc}. The power supply pins are protected against polarity reversal and may be operated up to +30 V_{dc}. In most applications, both +24 V_{dc} supplies (heater and electronic supplies) will be connected together and operated from a +24 V_{dc} supply.

Logic outputs (LOCK/1PPS and TXD/PHOTO) have a 1 kΩ output resistance driven by a CMOS logic device operating between +5 V_{dc} and ground. Logic inputs (RXD/EFC and 1PPS_IN) have 100 kΩ to ground and 3.9 kΩ CMOS gate inputs (which have input protection diodes to +5 V and ground).

RS-232 data is sent to the host on pin 4, received from the host on pin 7. The baud rate is fixed at 9600 baud, 8 bits, no parity, with 1 start and 1 stop bit. No DTR or CTS controls are used; rather, the XON/XOFF protocol has been implemented. The transmit drive level is 0 and 5 V, not the +/-12 V normally associated with RS-232. These levels are compatible with most RS-232 line receivers, but does not require their use (a TTL inverter may be used instead), hence simplifies the interface when used inside an instrument at the sacrifice of degraded noise immunity over long lines.

The PRS10 may be connected directly to a PC's COM2: port with three wires: TXD, RXD, and ground. As the PRS10 sources only +5/0 V for the RS-232 (via 1 kΩ) the connecting cable should be kept short.

PRS10	PC's COM: (DB9 Connector)	PC's COM: (DB25 Connector)
Pin 7 (RXD)	Pin 3 (TXD)	Pin 3 (TXD)
Pin 4 (TXD)	Pin 2 (RXD)	Pin 2 (RXD)
Pin 10 (GND)	Pin 5 (GND)	Pin 7 (GND)

Operating Temperature

The unit should be operated so that the baseplate temperature stays below +65 °C. This requirement is usually met by units operating on the bench at room temperature when powered by +24 V_{dc}.

Frequency Adjustment

A magnetic field coil inside the resonance cell is used to tune the hyperfine transition frequency. The magnetic field is controlled by a 12-bit DAC. The output frequency (at 10MHz) tunes quadratically with the DAC setting ($0 \le DAC \le 4095$), and $\Delta f(Hz) \approx 5x10^{-9} \times DAC^2$. The DAC setting is changed from the nominal calibration value (see MO command) in various ways, including, calibration pot position, external calibration voltage, direct setting (see SF command), and external 1pps PLL control.

When the unit is first turned on (or restarted), the internal frequency calibration pot position will be used to set the DAC relative to the calibration value stored in EEPROM. (If a voltage is applied to pin 2 of J100 (POT_W) then this voltage will override the pot position.) An SF command may be sent, or a 1pps input may be applied, to control the frequency offset directly. If either the SF command or the 1pps input control the frequency offset, then the pot position (or external control voltage) will not be used again until the power is cycled or the unit is restarted. All the various ways to adjust the frequency of the 10 MHz output are linearized, and they have a span of $\pm 2000 \times 10^{-12}$ or ±0.020 Hz.

RS-232 Instruction Set

Syntax

Commands consist of a two letter mnemonic and one or more parameters. Commands which end with a question mark (?) will return a value. Commands which end with an exclamation point (!) write the current parameter value to EEPROM for use after the next restart. Commands which end in an exclamation point and a question mark (!?) return the value stored in EEPROM.

All data is communicated in ASCII codes. Commands are case insensitive, and spaces (ASCII 32_{10}) are ignored. Commands are processed when a carriage return (ASCII13_{10}) is received. Returned values are delimited with commas (in the case of multiple returned values) or a carriage return (in the case of a single or the last returned value). Commands available to the end user are in **bold**: some commands are for factory use only and a special code must be transmitted to enable these commands. Parameter lists are enclosed in curly brackets { }, the brackets are not part of the command.

On reset, the unit will transmit the characters: PRS_10 with a carriage return.

Initialization

RS 1

Restart. This command will restart the PRS10's microcontroller just like power-on. (It is not necessary to send a **RS** command on power-up.) All values will return to the values stored in EEPROM. (verbose mode disabled, 10 MHz set to last stored value, etc.) The frequency lock-loop will be disabled until the microcontroller verifies that the unit is warmed-up and that a useful signal level is present. Example**: RS 1** will cause the unit to restart.

VB{0 or 1}
VB?

Set verbose mode. The verbose mode is useful when a human is communicating with the PRS10 using a terminal program (the PRS10 will provide an "OK", command prompts, etc.) The verbose mode should be disabled when a computer program is communicating with the PRS10 (where format characters would interfere.) **Examples: VB0** disables the verbose mode (this is the power-on default mode.) **VB1** will enable the verbose mode.

ID?

Identify. This command returns an identification string which includes the serial number and firmware version of the PRS10. **Example: ID?** will return the identification string PRS10_3.15_SN_12345 (model _firmware version_serial-number).

SN?
SN{value}
SN!
SN!?

Serial number. This command returns the unit's serial number. **Example: SN?** will return 21567 for a unit with serial number 21567. The command to write and burn a serial number are for factory use only.

ST?

Status. This command will return a six number string corresponding to the values of the six status bytes. Each number will range between 0 and 255, and will be separated by commas. (For definitions of the status bytes, refer to the end of the detailed command descriptions.)

LM{value} value = 0, 1, 2, or 3
LM?
LM!
LM!?

Lock mode pin configuration. This command is used to configure the LOCK/1PPS output (pin 1 on the main connector, J100.) The LOCK/1PPS pin may be configured per the following table:

LM	Description of LOCK/1pps Output
0	Output goes low when locked to Rb, pulses high for 10 µs at 1 Hz 1pps locking pre-filter disabled
1	Output goes low when locked to Rb, pulses high for 10 µs at 1 Hz 1pps locking pre-filter enabled (default)
2	Output goes low when locked to Rb, 1pps is disabled
3	Output goes high when locked to Rb, 1pps is disabled

The default value is 1, so that pin 1 will go low when the unit is locked to rubidium, and will pulse high for 10 µs at a 1 Hz rate. The position of the 1pps pulse may be moved with the PP command. **Example: LM?** Could return 1, indicating that the unit is in its default configuration so that the lock pin goes low when locked to Rb, pulsing high for 10 µs at a 1 Hz rate. To configure the unit for no 1pps output, the command string **LM 2** followed by **LM !** will change the unit's power on default for no 1pps output.

RC 1
RC!

Recall. This command is used to return all values in EEPROM to the values which were present when the unit was first shipped from the factory (except for the unit-start and lamp-start counters.) This command should be used if you have been writing values to EEPROM and have somehow corrupted the operation of the device. Executing this command may require calibration of the unit, as the frequency calibration values are also returned to their factory values. The unit will be restarted after the values in EEPROM have been restored to their factory values. **Example: RC 1** will return all calibration values to the values which were determined for the unit when it was manufactured and restart the unit. The RC! command is a factory-only command which writes all of the current parameter values to the EEPROM.

Frequency Lock-loop Parameters

LO{value} value = 0 or 1
LO?

Lock. This command can be used to stop the frequency lock-loop (FLL). It is essentially the same as setting the gain parameter to zero. It may be desirable in a particular application to stop the FLL and set the frequency control value for the 10MHz oscillator manually. (See the FC command.) **Example: LO 0** will stop the FLL. **LO?** will return a value of 0 (if the FLL is not active) or 1 (if the FLL is active.)

FC?
FC{high,low} $0 \le high \le 4095$ $1024 \le low \le 3072$
FC!
FC!?

Frequency control. These commands allow direct control of the 22bit value which controls the frequency of the 10 MHz ovenized oscillator. Normally, this value is controlled by the FLL control algorithm, however, the FLL may be stopped, and the value adjusted manually. (See the LO command.)

Two 12-bit DACs are scaled (by 1000:1) and summed to provide a varactor voltage which controls the frequency of the 10 MHz oscillator. The low DAC, which operates over half its range (to avoid FFL oscillations at the roll-over to the high DAC) provides a LSB frequency resolution of $1.5{:}10^{-12}$. The high DAC, which has a nominal value of 2048, has a LBS resolution of $1.5{:}10^{-9}$. These DACs provide a total tuning range of about ±3 ppm.

Example: Suppose a unit's FLL has been operating for some time and has settled. An **FC?** will return the current value of the DAC pair which might be 2021,1654. (Tracking the FC value over a long period of time tells you about the frequency variations of the 10MHz

crystal. The FC values will change to correct for variations in the crystal frequency due to aging and ambient conditions.)

Both DACs may be set to any value in the range specified above. **Example: FC 2048,2048** will set the 10MHz oscillator back to the middle of its tuning range. However, it is possible to set the frequency of the 10 MHz oscillator so far from the correct frequency that the FLL signal disappears, making the lock impossible. If this happens, the last saved FC value may be read from EEPROM with the **FC!?** command and restored with the **FC{high,low}** command.

The **FC!** command is used to save the current FC values in the unit's EEPROM. The **FC!?** Command may be used to read the value which is stored in the EEPROM. The value stored in EEPROM is used to set the 10 MHz at startup, before the FLL can be established. Occasionally while the unit is operating (at about 20 minutes after power-on and once a day there after) the program will write a new value to EEPROM to correct the value for crystal aging. **Example: FC!?** will return four values (separated by commas), the number of power cycles the unit has undergone, the number of times the FC pair has been written to EEPROM, and the value of the FC pair (high, low) which is used at turn-on and restart.

DS?

Detected signals. This command returns two numbers corresponding to the synchronously detected signals at the modulation frequency, ω_{mod}, and at twice the modulation frequency, $2\omega_{mod}$.

The first number, the amplitude of the signal at ω_{mod}, is the error signal in the rubidium frequency lock loop. The value is proportional to the instantaneous frequency error of the 10 MHz oscillator as detected by the physics package. The value may be large when the unit is first locking, and will bobble around zero in steady state. Each LSB corresponds to about 15 μVrms of signal at ω_{mod}.

The second number is the amplitude (in millivolts rms) of the synchronously detected signal at twice the modulation frequency, $2\omega_{mod}$. The amplitude of this signal is proportional to the strength of the rubidium hyperfine transition signal.

The returned value is a spot measurement taken over just one cycle of the modulation frequency. Since the signals have several Hz of equivalent noise bandwidth, they will be rather noisy.

Example: DS? could return 55,800 indicating a small error signal and a strong resonance signal.

SF{value} -2000 ≤ value ≤ +2000
SF?

Set frequency. This command is used to override the internal calibration pot (or external calibration voltage) to set the frequency directly, relative to the calibration values in EEPROM (see the SP and MO commands.) The command sets the frequency offset in units of parts in 10^{-12} (corresponding to a frequency resolution of 10 μHz at 10 MHz.) The SF? command will return the currently set relative frequency value (with a range of ±2000) whether the value comes from the internal calibration pot position, an external frequency control voltage, an SF command, or from the external 1pps phase lock loop control algorithm. However, SF set command is ignored if the unit is phase-locked to an external 1pps signal. (To re-establish direct control via the SF command, the PLL must be disabled. See PL 0 command.)

Example: SF 100 will set the frequency 100 x 10^{-12} (or 0.001 Hz) above the stored calibration value, and the **SF?** command will return 100.

Data from the SF command cannot be saved when the power is turned off. (To do this type of calibration, see the SP and MO commands.) Once executed, the SF command will disable the analog channels (internal calibration pot and external calibration voltage) until the power is cycled or the unit is restarted.

SS?
SS{value} 1000 ≤ value ≤ 1900
SS!
SS!?

Set slope. This command is used to read the slope calibration parameter for the SF command. This parameter compensates for a variety of factors which affect the magnitude of the coefficient between magnetic coil current and transition frequency. **Example: SS?** might return 1450, the nominal parameter value. This calibration parameter may not be altered by the end user.

The (factory only) SS! command is used to store the current value of the SS parameter to the unit's EEPROM. The SS!? will return the value of the SS parameter which is used on power-up or restart.

GA?
GA{value} 0≤ value ≤ 10
GA!
GA!?

Gain. This command sets the gain parameter in the frequency lock-loop algorithm. Higher gain values have shorter time constants, (the time constant is the time it takes for the frequency lock-loop to remove 67% of the frequency error) but have larger equivalent noise

bandwidths (which will reduce the short-term stability of the 10 MHz output.) A gain of 0 will stop the frequency lock-loop so that the frequency of the output is determined by the 10MHz ovenized oscillator alone. The gain setting, approximate time constants, and approximate equivalent noise bandwidths are detailed in the following table. The gain parameter is set automatically by the program, however, the user may want control over the parameter in special circumstances. **Example: GA7** will set the gain parameter to 7, which has a time constant of about 2 s, which is a typical value for normal operation. **GA?** could return a value of 8 just after restart, which has a short time constant of about 1 s to assist the initial frequency locking. Setting the gain parameter during the first 6 minutes after turn-on or restart will abort the automatic gain sequencing.

Command	Time Constant (seconds)	Noise Bandwidth (Hz)
GA 0	Infinite	0
GA 1	128	0.002
GA 2	64	0.004
GA 3	32	0.008
GA 4	16	0.016
GA 5	8	0.032
GA 6	4	0.064
GA 7	2	0.128
GA 8	1	0.256
GA 9	0.5	0.512
GA 10	0.25	1.024

The **GA!** command stores the current value of the frequency lock loop gain parameter into the unit's EEPROM. **Example:** If the current value of the gain is 6, the command **GA!** will write 6 to the unit's EEPROM which will be used to initialize the gain parameter after the next power-on or restart. Then **GA!?** will return a 6.

PH?
PH{value} $0 \leq$ value ≤ 31
PH!
PH!?

Phase. This command is used to set the phase of the synchronous detection algorithm. The frequency lock-loop (FLL) uses the in-phase component of the photo-signal at the modulation frequency (70 Hz) as the error signal for the FLL. The phase between modulation source and the error signal is affected by phase shifts in the modulation and signal filters and by optical pumping time constants. This parameter corrects for the accumulation of all of these phase shifts. Each modulation cycle consists of 32 phase slots, so each phase increment corresponds to 11.25°. **Example: PH?** would typically return a value of 24.

The PH! command is used to write the current phase parameter into the unit's EEPROM. This is a factory only command. The value which is burned in EEPROM is used on power-on and restart, and may be queried by the **PH!?** command. **Example: PH!?** could return a typical value of 24.

Frequency Synthesizer Control

A frequency synthesizer, which uses the 10 MHz OCXO as a frequency reference, is used to generate the RF which sweeps the rubidium hyperfine transition. The frequency synthesizer multiplies the 10 MHz by a factor M = 19 * (64*N + A) / R, to generate a frequency near 6.834 GHz. (The factor of 19 is from frequency multiplication in the step recovery diode, and the other terms come from the operation of the dual modulus frequency synthesizer integrated circuit.)

The apparent transition frequency is different for each physics package, due mostly to variations in the fill pressure of the resonance cell. The frequency synthesizer parameters, R, N and A, are used to adjust the frequency synthesizer's output frequency to the closest frequency just above the apparent transition frequency, then the magnetic field is set to move the transition frequency up to the synthesizer frequency.

During frequency locking, the frequency of the 10 MHz OCXO is adjusted to maintain the output of the frequency synthesizer on the rubidium hyperfine transition frequency. Initial calibration of the unit will involve finding the synthesizer parameters and magnetic field value which will lock the 10 MHz OCXO at exactly 10 MHz.

During the lifetime of the unit, there will be some aging of the physics package, which will cause the apparent transition frequency to change. This is usually corrected by minor calibration adjustments of the magnetic field strength, which provides a setting resolution of a few parts in 10^{-12}. (See the MO command.) However, if the magnetic field strength reaches its lower or upper limit, it is necessary to change the frequency synthesizer parameters, which can change the output frequency in steps of about one part in 10^{-9}.

The table in Appendix A details the values for R, N and A for the range of frequencies needed.

SP?
SP {R,N,A} $1500 \leq R \leq 8191$ $800 \leq N \leq 4095$ $0 \leq A \leq 63$
SP!
SP!?

Set Parameters. This command is used to set or query the frequency synthesizer's parameters, which will coarsely adjust the unit's output frequency. These parameters may need to be adjusted if the unit cannot be calibrated by magnetic field adjustment.

Example: During calibration, a unit's 10 MHz output frequency is found to be low by 0.010 Hz, and the magnetic field offset adjustment is already at its maximum. (See the MO command.) Sending the **SP?** command returns the current values of R, N and A which are 2610,1466,63 in this example. This corresponds to line 38 in the table in Appendix A. To *increase* the frequency of the 10 MHz output, we select the next *higher* setting, line 37, which will *increase* the frequency by 0.01986 Hz. To do this, we send the command **SP 5363,3014,22** (which are the parameters from line 37). Waiting for the frequency to settle, we now measure the output to be about 0.0098 Hz high. Now the magnetic field is adjusted down to calibrate the unit to exactly 10 MHz. (The **SP!** command is used to save these new values in EEPROM for the next power-on or restart. Also see the MO command for adjusting the magnetic field.)

The **SP!** command is used to write the current frequency synthesizer parameters to the unit's EEPROM for use after the nest restart or power-on cycle. This command is used after the SP command is used during the calibration of the unit. **Example: SP!** will write the frequency synthesizer parameters (R, N and A) which are currently in use to the unit's EEPROM. **SP!?** will return the values for R, N and A which are currently in the unit's EEPROM. The **SP!?** command may be used to verify that the **SP!** write command executed correctly.

Magnetic field Control

A magnetic field coil inside the resonance cell is used to tune the apparent hyperfine transition frequency. The magnetic field is controlled by a 12-bit DAC. Increasing the magnetic field will increase the hyperfine transition frequency, which will increase the frequency of the 10 MHz output. The transition frequency may be tuned over about $\pm 3 \times 10^{-9}$ by the magnetic field, which corresponds to ±0.030 Hz at 10 MHz. The output frequency (at 10 MHz) tunes quadratically with field strength, and $\Delta f(\text{Hz}) \approx 0.08 * (\text{DAC}/4096)^2$.

A minimum magnetic field should always be present to avoid locking to the wrong Zeeman component of the hyperfine transition, so the 12-bit DAC may be set from 1000 to 4095 with 3000 being the nominal midscale value. (A DAC value of 1000 corresponds to about 6% of the full-scale frequency tuning range, 3000 corresponds to about 53%, while 4095 is 100% of the full-scale range.)

To help cancel frequency shifts due to external magnetic fields, the current in the coil is switched at a 5 Hz rate. The frequency lock-loop averages over a full period of the switch rate to avoid injecting a spur at 5 Hz onto the 10 MHz control signal. The switching of the magnetic field is enabled at power-on and restart, but may be turned on or off by RS-232 command. (see MS command.)

The commands associated with magnetic field control (MO, MS, and MR) allow direct control of the magnetic field circuitry. Most users will not want to control the magnetic field directly, but will instead allow the program to read the frequency calibration pot or external control voltage and then control the magnetic field. If they want software control of the unit's

calibration, they may choose to use the SF commands, which disable the analog control and allow the frequency to be adjusted over a range of $\pm 2000 \times 10^{-12}$. (The program will linearize the magnetic field control of the frequency offset with either analog or software control.)

MS?
MS{0 or 1}

Magnetic switching. The MS command is used to turn off or on the 5Hz switching of the frequency tuning magnetic field. Magnetic switching is enabled when the unit is powered-on or after a restart. (Since the PRS10 is calibrated with the field switching enabled, turning off the field switching may alter the calibration.) **Example: MS 1** will turn on the magnetic field switching, and **MS 0** will turn it off. **MS?** will return a "1" if the field switching is currently enabled.

MO?
MO{value} $2300 \leq \text{value} \leq 3600$
MO!
MO!?

Magnetic offset. The magnetic offset is the value, determined when the unit is calibrated, which calibrates the unit to 10 MHz. The restricted range is necessary to allow room for user calibration via the internal frequency calibration pot or by an external voltage. If the unit cannot be calibrated to 10 MHz within the allowed range of MO values, then a different setting for the frequency synthesizer is required. (See SP command and the table in Appendix A. **Example: MO 3000** sets the magnetic offset to 3000, which is its nominal (mid-linear scale) value. The **MO?** command reads back the current value of the magnetic offset. **MO!** is used to store the current value of the magnetic offset parameter to EEPROM for use after the next restart. **MO!?** may be used to query the value stored in EEPROM. This value is used on power-up or restarts.

MR?

Magnetic read. This command returns the value that the 12-bit DAC is using to control the magnetic field. This value is computed from the magnetic offset value (see MO command) and the position of the internal frequency calibration pot, external calibration voltage, or value sent by the SF command.

The value is computed from the equation $DAC = \sqrt{(SF*SLOPE + MO^2)}$ where SF is the desired frequency offset in parts per 10^{-12} (from the cal pot position, the SF command, or the 1pps PLL and is in the range $-2000 < SF < 2000$), SLOPE is the SF calibration factor with a nominal value of 1450 (see SS command), and MO is the magnetic offset value. The returned value should be in the range of 1000 to 4095.

Example: MR? would return a value of 3450 if the magnetic offset is at 3000, the SF command requested an offset of +2000 x 10^{-12}, and the SS CAL factor has the nominal value of 1450.

Frequency Control

The frequency of the 10 MHz output may be adjusted in a number of ways: the internal calibration potentiometer may be set (accessible via a hole in the bottom plate), an external voltage (0 to +5.00 Vdc, applied to the interface connector pin 2) can override the internal pot, or, these analog channels may be overridden with a software command which sets the frequency directly.

When the unit turns on, or after a restart command, the control program will default to reading the analog channel for frequency calibration. (This is important to maintain compatibility with existing sockets.) The calibration pot and the external voltage control provide a full-scale tuning range of ± 2000 x 10^{-12}, with a worst case resolution of 5 x 10^{-12}.

All of the channels for calibrating the unit are linearized, so that the frequency characteristic will be linear with applied voltage, pot setting, or SF value even though the transition frequency changes quadratically with field strength.

One pulse per second (1pps) control

To facilitate system integration, the PRS10 provides a 1pps output which may be set over an interval from 0 to 999,999,999 ns with 1ns resolution. The unit also has the ability to measure the arrival time of a 1pps input over the same interval and with the same resolution.

The ability to time-tag a 1pps input allows the PRS10 to be phase-locked to other clock sources (such as the 1pps output from a GPS receiver) with very long time-constants. This is a very useful feature for network synchronization, and allows the configuration of a reliable Stratum I source at a very low cost.

TT?

Time-tag. This command returns the value of the most recent time-tag result in units of nanoseconds. If a new time-tag value is not available then -1 (the only case for which the returned value is negative) will be returned. **Example: TT?** would return the value 123456789 to indicate that the most recent 1pps input arrived 123,456,789ns after the 1pps output. Returned values range from 0 to 999999999.

TS?
TS{value} 7000 ≤ value ≤ 25000
TS!
TS!?

Time slope. This command is used to calibrate the analog portion of the time-tagging circuit. The analog portion is used to digitize the time of arrival with 1 ns resolution and 400 ns full-scale. (Counters are used for the portion of a time interval longer than 400 ns.) The analog circuit stretches the time interval between the 1pps input and the next edge of a internal 2.5 MHz clock by a factor of about 2000, and measures the duration of the stretched pulse by counting a 2.5 MHz clock. The analog portion of the time-tag result is calculated from the equation $\Delta T(ns) = counts * TS / 2^{16}$, where TS is the time slope value, which has a nominal value of 13,107.

Example: TS? might return 14,158 which is a time slope parameter value a bit above the nominal value, which would be required if the analog portion of the time-tagging circuit stretched the pulse by a bit less than a factor of 2000. **TS?** will return the current value of the time slope.

The TS! command is used to write the current value of the time slope parameter into the unit's EEPROM. The TS {value} and TS! are factory only commands. Example: TS! will write the current value of the time slope (which may be queried with the TS? command) to the unit's EEPROM. **TS!?** will return the time slope calibration factor which is in the unit's EEPROM.

TO?
TO{value} -32767 ≤ value ≤ 32768
TO!
TO!?

Time offset. This calibration value (in ns) is added to the measured time-tag value to reference the result to the 1pps output. To calibrate, the 1pps output is connected to the 1pps input and the time-tag is read with the TT? command. The returned value is subtracted from the current TO value and sent with the TO command to calibrate the offset.

Example: Suppose: the 1pps output is connected to the 1pps input. A time tag value, read with the TT? query, returns a value of 25ns. The TO parameter, read via the TO? query, returns a value of -1750ns. The command TO -1775 is sent to correct for the offset. After waiting about one second (to allow another time-tag value to be acquired) the next TT? query returns a value of 2ns (indicating a measurement of 2ns after the 1pps output) Waiting another second, the next TT? query returns the value 999,999,999ns (indicating 1 ns before the 1pps output). These values are consistent with a well calibrated time-tag offset.

Following calibration of the TO parameter, the **TO!** command is used to write the current value of the time offset to the unit's EEPROM. Example: **TO!** will write the current time-tag

offset value to the unit's EEPROM for use after the next power-up cycle or restart command. **TO!?** will return the value which is burned in the unit's EEPROM. (Note: Firmware revisions prior to Rev 3.23 do not allow user TO! commands. Check the firmware revision with the ID? command.

PP{value} $0 \leq$ value $\leq$ 999999999

Place pulse. This command is used to move the 1pps output from its current position. The 1pps output can be moved earlier in time by 1 ns to 999999999 ns. Since the 1pps input time-tag is referenced to the 1pps output, changing the 1pps output placement will change the report time-tag values as well. (See the TT and TO commands.) **Example: PP 123456789** will move the 1pps pulse train earlier by 123,456,789 ns.

PS?
PS{value} $100 \leq$ value $\leq$ 255
PS!
PS!?

Pulse slope calibration. This command is used to calibrate the analog portion of the 1pps output time delay circuit. This circuit is used to delay the 1pps pulse train with 1 ns resolution and 100 ns full-scale. (Counting logic is used for the portion of the time interval longer than 100 ns.) The pulse slope value corresponds to the DAC8 value which provides a delay closest to (but not exceeding) 100 ns. Example: PS 200 set the pulse slope to its nominal value of 200. (PS{value} is a factory only command.) The **PS?** command will return the current value of the pulse slope.

The PS! command writes the current value of the pulse slope to the unit's EEPROM for use after the next power-on or restart. This command is used after the pulse output analog output is calibrated. Example: PS! will write the current value of the pulse slope (which calibrates the 100 ns analog delay portion of the 1pps pulse delay circuit) to the unit's EEPROM. Note that PS! is a factory-only command.

1PPS Locking Control

To facilitate integration into systems which require very low aging, automatic calibration, or a traceable frequency standard, the PRS10 may be locked to an external 1pps input.

A second-order digital PLL is used to lock the unit's frequency (both the 10 MHz and 1pps outputs) to an external 1pps input with time constants ranging from 256 s to 65536s (about 4 minutes to about 18 hours).

When provided with an accurate and stable 1pps source, the unit will automatically align its 1pps output to the 1pps input and then adjust the frequency of the rubidium reference to

maintain the alignment over time. A typical application would lock the PRS10 to the 1pps output from a GPS receiver with a time constant of several hours.

Several commands and one status byte may be used to control and monitor the PLL, however, default values will allow units to lock to clean 1pps inputs without any software interaction.

PL?
PL{0 or 1}
PL!
PL!?

Phase lock control. This command may be used to disable the 1pps PLL, or to re-enable (and so restart) the 1pps PLL. The unit is shipped with the phase lock control enabled. This command would be used if the 1pps time-tagging were being used to measure the position of 1pps inputs and phase locking is not desired. **Example: PL 0** will disable the PLL to the 1pps inputs so that the frequency of the rubidium standard will not be affected by the 1pps inputs. **PL?** will return a "1" if the PLL to the 1pps is enabled. **PL!** is used to write the current value (0 or 1) to the EEPROM for use after the next start up. **PL!?** is used to query the value of the phase lock control parameter which is stored in the unit's EEPROM.

PT?
PT{value} $0 \le \text{value} \le 14$; $\tau_1 = 2^{(\text{value}+8)}$ seconds (256, 512, ... 4,194,304)
PT!
PT!?

Phase-lock integrator time constant. This command is used to set the PLL's integrator's time constant, τ_1, which phase-locks the PRS10 to an external 1pps input. The integrator time constant is equal to $2^{(\text{value}+8)}$ seconds. The default value is 8, which provides an integrator time constant of $2^{(8+8)}$ or 65536 seconds. Integrator's time constants can range from 256 to 4,194,304 seconds, or from about 4 minutes to 18 days. It is important to note that the natural time constant, τ_n, is different from the integrator time constant, as shown in the table below. The natural time constant is the best measure of the loop response. The PLL natural time constant spans between 8 minutes and 18 hours for PT values between 0 and 14.

Example: PT10 sets the integrator time constant to $2^{(10+8)}$ seconds, or about 72 hours. (Refer to Table below.) For PT10 the natural time constant is about 4.5 hours. **PT?** will return the current value of the time constant parameter. A phase lock time constant may be stored in EEPROM as a new default with the **PT!** command. The **PT!?** command may be used to verify the value stored in EEPROM.

The following case will illustrate the operation of the PLL: Suppose that the PRS10 has been phase locked to a stable 1pps reference for a very long time (several periods of τ_n) when the 1pps reference input makes an abrupt shift of +100ns (moving later in time). The PRS10's 1pps PLL algorithm will reduce the PRS10's frequency of operation (by adjusting its SF

parameter) to eliminate the 100ns phase shift between the 1pps reference input and the 1pps output. After the phase shift is eliminated, the PRS10 will settle to the "correct" operating frequency.

The PLL algorithm computes integral and proportional terms from time-tag measurements, adjusting the SF parameter to phase lock the 1pps output to the 1pps input. The table below shows the integral and proportional gain terms. For the nominal PT value of 8, the integral term is -0.055 SF bits per hour per ns of time-tag and the proportional gain is -0.25 SF bits per ns of time-tag.

Per the table below for PT8, if the input reference shifts by +100ns, the proportional term will adjust the SF by -0.25bits/ns * 100ns = -25 bits. Each SF bit corresponds to $1{:}10^{-12}$ of the operating frequency, and so the PRS10 frequency will be shifted by about -25×10^{-12}. The integral term will begin ramping by (-0.055bits/hour/ns) * 100ns, or by -5.5 bits per hour. The phase shift between the 1pps input and 1pps output will be gradually eliminated.

(Phase jumps of 100ns are quite common on 1pps outputs from GPS receivers, which are a likely 1pps reference to the PRS10. The corresponding frequency jumps of 25×10^{-12} may be excessive in some applications, and so a digital pre-filter is used to smooth the time-tag values before they are used by the PLL algorithm. See LM command.)

PLL Table for all PT values, assuming a stability factor, ζ=1.

PT Parameter Parameter set by PT command	Integrator Time-Constant (hours)	Integral Gain (SF bits per hour per ns of time-tag)	Proportional Gain (SF bits per ns of time-tag)	Natural Time-Constant Characterizes PLL response (hours)
0	0.07	-14.063	-3.95	0.14
1	0.14	-7.031	-2.80	0.20
2	0.28	-3.516	-1.98	0.28
3	0.57	-1.758	-1.40	0.40
4	1.14	-0.879	-0.99	0.56
5	2.28	-0.439	-0.70	0.80
6	4.55	-0.220	-0.49	1.12
7	9.10	-0.110	-0.35	1.59
8	18.20	-0.055	-0.25	2.25
9	36.41	-0.027	-0.17	3.18
10	72.82	-0.014	-0.12	4.50
11	145.64	-0.007	-0.09	6.36
12	291.27	-0.003	-0.06	8.99
13	582.54	-0.002	-0.04	12.72
14	1,165.08	-0.001	-0.03	17.99

PF?
PF{value} 0 ≤ value ≤ 4 ; (value:ζ) : (0:1/4, 1:1/2, 2:1, 3:2, or 4:4)
PF!
PF!?

Phase-lock stability factor. This command is used to set the stability factor, ζ, of the 1pps PLL. The stability factor is equal to $2^{(value-2)}$. The default value is 2, which provides a stability factor of $2^{(2-2)} = 2^0 = 1$. Stability factors can range from 0.25 to 4.0. **Example: PF 1** sets the stability factor to 0.5, which will reduce the equivalent noise bandwidth of the PLL at the cost of increasing the ringing near the natural frequency (relative to the default settings). **PF?** will return the current value of the stability factor parameter. **PF!** may be used to write the current stability factor to the EEPROM for use as the new default. **PF!?** may be used to read the value of the stability factor which is stored in EEPROM.

PI?
PI {value} -2000 ≤ value ≤ 2000

Phase-lock integrator. This command is used to set the value of the integral term in the PLL's digital filter. It is not necessary to set this value, as it will be initialized by the PLL routine to the current frequency setting parameter when the PLL begins. Users may want access to the value to alter the PLL characteristics, or to investigate its operation. **Example: PI 0** will set the integrator in the PLL's digital filter to 0, which is the center of the ±2000 bit range. **PI?** will return the current value of the PLL integrator. (There are two terms which control the phase locking of the PRS10 to an external 1pps source: the integral term and the proportional term. The proportional term is equal to the value returned by an **SF?** minus the value returned by the **PI?**.)

Analog Control

SD{port}?
SD{port,value} 0 ≤ port ≤ 7 and 0 ≤ value ≤ 255 (factory only)
SD{port}!
SD{port}!?

Set DAC. This command is used to set (or read the settings of) an octal 8bit DAC which provides analog signals to control systems parameters. The command which sets values is only available to the factory. The command to query values may be used by all. The query command returns a single integer in the range of 0 to 255.

Port	Function
0	Controls the amplitude of the RF to multiplier in resonance cell
1	Controls the analog portion (0 to 99 ns) of the delay for the 1pps output

2	Controls the drain voltage for the discharge lamp's FET oscillator
3	Controls the temperature of the discharge lamp
4	Controls the temperature of the 10 MHz SC-cut crystal
5	Controls the temperature of the resonance cell
6	Controls the amplitude of the 10 MHz oscillator
7	Controls the peak deviation for the RF phase modulation

Example: SD2? could return the value 255 indicating that the unit has set the discharge lamp's FET drain voltage to the maximum (which it does while it is trying to start the lamp.)

The SD{port}! is a factory only command which writes the data from the corresponding SD port to the unit's EEPROM for use on subsequent restarts. **Example: SD3!?** will return the start-up value for SD3 (lamp temperature control value) which is stored in the unit's EEPROM.

Analog Test Voltages

AD{port}? port = 0,1,2,...15
Analog to digital. This command reads the voltage at the corresponding 12-bit ADC port and returns the voltage as a floating point number. Values can range from 0.000 to 4.998. The voltages correspond to various test points in the system per the following table. Note that this command can only query. **Examples: AD10?** could return the value 0.710 indicating that the case temperature sensor is at 71 °C (this sensor indicates a temperature which is about midway between the baseplate temperature and the lamp temperature.)

Command	Returned voltage
AD 0?	Spare (J204)
AD 1?	+24V(heater supply) divided by 10.
AD 2?	+24V(electronics supply) divided by 10
AD 3?	Drain voltage to lamp FET divided by 10
AD 4?	Gate voltage to lamp FET divided by 10
AD 5?	Crystal heater control voltage
AD 6?	Resonance cell heater control voltage
AD 7?	Discharge lamp heater control voltage
AD 8?	Amplified ac photosignal
AD 9?	Photocell's I/V converter voltage divided by 4
AD 10?	Case temperature (10 mV/°C)
AD 11?	Crystal thermistors
AD 12?	Cell thermistors
AD 13?	Lamp thermistors
AD 14?	Frequency calibration pot / external calibration voltage
AD 15?	Analog ground

AD{port}? 16 ≤ port ≤ 19

A/D via CPU's E-port. This command returns a value corresponding to the voltage present at the input to the microcontroller's octal 8bit ADC (port E on the MC68HC11). Only the first four ports are in use. The voltage corresponds to various test point in the system per the following table. **Example: AD17?** could return a value of 4.81 indicating that the 360 MHz RF synthesizer has acquired lock.

Command	Returned voltage
AD 16?	Varactor voltage for 22.48 MHz VCXO (inside RF synthesizer) / 4
AD 17?	Varactor voltage for 360 MHz VCO (output of RF synthesizer) / 4
AD 18?	Gain control voltage for amplifier which drives frequency multiplier / 4
AD 19?	RF synthesizer's lock indicator voltage (nominally 4.8 V when locked)

Status Bytes

ST?

Status query. This command returns the six system status bytes which are used to indicate the health and status of the unit. The values ranges from 0 to 255. The six status bytes are detailed in the tables below. A status bit will remained set until it is read, even though the condition which caused the error has been removed. Some status bits are not errors: for example, during warmup the status bytes may indicate that the lamp is not lit, temperatures are low, and the unit is not locked.

Example: Immediately after power is applied to a unit, the command **ST?** returns 16, 3, 21, 1, 2, 129. From the status byte definitions below, we see that the following conditions exist:

16… the lamp has not yet started
3… the RF VCXO has not yet locked
21… the lamp, crystal, and cells are all below their set point temperatures
1… the frequency lock has not been established
2… fewer than 256 1pps inputs have been qualified
129.. both the lamp and unit have been restarted

ST1 : Power supplies and Discharge Lamp

ST1 bit	Condition which sets bit	Corrective Action
0	+24 for electronic < +22 Vdc	Increase supply voltage
1	+24 for electronics > +30 Vdc	Decrease supply voltage
2	+24 for heaters <+22 Vdc	Increase supply voltage

3	+24 for heaters > +30 Vdc	Decrease supply voltage
4	Lamp light level too low	Wait: check SD2 setting
5	Lamp light level too high	Check SD2 setting
6	Gate voltage too low	Wait: check SD2 setting
7	Gate voltage too high	Check SD2 setting

ST2: RF Synthesizer

ST2 bit	Condition which sets bit	Corrective Action
0	RF synthesizer PLL unlocked	Query SP? verify values
1	RF crystal varactor too low	Query SP? verify values
2	RF crystal varactor too high	Query SP? verify values
3	RF VCO control too low	Query SP? verify values
4	RF VCO control too high	Query SP? verify values
5	RF AGC control too low	Check SD0? values
6	RF AGC control too high	Check SD0? values
7	Bad PLL parameter	Query SP? verify values

ST3: Temperature Controllers

ST3 bit	Condition which sets bit	Corrective Action
0	Lamp temp below set point	Wait for warm-up
1	Lamp temp above set point	Check SD3, ambient
2	Crystal temp below set point	Wait for warm-up
3	Crystal temp above set point	Check SD4, ambient
4	Cell temp below set point	Wait for warm-up
5	Cell temp above set point	Check SD5, ambient
6	Case temperature too low	Wait for warm-up
7	Case temperature too high	Reduce ambient

ST4: Frequency Lock-Loop Control

ST4 bit	Condition which sets bit	Corrective Action
0	Frequency lock control is off	Wait for warm-up
1	Frequency lock is disabled	Enable w/LO1 command
2	10 MHz EFC is too high	SD4,SP,10MHz cal,T_{amb}
3	10 MHz EFC is too low	SP, 10 MHz cal

4	Analog cal voltage > 4.9 V	Int cal. pot, ext cal. volt
5	Analog cal voltage < 0.1	Int cal. pot, ext cal. volt
6		
7		

ST5: Frequency Lock to External 1pps

ST5 bit	Condition which sets bit	Corrective Action
0	PLL disabled	Send PL 1 to enable
1	< 256 good 1pps inputs	Provide stable 1pps inputs
2	PLL active	
3	> 256 bad 1pps inputs	Provide stable 1pps inputs
4	Excessive time interval	Provide accurate 1pps
5	PLL restarted	Provide stable 1pps inputs
6	f control saturated	Wait, check 1pps inputs
7	No 1pps input	Provide 1pps input

ST6: System Level Events

ST6 bit	Condition which sets bit
0	Lamp restart
1	Watchdog time-out and reset
2	Bad interrupt vector
3	EEPROM write failure
4	EEPROM data corruption
5	Bad command syntax
6	Bad command parameter
7	Unit has been reset

Calibration Procedures

Many applications for the PRS10 only require that the frequency of the 10 MHz output be calibrated. This may be done by adjusting a potentiometer, which is accessible through a hole in the bottom of the unit. The unit should be operating for at least 24 hours before it is calibrated. The 15 turn pot has a range of ±0.020 Hz. The frequency increases if the pot is turned clockwise, by about 0.001 Hz for 3/8's of a turn.

Note: the potentiometer position will not affect the frequency of operation if : (1) it is turned to either extreme, (2) an external control voltage is applied to pin 2 of the main connector, J100, (3) an SF (set frequency) command has been sent via the RS-232 interface, or, (4) the unit is locked to an external 1pps input. The time constant for pot adjustments depend on the setting of the frequency lock-loop gain (see GA command: the default is about 2 seconds.)

In the case that the unit cannot be calibrated because the internal pot has reached an extreme position, it will be necessary to modify a calibration values which are stored in the unit's EEPROM. To verify that the pot has been turned to a limit of its motion, measure the voltage on pin 2 (POT_W) of J100 (the main connector) with respect to the chassis. Zero volts on pin 2 indicates that the pot has been adjusted for the lowest frequency, and +5.0 Vdc indicates that the pot has been adjusted for the highest frequency.

To modify EEPROM calibration values, it will be necessary to establish RS-232 communications with the PRS10. This can be done with a three wire connection between the PC COM: port and the PRS10's main connector. A communication program (see Windows Accessories or other) will be needed as well. (See MO and SP commands.)

Circuit Descriptions

Schematic RB_F1 (sheet 1 of 6)

Components shown on this schematic are located on the vertical PCB which holds the main connector to the outside. This board has a 10MHz SC-cut ovenized oscillator which is frequency locked by the microprocessor to the hyperfine transition in rubidium via a high resolution DAC. This will overcome two important shortcomings of the oscillator circuit: frequency aging of a few parts in 10^{-10}/day , and a sensitivity of a few parts in 10^{-9} over the ambient temperature range of 0°C to 65°C.

Input Power

D101 and D102 (MBRD660CT Schottky diodes in DPAKs) protect the unit from input power supply polarity reversals on +24_CLEAN and +24_HEAT. The supplies are filtered by L104 and L105 (ferrite beads with about 3µH and Q=15 at 100kHz) and C115 and C116. These filters are designed to reduce EMI emission and susceptibility but they have a low Q resonance at about 40kHz.

Voltage Reference

U100 provides a 10.00V low noise reference for the entire unit and various biases for the crystal oscillator. The reference voltage is divided by two and buffered by U102B to provide a +5.00V reference for the internal calibration pot and for the POT+ output.

Crystal Oscillator

The crystal oscillator uses a Colpitts configuration. The 3rd overtone SC-cut crystal is specified to operate at 10.0MHz with a series load of 20pF. (Hence the crystal will operate slightly above its series resonance to contribute an inductive reactance equal in magnitude to the series capacitive reactance.) At 10MHz, the network L100, L101 and C102 has a capacitive reactance equivalent to an 87pF capacitor. At the fundamental (3.3MHz) and at the B-mode frequency (10.8MHz) this network is inductive, and so there will be no gain provided by Q100. In addition to this network, C103, C104, the varactor D100, and C106 (which connects to the ac ground at the emitter of Q101) are all in series with the crystal. C104 is selected when the unit is calibrated so that the crystal will operate at 10.0MHz with the nominal EFC voltage applied to the varactor.

The crystal frequency tunes linearly with the net series reactance, with a tuning coefficient of -1Hz/20Ω. Series capacitors tune the crystal to higher frequencies, series inductors tune the crystal to lower frequencies. Only NPO capacitors are to be used and inductors should be either air or iron powder core (no ferrites) in order to preserve the relative insensitivity to ambient temperature variations. To move the oscillator to higher frequencies, $C(pF)=808/\Delta f(Hz)$. To move the oscillator to lower frequencies, $L(\mu H)=0.29\Delta f(Hz)$.

The MMBV609 varactor provides an approximate linear tuning characteristic over ±2 ppm. This will allow the unit to correct for aging of the crystal for a nominal 27 year life, given a daily aging of 2 parts in 10^{-10}.

The crystal is operated at its temperature plateau of about 80°C. (The plateau temperature is determined at calibration for each unit.) The frequency is a maximum at the plateau and so the oscillator will typically be a few hundred Hertz low when the unit is turned on at room temperature. Near the plateau top, the frequency deviation verses temperature is about $\Delta f(Hz) = -0.061x\ \Delta T(°C)^2$. Note that if the crystal oven were to lose regulation by 12.8°C (perhaps the baseplate is too hot) that this would cause a 1ppm frequency error, which could be corrected by the Rb frequency lock loop.

Power to overcome losses (to sustain oscillation) is provided by Q100. The dominate loss is the series resistance of the crystal (about 80Ω). Q100 provides power by injecting a current at the top of L100 which is in phase with the 10MHz voltage at this node. The amount of current injected depends on the size of C103 and R103: the current injected is equal to the ac voltage across C103 divided by the resistance of R103 (assuming emitter following action of Q100). The magnitude of the oscillation will grow until the peak voltage at the base exceeds the collector voltage, causing Q100 to saturate.

The circuit is designed to allow about 1mA(rms) to circulate through the crystal. The ac current is high enough to provide low phase noise, but low enough to minimize aging. This ac current is cascoded to the inverting input of the high speed op-amp, U101, by Q101. Q101 provides a good ac ground for the crystal circuit (to maintain high in-circuit Q). With an emitter current of 4mA the emitter resistance of Q101 will be about 6Ω. Q101 also helps to isolate the crystal circuit from variations from the external 10MHz load (as does U101) so that the frequency of operation of the circuit will not be pulled by the load.

The op-amp operates as a transconductance amplifier with a transconductance gain of about 2000Ω at 10MHz. The dc output of the op-amp is midway between the supplies (at about 8.25Vdc), which is controlled by the current drawn by Q101 and the value of R111. There is a 10Vpp sine at 10MHz at the output which is ac coupled, reverse terminated, and matched to a 50Ω load by C111, R114, and T100. The primary of T100 is tuned to 10MHz, so that spurs and harmonics are attenuated. The 7:2 turns ratio transforms the 50Ω into a 612Ω load at 10MHz. The output amplitude into 50Ω is 0.50Vrms (1.414Vpp or +7dBm).

Extremely low phase noise is an important specification for this oscillator. The phase noise close to carrier (10Hz offset and below) is dominated by 1/f components, including, crystal parameters, temperature stabilization, amplitude limiting, and gain mixing. Far away from carrier (>1kHz) the noise floor is determined by ratio of broadband noise sources to the signal current at 10MHz. Examples of broadband sources include the shot noise current on base currents, the Johnson noise current from bias resistors, and the op-amp's input current and voltage noise. It is also important to maintain very low noise on the EFC and amplitude

control signals. Typical phase noise is -125dBc/Hz @ 10Hz, -145dBc/Hz @ 100Hz, and -155dBc/Hz @ >1kHz.

Circuit elements and operating points were chosen to reduce noise sources. An SC-cut resonator was chosen for high Q and stable motional impedances. The transistors are operated at a few mA, trading off base bias current noise against emitter resistance. Metal film resistors are used to reduce 1/f noise. Series 100µH inductors are used to reduce the Johnson noise current of bias resistors. The op-amp was chosen for low input current noise, and it is operated with sufficient gain so that its voltage noise would not degrade the phase noise floor. Finally, the crystal is operated at its plateau temperature to reduce the frequency instability associated with temperature fluctuations.

Crystal Heater

The crystal heater has the same design as the two other heaters (resonance cell and lamp) in the system. There are two heaters in TO-220 packages: an LM340-12 (a +12Vdc voltage regulator) and a TIP107 (a pnp power Darlington). The tabs of both TO-220 heaters are at ground, so they are bolted directly to the block. All of the heater current passes through three parallel 1Ω shunt resistors to sense current. The block temperature is sensed by two series 100kΩ thermistors, which are directly beneath the TO-220 heaters in the oven block. (Two sensors are used because the division of power will depend on the heater voltage applied to the unit.) At the operating temperature of 75°C, each thermistor will have a resistance of about 15kΩ. The control circuit will allow operation up to 90°C. (For the lamp, the nominal operating temperature is 105°C, for which each thermistor will have a resistance of about 5.5kΩ. The maximum setpoint for the lamp is 122°C.) The control circuits for all of the heaters are on the top (analog) PCB. The control circuit can vary the heater current from 0 to 0.7A to maintain the set point. In the case of a control failure, the LM340-12 will turn off the current if the junction temperature reaches 125°C.

Schematic RB_F2 (Sheet 2 of 6)

The components contained on this schematic are all located on the top (analog) PCB. This board contains most of the analog circuitry for the system, including, temperature servos, photodiode amplifier and filter, analog signal multiplexers, and noise filters for the crystal's EFC and amplitude control signals.

Temperature Control Servos

There are three temperature control servos (for the crystal oven, the Rb discharge lamp, and the Rb resonance cell). The three servos are identical except for the maximum set point (122°C for the lamp, and 90°C for the others.) The circuit description will refer to the crystal temperature controller.

The controller is a proportional-integral controller. The output of the error amplifier (U200A) is used to control the current flowing in the heater circuit, with a range from 0 to 500mA (to provide heater powers from 0 to 12W). The error amplifier has a proportional gain of (R205/R204)+1=6.5 and an integration time constant of R204xC201=1 s for the signal at its non-inverting input. The inverting input is biased near 1.00Vdc, so that the servo will try to maintain the temperature so that there is 1.00Vdc on the thermistors.

For a set point of 75°C the series thermistor pair will have a resistance of 30kΩ. To get 1.00Vdc at the non-inverting input of U200A, XTAL_SET is set to 170 bits (full-scale of 4V/255=0.01568V/bit, so 170 bits=2.66Vdc).

After settling, a LSB step in XTAL_SET (15.6mV) will become about 5.8mV at the on-inverting input, and cause an immediate change of 2x5.8mV = 11.6mV at the output of U200A, followed by a ramp of 5.8mV per second. This quickly increases the power by about 0.27W, then by 0.14W/S thereafter. The servo will settle when the thermistors heat-up, decreasing their resistance, so that the voltage at the non-inverting input returns to 1.00Vdc.

The thermistor resistance decreases by about 3%/°C. An LSB increase in XTAL_SET near the nominal 2.66Vdc will cause the current to increase by .0156/(2.66-1.00) or about 0.9%. So the servo will settle when the temperature of the block increases by 0.9%/3%/°C =0.3°C.

There is a small temperature offset between the temperature sensor and the device whose temperature we wish to control. Since the sensor is located very near the heat source, the sensor will be warmer, and the temperature offset will increase as more heat is required. To compensate for this effect, a small portion of a voltage proportional to the baseplate temperature (10mV/°C) is summed to the voltage at the inverting input of the error amplifier. This is the electronic equivalent of a double oven, as the errors due to changes in ambient temperature are greatly reduced.

U200B controls the current in the heaters in proportion to the signal from error amplifier (U200A). When the output of the error amplifier goes up, the output of U200B goes down, increasing the current in the heaters, causing the signal XTAL_SHUNT- to go down. The gain (from error amplifier to shunt voltage) is set by R207 and R208. Offsets are arranged so that the heaters will be off when the output of the error amplifier is less than +5Vdc.

Conversion to 10MHz TTL

U205 converts a 10MHz offset sinewave from the crystal oscillator into complimentary 10MHz TTL level signals. The +10MHZ signal is used as a reference for the microwave frequency synthesizer and the -10MHZ signal is used as a clock for the microprocessor. Separate signals are used to improve the isolation between the CPU and the synthesizer.

The 10MHz sine has an offset of 8.2Vdc and an amplitude of 10Vpp and is sourced via a 2.0kΩ resistor. After attenuation by R249, R250 and C210, the non-inverting input to U205

sees a signal with 0.91Vdc offset and an amplitude of 0.91Vpp, while the inverting input is biased at 0.91Vdc.

Photocell Amplifier

The output from the photocell is a sink current which is proportional to the light intensity of the discharge lamp as attenuated by the resonance cell. The light transmission through the resonance cell decreases slightly (by about 1 part in 1000) when the microwave synthesizer sweeps through the hyperfine transition frequency. The microwave frequency is modulated at 70Hz, so the light output will dip at 140Hz when centered on the hyperfine transition.

The S/N of the photocell is limited by shot noise: the shot noise current on a dc current of I amps is given by $\sqrt{(2qI)}$ (amps/$\sqrt{Hz}$) where $q=1.6x10^{-19}$. On a 50µA dc current the best we can do is 4pA/$\sqrt{Hz}$ of noise. A good design requires that the shot noise be the dominate noise term.

U206A is a low noise bipolar input op-amp whose input range includes ground. A 150kΩ metal film resistor shunted by a 1nF film capacitor is used in feedback, providing a transconductance bandwidth of 1kHz. The input current noise of the op-amp (0.4pA/$\sqrt{Hz}$) and the Johnson noise current of the feedback resistor (0.33pA/$\sqrt{Hz}$) are not important noise terms. Also, the voltage noise of the op amp (3nv/$\sqrt{Hz}$) times the noise gain (which is about 10x for a photocell whose shunt resistance is 1MΩ at 25°C, but drops to 15kΩ at the operating temperature of 80°C) is not important as the expected shot noise current times the transconductance gain is about 600nV/$\sqrt{Hz}$.

The transconductance amplifier is followed by a high gain amplifier (x288 for ac signals). This amplifier has a pass band from 16Hz to 1.6kHz. The non-inverting input to this amplifier is biased to place the output of the following bandpass filter at midscale.

A two-pole Butterworth low pass filter (300Hz bandwidth) is used to reduce noise at the A/D input, while preserving gain between 70Hz and 140Hz. The filter has a gain of 1.59 for signals in the pass band.

The input voltage noise specifications for the high gain and filter amplifiers are not particularly important as there is about 600nV/$\sqrt{Hz}$ of noise on the output of the transconductance amplifier. With an noise equivalent bandwidth of about 400Hz, we expect a total noise (from the shot noise of the photocell's dc current) of about 3.4mVrms or about 17mVpp. This is much larger than the LSB (1.25mV) of the A/D converter, so the quantization noise of the A/D will not be important.

Signal Filters for Oscillator Control

The amplitude and frequency of the crystal oscillator are controlled by signals from D/A converters. In order to preserve low phase noise, these signals must have very little voltage noise.

The EFC signal has a full scale of 17Vdc, and a resolution of 22 bits. A LSB represents a step of about 4μV which is a fractional frequency step of about $1{:}10^{-12}$. We would like for noise on the EFC to be less than one LSB. To arrange this, the DAC22 signal is filtered with a time constant of 1s and buffered by a FET input op-amp (U210B, an AD822). The FET op-amp has 1/f noise of about 2μVpp in the two decade band from 0.1Hz to 10Hz. Both the op-amp and the 10.0kΩ feed back resistor will have noise of about 30nV/√Hz at 10Hz, which is well under the target of 1.6μV/√Hz required to meet the specification of -125dBc/Hz at 10Hz offset.

The oscillator's amplitude control is filtered is a similar fashion, using U210A. Noise on this signal would be detrimental to the phase noise spectrum, but would not affect zero-crossings of the sine output.

Analog Multiplexers

There are 16 analog signals which may be multiplexed to the 12-bit A/D converter. One of these signals, PHOTO_AMP, is be digitized 32 times during each cycle of the 70Hz modulation (2240 Hz) in order to lock the crystal to the Rb hyperfine transition. The other 15 signals are monitored intermittently and in response to RS-232 requests.

A0	Amplified and filtered photocell signal
A1	Photocurrent (x150kΩ/4) (37.5mV/μA)
A2	Case temperature (10mV/°C)
A3	Crystal thermistor voltage
A4	Resonance cell thermistor voltage
A5	Lamp thermistor voltage
A6	Calibration voltage (Pot or user input)
A7	Signal Ground
B0	J204 (Spare)
B1	+24_HEAT/10
B2	+24_CLEAN/10
B3	Discharge lamp FET's drain voltage
B4	Discharge lamp FET's gate voltage
B5	Crystal heater control signal
B6	Resonance cell heater control signal
B7	Discharge lamp heater control signal

Schematic RB_F3 (Sheet 3 of 6)

All of the components shown on this schematic reside on the vertical PCB on the left side of the unit. The large hole in this PCB allows access to an SMB connector to sample the microwave field in the resonance cell.

Power on reset, low voltage protection, and a watch-dog time-out is provided by U300, a MAX705. The RESET input to the microcontroller is asserted on power-up. The reset will be asserted for about 1 second after power is applied (to allow time for the 10MHz crystal oscillator to start.). A non-maskable interrupt (XIRQ) is asserted if the SPI clock is inactive for more than 1.6 seconds, which should never occur. A maskable interrupt (IRQ) is asserted (which will also retrigger the reset cycle) when the +18V supply drops below 16.0Vdc.

Microcontroller

The system is controlled by U302, a MC68HC11E9, which is an 8-bit microcontroller with RAM, ROM, EEPROM, A/Ds, UART, serial interface, timers, and I/O control bits. The controller is clocked by the 10 MHz timebase which is to be disciplined to the atomic transition frequency.

The microcontroller communicates with external devices via a the serial peripheral interface (SPI). Data is clocked by SPI_CLK to (or from) these devices on SPI_DATA. To reduced digital crosstalk to the most sensitive devices, the SPI data and clock are gated, so that these outputs are only active when necessary.

The microcontroller is also responsible for a variety of housekeeping tasks: power on circuit checks, setting and reading temperatures, boost-starting the discharge lamp, digitally filtering the frequency-lock error signal, passing the filtered error signal to the 22 bit D/A converter, and responding to commands and queries via the RS-232 interface.

A description of I/O from the controller follows:

Name	Function
CLK	10MHz TTL clock input
RESET	TTL low to assert system reset
XIRQ	Non-maskable interrupt on watch-dog time-out (SPI dead)
IRQ	Maskable interrupt on power failure (+18 goes below +16V)
MODA	Configure for internal program memory
MODB	Configure for internal program memory
PORT A	Mixed inputs and outputs
PA0	Time tag input to measure 1PPS input to 400ns
PA1	Interpolation input to measure 1PPS input to 0.2ns

PA2	ADC_BUSY input is high during 12-bit A/D conversions
PA3	MAG_SIGN output controls sign of magnetic field
PA4	-CONV strobe low to initiate 12-bit A/D conversion
PA5	EN/-CLR control for 1PPS time-tagging
PA6	1PPS output strobe (400ns resolution)
PA7	Spare output (connected to J305)
PORT B	Eight TTL outputs
PB0	MPX0 Select bit for analog multiplexer
PB1	MPX1 Select bit for analog multiplexer
PB2	MPX2 Select bit for analog multiplexer
PB3	MPX3 Low to select MPX-A, high for MPX-B
PB4	1PPS_SEL0 Low bit for 100ns 1PPS output delay
PB5	1PPS_SEL1 High bit for 100ns 1PPS output delay
PB6	Spare (connected to J306)
PB7	LOCKED bit is set high to indicate Rb frequency lock
PORT C	Chip select outputs
PC0	-CS_PLL
PC1	-STB_DAC8
PC2	-CS_EFC_HIGH
PC3	-CS_MAGNET
PC4	Spare (connected to J308)
PC5	-CS_EFC_LOW
PC6	-CS_PHASE_MOD
PC7	EN_ADC_CLK
PORT D	SPI and RS-232
PD0	RS-232_IN
PD1	RS-232_OUT
PD2	SPI_IN
PD3	SPI_DATA
PD4	SPI_CLK
PD5	SPI_GATE
PORT E	Octal 8-bit A/D converter with +5.12V full-scale
PE0	RF_XVCO. Should be between 0.2 and 3.5Vdc
PE1	RF_VCO. Should be between 3.0 and 4.0Vdc
PE2	RF_AGC. Should be 1.0 and 3.75Vdc

PE3	PLL_LOCK. Should be >4.0Vdc
PE4	Ground
PE5	Spare analog input (J302 with 100kΩ to ground)
PE6	Spare analog input (J303 with 100kΩ to ground)
PE7	Spare analog input (J304 with 100kΩ to ground)

RS-232

The system may be controlled by commands sent via the RS-232. Two pins on the system connector (J100) are used for transmit and receive. Data is sent to the host on pin 4, received from the host on pin 7. The baud rate is fixed at 9600 baud, 8 bits, no parity, with 1 start and 2 stop bits. No DTR or CTS controls have been used, rather, the XON/XOFF protocol has been implemented. The transmit drive level is 0 and 5V, not the +/-12V normally associated with RS-232. These levels are compatible with RS-232 line receivers, but does not require their use (a TTL inverter may be used instead), hence simplifies the interface when used inside an instrument at the sacrifice of degraded noise immunity over long lines.

12 Bit A/D Conversion

A serially interfaced 12 bit A/D converter is used to measure the ac and dc components of the photocell signal. The analog input to the ADC is buffered by U309A, a FET input op-amp configured as a unit follower. The quantization noise of this converter will not degrade the S/N of the ac signal, even in the case when the ac signal occupies a relatively small portion of the converter's full scale range. The A/D converter can also measure the position of a 10 turn "user cal" pot, which has a (software defined) range of +-2E-9. The 12 bits of resolution will provide a frequency trim of 1E-12.

12-Bit Digital to Analog Converters

There are four 12-bit DACs. Two of the DACs are scaled, summed, and offset to provide a level with 22-bits of resolution to control the crystal frequency. One of the DACs is used to control the magnitude of the magnetic field in the resonance cell. The forth DAC is used to digitally synthesize the 70Hz phase modulation of the 6.834GHz microwave field.

Two of the DACs (the upper DAC of the 22-bit pair and the DAC which controls the magnetic field) are rarely changed and would be very sensitive to digital crosstalk and so are communicated with via the gated SPI interface.

Magnetic Field Control

R331, a 348Ω shunt resistor, is used to measure the current through the magnetic field coil which is in the resonance cell. U307B, an LM358 op amp, maintains a current through the field coil so that the voltage across the shunt resistor matches the output from the 12-bit DAC (U310, an LTC1452). The coil current can be programmed from 0 to 8mA, but a minimum level (3mA) is always maintained to spread out the non 0-0 Zeeman transitions. The

frequency offset is quadratic in the field strength, with a fractional frequency resolution of about $1x10^{-12}$ at 3mA, and of $2.5x10^{-12}$ at 8mA.

To reduce the susceptibility of the transition frequency to external magnetic fields, the polarity of the magnetic field is chopped at 5Hz by the CPU control signal (MAG_SIGN) and U306 (a DG211 quad analog switch). The apparent transition frequency is synchronously filtered by the CPU over the field reversal period so as to notch out any 5Hz noise from the EFC signal.

Phase Modulation

The main task for the microcontroller is to modulate the microwave carrier to sweep through the Rb hyperfine transition frequency. The microcontroller will A/D the optical signal via a 12 bit A/D converter, synchronously detect the components of the optical signal at the sweep rate and at twice the sweep rate, and adjust the frequency of the 10 MHz timebase so as to null the component at the sweep rate (which keeps the optical dip centered in the middle of the sweep).

The CPU digitally synthesizes the 70Hz sinewave which phase modulates the RF frequency synthesizer. U313, an 12-bit DAC, outputs 32 samples during each cycle of the 70Hz sinewave. The amplitude of the sinewave is controlled by the signal "PHASE_DEV", which comes from an 8-bit DAC on the frequency synthesizer PCB. The amplitude of the sinewave controls the magnitude of the frequency deviation (which is adjusted to optimize the deviation sensitivity of the resonance cell). The frequency deviation is about ±300Hz at 6.834GHz.

1PPS Output

A port bit on the microcontroller (PA7) may be used to output a 10µs pulse at a rate of 1Hz. This pulse is combined with the LOCK output signal on the main connector (pin 1 of J100). (The function of the LOCK/1PPS output may be configured via RS-232.)

This port bit is controlled by the microcontroller's timer which has a resolution of one E_CLK cycle (400ns). Hardware on the bottom circuit board provides delays in 100ns steps (under control of the port bits 1PPS_SEL0 and 1PPS_SEL1) and in steps of about 0.5ns via an analog signal from an 8-bit DAC. The combination of these three delays allows the 1PPS output pulse to be placed with an accuracy, resolution, and differential non-linearity of about 1ns.

1PPS Input Time-Tag

The rising edge of a 1PPS input signal on pin 5 of the main connector can be time-tagged with 1ns resolution. The time may reported via RS-232, or used to servo the unit to another frequency standard (such as GPS).

Hardware on the bottom board provides two signals: TIME_LATCH and INTERPOLATE. These signals latch the value of a free-running counter (clocked by the E_CLK) which is part of the microcontroller. TIME_LATCH is just the 1PPS input re-synchronized to the CPU's E_CLK, which allows the processor to time-tag the input to 400ns resolution. INTERPOLATE will go low for a time equal to about 2000 times the interval between the 1PPS input and the next E_CLK. Measuring the duration of INTERPOLATE allows the position of the 1PPS input to be measured to about 400ns/2000=0.2ns.

Schematic RB_F4. (Sheet 4 of 6)

High Resolution, Low Phase Noise, RF Synthesizer

The pressure tuned Rb hyperfine transition lies at about 6,834,685,850Hz. This will vary depending on the fill pressure and gas composition of the Rb resonance cell. In order to lock the crystal oscillator to this transition, we need to synthesize and sweep frequencies in this region.

In order to minimize the amount of magnetic field tuning needed, the frequency synthesizer should be capable of being set with high resolution (about $1{:}10^{-9}$). In order to detect the transition with good signal to noise, the synthesizer will need to have very low phase noise (on the order of -70dBc/Hz at 6.8GHz).

Since we want to stabilize a 10.000MHz crystal to an (essentially) arbitrary frequency with low phase noise, we will need a dual loop synthesizer: a fast loop to stabilize an RF VCO to a crystal (for good phase noise), and a slow loop to stabilize the crystal to the 10.000MHz reference.

Typical numbers:

A typical microwave frequency is 6,834,685,853Hz
Which is the 19th harmonic of the RF frequency: 359,720,308Hz
Which is 16 times the crystal frequency: 22,482,519Hz
In this case, dividing the RF frequency by (1386*64+39)=4053.5Hz
Which equals the reference frequency (10,000,000Hz) divided by 2467.
The dual modulus frequency synthesizer will be programmed with R=2467, N=1386, and A=39.

The microwave frequency is generated by frequency multiplication of the RF frequency in a step recovery diode (SRD). The RF frequency was chosen to give good conversion efficiency, with favorable "numerology" (so that the gaps between available frequency steps from the dual modulus synthesizer are small).

A reasonable crystal frequency is the RF frequency divided by 16 (dividers and oscillator/mixers are available in this frequency range). A third overtone crystal resonator with a nominal frequency of 22.48252MHz is used to provide a low-noise "flywheel". We

only need to tune over a range of 0.1ppm to accommodate for fill pressure variations of the resonance cell.

The varactor tuned crystal oscillator has a tuning coefficient of about 2 ppm/V. The RF VCO is phase locked to this oscillator by a mixer/loop filter combination with a high natural frequency (about 400,000r/s), a high comparison frequency (22.48MHz), and a damping factor of one. Low noise components (metal film resistors, film capacitors and an OP27 op amp) help achieve the low phase noise.

The varactor for the crystal is tuned by the dual modulus frequency synthesizer (U400, an MC145190) which compares the divided reference (10.00MHz) to the divided RF (at about 359.72MHz). Since large divisors must be used to achieve the high frequency resolution, the comparison frequency will be low (a few kHz), but the crystal oscillator provides good frequency stability in spite of the low comparison rate.

The gain of U400's phase detector may be set (coarsely) by the CPU, and it is adjusted to maintain roughly the same PLL damping factor as divisors are changed. This loop has a very low natural frequency (about 10 r/s) and a damping factor which ranges from 0.84 to 1.19.

After multiplication to 6.834GHz, the phase noise has been measured at -72dBc/Hz. This is low enough so that the S/N of the dip signal is not adversely affected by the microwave phase noise.

RF Output Amplifier

The 359.720MHz RF must be amplified to drive the SRD. It is important to maintain a constant RF level, optimized to provide a large frequency deviation sensitivity and immunity to RF level variations.

The variable gain output amplifier is designed to provide a conjugate match of Q400 (an MFR5812 medium power RF transistor) to the 50Ω source (U404, the VCO) and to the 50Ω load (the SRD, which has its own matching network).

The gain of Q400 is adjusted by changing its dc collector current. U406A compares the DAC signal (RF_LEVEL) to the rectified RF current in the SRD (which is the dc current sourced by R444). If the detected RF is low, the output of U406A will ramp up, increasing the output of U406B, which increases the base current to Q400, increasing the available power from Q400. The output of U406A linearly controls the collector current of Q400 from 0 to about 35mA. U406A's output settles when the detected RF signal on R444 is exactly 1/10th of the RF_LEVEL DAC signal.

Step Recovery Diode Matching

The output of the RF amplifier is connected to the SRD via an SMB connector. The SRD can be modeled at RF frequencies and at our drive level as a resistor (20-40Ω, depending on

drive level) with a shunt capacitor (about 1pF) and a series inductor (a few nH). Matching (for best return loss) is achieved by adding a shunt capacitor (5pF) across the SMB and with a series inductor (10nH) to the SRD.

The SRD is inside the mu-metal can which encloses the resonance cell and photodetector. The can is not resonant at the microwave frequency (as is common practice), and so there is no need to tune the length of the cavity or worry about the affect of coming off resonance. Sufficient field strength at 6.834GHz is available without resonant enhancement due to the high RF drive frequency and efficient coupling into the SRD.
The SRD loop is oriented inside the can in such a way as to minimize the drive level required for a good hyperfine optical signal.

Analog Control

Various analog voltages are provided by an octal 8-bit DAC to control temperatures, intensities, and for system tests. U407, a TLC5628, is connected to the microcontroller via the gated serial interface. Each of the eight analog outputs may be set from 0 to 4.00V with 10mV resolution. (Except for the PHASE_DEV output, which has a full scale of 2.00V and a step size of 5mV.) The outputs are dedicated as follows:

OUTPUT	NAME	DESCRIPTION
A	RF_LEVEL	Controls the RF power level to the SRD
B	1PPS_DELAY	Analog control of 1PPS output delay (0.5ns/bit)
C	LAMP_DRAIN	Drain voltage (x6) to lamp FET
D	LAMP_TSET	Controls the lamp temperature (Tmax=122°C)
E	XTAL_TSET	Controls the crystal temperature (Tmax=90°C)
F	CELL_TSET	Controls the cell temperature (Tmax=90°C)
G	OSC_AMPL	Controls the 10.00MHz output amplitude
H	PHASE_DEV	Controls the frequency deviation of RF

Schematic RB_F5 (Sheet 5 of 6)

Power Supply, Lamp Control and 1PPS Timing PCB

Components shown on this schematic are located on the bottom PCB. Three TO-220 power regulators are mounted to the back wall of the device.

Linear Power Supplies

All of the power supplies operate from the +24_CLEAN input (pin 9 of the main connector). U503, an LM317 adjustable voltage regulator, is used to supply +18Vdc to the system. The +18V is used on the analog PBC, on the frequency synthesizer, for the crystal oscillator, and for the analog switches and ADC buffer on the CPU PCB.

U504, an LM340-5 three terminal regulator is used to provide +5.0Vdc. This supply is used for all logic circuits and for analog circuits which interface to analog devices which must not be driven above their logic supplies.

Lamp Regulator

A discharge is ignited and maintained by a MOSFET powered oscillator operating at about 150MHz inside the lamp enclosure. It is very important that the voltage provided to the lamp circuit be well regulated, as the lamp intensity is nearly proportional to this voltage. Since the synchronously detected light signal at 70Hz is used to lock to the hyperfine transition, noise at 70Hz will add noise to the frequency lock-loop. Also, noise at other frequencies may be heterodyned by the 2ω signal (140Hz), which is really a modulation of the attenuation of light through the resonance cell. For example, if the power supply has noise at 210Hz, the lamp will have an intensity fluctuation at 210Hz, which when mixed by the 140Hz attenuation modulation will create a component at 70Hz, which will interfere with the frequency lock loop.

Long term stability (thermal and aging) of the lamp voltage regulator is also important. The voltage provided to the lamp oscillator affects the operating conditions of the lamp (temperature, Rb vapor pressure, and discharge intensity) which will affect the apparent hyperfine transition frequency.

The drain voltage and current are controlled by the lamp regulator. The gate voltage to the MOSFET is controlled so that the drain current is about 60mA + (10mA/V)*V_{drain}. The gate voltage is supplied by U502B which measures the drain current through the shunt resistors R504, R505, R552 and R553. The offset and slope of the drain current vs. drain voltage is set by R510 and R511.

The drain voltage is controlled by an 8bit DAC whose output is multiplied by 6 and buffered by U502 and Q500. An adjustable regulator, U501, is bootstrapped at 1.75Vdc above the drain voltage. This regulator will provide the drain current for drain voltages above 6.25Vdc. When the drain voltage is set below 6.25Vdc, the drain current is sourced from a +8V regulator, which is part of the lamp heater circuit. (This is done to reduce the power required by the unit by redirecting the heat of the regulator to the lamp block which needs to operate at a high temperature.)

To start the discharge, the drain voltage to the MOSFET is set to about 20Vdc, which is regulated from the +24_HEAT supply. The drain voltage is reduced to about 5V after the lamp starts.

1PPS Input Time-Tag

The rising edge of a 1PPS input signal on pin 5 of the main connector can be time-tagged with 1ns resolution. The time may reported via RS-232, or used to servo the unit to another frequency standard (such as GPS).

Hardware on this board provides two signals: TIME_LATCH and INTERPOLATE. These signals latch the value of a free-running counter (clocked by the E_CLK) which is part of the microcontroller. TIME_LATCH is just the 1PPS input re-synchronized to the CPU's E_CLK, which allows the processor to time-tag the input to 400ns resolution. INTERPOLATE will go low for a time equal to about 2000 times the interval between the 1PPS input and the next E_CLK. Measuring the duration of INTERPOLATE allows the position of the 1PPS input to be measured to about 400ns/2000=0.2ns.

The E_CLK is synchronized to the 10MHz clock, and four phases are generated by U500, an octal latch. E_0 is used to synchronize EN/-CLR (U506A), and E_90 is used to arm the time-tagging circuit (U507A). A gate pulse (the output of U507B) will start with the first 1PPS input after U507A is set, and end synchronously with the first E_180 rising edge after the first E_90 rising edge after the 1PPS input. This will generate a gate pulse of 100ns to 500ns duration that is a measure of the position of the 1PPS input relative to the E_CLK.

The width of the gate pulse is multiplied by a factor of about 2000 by the pulse stretcher circuit. Initially, C509 is charged to 11.4Vdc. C509 is rapidly discharged by Q502's collector current (about 10.8mA) during the gate pulse, driving the output of the comparator (U509) low. C509 is then recharged by Q501, a 5.4µA constant current source. When C509 reaches 11.0V, the output of the comparator goes high. The ratio of the collector currents of Q501 and Q502 sets the stretch multiplier.

The circuit is temperature compensated against variations in the transistors' base-emitter voltages as both the charge and discharge currents are equally affected by their junction temperature, leaving the ratio unchanged.

1PPS Output Pulse Delay

A port bit on the microcontroller (PA7) may be used to output a 10µs pulse at a rate of 1Hz. This port bit is controlled by the microcontroller's timer which has a resolution of one E_CLK cycle (400ns). Hardware on this circuit board provides delays in 100ns steps (under control of the port bits 1PPS_SEL0 and 1PPS_SEL1) and in steps of about 0.5ns via an analog signal from an 8-bit DAC. The combination of these three delays allows the 1PPS output pulse to be placed with an accuracy, resolution, and differential non-linearity of about 1ns.

The 1PPS port bit from the CPU is synchronized to E_0 by U506B, then synchronized and delayed by U500. The multiplexer, U510, selects one of the four phases of the 1PPS output, delayed in steps of 100ns by the 10MHz clock.

The selected 1PPS pulse may be delayed by an analog control signal. C513 is charged to a level of $10+V_{dac}/2$ by Q503's collector current, which turns on D503, connecting C513 to the output of U512B. The selected 1PPS output turns Q503's current down, and turns Q504's current up, discharging C513. As C513 passes through 9.0Vdc, the comparator output (U514) is forced low. C513 continues to discharge down to $8- V_{dac}/2$, where it stays until the 1PPS

pulse goes low. When the 1PPS pulse goes low, the process is reversed, and Q504's current is reduced while Q503's current is increased, charging C513 back towards $10+V_{dac}/2$. This time, as C513 passes through 9.0V, the comparator's output is set high. In this way, both the leading and trailing edges off the 1PPS output are delayed the same amount.

Baseplate Temperature Sensor

U505, an LM45 centigrade temperature sensor, has an output of 10mV/°C. This sensor is in thermal contact with one of the baseplate standoffs that hold the thermal shield which encloses the lamp. The sensor's output may be read by the CPU via the 12-bit DAC so that the baseplate temperature may be read with 0.125°C resolution.

The output of the temperature sensor is also used to tweak the setpoints of the temperature control servos, which will reduce the affect of ambient temperature changes on the temperatures of the lamp, resonance cell, and crystal ovens.

Schematic RB_F6 (Sheet 6 of 6)

Resonance Cell and Lamp Heaters

The heater and control circuits for the lamp and resonance cell are identical to the circuit described for the crystal oscillator. (See Sheet 1 of 1.) The resonance cell heaters (U600 and Q600) are located on the back of the resonance cell. The lamp heaters (U800 and Q800) are located on the bottom of the lamp block. The other passive components are located on the small vertical PBCs attached to the back of the resonance cell and lamp blocks. The control circuits of the heaters are located on the top PCB.

Resonance Cell

Components shown inside the resonance cell include: L700, a 50 turn magnetic field coil, D700, the SRD with its input matching network mounted on an SMB connector, and D701, the photodiode. Another SMB connector, J701, is used to pick-up some of the microwave field to allow diagnostic tests with an RF spectrum analyzer.

Discharge Lamp

A plasma discharge is maintained inside a small bulb (filled with a few Torr of an inert gas and some Rb metal) by an RF oscillator. The oscillator operates at about 150MHz, with a peak-to-peak voltage of about 10 times the dc voltage applied to the FET's drain.

Q900, an MRF134 medium power n-channel FET, is used as the active element in the oscillator circuit. This part is characterized for operation at +28Vdc and 150MHz, and is rated for a dissipation of 9.5W (derated for our 105°C operation). Our most severe operation is during lamp ignition, with an total input power of about 3.2W. The total input power

during normal operation is 0.5W. (The power dissipated in the MRF134 is probably about 1/2 the total input power.)

The oscillator current circulates through the series LC network consisting of C903-906 and L903. The coil, L903, is in contact with the bulb. The high voltage end of the coil connects to C905. When oscillating, the drain of the FET swings between ground and twice the dc drain voltage. C903 is in parallel with the FET's drain-source capacitance (about 10pF), for a total capacitance of 78pF (or a reactance of about –j13.6Ω at 150MHz). With a drain voltage of 20Vdc, the drain will have about 40V peak-to-peak, so there will be a circulating current of 2.9A, peak-to-peak. The series capacitance of C904/C905 is 9pF (a reactance of about -j118Ω), so they will have about 340Vpp across the pair (due to the circulating current), which is in phase with the 40Vpp drain voltage, for a total of 380Vpp at the top of the coil.

It is very important that C903-906 be very low loss and high stability capacitors. Porcelain capacitors are used in this circuit: they have Qs of about 500, for ESRs of about 0.03Ω (for the 56pF part at 150MHz). Low loss is important to reduce self-heating (which can destroy other types of capacitors), and high stability is important to maintain a constant discharge intensity.

The operation of the oscillator depends somewhat on the conditions of the discharge. Over certain temperature ranges (which are carefully avoided) the losses caused by the discharge can quench the oscillation, which stops the discharge, which allows the oscillation to start again. This cycle can occur at several kHz, which makes frequency locking impossible.

Schematic RB_F7 (Sheet 1 of 1)

Connector Interface Board (Not part of standard product)

This board is not part of the standard product and is available from the factory at and additional charge. It is intended to facilitate customer evaluation of the product by adapting the standard product's interface connector to connector types which are more readily available in the laboratory (such as BNCs and DB9 for RS-232).

This board connects to the outside of the unit. Three BNCs are used to source 10MHz and the 1PPS outputs, and to receive the 1PPS input. A DB9(female) allows direct connection to a computer (usually via COM2:). A 2.1mm power connector allows the unit to be connected to a standard +24V/2.5A power supply (center conductor must be positive).

The 10MHz output should be terminated into a 50Ω load. The output will be about 0.5Vrms (about 1.41Vpp).

The RS-232 interface uses CMOS logic levels (0V and +5V) which will work with standard RS-232 line drivers and receivers. The ±12V of the standard RS-232 line driver will not harm the logic input, and the 0/+5V RS-232 output from the rubidium standard will work with virtually all computers, provided the cable is less than 25 feet long. The RS-232 control lines, CD, DSR and CTS are all pulled high via 10kΩ resistors. An XON/XOFF protocol is used to pause communications as needed.

The LOCK/1PPS function may be configured via RS-232. The factory default is a low level to indicate lock, with a 10μs pulse to +5V at 1PPS, with the leading edge being defined as the 1PPS timing reference. This BNC output is a CMOS logic output via a 1kΩ resistor. LEDs are used to indicate +24 power (electronics and heaters), lock status, and RS-232 data received and RS-232 data transmitted.

Appendix A: Frequency Synthesizer Table

This table provides a list of frequency synthesizer parameters and the frequency offset relative to the settings for a nominal cell. Also listed is the frequency step between adjacent settings.

This information is needed to calibrate units which have aged by more than ± $2x10^{-9}$, or in the case that an application may require operating the unit at a frequency up to 0.6Hz away from 10MHz.

Number	R	N	A	f-fo(Hz)	df(hz)
1	6900	3878	15	0.000000	
2	6757	3797	55	-0.005963	0.005963
3	6614	3717	31	-0.012183	0.006220
4	6471	3637	7	-0.018678	0.006495
5	6328	3556	47	-0.025467	0.006789
6	6185	3476	23	-0.032570	0.007103
7	6042	3395	63	-0.040009	0.007439
8	5899	3315	39	-0.047809	0.007800
9	5756	3235	15	-0.055996	0.008187
10	5613	3154	55	-0.064600	0.008604
11	5470	3074	31	-0.073654	0.009054
12	5327	2994	7	-0.083195	0.009540
13	5184	2913	47	-0.093261	0.010067
14	5041	2833	23	-0.103899	0.010638
15	4898	2752	63	-0.115158	0.011259
16	4755	2672	39	-0.127094	0.011936
17	4612	2592	15	-0.139771	0.012676
18	4469	2511	55	-0.153258	0.013488
19	4326	2431	31	-0.167638	0.014379
20	4183	2351	7	-0.183000	0.015362
21	4040	2270	47	-0.199450	0.016450
22	3897	2190	23	-0.217108	0.017657
23	3754	2109	63	-0.236110	0.019002
24	3611	2029	39	-0.256618	0.020508
25	7079	3978	54	-0.267493	0.010875
26	3468	1949	15	-0.278816	0.011324
27	6793	3818	6	-0.290617	0.011800
28	3325	1868	55	-0.302924	0.012308
29	6507	3657	22	-0.315773	0.012849
30	3182	1788	31	-0.329199	0.013426
31	6221	3496	38	-0.343243	0.014043
32	3039	1708	7	-0.357947	0.014704
33	5935	3335	54	-0.373360	0.015413
34	2896	1627	47	-0.389534	0.016174
35	5649	3175	6	-0.406527	0.016993
36	2753	1547	23	-0.424402	0.017875

Number	R	N	A	f-fo(Hz)	df(hz)
37	5363	3014	22	-0.443231	0.018829
38	2610	1466	63	-0.463091	0.019860
39	5077	2853	38	-0.484071	0.020979
40	2467	1386	39	-0.506266	0.022195
41	7258	4079	29	-0.521791	0.015526
42	4791	2692	54	-0.529786	0.007995
43	7115	3999	5	-0.537941	0.008155
44	2324	1306	15	-0.554753	0.016812
45	6829	3838	21	-0.572269	0.017516
46	4505	2532	6	-0.581306	0.009036
47	6686	3757	61	-0.590535	0.009229
48	2181	1225	55	-0.609599	0.019064
49	6400	3597	13	-0.629515	0.019916
50	4219	2371	22	-0.639810	0.010295
51	6257	3516	53	-0.650341	0.010531
52	2038	1145	31	-0.672141	0.021800
53	5971	3356	5	-0.694986	0.022845
54	3933	2210	38	-0.706824	0.011838
55	5828	3275	45	-0.718952	0.012128
56	1895	1065	7	-0.744123	0.025171
57	5542	3114	61	-0.770593	0.026470
58	3647	2049	54	-0.784348	0.013754
59	5399	3034	37	-0.798466	0.014118
60	7151	4019	20	-0.805666	0.007200
61	1752	984	47	-0.827855	0.022189
62	6865	3858	36	-0.850968	0.023113
63	5113	2873	53	-0.858888	0.007920
64	3361	1889	6	-0.875065	0.016177
65	4970	2793	29	-0.891707	0.016642
66	6579	3697	52	-0.900209	0.008502
67	1609	904	23	-0.926471	0.026261
68	6293	3537	4	-0.953926	0.027455
69	4684	2632	45	-0.963357	0.009431
70	3075	1728	22	-0.982657	0.019301
71	4541	2552	21	-1.002566	0.019908
72	6007	3376	20	-1.012757	0.010191
73	1466	823	63	-1.044325	0.031568

Number	R	N	A	f-fo(Hz)	df(hz)
74	7187	4039	35	-1.070709	0.026385
75	5721	3215	36	-1.077471	0.006761
76	4255	2391	37	-1.088890	0.011420
77	7044	3959	11	-1.098166	0.009275
78	2789	1567	38	-1.112316	0.014150
79	6901	3878	51	-1.126759	0.014444
80	4112	2311	13	-1.136556	0.009796
81	5435	3054	52	-1.148995	0.012439
82	6758	3798	27	-1.156563	0.007569
83	1323	743	39	-1.187656	0.031093
84	6472	3637	43	-1.220123	0.032467
85	5149	2894	4	-1.228465	0.008342
86	3826	2150	29	-1.242576	0.014111
87	6329	3557	19	-1.254056	0.011480
88	2503	1406	54	-1.271605	0.017548
89	6186	3476	59	-1.289559	0.017954
90	3683	2070	5	-1.301761	0.012202
91	4863	2733	20	-1.317282	0.015521
92	6043	3396	35	-1.326742	0.009460
93	7223	4059	50	-1.333111	0.006369
94	1180	663	15	-1.365727	0.032616
95	6937	3899	2	-1.399688	0.033961
96	5757	3235	51	-1.406649	0.006961
97	4577	2572	36	-1.417199	0.010550
98	3397	1909	21	-1.435079	0.017880
99	5614	3155	27	-1.449656	0.014577
100	2217	1246	6	-1.471991	0.022336

Appendix B: Precision Frequency Measurement

One goal for the calibration of the PRS10 is to set the frequency to within 1 part in 10^{11} of 10MHz (which is 10MHz ± 0.0001Hz, or 10MHz ±100μHz). Two things are required to make this measurement: (1) a very good 10MHz frequency reference, and, (2) a very good time-interval counter.

The frequency reference should be stable and accurate to a few parts in 10^{12}. Another PRS10 locked to the 1pps from a GPS receiver, or a cesium beam standard (such as HP 5071A), are two possibilities.

The time-interval counter needs to measure time intervals with a resolution of better than 50ps, and should be able to do fast averaging of the time-interval measurements. Suitable instruments include the SR620 or an HP5370B.

The time-interval counter may be used to directly measure the frequency of the device under test (DUT). In this case, the frequency reference is used as the timebase for the time-interval counter. Unfortunately, the time-interval counter will require about 100 seconds to measure the frequency to a resolution of 1 part in 10^{12} when used in the frequency measurement mode.

A faster way to make the comparison between the reference frequency and the DUT is to use the time interval measurement mode of the counters. In this case, the time intervals between the 10MHz zero crossings of the reference frequency and the DUT are measured and averaged. If this time interval changes by less than 10ps per second, then the DUT is within 1 part in 10^{11} of the frequency reference.

This technique is very similar to the technique of offsetting the reference frequency from the DUT, mixing the two sources, amplifying and filtering and measuring the frequency of the beatnote. (Often referred to as a heterodyne measurement.) However, the time interval measurement technique does not require mixers or amplifiers or offsetting the reference from the DUT.

The resolution of the time-interval technique is remarkable. Each time-interval measurement has an rms jitter of about 25ps (in the case of the SR620). As the jitter is randomly distributed, the jitter of the mean is reduced by the square root of the number of samples. For a 1000 sample measurement, (which takes less than one second to complete) the rms jitter of the mean will be less than 1ps, and the difference between two time interval measurements will have a jitter of less than 2ps. This provides a relative frequency measurement to 2 parts in 10^{12} in 2 seconds.

Set-up for an SR620

Described here is the set-up for an SR620 Time Interval Counter to make precision frequency measurements. For a detailed description for the operation of the SR620, refer to the instrument's operation and service manual.

Four input connections:

The 10MHz reference frequency is connected to both the rear panel 10MHz input and to the "A" (START) input. (Place the tee on the rear panel input.)
Connect the 10MHz from the DUT to the "B" (STOP) input.
Connect the 1kHz TTL square wave from "REF" output to gate "EXT" input BNC.

Four input setups:

From the front panel "CONFIG" menu, use "SET" to choose the "cAL" menu, then use "SELECT" to select the "cLoc SourcE". Use the arrow keys to set the clock source to "rEAr". This will allow the SR620 to use the 10MHz reference frequency which has been applied to the rear panel 10MHz input as the timebase for all measurements.

Set the "EXT" gate input "LOGIC" to POS, "TERM" to 50Ω, and "LEVEL" to +1.0V. The "TRIG" LED will go on when the "GATE/ARM" is setup properly.

Both "A" (START) and "B" (STOP) are AC coupled and terminated into 50Ω. The "SLOPE" is set to "+", and the "LEVEL" is turned full counter-clockwise to "AUTO" and the "UHF" LED should be off. The "TRIG" LEDs will be on when the 10MHz sources are present.

"Coarse" Frequency Measurements

You should verify that the DUT is very close (within 0.1Hz) to 10MHz. To measure the frequency, set "MODE" to "FREQ", set "SOURCE" to "B", set the "GATE/ARM" to 1s, and set the "SAMPLE SIZE" to 1. Hold the "START" button down for a few seconds to start continuous measurements. Set the display to "MEAN" to display the frequency of the 10MHz output from the DUT.

"Fine" Frequency Measurements

If the 10MHz from the DUT is within 0.1Hz of 10MHz, you may use the "fine" frequency measurement technique to make measurements to a few parts in 10^{12} in a one second interval. As explained above, the frequency offset between the reference and the DUT is inferred by time-interval measurements between their zero-crossings.

To carry out these measurements: Set the "MODE" to "TIME", select the "SOURCE" (of START) to "A", set the "GATE/ARM" mode to "+TIME" and "EXT", and set the

"SAMPLE SIZE" to 1000. With the external gate triggered by the SR620's 1kHz reference output, the unit will display a new "MEAN" every second. If the DUT is adjusted so that the mean of the time interval measurements changes by less than 10ps per second, then the DUT is within 1 part of 10^{11} of the reference frequency.

Parts list for Revision H

Part reference numbers may be used to help locate the part per the following table:

Reference Designator	Location
100 to 149	10MHz oven oscillator (front vertical) PCB
150 to 199	Crystal heater PCB (front vertical)
200 to 299	Analog servos and amplifiers (top) PCB
300 to 399	Microcontroller (left-side, vertical) PCB
400 to 499	Frequency synthesizer (right side, vert) PCB
500 to 599	P/S and 1PPS circuits (bottom) PCB
600 to 699	Cell heater PCB (rear vertical)
700 to 799	Inside the resonance cell
800 to 899	Lamp heater PCB (center vertical)
900 to 999	Inside lamp enclosure

Rubidium Oscillator PC Board Assembly Parts List

REF.	SRS PART	VALUE	DESCRIPTION
C 100	5-00595-569	2.2U/50V	Cap, Tantalum, SMT (all case sizes)
C 101	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 102	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 103	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 106	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 107	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 109	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
C 110	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 111	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 112	5-00361-552	6.8P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 113	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 114	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 115	5-00586-569	4.7UF/50V	Cap, Tantalum, SMT (all case sizes)
C 116	5-00586-569	4.7UF/50V	Cap, Tantalum, SMT (all case sizes)
C 151	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 152	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 200	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 201	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 202	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 203	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 204	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 205	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 206	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 207	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes

REF.	SRS PART	VALUE	DESCRIPTION
C 208	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 210	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 212	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 216	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 217	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 218	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 219	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 220	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 221	5-00454-572	.01U	SMT Film Capacitors, 50V, 5%, All Sizes
C 222	5-00454-572	.01U	SMT Film Capacitors, 50V, 5%, All Sizes
C 223	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 224	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 226	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 227	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 228	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 229	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 230	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 231	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 232	5-00355-552	2.2P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 301	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 302	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 304	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 306	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 308	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 309	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 310	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 311	5-00586-569	4.7UF/50V	Cap, Tantalum, SMT (all case sizes)
C 400	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 401	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 402	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 403	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 404	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 405	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 406	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 407	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 408	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 409	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 410	5-00462-572	.047U	SMT Film Capacitors, 50V, 5%, All Sizes
C 411	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 413	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 414	5-00373-552	68P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 415	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 416	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 417	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 418	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 419	5-00456-572	.015U	SMT Film Capacitors, 50V, 5%, All Sizes
C 420	5-00456-572	.015U	SMT Film Capacitors, 50V, 5%, All Sizes
C 421	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

REF.	SRS PART	VALUE	DESCRIPTION
C 422	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 423	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 424	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 425	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 426	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 427	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 428	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 429	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 430	5-00359-552	4.7P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 431	5-00356-552	2.7P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 432	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 433	5-00364-552	12P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 434	5-00366-552	18P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 436	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 437	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 438	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 439	5-00298-568	.01U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 440	5-00466-572	.1U	SMT Film Capacitors, 50V, 5%, All Sizes
C 500	5-00595-569	2.2U/50V	Cap, Tantalum, SMT (all case sizes)
C 502	5-00595-569	2.2U/50V	Cap, Tantalum, SMT (all case sizes)
C 504	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 506	5-00595-569	2.2U/50V	Cap, Tantalum, SMT (all case sizes)
C 507	5-00595-569	2.2U/50V	Cap, Tantalum, SMT (all case sizes)
C 508	5-00595-569	2.2U/50V	Cap, Tantalum, SMT (all case sizes)
C 509	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 510	5-00356-552	2.7P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 511	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 512	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 513	5-00376-552	120P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 514	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 515	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 516	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 517	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 518	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 519	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 520	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 521	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 600	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 601	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 602	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 700	5-00480-574	5.6P 500V	SMT, High Voltage Porcelain Cap.
C 800	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 801	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 802	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 803	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 804	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 805	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 900	5-00100-517	2.2U	Capacitor, Tantalum, 35V, 20%, Rad

REF.	SRS PART	VALUE	DESCRIPTION
C 903	5-00487-574	68P 500V	SMT, High Voltage Porcelain Cap.
C 904	5-00479-574	18P 500V	SMT, High Voltage Porcelain Cap.
C 905	5-00479-574	18P 500V	SMT, High Voltage Porcelain Cap.
C 906	5-00487-574	68P 500V	SMT, High Voltage Porcelain Cap.
D 100	3-00803-360	MMBV609	Integrated Circuit (Surface Mount Pkg)
D 101	3-00648-360	MBRD660CT	Integrated Circuit (Surface Mount Pkg)
D 102	3-00648-360	MBRD660CT	Integrated Circuit (Surface Mount Pkg)
D 202	3-00538-360	MMBD352L	Integrated Circuit (Surface Mount Pkg)
D 203	3-00854-313	ZMM5230B	Diode, SMT
D 204	3-00854-313	ZMM5230B	Diode, SMT
D 205	3-00854-313	ZMM5230B	Diode, SMT
D 400	3-00803-360	MMBV609	Integrated Circuit (Surface Mount Pkg)
D 401	3-00803-360	MMBV609	Integrated Circuit (Surface Mount Pkg)
D 500	3-00648-360	MBRD660CT	Integrated Circuit (Surface Mount Pkg)
D 501	3-00806-360	BAV170LT1	Integrated Circuit (Surface Mount Pkg)
D 502	3-00649-360	BAW56LT1	Integrated Circuit (Surface Mount Pkg)
D 503	3-00544-360	BAV70LT1	Integrated Circuit (Surface Mount Pkg)
D 504	3-00806-360	BAV170LT1	Integrated Circuit (Surface Mount Pkg)
D 700	3-00235-308	MP4025	Diode, Step Recovery
J 100	1-00319-166	10 PIN MALE	Connector, D-Sub, Male
J 100X	1-00320-100	COAX INSERT	Connector, Misc.
J 400	1-00224-141	STRAIGHT PLUG	SMB Connector
J 700	1-00222-141	REAR MT JACK	SMB Connector
J 701	1-00222-141	REAR MT JACK	SMB Connector
J 800	6-00017-630	FB43-301	Ferrite Beads
J 801	6-00017-630	FB43-301	Ferrite Beads
J 802	6-00017-630	FB43-301	Ferrite Beads
JP500	1-00323-130	64 PIN STRIP	Connector, Male
JP501	1-00324-130	64 HDR PIN R/A	Connector, Male
L 100	6-00171-606	4.7UH-5PH	Inductor, Variable
L 101	6-00171-606	4.7UH-5PH	Inductor, Variable
L 102	6-00264-609	100UH - SMT	Inductor, Fixed, SMT
L 103	6-00264-609	100UH - SMT	Inductor, Fixed, SMT
L 104	6-00174-630	6611 TYPE 43	Ferrite Beads
L 105	6-00174-630	6611 TYPE 43	Ferrite Beads
L 200	6-00236-631	FR47	Ferrite bead, SMT
L 300	6-00236-631	FR47	Ferrite bead, SMT
L 301	6-00236-631	FR47	Ferrite bead, SMT
L 302	6-00236-631	FR47	Ferrite bead, SMT
L 400	6-00530-609	.027UH - SMT	Inductor, Fixed, SMT
L 401	6-00513-609	.012UH - SMT	Inductor, Fixed, SMT
L 402	6-00266-609	.18UH - SMT	Inductor, Fixed, SMT
L 403	6-00281-609	2.2U - SMT	Inductor, Fixed, SMT
L 902	6-00011-603	1.0U	Inductor, Axial
LX104	0-00772-000	1.5" WIRE	Hardware, Misc.
LX105	0-00772-000	1.5" WIRE	Hardware, Misc.
P 100	4-01576-459	50K 9MM SIDE	Pot, Multi-Turn Cermet, Various sizes
PC1	7-00767-701	RB MULTIPLES	Printed Circuit Board

REF.	SRS PART	VALUE	DESCRIPTION
Q 100	3-00808-360	MMBR5179	Integrated Circuit (Surface Mount Pkg)
Q 101	3-00555-360	MMBR941L	Integrated Circuit (Surface Mount Pkg)
Q 150	3-00325-329	TIP107	Voltage Reg., TO-220 (TAB) Package
Q 400	3-00895-360	NE461M02	Integrated Circuit (Surface Mount Pkg)
Q 500	3-00807-360	MJD47	Integrated Circuit (Surface Mount Pkg)
Q 501	3-00540-360	MMBT5087	Integrated Circuit (Surface Mount Pkg)
Q 502	3-00808-360	MMBR5179	Integrated Circuit (Surface Mount Pkg)
Q 503	3-00809-360	MMBTH81LT1	Integrated Circuit (Surface Mount Pkg)
Q 504	3-00810-360	MMBTH10LT1	Integrated Circuit (Surface Mount Pkg)
Q 600	3-00325-329	TIP107	Voltage Reg., TO-220 (TAB) Package
Q 800	3-00325-329	TIP107	Voltage Reg., TO-220 (TAB) Package
Q 900	3-00665-360	MRF134	Integrated Circuit (Surface Mount Pkg)
R 100	4-01242-462	20.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 101	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 103	4-00954-462	20	Thin Film, 1%, 50 ppm, MELF Resistor
R 104	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 105	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 106	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 107	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 108	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 109	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 110	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 111	4-01067-462	301	Thin Film, 1%, 50 ppm, MELF Resistor
R 112	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 113	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 114	4-01096-462	604	Thin Film, 1%, 50 ppm, MELF Resistor
R 115	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 116	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 117	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 118	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 119	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 120	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 121	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 123	4-00925-462	10	Thin Film, 1%, 50 ppm, MELF Resistor
R 150	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 151	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 153	4-00899-431	P1H104-T-NTC	Thermistor, various
R 154	4-00899-431	P1H104-T-NTC	Thermistor, various
R 200	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 201	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 202	4-01295-462	71.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 203	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 204	4-01557-461	1.8M	Thick Film, 5%, 200 ppm, Chip Resistor
R 205	4-01575-461	10M	Thick Film, 5%, 200 ppm, Chip Resistor
R 206	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 207	4-01376-462	499K	Thin Film, 1%, 50 ppm, MELF Resistor
R 208	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor

REF.	SRS PART	VALUE	DESCRIPTION
R 209	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 210	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 211	4-01278-462	47.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 213	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 214	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 215	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 216	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 217	4-01557-461	1.8M	Thick Film, 5%, 200 ppm, Chip Resistor
R 218	4-01575-461	10M	Thick Film, 5%, 200 ppm, Chip Resistor
R 219	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 220	4-01376-462	499K	Thin Film, 1%, 50 ppm, MELF Resistor
R 221	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 222	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 223	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 224	4-01278-462	47.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 226	4-01238-462	18.2K	Thin Film, 1%, 50 ppm, MELF Resistor
R 227	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 228	4-01363-462	365K	Thin Film, 1%, 50 ppm, MELF Resistor
R 229	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 230	4-01557-461	1.8M	Thick Film, 5%, 200 ppm, Chip Resistor
R 231	4-01575-461	10M	Thick Film, 5%, 200 ppm, Chip Resistor
R 232	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 233	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 234	4-01376-462	499K	Thin Film, 1%, 50 ppm, MELF Resistor
R 235	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 236	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 237	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 238	4-01278-462	47.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 240	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 241	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 248	4-01439-461	22	Thick Film, 5%, 200 ppm, Chip Resistor
R 249	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 250	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 252	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 256	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 261	4-01335-462	187K	Thin Film, 1%, 50 ppm, MELF Resistor
R 262	4-01355-462	301K	Thin Film, 1%, 50 ppm, MELF Resistor
R 263	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 264	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 265	4-01098-462	634	Thin Film, 1%, 50 ppm, MELF Resistor
R 266	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 267	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 268	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 269	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 270	4-01347-462	249K	Thin Film, 1%, 50 ppm, MELF Resistor
R 271	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 272	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 273	4-01455-461	100	Thick Film, 5%, 200 ppm, Chip Resistor

REF.	SRS PART	VALUE	DESCRIPTION
R 274	4-01191-462	5.90K	Thin Film, 1%, 50 ppm, MELF Resistor
R 275	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 276	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 277	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 278	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 279	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 280	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 281	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 282	4-01305-462	90.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 283	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 284	4-01294-462	69.8K	Thin Film, 1%, 50 ppm, MELF Resistor
R 285	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 286	4-01294-462	69.8K	Thin Film, 1%, 50 ppm, MELF Resistor
R 287	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 288	4-01294-462	69.8K	Thin Film, 1%, 50 ppm, MELF Resistor
R 289	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 290	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 291	4-01575-461	10M	Thick Film, 5%, 200 ppm, Chip Resistor
R 292	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 293	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 294	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 295	4-01575-461	10M	Thick Film, 5%, 200 ppm, Chip Resistor
R 296	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 297	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 298	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 299	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 300	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 301	4-01302-462	84.5K	Thin Film, 1%, 50 ppm, MELF Resistor
R 303	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 304	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 305	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 324	4-01249-462	23.7K	Thin Film, 1%, 50 ppm, MELF Resistor
R 325	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 326	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 327	4-01455-461	100	Thick Film, 5%, 200 ppm, Chip Resistor
R 329	4-01455-461	100	Thick Film, 5%, 200 ppm, Chip Resistor
R 331	4-01073-462	348	Thin Film, 1%, 50 ppm, MELF Resistor
R 332	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 333	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 334	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 335	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 336	4-01575-461	10M	Thick Film, 5%, 200 ppm, Chip Resistor
R 337	4-01455-461	100	Thick Film, 5%, 200 ppm, Chip Resistor
R 338	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 339	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 340	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 341	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 342	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor

REF.	SRS PART	VALUE	DESCRIPTION
R 343	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 344	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 345	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 346	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 347	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 348	0-00000-000	UNDECIDED PART	Hardware, Misc.
R 349	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 350	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 351	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 352	4-01464-461	240	Thick Film, 5%, 200 ppm, Chip Resistor
R 353	0-00000-000	UNDECIDED PART	Hardware, Misc.
R 354	4-01493-461	3.9K	Thick Film, 5%, 200 ppm, Chip Resistor
R 355	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 356	4-01493-461	3.9K	Thick Film, 5%, 200 ppm, Chip Resistor
R 357	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 358	0-00000-000	UNDECIDED PART	Hardware, Misc.
R 359	0-00000-000	UNDECIDED PART	Hardware, Misc.
R 360	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 400	4-01347-462	249K	Thin Film, 1%, 50 ppm, MELF Resistor
R 401	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 402	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 403	4-01463-461	220	Thick Film, 5%, 200 ppm, Chip Resistor
R 404	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 405	4-01201-462	7.50K	Thin Film, 1%, 50 ppm, MELF Resistor
R 406	4-01561-461	2.7M	Thick Film, 5%, 200 ppm, Chip Resistor
R 407	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 408	4-01259-462	30.1K	Thin Film, 1%, 50 ppm, MELF Resistor
R 409	4-01355-462	301K	Thin Film, 1%, 50 ppm, MELF Resistor
R 410	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 411	4-01527-461	100K	Thick Film, 5%, 200 ppm, Chip Resistor
R 412	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 413	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 414	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 415	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 416	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 417	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 418	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 419	4-01467-461	330	Thick Film, 5%, 200 ppm, Chip Resistor
R 420	4-01467-461	330	Thick Film, 5%, 200 ppm, Chip Resistor
R 421	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 422	4-01355-462	301K	Thin Film, 1%, 50 ppm, MELF Resistor
R 423	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 424	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 425	4-01471-461	470	Thick Film, 5%, 200 ppm, Chip Resistor
R 426	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 427	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 428	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 429	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor

REF.	SRS PART	VALUE	DESCRIPTION
R 430	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 431	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 432	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 433	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 434	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 435	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 436	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 437	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 438	4-01355-462	301K	Thin Film, 1%, 50 ppm, MELF Resistor
R 439	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 440	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 441	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 442	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 443	4-01439-461	22	Thick Film, 5%, 200 ppm, Chip Resistor
R 444	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 445	4-01511-461	22K	Thick Film, 5%, 200 ppm, Chip Resistor
R 446	4-01503-461	10K	Thick Film, 5%, 200 ppm, Chip Resistor
R 447	4-01455-461	100	Thick Film, 5%, 200 ppm, Chip Resistor
R 448	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 449	4-01551-461	1.0M	Thick Film, 5%, 200 ppm, Chip Resistor
R 450	4-01439-461	22	Thick Film, 5%, 200 ppm, Chip Resistor
R 500	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 501	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 502	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 503	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 504	4-00925-462	10	Thin Film, 1%, 50 ppm, MELF Resistor
R 505	4-00925-462	10	Thin Film, 1%, 50 ppm, MELF Resistor
R 506	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 507	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 508	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 509	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 510	4-01347-462	249K	Thin Film, 1%, 50 ppm, MELF Resistor
R 511	4-01280-462	49.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 512	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 513	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 514	4-01167-462	3.32K	Thin Film, 1%, 50 ppm, MELF Resistor
R 515	4-01487-461	2.2K	Thick Film, 5%, 200 ppm, Chip Resistor
R 516	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 517	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 518	4-01242-462	20.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 519	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 520	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 521	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 522	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 523	4-01251-462	24.9K	Thin Film, 1%, 50 ppm, MELF Resistor
R 524	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 525	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 526	4-01242-462	20.0K	Thin Film, 1%, 50 ppm, MELF Resistor

REF.	SRS PART	VALUE	DESCRIPTION
R 527	4-01230-462	15.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 528	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 529	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 530	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 531	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 532	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 533	4-01493-461	3.9K	Thick Film, 5%, 200 ppm, Chip Resistor
R 534	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 536	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 537	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 538	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 539	4-01489-461	2.7K	Thick Film, 5%, 200 ppm, Chip Resistor
R 540	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 541	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 542	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 543	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 544	4-01218-462	11.3K	Thin Film, 1%, 50 ppm, MELF Resistor
R 545	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 546	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 547	4-01447-461	47	Thick Film, 5%, 200 ppm, Chip Resistor
R 548	4-01469-461	390	Thick Film, 5%, 200 ppm, Chip Resistor
R 550	4-01405-462	1.00M	Thin Film, 1%, 50 ppm, MELF Resistor
R 551	4-01479-461	1.0K	Thick Film, 5%, 200 ppm, Chip Resistor
R 552	4-00925-462	10	Thin Film, 1%, 50 ppm, MELF Resistor
R 553	4-00925-462	10	Thin Film, 1%, 50 ppm, MELF Resistor
R 600	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 601	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 602	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 603	4-00899-431	P1H104-T-NTC	Thermistor, various
R 604	4-00899-431	P1H104-T-NTC	Thermistor, various
R 605	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 800	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 801	4-01407-461	1	Thick Film, 5%, 200 ppm, Chip Resistor
R 803	4-00899-431	P1H104-T-NTC	Thermistor, various
R 804	4-00899-431	P1H104-T-NTC	Thermistor, various
R 900	4-01597-405	10K	Resistor, Carbon Film, 1/8W, 5%
T 100	6-00195-610	10.7 MHZ	Transformer
U 100	3-00542-360	AD587JR	Integrated Circuit (Surface Mount Pkg)
U 101	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 102	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 150	3-00346-329	7812	Voltage Reg., TO-220 (TAB) Package
U 200	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 201	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 202	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 205	3-00653-360	AD8561AR	Integrated Circuit (Surface Mount Pkg)
U 206	3-00659-360	OP284FS	Integrated Circuit (Surface Mount Pkg)
U 207	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 208	3-00661-360	74HC4051	Integrated Circuit (Surface Mount Pkg)

REF.	SRS PART	VALUE	DESCRIPTION
U 209	3-00661-360	74HC4051	Integrated Circuit (Surface Mount Pkg)
U 210	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 300	3-00563-360	MAX705CSA	Integrated Circuit (Surface Mount Pkg)
U 301	3-00662-360	74HC14	Integrated Circuit (Surface Mount Pkg)
U 303	3-00663-360	74HC08	Integrated Circuit (Surface Mount Pkg)
U 304	3-00662-360	74HC14	Integrated Circuit (Surface Mount Pkg)
U 306	3-00643-360	DG211BDY	Integrated Circuit (Surface Mount Pkg)
U 307	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 308	3-00659-360	OP284FS	Integrated Circuit (Surface Mount Pkg)
U 309	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 310	3-00652-360	LTC1452CS8	Integrated Circuit (Surface Mount Pkg)
U 311	3-00652-360	LTC1452CS8	Integrated Circuit (Surface Mount Pkg)
U 312	3-00652-360	LTC1452CS8	Integrated Circuit (Surface Mount Pkg)
U 313	3-00652-360	LTC1452CS8	Integrated Circuit (Surface Mount Pkg)
U 314	3-00658-360	AD7896AR	Integrated Circuit (Surface Mount Pkg)
U 400	3-00946-360	MC145193F	Integrated Circuit (Surface Mount Pkg)
U 401	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 402	3-00654-360	SA602D	Integrated Circuit (Surface Mount Pkg)
U 403	3-00660-360	OP27GS	Integrated Circuit (Surface Mount Pkg)
U 404	6-00193-625	380 MHZ	Voltage Controlled Crystal Oscillator
U 405	3-00650-360	MC12026AD	Integrated Circuit (Surface Mount Pkg)
U 406	3-00773-360	LM358	Integrated Circuit (Surface Mount Pkg)
U 407	3-00655-360	TLC5628	Integrated Circuit (Surface Mount Pkg)
U 500	3-00751-360	74HC574	Integrated Circuit (Surface Mount Pkg)
U 501	3-00149-329	LM317T	Voltage Reg., TO-220 (TAB) Package
U 502	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 503	3-00149-329	LM317T	Voltage Reg., TO-220 (TAB) Package
U 504	3-00112-329	7805	Voltage Reg., TO-220 (TAB) Package
U 505	3-00775-360	LM45CIM3	Integrated Circuit (Surface Mount Pkg)
U 506	3-00742-360	74HC74	Integrated Circuit (Surface Mount Pkg)
U 507	3-00742-360	74HC74	Integrated Circuit (Surface Mount Pkg)
U 508	3-00742-360	74HC74	Integrated Circuit (Surface Mount Pkg)
U 509	3-00813-360	LM311M	Integrated Circuit (Surface Mount Pkg)
U 510	3-00812-360	74HC153	Integrated Circuit (Surface Mount Pkg)
U 511	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 512	3-00581-360	AD822	Integrated Circuit (Surface Mount Pkg)
U 514	3-00534-360	AD790JR	Integrated Circuit (Surface Mount Pkg)
U 600	3-00346-329	7812	Voltage Reg., TO-220 (TAB) Package
U 800	3-00561-329	7808	Voltage Reg., TO-220 (TAB) Package
Y 100	6-00132-620	10 MHZ SC-CUT	Crystal
Y 400	6-00194-620	22.4825 MHZ	Crystal
Z 0	0-00045-013	4-40 MINI	Nut, Mini
Z 0	0-00096-041	#4 SPLIT	Washer, Split
Z 0	0-00098-042	#6 LOCK	Washer, lock
Z 0	0-00231-043	1-32, #4 SHOULD	Washer, nylon
Z 0	0-00243-003	TO-220	Insulators
Z 0	0-00605-025	4-40X1/4 SOCKET	Screw, Allen Head
Z 0	0-00606-025	4-40X1/4 BUTTON	Screw, Allen Head

REF.	SRS PART	VALUE	DESCRIPTION
Z 0	0-00607-025	4-40X1/2 SOCKET	Screw, Allen Head
Z 0	0-00608-025	6-32X1/4 BUTTON	Screw, Allen Head
Z 0	0-00609-025	6-32X5/8 SOCKET	Screw, Allen Head
Z 0	0-00629-066	FOIL;CU 1/2"	Copper Foil Tape, Self Adhesive
Z 0	0-00630-034	#22 INSULATING	Tubing
Z 0	0-00641-031	4-40X3/16 M/F	Standoff
Z 0	0-00642-031	4-40X3/8 M/F	Standoff
Z 0	0-00643-020	4-40X3/16PF UND	Screw, Flathead Phillips
Z 0	0-00644-020	4-40X1/4PF UNDR	Screw, Flathead Phillips
Z 0	0-00645-055	#34AWG MAGNET	Wire, Other
Z 0	0-00902-034	S/S SEAMLESS	Tubing
Z 0	0-00908-030	PROTO MATERIAL	Spacer
Z 0	0-00915-034	CU TUBING 1/16	Tubing
Z 0	1-00323-130	64 PIN STRIP	Connector, Male
Z 0	1-00324-130	64 HDR PIN R/A	Connector, Male
Z 0	3-00668-312	PHOTODIODE	Photodiode
Z 0	7-00557-717	RB-10	Deep-Drawn or Stamping
Z 0	7-00560-721	RB-1	Machined Part
Z 0	7-00636-720	RB-4	Fabricated Part
Z 0	7-00638-721	RB-6	Machined Part
Z 0	7-00639-721	RB-7	Machined Part
Z 0	7-00641-721	RB-9	Machined Part
Z 0	7-00862-720	RB SPACER	Fabricated Part
Z 0	9-00571-924	SPECIALTY #56	Tape, All types

Miscellaneous Parts List

REF.	SRS PART	VALUE	DESCRIPTION
R 901	4-01620-409	536-2W	Resistor, Wire Wound
U 302	3-00646-360	68HC711E20CFN	Integrated Circuit (Surface Mount Pkg)
Z 0	0-00096-041	#4 SPLIT	Washer, Split
Z 0	0-00602-060	4-40X3/32 SET	Screw, Misc
Z 0	0-00606-025	4-40X1/4 BUTTON	Screw, Allen Head
Z 0	0-00628-065	4-40X10-32X1/4"	Inserts, Threaded
Z 0	0-00644-020	4-40X1/4PF UNDR	Screw, Flathead Phillips
Z 0	0-00659-044	LAMP WINDOW	Window
Z 0	0-00668-025	4-40X3/16 HEX	Screw, Allen Head
Z 0	0-00669-025	4-40X5/16 HEX	Screw, Allen Head
Z 0	0-00670-025	4-40X3/8 BUTTON	Screw, Allen Head
Z 0	1-00355-150	LAMP	Socket, THRU-HOLE
Z 0	6-00505-600	RB CLOCK	Misc. Components
Z 0	7-00556-717	RB-12	Deep-Drawn or Stamping
Z 0	7-00637-720	RB-5	Fabricated Part
Z 0	7-00640-720	RB-8	Fabricated Part
Z 0	7-00764-720	RB-15	Fabricated Part
Z 0	9-00805-917	RUBIDIUM SERIAL	Product Labels

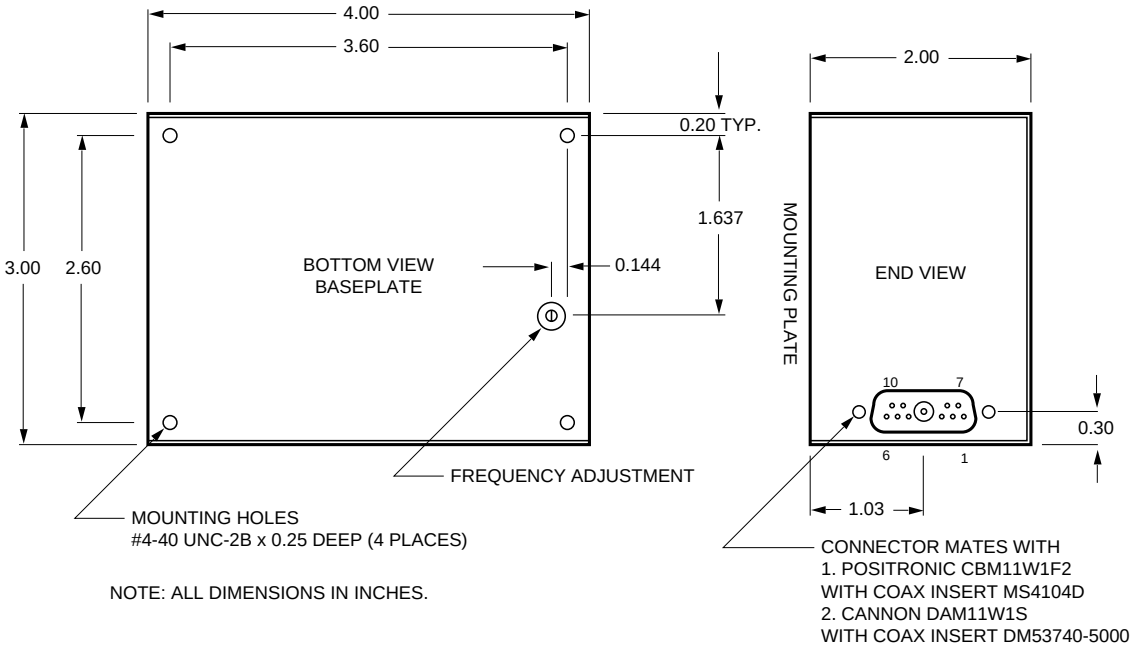
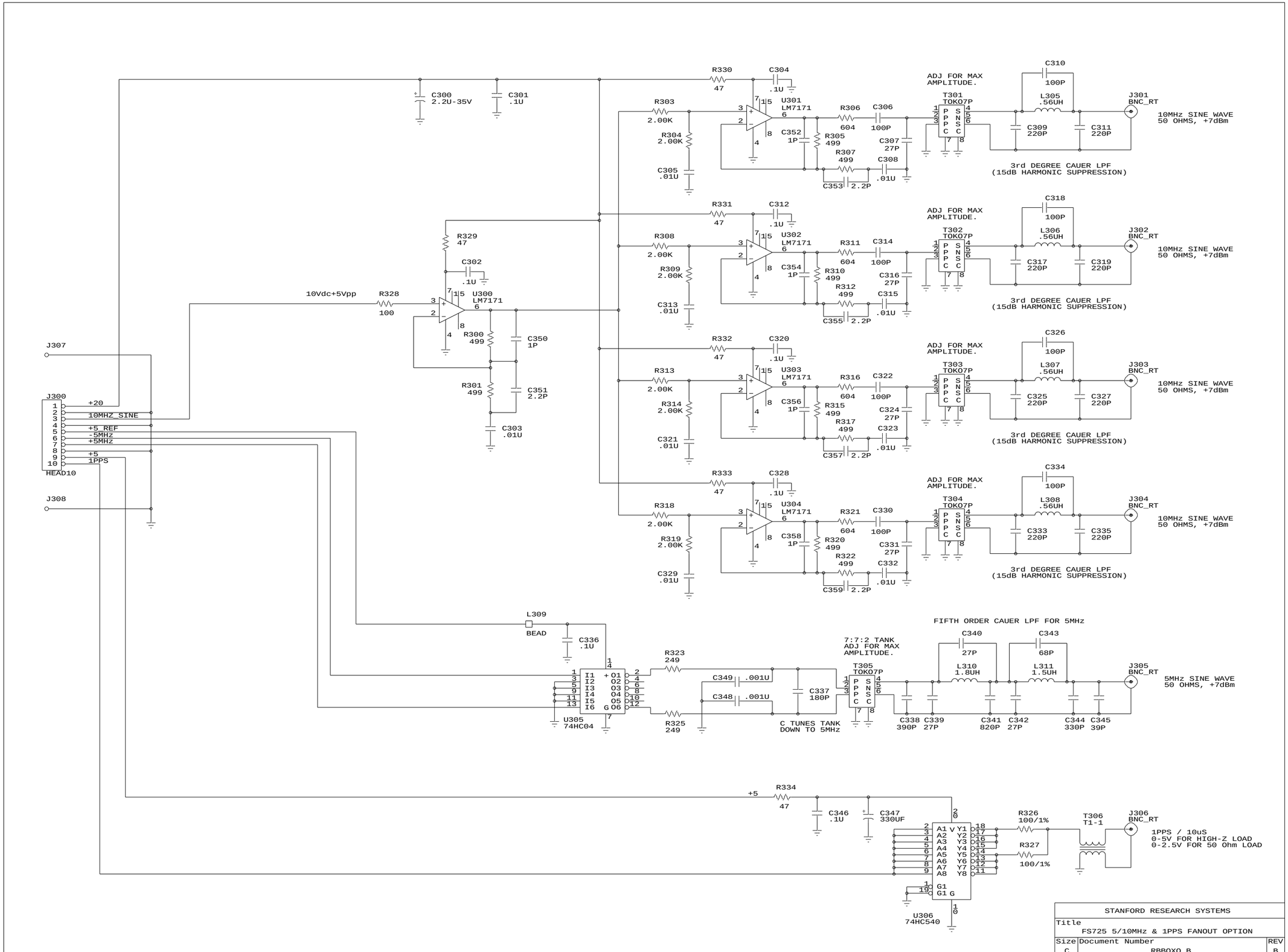
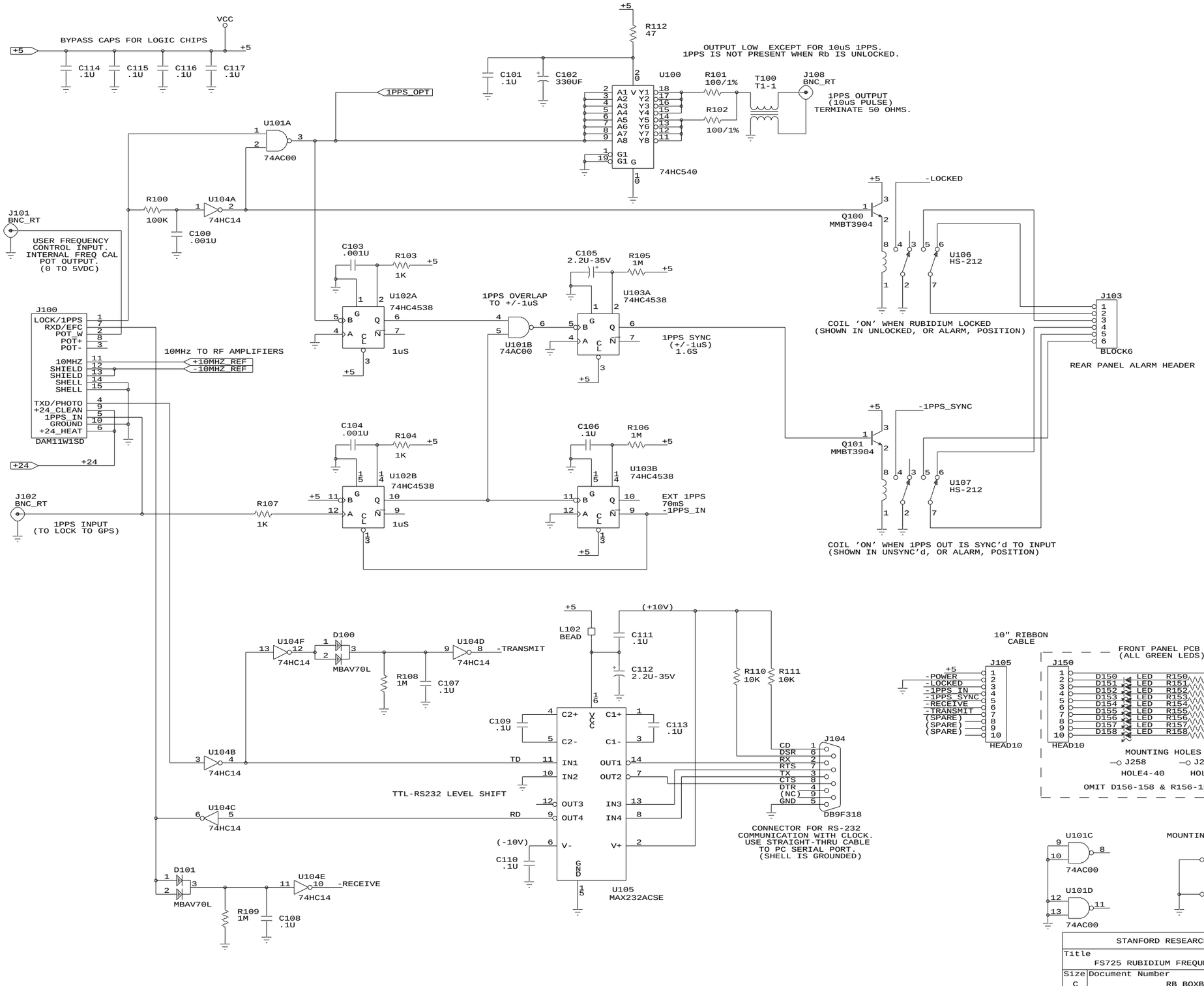


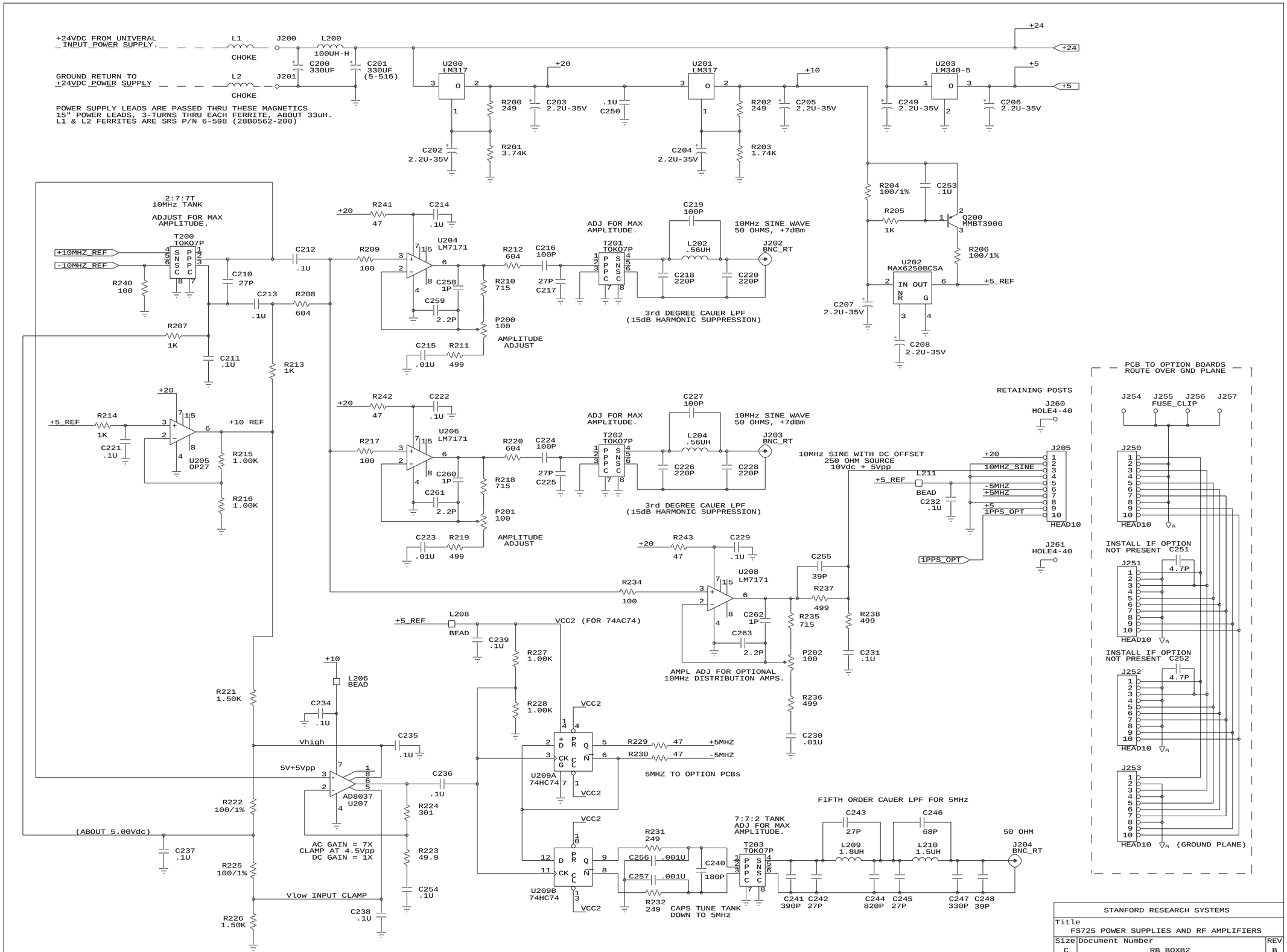
Figure 4. Mechanical Dimensions



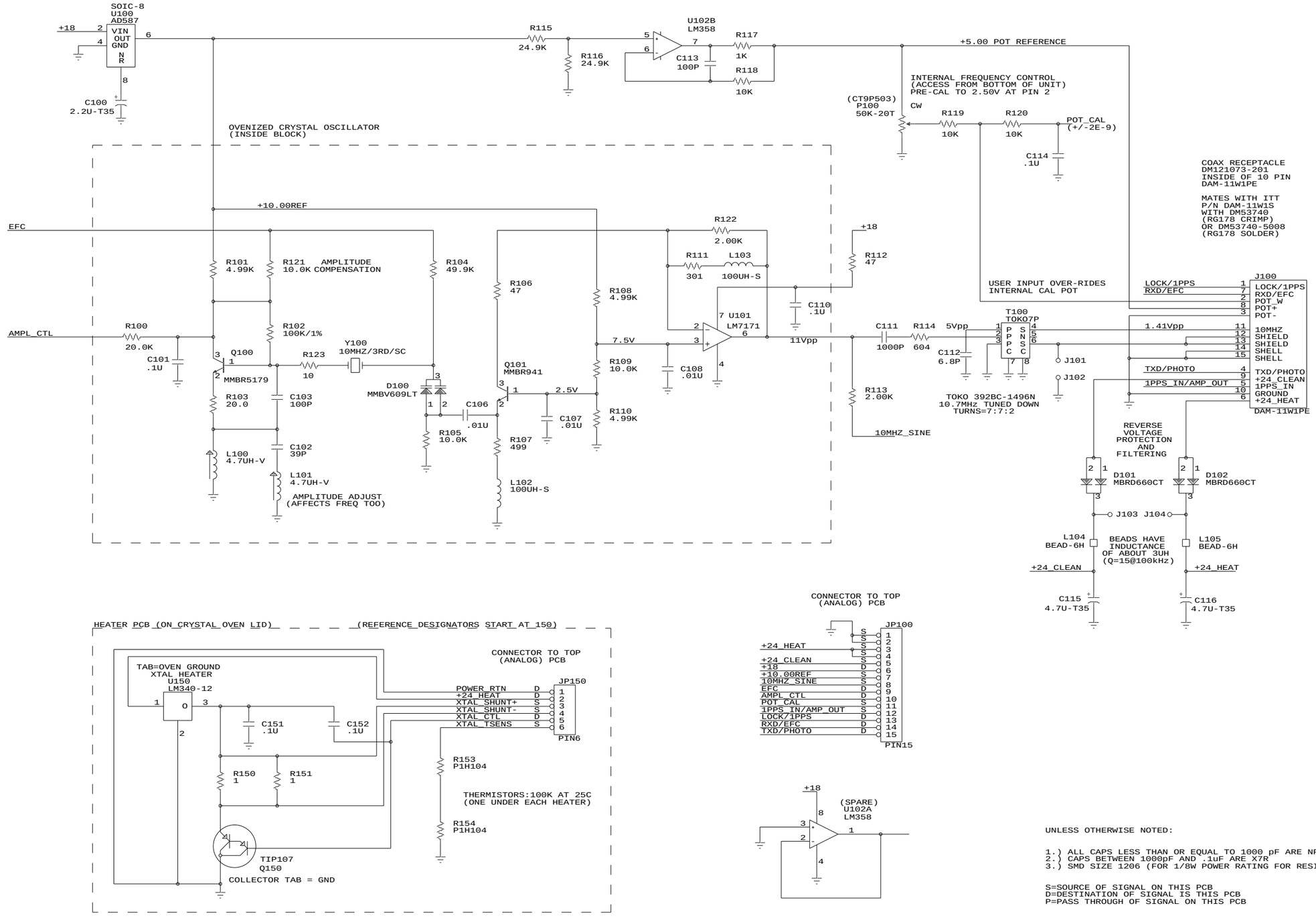
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Size: C	Document Number: RBBOXO_B	REV: B
Date: March 10, 2002	Sheet 1 of 1	



STANFORD RESEARCH SYSTEMS		
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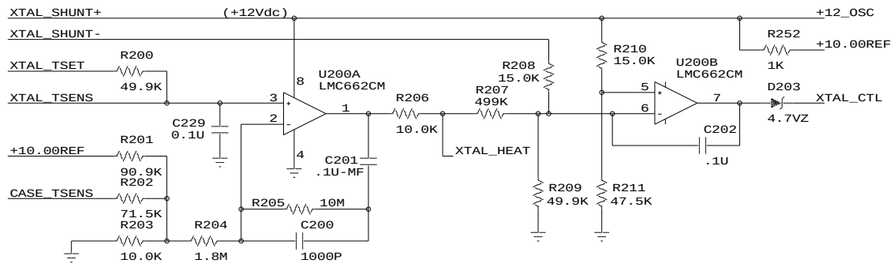


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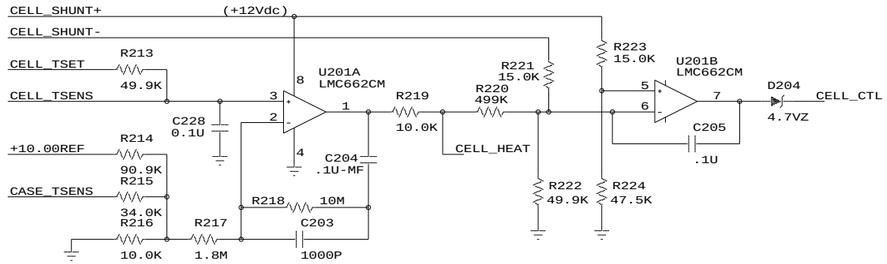


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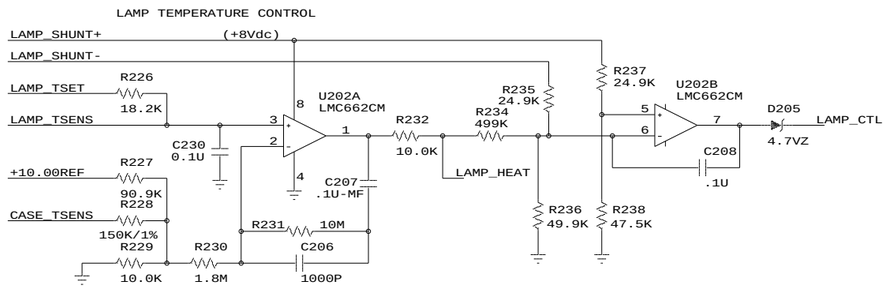
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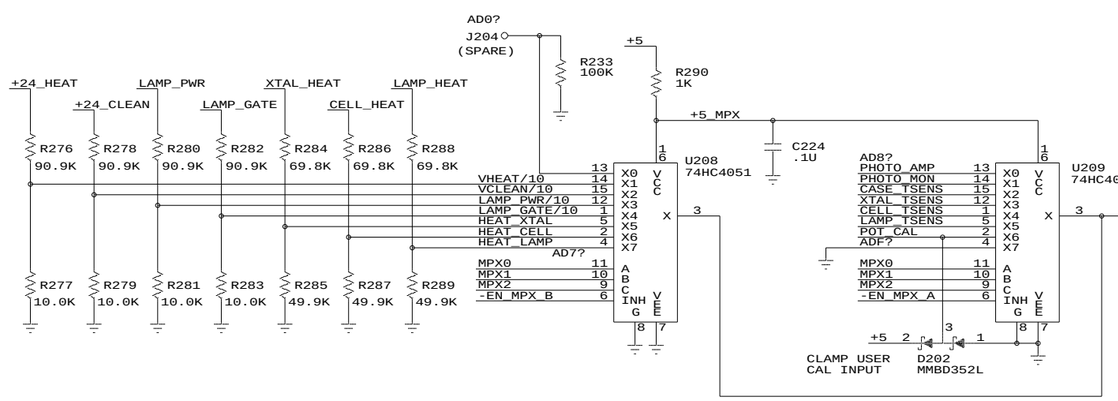


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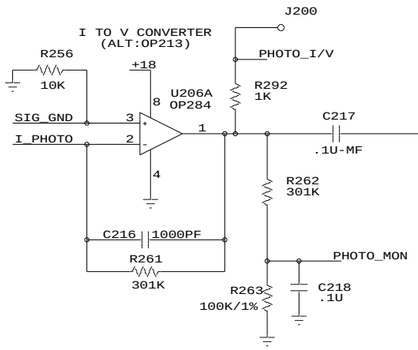


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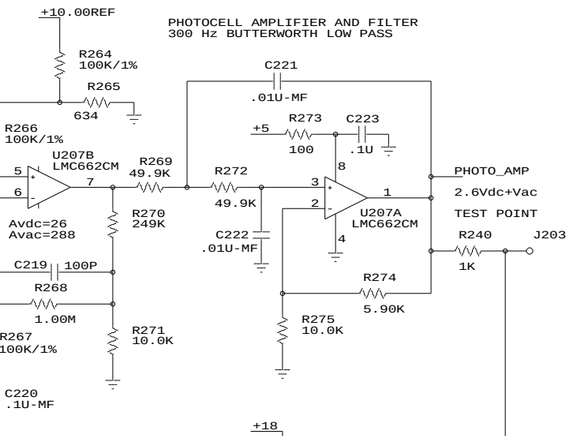


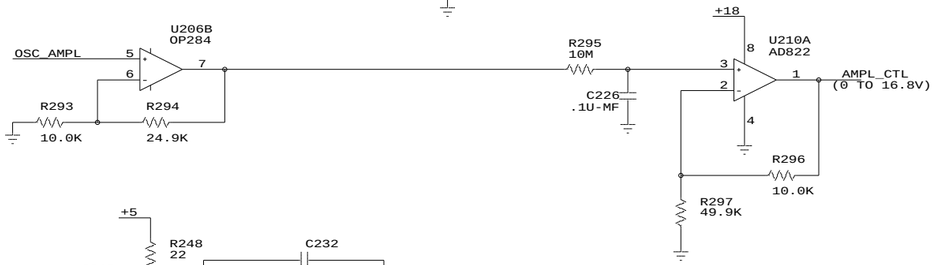


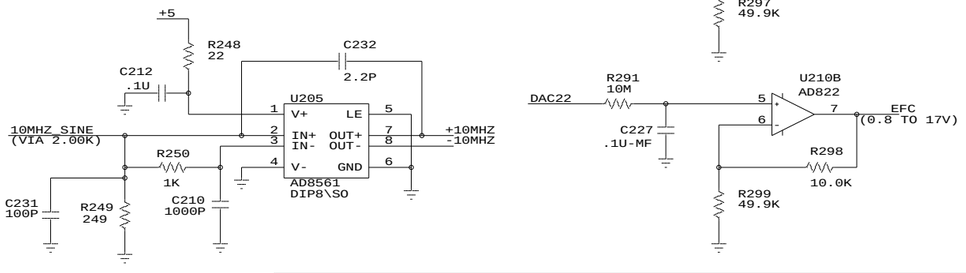
I TO V CONVERTER (ALT:OP213)



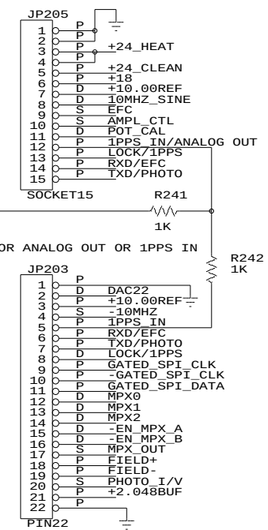
PHOTOCELL AMPLIFIER AND FILTER 300 Hz BUTTERWORTH LOW PASS



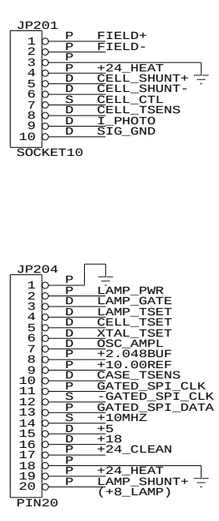




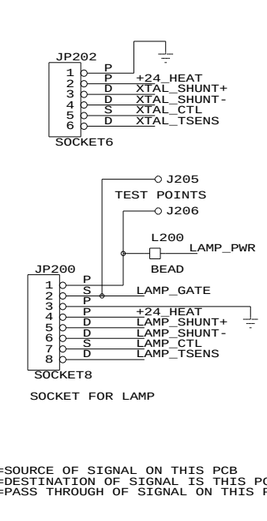
SOCKET FOR OVEN OSCILLATOR PCB



SOCKET FOR RESONANCE CELL



SOCKET FOR CRYSTAL OVEN



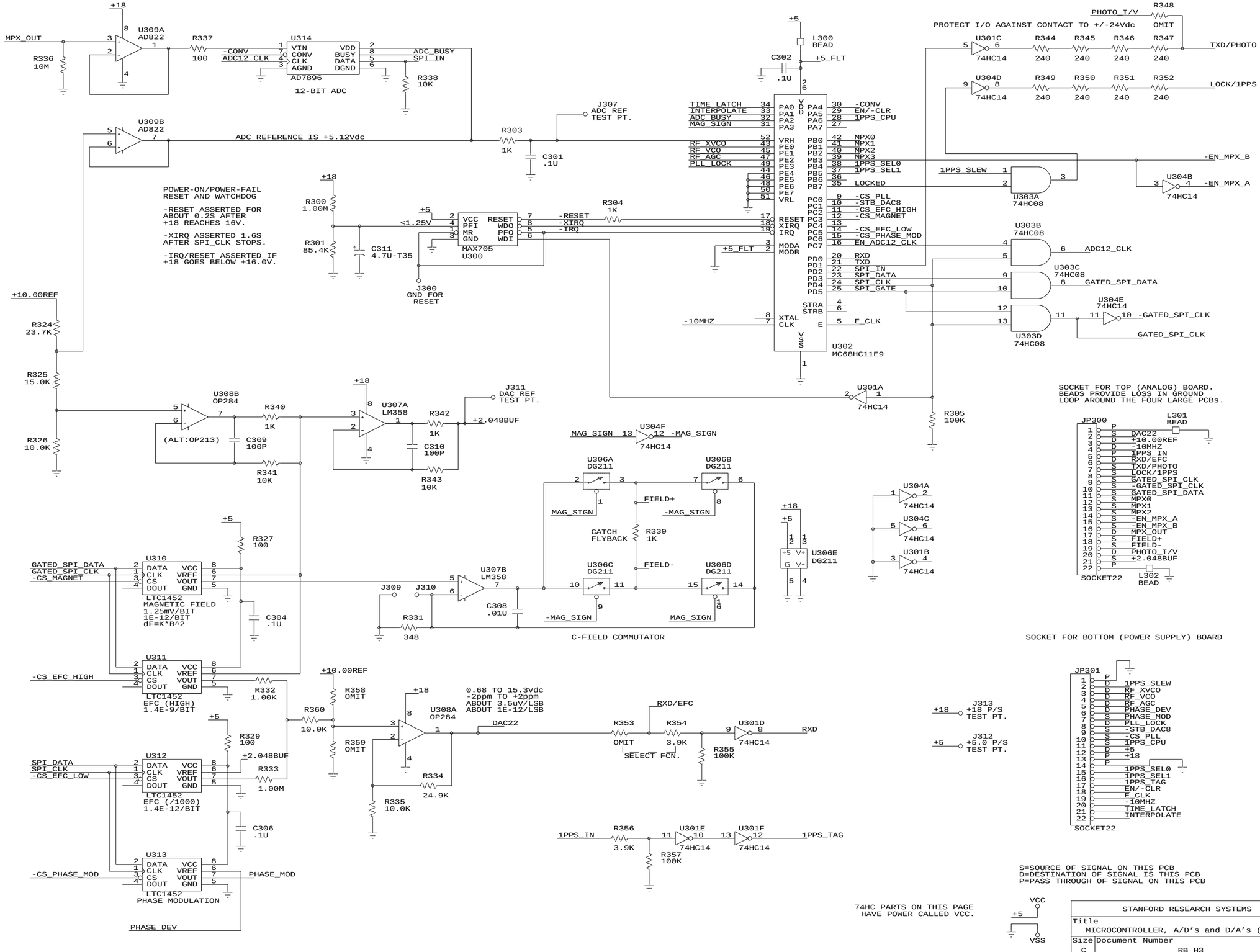
S=SOURCE OF SIGNAL ON THIS PCB
D=DESTINATION OF SIGNAL IS THIS PCB
P=PASS THROUGH OF SIGNAL ON THIS PCB

HEADER TO CPU PCB

HEADER TO FREQ. SYNTH. PCB

NOTE: ADDED C231 AND C232 AND CHANGED VALUE OF C210 AS OF 9/26/01.

STANFORD RESEARCH SYSTEMS		
Title: TEMPERATURE CONTROL & SIGNAL AMPS (TOP PCB)		
Size: C	Document Number: RB_H2	REV: H
Date: December 21, 2001	Sheet 2 of 6	


MPX_OUT
U309A AD822
R336 10M
R337 100
U314
-CONV
ADC12_CLK
VIN CONV CLK AGND
VDD BUSY DATA DGND
AD7896
12-BIT ADC
ADC_BUSY
SPI_IN
R338 10K
U309B AD822
ADC REFERENCE IS +5.12Vdc
R303 1K
C301 .1U
J307 ADC REF TEST PT.
L300 BEAD
C302 .1U
+5_FLT
U302 MC68HC11E9
TIME_LATCH
INTERPOLATE
ADC_BUSY
MAG_SIGN
RF_XVCO
RF_VCO
RF_AGC
PLL_LOCK
-CONV
EN/-CLR
1PPS_CPU
1PPS_SEL0
1PPS_SEL1
LOCKED
-CS_PLL
-STB_DAC8
-CS_EFC_HIGH
-CS_MAGNET
-CS_EFC_LOW
-CS_PHASE_MOD
EN_ADC12_CLK
RXD
TXD
SPI_IN
SPI_DATA
SPI_CLK
SPI_GATE
-10MHZ
E_CLK
PHOTO_I/V
R348 OMIT
PROTECT I/O AGAINST CONTACT TO +/-24Vdc
U301C 74HC14
R344 240
R345 240
R346 240
R347 240
TXD/PHOTO
U304D 74HC14
R349 240
R350 240
R351 240
R352 240
LOCK/1PPS
-EN_MPX_B
U304B 74HC14
-EN_MPX_A
1PPS_SLEW
U303A 74HC08
U303B 74HC08
ADC12_CLK
U303C 74HC08
GATED_SPI_DATA
U304E 74HC14
-GATED_SPI_CLK
GATED_SPI_CLK
U303D 74HC08
POWER-ON/POWER-FAIL RESET AND WATCHDOG
-RESET ASSERTED FOR ABOUT 0.2S AFTER +18 REACHES 16V.
-XIRQ ASSERTED 1.6S AFTER SPI_CLK STOPS.
-IRQ/RESET ASSERTED IF +18 GOES BELOW +16.0V.
R300 1.00M
R301 85.4K
C311 4.7U-T35
<1.25V
MAX705 U300
-RESET
-XIRQ
-IRQ
R304 1K
J300 GND FOR RESET
+10.00REF
R324 23.7K
R325 15.0K
R326 10.0K
U308B OP284
(ALT:OP213)
C309 100P
R340 1K
R341 10K
U307A LM358
R342 1K
C310 100P
R343 10K
J311 DAC REF TEST PT.
+2.048BUF
U301A 74HC14
R305 100K
SOCKET FOR TOP (ANALOG) BOARD.
BEADS PROVIDE LOSS IN GROUND
LOOP AROUND THE FOUR LARGE PCBs.
JP300
L301 BEAD
P
DAC22
+10.00REF
-10MHZ
1PPS_IN
RXD/EFC
TXD/PHOTO
LOCK/1PPS
GATED_SPI_CLK
-GATED_SPI_CLK
GATED_SPI_DATA
MPX0
MPX1
MPX2
-EN_MPX_A
-EN_MPX_B
MPX_OUT
FIELD+
FIELD-
PHOTO_I/V
+2.048BUF
SOCKET22
L302 BEAD
MAG_SIGN
U304F 74HC14
-MAG_SIGN
U306A DG211
U306B DG211
FIELD+
-MAG_SIGN
CATCH FLYBACK
R339 1K
U306C DG211
U306D DG211
FIELD-
-MAG_SIGN
MAG_SIGN
U306E DG211
C-FIELD COMMUTATOR
U304A 74HC14
U304C 74HC14
U301B 74HC14
GATED_SPI_DATA
GATED_SPI_CLK
-CS_MAGNET
U310
LTC1452
MAGNETIC_FIELD
1.25mV/BIT
1E-12/BIT
dF=K*B^2
C304 .1U
J309
J310
R331 348
C308 .01U
R327 100
-CS_EFC_HIGH
U311
LTC1452
EFC (HIGH)
1.4E-9/BIT
R332 1.00K
R329 100
SPI_DATA
SPI_CLK
-CS_EFC_LOW
U312
LTC1452
EFC (/1000)
1.4E-12/BIT
R333 1.00M
C306 .1U
-CS_PHASE_MOD
U313
LTC1452
PHASE MODULATION
PHASE_MOD
PHASE_DEV
R358 OMIT
R359 OMIT
R360 10.0K
U308A OP284
0.68 TO 15.3Vdc
-2ppm TO +2ppm
ABOUT 3.5uV/LSB
ABOUT 1E-12/LSB
R334 24.9K
R335 10.0K
R353 OMIT
R354 3.9K
SELECT FCN.
R355 100K
U301D 74HC14
RXD
1PPS_IN
R356 3.9K
U301E 74HC14
U301F 74HC14
R357 100K
1PPS_TAG
SOCKET FOR BOTTOM (POWER SUPPLY) BOARD
JP301
1PPS_SLEW
RF_XVCO
RF_VCO
RF_AGC
PHASE_DEV
PHASE_MOD
PLL_LOCK
-STB_DAC8
-CS_PLL
1PPS_CPU
+5
+18
1PPS_SEL0
1PPS_SEL1
1PPS_TAG
EN/-CLR
E_CLK
-10MHZ
TIME_LATCH
INTERPOLATE
SOCKET22
J313 +18 P/S TEST PT.
J312 +5.0 P/S TEST PT.
S=SOURCE OF SIGNAL ON THIS PCB
D=DESTINATION OF SIGNAL IS THIS PCB
P=PASS THROUGH OF SIGNAL ON THIS PCB
74HC PARTS ON THIS PAGE HAVE POWER CALLED VCC.
VCC
VSS
STANFORD RESEARCH SYSTEMS
Title
MICROCONTROLLER, A/D's and D/A's (SIDE)
Size C
Document Number RB_H3
REV H
Date: August 12, 1999
Sheet 3 of 6

DUAL LOOP 359.72MHz FREQUENCY SYNTHESIZER

+10.00REF
R400 249K
R401 1.00M
C400 .1U
+18
R448 47
C437 .1U
U401A AD822
8.0V
R412 499
VCXO TEST POINT
J404
R409 301K
RF_XVCO
R410 100K/1%
C408 .01U
25Hz TO 350Hz BPF
PHASE_MOD
C409 .1U-MF
R415 24.9K
R416 24.9K
C410 .047U-MF
R413 499
R414 499
C411 .1U
VCO IS PHASE LOCKED TO 22.48252MHz CRYSTAL
+5
R402 47
R403 1K
C401 .1U
U400
MC145191
-CS_PLL
GATED_SPI_DATA
GATED_SPI_CLK
+10MHZ
C404 .1U
R404 100K
NOM:+5Vdc PLL_LOCK
C405 .1U
ASSIST FREQ LOCK AT START-UP
R429 10K
R446 10K
C438 .1U-MF
CRYSTAL IS PHASE LOCKED TO 10.000MHz
U401B AD822
R411 100K
C413 .1U
Y400 22.48252MHZ/3RD TURN AT 65C
J401
D400 MMBV609LT
D401 MMBV609LT
ADD D401 TO TUNE Y400 DOWN
TEST POINT
J405
C414 68P
C415 100P
L403 2.2UH
C417 1000P
U402 NE602
OSC V OSC OUT OUT RF RF G
C418 100P
R417 1.00K
R418 1.00K
R419 330
C420 .015U-MF
U403 OP27
R420 330
C419 .015U-MF
NOM:+13Vdc
+18
R421 270
C421 .1U
U404 POS-400
VT V RF
GGGGG
360MHz VCO
R422 301K
RF_VCO
R423 100K/1%
C422 .01U
R406 2.7M
C406 1000P
C407 .1U-MF
R405 39K
R407 10.0K
R408 30.1K
DUAL MODULUS SYNTHESIZER HAS SETTABLITY OF 1E-9.
C402 1000P
C403 1000P
R425 470
R428 47
C423 .1U
U405 MC12026D
M V IN OUT IN NC S G
C424 1000P
C425 1000P
R424 1K
DIVIDE BY 16
DIVIDE BY 16 TEST POINT
J402
J403 'SCOPE GND
R426 1K
C416 1000P
R427 1K
R445 22K
C439 .01U
OSCILLATOR/MIXER
359.72032MHz
359.72032MHz

RF_LEVEL
R430 49.9K
R431 1.00K
+18
R432 47
C426 .1U
R436 49.9K
R435 10.0K
C427 100P
R433 47
U406B LM358
R434 47
U406A LM358
R440 49.9K
R441 10.0K
C432 .1U
C428 1000P
OUTPUT AMPLIFIER WITH AGC FEEDBACK
L401 .018UH
C433 9.1P
359.72032MHz OUTPUT TO SRD (6.834,686GHz)
R437 10K
R438 301K
R442 4.99K
C434 7.5P
R443 47
J400 SMB-R
RF_AGC
C429 .01U
R439 100K/1%
L402 .18UH
C430 4.7P
L400 .018UH
Q400 NE461M02 4GHz NPN
C B E E
R450 22
C431 2.7P
0 TO -.40Vdc
R444 49.9
RF IS RECTIFIED BY SRD AND USED FOR GAIN CONTROL.

OCTAL 8-BIT DAC PROVIDES ANALOG CONTROL VOLTAGES

R447 100
+5
C436 .1U
U407 TLC5628
+2.048BUF
-STB_DAC8
GATED_SPI_DATA
-GATED_SPI_CLK
VDD REF1 REF2 LDAC LD DATA CLK GND
A B C D E F G H
RF_LEVEL
1PPS_DELAY
LAMP_TSET
XTAL_TSET
CELL_TSET
OSC_AMPL
PHASE_DEV
0 TO 4.00Vdc (EXCEPT 0 TO 2Vdc FOR PHASE_DEV)
R449 1.00M
LAMP_DRAIN
C440 .1U-MF

SOCKET TO BOTTOM (P/S) PCB

JP400 SOCKET20

1	P	
2	P	LAMP_PWR
3	S	LAMP_DRAIN
4	S	RF_XVCO
5	S	RF_VCO
6	S	RF_AGC
7	S	PHASE_DEV
8	D	PHASE_MOD
9	P	CASE_TSENS
10	S	PLL_LOCK
11	D	-CS_PLL
12	D	-STB_DAC8
13	D	+5
14	D	+18
15	P	+24_CLEAN
16	P	
17	P	LAMP_GATE
18	P	1PPS_DELAY
19	P	+24_HEAT
20	P	+12_LAMP

SOCKET TO TOP (ANALOG) PCB

JP401 SOCKET20

1	P	
2	P	LAMP_PWR
3	S	LAMP_GATE
4	S	LAMP_TSET
5	S	CELL_TSET
6	S	XTAL_TSET
7	S	OSC_AMPL
8	D	+2.048BUF
9	D	+10.00REF
10	P	CASE_TSENS
11	D	GATED_SPI_CLK
12	D	-GATED_SPI_CLK
13	D	GATED_SPI_DATA
14	D	+10MHZ
15	P	+5
16	P	+18
17	P	+24_CLEAN
18	P	
19	P	+24_HEAT
20	P	+12_LAMP

S=SOURCE OF SIGNAL ON THIS PCB
D=DESTINATION OF SIGNAL IS THIS PCB
P=PASS THROUGH OF SIGNAL ON THIS PCB

STANFORD RESEARCH SYSTEMS		
Title: 359.72032MHz FREQUENCY SYNTHESIZER (SIDE)		
Size: C	Document Number: RB_H4	REV: H
Date: August 12, 1999	Sheet 4 of 6	

SOURCE LAMP FROM +8V
SWITCH OVER TO +24V
WHEN Vout>6.25Vdc

U501
LM317

+24_HEAT

C500
2.2U-T35

R500
249

C502
2.2U-T35

+8_LAMP

D500
MBRD660CT

U502A
AD822

LAMP_DRAIN
(0-4Vdc FROM DAC)

Q500
MJD47

R501
100/1%

R502
49.9K

R503
10.0K

BOOTSTRAP 1.75Vdc
ABOVE OUTPUT VOLTAGE

R504
10.0

R505
10.0

R552
10.0

R553
10.0

0 < Vout < 24Vdc

LAMP_PWR

R506
10.0K

R507
10.0K

C504
1000P

U502B
AD822

R512
1K

LAMP_GATE

R508
100K/1%

R509
100K/1%

ADJUST GATE VOLTAGE
FOR Id=38mA+Vd*10mA/V

R510
249K
(OFFSET)

+8_LAMP

R511
49.9K
(SLOPE)

U503
LM317

+24_CLEAN

R513
249

C507
2.2U-T35

+18

U504
LM340-5

C506
2.2U-T35

R514
3.32K

+5

C508
2.2U-T35

BASEPLATE TEMPERATURE MEASUREMENT
(10mV PER DEGREE C)

U505
V+
OUT
GND
LM45

CASE_TSENS

R515
2.2K

HEADER TO FREQ SYNTHESIZER BOARD

JP500

1	P	
2	S	LAMP_PWR
3	D	LAMP_DRAIN
4	P	RF_XVCO
5	P	RF_VCO
6	P	RF_AGC
7	P	PHASE_DEV
8	P	PHASE_MOD
9	S	CASE_TSENS
10	P	PLL_LOCK
11	P	-CS_PLL
12	P	-STB_DAC8
13	S	+5
14	S	+18
15	D	+24_CLEAN
16	P	
17	S	LAMP_GATE
18	D	1PPS_DELAY
19		+24_HEAT
20		+8_LAMP

PIN20

HEADER TO CPU PCB

JP501

1	P	
2	S	1PPS_SLEW
3	P	RF_XVCO
4	P	RF_VCO
5	P	RF_AGC
6	P	PHASE_DEV
7	P	PHASE_MOD
8	P	PLL_LOCK
9	P	-STB_DAC8
10	P	-CS_PLL
11	D	1PPS_CPU
12	S	+5
13	S	+18
14	P	
15	D	1PPS_SEL0
16	D	1PPS_SEL1
17	D	1PPS_TAG
18	D	EN/-CLR
19	D	E_CLK
20	D	-10MHZ
21	S	TIME_LATCH
22	S	INTERPOLATE

PIN22

C516 .1U
C517 .1U
C518 .1U
C519 .1U
C520 .1U
C521 .1U

1PPS_TAG

ENABLE

U506A
74HC74-5

EN/-CLR

ARM

U507A
74HC74-5

GATE

U507B
74HC74-5

U506B
74HC74-5

1PPS_CPU

U508A
74HC74-5

SYNC

U508B
74HC74-5

END

100NS<GATE<500NS

Q502
MMBR5179
(0/10.8mA)

R519
2.00K

TIME_LATCH

R520
499

FRACTIONAL E-CLOCK INTERPOLATOR
FOR TIME-TAGGING 1PPS INPUT.

R516
10.0K

R517
1.00M

-2.4mV/C

12.0V

Q501
MMBT5087LT1
(5.4uA)

R518
20.0K

R521
15.0K

11.4Vdc

R522
1.00K

D504
BAV170LT1

D501
BAV170LT1

R523
24.9K

C509
1000P

R524
47

C511
1000P

R550
1.00M

11.0Vdc

R525
1K

C510
2.7P

U509
LP311M

INTERPOLATE

2000X PULSE STRETCHER
"INTERPOLATE" GOES LOW
FOR 2000X GATE WIDTH

(SEPARATE DIODES TO AVOID
PARASITIC TRANSISTORS)

U500
74HC574-5

E_CLK

-10MHZ

E_0
E_90
E_180
E_270

U510
74HC153-5

1PPS_0
1PPS_100
1PPS_200
1PPS_300

1PPS_SEL0
1PPS_SEL1

0 TO 100NS ANALOG DELAY FOR
BOTH RISING AND FALLING EDGES.

R526
20.0K

R527
15.0K

4.0V

R528
10.0K

U512A
AD822

D502
BAW56LT

1PPS_DELAY
(0 TO 4Vdc)

R529
10.0K

R530
10.0K

U511B
AD822

R531
10.0K

R532
10.0K

8V-DAC/2

R540
4.99K

R533
3.9K

R534
10.0K

R539
2.7K

R541
4.99K

D503
BAV70LT

U511A
AD822

10V

R536
10.0K

U512B
AD822

R537
10.0K

R538
10.0K

10V+DAC/2

R542
4.99K

R543
2.00K

13.3Vdc
TO 16.96

Q503
MMBTH81LT1

C514
.1U

R548
390

+/-2.1mA

R547
47

C513
120P

R544
11.3K

C512
.1U

1.04Vdc
TO 5.20

Q504
MMBTH10LT1

R545
1.00K

R546
2.00K

C515
1000P

ABOUT 9Vdc

R551
1K

1PPS_SLEW

U514
AD790JR

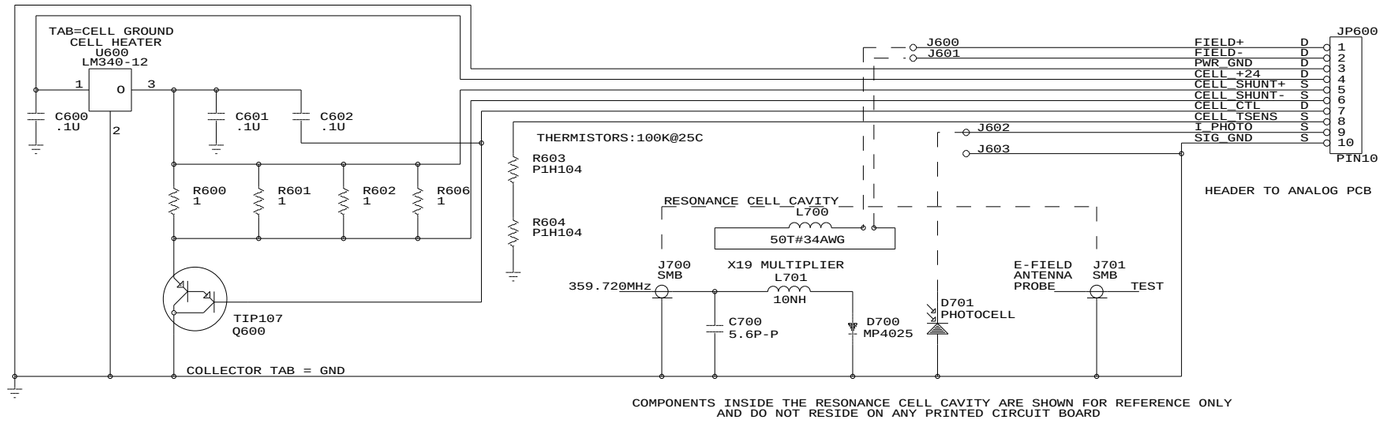
74HC PARTS HAVE
POWER CALLED VCC5

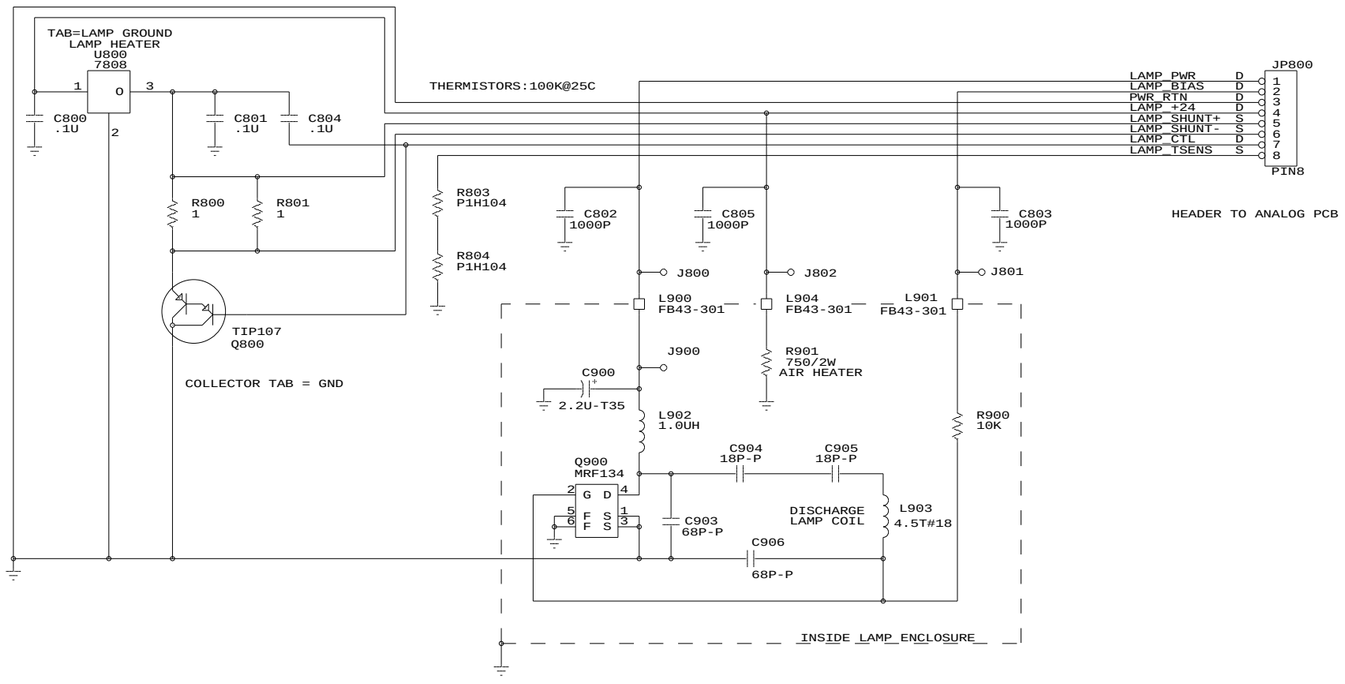
VCC5

VSS

S=SOURCE OF SIGNAL ON THIS PCB
D=DESTINATION OF SIGNAL IS THIS PCB
P=PASS THROUGH OF SIGNAL ON THIS PCB

STANFORD RESEARCH SYSTEMS		
Title: POWER SUPPLIES AND 1PPS TIMING (BOTTOM)		
Size: C	Document Number: RB_H5	REV: H
Date: August 12, 1999	Sheet 5 of 6	





REFERENCE DESIGNATORS:

600's ARE PART OF CELL HEATER
700's ARE INSIDE RESONANCE CELL
800's ARE PART OF LAMP HEATER
900's ARE PART OF DISCHARGE CIRCUIT

S=SOURCE OF SIGNAL ON THIS PCB
D=DESTINATION OF SIGNAL IS THIS PCB
P=PASS THROUGH OF SIGNAL ON THIS PCB

STANFORD RESEARCH SYSTEMS		
Title: RESONANCE CELL AND DISCHARGE LAMP		
Size: C	Document Number: RB_H6	REV: H
Date: August 12, 1999	Sheet 6 of 6	

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