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SMT320v4

User Guide

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Author:	Fabio Ancona	Original Date:	5 March 1998

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Revision History

Date	Comments	Engineer	Version
5/03/98	SMT320v2 and SMT320v3	LeoM	1.0
23/08/00	Upgrade to SMT320v4	FabioA	2.0

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1. Introduction

This document explains the testing and initialisation of the SMT320.

The SMT320 is a TIM-40 standard PCI compatible carrier board. Features include:

- Four TIM sites which can accommodate module sizes of 1, 2, 3 & 4.
- Global bus interface on TIM site 1 for high speed host communication; Data Rate up to 50Mbytes/s.
- XDS-510 emulation for debugging using GO-DSP's Code Composer.
- Host interface to comm-port at full bandwidth up to 4Mbytes/s
- Fully re-configurable comm-port topology using FMS cables.
- Comport control: Interconnection of on-board comports can be selected by IO mapped registers controlling quick switches.
- Flash memory: Xilinx device is configured from Flash memory and may be upgraded in the field.
- Tim Connectors: Now uses zero height TIM connectors.

To accommodate four TIMs the SMT320 board height is 120mm, this is 14mm greater than the PCI standard. In all other respects the board complies with the standard.

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2. Installation and Testing the SMT320

- Insert a TIM card into TIM site 1. With the power to the host system switched off and taking anti-static precautions, (e.g., wearing an anti-static earth strap), plug the SMT320 into the PCI slot. Ensure that the SMT320 is located correctly.

If in the Site1 of the SMT320 you have got a C6x-based TIM then:

- If you use the Diamond host server ensure that the carrier board environment variables are set up correctly and run a confident test as described in chapter 1 (sections 1.5 and 1.6) of the 3L Diamond User Guide for C6000 and in the Diamond Board Support Package Release Note.
- Both the Diamond host server and the SMT6015/SMT6000 (Sundance Servers) communicate with the hardware via one of the following Sundance device-driver products: SMT6010 (driver SDK, WinNT), SMT6011 (only driver, WinNT), SMT6020 (driver SDK, Win9x), SMT6021(only driver, Win9x).
- Code Composer Driver Software: install the appropriate SMT320 driver by installing the SMT6012.

If in the Site1 of the SMT320 you have got a C4x-based TIM then:

- Ensure that the carrier board environment variables are set up correctly and run a confident test as described in chapter 1 of the 3L Diamond User Guide for C4x (sections 1.3, 1.4, 1.5, 1.6 and 1.7 of the User Guide). If you work under WinNT you have to set also the following environment variable: TISLINK = SMT320, INDEX:0 (see 3L's *C40 Technical Note 62*).
- The Diamond host server communicates with the hardware via the SMT6320 (Sundance device-driver product) under WinNT and it does NOT need any driver under DOS and under Win9x.
- The SMT6015 (Sundance Server) communicates with the hardware via one of the following Sundance device-driver products (you do NOT need to set any environment variables): SMT6010 (driver SDK, WinNT), SMT6011 (only driver, WinNT), SMT6020 (driver SDK, Win9x), SMT6021 (only driver, Win9x).
- Code Composer Driver Software: install the appropriate SMT320 driver by installing the SMT6012.

The user can not put any TIMs on the SMT320 when it wants to use the carrier board as a stand-alone JTAG master (XDS510): this part is covered by the SMT6012 *User Guide* (Code Composer Driver Software).

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Comm-Ports.

2.1. Comm-Port Layout

See SMT320.pdf document included in the SMT320 package.

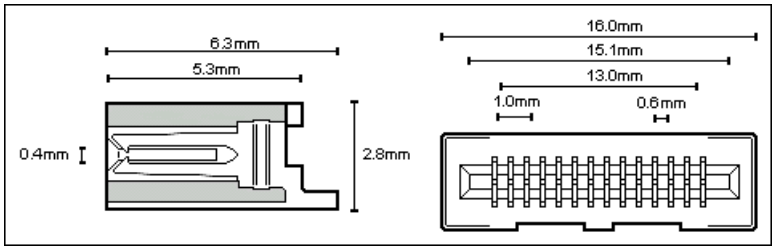
The CP3 on TIM Site1 is connected to the CP interface on the SMT320 which will allow data transfers through the PCI bus.

2.2. PCI Supplementary Power Connection

The PCI specification for power over the PCI connector is limited to 25Watts. If more power is required the supplementary power connector on the SMT320 must be used.

2.3. FMS Comm-port Connection & Pin Out

Note that when connecting comm-ports with the FMS cables, to ensure pin 1 is connected to pin 1 on the alternative comm-port. One end of the cable must be inserted opposite to the other, I.E. on one the blue backing must be facing out and on the other the silver of the connectors must be facing outwards.



Signal	Pin No.	Function	Type
CxD(0-7)	2-9	Comm-Port DataBus	I/O
CREQx	10	Comm-Port Token Request	I/O
CACKx	11	Comm-Port Token Acknowledge	I/O
CSTRBx	12	Comm-Port Data Strobe	I/O
CRDYx	13	Comm-Port Ready	I/O

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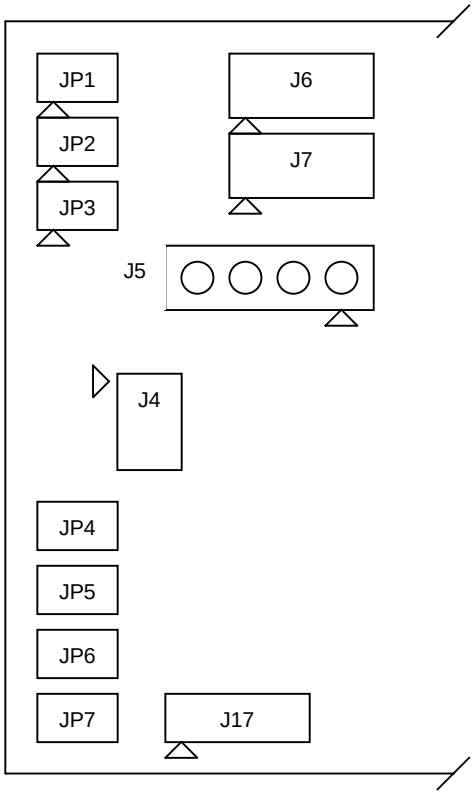
3. Connector layout and Assignments



3.1. Bus Reset (JP1/JP2)

BUSRST_L	1	2	GND

BUSRST_L is an active low bi-directional signal that can be driven by an external source. The external source must use an open-drain or open-collector signal.

3.2. Reset Input (JP3)

RSTIN_L	1	2	GND

RSTIN_L is an active low input signal that can be used to reset the board.

3.3. JTAG-IN Connector (J6)

TRST_L	GND	POL	GND	GND	GND	EMU1
2	4	6	8	10	12	14
1	3	5	7	9	11	13
TMS	TDI	+5V	TDO	TCK	TCK	EMU0

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The JTAG-IN connector can be used to debug the processors on the board from an external source. This connection does not operate unless JP7 is fitted. Note that +5V is emitted on pin 5 to enable detection of the port by a master XDS510 device.

3.4. JTAG-OUT Connector (J7)

TRST_L	GND	POL	GND	GND	GND	EMU1
2	4	6	8	10	12	14
1	3	5	7	9	11	13
TMS	TDI	PD	TDO	TCK	TCK	EMU0

The JTAG-OUT connection can be used to extend the on-board JTAG chain to an external device. This port does not operate unless the PD pin is pulled high by the slave device. PD is pulled low by a 1K0 resistor.

3.5. Config & Reset Connector (J4)

GND	1	2	CONFIG_L
GND	3	4	EXRST_L
GND	5	6	BUSRST_L
NC	7	8	NC

This connector is a collection of signals for use only within a PC. The signals are not suitable for driving long cables but can be safely used between boards in the same machine.

3.6. Option Jumpers (JP4 to JP7)

These jumpers can be fitted to alter the behaviour of the board.

JP4 to JP6 currently have no function.

JP7 must be fitted to enable the JTAG-IN connector.

3.7. Xilinx JTAG Header (J17)

1	2	3	4	5	6	7	8	9
+5V	GND		TCK	TDO		TDI		TMS

The Xilinx JTAG header is reserved for board configuration and update.

IMPORTANT. TDO is on pin 5 instead of 6 for REV 4.0 PCB.

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4. Multi board Reset

The SMT320 has a reset connection available on JP1. The 2 pin header may be used to link multiple SMT320 carrier boards to provide a simultaneous reset to all processors. This is important in systems which have comport connections between carrier boards.

The connection is shown below.

1	2
!RST	GND

The !RST signal is designed for wired-OR configuration and is active low. A pull up resistor is fitted to !RST on each SMT320. A maximum of four SMT320's may be daisy chained together.

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5. Registers

In target mode, the SMT320 is accessed by a host device across the PCI bus. This allows access to the target mode registers. The operating system or BIOS will normally allocate a base address for the target mode registers of each SMT320. Access to each register within the SMT320 is then specified by this base address and the offset shown in the table below.

The I/O address space is decoded as shown in the table below.

Offset	Register(Write)	Register(Read)	Width
0	-	-	
+4	-	-	
+8	-	-	
+0C	-	-	
+10	COMPORT_OUT	COMPORT_IN	32
+14	CONTROL	STATUS	32
+18	INT_CONTROL		32
+1C	-	-	
+20 to +3F	Not used	Not used	
+80 to +AF	TBC Write	TBC Read	16

5.1. Comport Registers (Offset 10h)

The host is connected to the first TIM site using comport 3. This port is bi-directional and will automatically switch direction to meet a request from either the host or the C40. Both input and output registers are 32 bits wide. Data can only be written to COMPORT_OUT when STATUS[OBF] is 0. Data received from the C40 is stored in COMPORT_IN and STATUS[IBF] is set to 1. Reading COMPORT_IN will clear STATUS[IBF] and allow another word to be received from the C40.

5.2. Control Register (Offset 14h)

The CONTROL register can only be written. It contains flags which control the boot modes of the first TIM site.

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Boot Control

Bit	7-5	4	3	2	1	0
Name	Not used	notNMI	IIOF2	IIOF1	IIOF0	RESET

RESET	Write a 1 to this bit to assert the reset signal to all TIM modules on the SMT320.
IIOF0 IIOF1, IIOF2	These bits connect to the corresponding pins on the first TIM site. These bits are open-drain and can only pull down. If not required before or after booting they should be written with 1's.
NotNMI	A 0 written to this bit will assert the active low NMI to the TIM1 C40.

Note. On PCI system reset, RESET is asserted to all TIM sites.

5.3. Status Register (Offset 14h)

The STATUS register can only be read.

Bit	31:22	21	20	19	18	17	16
Name	X	CONFIG_L	TBC RDY	0	MASTER	IBF	OBF

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	INTA

Bit	7	6	5	4	3	2	1	0
Name	C40 INT	TBC INT	IBF INT	OBE INT	C40 IE	TBC IE	IBF IE	OBE IE

OBE IE	Set if comport output buffer empty interrupts enabled.
IBF IE	Set if comport input buffer full interrupts enabled
TBC IE	Set if JTAG interrupts enabled
C40 IE	Set if interrupt from TIM1 C40 enabled
OBE INT	Set if comport output buffer becomes empty. Cleared by writing a 1 to the corresponding bit in the interrupt control register.
IBF INT	Set if comport input buffer receives a word. Cleared by writing a 1to the corresponding bit in the interrupt control register

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TBC INT	Set when the TBC asserts its interrupt. Cleared by removing the source of the interrupt in the TBC.
C40 INT	Set when the TIM1 C40 sets its host interrupt bit. Cleared by writing a 1 to the corresponding bit in the interrupt control register.
INTA	This is a logical OR of bits 7 to 4 in this register gated with each ones enable bit.
OBF	Set when a word is loaded into the comport output register. Cleared when the word is transmitted to the C40.
IBF	Set when a word is received into the comport input register from the TIM1 C40.
MASTER	When set, the comport interface token is owned by the SMT320 bridge.
TBC RDY	Reflects the current state of the TBC RDY pin. This bit is active high and therefore and inversion of the TBC pin.
CONFIG_L	Reflects the current state of the CONFIG signal from the TIM1 C40. Active low.

5.4. Interrupt Control Register (Offset 18h)

This write-only register controls the generation of interrupts on the PCI bus. Each interrupt source has an associated enable and clear flag. This register can be written with the contents of bits 7:0 of the Status Register.

Enable Group

Bit	7	6	5	4	3	2	1	0
Name	CLEAR C40 INT	0	CLEAR IBF INT	CLEAR OBE INT	C40 IE	TBC IE	IBF IE	OBE IE

IBF IE	Input Buffer Full Interrupt Enable. Allows an interrupt to be generated when the host comport input register is loaded with data from the C40.
OBE IE	Output Buffer Empty Interrupt. Allows an interrupt to be generated when the host comport register has transmitted its contents.
TBC IE	Test Bus Controller Interrupt Enable. Interrupts from the Texas JTAG controller are enabled when set.

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C40 IE	C40 Interrupt Enable. Allows a programmed interrupt to be generated by the C40 when set.
CLEAR OBE INT	Write a one to this bit to clear the interrupt resulting from a comport output event.
CLEAR IBF INT	Write a one to this bit to clear the interrupt event resulting from comport input.
CLEAR C40 INT	Write a one to this bit to clear down the C40 INT event.

The JTAG controller, that generates TBC INT, must be cleared of all interrupt sources in order to clear the interrupt.

5.5. Test Bus Controller-TBC (Offsets 80h-AFh)

Refer to the Texas 74ACT8990 data manual for register usage.

The clock for the TBC is 1/4 the PCI clock rate. So for a standard PCI slot this will therefore clock the 74ATC8990 at 8.3 MHz approximately.

The offsets and write / read capability of all TBC registers is shown below.

Offset (hex)	Write	Read
80	Control0	Control0
82	Control1	Control1
84	Control2	Control2
86	Control3	Control3
88	Control4	Control4
8A	Control5	Control5
8C	Control6	Control6
8E	Control7	Control7
90	Control8	Control8
92	Control9	Control9
94	Minor Command	Minor Command
96	Major Command	Major Command
98	Counter 1 Update 0	Counter 1 Update 0
9A	Counter 1 Update 1	Counter 1 Update 1
9C	Counter 2 Update 0	Counter 2 Update 0

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9E	Counter 2 Update 1	Counter 2 Update 1
A0	-	Status 0
A2	-	Status 1
A4	-	Status 2
A6	-	Status 3
A8	-	Capture 0
AA	-	Capture 1
AC	-	Read Buffer
AE	Write Buffer	-

The organisation of the TBC registers is of a stack of 16 bit registers aligned to 16 bit boundaries. They are however accessed using both lower and upper 16 bits of the PCI bus.

IMPORTANT. Only 16 bit I/O operations should be used to access the TBC registers and each transfer must be WORD aligned.

The state of the TBC RDY signal can be tested in the Status register.

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6. Revision 4 Additional Registers

The SMT320 Revision 4 includes a CPLD to control the JTAG, buffered ports and comport switches. New registers have been added to allow the functionality of these resources to be accessed. In most cases, the board is compatible with Revision 3 and no software changes are required.

The registers in the PCI FPGA are accessed using I/O transactions and can be 16 or 32 bit depending on the region accessed.

6.1. Register Map

Offset	Register(Write)	Register(Read)	Width
0	-	-	
+4	-	-	
+8	-	-	
+0C	-	-	
+10	COMPORT_OUT	COMPORT_IN	32
+14	CONTROL	STATUS	32
+18	INT_CONTROL	-	32
+1C	-	LAST PCI ADD	32
+20 to +3F	Not used	Not used	
+40 to +7E	Reserved	Reserved	32
+80 to +AF	TBC Write	TBC Read	16
+C0 to +CF	CPLD Write	CPLD Read	16

The new registers are from offset C0 to CF and exist in 16 bit I/O space. These registers however only use 8 bits of data.

Offset	Register(Write)	Register(Read)
C0	Flash Data	Flash Data
C2	Flash Data ++	FA[7:0]
C4	Flash Add [7:0]	FA[15:8]
C6	Flash Add [15:8]	FA[18:16]

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C8	Flash Add [18:16]	BEX[7:0]
CA	Comport Control	BEX[15:8]
CC	Interrupt Control	BEX[16]
CE	-	Version

6.2. Flash Registers

The flash device is a standard device of 512k x 8 capacity, typically an AMD29LV040. The address for the flash must be written to the registers (C4, C6, C8) before access. Once the address is written data can be written or read via C0. Writing flash data to C2 will result in the address auto incrementing. The flash address can be readback via (C2, C4, C6).

6.3. Comport Control

The register at offset CA controls the state of the quick switches connecting the 4 TIM sites and the buffered comport. The bits in this register are named BEX[16:0] and control the comports as shown in the table below. The order of writing these bits is : BEX[16] followed by BEX[15:8] and BEX[7:0]. These bits operate as a byte pipeline and all 3 bytes must be written.

BEX[]	From	To
0	T4C3	LINKC
1	T3C3	T4C0
2	T2C3	T3C0
3	T1C3	T2C0
4	LINKC	T1C0
5	T4C2	LINKB
6	T3C2	T4C5
7	T2C2	T3C5
8	T1C2	T2C5
9	LINKB	T1C5
10	T4C1	LINKA
11	T3C1	T4C4
12	T2C1	T3C4
13	T1C1	T2C4

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14	LINKA	T1C4

BEX[n] = 0 Connects the link

BEX[n] = 1 Routes ports to FMS

BEX[16:15]	From	To
00	BCFMS	BCOM
01	No connect	No connect
10	Host	T1C3
	BCFMS	BCOM
11	Host	BCOM
	BCFMS	T1C3

BCFMS = Buffered comport access FMS

BCOM = Buffered comport

Host = PCI FPGA host comport

The default state is for BEX[16:15] = 2'b10, BEX[14:10] = 5'b11111, BEX[9:5] = 5'b00000 and BEX[4:0] = 5'b11111;

This enables a pipe around the board between comports 2 and 5 whilst enabling the host onto T1C3. The buffered comport is left connected to its FMS and available for any TIM to use.

6.4. Interrupt Control

This board supports interrupts between TIM sites using the IIOF0 bit. By default the IIOF lines are not affected.

The register is defined below.

7	6	5	4	3	2	1	0
T4IIOF[1:0]		T3IIOF[1:0]		T2IIOF[1:0]		T1IIOF[1:0]	

Each pair of bits is decoded to allow the routing of IIOF bits to take place. For each TxIIOF pair, the decoding is different so careful use is advised.

T1IIOF[1:0]	TIM1 IIOF0=

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00	High Z
01	TIM2 IIOF0
10	TIM3 IIOF0
11	TIM4 IIOF0

T2IIOF[1:0]	TIM2 IIOF0=
00	High Z
01	TIM1 IIOF0
10	TIM3 IIOF0
11	TIM4 IIOF0

T3IIOF[1:0]	TIM3 IIOF0=
00	High Z
01	TIM1 IIOF0
10	TIM2 IIOF0
11	TIM4 IIOF0

T4IIOF[1:0]	TIM4 IIOF0=
00	High Z
01	TIM1 IIOF0
10	TIM2 IIOF0
11	TIM3 IIOF0

Each TIMnIIOF0 line is driven using an open drain output from the CPLD and maintains the polarity of the originating IIOF.

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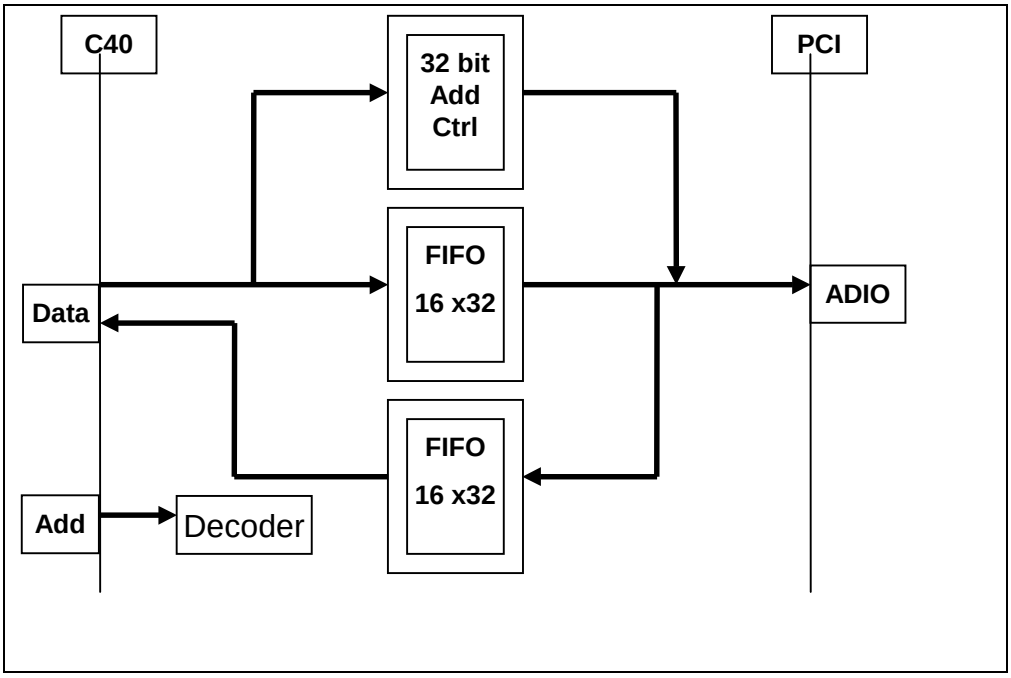
7. Bridge - C4x/C6x Operation.

The first TIM position on the SMT320 makes use of the global bus to allow the C4x/C6x to read and write the entire PCI address space. Burst mode and single transfers can be used to access the PCI address space.

The C4x/C6x can access any PCI location but it should be noted that data written and read will always be long word aligned and 32 bits



wide. The table below illustrates the available registers.

Address	Register(Write)	Register(Read)	Width
C0000000	FIFO	FIFO	32
C0400000	PCI Address	-	32
C0800000	Control	-	2

7.1. FIFO

The SMT320 incorporates 16 deep x 32 wide FIFO buffers on both read and write paths between the C4x/C6x and PCI bus. The FIFO is only effective when burst mode is enabled in the control register. With burst mode disabled, the bridge will request the PCI bus for each word transferred.

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With burst mode enabled, data written to the empty FIFO will be absorbed until 16 words make the FIFO full. This state will trigger a PCI burst write of 16 words in length thus transferring 64 bytes to the destination. The FIFO can be written with the next 16 words during the PCI burst transaction to maintain throughput. The C4x/C6x may incur wait states if the FIFO becomes full during this time.

For burst mode read transactions, reading from the empty FIFO will trigger a PCI burst of 16 words from source memory, filling the FIFO with 64 bytes of data. The C40 will be able to read the first word of data as soon as it is loaded into the FIFO from the PCI bus.

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