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SUNDANCE

SMT328

4 Site VME TIM Carrier User Guide

Certificate Number FM 55022

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Revision History

Date	Comments	Engineer	Version
30/11/00	Loaded the old file contents into the latest document template and changed some of the table layouts.	MA	6.0
24/01/01	Revised text to include answers to FAQs. Board rev 2 changes included.	SEC	7.0
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Features

- Four site TIM carrier
- Flexible comm-port linking
- All 6 front panel comm-ports fully buffered
- Double pipe architecture – TIM comm-ports unbuffered
- Global board resources
- 1MByte of one-wait-state SRAM accessible by TIM sites or VME
- JTAG debugging circuit - accessed as Slave
- On board comm-port interface to VME

Architectural Overview

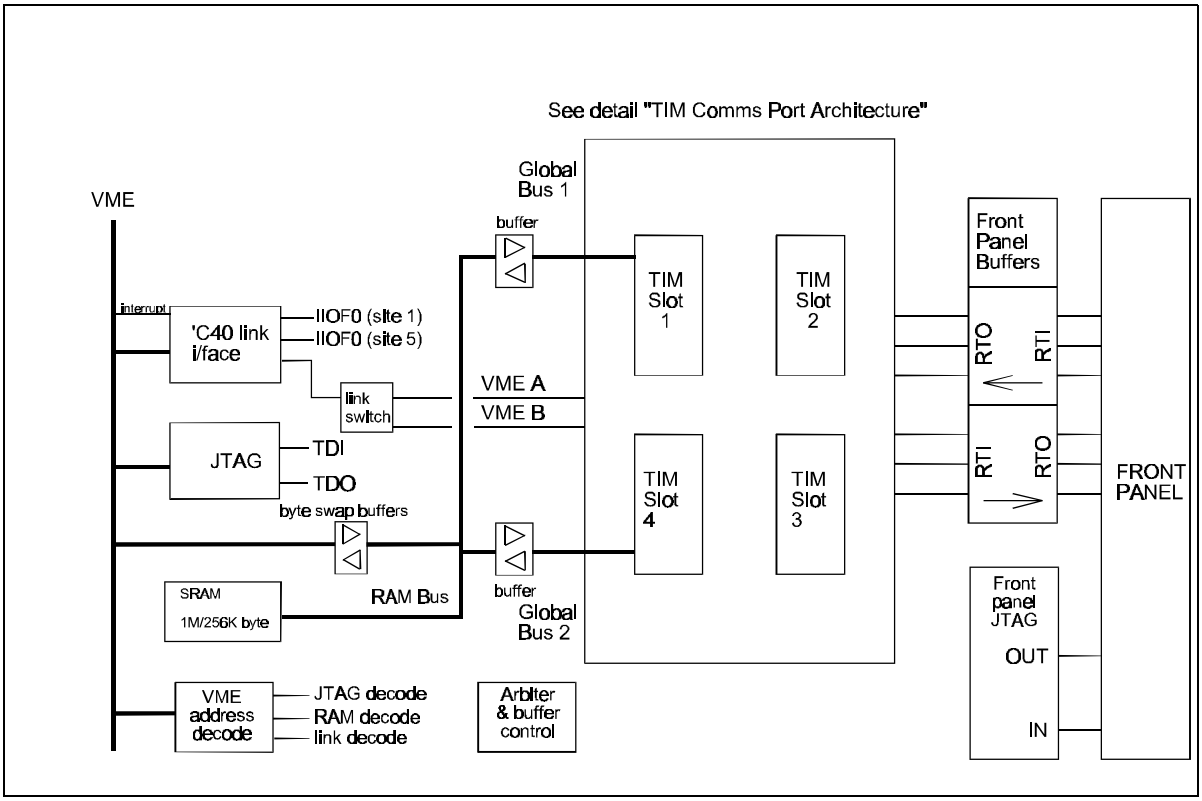


Figure 1: VME Carrier Architecture

This description should be read with reference to the diagram titled ‘VME Carrier Architecture’. Note that the layout of TIM sites on the board is in the same order as shown in the diagram.

Comm Ports Resources

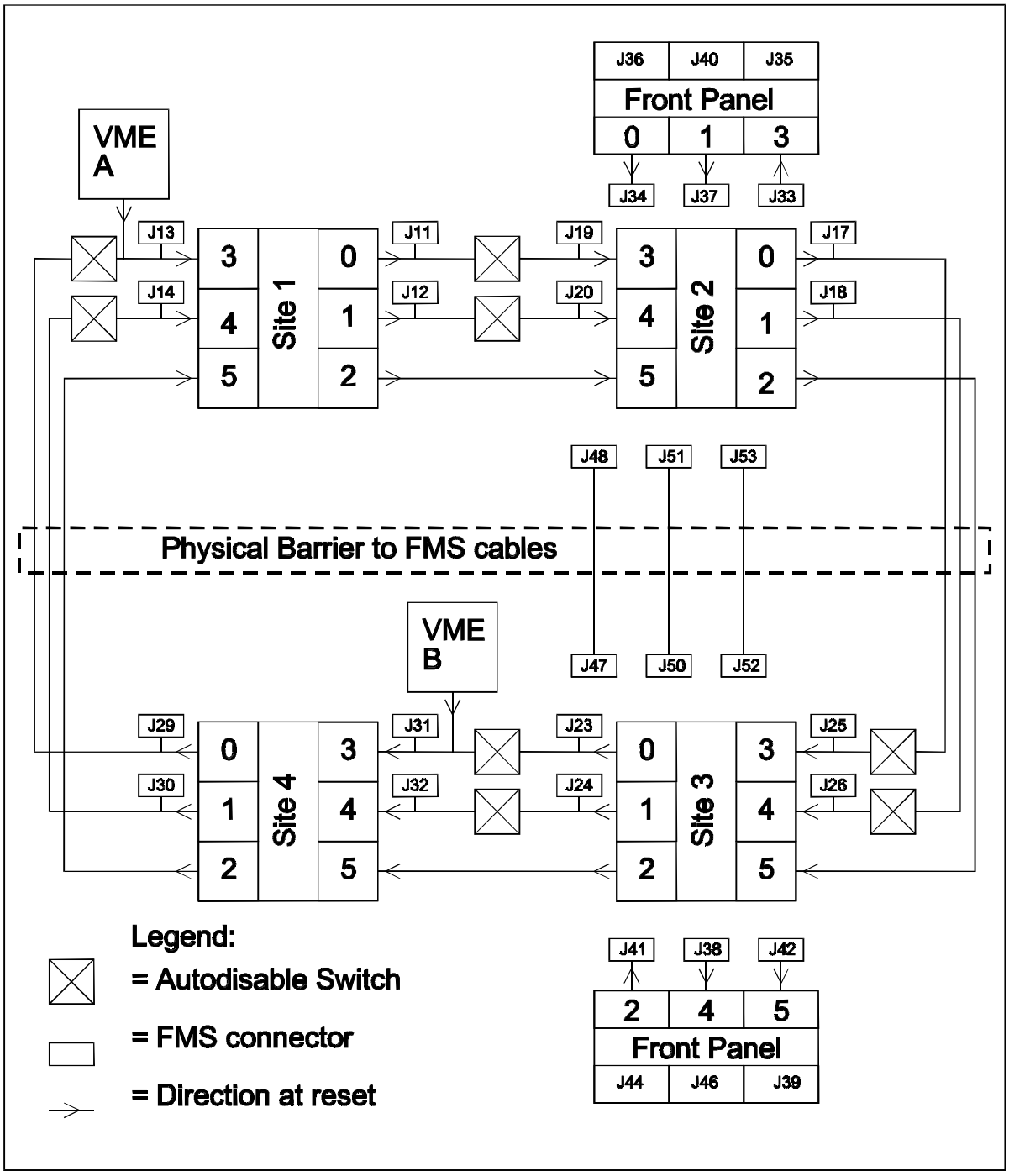


Figure 2: TIM Comm-port Architecture

The TIM comm-ports are connected as 3 off circular pipelines, with TIM sites 1 and 4 also having default access to the VME comm-port.

Comm-ports 2 to 5 are hardwired. Comm-ports 0 to 3 and 1 to 4, are wired to an analog switch with an FMS connector fitted on either side of the switch. Inserting an

FMS cable between any Reset To In (RTI) and any Reset To Out (RTO) comm-port disables their respective analog switches. Comm-ports 0-2 are RTO, Comm-ports 3-5 are RTI.

FMS cables must be used to connect the 6 Front Panel Comm-port FMS connectors. Front Panel comm-ports 0-2 are RTO at the FMS connector and RTI at the Front Panel connector, comm-ports 3-5 are RTI at the FMS connector and RTO at the Front Panel connector.

There are 3 unconnected through routes which bridge the physical barrier on the board. They allow the implementation of tree topologies.

When enabled by a board jumper, the VME comm-ports disable the associated analog switch, leaving comm-port 0 on TIM 4 and TIM 3 unconnected. The VME comm-ports can be disabled by the board jumper, which also enables the associated analog switch.

There are a total of 28 FMS connectors: 16 are connected to TIM comm-ports and their auto-disable switches, 6 are connected to the front panel buffers, and 6 are connected to 3 uncommitted routing pipes which traverse the physical barrier of the TIM connectors.

The 28 FMS connectors are split into 2 physically separate groups of 14, each of which is divided into 2 facing rows of 7. Each FMS site is 18mm wide, so each row of 7 is 126mm wide, and occupies almost all of the 130mm available. The facing rows are spaced 64mm apart, so that an unobstructed channel 64mm by 128mm is available for laying FMS cables. An FMS cable is 15mm wide, so 4 cables can be laid side by side, along the length of the routing channel, before cables need to be stacked. The rows are arranged so that each FMS connector, is physically as close as possible to the TIM connector or front panel buffer, to which it is connected.

Global Bus Resources

There are three global bus resources available on this motherboard. These are the 32 bit VME bus, the 1 Megabyte static Dual Port RAM (DPR), and the board control registers.

The two TIM sites with a global bus connector are the two nearest the VME connectors, at sites 1 (nearest P1) and 4 (nearest P2). The DPR bus also allows the TIMs to act as a VME bus master, whilst another VME bus master can access the DPR.

The DPR is organised to allow the VME bus master to perform D8, D16 or D32 cycles, 16 bit word swapping buffers are included for this purpose. The DPR access time is 12ns, and the TIMs are connected to this DPR through fast (approximately 5ns) buffers. This allows ‘C4x accesses to be performed with zero wait states. The DPR is decoded at TIM addresses 0xDFFC0000 and upward (on ‘C4x STRB1).

Access to the global resources is selected by arbitration state machines. Resources remain granted to the last resource master after the cycle has finished. Arbitration only occurs when two (or more) possible bus masters are requesting the same resource. Arbitration takes two ‘C4x cycles. Because VME bus arbitration and Global Bus Resource arbitration are separate, a deadlock situation can occur. This deadlock is only possible when a TIM starts a VME bus master cycle around the same time that another VME bus master starts a cycle to access the DPR. This situation is

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resolved by signaling ‘Bus Error’ to the existing VME bus master, which is forced to abort its’ VME bus cycle. This cycle may be re-tried after a short delay (a few microseconds) to allow the TIM VME cycle to complete. This possibility must be taken into account when designing system software.

VME to Comms Port Interface

The ‘C4x VME interface, is designed to allow a VME bus master to perform D16 or D32 cycles, to access the comm-port interface register. These accesses are converted to the correct protocol for communicating via a ‘C4x comm-port. This logic and associated circuitry includes double buffering on reads and writes negating the need for an external FIFO. The comm-port which is connected to this interface can be switched to either of the two TIMs which have global access (TIM1 or TIM4).

Link switch SW2 is provided to allow manual disabling of either the TIM1 or TIM4 or both VME to Comms port interface. When a VME comms port is disabled with SW2, the TIM comm port is automatically connected to the adjacent TIM instead (see Figure 2). To disable the VME interface to TIM1 fit a link between SW2 pins 1 and 4 which are both nearest the front panel. To disable the VME interface to TIM4 fit a link between SW2 pins 2 and 3 which are both furthest from the front panel.

JTAG

A Texas Instruments Test Bus Controller (TBC) can be used to control the JTAG daisy chain between TIMs. This means that the SMT328 can be used as a Jtag Slave.

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Interrupts

A single FPGA interrupt controller co-ordinates all interrupts. It contains a status register showing unmasked interrupt sources, and 3 mask registers. These allow the interrupt sources to be masked, before they are logically ORed, to generate 3 separate interrupt inputs, one for each of the global TIM sites and one for the VME bus.

A VME interrupt, with programmable level, can be generated by either global access TIM. From each of these TIMs, the IIOF0 signal is connected to the interrupt FPGA, and the assertion of this line generates the interrupt if it is unmasked. The interrupt is cleared by the VME master, when it masks the source of the interrupt.

The Global TIM sites have 2 interrupt sources:

A latched copy of VME bus error.

A software settable interrupt.

The VME bus has 6 interrupt sources:

A software settable interrupt.

The JTAG controller (currently not in use).

TIM1 IIOF0 output

TIM4 IIOF0 output

VME comm-port RXFUL

VME comm-port TXEMPTY

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VME Interface

The VME interface uses the P1 connector and the center row (B) of the P2 connector for additional data and address lines. The interface forms a complete D8/16/32 master/slave. The card does not support slot 0 operation, block transfers or unaligned transfers. The outer rows (A and C) of the P2 connector are not connected. The P2 input signals are connected to 10K Ohm pull ups to +5V so that operation is possible without a P2 back plane. In this configuration all transfers must be 16 bits and the I/O and DPR spaces must be set to addresses in the range: 0xFF000000 to 0xFFFFFFFF.

VME Slave Interface

There are 3 decoded address spaces:

Name	VME space	Size in Bytes	Description
VME configuration	A16	64	Identification and programmable base addresses for I/O and DPR.
I/O	A32	256	JTAG, Comm-port, Board Reset, Control 1
DPR	A32	1M	Dual Port Ram

The A16 VME configuration base address is set with an 8 way link block labelled SW1. This sets the value to compare to VME A6-A13, with A14-A15 always compared to 1 in order to generate a board decode. This A16 address space contains board identification registers and a pair of 16 bit registers which must be loaded with the base address of the I/O and DPR spaces.

VME Master Interface

The card can support D8, D16 and D32 transfers in A16, A24 and A32 address spaces. The TIM global data bus signals drive the VME data bus through buffers, but no byte or word swapping is performed. That is a D8 transfer to VME address 0x0000 would need the significant data to be in the ‘C4x data bits 7..0. A D8 transfer to address 0x0001 would need the significant data to be in the ‘C4x data bits 15..8. etc.

No support is provided for accessing words or long words across long word boundaries. i.e., all transfers must be within long word boundaries.

The ‘C4x address lines A0..A21 drive the VME address lines A2..23. The VME DS signals and the VME address bits A1, A24-31, AM0-5, LWORD are set by the

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contents of Control register 4. This requires the use of a 4M Word ‘C4x address region for VME m0000aster access.

There is a 3 way arbiter which allows the programmer to write VME access code for both TIM 1 and 4 without having to do any hardware checking. Cycles which clash will simply wait for the other TIM to finish.

VME Configuration Registers

Offset (hex)	Register
00	Board ID
02	Device type
04	Status / Control
06	DPR base address
08	I/O base address
0A-1D	Unused
1E	Manufacturer ID
20-3F	Unused

The address of this configuration register block is defined by an 8-bit DIL switch (LK1). It is only accessed in A16 address space. The top two address lines (A14 and A15) must be ‘1’. The base address (set by links at SW1) is compared to address bits A6 to A13. The address bits A1 to A5 select which register to access.

With no links fitted to SW1 A6-A13 must be 1 to decode the A16 space. Fitting a link at SW1 pin 1 (nearest the PCB corner) sets the decode for A13 to 0, and a link at SW1 pin 8 sets the decode for A6 to 0, etc.

For example:

Address 0xC000 = All links fitted.

Address 0xD000 = All links fitted except at pin 2

Address 0xF800 = All links fitted except at pins 1,2,3.

Address 0xFFC0 = No links fitted.

The VME address modifiers must be set to 0x29 or 0x2D as these define an A16 transfer.

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VME ID Register (00)

The bit definitions for this register are:

Bit	Definition
11..0	Manufacturer ID (123 decimal)
13..12	01
15..14	01

Always reads as 507B hex.

VME Device Type Register (02)

The bit definitions for this register are:

Bit	256K SRAM	1M SRAM
11..0	Model code (328 decimal)	Model code (328 decimal)
15..12	Memory size (13 decimal)	Memory size (11 decimal)

Memory size is defined as the number of significant bits in an A32 address used to specify the DPR base address.

This register reads as:

B148 hex with 1M byte SRAM

VME Status Register (04)

The bit definitions for the read only status register are:

Bit	Definition
0..1	0
2	1
3	Ready (connected to TIM config lines)
4	1
5..14	0
15	A32 enabled

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VME Control Register (04)

The bit definitions for the write only control register are:

Bit	Definition
0	Reset board when set
15	Enable A32 when set

Bit 15 is cleared by a board reset so that the A32 base address registers can be initialised before A32 enable is set. A32 enable MUST be set to allow A32 access to the rest of the board.

If this bit is clear (0) then no A32 access will be decoded and a bus error will occur for all A32 read/write cycles.

It is very strongly recommended that all VME bus cycles have some form of BUS_ERROR checking enabled, as it is an essential error reporting feature which should not be ignored.

VME DPR Offset Register (06)

This 16-bit register defines the base address of the DPR for A32 addressing modes. The most significant 11 bits (1M SRAM) of this register are compared to VME address signals A31..21. The number of significant bits is specified in the 'Device Type' register.

VME I/O Offset Register (08)

This 16-bit register is used to set the base address (in 256 byte blocks) of the I/O address space.

This base address is compared to the incoming A32 address bits A8-23, while bits A24-31 are compared to FF hex. A match decodes a 256 byte space which is further decoded to access the various devices in the I/O address space.

VME Sub-class Register (1E)

The bit definitions for this 16-bit read only register are given below:

Bit	Definition
11..0	Manufacturer ID (123 decimal)
14..12	Manufacturer sub-class (1)
15	0

Always reads as 107B hex.

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Summary of VME Address decoding

There are 3 VME block decodes:

VME Decode	VME A31..24	VME A23..16	VME A15..8	VME A7..0	VME space
Config	nnnnnnnn	nnnnnnnn	11aaaaaa	aaxxxxxx	A16
DPR	bbbbbbbb	bbbddyyy	yyyyyyyy	yyyyyyyy	A32
IO	11111111	cccccccc	cccccccc	zzzzzzzz	A32

Symbol	Description
A16	VME Address modifiers AM=$29 or $2D
A32	VME Address modifiers AM=$09 or $0D
X	VME Config register select for D16 transfer
Y	VME DPR address select for D16 or D32 transfers
Z	VME IO register select for D16 or D32 transfers
A	Manually set at LK1: 1=Off, 0=On
B	Programmed in register DPR Offset
D	Y if 1M SRAM, B if 256K SRAM
C	Programmed in register IO Offset
n	Do not care bit

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Control and Status Registers

There are 5 control registers:

Control Registers 1 & 2 = TIM Sites 1 & 4 Interrupt Masks

The VME bus error signal can generate a TIM interrupt at either site 1 or 4. Each of these TIM sites has its own register which is accessible to both the VME bus and the TIMs. The registers are the general control register 1 for TIM site 1, and general control register 2 for TIM site 3. These registers are identical. Note that 'VME Bus Error' is latched by either of the bit 8 masks below. Therefore both must be cleared to unlatch 'VME Bus Error', and at least 1 must be set to latch 'VME Bus Error'.

The software interrupt will always generate an interrupt when it is unmasked.

Note that a TIM must execute an 'IACK' instruction to external memory before any TIM interrupts can be generated.

Bit	Definition
0	Software interrupt
7..0	Unused
8	VME Bus Error mask
15..9	Unused

General Control Registers 1 and 2

Control Register 3 = VME Interrupt Masks

Each of the two TIM sites 1 and 4 can generate an interrupt on the VME bus. The interrupt level is selected by bits 12 ..10 of Control Register 4. These can be enabled within the general control register 3 bits, described below. Also the VME comm port can generate Receiver and Transmit ready interrupts, and there is a software interrupt which occurs as soon as it is unmasked.

Bit	Definition
0	Software interrupt
1	VME Comm-port RX full
2	VME Comm-port TX empty
7-3	Unused
8	JTAG
9	TIM1 IIOF0
10	TIM4 IIOF0
15..11	Unused

General Control Register 3

Control Register 4 = VME Bus Master cycle control

This 32-bit control register is defined as the general control register 4, and the function is described below.

Bit	Definition
7..0	VME interrupt acknowledge vector
8	VME DS0 during C4x master cycle
9	VME DS1 during C4x master cycle
12..10	VME interrupt level request bits 2..0
14..13	VME Bus request level bits 1..0
15	Comm-port to TIM4 when 1, TIM1 when 0
16	VME A1 during C4x master cycle
17	VME LWORD during C4x master cycle
23..18	VME AM5..0 during C4x master cycle
31..24	VME A31..24 during C4x master cycle

General Control Register 4.

If no response from the addressed slave is observed within a fixed time (time-out period) then the VME Slot 0 controller will generate a ‘Bus Error’, the ‘C4x cycle will be terminated and a VME Bus Error interrupt generated.

Control Register 5 = General Status Register

A status register is available for access by the TIMs and the VME. The bit definitions are shown below:

Bit	Definition
0	Unused
1	VME Comm-port RX full
2	VME Comm-port TX empty
7-3	Unused
8	VME Bus error (latched)
9	TIM 1 IIOF0
10	TIM 4 IIOF0

General Control Register 5

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Dual Port RAM (DPR)

The DPR is composed of 1M or 256K Byte SRAM. This can be accessed as D8, D16 or D32 via the VME data bus. It can only be accessed in the A32 address space. The base address of this memory is set by the VME DPR offset register, and it resides on a 1Mbyte boundary. The memory speed is 12ns, which allows zero wait state access from TIM 1 or 4, even with buffer delays.

JTAG Debugging Logic

An external Jtag controller can be used to access the Tim sites. Please refer to the Texas Instruments data sheet for details of this controller. The JTAG architecture is shown below:

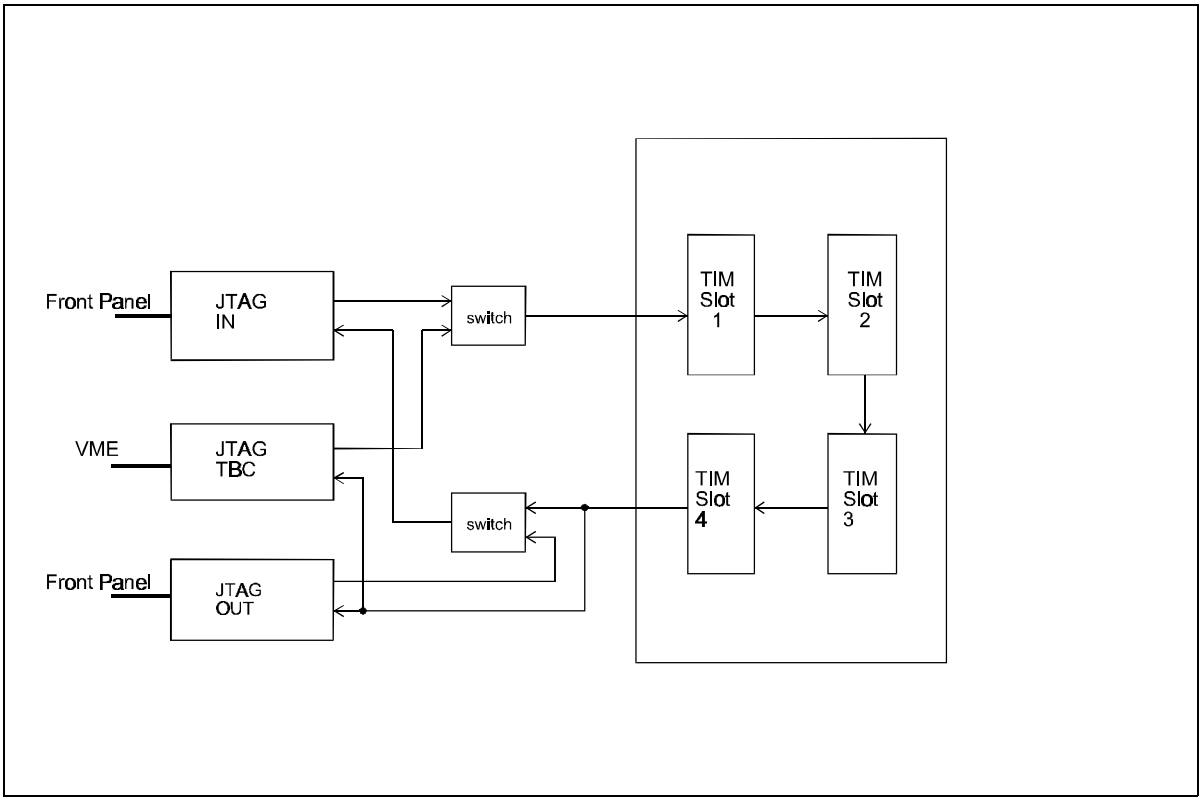


Figure 3: Routing of JTAG TDO and TDI Signals

The external Controller can drive the JTAG scan chain through all TIM modules. If a module is not present then the modules SENSE signal is used to enable a tri-state buffer inserted in the TDO/TDI (JTAG Data In and Data Out) scan chain. An FCT2244 type device is used which allows for the chain to function correctly with only one module site occupied. Each buffer has a propagation delay of 5ns maximum, which can limit the maximum JTAG clock frequency. Two connectors are present on the front panel. One is the scan chain out, and the other is the scan chain in.

The JTAG IN connector (nearest the PCB) has the following signals:

TDI, TDO, TRST, TMS, TCK, TCK_RET, EMU0, EMU1, GND, PD(+5v), JTOUT_DET.

The JTOUT_DET signal is pulled up on the motherboard, and if a JTAG OUT from one motherboard is connected to the JTAG IN then a corresponding GND pin on the JTAG OUT connector will pull JTOUT_DET low, to signal the TBC as described above. This connector also contains a reset_in signal and the config signal.

These details can all be found in the table in the section describing the JTAG front panel connections. The JTAG OUT connector has the following signals:

TDI, TDO, TRST, TMS, TCK, TCK_RET, EMU0, EMU1, GND, SENSE.

The SENSE line is pulled down on the motherboard, and thus if the JTAG OUT is connected to another motherboard's JTAG IN then the SENSE line is pulled high by the connection to PD(+5v). This configures the other selector as described above. This connector also contains a reset_out signal and the config signal. All outputs and inputs from and to the JTAG IN and OUT connectors are passed through buffers, except CONFIG which is a global open collector signal. Both the JTAG in and out connectors are 3M 20-way, part number 10220-5212JL. These details can be found in the table in the section describing the JTAG front panel connections.

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Comm-port Interface

This interface provides a route by which a VME host can talk to a ‘C4x comm-port. Both D16 and D32 accesses are allowed. The following address / register map is used:

Address	Register	Data bits	Read/Write
IO base + 80hex	Comm-port Data	31..0	R/W
IO base + 84hex	Comm-port Data	31..0	R/W
IO base + 90hex	Comm-port Status	15..0	R

There is only one comm-port interface, and its data register is accessible at both addresses indicated in the table above.

The comm-port data register is accessible as a D16 resource by first writing the upper data bits (31 to 16) to address base + 84h and then the lower data bits to address base + 86h. This register, when read, contains the last word to be received from the ‘C4x comm-port. Writing to this register causes a word to be sent to the ‘C4x comm-port. The receive and transmit sections of this register are separate.

The status register is accessible by the VME host as D16 at address base + 92h or in D32 at address base + 90h. The bit definition is as follows:

Bit	Definition
8	Receive data available
9	Transmit register empty
10	Receive data available
11	Transmit register empty

The receive data available bit becomes set when a receive word is in the comm-port data register. When the comm-port data register is read, this bit is reset.

When the transmit register empty bit is set, it indicates that the VME host can write a new word to the comm-port data register for later transmission to the ‘C4x comm-port.

Reset Board Register

This special control register is accessed in A32 space as either D16 or D32. When accessed as D16 it uses address base + C2h, and when using D32 at address base + C0h. Only bit-4 is defined, and if this bit is set by the VME host, it causes all TIM sites, comm-port buffers, and other motherboard logic to become reset. The board remains in such a state until this bit is cleared by the VME host. This reset is the **same** bit as defined in VME control register bit-0.

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TIM Memory Map

TIM sites 1 and 4 have access to the Dual Port RAM, general control registers, general status register and VME space. The addresses used are given in the table below:

Address	Resource	Read/Write
C000 0000	Gen Control reg 1	Read/Write
C000 0001	Gen Control reg 2	Read/Write
C000 0002	Gen Control reg 3	Read/Write
C000 0003	Gen Control reg 4	Read/Write
C000 0004	Gen Status reg	Read
C100 0000 – C13F FFFF	VME bus	Read/Write
DFFC 0000 – DFFF FFFF	1MB Dual Port Ram	Read/Write

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Comm-ports

The TMS320C4x processor has up to 6 byte-wide communications ports. In the case of the ‘C40, upon a reset 3 of these comm-ports are in output mode, and the other 3 are in input mode. Similarly the 6 front-panel comm-port buffers are divided so that 3 reset to input and 3 reset to output.

From the architectural diagram, the TIM sites (1 to 4) have six numbered comm-ports. Ports 0 to 2 are reset to output, and comm-ports 3 to 5 are reset to input. Front panel comm-ports 0 to 2 are reset to output at the FMS connector, and reset to input at the front panel connector, while comm-ports 3-5 are reset to input at the FMS connector and reset to output at the front panel connector.

Comm-port Patch Headers

The comm-port patch headers are 14-way surface-mount FMS connectors, located on the top of the board as close as possible to the respective TIM site. There are a total of 28 FMS connectors: 6 connect to the front panel comm-port buffers, and 16 connect to the TIM sites and 6 connect to through routing pipes.

They are arranged underneath the TIM sites, which use raised motherboard sockets, to allow clearance for the flat FMS cables. All signals to these connectors are pulled up to +5 volts with 10K resistors, this gives connected signals an effective pull up of 5K ohms. Series damping resistors of 33 ohms are also used on every signal line to reduce ringing effects. Tests have shown that 200mm long flat cables provide a reliable connection, and allow all connections between the FMS connectors to be made. For further details see Section 15: Patch Area Connector

Note that when connecting comm-ports with the FMS cables, to ensure pin 1 is connected to pin 1 on the alternative comm-port. The FMS headers have been arranged to make this task easier, with pin 1 clearly shown on the silk screen. The links will not work if incorrectly connected, although the 2 series 33 ohm damping resistors will prevent damage to a C4x comm-ports under these circumstances, for a limited period only.

Figure 2 shows the TIM comm-port architecture, which defaults to a triple circular pipeline. The pipeline from comm-ports 0-3 and 1-4 have auto-disable analog switches which are disabled when a cable is inserted into either of the associated FMS connectors. This function is implemented by using 2 signals on the FMS cable as connectivity indicators. An RTO comm-ports connects pin 1 to ground and pulls pin 14 up to +5 Volts through a 4K7 resistor. An RTI comm-port connects pin 14 to ground and pulls pin 1 up to +5 Volts through a 4K7 resistor. An analog switch is disabled when either pin 14 on the RTO FMS connector is at ground, OR when pin 1 on the RTI FMS connector is ground. When an FMS cable connects an RTI to an RTO port, both analog switches are disabled. The 2 VME comm-ports each have a manual override switch, which can be set to enable the VME and disable the analog switch, or disable the VME and enable the analog switch.

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FMS Pin	RTI Signal	RTO Signal
1	/SWITCH_DISABLE	GND
2	D0	D0
3	D1	D1
4	D2	D2
5	D3	D3
6	D4	D4
7	D5	D5
8	D6	D6
9	D7	D7
10	/REQ	/REQ
11	/ACK	/ACK
12	/STRB	/STRB
13	/RDY	/RDY
14	GND	/SWITCH_DISABLE

FMS connector pinout

Front Panel Comm-Ports

From the FMS comm-port patch headers, 6 comm-ports are taken to front panel mounted connectors via buffers, constructed from FCT245AT type devices with 64mA pull-down ability, and undershoot clamp diodes on all signals. All signals are pulled up to +3.3 volts with 100 ohm resistors. The active devices are mounted as close as possible to the connector they serve, and always within 50 mm of the connector.

The front panel comm-ports use 26 pin 3M connectors, (3M part number 10226-5212JL). The connector pin-out is given in the following table, with pair numbers for 13 off twisted pair cable (3M part number KUCKMPVVSB28-13PAIR).

The connectors are arranged in 2 rows of 3 such that 3 connectors are mounted directly on the main PCB and 3 connectors are mounted above them on daughter boards.

The buffer circuit for each connector is designed so that an FMS patch header which is RTI is connected to a front panel connector which is RTO. Conversely and FMS patch header which is RTO is connected to a front panel connector which is RTI.

So in order to simplify the wiring of adjacent boards in a rack:

All front panel connectors on the main PCB are RTI and they connect to FMS patch headers which are RTO.

All front panel connectors on the daughter boards are RTO and they connect to FMS patch headers which are RTI.

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As well as the 12 comm-port signals and signal grounds, there are 6 additional signals. Note that these signals are NOT essential for communications:

NAME	DESCRIPTION
I/O_OUT	Output high when port is outputting data, output low when port is receiving data.
I/O_IN	Input which prevents bus contention if connected to I/O_OUT
/RST_OUT	Active low open collector copy of the board reset drive.
/RST_IN	Active low board reset input, pulled up to 3.3V by 100 ohms.
VCC	1 AMP +5 Volt supply, with resettable 1 Amp fuse, to power a remote buffer, if required.
SHIELD	Overall cable shield, connected to plug shells and chassis.

The /RST_OUT is intended to allow synchronised reset of a number of boards by driving the /RST_IN input.

Comm-port FMS connector mapping

The connectivity between FMS comm-port connectors and front panel connectors is clearly shown in figure 2.

Physical location of front panel comm-port connectors

With the front panel flat on a bench and the pair of 20 pin JTAG connectors on the left, the front panel connector locations are:

JTAG_OUT J43	GAP	C3 RTO J35	C4 RTO J46	C5 RTO J39
JTAG_IN J49	GAP	C0 RTI J36	C1 RTI J40	C2 RTI J44

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TIM Sites

There are 4 TIM sites numbered 1 to 4. Sites 1 and 4 have the optional global connector to allow TIM access to the DPR and VME bus.

TIM Connector Pin-Out

The global connector contains the full set of TIM global bus signals. For accesses by the TIM to the global bus, the most significant address bit, A31 is a ‘1’. This bit is not an output pin but used internally on a ‘C4x TIM. The global bus connector does not contain any power or ground signals.

The bottom, or secondary, connector is used only for comm-ports, power and user definable connections (UDP 7 to 12). The user-definable pins are not implemented on this motherboard. Comm-ports 1, 2, 4 and 5 are on this connector.

The top, or primary, connector is used for the remaining two comm-ports (0 and 3), power, interrupts, control and JTAG. Both plus and minus 12v are supplied by the motherboard to these top connectors. The JTAG signals are derived from the JTAG control logic on the motherboard, or from an external source (see JTAG section).

An external clock is supplied to all TIM sites. This clock is currently 50MHz, and MUST be used by TIMs in sites 1 and 3 if they are to perform any external accesses via their Global TIM connector. Similarly, TIMs in sites 1 and 3 must provide both H1 and H3 clock outputs to the if they are to perform any global accesses.

A power supply of +3.3 Volts is present at both TIM mounting holes. This can be connected to the TIM by using metal bolts.

Refer to the TIM-40 Module Specification from Texas Instruments for exact connector placement. Adjacent TIM sites are separated by exactly 2.6".

The connectivity between TIM sites and FMS comm-port connectors is clearly shown in figure 2.

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Power Supplies

Connections are made to the following back plane power signals through VME connector P1: +12V, -12V, +5V. The +/-12V supplies are fed directly to the TIMs, they are not used anywhere else on the board. The +5V supply is also fed to the TIMs, and used for most of the logic, and to feed a DC-DC converter which generates +3.3V.

The DC-DC controller is an LTC1430 which has a +/-0.5% reference and guarantees +/-3% absolute maximum output variation subject to over current limiting and overheating. The feedback point is taken from the +3.3V power plane which is after a 10 AMP fuse. The power distribution is through a dedicated +3.3V power plane so the voltage drop here is minimal. The power plane distributes +3.3V to all 4 TIM sites through the metal TIM fixing posts. It is designed to supply 10 AMPS maximum, however this is only possible if the board receives adequate cooling. Failure to cool the board properly at high current levels could result in premature failure, and / or premature current limiting.

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Circuit / Schematic Details

The references given below are for board rev 2 and later.

Schematic Sheet Titles

Sheet	Title
1	VME Buffers
2	Static RAM
3	VME Comm-port interface
4	Global TIM site 1
5	Global TIM site 3
6	Comms TIM site 1
7	Comms TIM site 2
8	Comms TIM site 3
9	Comms TIM site 4
10	FP Comms 1 and 2
11	FP Comms 3 and 4
12	FP Comms 5 and 6
13	VME Control
14	VME Slaves
15	JTAG Control
16	Comm Port Control (front panel)

VME Configuration Registers in Short Address Space.

VME A13-6 are decoded by U140 on sheet 14 (QS74FCT2521CTQ) which compares them to the value set by links on SW1 as follows:

SW1	01	02	03	04	05	06	07	08
VME A	13	12	11	10	09	08	07	06

The corresponding switch must be on for the address line to be decoded as 0. U140 generates !VXIR1 which is fed to U131 (ISPLSI1016-90LT).

VME AM0-5 are decoded in U136 (ISPLSI2032-180LT), which generates !VXIR0 when the address modifiers are $29 (short non-privileged access) or $2D (short supervisory access).

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Control Bus Arbitration

The control bus arbiter U125 sets !CONTIM true when it grants the control bus to a TIM via the DPR bus. It sets !CONVME true when the VME bus is granted control of the Control bus, this is the default state when no requests are pending. The TIMs have a higher priority than the VME bus and are granted access as soon as any outstanding VME slave cycles have completed, signaled by !SLVSEL going false.

Programmable Logic Devices

J45 is the Lattice ISP programming port, which allows in circuit programming of all the following Lattice CPLDs:

ISP I/O	Nets	U	Type	Sheet	Controls
SDI (IN)	SD1				ISP Input
	SD1/2	136	2032	14	VME primary address decode
	SD2/3	41	1016	3	VME to C4x comm-port controller
	SD3/4	123	1016	13	Interrupt controller
	SD4/5	124	1016	13	VME buffer controller
	SD5/6	125	1016	13	VME & DPR bus arbitration
	SD6/7	131	1016	14	VME decodes
	SD7/8	132	1016	14	DPR control
	SD8/9	133	1016	14	VME secondary decodes
	SD9/10	134	1016	14	VME Config D0-7
	SD10/11	135	1016	14	VME Config D8-15
	SD11/12	50	2032	4	TIM site 1 global bus control
	SD12/13	59	2032	5	TIM site 4 global bus control
	SD13/14	24	1016	16	Front Panel Comm Port control
	SD14/15	42	1016	16	Front Panel Comm Port control
SDO (OUT)	SD15				ISP Output

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VME I/O Addressing

The VME address of these registers is an offset from the value set in the VME I/O Offset register:

Offset	C4x address	Peripheral	Read/Write
80	None	Comm-port data	Read/write
84	None	Comm-port data	Read/write
90	None	Comm-port status	Read/write
C2	None	Reset board	Read/Write
E0	C0000000	Control 1	Read/Write
E4	C0000001	Control 2	Read/Write
E8	C0000002	Control 3	Read/Write
EC	C0000003	Control 4	Read/Write
F0	C0000004	Status 1	Read

Setting bit 4 of the Reset Board register, generates a continuous reset.

VME to Comm-port Control State Machines

The ‘Port Arbitration Unit’ (PAU) state machine is exactly as described in the TMS320C4x User’s Guide of 1993. PAU state machine locations within U41 are:

GLB	State Machine
B0	PAU for TIM1 on bus R
B6	PAU for TIM 3 on bus P

There are 4 flags associated with occupancy:

Name	Description
TXFULL	VME TX register is full
RDAVAIL	VME RX register is full
TXMFULL	C4x TX register is full
RXMFULL	C4x RX register is full

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Patch Area FMS Connectors Layout

There are 28 FMS patch area connectors, as shown in figure 2. When viewed from the top of the board, with the front panel on the left and the VME bus on the right they are arranged in 4 rows of 7 as follows:

J34 J33 J37 J19 J17 J13 J11

TIM SITE 2 TIM SITE 1

J18 J20 J53 J51 J48 J12 J14

J25 J23 J52 J50 J47 J31 J29

TIM SITE 3 TIME SITE 4

J41 J42 J38 J24 J26 J30 J32

Note that on issue 1 of the PCB the silk screen markings for the TIM sites is incorrect,

Front Panel Comm-port Cabling

Connecting between ‘Reset to In’ and ‘Reset to Out’ comm-ports requires a 1 to 1 cable:

Cable plugs are: 3M Scotchflex 10126-6000EL FES part 038740A

Plug shells are : 3M Scotchflex 10326-A200-00 FES part 038760D

Cable type is: 3M Scotchflex KUCKMPVVSB28-13PAIR FES part 038781E

This cable has 13 individual pairs, with an overall shield, and an outer diameter of 7mm. Cable length should be as short as possible. The maximum tested cable length is 600mm, which allows connection between any boards in 1 rack, or between adjacent racks.

If connecting to an adjacent rack, **it is essential** that both racks share a common ground. This must include a separate chassis earthing strap connected between the racks.

Do not connect ‘Reset to In’ comm-ports together.

Do not connect ‘Reset to Out’ comm-ports together.

However if this should occur, no damage will result, because comm-port direction signals disable comm-ports connected together like this.

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The following table shows connector pinout and cable pair connections. This is important as the critical signals must be paired with a ground as shown. The allocation to twisted pairs is based on grouping the data signals because they change at the same time, so that crosstalk is not an issue. Each control signal has its own ground:

Pin	Twisted Pair	RTI Signal	RTO Signal
1	1	I/O_OUT	I/O_IN
2	1	GND	GND
3	2	I/O_IN	I/O_OUT
4	2	GND	GND
5	3	/CSTRB	/CSTRB
6	3	GND	GND
7	4	/CRDY	/CRDY
8	4	GND	GND
9	5	/CREQ	/CREQ
10	5	GND	GND
11	6	/CACK	/CACK
12	6	GND	GND
13	7	D0	D0
14	7	D1	D1
15	8	D2	D2
16	8	D3	D3
17	9	D4	D4
18	9	D5	D5
19	10	D6	D6
20	10	D7	D7
21	11	VCC	VCC
22	11	GND	GND
23	12	/RST_OUT	/RST_IN
24	12	GND	GND
25	13	/RST_IN	/RST_OUT
26	13	GND	GND
SHELL	-	SHIELD	SHIELD

Front Panel Comms Port connector pinout

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The overall shield is attached to the body of the metal plug shell.

The signal VCC is fused on the board at 1 amp. The fuse automatically resets when the load is removed.

On comm-ports which reset to input, pins 1 and 23 are always driven and pins 3 and 25 always received.

On comm-ports which reset to output, pins 3 and 25 are always driven and pins 1 and 23 always received.

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JTAG Front Panel Connectors

There are two 20-way front panel JTAG connectors. J43 is furthest from the board, and is an output to control another JTAG slave. J49 is nearest to the board, and is an input from a JTAG controller For example an XDS510. A special adapter cable is available to allow connection of a standard JTAG controller.

When a TIM is not fitted in a site, the SMT328 automatically through routes the JTAG serial data signal. This is done with a high speed buffer (74FCT2244CTQ) which has a maximum delay of 4.1ns. Where a number of boards are daisy chained the delay will be cumulative and it will be necessary to reduce the JTAG clock frequency below 10MHz.

JTAG front panel cabling

The 20-way JTAG connectors require the following cabling components:

Cable plugs are: 3M Scotchflex 10120-6000EL, FES part 038739R

Plug shells are: 3M Scotchflex 10320-A200-00, FES part 038759A.

Cable type is: 3M Scotchflex KUCKMPVVSB28-10PAIR, FES part 038780G

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The JTAG input or target is J49, nearest the main PCB. It has the following pin out:

Pin	Signal	Direction	Description
1	TDI	IN	JTAG data in
2	GND		
3	TDO	OUT	JTAG data out
4	GND		
5	TMS	IN	JTAG Test mode select
6	GND		
7	TCK	IN	JTAG clock, up to 10MHz
8	GND		
9	TCK_RET	OUT	JTAG clock return
10	GND		
11	/TRST	IN	JTAG Reset
12	GND		
13	/RESET	IN	Board Reset in
14	PD	OUT	Presence detect, +5V 1A fused
15	/DETECT	IN	Detect external JTAG controller when grounded
16	CONFIG	OPEN COLL	Global open collector C4x CONFIG
17	EMU0	OUT	Buffered EMU0 output
18	EMU1	OUT	Buffered EMU1 output
19	SPARE1		
20	SPARE2		

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The JTAG output or controller is J43, above J49 on a daughter board. It has the following pin out:

Pin	Signal	Direction	Description
1	TDI	OUT	JTAG data out
2	GND		
3	TDO	IN	JTAG data in
4	GND		
5	TMS	OUT	JTAG Test mode select
6	GND		
7	TCK	OUT	JTAG clock 10MHz
8	GND		
9	TCK_RET	IN	JTAG clock return
10	GND		
11	/TRST	OUT	JTAG Reset
12	GND		
13	/RESET	OUT	Board Reset out
14	PD	IN	Presence detect when pulled high
15	/DETECT	OUT	Detect external JTAG controller when grounded
16	CONFIG	OPEN COLL	Global open collector C4x CONFIG
17	EMU0	IN	Buffered EMU0 output
18	EMU1	IN	Buffered EMU1 output
19	SPARE1		
20	SPARE2		

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Application notes

C6201 Reset Sequencing and JTAG

We have observed a FATAL RESET sequencing problem on the C6201 in which the device fails to reset properly if the JTAG interface is in certain states when the main C6201 reset pin is activated. This problem has been solved by ensuring the C6201 JTAG system receives a hardware reset at the same time as the main reset. However because the JTAG reset is the responsibility of the JTAG controller, this fix only works when the 328 is using its own built in JTAG controller. When using an external JTAG controller it MAY be necessary for the USER to force the external JTAG controller to issue a JTAG reset either prior to, or at the same time as, a full board reset. This means that it must be able to drive JTAG signal “-JTRST” to ground in order to reset the C6201 JTAG system.

This problem was extremely difficult to diagnose on TIMs which rely on the C6201 to program an FPGA during the initialisation sequence after a reset. While the C6201 may reset correctly, quite often we found that the C6201 DMA correctly copies the contents of the ROM into SBSRAM, but does not then correctly release the C6201 core to execute the loaded program. However it is then possible to start Code Composer apparently without error, and use it to download an application program, and then run it. The snag is that the ROM boot code never correctly programmed the FPGA, which is still in program mode. Any reads from the global bus interface in this state can result in bus contention with the FPGA status register.

Code Composer support for the on board JTAG controller requires the following:

1. A suitable VME bus controller to host Code Composer. Please see the TI description of supported environments.
2. A custom I/O driver for the VME bus controller and Code Composer, which can map the 328 JTAG controller correctly for the Code Composer I/O interface. Note that this custom driver is likely to be very host specific, and may need to be adapted to avoid any interaction with your application software. Please contact Sundance regarding driver availability and authoring.

C4x asynchronous RDY signal

During development we observed C4x CPU crashes which were eventually traced to the use of an asynchronous RDY signal to terminate bus cycles. The C4x data sheet says that this will simply result in an uncertainty over the ending of a cycle i.e. the cycle may or may not last a further clock period. However there seems to be a critical point inside the RDY setup and hold time during which a transition on RDY will crash

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or hang the C4x depending on what it is doing at the time. This may be silicon revision dependant. The 328 avoids this problem by correctly synchronising the RDY signal to the H1/4 clock.

Device Drivers

Device drivers can vary widely with different VME bus controllers and their different operating software environments. Please contact Sundance regarding driver availability and authoring.

TIM memory access

There is no facility to access memory on a TIM module. The TIM must be able to write data to the dual port SRAM in order to share it with the other TIMs and the VME bus.

Generating VME Interrupts

Before you can do anything on the board, you must ensure the following minimal initialisation has been performed by the VME bus controller, in the following order:

1. Software reset is clear: VME control reg (04), bit 0 = 0.
2. DPR and I/O (A32) spaces are disabled: VME Control reg (04), bit 15 = 0.
3. VME DPR Offset Register (06) is set to a suitable address.
4. VME I/O Offset Register (08) is set to a suitable address.
5. DPR and I/O (A32) spaces are enabled: VME Control reg (04), bit 15 = 1.

As a simple test that the 328 can generate interrupts, try this code to generate a forced software interrupt:

```
*gen_control4 = (intlev << 10) | vector;    /* Set int level and vector */
*gen_control3 = 1;                          /* unmask software int */
```

The 328 should generate an interrupt immediately, as long as it is out of reset. Your host interrupt service routine should disable this 328 interrupt with:

```
*gen_control3 = 0;
```

To enable comms port transmit interrupts:

```
*gen_control3 = 4;
```

This interrupt follows the comms port status reg (IO base + 90 Hex) bit 9 which can be software polled. It is set by an empty transmit holding register, which is emptied by

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either a board reset or the TIM reading it. This test will work without anything being done to any TIMs, in fact it will work with NO TIMs fitted.

Included below is a sample VME interrupt test program, which is run on the VME controller. It performs a full test of the 328s ability to generate VME interrupts. To get an interrupt from TIM1 or 4, the user needs to select either bit 9 or 10 respectively in the 328 interrupt mask register, and then get the TIM to set IIOF0. VME Interrupts can not be generated from TIM 2 or 3.

```
/* Test code for SMT328 VME interrupts.

This code tests all levels and all vectors.
It runs on a Radisys EPC7 VXI bus controller running DOS.
I/O is performed through a 64K memory mapped window.
Each 328 register pointer is explicitly mapped with EpcSetAmMap.
The interrupt is acknowledged by EpcWaitIntr.
The line :

int_mask = 0x4; /* int is 328 Tx empty

can be changed to use the other 328 interrupts as follows:

Bit   Definition
0     Software interrupt
1     VME Comm-port RX full
2     VME Comm-port TX empty
7-3   Unused
8     JTAG
9     TIM1 IIOF0
10    TIM4 IIOF0
15..11      Unused

All in General Control Register 3.


*/



/* Test for VME interrupts from the 328: */
void  ev(void)
{
    unsigned long error;
    word vector;
    word ilev;
    word repeat;
    unsigned short ilev_mask;
    word interr;
    long intwait;
    unsigned word int_mask;
    unsigned long intstat;
    unsigned word control4, temp, trigger;
    unsigned long far *pintstat;
    unsigned word *con3_reg;  /* Control reg 3 */
    unsigned word *con4_reg;  /* Control reg 4 */
    unsigned word *const_reg;   /* Control status reg */
```

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```
    htoi(&repeat);
    if (repeat == 0) repeat = 1;
    puts("Testing for VME interrupts generated by the 328:");
    puts("WARNING: This test uses ALL vectors and ALL levels!.");
    setup_vme3(); /* set base_add to point to VME3 registers */
    error=0;
  while (repeat != 0){
    pintstat = &intstat;
    intwait = 500;
    int_mask = 0x4; /* int is 328 Tx empty */
    ilev = 1;
    EpcSetAmMap(BM_MBO | A32N, smt328_ex_vme3 + vme3_con3,
             (void *) &con3_reg);
    EpcSetAmMap(BM_MBO | A32N, smt328_ex_vme3 + vme3_con4,
             (void *) &con4_reg);
    EpcSetAmMap(BM_MBO | A32N, smt328_ex_vme3 + vme3_const,
             (void *) &const_reg);
    while((ilev < 8) && (error == 0)){
      put("Testing interrupt level =");
      puthl(ilev);
      ilev_mask = 1 << ilev; /* convert binary to bit mask */
      vector = 0;
      put(", starting with vector = $");
      puthw(vector);
      puts(".");
      while  ((vector < 256) && (error == 0)){
          control4 = (ilev << 10) | vector;
          *con4_reg = control4;
          temp = *con4_reg;
          if (temp != control4){
            trigger = *const_reg; /* Trigger the LA */
            put("ERROR: Control4 wrote $");
            puthl(control4);
            put(" read $");
            puthl(temp);
            puts(".");
            getch();
            error++;
          }
          *con3_reg = 0x0; /* Disable 328 ints */
          temp = *con3_reg;
          if((temp & int_mask) != 0){
            put("ERROR: While attempting to clear interrupt on level ");
            puthw(ilev);
            put(" , vector = $");
            puthw(vector);
            puts(".");
            put("       Control3 was written with $0, but reads $");
            puthl(temp);
            puts(".");
            getch();
            error++;
          }
          EpcWaitIntr(ilev_mask, pintstat, 0);  /* clear stale int */
          *con3_reg = int_mask;
          temp = *con3_reg;
          if((temp & int_mask) == 0){
            put("ERROR: While attempting to set interrupt on level ");
            puthw(ilev);
            put(" , vector = $");
```

```
            puthw(vector);
            puts(".");
            put("       Control3 was written with $");
            puthl(int_mask);
            put(", but reads $");
            puthl(temp);
            puts(".");
            getch();
            error++;
          }
          interr = EpcWaitIntr(ilev_mask, pintstat, intwait);
          if (interr != ilev_mask) {
            error++;
            put("ERROR: While waiting for interrupt on level ");
            puthw(ilev);
            put(" , vector = $");
            puthw(vector);
            puts(".");
            if (interr == 0) {
                put("       Timed out after $");
                puthl(intwait);
                put(" millisecs");
            }
            getch();
            puts(".");
          }
          if (((intstat & 0x00ff) != vector) & (error == 0)) {
            error++;
            put("ERROR: Incorrect Vector, received $");
            puthw(intstat);
            put(", expected $");
            puthw(vector);
            put(", ilev ");
            puthw(ilev);
            puts(".");
            getch();
          }
          vector++;
      } /* While vector... */
      ilev++;
    } /* While ilev... */
    *con3_reg = 0x00;   /* Disable 328 ints */
    repeat--;
  }
    put("Interrupt test complete");
    if(error == 0) put(" NO ERRORS");
    else {
      put("ERROR count = $");
      puthl(error);
    }
    puts(".");
}
```

Physical Characteristics

Power Consumption

The static power consumption was measured under the following conditions:

No TIMs fitted, no Front panel cables attached, the SMT328 is the only board fitted into a standard VME rack.

The empty rack backplane supply currents have been subtracted from the measured figures to obtain those given:

1.8 AMPS Maximum, 1.6 AMPS typical.

Board Dimensions

The board conforms to the VME standard for a ‘Double Height’ board. This is:

160.0 (+0, -0.3) mm by 233.35 (+0, -0.3) mm.

The board occupies 2 VME slots.

Recommended Operating Conditions

The DC Voltage Specification is the standard VME bus specification:

Specification	Minimum	Nominal	Maximum	Units
+5Volts	4.875	5.000	5.250	Volts
Temperature	0		70	Celsius

Absolute Maximum Ratings

These are **non** operating limits:

Specification	Maximum	Units
+5Volts	7.000	Volts
Temperature	-65 to +150	Celsius

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Airflow Requirements

The actual power consumption, airflow requirements and airflow resistance, are dependent on the TIMs fitted and on the activity on the board.

The minimum total airflow provided should be the greater of the following (A or B):

A. 1.0 Litre per second

B. The SUM of the airflow requirements of the fitted TIMs.

This airflow must be distributed evenly along the length of the board, to prevent hot spots.

Electromagnetic Shielding

Board drilling locations are available for customers who want to attach an EMI shield. Any such shield must **not** reduce the airflow to either side of the board. It is the customers responsibility to perform operational airflow resistance and temperature tests, with the shield fitted, to ensure premature failure is not caused by overheating, due to restricted airflow.

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References

Texas Instruments:
TMS320c4x User's Guide, 1993

Texas Instruments:
TIM-40 TMS320C4x Based Module, Specification 1993

Texas Instruments:
TMS320C6201 DSP data sheet SPRS051F, dated August 1999.

VMEbus International Trade Association:
VMEbus Specification, 1987

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