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SMT332

User Manual

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Revision History

Date	Comments	Engineer	Issue
7/3/00	Original Revision	GP	01
9/3/00	General reorganisation	GP	02

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Outline Description

The SMT332/372 is a size 1 TIM offering the following features:

- SMT332: TMS320C6201 processor running at 200MHz
- SMT372: TMS320C6701 processor running at 166MHz
- Four communications ports (approx 15M bytes/s)
- 512k bytes of fast SBSRAM, 16M bytes SDRAM
- 256k byte Flash ROM for boot code
- Global expansion connector
- High bandwidth data input via 2 x 16-bit x 32K synchronous FIFOs (SDB)

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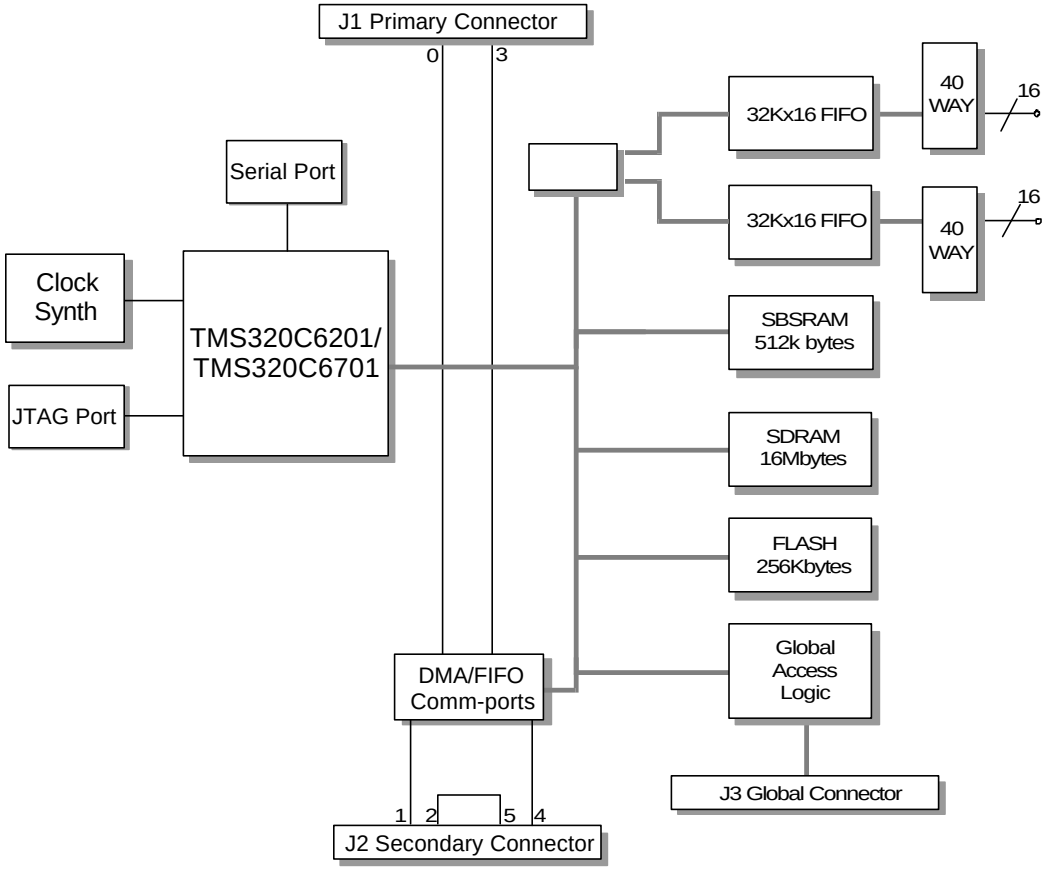
Block Diagram



Architecture Description

The SMT332 TIM consists of a Texas Instruments TMS320C6201 running at 200MHz and the SMT372 has a TMS320C6701 running at 166MHz. The TIM is populated with 512k bytes of SBSRAM (synchronous burst SRAM) and 16M bytes of SDRAM (synchronous DRAM) offering a total memory capacity of 16.5M bytes.

Additionally there are several programmable logic devices controlling such functions as communications ports and global bus access.

256k bytes of in-circuit re-programmable Flash ROM is provided to store boot code.

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TMS320C6201/6701 (‘C6x01)

The TMS320C6201 (‘C6201) will run at 200MHz with zero wait-states from internal SRAM. The TMS320C6701 (‘C6701) will run at 166MHz with zero wait-states from internal SRAM.

The clock used for the ‘C6x01 is provided from an on-board source only, unlike other ‘C4x (TMS320C4x) TIMs which can select the CPU speed from an external source via the TIM motherboard. The on-board source is a clock synthesiser from MicroClock, and its clock output is user selectable (via jumpers) from between 118 and 200MHz.

The configuration (config) feature is fully implemented and provides a single open collector line which can be held low until the module has been configured. This is provided by a control register accessible by the ‘C6x01.

Boot Mode

The ‘C6x01 is capable of booting in several different modes. On the SMT332/372, the boot mode is defined such that the ‘C6x01, after reset, will copy the first 64kb of flash data into internal program RAM, and then execute that code.

The second stage (code execution), sets up all necessary ‘C6x01 internal registers, and then configures the FPGA (communications port {comm port} controller) from other data held within the flash memory.

The final stage is to execute a ‘C4x type boot loader. This process continually examines the state of the comm port status register and will, when it determines which port data is present, then load a ‘C6x01 boot file which is then executed. Refer to the **Application Development** section for more information.

Whilst this stage of booting is in progress, all of the other comm ports will be ignored

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EMIF Control Registers

The ‘C6x01 contains several registers which control the operation of the external memory interface (EMIF). Each memory space (CE0 to 3) has an independent register, and in addition, there is a global control register.

A full description of these registers is within the ‘C6x01 Peripherals Reference Guide.

Briefly, these registers should contain the following values:

GC (global control)	0x00003779 0x0000377D	For ½speed SBSRAM For full speed SBSRAM
CE0	0x00000040	Indicates SBSRAM
CE1	0x8238C823	Defines async memory timings
CE2	0x00000030	Indicates SDRAM
CE3	0x00000030 0xFFFF3F23	Defines SDRAM timings for access to the FIFO data. Defines async memory timings for access to FIFO flag programming.

SBSRAM

Connected to the ‘C6x01 external memory interface (EMI), using memory space CE0, are 512k byte of zero wait state SRAM.

The SBSRAM can be set (via an internal ‘C6x01 register) to operate at either the ‘C6x01 core clock, or ½the core clock speed. This requirement has to be considered in conjunction with the ‘C6x01 core speed and external memory speed refer to **clock speed** for further details), but normally the SBSRAM would be set to run at the core speed.

SDRAM

Connected to the ‘C6x01 external memory interface, using memory space CE2, is a 16M byte bank of SDRAM.

The SDRAM operates at ½the core clock speed.

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Flash

A 256k byte Flash ROM device is fitted to the 'C6x01 EMI. This device is byte accessed using strobe CE1 (from 0x0140 0000 to 0x0143 ffff)

This device contains boot code for the 'C6x01 and configuration data for the FPGA.

A software protection algorithm is in place to protect erroneous altering of the device's contents. Please contact Sundance for further information with regard to re-programming this device.

Comm ports

The 'C6x01 does not include, within the device itself, any means of communicating high speed data to other processors. For operation in a TIM 40 environment, 4 communication (comm) ports are provided.

The comm ports on the SMT332/372 will interface to any standard 'C4x comm port.

The comm ports can operate in two modes. The first mode is for the 'C6x01 to transfer data to the port directly using a polling technique. The second mode is for the 'C6x01's DMA controller to be set to event triggered and select the appropriate trigger (INT4..7) for the transfer.

The following table shows the 'C6x01 address map for the comm port interface.

Address (hex)	Function
0160 0000	Comm port data register – Comm Port 0
0160 0004	Comm port data register – Comm Port 3
0160 0008	Comm port data register – Comm Port 1
0160 000c	Comm port data register – Comm Port 4
0160 0010	Comm port status register (read only)
0160 0014	Comm port interrupt control register - ICRA (write only)
0160 0018	Generate TIM IACK signal (read or write)
0160 001c	Reset register (read or write)

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The following table defines the bit functions within the status register.

Status Register Bit	Function
0	Comm port 0 rx data available
1	Comm port 0 tx buffer empty
2	Comm port 3 rx data available
3	Comm port 3 tx buffer empty
4	Comm port 1 rx data available
5	Comm port 1 tx buffer empty
6	Comm port 4 rx data available
7	Comm port 4 tx buffer empty

The comm ports are implemented within a Xilinx FPGA.

The normal Sundance boot procedure will automatically configure this device. It is not recommended that the user attempts to re-program this FPGA.

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Interrupts

The interrupts to the ‘C6x01 can be produced by

- comm port status change
- DMA completion
- FIFO flag status change
- external IIOF and TCLK signals present on the TIM connector

There are two registers that control the interrupt enabling. Interrupt Control register A (ICRA) provides the first stage of interrupt selection, followed by Interrupt Control Register B (ICRB).

When interrupts are enabled, they will be generated for every comm port word received or transmitted (as appropriate). The selection of fast or slow interrupts requires understanding of the timings between the STRB and RDY signals on the comm port. Slow interrupts are generated when the fourth STRB of a word transfer goes high. At some point after this the ‘C6x01 External Memory Interface strobe (nCE1) becomes active. However, to allow the comm port data transfer to be speeded up, the fast interrupts are generated on the second STRB going high. This assumes the fourth STRB and RDY arrive before the ‘C6x01 has reacted to the early interrupt. This is normally the case, but if the comm port is being connected to a slow peripheral which does not guarantee the arrival of the last two comm port strobes, then data errors may result. These enable signals can be delayed by writing to the EMIF CE1 space control register. Warning - if fast interrupts are used and the enable signal goes low too early this could result in the transfer hanging or incorrect data transfer.

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Address (hex)	Function
0160 0014	Interrupt control register A

Interrupt Control Register Bit	Function
1 & 0	00: Enable Comm Port 0 rx data available to INT4 01: Enable Comm Port 0 tx data available to INT4 10: Enable IIOF0 to INT4 11: Enable TCLK0 to INT4
3 & 2	00: Enable Comm Port 3 rx data available to INT5 01: Enable Comm Port 3 tx data available to INT5 10: Enable IIOF1 to INT5 11: Enable TCLK1 to INT5
5 & 4	00: Enable Comm Port 1 rx data available to INT6 01: Enable Comm Port 1 tx data available to INT6 10: Enable IIOF2 to INT6 11: Enable IIOF1 to INT6
7 & 6	00: Enable Comm Port 4 rx data available to INT7 01: Enable Comm Port 4 tx data available to INT7 10: Enable IIOF0 to INT7 11: Enable IIOF2 to INT7
8	0: Comm Port 0 rx slow1: Comm Port 0 rx fast
9	0: Comm Port 0 tx slow1: Comm Port 0 tx fast
10	0: Comm Port 3 rx slow1: Comm Port 3 rx fast
11	0: Comm Port 3 tx slow1: Comm Port 3 tx fast
12	0: Comm Port 1 rx slow1: Comm Port 1 rx fast
13	0: Comm Port 1 tx slow1: Comm Port 1 tx fast
14	0: Comm Port 4 rx slow1: Comm Port 4 rx fast
15	0: Comm Port 4 tx slow1: Comm Port 4 tx fast
16	Enable Comm Port 0 rx to INT7
17	Enable Comm Port 0 tx to INT7
18	Enable Comm Port 3 rx to INT7
19	Enable Comm Port 3 tx to INT7
20	Enable Comm Port 1 rx to INT7
21	Enable Comm Port 1 tx to INT7
22	Enable Comm Port 4 rx to INT7
23	Enable Comm Port 4 tx to INT7

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Address (hex)	Function
0158 0000	Interrupt control register B - ICRB (write only)

Interrupt Control Register Bit	Function
8	Clear to enable FIFO Channel A, flag to INT4. Set to enable CINT4 to INT4.
9	Clear to enable FIFO Channel A, flag to INT5. Set to enable CINT5 to INT5.
10	Clear to enable FIFO Channel B, flag to INT6. Set to enable CINT6 to INT6.
11	Clear to enable FIFO Channel B, flag to INT7. Set to enable CINT7 to INT7.
13 & 12	Channel A FIFO flag control. 00: select empty flag 01: select almost empty flag 10: select almost full flag 11: select full flag
15 & 14	Channel B FIFO flag control. 00: select empty flag 01: select almost empty flag 10: select almost full flag 11: select full flag

Note: Channel A/B relates to the 2 FIFO devices. Refer to the **FIFO** section for further details.

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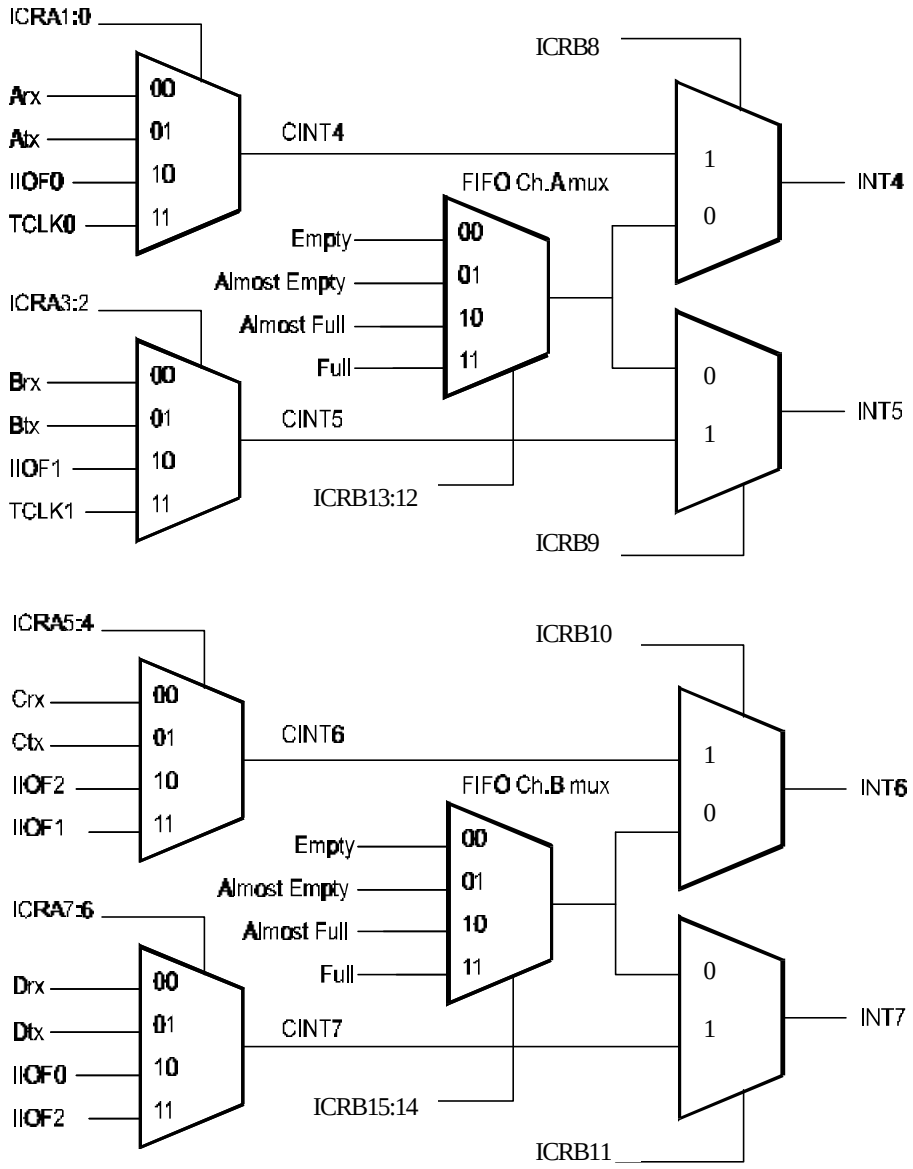
The functions of ICRA and ICRB are shown diagrammatically below:



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NMI

The NMI pin is routed to the TIM connector.

IACK

On a standard ‘C4x TIM, the processors IACK (interrupt acknowledge) signal is connected to the TIM connector.

On the SMT332/372, this IACK signal is generated by the ‘C6x01 writing to address 0x01600018. The length of the pulse will be determined by the External Memory Interface register settings for memory space CE1. With the default timings, this pulse will be 40ns.

CONFIG

The TIM specification describes the operation of an open-collector type signal (CONFIG) which is asserted (low) after reset.

This signal, on a standard ‘C4x based TIM, is connected to the processor’s IIOF3 pin. On the SMT332/372, the CONFIG signal is asserted after power on, and can be released by writing to the interrupt control register A (address 0x0160 0014) with bit 8 set. Conversely, CONFIG may be re-asserted by writing this bit with a 0.

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FIFO Data Input/Output

The SMT332/372 provides a high bandwidth data input facility for up to 32-bit data. The inputs are split in two 16-bit channels. Both channels are identical and may be referred to as Channel A & B with Channel A representing the least significant 16-bits and B the most significant 16-bits of the 32-bit word.

Each data source is connected to the SMT332/372 via a 40-way connector allowing for signal and return paths. The 40 way connectors are mounted on the topside of the PCB for direct cable connection. Alternatively an 80-way connector may be mounted on the underside of the PCB for connection to customised TIM carriers, etc. The default option is for connectors on the TOP of the PCB.

Each input channel is provided with a separate clock (WCLK*), enable (WEN*), FIFO reset (Reset*) and flag (programmable almost full flag) signals in the event that independent data sources are required.

Data is routed from the connectors to FIFOs which provide 32K x 16 storage of Input data at rates up to 100MHz. The FIFOs are interfaced to the 'C6x EMIF which enables them to be address as a 32-bit word. The 'C6x can be programmed to receive an interrupt when the FIFO has reached a certain level (see Interrupts).

The pin allocation for the I/O connectors is shown in Appendix.

The control signals are derived from the FIFO requirements that may be seen in the appropriate data sheet. The device used is an IDT72284 a copy of which is available in PDF format from Sundance.

Channel B's control signals will be used by default in a 32-bit application

WCLK	Data is written in to the FIFO on every rising edge when WEN is valid.
/WEN	WEN enables WCLK for writing data into the FIFO memory
/Reset	FIFO Reset resets the pointer to the first FIFO location
/FLAG	Programmable FIFO Almost Full Flag

For the 'C6x01 to read the FIFO, the EMIF needs to have the CE3 memory space defined as SDRAM (see **EMIF Control Register** section). This is the only method by which a 100MHz data rate can be sustained. The FIFO must be read using address 0x03000000 for port A (bottom 16 bits active), address 0x03400000 for port B (top 16 bits active) or address 0x03800000 for both ports (all data bits active).

In addition to an external device writing to the FIFO, it is necessary for the 'C6x01 to be able to have a limited write capability. This is required in order that the programmable FIFO flags can be programmed. To set this access mode, the CE3 memory space must be defined as an asynchronous space, with maximum strobe widths. Next the WEN and WCLK multiplexer needs to be switched. To enable 'C6x01 access, it is necessary to write to address 0x03800000. Notice that this is the

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same address as that needed for 'both ports read' function, but as we have switched memory types (SDRAM to ASYNC) then the FIFOs are not actually accessed at all. The FIFO flag positions need to be serially loaded. Data bit D19 is used for port A FIFO, and data bit D23 for port B. Both FIFOs are programmed at the same time. D17, D18, D21 and D22 must be set to 0s during the serial load. The serial load address is 0x03000000. Upon completion of programming, the multiplexer needs to be set to normal operating mode. This is done by writing to address 0x0300C000. And finally, the memory needs to be defined as SDRAM.

For convenience, C source code routines for performing these function are included on the distribution disc.

FIFO Status

The FIFO status can be read from address 0x01580000. The EMIF CE3 memory space register must be set for asynchronous access. Note that the status is returned on data bits 8-15 (not 0-7). Note also that the flag status bits are active when read as a '0'.

Address (hex)	Function
0158 0000	FIFO Status register (Read)

FIFO status Bit	Function
8	FIFO Channel A not empty flag.
9	FIFO Channel A not almost empty flag.
10	FIFO Channel A not almost full flag.
11	FIFO Channel A not full flag.
12	FIFO Channel B not empty flag.
13	FIFO Channel B not almost empty flag.
14	FIFO Channel B not almost full flag.
15	FIFO Channel B not full flag.

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Global Expansion

Part of the TIM4x specification defines an optional global expansion connector (J3). This expansion connector allows the TIM's CPU access to host motherboard resources, where available.

The 'C6x01's EMIF is not directly compatible with the TIM global connector standard. This is due primarily to the 'C6x01 bus speed and bus voltage levels.

The SMT332/372 does implement a fully compatible TIM global connector through the use of an EPLD.

The global bus transactions are synchronised to the 'C6x01 clock speed.

The global bus may be accessed directly by the 'C6x01 (via this EPLD) where it may perform reads or writes.

A maximum block size of 64k words can be accessed at any one time due to the limited number of address bits from the 'C6x01. So to access the whole global memory range, a page register is used which holds the value of the upper 15 address bits.

Address (hex)	Function
0170 0000 – 0173 FFFC	Global access (4 byte boundaries)
0178 0000	Global address page register

The global address page register must have the bottom 15 bits loaded with the top 15 bits of the global address.

An example of how to use this interface is given in the **Example Code** section.

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Clock Speed

The ‘C6x01 clock speed must be set in conjunction with consideration to EMIF device speeds. Under most circumstances, the ‘C6201 would be set to 200MHz and have an SBSRAM speed equal to the core speed. The ‘C6701 would be set to 166MHz.

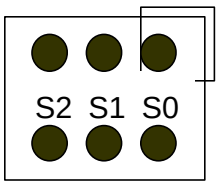
The following table shows all available possibilities:

Device			Comment
‘C6x01	SBSRAM	SDRAM	
133	133	67	Zero wait state SBSRAM
166	166	83	Zero wait state SBSRAM
200	100	100	One wait state SBSRAM
200	200	100	Zero wait state SBSRAM

The following table defines the link positions of JP1 and the resultant clock speed.

S2	S1	S0	CLK (MHz)
0	0	0	200
0	0	1	182
0	1	0	167
0	1	1	154
1	0	0	143
1	0	1	133
1	1	0	125
1	1	1	118

S0, S1 and S2 refer to the following link positions on JP1. Link in to force a ‘0’.



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Memory Map (MAP 1)

Starting Address	RESOURCE	Refer to
0000 0000	Internal Program RAM	
0001 0000	Reserved	
0040 0000	External Memory Space CE0 512kb SBSRAM	SBSRAM
0140 0000	External Memory Space CE1 256kb Flash	Flash
0150 0000	External Memory Space CE1 FPGA program pin control	Comm Ports
0158 0000	External Memory Space CE1 WR: Interrupt Control Register B – ICRE RD: FIFO Flag Status	Comm Ports
0160 0000	External Memory Space CE1 FPGA internal registers (Comm ports)	Comm Ports
0170 0000	External Memory Space CE1 Global bus access	Global Expansion
0178 0000	External Memory Space CE1 Global bus page register	Global Expansion
0180 0000	Internal Peripherals	
01C0 0000	Reserved	
0200 0000	External Memory Space CE2 16Mb SDRAM	SDRAM
0300 0000	External Memory Space CE3 FIFO A:0x03000000, FIFO B:0x03400000 FIFO A+B:0x03800000	FIFO
0400 0000	Reserved	
8000 0000	Internal Data RAM	
8001 0000	Reserved	
8040 0000	Reserved	

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Example Code

The following examples illustrate the use of the FIFOs.

FIFO Reset

```
// make a copy of the current EMIF CE3 mode

      old_ce3 = *EMIF_CE3_CTRL;

// This writes to the 'C6x01 internal EMIFCE3 control register
// at address 0x01800014, and sets it to async mode

      *EMIF_CE3_CTRL = 0xffff3f23;

// To reset the FIFOs (including flag positions), just write to
// address 0x03004000
// The value of 0 is important to set the correct FIFO mode

      *SMT332FIFORST=0x00000000;

// This is a delay before we switch the EMIF_CE3 space back to
// synchronous mode

      for(i=0;i<1;i++) {};

// Switch back to sync mode

      *EMIF_CE3_CTRL = old_ce3;
```


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Programmable Flags

Example code is included here to show how to configure the programmable flag offsets of the FIFOs.

Both the FIFO control register and the FIFO data is accessible using ‘C6x memory space CE3. For FIFO data access, this memory space is configured to be SDRAM, but for control register access it must be configured as asynchronous memory. The CE3 control register, internal to the ‘C6x, is at address 0x01800014.

The first operation is to switch on a control multiplexer which enables the ‘C6x to access the ‘write’ side of the FIFO. This is needed to program the FIFO offsets.

```
// make a copy of the current EMIF CE3 mode

      old_ce3 = *EMIF_CE3_CTRL;

// This writes to the ‘C6x01 internal EMIFCE3 control register
// at address 0x01800014, and sets it to async mode

      *EMIF_CE3_CTRL = 0xffff3f23;

// Then we have to switch the FIFO mux which is accessed at
// address 0x03008000 (in asynchronous memory space)

      *SMT332MUXON = 0x00;

// The FIFO flags are serially programmed here
// Example
// almost empty position = 0x2000
// almost full position = 0x8000-0x6000
// note: max FIFO entries = 0x8000

      flagpos = almost_empty + (almost_full<<15);

      for(i=0;i!=30;i++) {
            *SMT332FIFOA=((flagpos&1)<<19) + ((flagpos&1)<<23);
            flagpos>>=1;
      }

// mux off address is 0x0300c000

      *SMT332MUXOFF=0x00;

// This is a delay before we switch the EMIF_CE3 space back to
// synchronous mode

      for(i=0;i<1;i++) {};

// Switch back to sync mode

      *EMIF_CE3_CTRL = old_ce3;
```


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Data Aquisition

This is a simple example of how to capture data from the SDB into SDRAM.

```
// The flags are read at address 0x01580000

volatile unsigned *flags = (unsigned *)0x01580000;
j = 0;

do {

      do {

// Read flags

            temp = *flags;

// Wait on channel A nearly full

            temp = temp&0x0400;
            temp = temp>>8;

      } while (temp != 0x00);

// Setup the ICRs (ICRA = 0x01600014, ICRB = 0x01580000)

      *SMT332INTCTRLA = 0x00;

// FIFOA full -> INT4, FIFOB full -> INT5

      *SMT332INTCTRLB = 0xF000;

// Setup the DMA channel to read the FIFO

// DMA Priority > CPU, no TCINTerrupt, INCrement destination
// address only

      *DMA_PRI_CRTL0 = 0x01000040;

// Set the source address to be a read from both FIFOs

      *DMA_SRC_ADDR0 = 0x03800000;

// And the destination address to be internal data memory

      *DMA_DST_ADDR0 = (unsigned int)0x80008000;

// Set the frame count, reload and index register

      *DMA_XFR_CNTR0  = 0x00002000;
      *DMA_GL_CNT_RLD = 0x00002000;
      *DMA_GL_INDEX   = 0x00040004;

// Start the DMA

      *DMA_PRI_CRTL0 = 0x01000041;
```


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```
// Wait for DMA to finish (could be linked to the DMA TCINT)

      while((*DMA_PRI_CRTL0 & 0xc)!=0);


// Then setup the DMA to move the data from internal data memory
// into external SDRAM

      *DMA_PRI_CRTL0  = 0x01000050;
      *DMA_SRC_ADDR0  = (unsigned int)0x80008000;

// SDRAM is at address 0x02000000

      *DMA_DST_ADDR0  = (unsigned int)(0x02000000+j*0x00008000);

      *DMA_XFR_CNTR0  = 0x00002000;

// Start DMA

      *DMA_PRI_CRTL0  = 0x01000051;

// Wait for move complete. As DMA priority > CPU, this move
// should be very fast

      while((*DMA_PRI_CRTL0 & 0xc) != 0);

      j++;

// Repeat for 512 blocks

} while (j < 512);
```


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Global Bus Example

This example shows the ‘C6x01 DMA controller being used to transfer data via the PCI bus. In this example, the target is host display memory. Note that the host display memory must be linear (not an old PC-AT style VGA type card).

```
// Create pointers to the ‘C6x01’s DMA registers

dma_cfg =(unsigned *)0x01840000;
dma_src =(unsigned *)0x01840010;
dma_dst =(unsigned *)0x01840018;
dma_tc  =(unsigned *)0x01840020;

// Change CE1 memory space decode to async, with optimum
// global bus timings

emif_ce1 =(unsigned *)0x01800004;
*emif_ce1=0x8238c823;

// If we stick a little ramp into SBSRAM and use this as
// the source of our DMA, then we get a pretty result!
// Make sure you don’t overwrite the program itself!

sbsram=(unsigned *)0x00420000;
for(i=0;i!=16384;i++) {
     *sbsram++=i;
}

// First we have to change the 331 page register (at
// address 0x017800000) to point it to the smt320’s
// control register at address 0xC0800000.
// This address is a TIM global address and NOT a PCI one.

global=(unsigned *)0x01780000;
*global=0xc080;

// Then we write to the SMT320’s control register. The ‘window’
// onto the TIM global bus, is via ‘C6x01 address space
// at 0x01700000.
// Setting the control register to 1 enables SMT320 PCI burst
// mode.

global=(unsigned *)0x01700000;
*global = 1;
```


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```
for(loop=0;loop!=256;loop++) {
      for(blocks=0;blocks!=16;blocks++) {

// Set the 331 page register to point to the address register
// on the SMT320. This is at address 0xC0400000.

            global=(unsigned *)0x01780000;
            *global=0xc040;

// Then we set the SMT320 address register to the start of the
// host's display memory. Note that this will be different
// from PC to PC. In this case it is at address 0xFE000000.

            global=(unsigned *)0x01700000;
            *global = 0xfe000000 + blocks*0x8000;

// Back to the page register, and point to the SMT320 FIFO.
// This is where reads and writes will be over the PCI bus.

            global=(unsigned *)0x01780000;
            *global=0xc000;

// Now we are ready to do the DMA.

      global=(unsigned *)0x01700000;

// DMA source is SBSRAM, destination is global bus,
// transfer count is 8k (32k bytes)

            *dma_src=0x00420000+loop;
            *dma_dst=0x01700000;
            *dma_tc =0x00002000;

// and start

            *dma_cfg=0x01000051;

// Now we wait for DMA to finish.

            while (((*dma_cfg)&0xc) != 0) {};
      }
}
```


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Code Composer

This module is fully compatible with the Code Composer debug environment. This extends to both the software and JTAG debugging hardware including the SMT320, SMT327, SMT328 and TI's XDS-510.

In some circumstances, normally after a reset when the boot flash device is not configured correctly, there is a requirement to perform a hardware reset during the Code Composer start up sequence. If a Windows dialog box appears when Code Composer is started and requests an 'Abort Retry Ignore' action, then a reset must be made to the module, and then a retry actioned. The reset is most easily done using the SMT6000 Server/Loader.

Application Development

Various methods exist to develop code for the SMT332/372 module. The simplest, and probably the most cost effective, is by the use of the Sundance SMT6000 Server Loader, and the associated library.

The Server Loader is an application which runs on a host PC under either Windows 98 or NT. It allows applications (in the standard TI COFF format) to be downloaded and for stdio calls to be served.

A modified form of the TI rts library is supplied. One library for the 'C6201 and a separate library for the 'C6701.

Using the SMT6000 supplied tools, a .out file is easily generated.

The Server Loader will read the .out file, decode it, and then transmit it via comm port to the SMT332/372. The Server Loader includes a COFF decoder, and translates this into 'C4x style boot code.

The boot code has the following format:

Word 0:	either 0x00003779 for half speed SBSRAM
	or 0x0000377D for full speed SBSRAM (recommended)
Word 1-3	0, 0, 0
Word 4:	execution address
Word 5:	0
Word 6:	block length, n
Word 7:	destination address (external memory only)
Word 8 to 8+n	data or code

Word group 6,7 & 8 are repeated as necessary until the whole application is loaded.

To start the application, the last word transmitted must be a 0 (zero block length).

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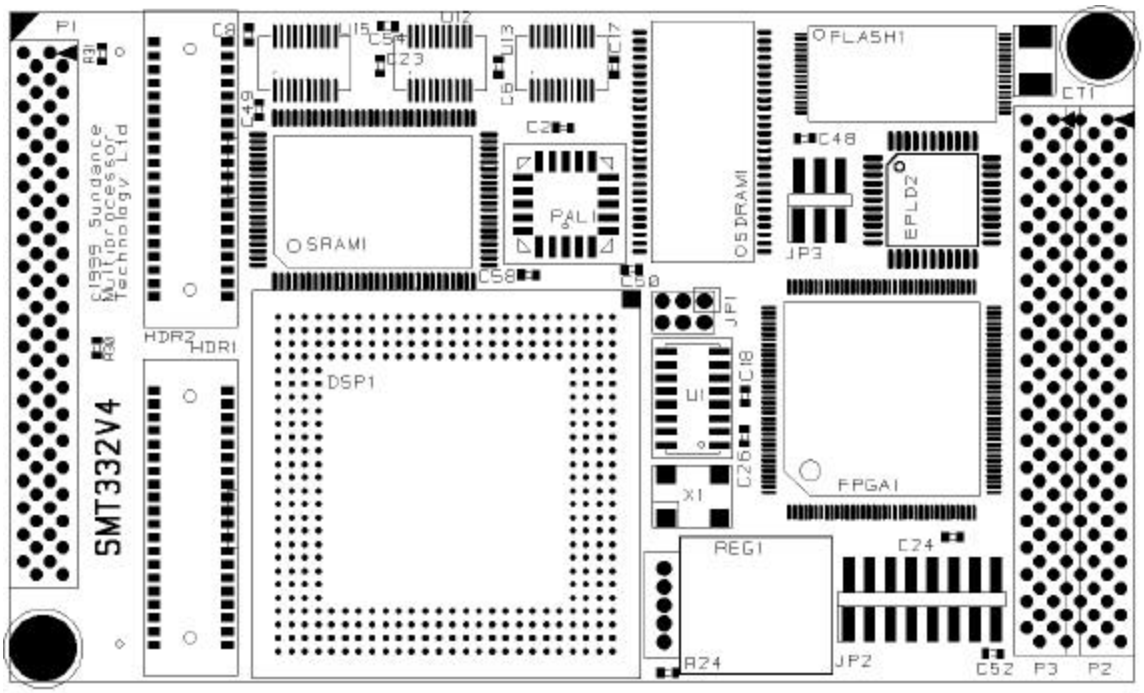
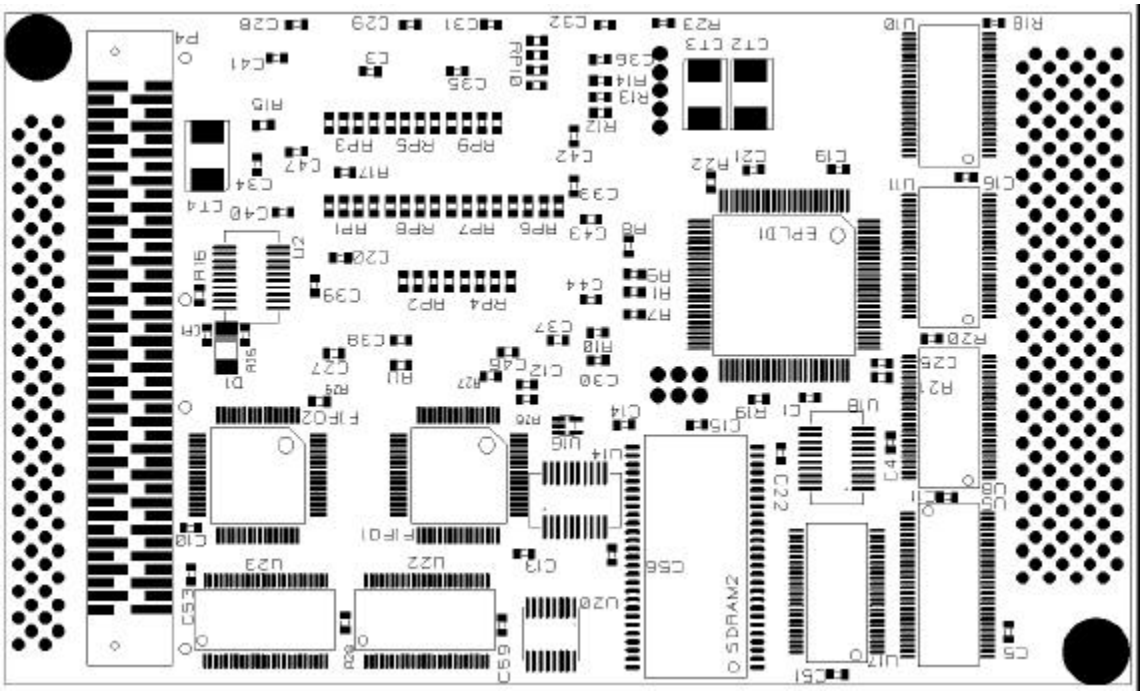
Mechanical Configuration





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Operating Conditions

Safety

This module presents no hazard to the user.

EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

Power Requirements

This module must be fixed to a TIM40 compliant carrier board. Additionally, a 3v3 power source must be provided to the fixings. This is normally achieved by means of a power source provided directly through conducting pillars on the carrier board.

The SMT332/372 TIM is in a range of modules which must be supplied with a 3.3v power source. In addition to the 5v supply specified in the TIM specification, these new generation modules require the additional 3.3v supply to be presented onto the two diagonally opposite TIM mounting holes.

Although no damage should result from not supplying 3.3v (the module obviously will be inoperable), prolonged operation in these circumstances is not recommended.

This module is then not directly compatible with earlier generations of TIM motherboards, although the 3.3v supply can be connected from a separate source. The module is however, compatible with the latest generation of Sundance TIM carrier boards such as the SMT320 (PCI), SMT327 (cPCI) and SMT328 (VME).

External ambient temperature must not exceed the limits of 0 to 40 °C, and relative humidity not greater than 95% (non-condensing).

Power Consumption

The power consumption of this TIM is dependant on the operating conditions in terms of core activity and i/o activity. The maximum power consumption is 6W.

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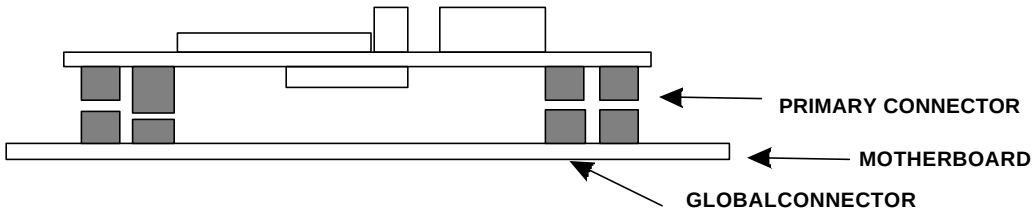
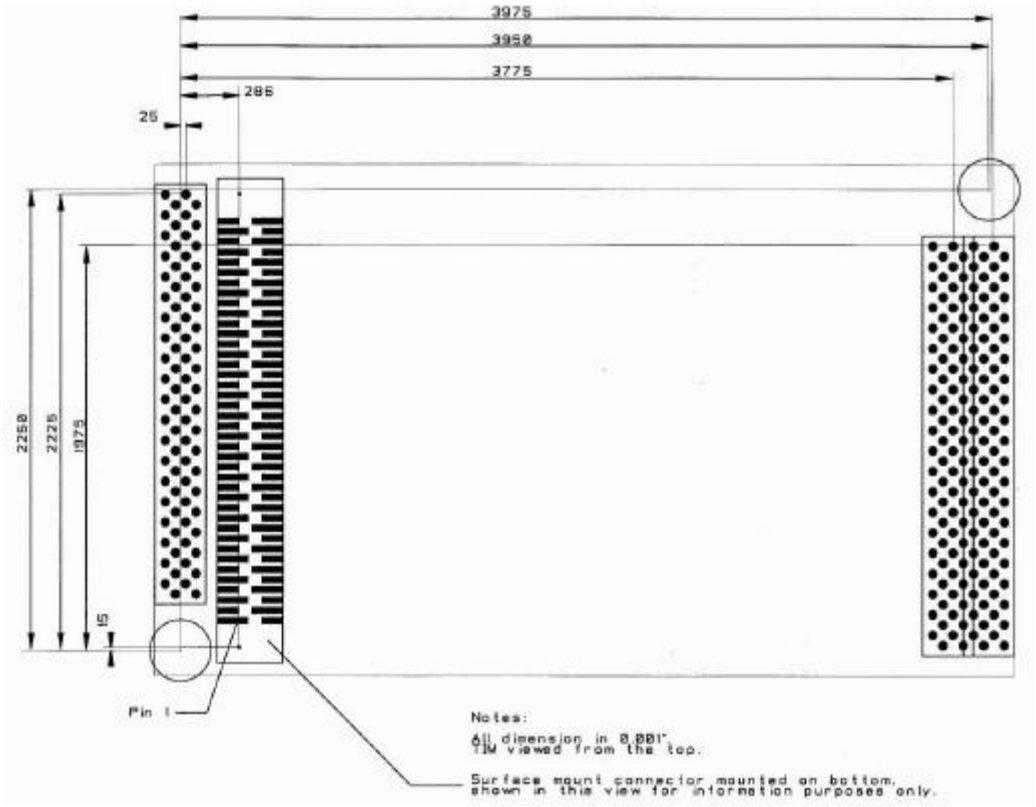
Connectors

Tim Connector Position

The following drawings illustrate the respective positions of the TIM connectors and the FIFO data optional connector.





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SDB

The FIFO data is input via a connector known as the Sundance Digital Bus (SDB). This is a 40 pin connector suitable for connection with ribbon cables. The pin-out of this header is given here.

Function	Pin	Pin	Function
GND	2	1	WCLK
GND	4	3	DIN0
GND	6	5	DIN1
GND	8	7	DIN2
GND	10	9	DIN3
GND	12	11	DIN4
GND	14	13	DIN5
GND	16	15	DIN6
GND	18	17	DIN7
GND	20	19	DIN8
GND	22	21	DIN9
GND	24	23	DIN10
GND	26	25	DIN11
GND	28	27	DIN12
GND	30	29	DIN13
GND	32	31	DIN14
GND	34	33	DIN15
GND	36	35	FLAG
GND	38	37	WEN
GND	40	39	RESET

The SMT332/372 has two SDB connectors. FIFO channel A uses connector labelled HDR1, and channel B uses HDR2.

RESET and WEN are active low.

RESET will cause a partial FIFO reset only. It will not alter the programmable flag positions.

WEN must be active for data to be written into the FIFO.

DIN0 is the lsb. The data (DIN15:0) must have setup and hold times of 4ns with respect to the rising edge of WCLK.

The standard header used on the top side of the PCB is made by ODU. The part number for this header is: 515-568-035-040-000. The mating IDC socket part number is 525.060.035.040.000.

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Optionally, at build time, the module may be supplied with an 80-way connector mounted on the underside of the TIM. The pin-out of this connector is given here.

Function	Pin	Pin	Function
GND	2	1	WCLKA
GND	4	3	DIN0A
GND	6	5	DIN1A
GND	8	7	DIN2A
GND	10	9	DIN3A
GND	12	11	DIN4A
GND	14	13	DIN5A
GND	16	15	DIN6A
GND	18	17	DIN7A
GND	20	19	DIN8A
GND	22	21	DIN9A
GND	24	23	DIN10A
GND	26	25	DIN11A
GND	28	27	DIN12A
GND	30	29	DIN13A
GND	32	31	DIN14A
GND	34	33	DIN15A
GND	36	35	FLAGA
GND	38	37	WENA
GND	40	39	RESETA
GND	42	41	WCLKB
GND	44	43	DIN0B
GND	46	45	DIN1B
GND	48	47	DIN2B
GND	50	49	DIN3B
GND	52	51	DIN4B
GND	54	53	DIN5B
GND	56	55	DIN6B
GND	58	57	DIN7B
GND	60	59	DIN8B
GND	62	61	DIN9B
GND	64	63	DIN10B
GND	66	65	DIN11B
GND	68	67	DIN12B
GND	70	69	DIN13B
GND	72	71	DIN14B
GND	74	73	DIN15B
GND	76	75	FLAGB
GND	78	77	WENB
GND	80	79	RESETB

Signals ending with an ‘A’ correspond to FIFO channel A, ‘B’ with FIFO channel B.

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To design a custom carrier you will require the TIM specification and the following details of the header for the underside of the PCB. This connector is the same as the standard TIM carrier connectors, namely Hirose FX4 series:

Underside Header: FX4A1-80P-1.27SV

Mating Socket on Carrier: FX4C-80S-1.27DSA

TIM site Socket on Carrier:FX4C1-80S-1.27DSA

Serial Ports

The ‘C6x contains two multi-channel buffered serial ports (McBSP). The signals involved are connected to a 0.1” pitch DIL pin header (JP2). For a full description of signal activity and the serial protocols available, please refer to the relevant TI documentation.

JP2 pin out is given here;

Signal	Pin	Pin	Signal
FSX1	1	2	FSX0
FSR1	3	4	FSR0
DX1	5	6	DX0
DR1	7	8	DR0
CLKX1	9	10	CLKX0
CLKR1	11	12	CLKR0
CLKS1	13	14	CLKS0
GND	15	16	GND

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FPGA Configuration

This device must be configured, by the 'C6x01, before proper operation. To do this, the General Control Register (address 0x0150 0000) must have the PROG bit set, and then cleared. This register is defined here.

General Control Register Bit	Function
8	Set to assert the PROG pin to the FPGA

After the PROG pin has been cycled high and low, the FPGA must have its configuration file loaded a byte at a time using the Comm port control register address (0x0160 0000).

The configuration data is normally read from the flash into SBSRAM and then copied into the FPGA. The format of this data is determined by the Xilinx development tools.

As mentioned in the **boot** section, under normal use this configuration is done automatically.

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