SUNDANCE

SMT335
SMT375

User Manual

Certificate Number FM 55022

Revision History

Date	Comments	Engineer	Version
08/05/00	Comm port	J.V.	0.1
12/06/00	SDB	J.V.	0.2
10/07/00	Pre-release version	J.V.	0.9
26/07/00	First version	J.V.	1.0
27/07/00	Typing error corrected. (Comm Port status)	J.V.	1.1
08/08/00	New Burst mode selection from CP status Global register display the interrupt status	J.V.	1.2
09/08/00	Output FIFO status displays how many words can be sent	J.V.	1.3
14/08/00	Global register and Interrupt control register reordered. (Need Bootv1.2)	J.V.	1.4
03/09/00	SDB naming corrected to A and B. Global Bus modification for DMA use. Comm port drawing modified Boot code Version 1.4 FPGA Firmware Version 2.0 (top335V2_0_6.dat)	J.V.	1.5
14/09/00	NMI routing selection added.	J.V.	1.6
18/09/00	Global Bus transfer example corrected	J.V.	1.7
10/10/00	Global Bus wait state and bus sharing feature added. Comm-port status register: OCPRDY and ICPRDY moved to allow FIFO depth expansion. Firmware version 2.5.6	J.V.	1.8
27/10/00	Global Bus wait state increased to 15. Cf. Control register. Comm-port status register: Full reset bit added for crash recovery. Firmware version 2.7.6	J.V.	1.9

09/11/00	Documentation added for DMA transfers FPGA I/O Slew rate changed to S_12. Firmware version 2.8.6	J.V.	2.0
07/12/00	SDB interrupt flags modified. Global bus tri-state signal not latched. Global bus flag cleared when transfer direction is changed. Comm-port reply disabled during token exchange. Firmware version 2.9.6	J.V.	2.1
11/12/00	SDB Memory mapping updated. Firmware version 3.0.6	J.V.	2.2
24/01/01	Manual updated with quality template. Timer routing detailed. Comm-port drawing corrected. Reprogramming and version control described. SDB Interrupt Bug fixed. SDB handling detailed. Comm-port bug reported. Firmware version 3.3.6	J.V.	2.3
13/4/01	General overhaul and clarification	PSR	3.0
30/8/01	Power consumption and reset timing added. Value of Bit 12-13 of the global control register explained.	J.V.	3.1
11/04/02	Global bus additional feature. Synchronisation with carrier board on SMT328 and SMT310. External trigger for ADC acquisition for SMT118. Fix for Comm-port Burst mode selection between threads in bi-directional transfer. Firmware version 3.11.6	J.V.	3.2

15/05/02	IIOF Interrupt description. Global bus BUSY bit description Interrupt control register 6 address corrected. Global bus transfers description for SMT310 family. Firmware version 3.11.6	J.V.	3.3
30/01/03	Restructure of the document. Double buffered global bus. Will require code change if transfer via dma were used. SDB dma synchronisation changed no software change required. Firmware version 3.13.6	J.V.	3.4

It is important that you use the correct version of the firmware; you should use firmware version 3.13.6 or later.

Check your firmware revision number with the program read_version_335.out and ask for a more recent version if necessary.

E-mail: **support@sundance.com**

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Contacting Sundance

You can contact Sundance for additional information by sending email to **support@sundance.com**

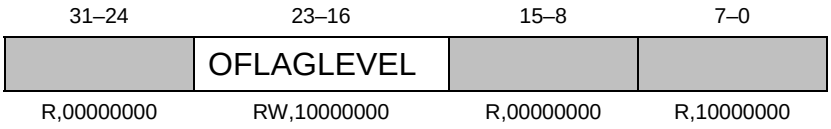
Notational Conventions

SMT335

Throughout this document the term SMT335 will usually be used to refer to both the SMT335 and the SMT375. It should be clear from the context when a distinction is being drawn between the two types of module.

Register Descriptions

The format of registers is described using diagrams of the following form:



The digits at the top of the diagram indicate bit positions within the register and the central section names bits or bit fields. The bottom row describes what may be done to the field and its value after reset. Shaded fields are reserved and should only ever be written with zeroes.

R	Readable by the CPU
W	Writeable by the CPU
RW	Readable and writeable by the CPU

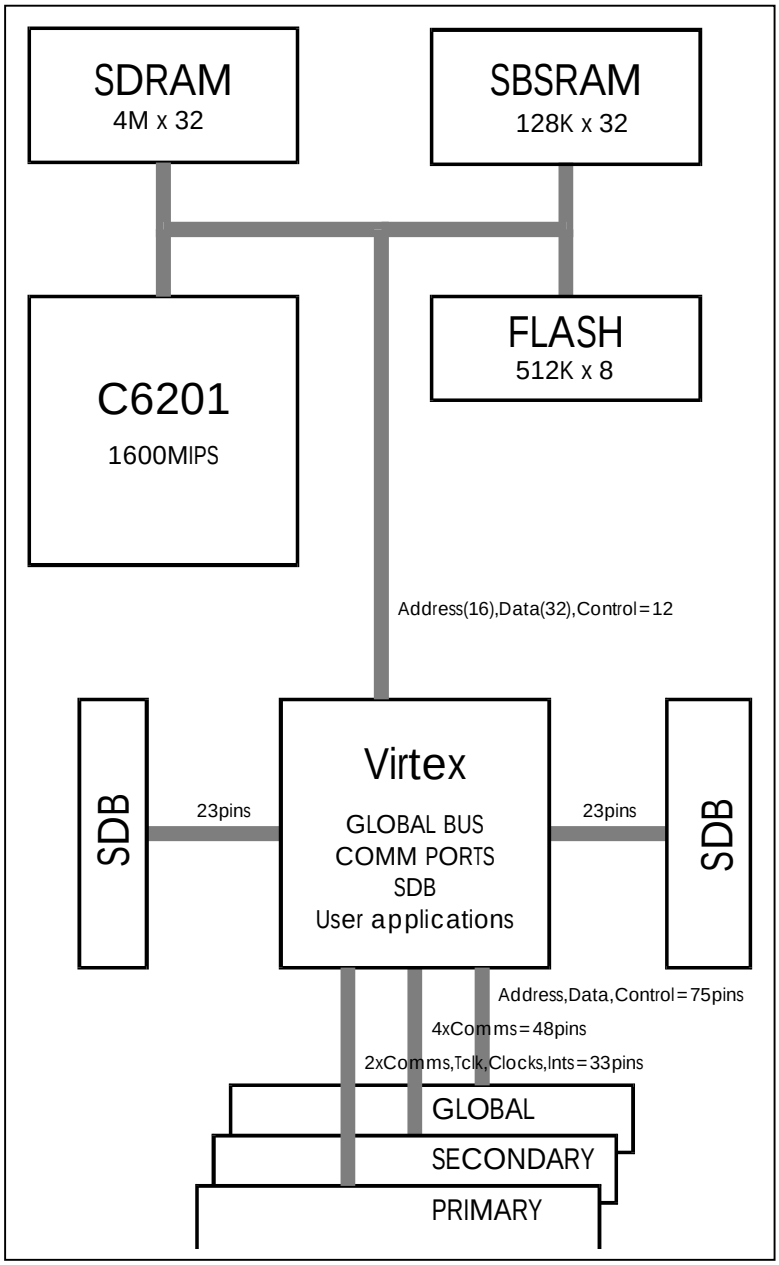
Binary digits indicate the value of the field after reset.

Outline Description

The SMT335 is a C6000-based size 1 TIM offering the following features:

- SMT335: TMS320C6201 processor running at 200MHz
- SMT375: TMS320C6701 processor running at 166MHz
- Six 20MB/s communication ports (comm.-ports)
- 512KB of fast SBSRAM, 16MB of SDRAM
- 512KB Flash ROM for boot code and FPGA programming
- Global expansion connector
- High bandwidth data I/O via 2 Sundance Digital Buses (SDB).

Block Diagram



Architecture Description

The SMT335 TIM consists of a Texas Instruments TMS320C6201 running at 200MHz while the SMT375 has a TMS320C6701 running at 166MHz. Modules are populated with 512KB of synchronous burst SRAM (SBSRAM) and 16MB of synchronous DRAM (SDRAM), giving a total memory capacity of 16.5MB.

A Field Programmable Gate Array (FPGA) is used to manage global bus accesses and implement six communication ports and two Sundance Digital Buses.

TMS320C6201/6701

Bother processors will run with zero wait states from internal SRAM, the TMS320C6201 at 200MHz and the TMS320C6701 at 166MHz.

An on-board synthesiser from MicroClock provides the clock used for the C6000; jumpers on the TIM allow you to select clock speeds from 118MHz to 200MHz. Unlike similar TIMs based on the TMS320C4x, there is no option to provide an external clock source.

The TIM configuration feature is fully implemented. This provides a single open-collector line that can be held low until software configuration has been completed.

Boot Mode

The SMT335 is configured to use the following boot sequence each time it is taken out of reset:

1. The processor copies a bootstrap program from the first 32KB of the flash memory into internal program RAM starting at address 0.
2. Execution starts at address 0.

The standard bootstrap supplied with the SMT335 then performs the following operations:

1. All relevant C6000 internal registers are set to default values;
2. The FPGA is configured from data held in flash memory and sets up the communication ports, the global bus and the Sundance Digital Buses. This step must have been completed before data can be sent to the comm-ports from external sources such as the host or other TIMs;
3. A C4x-style boot loader is executed. This will continually examine the six communication ports until data appears on one of them. The bootstrap will then load a program in boot format from that port; the loader will not read data arriving on other ports. See “Application Development” on page **Error! Bookmark not defined.** for details of the boot loader format;
4. Finally, control is passed to the loaded program.

The delay between the release of the board reset and the FPGA configuration is around 280ms for a SMT335 (200MHz clock) and 330ms for a SMT375 (166MHz). The worse case is with a board clocked at 118MHz (no jumper fitted) in which case the FPGA will be configured 480ms after the reset is released.

A typical time to wait after releasing the board reset is 500ms.

EMIF Control Registers

The C6000 contains several registers that control the external memory interface (EMIF). There is one global control register and a separate register for each of the memory spaces CE0 to CE3. A full description of these registers can be found in the *C60000 Peripherals Reference Guide****Error! Reference source not found.Error! Reference source not found.[Error! Reference source not found.]***.

The standard bootstrap will initialise these registers to the following values:

GC (global control)	0x00003779 0x0000377D	For half speed SBSRAM For full speed SBSRAM (default)
CE0	0x00000040	Indicates SBSRAM
CE1	0x30FF3F03	Defines asynchronous memory timings
CE2	0x00000030	Indicates SDRAM
CE3	0x00000030	VIRTEX FPGA

Note: Bits 12&13 of the Global control register are listed as 'reserved' in the current TI documentation. With earlier versions of the C6000 silicon, these 2 bits controlled the polarity of two clock outputs from the device. To maintain code compatibility for all of our version modules, we have left our documentation with bits 12&13 set.

SBSRAM

Memory space CE0 is used to access 512KB of zero wait-state SBSRAM over the C6000 external memory interface (EMI).

SBSRAM is normally set to run at the speed of the C6000 core clock, but the GC register can be used to reduce this to one half of the core clock speed. The appropriate setting has to be determined in conjunction with the C6000 core speed and the external memory speed; refer to ***Clock Speed*** on page **Error! Bookmark not defined.** for further details.

SDRAM

Memory space CE2 is used to access 16MB of SDRAM over the EMI. The SDRAM operates at one half of the core clock speed.

FLASH

A 512KB Flash ROM device is connected to the C6000 EMI. This device is accessed, a byte at a time, with word addresses from 0x0140 0000 to 0x015F FFFF using strobe CE1 in 32-bit asynchronous mode. Each 32-bit load will give 8 bits of data in bits 7–0 of the result; the state of bits 31–8 is undefined.

The ROM holds boot code for the C6000, configuration data for the FPGA, and optional user-defined code.

A software protection algorithm is in place to prevent programs accidentally altering the ROM's contents. Please contact Sundance for further information about re-programming this device [**Error! Reference source not found.Error! Reference source not found.Error! Reference source not found.Error! Reference source not found.**].

Version control

Revision numbers for both the boot code and FPGA firmware are stored in the Flash ROM during programming as zero-terminated ASCII strings. These revision numbers are located using byte offsets from the base of the Flash ROM (0x01400000). The offsets are held as 4-byte words at the end of the ROM: 0x015FFFF8 for the FPGA firmware offset and 0x0147FFFC for the boot code offset.

The distribution disk contains a program, **`read_version_335.out`**, in the directory **`Reprogramming\version_control`**. You can load and run this program from code composer to display both the FPGA and boot code version numbers.

Reprogramming the firmware and boot code

The **`Reprogramming\flash`** directory of the distribution disk contains a utility that will run under code composer and program the flash ROM. The utility is called **`pflash`*`x_y_z`*`.out`**, where ***`x_y_z`*** is the FPGA version number.

You load the utility with the code composer "Load Program" option from the "File" menu. Once the program has loaded, you should select "Run" from the "Debug" menu. The reprogramming process takes a minute or so and should display "Flash programming complete" when it has finished. After the program has run you should "Halt" the processor from the "Debug" menu and select "Run Free". To confirm that the programming has been successful you should use the Sundance Server to reset the board and execute one of the supplied test programs.

A detailed description of the reprogramming process is available as an Application Note [**Error! Reference source not found.**], which will also help you to develop your own core in the FPGA.

Interrupts

See general firmware description

Communication ports

The SMT335 provides six comm-ports.

See general firmware description

Data rates

When using the communication links of a C6000 you must remember that the links share a single bus, so the performance you get will depend on the way you sequence bus accesses.

C6201 can read at 100MHz from external to internal memory; the rate for the C6701 is 83MHz. If you want to store in external memory then the rate achievable are divided by two as the read and writes share the same bus, which means respectively 50MHz and 41MHz.

The C6000 DMA channels are not efficient when moving data between two external memory areas sharing a common bus; the transfer will take place a word at a time and not in more efficient bursts. This is why it may not be advisable to use DMA to transfer data directly between external memory and a communication link. Performance can be greatly improved by using an intermediate buffer in internal memory.

SDB

The SMT335 provides two Sundance Digital Buses (SDBs).

See general firmware description

SDB update

You should be aware that revisions of the SDB before V3.0.6 have a significantly different treatment of the status flags and a different address is used to program the SDB flag levels for input and output. When upgrading from versions before V3.0.6, you will need to change the code for flag programming and accessing the status bits. You should use version V3.3.6 or above because previous versions could generate spurious interrupts on input.

SDB Clock selection

At any time you can change the speed of an SDB clock by altering SDBCLK.

Module	SDBCLK	Clock Speed
SMT335	0	50MHz
	1	100MHz
SMT375	0	41MHz
	1	83MHz

Global bus

The SMT335 provides one global bus interface.

See general firmware description

The latest global bus interface is double buffered for dma so that it can read ahead the next buffer while the first one is being read by the DSP. Similarly a buffer is being written while the previous one is being sent.

The important thing is to set the global bus operation register before enabling the global bus interrupt on an external interrupt line so that the interrupt generated is the one relevant to the operation (read/write).

This has changed for the SMT335 firmware as it used to need the dma event to be forced for a write and that the external interrupt was enabled before the operation register was set. This is the only change needed when updating from a version of the SMT335 prior to 3.13.6.

Note for SMT310, SMT310Q, SMT300, SMT300Q

Burst Transfer across a 1KBytes page boundary is only supported from version 3.13.6 of the firmware.

To transfer over the PCI the global bus is set-up to be able to perform burst transfer across the PCI bridge chip. A burst transfer is happening whenever the global bus transfer size register is set to transfer more than one word at a time. During a burst a word is transferred on every clock cycle.

The PC memory can be accessed through aperture 0 of the PCI Bridge but a burst transfer must not cross a 1KBytes boundary (256 words). This is because the page size of the bridge chip is 1KBytes.

In other words burst transfer must always be ended on a page boundary. For example you should never burst from the pci address XXXXX3FCH to XXXXX400H. Address XXXXX400H would actually be targeting address XXXXX000H in the pci address space as the page accessed by this burst was in the address range XXXXX000H - XXXXX3FCH.

To make sure a page crossing does not happen during burst access an address alignment has to be performed. The global bus transfer size has to be reduced not to

cross a page. For DMA it is advised to align the transfer on 256 words and then set-up the DMA to transfer by bursts of 256 words to ensure no page boundary is crossed during burst.

Clock Speed

You must consider EMIF device speeds when choosing the appropriate C6000 clock speed. Under most circumstances, the C6201 would be set to 200MHz and have an SBSRAM speed equal to the core speed; the C6701 would be set to 166MHz. See the description of jumper JP1 on page **Error! Bookmark not defined.**.

C6000 clock	SBSRAM	SDRAM	FPGA
133	133	67	67
166	166	83	83
200	100	100	100
200	200	100	100

LED Setting

The SMT335 has 5 LEDs.

LED 1 always displays the state of the FPGA DONE pin. This LED is off when the FPGA is configured (DONE=1) and on when it is not configured (DONE=0).

This LED should go on when the board is first powered up and go off when the FPGA has been successfully programmed. If the LED does not light at power-on, check that you have the mounting pillars and screws fitted properly. If it stays on, the DSP is not booting correctly.

The remaining LEDs can be controlled with the LED register. Writing 1 will illuminate the LED; writing 0 will turn it off.

See general firmware description

CONFIG & NMI

See general firmware description

Timer

See general firmware description

IIOF interrupt

From version 3.11.6 of the firmware it is possible to generate pulses on the external interrupt lines of the TIM.

See general firmware description

Code Composer

This module is fully compatible with the Code Composer debug environment. This extends to both the software and JTAG debugging hardware including the SMT320V4, SMT327, SMT328 and TI's XDS-510.

Application Development

You can develop code for SMT335/375 modules in several ways. The simplest is to use the Sundance SMT6000 Server Loader and its associated libraries.

The Server Loader is an application that runs on a host PC under either Windows 98 or NT and allows you to run COFF-format applications. Modified forms of the TI rts library, one for the C6201 and one for the C6701, support standard C I/O.

The Server Loader will read a **`.out`** file and convert it into C4x-style boot code which is then transmitted down a comm-port to the SMT335.

The boot code is in the following format:

6-word header	Word[1] 1	0x00003779 half speed SBSRAM 0x0000377D full speed SBSRAM (recommended)
	Words 2, 3, 4	0, 0, 0
	Word 5	start address
	Word 6	0
Load Block	Word 1	4*N: Length of load block (in bytes)[2]
	Word 2	Destination address (external memory only)
	Next N words	N data words
0 or more Load Blocks		
Terminator	Word 1	0[3]

[1] A word is 32 bits

[2] The length of each data block will be rounded up to a multiple of 4 bytes if necessary.

[3] Effectively a zero-length Load Block

Operating Conditions

Safety

The module presents no hazard to the user.

EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

General Requirements

The module must be fixed to a TIM40-compliant carrier board.

The SMT335 TIM is in a range of modules that must be supplied with a 3.3v power source. In addition to the 5v supply specified in the TIM specification, these new generation modules require an additional 3.3v supply to be presented on the two diagonally-opposite TIM mounting holes. The lack of this 3.3v power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended.

This module is not directly compatible with earlier generations of TIM motherboards, although the 3.3v supply can be provided from a separate source. It is, however, compatible with the latest generation of Sundance TIM carrier boards such as the SMT320V4 and subsequent versions (PCI), and SMT328 (VME), which present the 3.3v via conductive mounting pillars.

Use of the TIM on SMT327 (cPCI) motherboards may require a firmware upgrade. If LED #1 on the SMT335 remains illuminated once the TIM is plugged in and powered up, the SMT327 needs the upgrade. The latest firmware is supplied with all new boards shipped. Please contact Sundance directly if you have an older board and need the upgrade.

A SMT320V3 motherboard can be used providing a SMT335 TIM is not located in the first slot; putting one there prevents the SMT320V3 from coming out of reset. Any other type of TIM must be placed in the first slot of this motherboard to ensure correct operation.

The external ambient temperature must remain between 0°C and 40°C, and the relative humidity must not exceed 95% (non-condensing).

Power Consumption

The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity. The maximum power consumption is 6W.

Serial Ports

The C6000 contains two multichannel buffered serial ports (McBSP). The signals involved are connected to a 0.1” pitch DIL pin header (JP2). For a full description of signal activity and the serial protocols available, please refer to Chapter 11 of [**Error! Reference source not found.**].

Signal	Pin	Pin	Signal
FSX1	1	2	FSX0
FSR1	3	4	FSR0
DX1	5	6	DX0
DR1	7	8	DR0
CLKX1	9	10	CLKX0
CLKR1	11	12	CLKR0
CLKS1	13	14	CLKS0
GND	15	16	GND

C6201 Memory Map

Starting Address	RESOURCE	Refer to
00000000	Internal Program RAM	
00010000	Reserved	
00400000 – 0047FFFF	External Memory Space CE0 512KB SBSRAM	SBSRAM
01400000 – 015FFFFF	External Memory Space CE1 512KB Flash	Flash
01800000	Internal Peripherals	
01C00000	Reserved	
02000000 -02FFFFFF	External Memory Space CE2 16MB SDRAM	SDRAM
03000000 – 03FFFFFF	External Memory Space CE3 See Virtex memory map	Comm-ports, SDB, Global bus
04000000	Reserved	
80000000	Internal Data RAM	
80010000	Reserved	
80400000	Reserved	

Flash Access

Address	Resource		
	ED31	ED30	CE1
01400000 – 015FFFFF	0	0	Read Flash / Write Flash
	0	1	Read Flash / Pulse PROG
	1	0	Read Flash / Write CCLK
	1	1	Read Flash / Write Flash

Virtex Memory Map

See general firmware description with i = 18

The memory mapping is as follows:

```
#define CP0                     (volatile unsigned int *)0x03000000
#define CP1                     (volatile unsigned int *)0x03080000
#define CP2                     (volatile unsigned int *)0x03100000
#define CP3                     (volatile unsigned int *)0x03180000
#define CP4                     (volatile unsigned int *)0x03200000
#define CP5                     (volatile unsigned int *)0x03280000
#define CP0_STAT                (volatile unsigned int *)0x03040000
#define CP1_STAT                (volatile unsigned int *)0x030C0000
#define CP2_STAT                (volatile unsigned int *)0x03140000
#define CP3_STAT                (volatile unsigned int *)0x031C0000
#define CP4_STAT                (volatile unsigned int *)0x03240000
#define CP5_STAT                (volatile unsigned int *)0x032C0000
#define GBSTAT                  (volatile unsigned int *)0x03340000
#define SDBSTAT                 (volatile unsigned int *)0x03380000
#define STAT                    (volatile unsigned int *)0x033C0000
#define SDBA                    (volatile unsigned int *)0x03400000
#define SDBB                    (volatile unsigned int *)0x03500000
#define SDBA_STAT               (volatile unsigned int *)0x03480000
#define SDBB_STAT               (volatile unsigned int *)0x03580000
#define SDBA_INPUTFLAG          (volatile unsigned int *)0x03440000
#define SDBB_INPUTFLAG          (volatile unsigned int *)0x03540000
#define SDBA_OUTPUTFLAG         (volatile unsigned int *)0x034C0000
#define SDBB_OUTPUTFLAG         (volatile unsigned int *)0x035C0000
#define GLOBAL_BUS              (volatile unsigned int *)0x03A00000
#define GLOBAL_BUS_CTRL         (volatile unsigned int *)0x03800000
#define GLOBAL_BUS_START        (volatile unsigned int *)0x03880000
#define GLOBAL_BUS_LENGTH       (volatile unsigned int *)0x03900000
#define TCLK                    (volatile unsigned int *)0x03C00000
#define TIMCONFIG               (volatile unsigned int *)0x03C80000
#define LED                     (volatile unsigned int *)0x03D00000
#define IIOF                    (volatile unsigned int *)0x03D80000
#define INTCTRL4                (volatile unsigned int *)0x03E00000
#define SDBINTCTRL4             (volatile unsigned int *)0x03E40000
```

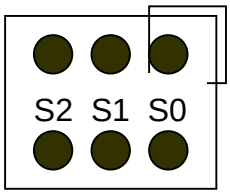
```
#define INTCTRL5                    (volatile unsigned int *)0x03E80000
#define SDBINTCTRL5                 (volatile unsigned int *)0x03EC0000
#define INTCTRL6                    (volatile unsigned int *)0x03F00000
#define SDBINTCTRL6                 (volatile unsigned int *)0x03F40000
#define INTCTRL7                    (volatile unsigned int *)0x03F80000
#define SDBINTCTRL7                 (volatile unsigned int *)0x03FC0000
```

Jumpers

JP1: Clock speed select

S2	S1	S0	C6000 CLK (MHz)
IN	IN	IN	200
IN	IN	OUT	182
IN	OUT	IN	167
IN	OUT	OUT	154
OUT	IN	IN	143
OUT	IN	OUT	133
OUT	OUT	IN	125
OUT	OUT	OUT	118

S0, S1 and S2 refer to the following link positions on JP1.



JP2: Serial port header

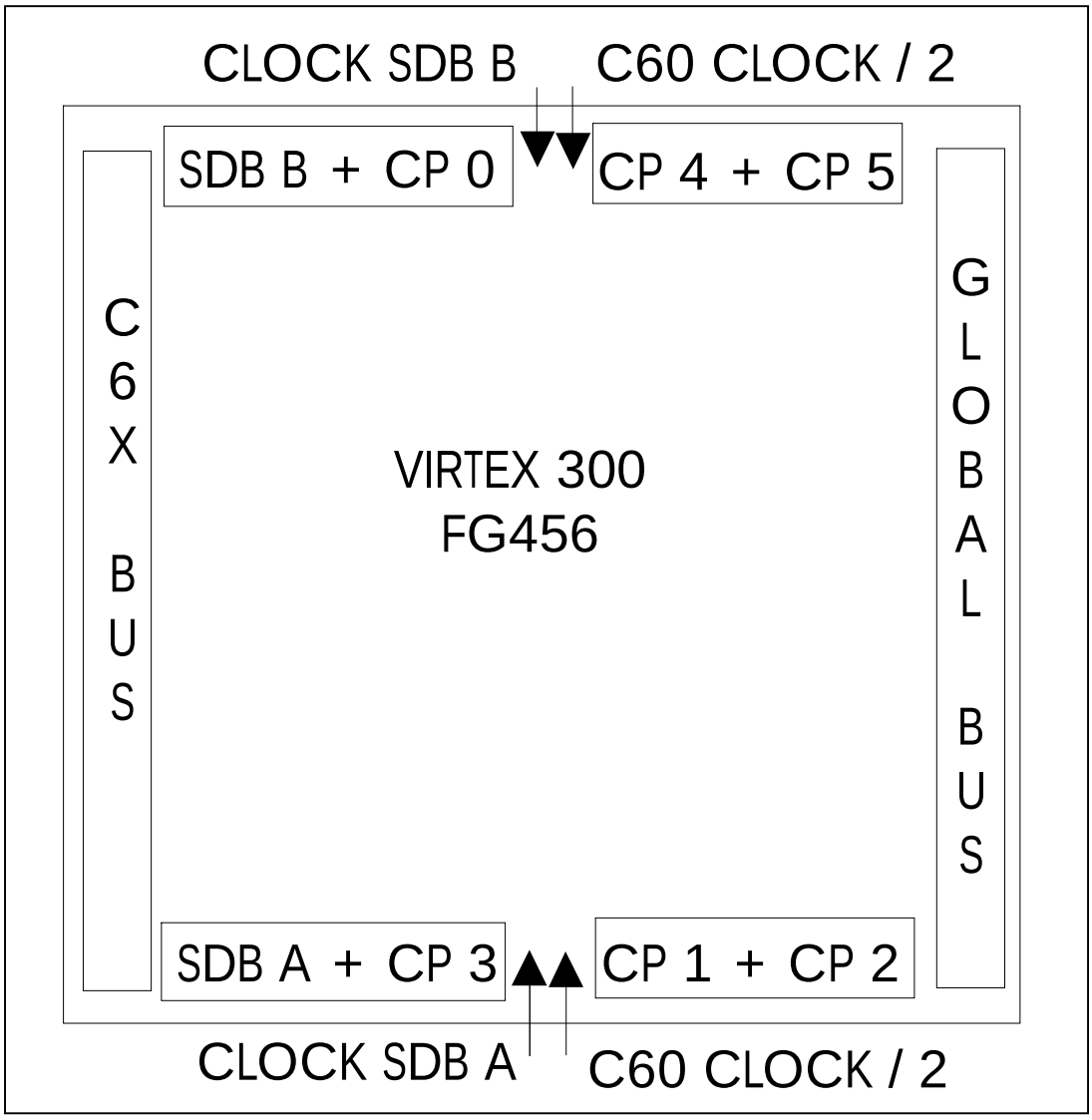
Refer to the *TMS320C6201 Peripheral Reference Guide* [**Error! Reference source not found.**] for a description of the signals and their usage.

2	4	6	8	10	12	14	16
FSX0	FSR0	DX0	DR0	CLKX0	CLKR0	CLKS0	GND
FSX1	FSR1	DX1	DR1	CLKX1	CLKR1	CLKS1	GND
1	3	5	7	9	11	13	15

SDB Pin-Out

Pin	Signal	Signal	Pin
1	CLK	GND	2
3	D0	GND	4
5	D1	GND	6
7	D2	GND	8
9	D3	GND	10
11	D4	GND	12
13	D5	GND	14
15	D6	GND	16
17	D7	GND	18
19	D8	GND	20
21	D9	GND	22
23	D10	GND	24
25	D11	GND	26
27	D12	GND	28
29	D13	GND	30
31	D14	GND	32
33	D15	GND	34
35	UD0	DIR	36
37	WEN	REQ	38
39	UD1	ACK	40

Virtex layout



Virtex Pin-Out

A1	
A2	C0S10
A3	SDBD15
A4	SDBD12
A5	SDBD9
A6	C0S11
A7	SDBD6
A8	SDBD3
A9	C0S4
A10	SDBD0
A11	CLK100
A12	C5S5
A13	C5S6
A14	C5S7
A15	/C60NMI
A16	C5S8
A17	/C60IACK
A18	
A19	
A20	
A21	
A22	

B1	ED0
B2	
B3	SDBBWEN
B4	C0S5
B5	SDBBUD0
B6	SDBBUD1
B7	SDBBD13
B8	SDBBD10
B9	SDBBD7
B10	SDBBD4
B11	SDBBD1
B12	C5S9
B13	C4S10
B14	C5S10
B15	C5S11
B16	/TIMIACK
B17	IIOF2
B18	/TIMNMI
B19	CONFIG
B20	
B21	
B22	CCLK

C1	ED1
C2	ED15
C3	
C4	
C5	C0S8
C6	C0S6
C7	C0S9
C8	DIRB
C9	
C10	CLKB
C11	CLKB
C12	C5S0
C13	C5S1
C14	C5S2
C15	C5S3
C16	C5S4
C17	
C18	
C19	
C20	
C21	
C22	GA27

D1	ED16
D2	/AWE
D3	
D4	
D5	SDBBD2
D6	SDBBD5
D7	SDBBD8
D8	SDBBD11
D9	SDBBD14
D10	SDBBREQ
D11	C4S0
D12	C4S1
D13	C4S2
D14	C4S3
D15	C4S4
D16	C4S5
D17	C4S6
D18	GA29
D19	
D20	Config D0
D21	GA26
D22	STAT0

Comm-ports are numbered C0 to C5. Each has 12 elements (i.e. CnS[0..11]).

CnS0	STRB
CnS1	RDY
CnS2	REQ
CnS3	ACK
CnS[4..11]	Data[0..7]

E1	ED2
E2	/RAS
E3	ED3
E4	ED4
E5	
E6	SDBBACK
E7	C0S0
E8	C0S7
E9	C0S1
E10	C0S2
E11	C0S3
E12	C4S7
E13	/TIMNMI
E14	C4S11
E15	C4S8
E16	C4S9
E17	/RESET
E18	
E19	GA30
E20	GA25
E21	GA24
E22	GA23

F1	ED5
F2	ED6
F3	ED7
F4	ED8
F5	ED9
F6	
F7	
F8	
F9	
F10	
F11	
F12	
F13	
F14	
F15	
F16	
F17	
F18	GA22
F19	GA21
F20	GA20
F21	STAT1
F22	GA19

G1	ED10
G2	ED17
G3	ED11
G4	ED12
G5	ED13
G6	
G7	
G8	
G9	
G10	
G11	
G12	
G13	
G14	
G15	
G16	
G17	
G18	GA18
G19	GA17
G20	GA16
G21	GA15
G22	GA14

H1	ED14
H2	ED22
H3	ED23
H4	/CAS
H5	ED24
H6	
H7	
H8	
H9	
H10	
H11	
H12	
H13	
H14	
H15	
H16	
H17	
H18	STAT2
H19	GA13
H20	
H21	GA12
H22	

J1	ED18
J2	ED25
J3	ED26
J4	ED19
J5	ED27
J6	
J7	
J8	
J9	
J10	
J11	
J12	
J13	
J14	
J15	
J16	
J17	
J18	GA28
J19	GA11
J20	GA10
J21	GA8
J22	GA7

K1	ED28
K2	ED20
K3	/SDRAMWE
K4	ED29
K5	ED30
K6	
K7	
K8	
K9	
K10	
K11	
K12	
K13	
K14	
K15	
K16	
K17	
K18	GA6
K19	GA5
K20	
K21	STAT3
K22	GA4

L1	ED31
L2	ED21
L3	/SDRAMCS
L4	/ARE
L5	/ARDY
L6	/AOE
L7	
L8	
L9	
L10	
L11	
L12	
L13	
L14	
L15	
L16	
L17	GA9
L18	/AE
L19	GA3
L20	GA2
L21	GA1
L22	GA0

M1	EA2
M2	EA17
M3	EA3
M4	EA4
M5	EA5
M6	EA6
M7	
M8	
M9	
M10	
M11	
M12	
M13	
M14	
M15	
M16	
M17	
M18	
M19	/DE
M20	GD31
M21	GD30
M22	GD29

N1	EA18
N2	TIN0
N3	EA7
N4	EA8
N5	EA9
N6	
N7	
N8	
N9	
N10	
N11	
N12	
N13	
N14	
N15	
N16	
N17	
N18	GD28
N19	GD27
N20	GD26
N21	GD25
N22	

P1	EA19
P2	EA10
P3	EA11
P4	EA12
P5	EA20
P6	
P7	
P8	
P9	
P10	
P11	
P12	
P13	
P14	
P15	
P16	
P17	
P18	GD24
P19	GD23
P20	GD22
P21	GD21
P22	GD20

R1	EA13
R2	EA14
R3	EA21
R4	TIN1
R5	EA15
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	
R16	
R17	
R18	GD19
R19	GD18
R20	GD17
R21	
R22	GD16

T1	EA16
T2	/BE0
T3	TCLK0
T4	/BE1
T5	/BE2
T6	
T7	
T8	
T9	
T10	
T11	
T12	
T13	
T14	
T15	
T16	
T17	
T18	GD15
T19	GD14
T20	GD13
T21	GD12
T22	

U1	/BE3
U2	DMAC0
U3	DMAC1
U4	DMAC2
U5	M1=V33
U6	
U7	
U8	
U9	
U10	
U11	C3S0
U12	C1S0
U13	
U14	
U15	
U16	
U17	
U18	GD11
U19	GD10
U20	GD9
U21	GD8
U22	GD7

V1	LED1
V2	LED2
V3	LED3
V4	LED4
V5	
V6	
V7	C3S1
V8	C3S2
V9	C3S3
V10	C3S4
V11	C3S5
V12	C1S1
V13	C1S2
V14	C1S3
V15	C1S4
V16	C1S5
V17	C1S6
V18	
V19	INIT
V20	GD6
V21	GD5
V22	GD4

W1	DMAC3
W2	
W3	TOUT0
W4	
W5	C3S6
W6	C3S7
W7	C3S8
W8	SDBAWEN
W9	SDBAD14
W10	SDBAD13
W11	SDBAD11
W12	CLK100
W13	/TIMCE1
W14	C1S7
W15	/TIMLOCK
W16	C1S8
W17	C1S9
W18	C1S10
W19	
W20	/PROG
W21	GD3
W22	GD2

Y1	TCLK1
Y2	TOUT1
Y3	
Y4	M2=V33
Y5	
Y6	SDBAUD0
Y7	SDBAD8
Y8	SDBAD5
Y9	SDBAD2
Y10	
Y11	CLKA
Y12	C1S11
Y13	
Y14	/TIMRW1
Y15	/TIMSTRB1
Y16	INT4
Y17	INT5
Y18	INT6
Y19	DONE
Y20	
Y21	
Y22	GD1

AA1	
AA2	
AA3	SDBAD10
AA4	C3S9
AA5	SDBAUD1
AA6	C3S10
AA7	C3S11
AA8	DIRA
AA9	SDBAD7
AA10	SDBAD4
AA11	SDBAD1
AA12	INT7
AA13	C2S8
AA14	IIOF0
AA15	IIOF1
AA16	/TIMRDY1
AA17	C2S0
AA18	C2S1
AA19	C2S2
AA20	C2S3
AA21	
AA22	GD0

AB1	
AB2	M0=V33
AB3	SDBAD15
AB4	SDBAD12
AB5	SDBAD9
AB6	SDBAD6
AB7	SDBAREQ
AB8	SDBAACK
AB9	SDBAD3
AB10	SDBAD0
AB11	CLKA
AB12	TIMPAGE1
AB13	C2S4
AB14	H3
AB15	C2S5
AB16	C2S9
AB17	C2S6
AB18	C2S7
AB19	C2S10
AB20	C2S11
AB21	H1
AB22	

Bibliography

1. *TMS320C6201/C6701 Peripherals Reference Guide (literature number SPRU190)* describes common peripherals available on the TMS320C6201/C6701 digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, multichannel-buffered serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.
2. *Application Note: Flash Programming*
3. *TIM-40 MODULE SPECIFICATION Including TMS320C44 Addendum*
4. *SDB Technical Specification V2.1* or above
5. *TMS320C4x User's Guide (literature number SPRU063)* describes the C4x 32-bit floating-point processor, developed for digital signal processing as well as parallel processing applications. Covered are its architecture, internal register structure, instruction set, pipeline, specifications, and operation of its six DMA channels and six communication ports. Software and hardware applications are included.
6. *Application Note: Creating New Firmware*

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