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SYCARD TECHNOLOGY

PCCtest 172 Technical Reference Manual

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Preliminary

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1. Introduction

The PCCtest 172 16-bit PC Card tester is designed to provide manufacturers of PCMCIA based hosts a quick method of testing and verifying the operation of the PC Card sockets.

The PCCtest is Type II PC Card that plugs into a standard PC Card Type II or III socket. The board is designed for both automated GO/NO-GO testing and component level debug. Test software is required on the host system.

A custom ASIC is the core of the PCCtest 172. All testing logic is contained in this ASIC. The PCCtest contains an on-board A/D to provide accurate measurement of VCC and VPP voltages.

Sycard Technology provides a DOS application to test Intel 82365SL compatible socket controllers. Simple command line invocation allows tests to be embedded into batch test files. OEMs that wish to use the PCCtest on a non-DOS platform can use this specification to develop custom test applications.

1.1 Differences between the PCCtest 172 and the PCCtest 170

Although the PCCtest 170 and the 172 appear to be the same, there are slight differences that make the PCCtest 172 suitable for certain applications. The PCCtest 172 was created to solve a problem with socket controllers that do not support 8 bit I/O windows (e.g. StrongArm SA-1100). On power-up the PCCtest 170 and 172 will put the WP/IOIS16# signal into a low state. Socket controllers that do not support 8 bit windows will use the IOIS16# signal to determine if the register is 16-bit or 8-bit. These socket controllers will not be able to access the odd numbered registers in the PCCtest 170. Since the control of the WP/IOIS16# is located in an odd numbered register (in the PCCtest 170) it is impossible to put the card into 8-bit mode. The PCCtest 172 solves this problem by placing the WP/IOIS16# control in an even numbered register. Table 1.1-1 illustrates the differences between the PCCtest 170 and 172.

Control Bit	PCCtest 170	PCCtest 172
WP/IOIS16#	MISC Register (offset 3) bit 6	CNTL Register (offset 4) bit 0
RDY/BSY/IREQ#	MISC Register (offset 3) bit 7	CNTL Register (offset 4) bit 1
ADCCE	CNTL Register (offset 4) bit 0	MISC Register (offset 3) bit 6
ADCLK	CNTL Register (offset 4) bit 1	MISC Register (offset 3) bit 7

Table 1.1-1 PCCtest 170 and 172 differences

In addition to register changes, the PCCtest 172 CIS has been modified to identify the model.

2.0 Architecture of the PCCtest

Figure 2.0-1 Illustrates the architecture of the PCCtest model 172. The functional blocks can be partitioned in to the following major sub-sections:

- Tester ASIC (Test ASIC)
- A/D Converter and Logic

All interfaces to the PCCtest unit is via eight registers contained in the test ASIC. These eight registers control the various test functions contained within the PCCtest unit. The location at which these registers are accessed depends on which mode the PCCtest unit is in. On power-up, these test registers are located in attribute memory space. The test software can then enable I/O and/or common memory modes to test the various access modes of the PC Card interface.

There are two major types of tests performed by the PCCtest unit - those implemented by the Test ASIC and the A/D tests. The Test ASIC based tests are designed to test the basic functionality of the interface. These tests will verify the basic operation of the interface including access strobes, data bus and address bus. Once these basic access modes are verified, the A/D test verifies the Vcc and Vpp levels.

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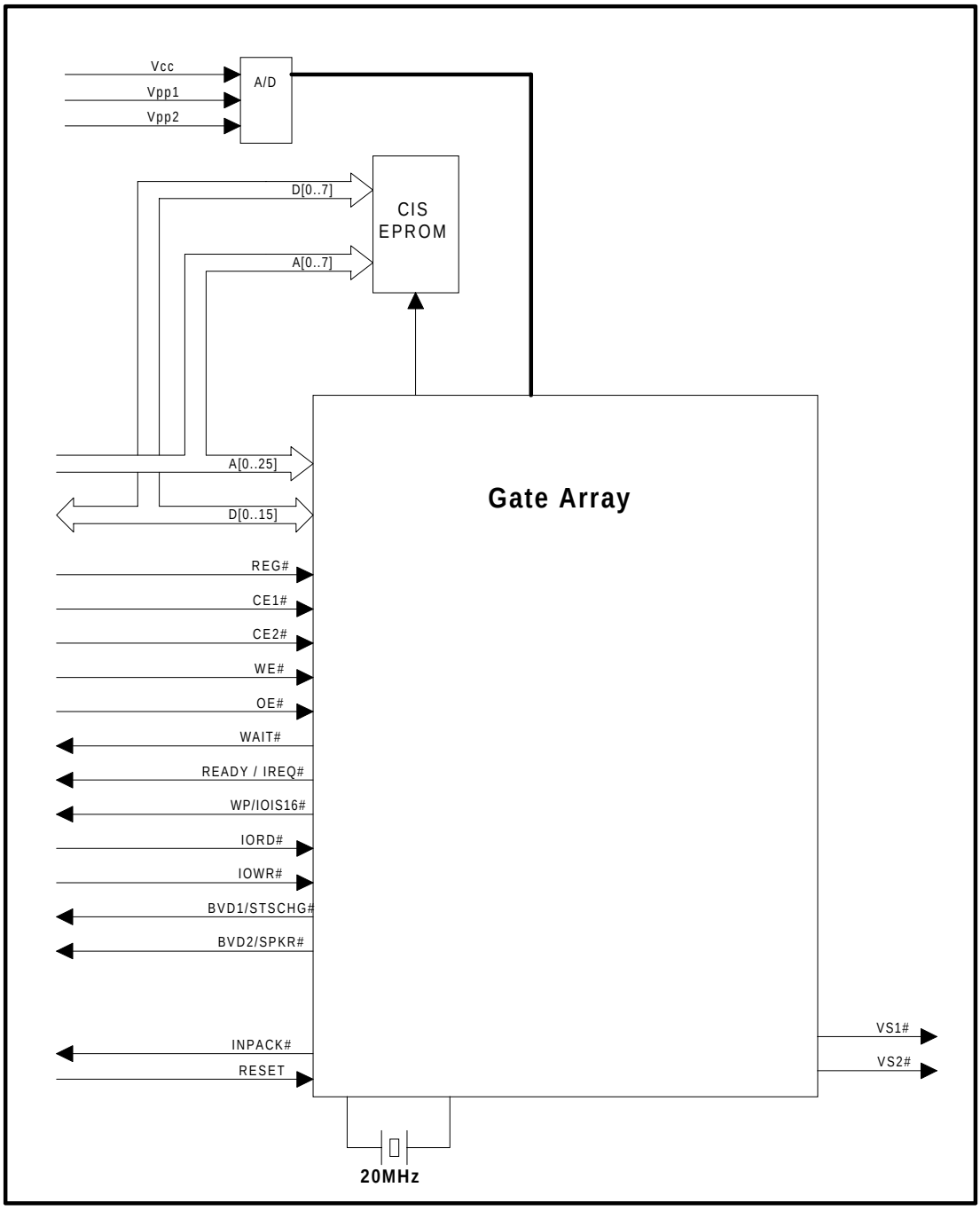


Figure 2.0-1 PCCtest 172 block diagram

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3.0 Testing the 16-bit PC Card Interface

Most of the basic interface tests are handled in the Test ASIC. Eight registers control the operation of the Test ASIC. Appendix A lists the Test ASIC's register description. Note that most write registers cannot be read back. It is up to the programmer to maintain an image of the write registers, since a read/modify/write operation is not possible for most of the register bits. Testing the 16-bit PC Card interface involves writing various test patterns to the PCCtest unit through the host socket controller. Status read back through these registers verify the functionality of the various portions of the interface.

3.1 Initializing the PCCtest

The PCCtest must be powered through the host socket before any test operations can begin. The PCCtest model 172 can be powered to 3.3 or 5.0 Volts. The PCCtest 172 requires a power-on reset to initialize the internal operating circuitry. Care must be taken when switching operating voltages on the PCCtest. Do not switch from 3.3V to 5.0V or 5.0V to 3.3V without allowing the power to go to first go to 0V. The PCCtest on-board circuitry requires a minimum of 1200ms after Vcc is stable to initialize.

***Note**: Vpp1 and Vpp2 can be measured by the PCCtest, but are not required for PCCtest operation.*

3.2 Opening a Memory and I/O Window to the PCCtest

In order to access the test resources in the PCCtest, an 8-bit attribute memory and an 8-bit I/O window must be opened to the PCCtest. Both an I/O and memory window is required to fully test the PC Card interface. The PCCtest contains eight 8-bit registers. These registers are accessed as 8 consecutive bytes.

***Note**: For information on opening an I/O window, consult your socket controller chip user's manual.*

A memory window with a length of at least 8 bytes is required to test the interface's memory interface. Most socket controllers provide a minimum window length of 4K bytes.

3.2.1 PCCtest Memory and I/O Map

The PCCtest 172 supports all three address spaces defined in the PC Card Standard. On power-up the PCCtest 172 responds to attribute memory accesses. Attribute memory reads from address 0H-FFH access the on-board Card Information Structure (CIS). The CIS contains tuples that identify the PCCtest 172. Appendix B contains a listing of the tuples contained in the CIS. Attribute Memory addresses 100H-107H contains the control registers used to test the PC Card Interface. The function of these registers are described in Appendix A.

Attribute Space	Description
0H – 0FFH	Card Information Structure
100H – 107H	Control Registers
108H-FFFFFFFH	Control Registers (mirrored)

Table 3.2-1 Attribute Memory Space

The MODE register (offset 6) controls, which address spaces, the PCCtest responds to. Once the PCCtest unit it programmed out of its power-on mode, the control registers are accessed through I/O or common memory space. When accessing these registers in I/O or common memory mode, the registers appear at offset 0. Since there is no address decode for I/O or common memory mode, these registers are accessible on any 8 bit boundary. The following table describes the various PCCtest modes.

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MODE.2	MODE.1	MODE.0	PCCtest Mode	PCCtest operating mode
0	0	0	MODE 0	Attribute memory space enabled, I/O and common memory accesses disabled
0	0	1	MODE 1	I/O space enabled, attribute and common memory space disabled
0	1	0	MODE 2	I/O space at 1F0H-1F7H enabled, attribute and common memory space disabled
0	1	1	MODE 3	I/O space at 170H-177H enabled, attribute and common memory space disabled
1	0	0	MODE 4	Common and attribute memory space enabled, I/O space disabled
1	0	1	MODE 5	Common memory and I/O space enabled. Attribute space disabled.

Table 3.2-2 PCCtest modes accessed through MODE register

***Note**: Once Mode 1, 2, 3 or 5 is enabled, all access to attribute memory space is disabled. Access to the PCCtest internal registers should be made through the enabled common memory or I/O space.*

***Note**: The RESET signal will NOT put the PCCtest into its power-on state. To reset the PCCtest unit, cycle power to the slot.*

3.3 Preliminary Tests

Before accessing the PCCtest hardware, the test software should verify the basic operation of the socket controller and that the PCCtest is properly inserted into the socket. This will avoid any unnecessary delays or erroneous error messages. The following sequence is used in Sycard's PCT172 software:

1. Verify socket controller is present by executing a simple register test.
2. Power-up socket.
3. Verify that the socket controller has powered up the slot (through the socket controller status)
4. Wait 1200ms for PCCtest to initialize.
5. Verify card detects are active (CD1# and CD2# are low)

If any of these tests fail, further testing is not possible.

3.4 Basic Tests

Once the socket controller has been verified and card detects are active, the PCCtest functions can be accessed. This part of the test procedure verifies the basic read/write operation of the card. If any failures are detected in the basic test, more advanced tests may return erroneous results. In order to run the first set of tests, an attribute memory window to the card must be opened.

a) Read the CIS and compare with values contained in Appendix B.
b) Basic 8-bit attribute memory read/write to the DATALO register - Verify basic 8-bit memory read.
c) Basic 16-bit attribute memory read/write to the DATALO/DATAHI register - Verify basic 16-bit memory read.

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Once these tests pass, further more detailed tests can be run.

Note: Basic 8-bit operation of the PCCtest requires the following signals to be working:

D[7:0]
OE#
WE#
CE1#
A[2:0]

3.5 Data Tests

The 16-bit PC Card data bus may be tested through several methods. When the PCCtest 172 is in MODE 0 the host writes data to the data latches DATALO at attribute memory offset 100H or DATAHI at 101H. Both 8 and 16 bit accesses are allowed. Data is latched into these registers on an attribute memory write to the DATALO and DATAHI registers. Once data is written, it can be read back to verify that all data bits that have been written are correct.

The data pattern test can be also run via I/O or common memory accesses. The test software enables I/O or common memory accesses via the MODE register at attribute memory offset 106H. See table 3.2-2 for the valid modes. Data pattern tests can be run through attribute memory, common memory or I/O space depending on the setting of the MODE register. Common and attribute memory data pattern tests can be accomplished by accessing the same DATALO and DATAHI registers starting at offset 0 in I/O or memory space. On power-on reset access to these registers through the memory space are disabled.

Prior to running the data test, the lower 8 bits of the data bus can be verified by reading the CIS data. A listing of the CIS is contained in Appendix B.

3.6 Address and REG# Tests

Writing various address patterns to the PCCtest unit can test the PC Card's 26-bit address bus. All address bits can be latched and read through the PC Card host interface. The address latching circuit must be armed prior to the access that triggers the latching circuitry. Addresses are latched on the falling edge of the control strobes, WE#, OE#, IORD#, or IOWR#.

***Note**: The latching signal is a logical OR of the OE#, WE#, IORD# and IOWR# strobes qualified by either CE1# or CE2#.*

Arming of the address latches is accomplished through the ALAT bit in CNTL register (offset 4). A low to high transition of this bit will arm the latch. Any access after this arm will result in the latching of all 26-address signals on the interface. The following C code is used to arm the address latch:

```
outportb(tester_addr+4,reg4_image & 0xfb);
outportb(tester_addr+4,reg4_image | 0x04);
```

***Note**: tester_addr is the base I/O address programmed into the host socket controller I/O mapping registers.*

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The latched values of the address and REG- signal may be read directly from the registers

Signal	Register	Offset	Description
A[7:0]	LADDRLO	4	A0-A7
A[15:8]	LADDMID	5	A8-A15
A[23:16]	LADDHI	2	A16-A23
A24	LATMISC.0	3	A24
A25	LATMISC.7	3	A25
CE1#	STBLAT.2	7	Latched CE1#
CE2#	STBLAT.3	7	Latched CE2#
OE#	STBLAT.0	7	Latched OE#
WE#	STBLAT.1	7	Latched WE#
IORD#	STBLAT.4	7	Latched IORD#
IOWR#	STBLAT.5	7	Latched IOWR#
REG#	LATMISC.5	3	Attribute Memory Select

Table 3.6-1 Address Latch Locations

The following procedure is used to latch the address and read the data from the address latches to create a 26-bit address.

1. Clear the ALAT bit in CNTL register at offset 4.
2. Set the ALAT bit in the CNTL register. The address latch is now armed.
3. Access the card with IORD#, IOWR#, OE# or WE# strobe. The address of the access is latched on the falling edge of the strobe.
4. Read the lower 8 bits A[7:0] from the LADDRLO register at offset 4.
5. Read the contents of the A[15:8] latch from the LADDMID register at offset 5.
6. Read the contents of the A[23:16] latch from the LADDHI register at offset 2.
7. Read the contents of the A[25:24] and REG# latch from the LATMISC register at offset 3.
8. Read the contents of the CE1#, CE2# OE#,WE#,IORD#,IOWR# from the STBLAT register at offset 7.

3.7 Timing Measurements

The PCCtest provides a flexible timing measurement circuit providing 50ns resolution. This circuit can measure from the rising/falling edge of any of the control strobes to the rising falling edge of the same set of signals. The following table lists the various control strobes that can be measured:

Signal	Description	TCR Value
OE#	Memory Read Strobe	08H
WE#	Memory Write Strobe	19H
IORD#	I/O Read Strobe	6EH
IOWR#	I/O Write Strobe	7FH
CE1#	Chip Enable 1	2AH
CE2#	Chip Enable 2	3BH

Table 3.7-1 Common Strobe Measurements TCR Values

The signal and polarity that start the timer is selected via the STR[2:0] and the STRPOL bits in the TCR register. The STP[2:0] and STPPOL bits determine the signal that stops the timer. The following examples illustrate the values programmed into the TCR register (offset 2) for various timing measurements:

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Timing Measurement	TCR Value
Falling edge of CE1# to rising edge of OE#	A0H
Pulse width of IORD#	6EH
Pulse width of IOWR#	7FH
Rising edge of CE1# to rising edge of OE#	20H
Pulse width of WE#	19H

Table 3.7-2 Various Strobe Measurements TCR Values

As with the address latching circuit, the timing logic is armed and the next access to the card is measured. The timing measurement is armed through an I/O write to the TRST register (offset 5). Once armed, the timer will start on first instance of the value programmed into the STR[2:0] register. The value can be read from the TIM register (offset 6). The value read from the TIM register is multiplied by the sample rate (50ns) to obtain the strobe width.

3.8 Testing RESET

The RESET signal is an input to the PCCtest unit. RESET is only monitored by the PCCtest and will not reset the PCCtest. The current state of the RESET signal can be read from RESET bit in the LATMISC register (offset 3 bit 4). Testing of RESET involves forcing the state of RESET and reading the status in the RESET bit in the LATMISC register.

In some socket controllers when RESET is asserted, the PC Card interface is tri-stated or disabled. In systems such as these, the previously described method of testing RESET will not work. With socket controllers such as these, the PCCtest 172 contains a RESET latch that stores the fact that a transition occurred RESET. The status of this latch can be read from LRESET bit in the STBLAT register (offset 7 bit 7). This latch is armed by setting, then clearing, the CLR_RST bit the CNTL register (offset 4 bit 4). Once the reset latch is armed the test software will then strobe the RESET signal from high to low. The latch will capture the low to high transition of the reset signal. Software can verify this by reading the LRESET bit in the STBLAT register

3.9 INPACK# Tests

PCCtest can generate INPACK# on all I/O reads. Most socket controllers can use INPACK# to gate the PC Card data on to the host system data bus. Setting the INPKEN bit in the CNTL control register (offset 4 bit 3) enables INPACK# generation on all I/O reads.

3.10 Testing WAIT#

A programmable wait state generator is used to generate wait states to simulate slow I/O or memory devices. The wait state generator is capable of generating wait states up to 3160ns. This covers the full range of PC card access times. Used in conjunction with the pulse measuring circuits can result in accurate measurement of read/write strobe widths. Timing for the wait state generator is based on the PCCtest main crystal (20Mhz).

The wait state generator is accessed through WAIT[0:2] bits in the MISC control register at offset 3 bits [0:2]. In addition to the WAIT[0:2] bits, the WAITEN bit at offset 3 bit 3 must be set to enable wait states.

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WAIT 2	WAIT 1	WAIT 0	Time in ns
0	0	0	0
0	0	1	50
0	1	0	100
0	1	1	200
1	0	0	400
1	0	1	800
1	1	0	1650
1	1	1	3160

Table 3.10-1 Wait state delays

3.11 Testing BVD1 and BVD2

The BVD1 and BVD2 signal are outputs from the PCCtest card. They are implemented as parallel port bits in the CNTL register at offset 4. The host software writes various patterns to these bits and verifies continuity by reading the status through the socket controller's status registers. There are four bits used to control the BVD1 and BVD2 outputs. BVD1_EN# and BVD2_EN# must be set to 0 to enable the BVD1 and BVD2 tri-state outputs. The BVD1_OUT and BVD2_OUT bits control the state of the corresponding outputs.

3.12 Testing Ready and WP

The RDY/BSY/IREQ# and WP/IOIS16# signal are outputs from the PCCtest card. They are implemented as parallel port bits in the CNTL register (offset 4 bits 1 and 0). The host software writes various patterns to these bits and verifies continuity by reading the status through the socket controller's status registers.

3.13 Testing Card Interrupts

1. De-assert IREQ# by clearing RDY/BSY/IREQ# bit in MISC register (offset 4 bit 1).
2. Configure interrupt routing in host socket controller for desired interrupt.
3. Insert interrupt handler for desired interrupt.
4. Assert interrupt by setting RDY/BSY/IREQ# bit in MISC register (offset 4 bit 1).
5. Interrupt Service routine clears RDY/BSY/IREQ# bit to disable interrupt.
6. Disable interrupt routing in host socket controller.

3.14 Testing Status Change (STSCHG#) Interrupts

1. Enable the BVD1 output by clearing BVD1_EN# in the CNTL register (offset 4 bit 4).
2. De-assert STSCHG# by setting BVD1(STSCHG#) bit in CNTL register (offset 4 bit 5).
3. Configure interrupt routing in host socket controller for desired interrupt.
4. Insert interrupt handler for desired interrupt.
5. Clear BVD1(STSCHG#) bit in CNTL register (offset 4 bit 5).
6. Interrupt Service routine sets BVD1(STSCHG#) bit to disable interrupt.
7. Disable interrupt routing in host socket controller.

3.15 Testing Voltage Sense (VS1# and VS2#)

The PCCtest model 172 support testing of the VS1# and VS2# signals. On card initialization, VS1# and VS2# are both set inactive (high). VS1# and VS2# can be independently forced active (low) through the TCR register at offset 2. VS1# can be forced active (low) by setting STP[2:0] equal to 101. VS2# can be forced active (low) by setting STR[2:0]

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to 101. The test software is required to verify the state of VS1# and VS2# through the host controller's status registers.

3.16 Speaker (SPKR#) Testing

The PC Card's digital audio output (SPKR#) can be tested by enabling the host socket controller's speaker out signal. The host test software can then toggle the BVD2_OUT bit (offset 4 bit 7) at an audible frequency to verify the signal path between the PCCtest and the systems audio subsystem. In addition, the BVD2_EN# control (offset 4, bit 6) must be low to enable the SPKR# output. The test software is responsible for enabling the host socket controller's speaker output pin and any other hardware required to enable the speaker drivers.

3.17 Identifying the PCCtest

Test software can identify that a PCCtest unit has been inserted by reading the Card Information Structure (CIS). The CIS contains an ID string identifying the PCCtest along with the version of PCCtest hardware. Appendix B contains a listing of the PCCtest CIS.

3.18 Measuring Vcc, Vpp1 and Vpp2.

The PCCtest 172 unit contains an on-board 8-bit A/D converter. An input analog multiplexer selects which voltage is to be measured. Figure 3.18-1 details the A/D converter subsystem.

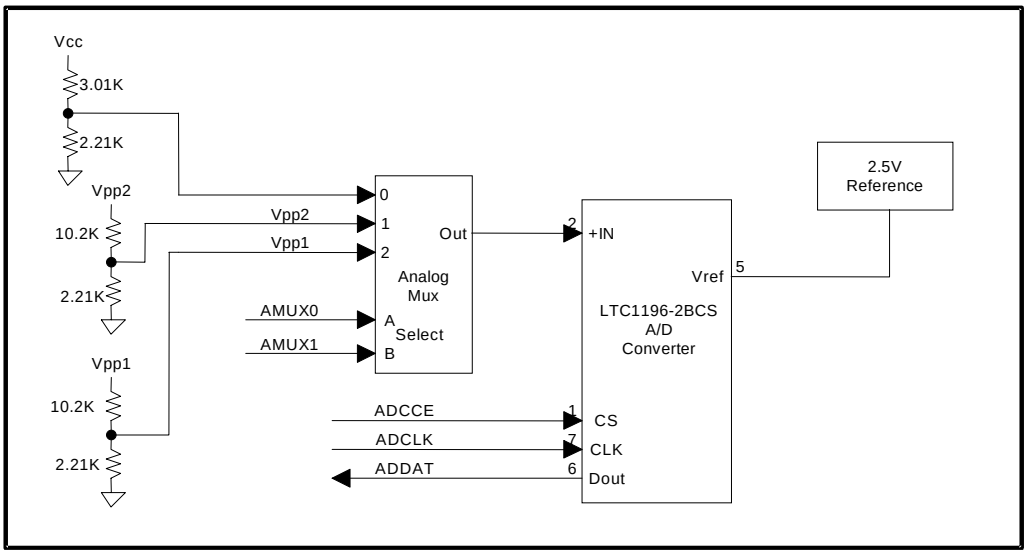


Figure 3.18-1 - PCCtest 172 A/D Subsystem

The A/D converter I/O pins are controlled via internal register bits. The following control bits are tied to the A/D converter:

Register Location	Register Bit	Description
MISC.7	ADCLK	Controls the A/D clock signal
MISC.6	ADCCE	Controls the A/D chip enable signal
LATMISC.1	ADDAT	A/D data output
MISC.5	AMUX0	Analog Mux control bit 0
CNTL.2	AMUX1	Analog Mux control bit 1

Table 3.18-1 A/D Control Bits

A four input analog multiplexer selects which voltage is to be measured:

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A/D Input Select	AMUX1	AMUX0
Vcc	0	0
Vpp2	0	1
Vpp1	1	0

Table 3.18-2 A/D Mux Control

The A/D converter is implemented using the Linear Technology LTC1196. The programming interface to the A/D converter is contained in the LTC1196 data sheet. A copy of the LTC1196 datasheet is contained in Appendix C.

3.19 PCCtest 172 versions

There are currently two versions of the PCCtest 170 in circulation. The following table describes the differences between the two:

PCCtest 170	Description
1.01	First release of the PCCtest 172.
1.02	Second release of the PCCtest 172. CISTPL_CONFIG added to CIS

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Appendix A - Register Description

This section describes the configuration of the PCCtest registers on initial power up. All PCCtest registers are written via attribute, memory or I/O write commands depending on the setting of the MODE register. There are eight writable 8-bit registers within the PCCtest unit. A[2:0] will select which register is written by the write strobe. The following table describes at which offset the PCCtest registers are located in each PCCtest mode.

Mode	Space	Register Offset
0	Attribute	100H
1	I/O	0
2	I/O	1F0H
3	I/O	170H
4	Attribute	100H
4	Common	0
5	Common	0
5	I/O	0

0 - DATALO - Low Data Byte to PC card bus

Any memory write (WE#) qualified with a valid CE1# and A[0:2] = 000 will cause the DATALO register to be updated with contents of the PC card data bus (D[7:0]). In addition an I/O write qualified with CE1# and A[0:2] = 000 will also cause a write to this register

Any memory read qualified with a valid CE1# will cause the value of the DATALO register to gated onto the PC card data bus (D[7:0]). An I/O read qualified with CE1# and A[0:2] = 000 will gate the contents of DATALO onto the PC Card data bus.

1 - DATAHI - High Data Byte to PC card bus

Any memory write memory qualified with a valid CE2# will cause the DATAHI register to be updated with contents of the PC card data bus (D[15:7]).

> ***Note**: An 8 bit I/O write to the DATAHI register is not possible.*

A memory read qualified with a valid CE2# will cause the value of the DATAHI register to be gated onto the PC card data bus (D[15:8). An 8 bit I/O read qualified by CE1# and A[0:2] = 001 will gate the contents of DATAHI onto the PC Card data bus D[7:0].

2 - LADRHI – Address latch for A[23:16] (read)

A read of this register returns the value of the specified latched address bits. Address is latched after the address latch circuitry is armed through the ADLAT bit located in the CNTL control register at offset 4.

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2 - TCR - Timer control register (write)

The TCR is a write-only register that controls the operation of the strobe measurement circuitry. STR[2:0] selects the strobe that will cause the measurement to start. STRPOL selects which edge of the signal will start the timer. STP[2:0] selects the strobe that will stop the timer. STPPOL selects which edge terminates the timer.

Bit	Name	Description			
D[2:0]	STR[2:0]	Start Pulse select			
		STR2	STR1	STR0	Signal
		0	0	0	OE#
		0	0	1	WE#
		0	1	0	CE1#
		0	1	1	CE2#
		1	0	0	Not Used
		1	0	1	Force VS2# Low
		1	1	0	IORD#
		1	1	1	IOWR#
D3	STRPOL	Start polarity 0 - Start timer on positive edge 1 - Start timer on negative edge			
D[6:4]	STP[2:0]	End Pulse Select			
		STP2	STP1	STP0	Signal
		0	0	0	OE#
		0	0	1	WE#
		0	1	0	CE1#
		0	1	1	CE2#
		1	0	0	Not Used
		1	0	1	Force VS1# Low
		1	1	0	IORD#
		1	1	1	IOWR#
D7	STPPOL	Stop polarity 0 - Stop timer on positive edge 1 - Stop timer on negative edge			

Table A-1: Register Offset 2H TCR - Timer Control Register

3 - LATMISC – Misc Latched Bits (read)

The LATMISC register contains various realtime and latched status signals from the PC Card interface.

Bit	Name	Description
D0	LA24	Latched Address 24
D1	ADC Data	A/D Data
D2	BVD1_RB	BVD1 Readback
D3	BVD2_RB	BVD2 Readback
D4	RESET	Unlatched Reset status
D5	LREG#	Latched REG# Signal
D6	WP/IOIS16#	WP/IOIS16# Readback
D7	LA25	Latched Address 25

Table A-2: - LATMISC Register – Misc Latched Bits (Offset 3)

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3 - MISC - Control Register (write)

The MISC Control register is a read/write register that contains various control bits for the PCCtest unit.

Bit	Name	Description			
D[0:2]	WAIT[0:2]	Wait State Select – control the number of wait states that are inserted for any I/O or memory access. The wait state generator must be enabled through bit 3 of this register.			
		WAIT2	WAIT1	WAIT0	Wait States
		0	0	0	No wait states
		0	0	1	50ns wait
		0	1	0	100ns wait
		0	1	1	200ns wait
		1	0	0	400ns wait
		1	0	1	800ns wait
		1	1	0	1600ns wait
		1	1	1	3200ns wait
D3	ENWAIT	Enable Wait State Generator			
D4	CIS Enable	0 = CIS ROM Enabled (Default) 1 = CIS ROM Disabled			
D5	AMUX0	A/D Mux Control bit 0			
D6	ADCCE	A/D Converter Chip Enable			
D7	ADCLK	A/D Converter Clock			

Table A-3: MISC Register - Misc control bits (offset 3)

4 - LADRLO – Address latch for A[7:0] (read)

A read of this register returns the value of the specified latched address bits. Address are latched after the address latch circuitry is armed through the ADLAT bit located in the CNTL control register at offset 4.

4 - CNTL – Control Register (write)

CNTL is a write only register.

Bit	Name	Description
D0	WP/IOIS16#	WP/IOIS16# Output
D1	RDY/BSY/IREQ#	RDY/BSY and IREQ# output (inverted)
D2	ALAT AMUX1	Address Latch Enable A/D Mux control bit 1
D3	INPKEN	INPACK# Enable
D4	BVD1_EN# CLR_RST	0 = Enable BVD1/STSCHG# output 1 = Tri-state BVD1/STSCHG# output 1 = Clear LRESET bit in STBLAT.7. 0 = Arm reset latch
D5	BVD1_OUT	0 = Force BVD1/STSCHG# output low 1 = Force BVD1/STSCHG# output high
D6	BVD2_EN#	0 = Enable BVD2/SPKR# output 1 = Tri-state BVD2/SPKR# output
D7	BVD2_OUT	0 = Force BVD2/SPKR# output low 1 = Force BVD2/SPKR# output high

Table A-4: CNTL Register - Control Signal Latch (Offset 4)

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5 - LADRMID – Address latch for A[15:8] (read)

A read of this register returns the value of the specified latched address bits. Address are latched after the address latch circuitry is armed through the ADLAT bit located in the CNTL control register (offset 4).

5 - TRST - Reset strobe to pulse counter

A write to the TRST register will arm the strobe timer circuitry. Once a write to the TRST register is complete, the counter will be armed and waiting for the selected PC card strobe.

6 - TIM[0..7] - Timer Register (read)

The Timer Register is a read-only register containing the results of the strobe timer. An 8-bit value represents the number of clocks that occurred between the selected start transition and the end transition specified in the TCR register. The actual value in nanoseconds can be calculated by multiplying the count by the sample clock period. The sample clock period for the PCCtest 172 is 50nS. The timer is armed by a write to the TRST register (offset 5).

6 - MODE – Mode Control Register (write)

The mode control register is used to enable the various PCCtest test modes. Bits in this register enable common memory and I/O modes.

Bit	**Name**	**Description**			
D[0:2]	MODE [0:2]	Mode Control			
		MODE2	MODE1	MODE0	Description
	Mode 0	0	0	0	Attribute memory enabled, I/O space and common memory not enabled
	Mode 1	0	0	1	I/O space enabled, common and attribute memory disabled
	Mode 2	0	1	0	I/O space at 1F0H-1F7H enabled, common and attribute memory disabled
	Mode 3	0	1	1	I/O space at 170H-177H enabled, common and attribute memory disabled
	Mode 4	1	0	0	Common and attribute space enabled, I/O space disabled
	Mode 5	1	0	1	Common memory space enabled, I/O space enabled, attribute memory space disabled.
D3	N.A.	Not Used			
D4	N.A.	Not Used			
D5	N.A.	Not Used			
D6	N.A.	Not Used			
D7	N.A.	Not Used			

Table A-5: MODE Register - Mode Control Register (Offset 6)

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7 - STBLAT – Latched Control Bits (read)

The STBLAT register is a read only register that contains the latched status of various control signals on the PC Card interface. All latched signal, except LRESET, are latched using the same mechanism at the address latch.

Bit	Name	Description
D0	LOE#	Latched OE#
D1	LWE#	Latched WE#
D2	LCE1#	Latched CE1#
D3	LCE2#	Latched CE2#
D4	LIORD#	Latched IORD#
D5	LIOWR#	Latched IOWR#
D6	N.A.	Not Used
D7	LRESET	Latched RESET status. Cleared by setting bit 4 in the CNTL register

Table A-6: STBLAT Register - Latched Status Bits (read)

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Appendix B – PCCtest 172 Rev 1.01 CIS

This section describes the Card Information Structure (CIS) stored in the attribute memory space of the PCCtest 172.

Addr	Byte	Description
00H	01H	CISTPL_DEVICE
02H	03H	Tuple link
04H	D1H	Device Info Field 1 - Function Specific Memory type 16K buffer @250nS
06H	0AH	2 units of 8K = 16K
08H	0FFH	End of tuple
0AH	15H	CISTPL_VERS_1
0CH	30H	Tuple link
0EH	05H	TPLLV1_MAJOR
10H	00H	TPLLV1_MINOR
12H	53H	'S'
14H	79H	'y'
16H	63H	'c'
18H	61H	'a'
1AH	72H	'r'
1CH	64H	'd'
1EH	20H	' '
20H	54H	'T'
22H	65H	‘e'
24H	63H	'c'
26H	68H	'h'
28H	6EH	'n'
2AH	6FH	'o'
2CH	6CH	'l'
2EH	6FH	'o'
30H	67H	'g'
32H	79H	'y'
34H	00H	00H
36H	50H	'P'
38H	43H	'C'
3AH	43H	'C'
3CH	74H	't'
3EH	65H	'e'
40H	73H	's'
42H	74H	't'
44H	00H	00H
46H	4DH	'M'
48H	6FH	'o'
4AH	64H	'd'
4CH	65H	'e'
4EH	6CH	'l'
50H	20H	' '
52H	31H	'1'
54H	37H	'7'
56H	32H	'2'
58H	00H	

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Addr	Byte	Description
5AH	52H	'R'
5CH	65H	'e'
5EH	76H	'v'
60H	20H	' '
62H	31H	'1'
64H	2EH	'.'
66H	30H	'0'
68H	31H	'1'
6AH	00H	
6CH	0FFH	
6EH	20H	CISTPL_MFG_ID
70H	04H	Tuple Link
72H	16H	Manufacturer ID - LSB
74H	02H	Manufacturer ID - MSB
76H	72H	Product Number - LSB
78H	01H	Product Number - MSB
7AH	21H	CISTPL_FUNC_ID
7CH	02H	Tuple Link
7EH	FEH	
80H	00H	
82H	14H	CISTPL_NO_LINK
84H	00H	
86H	0FFH	CISTPL_END - That’s all folks

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Appendix B.1 – PCCtest 172 Rev 1.02 CIS

This section describes the Card Information Structure (CIS) stored in the attribute memory space of the PCCtest 172 Rev 1.02.

Addr	Byte	Description
00H	01H	CISTPL_DEVICE
02H	03H	Tuple link
04H	D1H	Device Info Field 1 - Function Specific Memory type 16K buffer @250nS
06H	0AH	2 units of 8K = 16K
08H	0FFH	End of tuple
0AH	15H	CISTPL_VERS_1
0CH	30H	Tuple link
0EH	05H	TPLLV1_MAJOR
10H	00H	TPLLV1_MINOR
12H	53H	'S'
14H	79H	'y'
16H	63H	'c'
18H	61H	'a'
1AH	72H	'r'
1CH	64H	'd'
1EH	20H	' '
20H	54H	'T'
22H	65H	‘e'
24H	63H	'c'
26H	68H	'h'
28H	6EH	'n'
2AH	6FH	'o'
2CH	6CH	'l'
2EH	6FH	'o'
30H	67H	'g'
32H	79H	'y'
34H	00H	00H
36H	50H	'P'
38H	43H	'C'
3AH	43H	'C'
3CH	74H	't'
3EH	65H	'e'
40H	73H	's'
42H	74H	't'
44H	00H	00H
46H	4DH	'M'
48H	6FH	'o'
4AH	64H	'd'
4CH	65H	'e'
4EH	6CH	'l'
50H	20H	' '
52H	31H	'1'
54H	37H	'7'
56H	32H	'2'

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Addr	Byte	Description
58H	00H	00H
5AH	52H	'R'
5CH	65H	'e'
5EH	76H	'v'
60H	20H	' '
62H	31H	'1'
64H	2EH	'.'
66H	30H	'0'
68H	32H	'2'
6AH	00H	00H
6CH	0FFH	
6EH	20H	CISTPL_MFG_ID
70H	04H	Tuple Link
72H	16H	Manufacturer ID - LSB
74H	02H	Manufacturer ID - MSB
76H	72H	Product Number - LSB
78H	01H	Product Number - MSB
7AH	21H	CISTPL_FUNC_ID
7CH	02H	Tuple Link
7EH	FEH	TPFID_FUNCTION - Vendor Specific Function
80H	00H	
82H	1AH	CISTPL_CONFIG
84H	05H	Tuple Link
86H	01H	TPCC_SZ - Specify 2 byte address field
88H	01H	TPCC__LAST Index value of last table entry tuple
8AH	00H	TPCC_RADR(LSB) Config register base address (0x200)
8CH	02H	TPCC_RADR(MSB) Config register base address (0x200)
8EH	01H	TPCC_RMSK - Register Mask
90H	1BH	TPCC_CFTABLE_ENTRY
92H	07H	TPL_LINK
94H	C1H	TPL_INDEX
96H	01H	TPCE_IF - Interface Definition Byte
98H	18H	TPCE_FS - Feature Selection Byte
9AH	63H	TPCE_IO - I/O Window 8,16 bit, 3 address lines
9CH	30H	TPCE_IR - Interrupt Request Description (Level and Mask)
9EH	FFH	TPCE_IR - Interrupt Mask 1 (All interrupts allowed)
A0H	FFH	TPCE_IR - Interrupt Mask 2 (All interrupts allowed)
A2H	14H	CISTPL_NO_LINK
A4H	00H	
A6H	0FFH	CISTPL_END - That’s all folks

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Appendix C – Linear Technology LTC-1196 A/D Converter

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8-Bit, SO-8, 1MSPS ADCs with Auto-Shutdown Options

FEATURES

- **High Sampling Rates: 1MHz (LTC1196)**
  750kHz (LTC1198)
- **Low Cost**
- **SO-8 Plastic Package**
- Single Supply 3V and 5V Specifications
- Low Power: 10mW at 3V Supply
  50mW at 5V Supply
- Auto-Shutdown: 1nA Typical (LTC1198)
- ±1/2LSB Total Unadjusted Error over Temperature
- 3-Wire Serial I/O
- 1V to 5V Input Span Range (LTC1196)
- Converts 1MHz Inputs to 7 Effective Bits
- Differential Inputs (LTC1196)
- 2-Channel MUX (LTC1198)

APPLICATIONS

- High Speed Data Acquisition
- Disk Drives
- Portable or Compact Instrumentation
- Low Power or Battery-Operated Systems

DESCRIPTION

The LTC1196/LTC1198 are 600ns, 8-bit A/D converters with sampling rates up to 1MHz. They are offered in 8-pin SO packages and operate on 3V to 6V supplies. Power dissipation is only 10mW with a 3V supply or 50mW with a 5V supply. The LTC1198 automatically powers down to a typical supply current of 1nA whenever it is not performing conversions. These 8-bit switched-capacitor successive approximation ADCs include sample-and-holds. The LTC1196 has a differential analog input; the LTC1198 offers a software selectable 2-channel MUX.

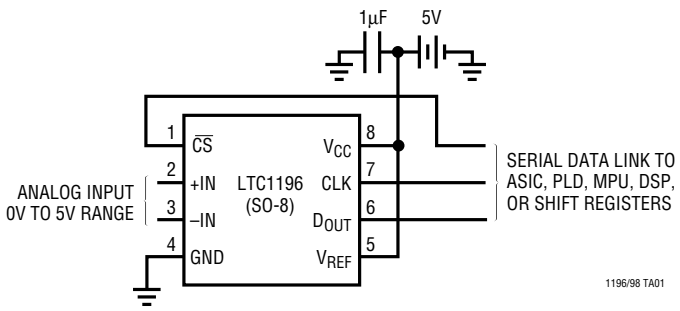
The 3-wire serial I/O, SO-8 packages, 3V operation and extremely high sample rate-to-power ratio make these ADCs an ideal choice for compact, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans below 1V full scale (LTC1196) allow direct connection to signal sources in many applications, eliminating the need for gain stages.

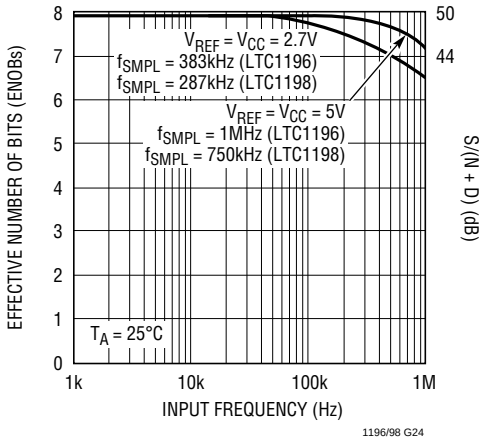
The A grade devices are specified with total unadjusted error of ±1/2LSB maximum over temperature.

TYPICAL APPLICATION

Single 5V Supply, 1MSPS, 8-Bit Sampling ADC



Effective Bits and S/(N + D) vs Input Frequency



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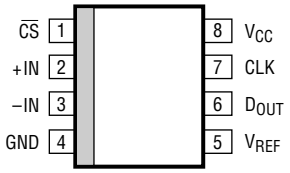
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) to GND 7V
Voltage
  Analog Reference ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 7V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW

Operating Temperature Range
  LTC1196-1AC, LTC1198-1AC, LTC1196-1BC, LTC1198-1BC, LTC1196-2AC, LTC1198-2AC, LTC1196-2BC, LTC1198-2BC ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

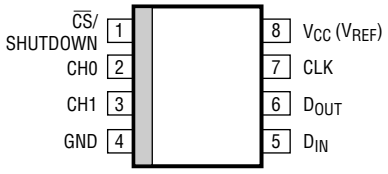


S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER*
LTC1196-1ACS8 LTC1196-1BCS8 LTC1196-2ACS8 LTC1196-2BCS8
S8 PART MARKING
1961A 1961B 1962A 1962B

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER*
LTC1198-1ACS8 LTC1198-1BCS8 LTC1198-2ACS8 LTC1198-2BCS8
S8 PART MARKING
1981A 1981B 1982A 1982B

*Parts available in N8 package. Consult factory for N8 samples.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7		6	2.7		6	V
V_{CC} = 5V Operation										
f_{CLK}	Clock Frequency		 ●	0.01 0.01		14.4 12.0	0.01 0.01		12.0 9.6	MHz MHz
t_{CYC}	Total Cycle Time	LTC1196 LTC1198		12 16			12 16			CLK CLK
t_{SMPL}	Analog Input Sampling Time			2.5			2.5			CLK
$t_{h\overline{CS}}$	Hold Time $\overline{CS}$ Low After Last CLK↑			10			13			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1, 2)			20			26			ns
t_{hDI}	Hold Time D_{IN} After CLK↑	LTC1198		20			26			ns

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	LTC1198		20			26			ns
t_{WHCLK}	CLK High Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
t_{WLCLK}	CLK Low Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles			25			32			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1196 LTC1198		11 15			11 15			CLK CLK

CONVERTER AND MULTIPLEXER CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, $f_{CLK} = f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1196-XA LTC1198-XA MIN	TYP	MAX	LTC1196-XB LTC1198-XB MIN	TYP	MAX	UNITS
No Missing Codes Resolution		●	8			8			Bits
Offset Error		●			±1/2			±1	LSB
Linearity Error	(Note 3)	●			±1/2			±1	LSB
Full-Scale Error		●			±1/2			±1	LSB
Total Unadjusted Error (Note 4)	LTC1196, V_{REF} = 5.000V LTC1198, V_{CC} = 5.000V	●			±1/2			±1	LSB
Analog and REF Input Range	LTC1196			−0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Note 5)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA V_{CC} = 4.75V, I_O = 360µA	● ●	4.5 2.4	4.74 4.71		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			45		mA
I_{REF}	Reference Current, LTC1196	$\overline{CS} = V_{CC}$ $f_{SMPL} = f_{SMPL(MAX)}$	● ●		0.001 0.5	3 1	µA mA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$, LTC1198 (Shutdown) $\overline{CS} = V_{CC}$, LTC1196 $f_{SMPL} = f_{SMPL(MAX)}$, LTC1196/LTC1198	● ● ●		0.001 7 11	3 15 20	µA mA mA

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DYNAMIC ACCURACY

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196 MIN	LTC1196 TYP	LTC1196 MAX	LTC1198 MIN	LTC1198 TYP	LTC1198 MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion	500kHz/1MHz Input Signal			47/45			47/45		dB
THD	Total Harmonic Distortion	500kHz/1MHz Input Signal			49/47			49/47		dB
	Peak Harmonic or Spurious Noise	500kHz/1MHz Input Signal			55/48			55/48		dB
IMD	Intermodulation Distortion	f_{IN1} = 499.37kHz, f_{IN2} = 502.446kHz			51			51		dB
	Full Power Bandwidth				8			8		MHz
	Full Linear Bandwidth [S/(N + D) > 44dB]				1			1		MHz

AC CHARACTERISTICS

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
t_{CONV}	Conversion Time (See Figures 1, 2)					600			710	ns
			●			710			900	ns
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1196		1.20			1.00			MHz
		LTC1196	●	1.00			0.80			MHz
		LTC1198		0.90			0.75			MHz
		LTC1198	●	0.75			0.60			MHz
t_{dDO}	Delay Time, CLK↑ to D_{OUT} Data Valid	C_{LOAD} = 20pF			55	64		68	78	ns
			●			73			94	ns
t_{DIS}	Delay Time $\overline{CS}$↑ to D_{OUT} Hi-Z		●		70	120		88	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 20pF	●		30	50		43	63	ns
t_{hDO}	Time Output Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	30	45		30	55		ns
t_r	D_{OUT} Fall Time	C_{LOAD} = 20pF	●		5	15		10	20	ns
t_f	D_{OUT} Rise Time	C_{LOAD} = 20pF	●		5	15		10	20	ns
C_{IN}	Input Capacitance	Analog Input On Channel			30			30		pF
		Analog Input Off Channel			5			5		pF
		Digital Input			5			5		pF

RECOMMENDED OPERATING CONDITIONS

V_{CC} = 2.7V Operation

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
f_{CLK}	Clock Frequency			0.01		5.4	0.01		4	MHz
			●	0.01		4.6	0.01		3	MHz
t_{CYC}	Total Cycle Time	LTC1196		12			12			CLK
		LTC1198		16			16			CLK
t_{SMPL}	Analog Input Sampling Time			2.5			2.5			CLK
$t_{h\overline{CS}}$	Hold Time $\overline{CS}$ Low After Last CLK↑			20			40			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1, 2)			40			78			ns

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RECOMMENDED OPERATING CONDITIONS

V_{CC} = 2.7V Operation

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
t_{hDI}	Hold Time D_{IN} After CLK↑	LTC1198		40			78			ns
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	LTC1198		40			78			ns
t_{WHCLK}	CLK High Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
t_{WLCLK}	CLK Low Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles			50			96			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1196 LTC1198		11 15			11 15			CLK CLK

CONVERTER AND MULTIPLEXER CHARACTERISTICS

V_{CC} = 2.7V, V_{REF} = 2.5V, $f_{CLK} = f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1196-XA LTC1198-XA MIN	TYP	MAX	LTC1196-XB LTC1198-XB MIN	TYP	MAX	UNITS
No Missing Codes Resolution		●	8			8			Bits
Offset Error		●			±1/2			±1	LSB
Linearity Error	(Note 3)	●			±1/2			±1	LSB
Full-Scale Error		●			±1/2			±1	LSB
Total Unadjusted Error (Note 4)	LTC1196, V_{REF} = 2.500V LTC1198, V_{CC} = 2.700V	●			±1/2			±1	LSB
Analog and REF Input Range	LTC1196			−0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Note 5)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.3 2.1	2.60 2.45		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			15		mA
I_{REF}	Reference Current, LTC1196	$\overline{CS} = V_{CC}$ $f_{SMPL} = f_{SMPL(MAX)}$	● ●		0.001 0.25	3.0 0.5	µA mA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$ = 3.3V, LTC1198 (Shutdown) $\overline{CS} = V_{CC}$ = 3.3V, LTC1196 $f_{SMPL} = f_{SMPL(MAX)}$, LTC1196/LTC1198	● ● ●		0.001 1.5 2.0	3.0 4.5 6.0	µA mA mA

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DYNAMIC ACCURACY

V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196 MIN	LTC1196 TYP	LTC1196 MAX	LTC1198 MIN	LTC1198 TYP	LTC1198 MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion	190kHz/380kHz Input Signal			47/45			47/45		dB
THD	Total Harmonic Distortion	190kHz/380kHz Input Signal			49/47			49/47		dB
	Peak Harmonic or Spurious Noise	190kHz/380kHz Input Signal			53/46			53/46		dB
IMD	Intermodulation Distortion	f_{IN1} = 189.37kHz, f_{IN2} = 192.446kHz			51			51		dB
	Full Power Bandwidth				5			5		MHz
	Full Linear Bandwidth [S/(N + D) > 44dB]				0.5			0.5		MHz

AC CHARACTERISTICS

V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time (See Figures 1, 2)		 ●			1.58 1.85			2.13 2.84	µs µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1196 LTC1196 LTC1198 LTC1198	 ● ●	450 383 337 287			333 250 250 187			kHz kHz kHz kHz
t_{dDO}	Delay Time, CLK↑ to D_{OUT} Data Valid	C_{LOAD} = 20pF	 ●		100	150 180		130	200 250	ns ns
t_{DIS}	Delay Time $\overline{CS}$↑ to D_{OUT} Hi-Z		●		110	220		120	250	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 20pF	●		80	130		100	200	ns
t_{hDO}	Time Output Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	45	90		45	120		ns
t_r	D_{OUT} Fall Time	C_{LOAD} = 20pF	●		10	30		15	40	ns
t_f	D_{OUT} Rise Time	C_{LOAD} = 20pF	●		10	30		15	40	ns
C_{IN}	Input Capacitance	Analog Input On Channel Analog Input Off Channel Digital Input			30 5 5			30 5 5		pF pF pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

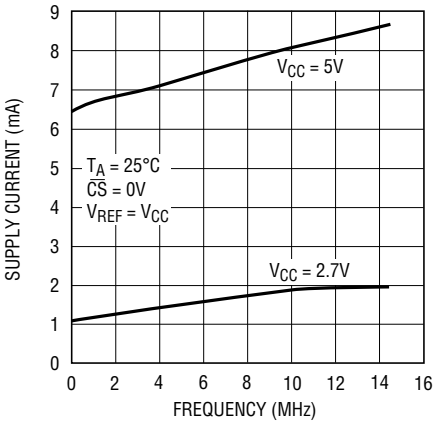
Note 4: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 5: Channel leakage current is measured after the channel selection.

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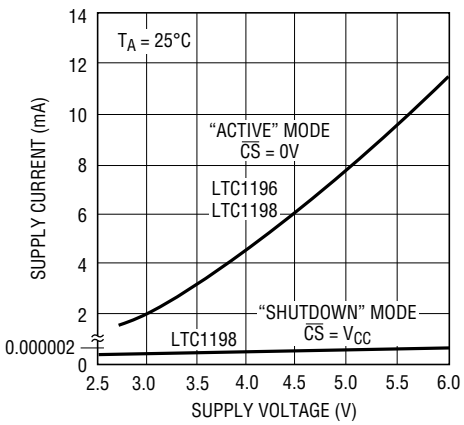
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Clock Rate



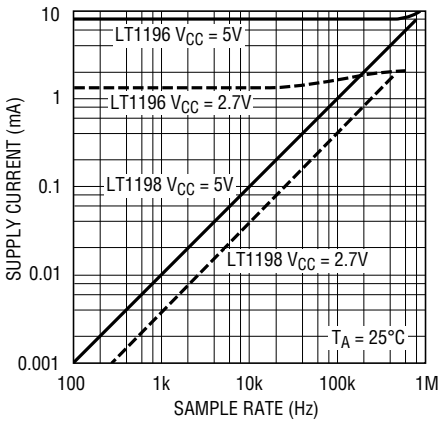
1196/98 G01

Supply Current vs Supply Voltage



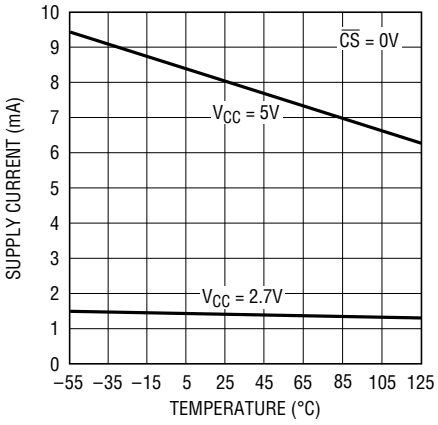
1196/98 G02

Supply Current vs Sample Rate



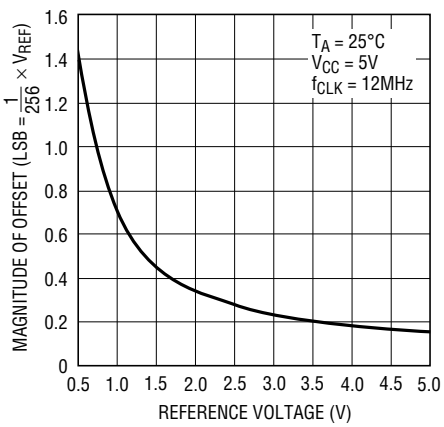
1196/98 G03

Supply Current vs Temperature



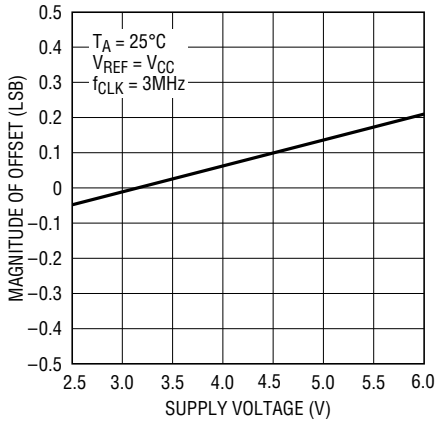
1196/98 G04

Offset vs Reference Voltage



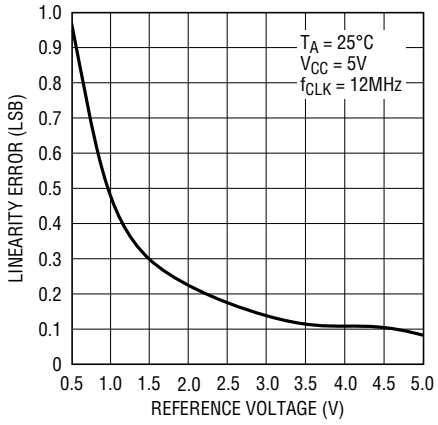
1196/98 G05

Offset vs Supply Voltage



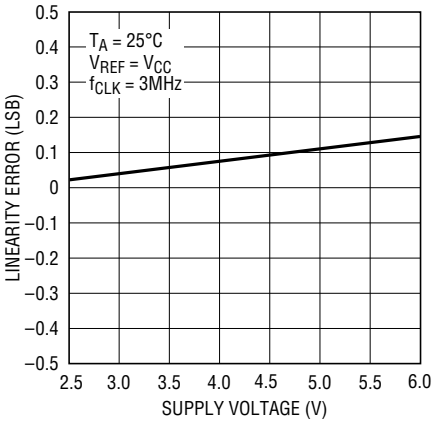
1196/98 G06

Linearity Error vs Reference Voltage



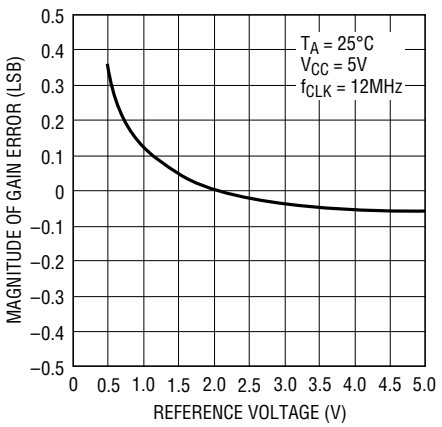
1196/98 G07

Linearity Error vs Supply Voltage



1196/98 G08

Gain Error vs Reference Voltage

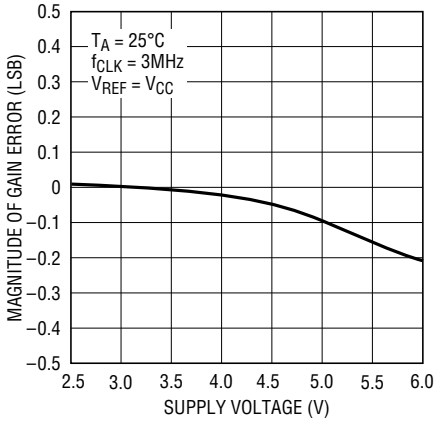


1196/98 G09

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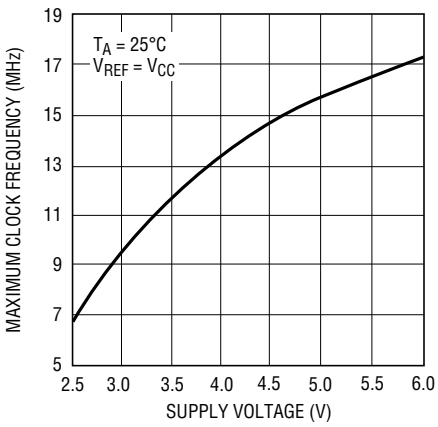
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Supply Voltage



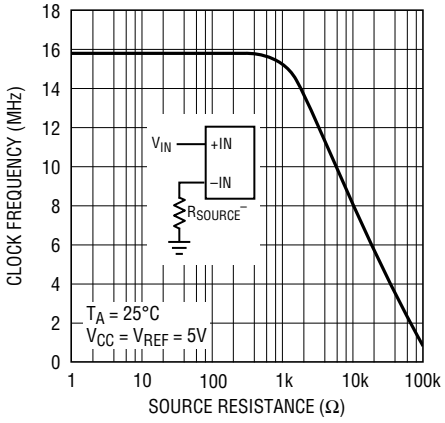
1196/98 G10

Maximum Clock Frequency vs Supply Voltage



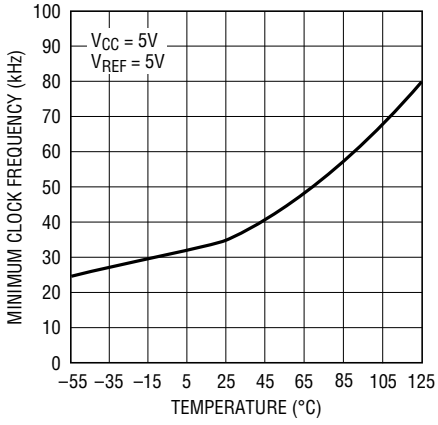
1196/98 G11

Maximum Clock Frequency vs Source Resistance



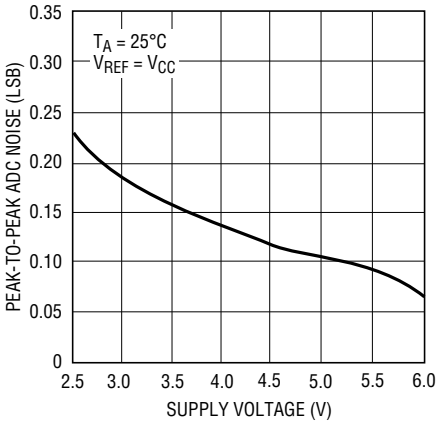
1196/98 G12

Minimum Clock Rate for 0.1LSB* Error



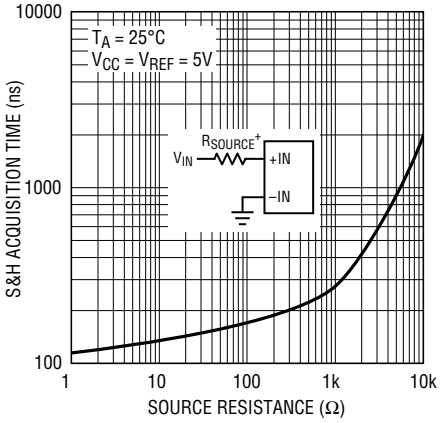
1196/98 G13

ADC Noise vs Reference and Supply Voltage



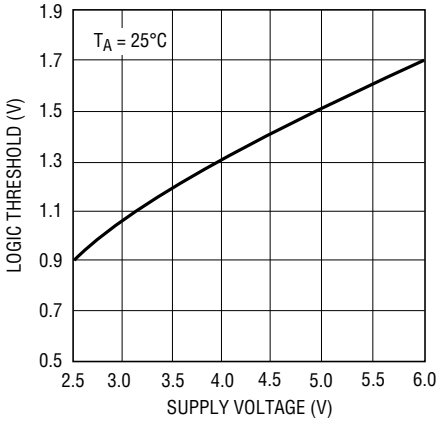
1196/98 G14

Sample-and-Hold Acquisition Time vs Source Resistance



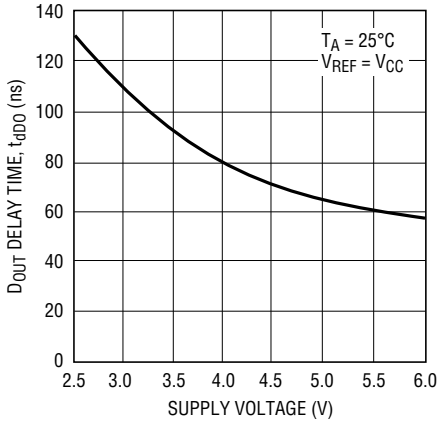
1196/98 G15

Digital Input Logic Threshold vs Supply Voltage



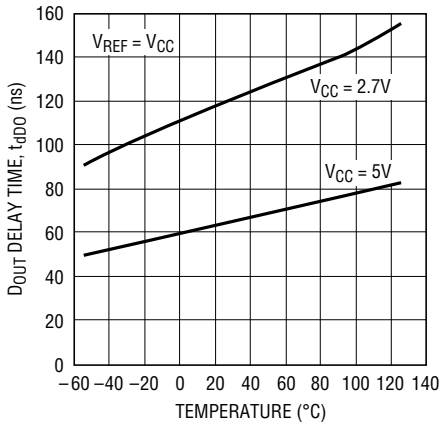
1196/98 G16

D_{OUT} Delay Time vs Supply Voltage



1196/98 G17

D_{OUT} Delay Time vs Temperature



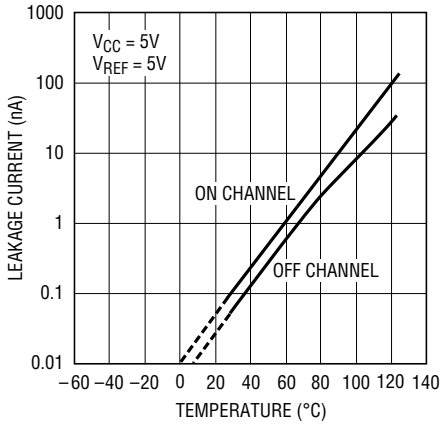
1196/98 G18

*AS THE FREQUENCY IS DECREASED FROM 12MHz, MINIMUM CLOCK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 12MHz VALUE IS FIRST DETECTED.

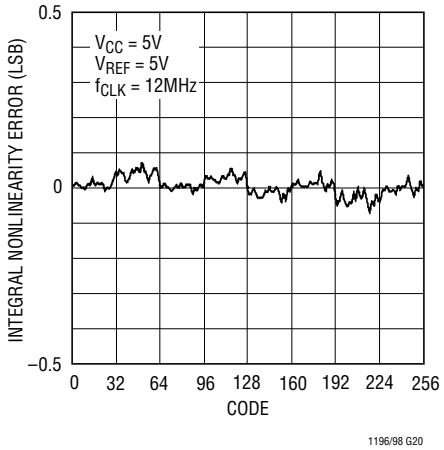
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TYPICAL PERFORMANCE CHARACTERISTICS

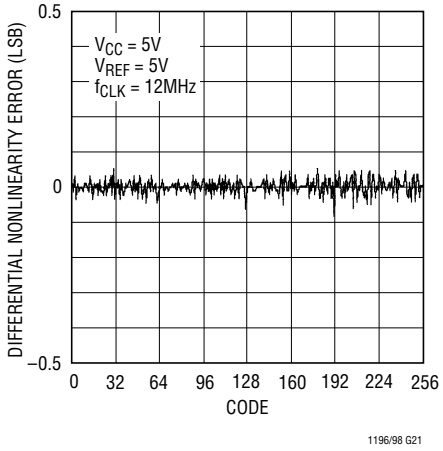
Input Channel Leakage Current vs Temperature



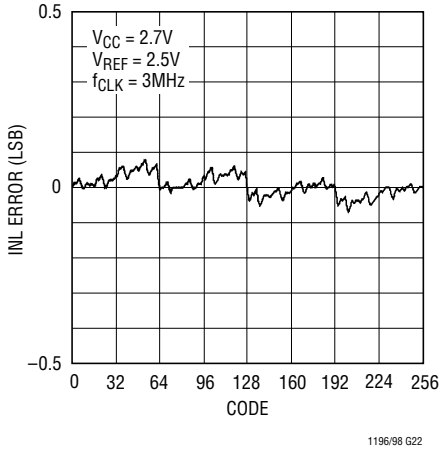
Integral Nonlinearity vs Code at 5V



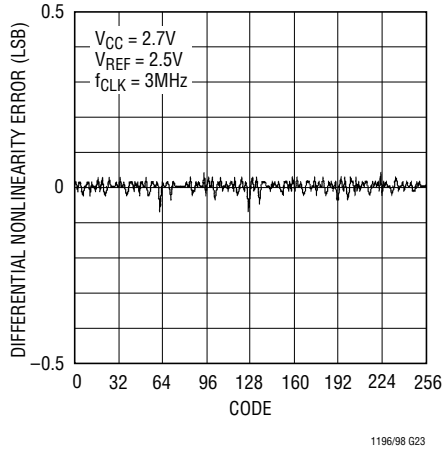
Differential Nonlinearity vs Code at 5V



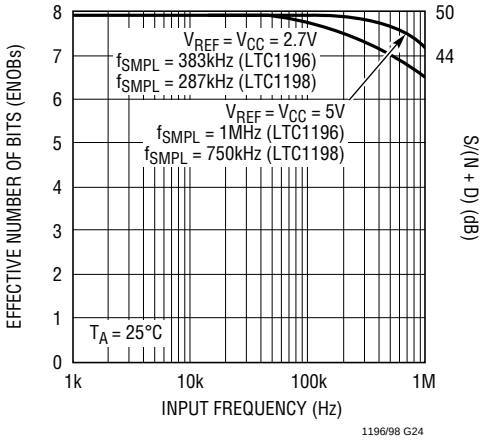
Integral Nonlinearity vs Code at 2.7V



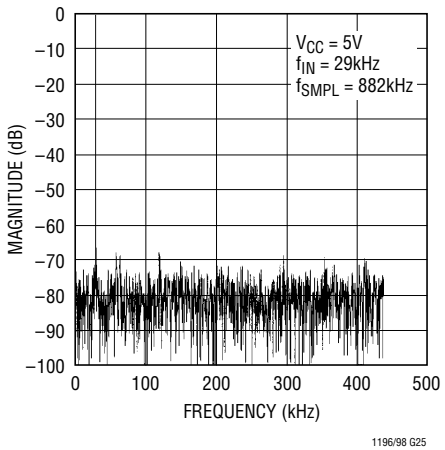
Differential Nonlinearity vs Code at 2.7V



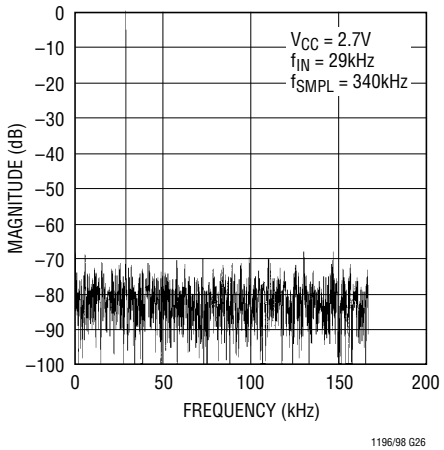
Effective Bits and S/(N + D) vs Input Frequency



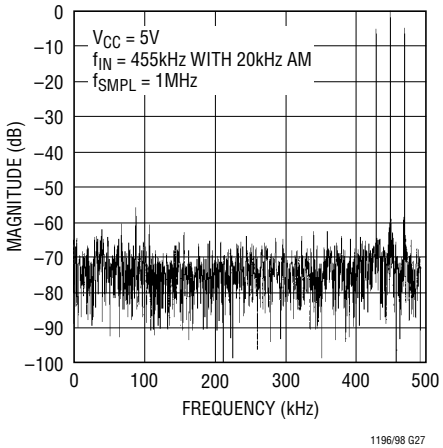
4096 Point FFT Plot at 5V



4096 Point FFT at 2.7V



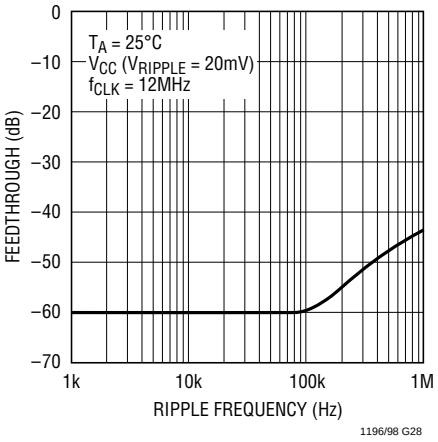
FFT Output of 455kHz AM Signal Digitized at 1MSPS



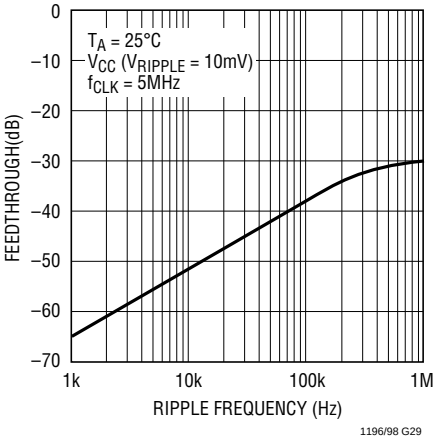
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TYPICAL PERFORMANCE CHARACTERISTICS

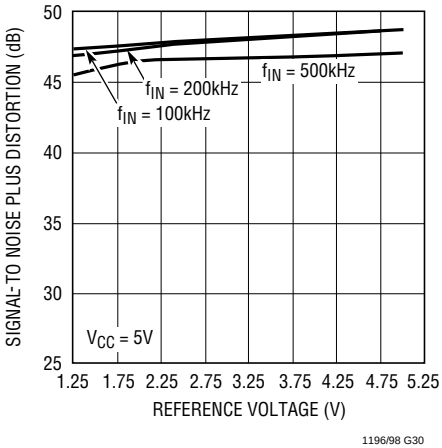
Power Supply Feedthrough vs Ripple Frequency



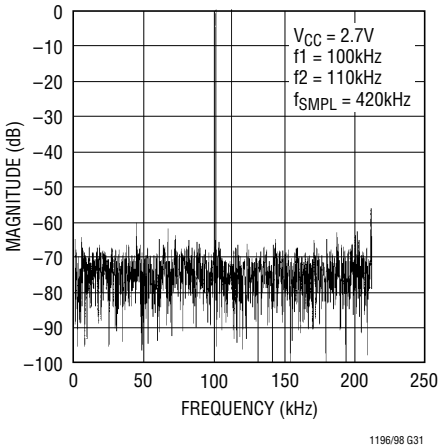
Power Supply Feedthrough vs Ripple Frequency



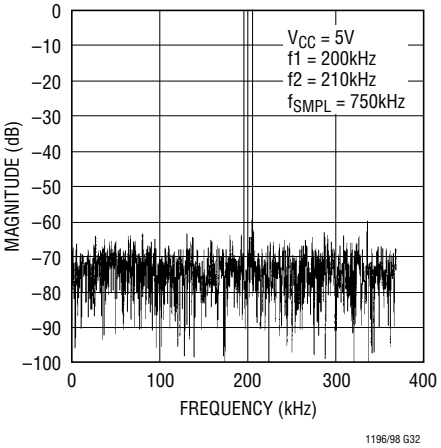
S/(N + D) vs Reference Voltage and Input Frequency



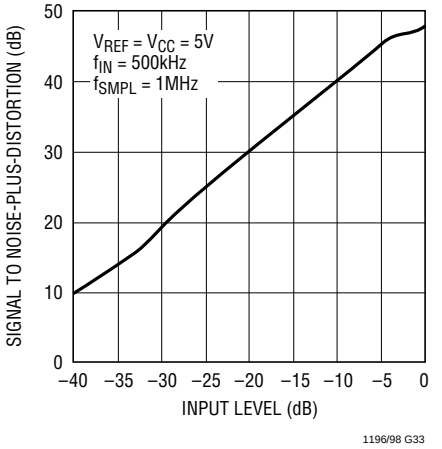
Intermodulation Distortion at 2.7V



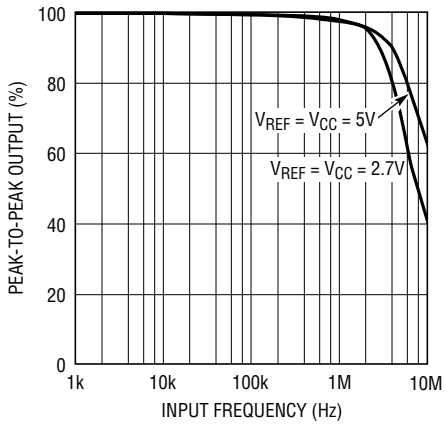
Intermodulation Distortion at 5V



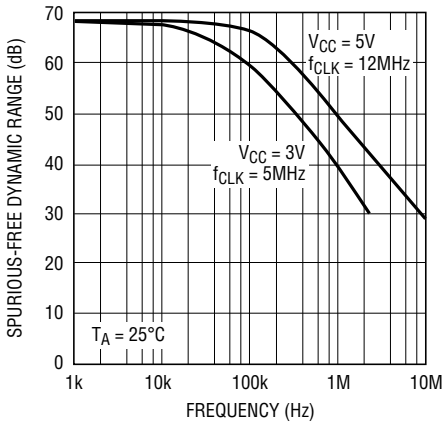
S/(N + D) vs Input Level



Output Amplitude vs Input Frequency



Spurious-Free Dynamic Range vs Frequency



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PIN FUNCTIONS

LTC1196

$\overline{CS}$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1196. A logic high on this input disables the LTC1196.

IN^+ (Pin 2): Analog Input. This input must be free of noise with respect to GND.

IN^- (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

V_{REF} (Pin 5): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1198

$\overline{CS}$/SHUTDOWN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1198. A logic high on this input disables the LTC1198 and DISCONNECTS THE POWER TO THE LTC1198.

CH0 (Pin 2): Analog Input. This input must be free of noise with respect to GND.

CH1 (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

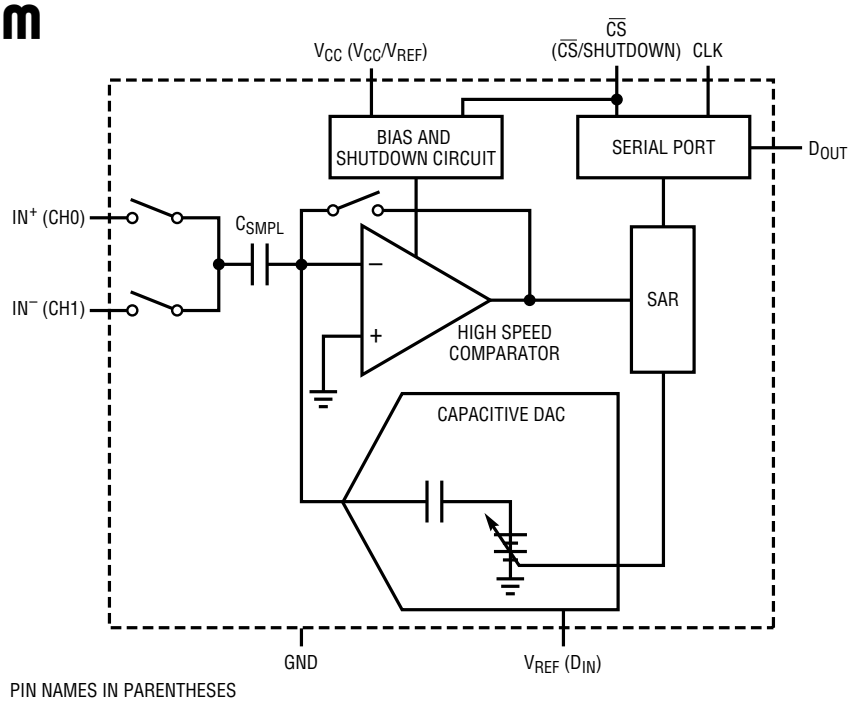
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC}(V_{REF})(Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

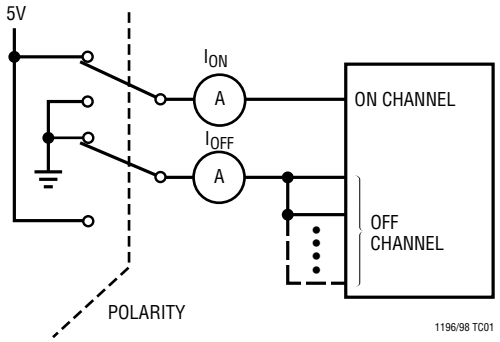
BLOCK DIAGRAM



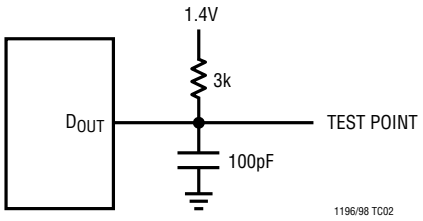
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TEST CIRCUITS

On and Off Channel Leakage Current



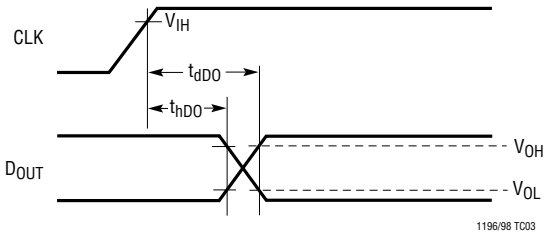
Load Circuit for t_{dDO}, t_r and t_f



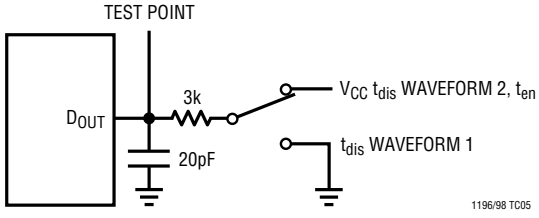
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



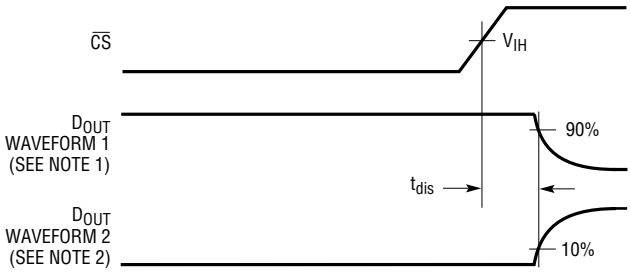
Voltage Waveform for D_{OUT} Delay Time, t_{dDO} and t_{hDO}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

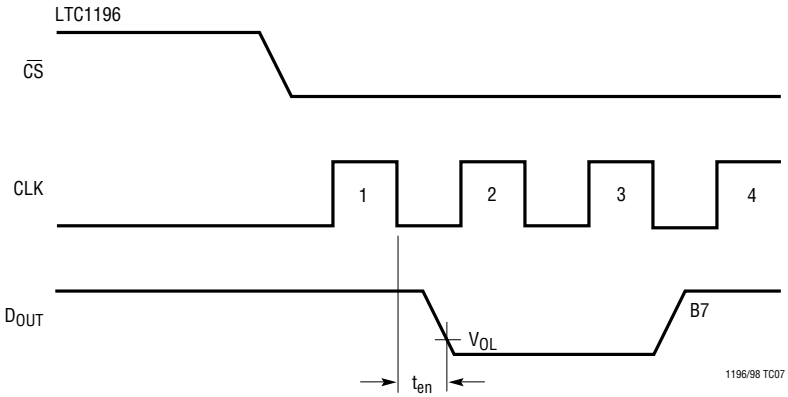
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

1196/98 TC06

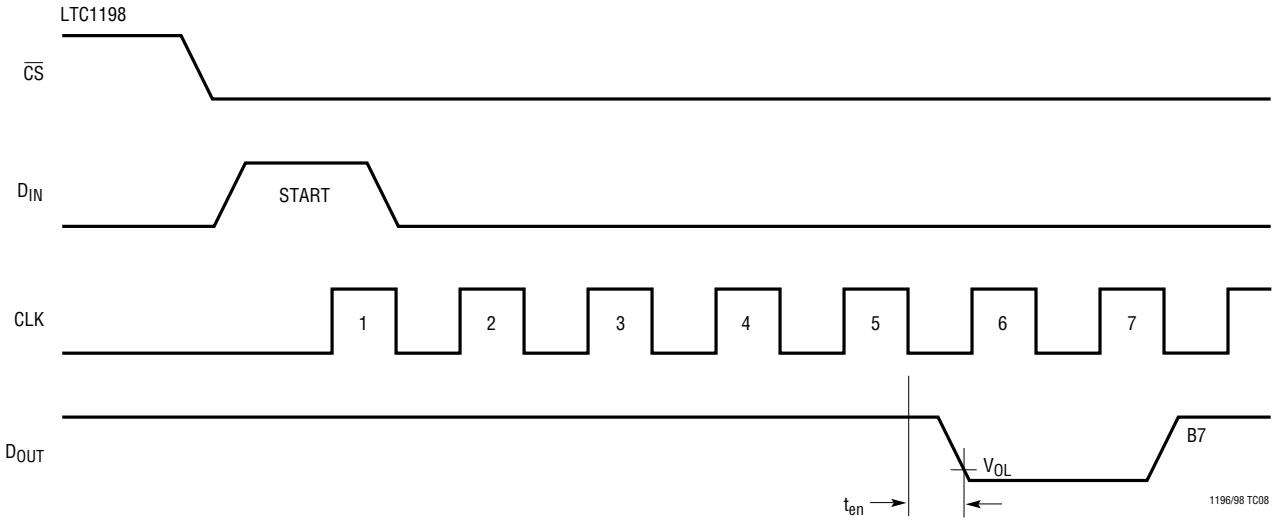
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TEST CIRCUITS

Voltage Waveforms for t_{en}



Voltage Waveforms for t_{en}



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APPLICATIONS INFORMATION

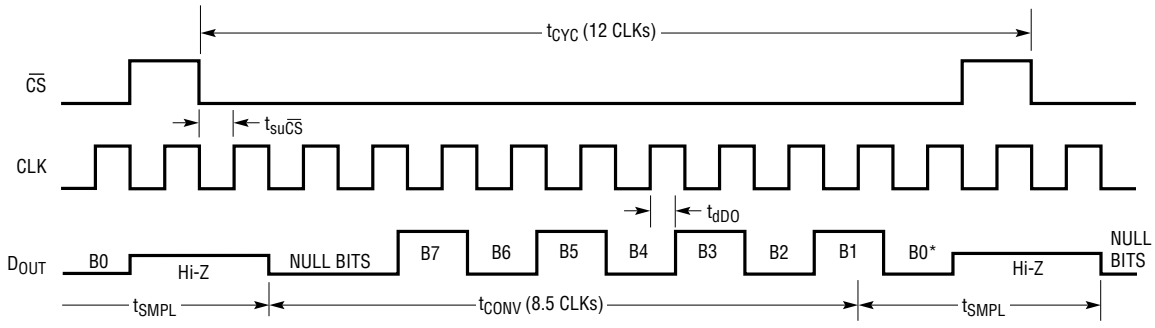
OVERVIEW

The LTC1196/LTC1198 are 600ns sampling 8-bit A/D converters packaged in tiny 8-pin SO packages and operating on 3V to 6V supplies. The ADCs draw only 10mW from a 3V supply or 50mW from a 5V supply.

Both the LTC1196 and the LTC1198 contain an 8-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). The on-chip sample-and-holds have full-accuracy input bandwidths of 1MHz. Although they share the same basic design, the LTC1196 and LTC1198 differ in some respects. The LTC1196 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans below 1V. The LTC1198 has a 2-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. It also automatically powers down when not performing conversion, drawing only leakage current.

SERIAL INTERFACE

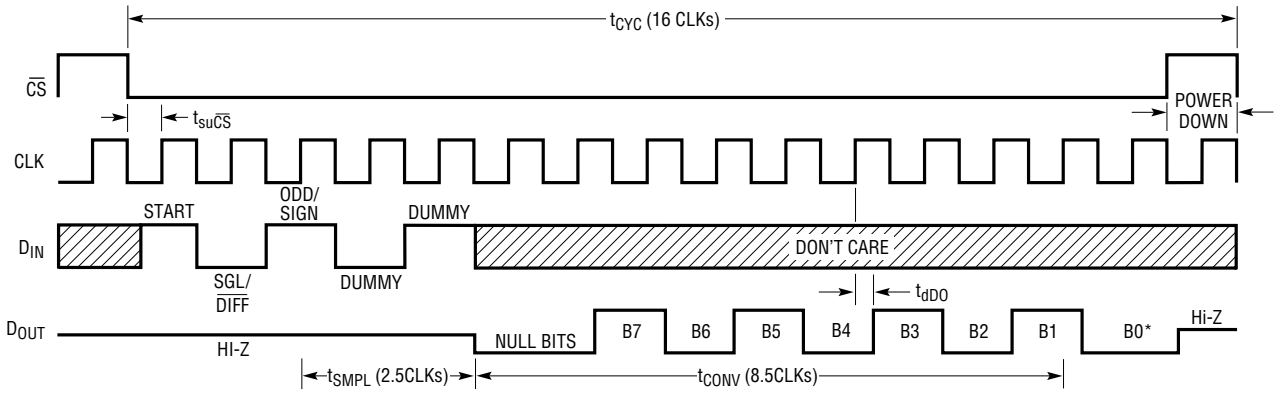
The LTC1196/LTC1198 will interface via three or four wires to ASICs, PLDs, microprocessors, DSPs, or shift registers (see Operating Sequence in Figures 1 and 2). To run at their fastest conversion rates (600ns), they must be clocked at 14.4MHz. HC logic families and any high speed ASIC or PLD will easily interface to the ADCs at that speed (see Data Transfer and Typical Application sections). Full speed operation from a 3V supply can still be achieved with 3V ASICs, PLDs or HC logic circuits.



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

1196/98 F01

Figure 1. LTC1196 Operating Sequence



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

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Figure 2. LTC1198 Operating Sequence Example: Differential Inputs (CH1, CH0)

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Connection to a microprocessor or a DSP serial port is quite simple (see Data Transfer section). It requires no additional hardware, but the speed will be limited by the clock rate of the microprocessor or the DSP which limits the conversion time of the LTC1196/LTC1198.

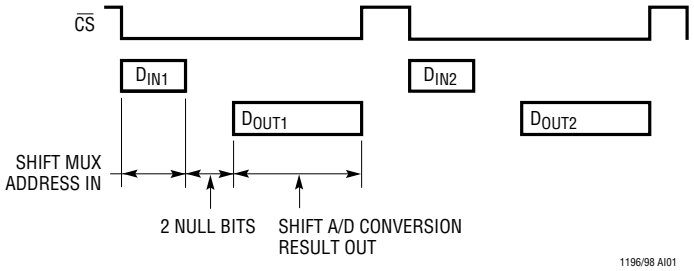
Data Transfer

Data transfer differs slightly between the LTC1196 and the LTC1198. The LTC1196 interfaces over 3 lines: $\overline{CS}$, CLK and D_{OUT}. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1196 Operating Sequence. After $\overline{CS}$ falls, the first CLK pulse enables D_{OUT}. After two null bits, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1196 for the next data exchange.

The LTC1198 can transfer data with 3 or 4 wires. The additional input, D_{IN}, is used to select the 2-channel MUX configuration.

The data transfer between the LTC1198 and the digital systems can be broken into two sections: Input Data Word and A/D Conversion Result. First, each bit of the input data word is captured on the rising CLK edge by the LTC1198. Second, each bit of the A/D conversion result on the D_{OUT} line is updated on the rising CLK edge by the LTC1198. This bit should be captured on the next rising CLK edge by the digital systems (see A/D Conversion Result section).

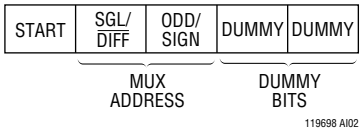
Data transfer is initiated by a falling chip select ($\overline{CS}$) signal as shown in the LTC1198 Operating Sequence. After $\overline{CS}$ falls the LTC1198 looks for a start bit. After the start bit is received, the 4-bit input word is shifted into the D_{IN} input. The first two bits of the input word configure the LTC1198. The last two bits of the input word allow the ADC to acquire the input voltage by 2.5 clocks before the conversion starts. After the conversion starts, two null bits and the conversion result are output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1198 in preparation for the next data exchange.



Input Data Word

The LTC1196 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result is output on the D_{OUT} line in an MSB-first sequence, followed by zeros indefinitely if clocks are continuously applied with $\overline{CS}$ low.

The LTC1198 clocks data into the D_{IN} input on the rising edge of the clock. The input data word is defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1198 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The 2 bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND.

LTC1198 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

1196/98 AI03

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Dummy Bits

The last 2 bits of the input word following the MUX Address are dummy bits. Either bit can be a "logical one" or a "logical zero." These 2 bits allow the ADC 2.5 clocks to acquire the input signal after the channel selection.

A/D Conversion Result

Both the LTC1196 and the LTC1198 have the A/D conversion result appear on the D_{OUT} line after two null bits (see Operating Sequence in Figures 1 and 2). Data on the D_{OUT} line is updated on the rising edge of the CLK line. The D_{OUT} data should also be captured on the rising CLK edge by the digital systems. Data on the D_{OUT} line remains valid for a minimum time of t_{hDO} (30ns at 5V) to allow the capture to occur (see Figure 3).

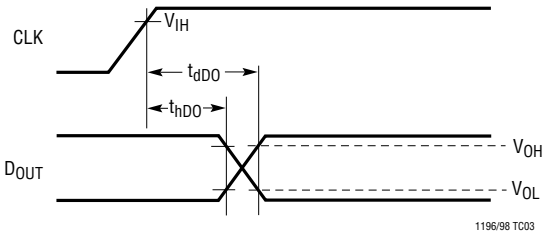
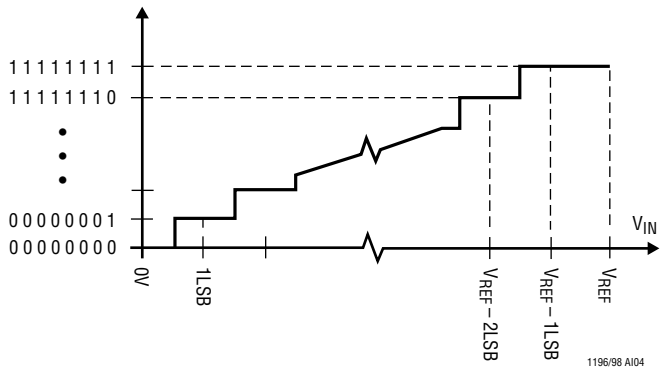


Figure 3. Voltage Waveform for D_{OUT} Delay Time, t_{dDO} and t_{hDO}

Unipolar Transfer Curve

The LTC1196/LTC1198 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

Unipolar Transfer Curve



Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
11111111	V_{REF} – 1LSB	4.9805V
11111110	V_{REF} – 2LSB	4.9609V
•	•	•
•	•	•
•	•	•
00000001	1LSB	0.0195V
00000000	0V	0V

1196/98 AI05

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1198 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the digital systems. Data is transmitted in both directions on a single wire. The pin of the digital systems connected to this data line should be configurable as either an input or an output. The LTC1198 will take control of the data line and drive it low on the 5th falling CLK edge after the start bit is received (see Figure 4). Therefore the port line of the digital systems must be switched to an input before this happens to avoid a conflict.

REDUCING POWER CONSUMPTION

The LTC1196/LTC1198 can sample at up to a 1MHz rate, drawing only 50mW from a 5V supply. Power consumption can be reduced in two ways. Using a 3V supply lowers the power consumption on both devices by a factor of five, to 10mW. The LTC1198 can reduce power even further because it shuts down whenever it is not converting. Figure 5 shows the supply current versus sample rate for the LTC1196 and LTC1198 on 3V and 5V. To achieve such a low power consumption, especially for the LTC1198, several things must be taken into consideration.

Shutdown (LTC1198)

Figure 2 shows the operating sequence of the LTC1198. The converter draws power when the $\overline{CS}$ pin is low and powers itself down when that pin is high. For lowest power consumption in shutdown, the $\overline{CS}$ pin should be driven with CMOS levels (0V to V_{CC}) so that the $\overline{CS}$ input buffer of the converter will not draw current.

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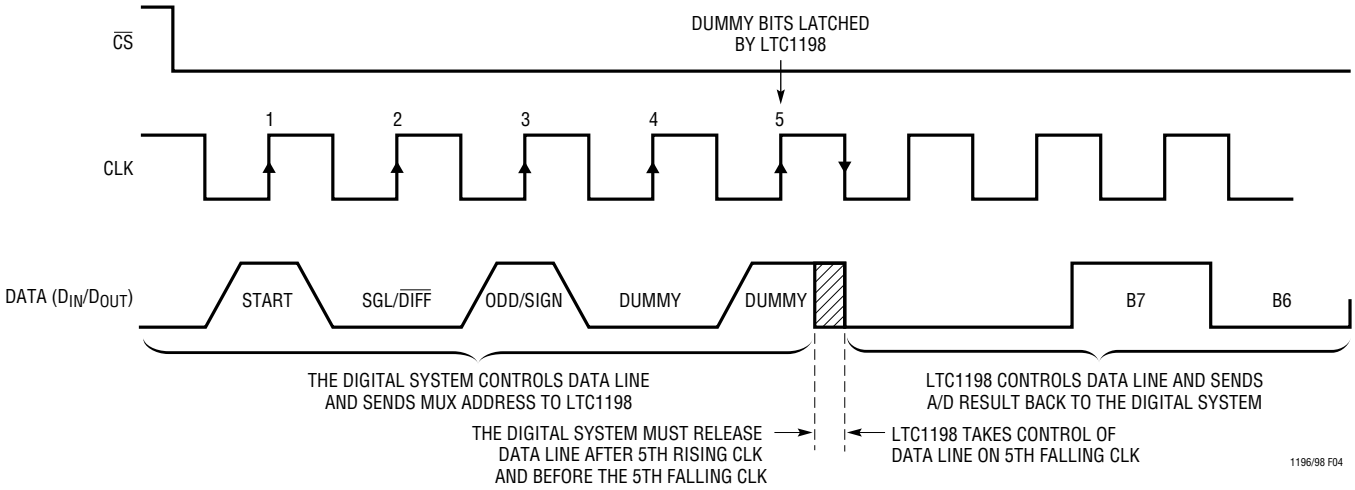


Figure 4. LTC1198 Operation with D_{IN} and D_{OUT} Tied Together

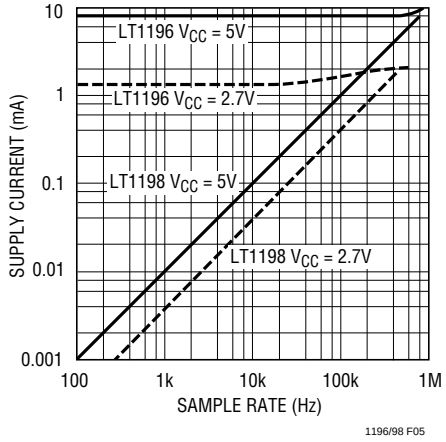


Figure 5. Supply Current vs Sample Rate for LTC1196/ LTC1198 Operating on 5V and 2.7V Supplies

When the $\overline{CS}$ pin is high (= supply voltage), the LTC1198 is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input has no effect on the supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high; they can continue to run without drawing current.

Minimize $\overline{CS}$ Low Time (LTC1198)

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transfering data as quickly as possible, then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power.

OPERATING ON OTHER THAN 5V SUPPLIES

The LTC1196/LTC1198 operate from single 2.7V to 6V supplies. To operate the LTC1196/LTC1198 on other than 5V supplies, a few things must be kept in mind.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on 5V supply. When the supply voltage varies, the input logic levels also change (see typical curve of Digital Input Logic Threshold vs Supply Voltage). For these two ADCs to sample and convert correctly, the digital inputs have to be in the logical low and high relative to the operating supply voltage. If achieving micropower consumption is desirable on the LTC1198, the digital inputs must go rail-to-rail between supply voltage and ground (see Reducing Power Consumption section).

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Clock Frequency

The maximum recommended clock frequency is 14.4MHz at 25°C for the LTC1196/LTC1198 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the supply is reduced, the clock rate must be reduced also. At 3V the devices are specified with a 5.4MHz clock at 25°C.

Mixed Supplies

It is possible to have a digital system running off a 5V supply and communicate with the LTC1196/LTC1198 operating on a 3V supply. Achieving this reduces the outputs of D_{OUT} from the ADCs to toggle the equivalent input of the digital system. The $\overline{CS}$, CLK and D_{IN} inputs of the ADCs will take 5V signals from the digital system without causing any problem (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1196 operating on a 3V supply, the output of D_{OUT} only goes between 0V and 3V. This signal easily meets TTL levels (see Figure 6).

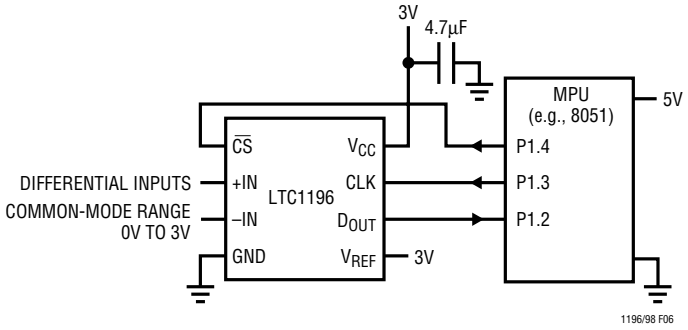


Figure 6. Interfacing a 3V Powered LTC1196 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1196/LTC1198 are easy to use if some care is taken. They should be used with an analog ground plane and single-point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 1µF tantalum with leads as short as possible. If the power supply is clean, the LTC1196/LTC1198 can also operate with smaller 0.1µF surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single-point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1196 and the LTC1198 provide a built-in sample-and-hold (S&H) function to acquire the input signal. The S&H acquires the input signal from "+" input during t_{SMPL} as shown in Figures 1 and 2. The S&H of the LTC1198 can sample input signals in either single-ended or differential mode (see Figure 7).

Single-Ended Inputs

The sample-and-hold of the LTC1198 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the first DUMMY bit is shifted in and continues until the falling CLK edge after the second DUMMY bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 8.5 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input, this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 8.5/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the

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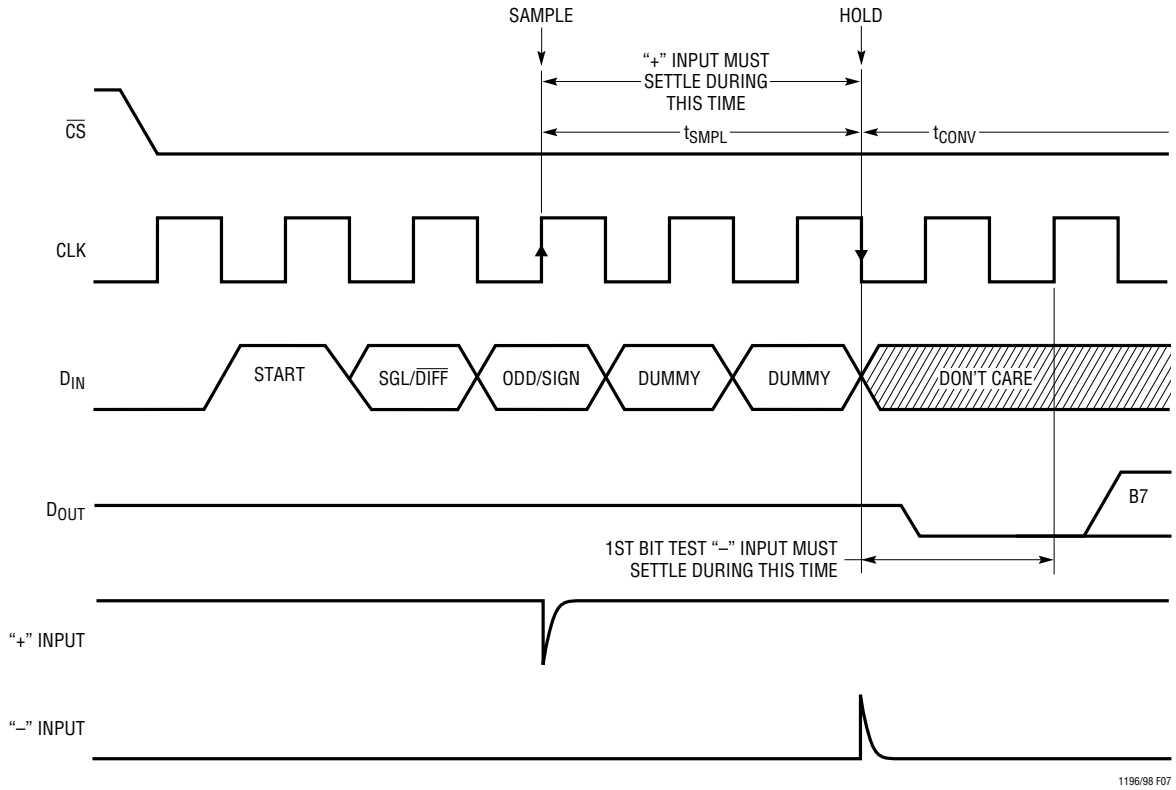


Figure 7. LTC1198 "+" and "–" Input Settling Windows

CLK. V_{ERROR} is proportional to f("–") and inversely proportional to f_{CLK}. For a 60Hz signal on the "–" input to generate a 1/4LSB error (5mV) with the converter running at CLK = 12MHz, its peak value would have to be 18.7V.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1196/LTC1198 have one capacitive switching input current spike per conversion. These current spikes settle quickly and do not cause a problem. However, if source resistances larger than 100Ω are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1196 is switched onto "+" input at the end of the conversion and samples the input signal until the conversion begins (see Figure 1). The input capacitor of the LTC1198 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 2.5 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{SMPL} for the LTC1196/LTC1198. Minimizing R_{SOURCE}^+ will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by allowing more time between conversions for the LTC1196 or by using a slower CLK frequency for the LTC1198.

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APPLICATIONS INFORMATION

"–" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figures 1 and 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps.

To achieve the full sampling rate, the analog input should be driven with a low impedance source (<100Ω) or a high speed op amp (e.g., the LT1223, LT1191, or LT1226). Higher impedance sources or slower op amps can easily be accommodated by allowing more time for the analog input to settle as described above.

Source Resistance

The analog inputs of the LTC1196/LTC1198 look like a 25pF capacitor (C_{IN}) in series with a 120Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within t_{SMPL}.

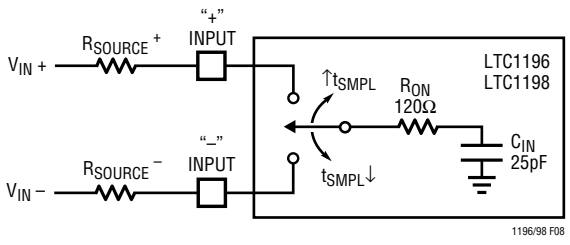


Figure 8. Analog Input Equivalent Circuit

REFERENCE INPUT

The voltage on the reference input of the LTC1196 defines the voltage span of the A/D converter. The reference input has transient capacitive switching currents which are due to the switched-capacitor conversion technique (see Figure 9). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the ADC. These high frequency current spikes will settle quickly and do not cause a problem if the reference input is bypassed with at least a 0.1µF capacitor.

The reference input can be driven with standard voltage references. Bypassing the reference with a 0.1µF capacitor is recommended to keep the high frequency impedance low as described above. Some references require a small resistor in series with the bypass capacitor for frequency stability. See the individual reference data sheet for details.

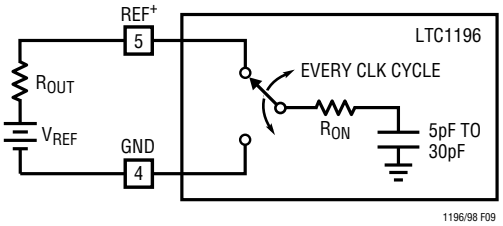


Figure 9. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1198 is limited to 2.7V because the V_{CC} supply and reference are internally tied together. However, the LTC1196 can operate with reference voltages below 1V.

The effective resolution of the LTC1196 can be increased by reducing the input span of the converter. The LTC1196 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full-Scale Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise

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Offset with Reduced V_{REF}

The offset of the LTC1196 has a larger effect on the output code when the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 2mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSB with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1196.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1196 can be reduced to approximately $2mV_{P-P}$ using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 2mV noise is only 0.1LSB peak-to-peak. In this case, the LTC1196 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 2mV noise is 0.5LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 200mV, the 2mV noise becomes equal to 2.5LSB and a stable code is difficult to achieve. In this case averaging readings is necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

DYNAMIC PERFORMANCE

The LTC1196/LTC1198 have exceptionally high speed sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using a FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 10 shows a typical LTC1196 FFT plot.

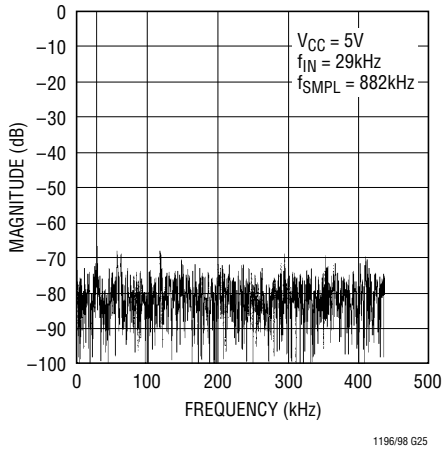


Figure 10. LTC1196 Non-Averaged, 4096 Point FFT Plot

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 10 shows a typical spectral content with a 882kHz sampling rate.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling

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APPLICATIONS INFORMATION

rate of 1.2MHz with a 5V supply the LTC1196 maintains above 7.5 ENOBs at 400kHz input frequency. Above 500kHz the ENOBs gradually decline, as shown in Figure 11, due to increasing second harmonic distortion. The noise floor remains low.

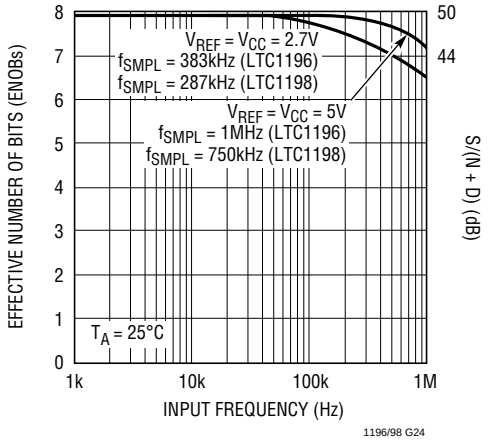


Figure 11. Effective Bits and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the N^{th} harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 100kHz input signal, the LTC1196/LTC1198 have typical THD of 50dB and 49dB with V_{CC} = 5V and V_{CC} = 3V, respectively.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a \pm f_b\right) = 20\log\left[\frac{\text{amplitude}\left(f_a \pm f_b\right)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 499kHz and 502kHz, the IMD of the LTC1196/LTC1198 is 51dB with a 5V supply.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the effective bits rating of the ADC falls to 7 bits. Beyond this frequency, distortion of the sampled input signal increases. The LTC1196/LTC1198 have been designed to optimize input bandwidth, allowing the ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency.

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APPLICATIONS INFORMATION

3V VERSUS 5V PERFORMANCE COMPARISON

Table 1 shows the performance comparison between 3V and 5V supplies. The power dissipation drops by a factor of five when the supply is reduced to 3V. The converter slows down somewhat but still gives excellent performance on a 3V rail. With a 3V supply, the LTC1196 converts in 1.6µs, samples at 450kHz, and provides a 500kHz linear-input bandwidth.

Dynamic accuracy is excellent on both 5V and 3V. The ADCs typically provide 49.3dB of 7.9 ENOBs of dynamic accuracy at both 3V and 5V. The noise floor is extremely low, corresponding to a transition noise of less than 0.1LSB. DC accuracy includes ±0.5LSB total unadjusted error at 5V. At 3V, linearity error is ±0.5LSB while total unadjusted error increases to ±1LSB.

Table 1. 5V/3V Performance Comparison

LTC1196-1	**5V**	**3V**
P_{DISS}	50mW	10mW
Max f_{SMPL}	1MHz	383kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 at 300kHz	7.9 at 100kHz
Linear Input Bandwidth (ENOBs > 7)	1MHz	500kHz
LTC1198-1		
P_{DISS}	50mW	10mW
P_{DISS} (Shutdown)	15µW	9µW
Max f_{SMPL}	750kHz	287kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 at 300kHz	7.9 at 100kHz
Linear Input Bandwidth (ENOBs > 7)	1MHz	500kHz

TYPICAL APPLICATIONS

PLD Interface Using the Altera EPM5064

The Altera EPM5064 has been chosen to demonstrate the interface between the LTC1196 and a PLD. The EPM5064 is programmed to be a 12-bit counter and an equivalent 74HC595 8-bit shift register as shown in Figure 12. The circuit works as follows: bringing ENA high makes the $\overline{CS}$ output high and the EN input low to reset the LTC1196 and disable the shift register. Bringing ENA low, the $\overline{CS}$ output goes high for one CLK cycle with every 12 CLK cycles. The inverted signal, EN, of the $\overline{CS}$ output makes the 8-bit data available on the B0-B7] lines. Figures 13 and 14 show the interconnection between the LTC1196 and EPM5064 and the timing diagram of the signals between these two devices. The CLK frequency in this circuit can run up to $f_{CLK(MAX)}$ of the LTC1196.

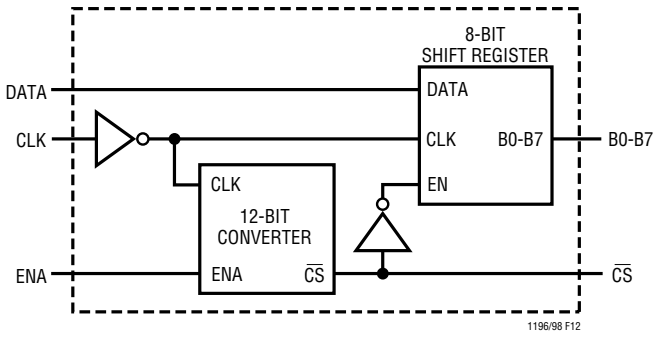


Figure 12. An Equivalent Circuit of the EPM5064

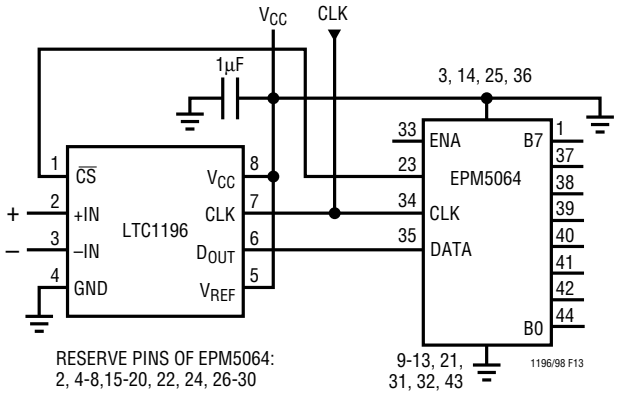


Figure 13. Intefacing the LTC1196 to the Altera EPM5064 PLD

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TYPICAL APPLICATIONS

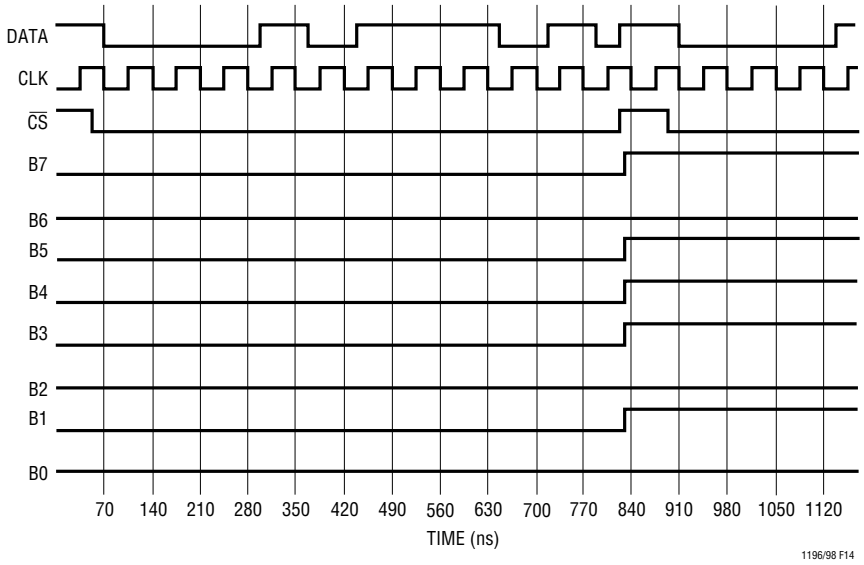


Figure 14. The Timing Diagram

Interfacing the LTC1198 to the TMS320C25 DSP

Figure 15 illustrates the interface between the LTC1198 8-bit data acquisition system and the TMS320C25 digital signal processor (DSP). The interface, which is optimized for speed of transfer and minimum processor supervision, can complete a conversion and shift the data in 4µs with f_{CLK} = 5MHz. The cycle time, 4µs, of each conversion is limited by maximum clock frequency of the serial port of the TMS320C25 which is 5MHz. The supply voltage for the LTC1198 in Figure 15 can be 2.7V to 6V with f_{CLK} = 5MHz. At 2.7V, f_{CLK} = 5MHz will work at 25°C. See Recommended Operating Conditions for limits over temperature.

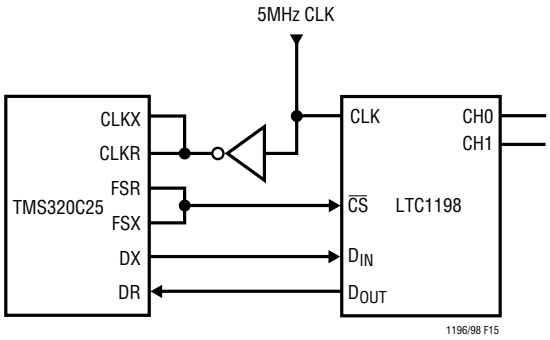


Figure 15. Interfacing the LTC1198 to the TMS320C25 DSP

Hardware Description

The circuit works as follows: the LTC1198 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a synchronous format over D_{IN} and D_{OUT}. The serial port of the TMS320C25 is compatible with that of the LTC1198. The data shift clock lines (CLKR, CLKX) are inputs only. The data shift clock comes from an external source. Inverting the shift clock is necessary because the LTC1198 and the TMS320C25 clock the input data on opposite edges.

The schematic of Figure 15 is fed by an external clock source. The signal is fed into the CLK pin of the LTC1198 directly. The signal is inverted with a 74HC04 and then applied to the data shift clock lines (CLKR, CLKX). The framing pulse of the TMS320C25 is fed directly to the $\overline{CS}$ of the LTC1198. DX and DR are tied directly to D_{IN} and D_{OUT} respectively.

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The timing diagram of Figure 16 was obtained from the circuit of Figure 15. The CLK was 5MHz for the timing diagram and the TMS320C25 clock rate was 40MHz. Figure 17 shows the timing diagram with the LTC1198 running off a 2.7V supply and 5MHz CLK.

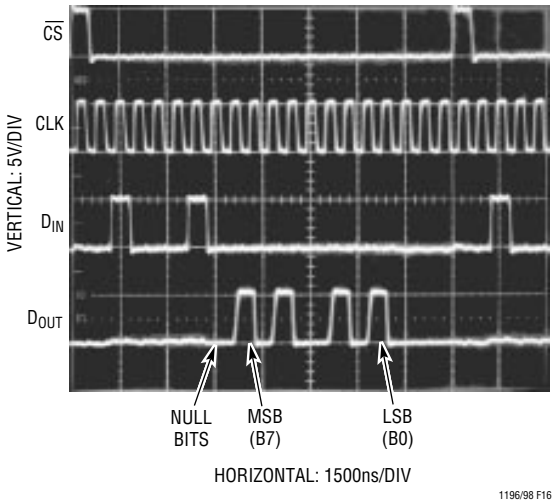


Figure 16. Scope Trace the LTC1198 Running Off 5V Supply in the Circuit of Figure 15

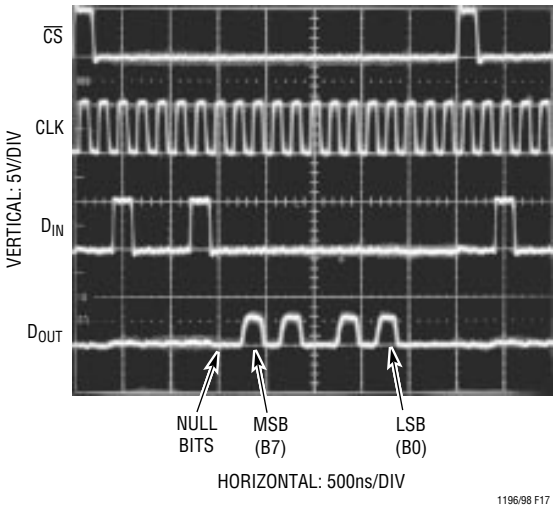


Figure 17. Scope Trace the LTC1198 Running Off 2.7V Supply in the Circuit of Figure 15

Software Description

The software configures and controls the serial port of the TMS320C25.

The code first sets up the interrupt and reset vectors. On reset the TMS320C25 starts executing code at the label INIT. Upon completion of a 16-bit data transfer, an interrupt is generated and the DSP will begin executing code at the label RINT.

In the beginning, the code initializes registers in the TMS320C25 that will be used in the transfer routine. The interrupts are temporarily disabled. The data memory page pointer register is set to zero. The auxiliary register pointer is loaded with one and auxiliary register one is loaded with the value 200 hexadecimal. This is the data memory location where the data from the LTC1198 will be stored. The interrupt mask register (IMR) is configured to recognize the RINT interrupt, which is generated after receiving the last of 16 bits on the serial port. This interrupt is still disabled at this time. The transmit framing synchronization pin (FSX) is configured to be an output. The F0 bit of the status register ST1, is initialized to zero which sets up the serial port to operate in the 16-bit mode.

Next, the code in TXRX routine starts to transmit and receive data. The D_{IN} word is loaded into the ACC and shifted left eight times so that it appears as in Figure 18. This D_{IN} word configures the LTC1198 for CH0 with respect to CH1. The D_{IN} word is then put in the transmit register and the RINT interrupt is enabled. The NOP is repeated 3 times to mask out the interrupts and minimize the cycle time of the conversion to be 20 clock cycles. All clocking and $\overline{CS}$ functions are performed by the hardware.

B15							B8
0	1 START	0 S/$\overline{D}$	0 O/S	0 DUMMY	1 DUMMY	0	0

L1196/98 F18

Figure 18. D_{IN} Word in ACC of TMS320C25 for the Circuit in Figure 15

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TYPICAL APPLICATIONS

Once RINT is generated the code begins execution at the label RINT. This code stores the D_{OUT} word from the LTC1198 in the ACC and then stores it in location 200 hex. The data appears in location 200 hex right-justified as shown in Figure 19. The code is set up to continually loop, so at this point the code jumps to label TXRX and repeats from here.

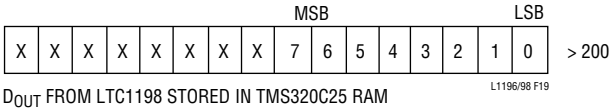


Figure 19. Memory Map for the Circuit in Figure 15

LABEL	MNEMONIC		COMMENTS
	AORG	0	ON RESET CODE EXECUTION STARTS AT 0
	B	INIT	BRANCH TO INITIALIZATION ROUTINE
	AORG	>26	ADDRESS OF RINT INTERRUPT VECTOR
	B	RINT	BRANCH TO RINT SERVICE ROUTINE
	AORG	>32	MAIN PROGRAM STARTS HERE
INIT	DINT		DISABLE INTERRUPTS
	LDPK	>0	SET DATA MEMORY PAGE POINTER TO 0
	LARP	>1	SET AUXILIARY REGISTER POINTER TO 1
	LRLK	AR1,>200	SET AUXILIARY REGISTER 1 TO >200
	LACK	>10	LOAD IMR CONFIG WORD INTO ACC
	SACL	>4	STORE IMR CONFIG WORD INTO IMR
	STXM		CONFIGURE FSX AS AN OUTPUT
	FORT	0	SET SERIAL PORT TO 16-BIT MODE
TXRX	LACK	>44	LOAD LTC1198 D_{IN} WORD INTO ACC
	SFSM		FSX PULSES GENERATED ON XSR LOAD
	RPTK	7	REPEAT NEXT INSTRUCTION 8 TIMES
	SFL		SHIFTS D_{IN} WORD TO RIGHT POSITION
	SACL	>1	PUT D_{IN} WORD IN TRANSMIT REGISTER
	EINT		ENABLE INTERRUPT (DISABLED ON RINT)
	RPTK	2	MINIMIZE THE CONVERSION CYCLE TIME
	NOP		TO BE 20 CLOCK CYCLES
RINT	ZALS	>0	STORE LTC1198 DOUT WORD IN ACC
	SACL	*, 0	STORE ACC IN LOCATION >200
	B	TXRX	BRANCH TO TRANSMIT RECEIVE ROUTINE
	END		

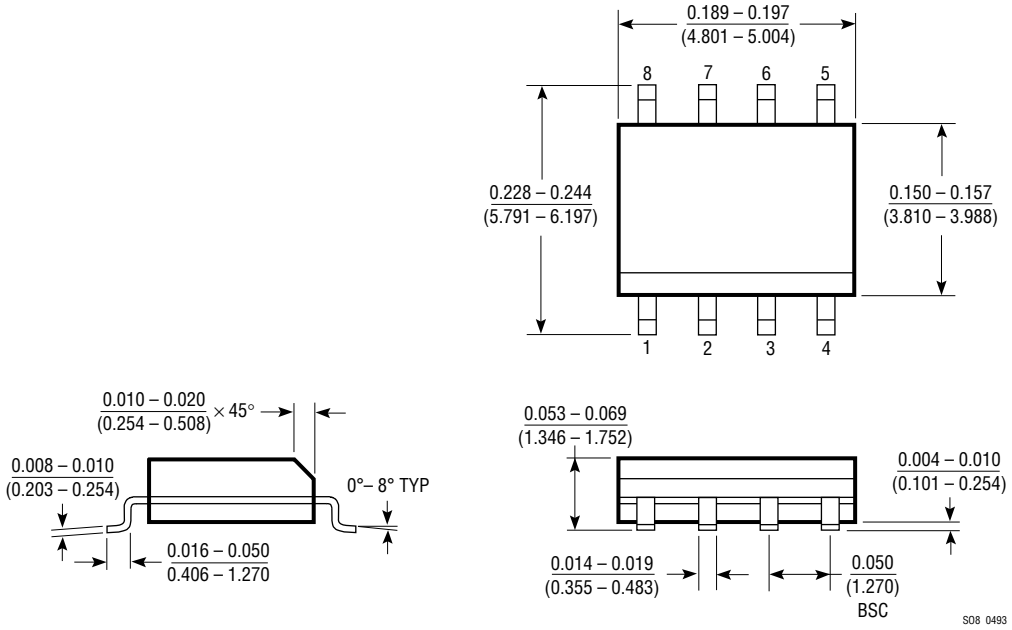
Figure 20. TMS320C25 Code for the Circuit in Figure 15

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PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic SOIC



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