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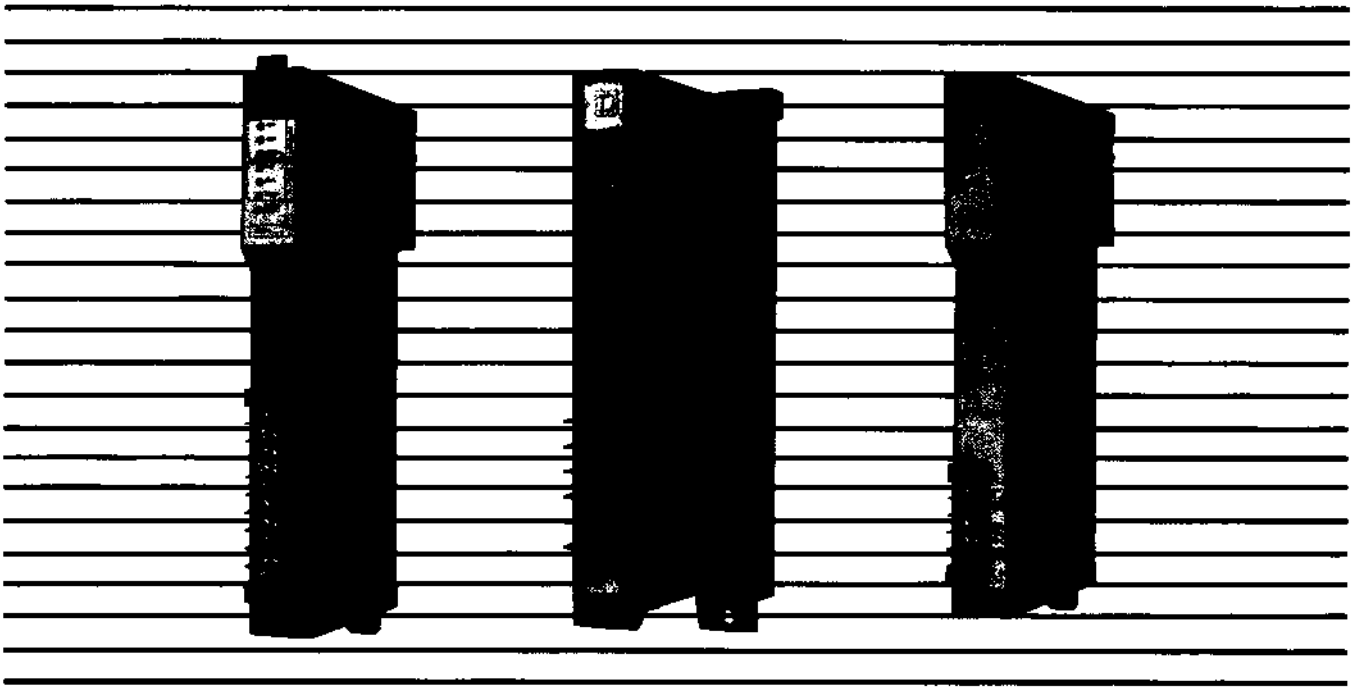
SQUARE D COMPANY

Instruction Bulletin

SY/MAX®

Local / Remote Inferface
Class 8030 Types CRM-210, 211, 220 222

Bulletin # 30598-247-01D2
October, 1990



Dedicated to Growth
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Supersedes 30598-247-D1 Dated July, 1990

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3) **Do not touch gold edge contacts.**

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1.0 INTRODUCTION

1.1 General Information

The local and remote interface (LI and RI) system for the SY/MAX programmable controller Family provides a versatile method of handling a wide variety of local and remote I/O and register module configurations. It has the interfacing capability to handle everything from the smallest single task machines to systems requiring thousands of remote I/O and register functions.

This bulletin provides the basics to configure a remote I/O system to meet a PC system design needs with a minimum of hardware, thereby reducing the total cost and time required for implementation of the control scheme.

1.2 Summary of Operation

By utilizing the SY/MAX LI and RI modules, both digital and register racks can be located remotely from a SY/MAX processor. The modules allow communication with the processor over a two pair, twisted, shielded cable, greatly reducing the cost of control wiring to the remote electrical inputs and outputs.

To establish a remote I/O system, an LI module is mounted in the rack containing the processor and an RI module is mounted in the remote rack (referred to as a drop). The dual twisted shielded pair cable is connected to a removable terminal strip on the face of each module.

As shown in Figure 1.1, the LI module has two communication channels. Each channel may consist of a chain of up to 8 drops (digital or register racks). More than one LI module may be used with many of the SY/MAX Family processors, depending upon system requirements.

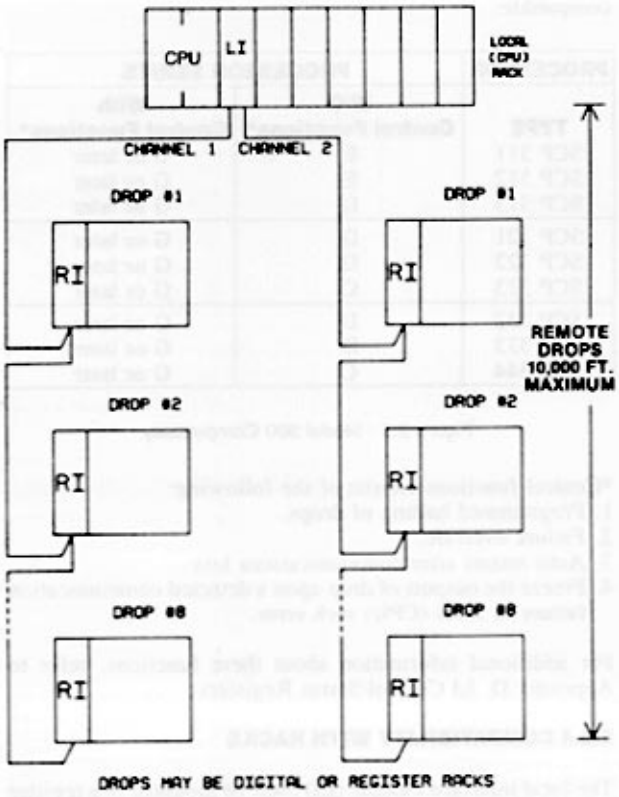


Figure 1.1 - Local/Remote System

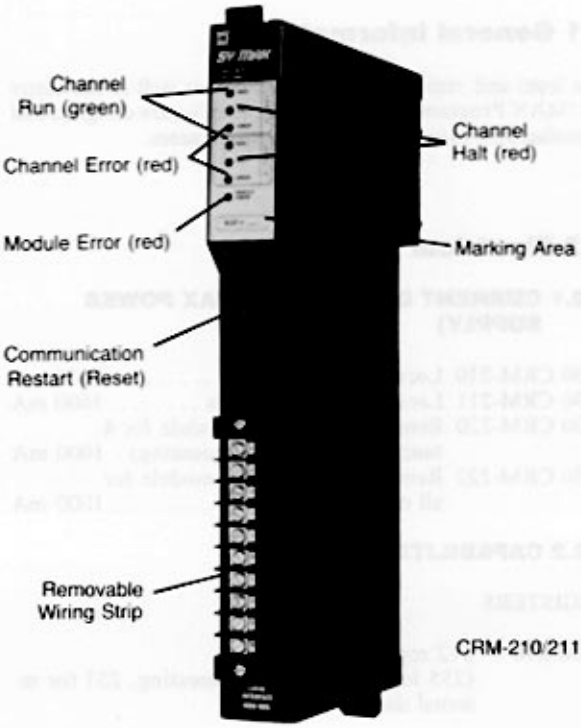


Figure 1.2 - Local Interface Features

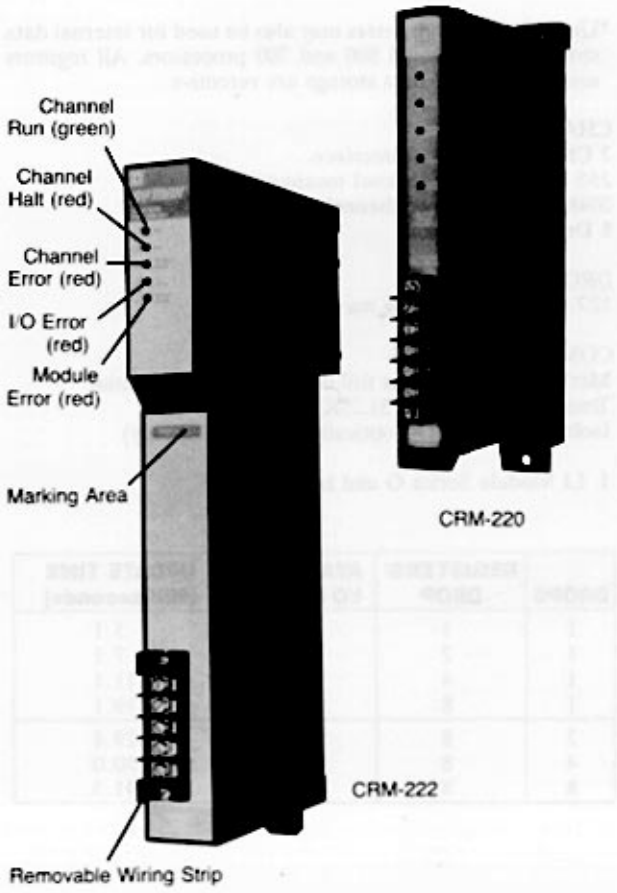


Figure 1.3 - Remote Interface Features

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2.0 SPECIFICATIONS

2.1 General Information

The local and remote interface modules, as well as the entire SY/MAX Programmable Controller Family, are designed and manufactured to comply with U.L. requirements.

2.2 Electrical

2.2.1 CURRENT DRAW (ON SY/MAX POWER SUPPLY)

8030 CRM-210 Local w/512 Registers . . . . . 1600 mA
8030 CRM-211 Local w/4096 Registers . . . . . 1600 mA
8030 CRM-220 Remote (low profile module for 4 function digital rack mounting) . 1000 mA
8030 CRM-222 Remote (standard size module for all rack mounting). . . . . 1000 mA

2.2.2 CAPABILITIES

REGISTERS

CRM-210 = 512 registers
(255 for external drop addressing, 257 for internal data storage*)

CRM-211 = 4096 registers
(255 for external drop addressing, 3841 for internal data storage*)

*Unused external registers may also be used for internal data storage in the model 500 and 700 processors. All registers used for internal data storage are retentive.

CHANNELS
2 Channels per local interface.
255 Registers per channel maximum.
2048 Digital I/O per channel maximum.
8 Drops per channel.

DROPS
127 Registers per drop maximum.

COMMUNICATIONS
Method — Continuous full duplex serial differential
Transmission Rate — 31.25K Baud
Isolation — 300VDC optically coupled[1] (LI only)

1. LI Module Series O and later only.

DROPS	REGISTERS/ DROP	AVAILABLE I/O POINTS	UPDATE TIME (Milliseconds)
1	1	16	5.1
1	2	32	7.1
1	4	64	11.1
1	8	128	19.1
2	8	256	29.4
4	8	512	50.0
8	8	1024	91.3

Figure 2.1 Maximum Channel Update Times (Digital I/O Only)

DROPS	REGISTERS/ DROP	TOTAL REGISTERS	UPDATE TIME (Milliseconds)
1	4	4	14.6
1	8	8	24.5
1	16	16	34.4
1	32	32	54.3
1	64	64	94.0
1	127	127	172.1
2	8	16	36.0
2	16	32	55.8
2	32	64	95.5
2	64	128	166.5
2	127	254	332.7
4	16	64	103.4
4	32	128	182.8
4	64	254	341.5
6	16	96	220.4
6	32	192	260.4
8	16	128	195.4
8	32*	255	352.9

* One drop has only 31 registers.

Figure 2.2 - Maximum Channel Update Times (Register and Digital I/O)

2.2.3 COMPATIBILITY WITH PROCESSORS

The local remote interface system is compatible with all Model 400, 500, 600 and 700 SY/MAX Processors. Multiple LIs may be used with Models 400, 500, 600 and 700. The Model 300 can support one LI Module.

The following Class 8030 Model 300 Processors are also compatible:

PROCESSOR	PROCESSOR SERIES	
TYPE	W/O Control Functions*	With Control Functions*
SCP 311	E	G or later
SCP 312	E	G or later
SCP 313	D	G or later
SCP 321	D	G or later
SCP 322	D	G or later
SCP 323	C	G or later
SCP 332	D	G or later
SCP 333	D	G or later
SCP 344	C	G or later

Figure 2.3 - Model 300 Compatibility

*Control functions consist of the following:
1. Programmed halting of drops.
2. Failure override.
3. Auto restart after communications loss.
4. Freeze the outputs of drop upon a detected communication failure or local (CPU) rack error.

For additional information about these functions, refer to Appendix D, LI Control/Status Registers.

2.2.4 COMPATIBILITY WITH RACKS

The local interface module (LI) must be mounted in a register slot of the CPU rack while the remote interface module (RI) is mounted into the CPU slot of a remote rack.

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RACK TYPES	LOCAL INTERFACE	REMOTE INTERFACE	
	TYPES CRM-210, 211	Type CRM-220	Type CRM-222
CRK-100, 210	NO	YES	YES
CRK-210, 300 DRK-210, 300 GRK-110, 210	YES	YES	YES
HRK-100, 150, 200 RRK-100, 200, 300	YES	NO	YES

Figure 2.4 - Rack Compatibility

2.2.5 COMPATIBILITY WITH I/O

The local/remote interface system is compatible with:

All register modules.
All 32 point I/O modules.
All 16 point I/O modules.
All 8 point I/O modules.
All 4 point input modules.
All 4 point output modules, Series B or later.
Bus Expander, Class 8030 Type CRM-115/116, Series D or later.

2.3 Environmental

Ambient Temperature
Operating 0°C to 60°C (32° to 140°F)
Storage -40°C to 80°C (-40° to 176°F)

Humidity 5-95% non-condensing

2.4 Physical

Dimensions (WxHxD)
CRM-210, 211, 222 1.5 x 12.8 x 6.6 in.
3.81 x 32.5 x 16.76 cm
CRM-220 ..... 1.5 x 9.6 x 6.6 in.
3.81 x 24.4 x 16.76 cm

Weight
CRM-210, 211, 222 3.0 lbs.
1.36 kg.
CRM-220 ..... 1.0 lb.
0.45 kg.
Terminal strips
CRM-210, 211 ..... Part Number 25410-02529
CRM-220 ..... Part Number 30605-255-02
CRM-222 ..... Part Number 25410-02526

3.0 INSTALLATION

3.1 General Information

CAUTION: To prevent possible equipment damage, remove power from all local and remote racks before inserting or removing any component including the interface modules or LI/RI communication cables.

Local Interface Modules identified as Series L or later incorporate diagnostic enhancements not available in earlier series devices. Expanded error checking of data registers will return a unique error code (901) in the event a data corruption is determined. When initially replacing or installing a new Local Interface (LI), the user should expect the posting of this error as a normal "out of the box" condition. After installing the device and powering up the system, upon initially keyswitching the processor to DISABLE OUTPUTS or RUN, the processor will remain in HALT and the LI will indicate a MODULE ERROR. The processor error register (8175) will identify the LI in error while the LI error register will contain the value 901. This is a normal occurrence, reflecting the fact that the LI storage registers are corrupt (contain random data). Key Switching the processor a second (or third) time will result in all LI registers being reset to zero and the error being cleared. Normal operation will then result.

3.2 Inspection

Although each module is subjected to strict quality control procedures, give each module a visual inspection before installation. Check for any shipping or handling damage that may have occurred. If damage is found, do not use the module, replace it.

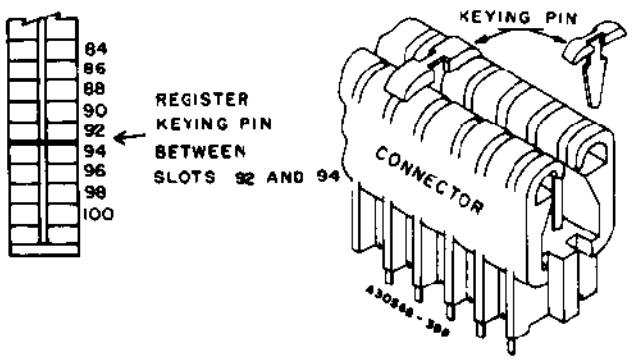
3.3 Module Keying

Each register or CPU slot on a rack assembly may be keyed. An optional keying pin kit, Class 8030 Type CBP 104, is available for this purpose.

The keying pin may be inserted manually into the slot using the keying pin insertion tool provided with the kit.

The correct positioning of the keying pin for the LI and RI modules follows:

TYPE	DESCRIPTION	PIN LOCATION
CRM-210	Local Interface (LI) Module w/512 Registers	Between 92 & 94
CRM-211	Local Interface (LI) Module w/4096 Registers	Between 92 & 94
CRM-220	Remote Interface (RI) Module (for 4 function digital racks)	None
CRM-222	Remote Interface (RI) Module (for all type rack assemblies)	None



Keying Pin Location Keying Pin Insertion

Figure 3.1 - Module Keying

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3.4 Module Location

3.4.1 LOCAL INTERFACE

The local interface module (LI) must be placed in the same rack assembly as the CPU. When a register rack is used to house the CPU, the LI module should be placed in the next closest slot. If more than one LI module is required, place additional modules in adjacent slots.

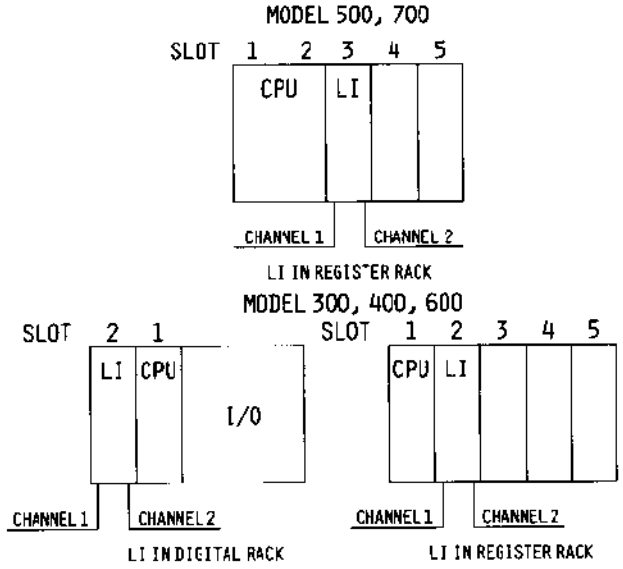


Figure 3.2 — Local Interface Location

3.4.2 REMOTE INTERFACE

The remote interface module (RI) must be placed into the CPU slot of any rack which is to be a drop.

Only one RI is required and allowed for each drop.

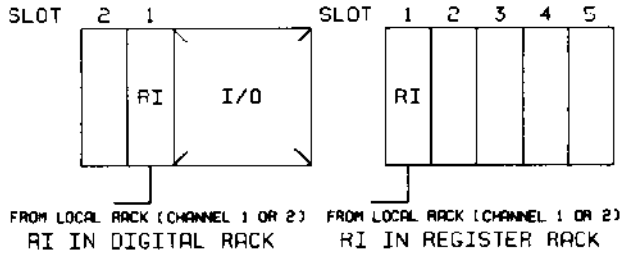


Figure 3.3 - Remote Interface Location

3.5 Field Wiring

3.5.1 POWER CONNECTION

No external power wiring is required. The LI and RI modules receive their power through the edge connector socket of the rack assembly. Insert the LI module in the register slot until firmly seated against the stud (the middle post above the socket in that slot) and tighten the captive mounting screw at the bottom of the module. These two connections not only provide support for the module but also provide a ground.

3.5.2 COMMUNICATION CABLE

The communication between the LI and RI modules is achieved via a dual shielded twisted pair cable. A hinged plastic flap covers the detachable terminal strip. In order to minimize the potential of electrical interference:

1. Route communication cable in different wire ducts than the power wiring is routed.
2. Connect each end of the communications cable shield to the shield terminal on each module.

Transmission cable should be electrically equivalent to:

Cable Type	Maximum Length	Conductor-Conductor Capacitance
Belden 8723	7,500 feet	35 pf/ft.
Belden 9463*	10,000 feet	19.7 pf/ft.

*Dual cables required.

NOTE: ADDITIONAL DATA LINE PROTECTION
In environments where lightning or induced transients over communication lines are likely to cause hardware failures, signal line protection devices are recommended. Even though transient protection is designed into our SY/MAX communication circuits, additional specialized protection devices are suggested in areas where there is a high probability of secondary lightning strikes occurring. The specific environments which are of greatest concern are where communication cable runs are in the outside environment. Refer to Appendix G.

3.5.3 LOCAL/REMOTE CONNECTIONS

The required method of wiring from one module to the next is daisy chain. Since the LI/RI is designed to operate as a serial link, any configuration other than daisy chain may result in erratic operation. Total allowed cable distance for each channel when using Belden 8723 is 7,500 ft.

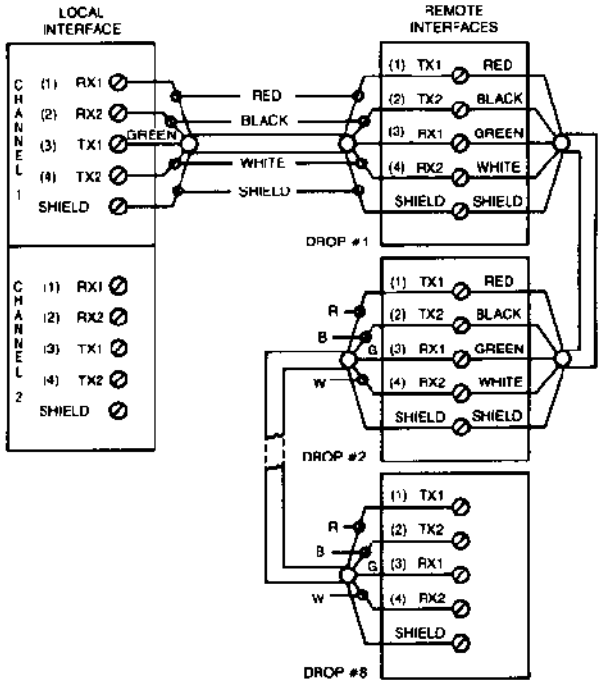


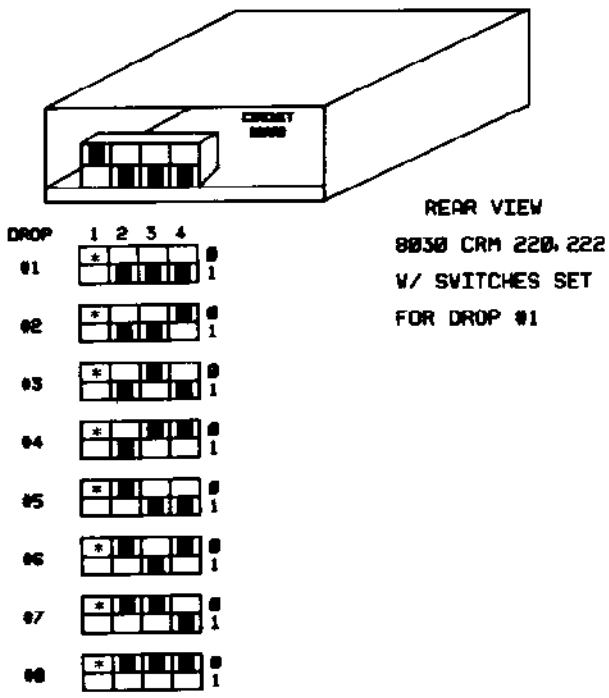
Figure 3.4 - LI/RI Wiring Connections

3.6 RI Switch Settings

The RI Module has four dip switches on the rear of the module near the edge of the circuit board. A module must be assigned as one of the eight drops on a specific channel. The switches must be set for the system to operate properly.

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Set the switches for the appropriate drop as shown in Figure 3.5 - RI switch settings.



*For each channel, the drop (RI module) farthest from the LI must have switch 1 set ON, to a (1). Only one drop per channel requires this switch to be set. Failure to do so may result in a noise susceptible communications link.

Figure 3.5 - RI Switch Settings

Label terminology may vary. The following equivalent terms are used:

0	0	UP	OPEN	OFF
1	X	DOWN	CLOSED	ON

Either one of these labels will be located on the side of the RI module.

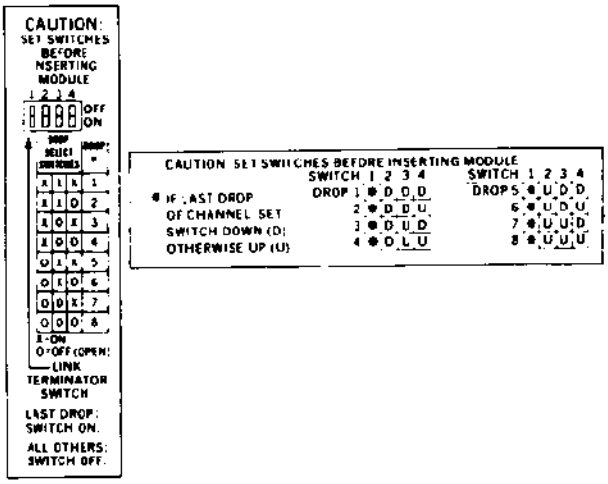


Figure 3.6 - RI Module Labels

4.0 OPERATION

4.1 General Description

Local and remote interface modules allow a programmable controller to communicate with remote I/O (digital and register input and output type devices).

The LI/RI interface system consists of:
1. A local interface module (LI) which plugs into a register slot of the rack containing the CPU.
2. A remote interface module (RI) placed in the CPU slot of a digital I/O rack or the first slot of a register rack.
3. An interconnecting cable between the LI and RI(s) consisting of dual twisted shielded pair.

Both the LI and RI modules have diagnostic LED's indicating the status of the communication link, individual drop operation and module operation.

The local/remote I/O interface system is a serial, multi-channel, multi-drop system. The local interface (LI) receives instructions from the CPU. The LI then serializes this information and transmits it to the appropriate remote interface (RI). An LI module does this over either of its two independent communication channels. Each channel operates full duplex at a rate of 31.25K baud.

The RI interprets this data, verifies and acknowledges it and then acts accordingly. The information being exchanged is stored in an image table located in each LI and RI.

The continuous exchange of information between the LI and RI image tables is independent of the CPU scan. Transmitted information includes ON/OFF commands for I/O as well as storage register information and housekeeping functions (e.g. loss of communications, error control, freeze or reset of I/O).

The LI module stores control register information while the RI maintains its own specific drop information. This information (user programmable bits) defines the action to be taken in the event of a fault at any drop. It can allow the operational drops to keep running or to shutdown. The shutdown state of the outputs will then be either a reset (OFF) or freeze (last state) condition.

Actual programming steps are described in the programming equipment instruction bulletins. For details on user programmable bits, refer to Appendix D, LI Control/Status Registers.

4.2 Local Interface Registers

Two versions of the LI module are available. The first, Class 8030 Type CRM-210, has 512* registers; and the second,

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Class 8030 Type CRM-211, has 4096* registers. With either version LI, the first 255** registers are available for external addressing of inputs, outputs, register modules, storage registers or as internals. The remaining registers (257 for CRM-210, or 3841 for CRM-211) are available for use as internal relay equivalents, timers, counters, and data storage in the Model 500 and 700.

*Although the registers exist, the ability to address them is dependent upon the type of CPU used.

**Any of the 255 registers not assigned to drops may be used as internals for the Model 500, 700.

4.2.1 EXTERNAL REGISTERS

A maximum of 255 consecutive registers can be assigned between the two independent LI channels. Each LI channel can support up to 8 drops. (A drop is a remotely located rack assembly.) Any drop may have a maximum of 127 registers assigned to it. The first 8 registers assigned to a drop are available for digital or register I/O. (e.g. 8 registers x 16 bits provide for 129 I/O points per drop.) Any registers beyond the first 8 are only for register I/O.

The registers assigned to drops will be reset to zero (OFF) upon processor halting or power loss. However, it is possible to freeze (maintain last state) registers assigned to drops. For more information, refer to Appendix D, LI Control/Status Registers.

4.2.2 INTERNAL REGISTERS

Internal registers (those not assigned to drops) retain information when the processor halts or there is a loss of main power. The clearing of these registers is dependent upon processor action.

4.2.3 CONTROL REGISTERS

All LI modules have an error code register and a channel control register for each serial channel. These registers monitor and provide additional control of the remote I/O. For more information, refer to Appendix B, Error Codes and Appendix D, LI Control/Status Registers.

4.3 Rack Addressing

Rack Addressing (also referred to as System Definition) is a user programmable identification scheme that enables a SY/MAX Processor to obtain information about a specific I/O point or register

It maps the physical location of where the processor (CPU) will "look" for a specific address and its associated information when required.

Once the register addresses have been assigned, they are fixed. If a change in address assignments is required, the user rack addressing software must be changed.

4.3.1 PROCESSOR (CPU) CONSIDERATIONS

The CPU determines the maximum system addressing range. SY/MAX Processor capabilities are as shown in Figure 4.1.

4.3.2 ADDRESSING ASSIGNMENT AND DISTRIBUTION

All address assignments must be made in a sequential and ascending order. The first 255 LI registers may be assigned to channel 1 and then to channel 2. Each of these channels can be further divided into 8 drops. The register addresses for each drop may be further distributed in ascending order to individual slots of the remote drops.

Internal addresss begin after external addresses have been assigned. Internal and external registers cannot be intermixed.

4.3.3 LI CONTROL REGISTER ALLOCATION

LI control registers are dynamically assigned on the basis of physical position and rack addressing.

1. LI control registers are assigned in a descending order starting with S8163 for the LI with the lowest numbered CPU rack slot number.
2. LI control registers are further defined by the number of channels used.

For example, if only channel 1 is assigned to the first LI, there will be no control register assigned to channel 2. S8163 is the error code control register. S8162 is the channel control register for channel 1, S8161 is left unassigned.

If an additional LI is put in a higher numbered CPU slot, it would be assigned the *next* available control register, i.e. S8161 becomes the second LI error code register. S8160 is the control register for channel 1 of the second LI. S8159 is unassigned and available for channel 2 or for a third LI's error code register. If only channel 2 is defined, the system automatically assigns a control register to channel 1 whether channel 1 is used or not.

For more information on the operation of the LI control registers, refer to Appendix B, Error Codes and Appendix D, LI Control/Status Registers.

CPU Model	Register Addressing Capability	Self Contained CPU Registers	Maximum Supportable LI Modules	Practical I/O Capability
300	112 (1)	112	1	256
500	2008 (2)	460 (3)	14	2000
700	8000 (2)	0	14	8000
400	4000	4000	15	4000
600	8000	8000	15	8000

(1) Only the bits of the first 32 registers may be forced ON/OFF.

(2) Only the bits of the first 256 registers in each LI may be forced ON/OFF.

(3) For internal use only as relays and storage registers.

Figure 4.1 - CPU Address Capabilities

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4.3.4 LI/RI ADDRESSING WITH MODEL 500

The following example is used to illustrate the concept of address assignment.

This example consists of a Model 500 system with two remote I/O channels. The first channel handles 256 digital I/O points and one register module. Two remote drops are used to handle these requirements. The second channel consists of a register rack with 5 register modules.

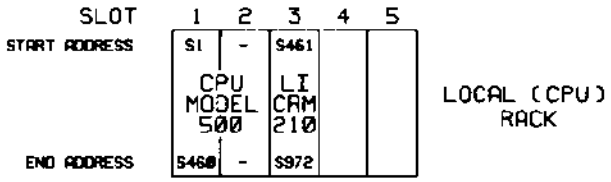


Figure 4.2 - Local (Model 500 CPU) Rack Address Assignments

LOCAL (CPU) RACK

Slot 1 - The Model 500 has been assigned all of its 460 internal registers. (S1 thru S460)

Slot 2 - The Model 500 physically takes up two slots therefore, slot 2 has no address assignments required.

Slot 3 - The LI module (CRM-210) has been assigned all of its 512 registers. (S461 thru S972)

Slot 4, 5 - No address assignments required.

Assigning all available registers to the CPU and LI does not affect the CPU scan. Note that the first register of the LI has a start address of S461, one more than the assigned end address of the processor. The LI end address is S972 which is 512 more than the end address of the processor.

Note that the start and end addresses of the system slots are shown. However, when programming addressing assignments, only ending addresses can be entered. Starting addresses are automatically assigned beginning with the next available register. For a full explanation of the step by step rack addressing programming procedure, refer to the SFW-3XX Programming Instruction Bulletin.

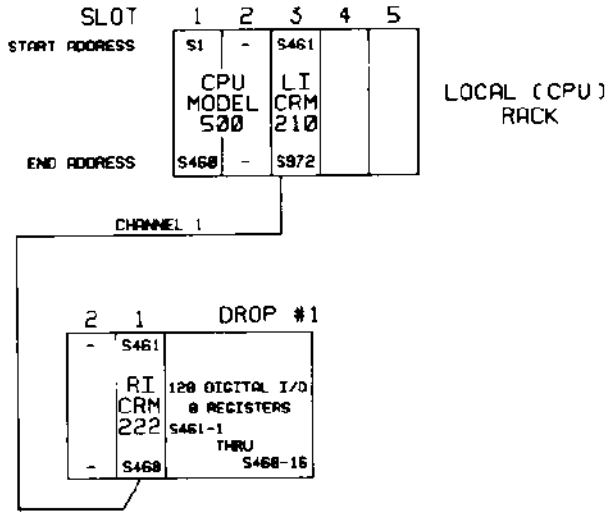


Figure 4.3 - Channel 1, Drop #1 Rack Address Assignments

CHANNEL 1, DROP #1

Slot 1 - To handle 128 digital I/O points, 8 - 16 bit registers are required. (S461-1 thru S468-16)

Note that the addresses for digital I/O are always assigned to slot 1.

Slot 2 - No address assignments required.

CHANNEL 1, DROP #2

The next order of business is to add another drop to an already existing channel. This drop also has 128 digital I/O points but unlike drop #1, it has a register module. The module is in the register slot, (slot 2) which requires 16 register addresses.

Slot 1 - 8 registers are assigned for the 128 digital I/O. (S469-1 thru S476-16).

Slot 2 - 16 registers are required for the register module. (S477 thru S492).

The total requirement for this drop is 24 registers. Observe that the start address for drop #2 is one more than the end address for drop #1. The first digital address for drop #2 is S469-1 and the last digital address is S476-16. Therefore, slot 1 has an ending register address of S476. Slot 2 ends at S492, allowing for the required 16 registers needed by the register module.

This process of adding a drop at a time in a daisy chain fashion could be continued until all 255 registers were assigned to a channel or until all 8 drops had been assigned.

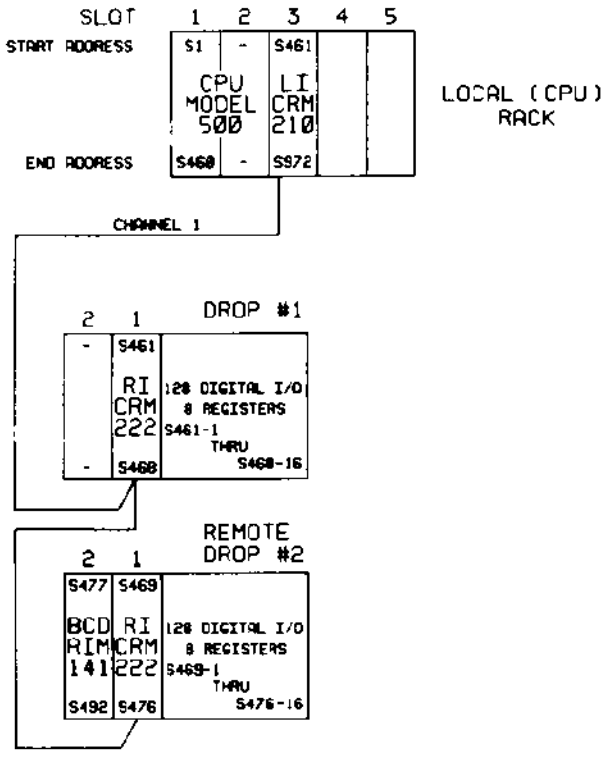


Figure 4.4 - Channel 1, Drop #2 Rack Address Assignments

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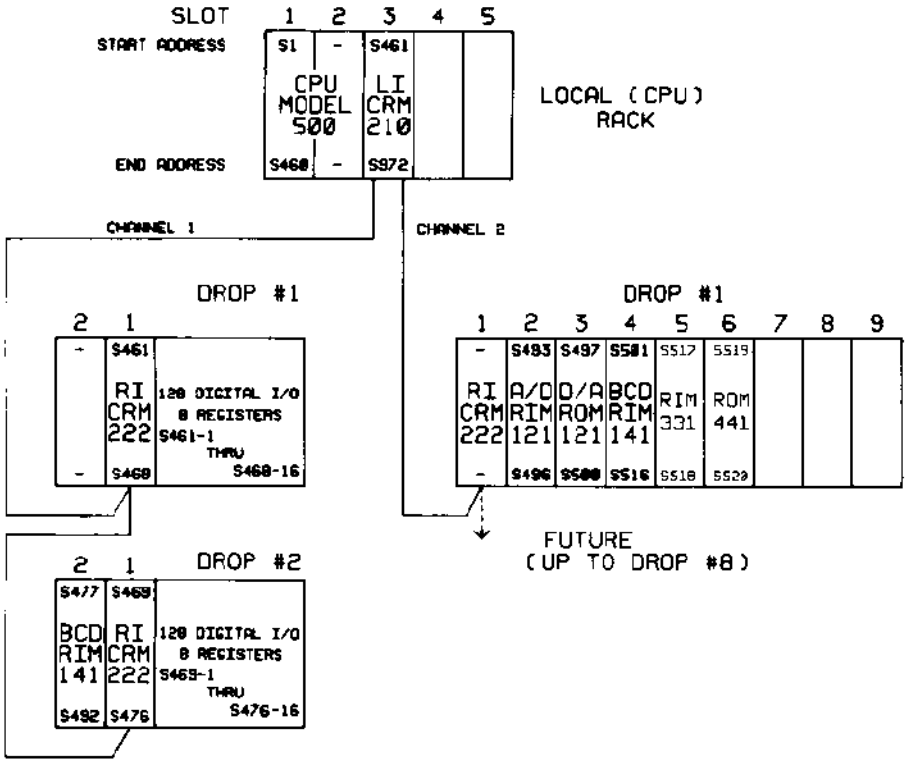


Figure 4.5 - Channel 2, Drop #1
Hack Address Assignment

CHANNEL 2, DROP #1

In this example, a 9 slot register rack is connected to channel 2.

Note that the starting address for channel 2 is one greater than the ending address of channel 1. In other words, when channel 1 ends, channel 2 begins.

Requirements for register modules vary. As an example, a 4 channel analog module requires 4 registers for complete addressing. A BCD I/O module requires 16 registers and a 32 point I/O module requires 2 registers each.

Slot 1 - No address registers are required since there is no digital I/O bus in the register rack. (The 32 point ditigal I/O modules appear as another register module to the LI.)

Slot 2 - 4 registers are assigned to a 4 channel analog input module. (S493 thru S496)

Slot 3 - 4 registers are assigned to a 4 channel analog output module. (S497 thru S500)

Slot 4 - 16 registers are assigned to a 16 (4 digit) BCD input module. (S501 thru S516)

Slot 5 - 2 registers are assigned to a 32 point digital input module. (S517 and S518)

Slot 6 - 2 registers are assigned to a 32 point digital output module. (S519 and S520)

Slot 7,8,9 - No address assignments required.

The total number of registers required for this drop is 28. Note the beginning and ending addresses for each slot are sequential and in ascending order.

LI ADDRESS DISTRIBUTION MAP

Here is a map of how the first LI has been user programmed in this example.

Observe that the LI has a fixed number of registers and rack addressing has assigned a unique address to each one.

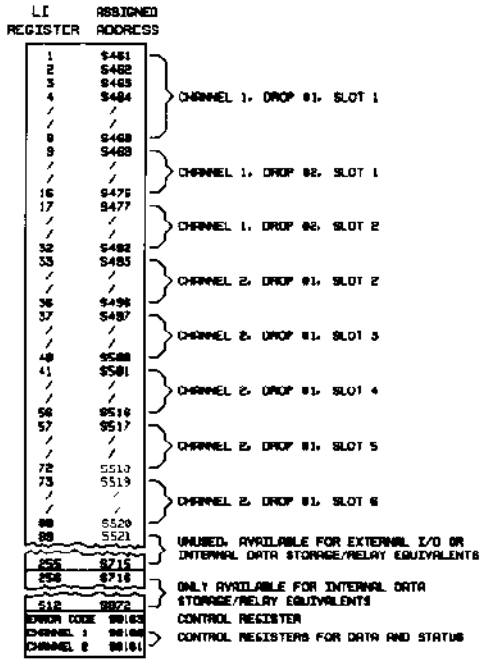


Figure 4.6 - LI Register Map

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4.3.5 LI ADDRESSING WITH THE MODEL 300, 400 AND 600

As **Figure 4.1, CPU Addressing Capabilities** shows, the Model 300, 400 and 600 processors differ from the Model 500 and 700 in the area of self-contained CPU registers. All of the registers available to the Model 300, 400 and 600 are self-contained. In other words, it is unnecessary to Rack Address storage registers to modules like the LI as in a Model 500 or 700 system. When creating rack addressing for a Model 300, 400 or 600 system, only assign the number of register required for current and future remote drops. While it is valid to assign additional registers to the LI, it may reduce overall system throughput.

As an example, the Rack Addressing presented in the previous section for a Model 500 system can be used, as is, for a Model 400 or 600 system. But in order to optimize the system, only those registers required for remote drops (S461 S520) should be assigned to the LI. All other registers (S521-S4000 for the Model 400 or S521-S8000 for the Model 600) would still be available for storage. Because the Model 300 has only 112 registers available, the Rack Addressing presented in the previous section would not apply. Refer to Appendix F for additional information on Rack Addressing with a Model 300.

4.3.6 MULTIPLE LIs

If more drops or registers are required than those that can be supported by the present LI, merely add an additional LI module.*

An LI module only provides storage register locations to a processor which possesses the capability to address them. The LI module does not increase the CPU addressing range capability.

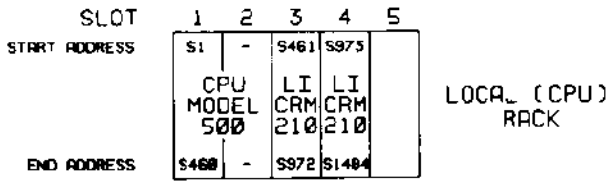


Figure 4.7 - Local (CPU) Rack Addresses with Multiple LIs

LI control register assignments are dependent upon LI position and number of channels used.

*The number of LIs per system is CPU dependent, the Model 300 will support only one LI Module.

4.4 Summary

These steps should be looked at prior to setting up any LI/RI system.

1. Sketch out the physical system configuration, (rack assemblies, power supplies, I/Os, etc.).
2. Determine the address allocations based upon requirements of the system.
3. Consider the system response time. Refer to Appendix A, LI/RI Update Time.

4.4.1 HARDWARE CONSIDERATIONS

1. Determine the physical I/O requirements including future expansion. (Quantity, voltages, racks)
2. Determine I/O locations and number of drops required as well as I/O per drop.
3. Determine the type of register modules required, including future expansion.
4. Determine the location of register modules, quantity, and types of racks required.
5. All modules used with the local/remote interfaces must be of compatible series.
6. Communications devices should be powered down when connecting and disconnecting communication cabling. If a communication wire were to be shorted, premature chip failure may result.
7. The LI module is always installed in the local CPU rack assembly.
8. The RI module is always installed in slot 1, the CPU slot of the remote drop.

4.4.2 SOFTWARE CONSIDERATIONS

CAUTION: Only qualified personnel should ever program or implement action which may override the default system operations. A thorough understanding of the control bits is required. If any control bits are misapplied, adverse consequences may result.

1. Any detected system error will result in the system halting. However, it is possible to override the halting of the total system when an error is in the remote location, dependent upon the severity of the error detected.
2. All digital I/O address on a drop must be assigned to slot 1.
3. No registers need be assigned to slot 1 of a register rack used as a drop.
4. Register Planning

   Register and I/O distribution for present and future needs should be considered prior to attempting any register address allocation (rack addressing).

   For effective distribution of register addresses:

   A. Distribute external addresses evenly among channels. This allows for a uniform LI/RI update time.

   B. Examine the LI/RI update time. If it is too long, add an additional LI module to obtain more channels. This will reduce the number of registers per channel. For more detail, refer to Appendix A, LI/RI Update Time.

   Determine the CPU's ability to access the registers in the LI. For more information, refer to Figure 4.1 and the appropriate processor instruction bulletin. Remote drop addressing must be done sequentially. Therefore, plan to add future remote drops to channel 2.

   For more information, refer to Appendix C, Channel Expansion.
5. CPU will go into the RUN mode only if all the drops are operational. Note that a drop may be made to appear operational by setting a channel control register Failure Override Bit ON (1). For more information, refer to Appendix D, LI Control/Status Registers.

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5.0 TROUBLESHOOTING

5.1 General Information

This section explains the procedures for troubleshooting the local and remote interface (LI/RI) system. Following the outlined procedures will aid in evaluating a malfunctioning system.

5.2 General Procedures

Always do the following:
1. Examine and note what the system is doing and has failed to do.
2. Examine and note the LED states on the LI/RI interfaces. (Refer to Figure 5.1 and Figure 5.2, LI and RI LED Explanation.)
3. Using a Programmer, examine and note the control register information. (Refer to Appendix D, LI Control/Status Registers.)

There are three primary types of malfunctions which can occur within the SY/MAX Family LI/RI systems.

1. A CPU processor malfunction.
2. Component failure.
3. User software program error.

5.2.1 CPU PROCESSOR MALFUNCTION

If a CPU processor malfunction is suspected, refer to the appropriate processor and CRT programmer instruction bulletins for further troubleshooting procedures.

If, however, it appears the problem may be related to the LI/RI system or user control program software, continue in this section.

5.2.2 COMPONENT FAILURE

Besides the CPU, the malfunctioning of the following hardware components may cause the PC system to halt or continue to run in a partial mode.

LI MODULES
RI MODULES
REGISTER MODULES
I/O MODULES
RACK ASSEMBLY
POWER SUPPLY

Also, the system may halt if there is a lack of, or insufficient power at any location or a communication error.

Before replacing any hardware items, verify the problem by interpreting the LEDs and control register information.

5.2.3 USER SOFTWARE PROGRAM ERROR

A CRT programmer is helpful in analyzing LI/RI problems whether they are user created or system malfunctions. Use the monitor mode to display the following registers:

8175 - processor error code register. (data & status field)
8176 - processor control register. (data field)
8186 - processor read only status control register. (data field)
8163 - first LI Error Code Register. (data & status field)
8162 - first LI channel 1 Control/Status Register. (data & status field)
8161 - first LI channel 2 Control/Status Register. (data & status field)*

Note: The error code registers only display the most critical error detected prior to a total system shutdown. An error code may indicate either a specific register problem or it may be indicating the first register address of a block of registers where a problem has been detected.

Progressively inspecting all of the available CPU and LI control registers will aid in pinpointing the trouble area. Inspection of the channel control register data field (bits 1-8) will indicate what racks are halted due to the user program initiated control action while the status field will display the errored drops (bits 21-28).

*For more information, refer to Section 4.3.3 LI Control Register Allocation.

5.3 LI/RI LED Explanation

For a normally operating system, all of the associated CPU, LI and RI modules should have their RUN LED's illuminated. When a detected system change occurs, the LED's indicate the status of the system. If an error has occured, it will also indicate where the error most likely originated.

However, if any of the RUN LEDs are off, it does not necessarily indicate that a system malfunction has occurred. The system could be in some mode of operation other than RUN such as DISABLE OUTPUTS, or even a HALT condition by virtue of the user program.

In most cases, inspection of the LEDs will directly indicate the status of each communications link and "point" to the error source.

The meaning of the LI and RI modules LED states is depicted in figures 5.1 and 5.2.

If it is impractical to view all the diagnostic LEDs or if they do not readily indicate where the failure has originated, inspection of the error code registers of the CPU and LI will aid in finding a fault.

General error code register information is described in Appendix B, Error Codes.

5.4 Fault Isolation Procedures

Note what the system is doing by examining the following:

1. LEDs

Determine which of the following LEDs are ON, FLASHING, or OFF.

A. CPU (system processor)
B. LI
C. RI

2. Error Registers

Determine the contents of the Error Code and Control Registers.

A. CPU (system processor register S8175)
B. LI register (i.e. S8163 for the first LI in a system) refer to Appendix B, Error Codes for further information.

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LOCAL INTERFACE	
All lights OFF indicates loss of 5VDC power.	
RUN (green)	
ON -	Indicates LI is operational and CPU is accessing image table information.
OFF -	Indicates LI is in self-diagnostics or has failed.
FLASHING -	Indicates LI is running but one or more drops on its channels have been programmed to halt. (Bits 1-8 of the LI channel control register.)
HALT (red)	
ON -	Indicates LI is in self-diagnostics and/or has halted operation.
OFF -	Indicates LI is fully operational and CPU is accessing image table information.
FLASHING -	Indicates LI is running but one or more drops on its channels have been programmed to halt. (Bits 1-8 of the LI channel control register.)
CHANNEL ERROR (red)	
ON -	Indicates LI cannot communicate with one or more of its drops which are shutdown.
OFF -	Indicates all drops operational.
FLASHING -	Indicates a module failure on a drop has caused a drop to shutdown on this channel.
MODULE ERROR (red)	
ON -	Indicates a self diagnostic error or internal timeout error has been recognized and halted the CPU.
OFF -	Indicates LI is operational even though a channel HALT or CHANNEL ERROR LED may be ON.
FLASHING -	Not valid

Figure 5.1 - LI LED Explanation

REMOTE INTERFACE	
All lights OFF indicates loss of 5VDC power.	
RUN (green)	
ON -	Indicates remote drop is operational.
OFF -	Indicates RI is shutdown or has not been initialized. Outputs will de-energize provided the shutdown is not a direct result of a communication error, and the Freeze function is also selected. (Some register modules are capable of maintaining register information.)
FLASHING -	Indicates CPU is in Disable Outputs mode. (50% ON, 50% OFF alternately with HALT LED.)
BLINKING -	Indicates LI HALT bit for the drop is set. (5% ON, 95% OFF, alternately with HALT LED.)
HALT (red)	
ON -	Indicates RI is shutdown. If the only LED ON, it indicates rack was shutdown due to program control or has not been initialized.
OFF -	Indicates remote drop is operational.
FLASHING -	Indicates CPU is in Disable Outputs mode. (50% ON, 50% OFF alternately with RUN LED.)
BLINKING -	Indicates LI HALT bit for the drop is set. (95% ON, 5% OFF, alternately with RUN LED.)
CHANNEL ERROR (red)	
ON -	Indicates invalid or loss of communications between RI and LI. HALT LED will also be ON.
OFF -	Indicates valid communication between RI and LI.
I/O ERROR (red)	
ON -	Indicates: (HALT LED should also be ON.) 1. A read after write error to an output. 2. Error caused by a malfunctioning register module. 3. RI malfunction.
OFF -	Indicates RI is properly communicating with modules in same rack.
FLASHING -	Indicates outputs and inputs are frozen (ON or OFF).
MODULE ERROR (red)	
ON -	Indicates self diagnostic error or internal timeout error has occurred.
OFF -	Indicates RI is operational although drop may be shutdown due to system shutdown or program control.
FLASHING -	Not valid

Figure 5.2 - RI LED Explanation

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3. Control Registers

   Determine the contents of the respective Channel Control Registers

   A. Channel 1, LI register (S8162 for the first LI in the system)
   B. Channel 2, LI register (S8161 for the first LI in the system) refer to Appendix D, LI Control/Status Registers for further information.

Progressive evaluation and interpretation of these bits indicate how to resolve, eliminate or compensate for the system malfunction.

5.5 Undervoltage Lockout Circuit (ULC) Operation

Series O and later Local Interface devices are designed with an on-board DC Undervoltage Lockout Circuit that monitors the incoming DC voltage level at the edge connector of the slot in which the LI Module resides. If the incoming DC voltage falls below 4.6 volts, the CRM-210, 211 enters a HALT state and no longer communicates with the processor on the rack, or its associated I/O. All LEDs on the front of the module are turned off and the processors in the CPU rack are halted.

When incoming DC voltage rises above 4.6V, the CRM-210/211 executes a standard power-up initialization sequence. When recovering from a ULC error, a 902 error code is posted in the LI error register (e.g. 8163).

Even though Series O and later Local Interface devices enter a HALT state when the incoming DC voltage falls below 4.6VDC, other devices in the same rack may remain powered-up, since the ULC resides in only selected SY/MAX Modules.

Some possible causes for the ULC being engaged are, an overloaded power supply or a poor cable connection between the power supply and the rack. If these or other problems arise, correct the respective problem first, then normal operation can be resumed.

5.6 Module Replacement Procedure

If it is necessary to replace components, use the following procedure:

1. Keyswitch the CPU to HALT prior to removing power.
2. Remove power from all rack assemblies in a system.
3. Disconnect communication cabling and remove module.
4. Set switches on replacement module.
5. Install module and attach communication cabling.
6. Reapply power to system.
7. Restart the system and verify operation.

NOTE: ERROR 901 identifying register corruption may require toggling processor keyswitch several times to clear the error.

5.7 LI/RI Communication Restart (Push Button)

Whenever communication is lost between the LI and an RI, an error code is generated and the Channel Error LED will be ON. Communication may be lost because of the following:

1. Loss of power at the Local CPU Rack.
2. A broken cable between the LI and RI.
3. Loss of power at a Remote Rack (DROP).
4. Hardware malfunction.

Reestablishment of LI/RI communications will always be attempted each time any of the following occurs:

LI/RI LED RESPONSES TO ERRORS

CPU STATUS		LI LIGHTS						RI LIGHTS								LI CHANNEL BITS		OPERATING CONDITION
		WITH A DROP FAILED			WITH ALL DROPS OPERATIONAL			FAILED DROP				OPERATION DROP						
RUN/HALT		CHANNEL RUN HALT	CHANNEL ERROR	MODULE ERROR	CHANNEL RUN HALT	CHANNEL ERROR	MODULE ERROR	RUN HALT	CHANNEL ERROR	I/O ERROR	MODULE ERROR	RUN HALT	CHANNEL ERROR	I/O ERROR	MODULE ERROR	FAILURE OVERRIDE BIT 13	FREEZE BIT 9	
R	C	–	–	C	R	O	O	R	O	O	O	R	O	O	O			Normal (CPU Run)
F	C	–	–	C	R	O	O	F	O	O	O	F	O	O	O	–	–	Disable Outputs (CPU Run)
R	C	–	–	C	F	O	O	B	O	O	O	B	O	O	O	–	–	Control Register Halt Bit Set
O	F	R	I	I	R	O	O	H	O	O	X	H	O	O	O	O	O	Transmission Error
O	F	R	F	I	R	O	O	H	O	I	O	H	O	O	O	O	O	Bus or Read After Write Error
O	F	R	I	I	R	O	O	H	O	F	X	H	O	F	O	O	I	Transmission Error
O	F	R	F	I	R	O	O	H	O	I	O	R	O	F	O	O	I	Bus or Read After Write Error
R	O	R	I	O	R	O	O	H	O	O	X	R	O	O	O	I	O	Transmission Error
R	O	R	F	O	R	O	O	H	O	I	O	R	O	O	O	I	O	Bus or Read After Write Error
R	C	R	I	C	R	O	O	H	O	F	X	R	O	O	O	I	I	Transmission Error
R	C	R	F	C	R	O	O	H	O	I	O	R	O	O	O	I	I	Bus or Read After Write Error

0 = OFF
I = ON
– = NOT APPLICABLE
R = RUN
H = HALT
F = FLASHING (50% Duty Cycle)
B = BLINKING (Halt 95% ON, Run 5% ON)
X = EITHER ON or OFF (2)

NOTES: 1. Run light on LI signifies that LI is operational no matter what error conditions(s) exist within the RI or CPU.

2. The state of the remote channel error light is dependent on which device detected communication error first: On-remote and OFF-local.

Figure 5.3 - LI/RI LED Response to Errors

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LI/RI FAULT STATUS

FAILURE OVERRIDE BIT 13	FREEZE BIT 9	CPU STATUS AFTER FAULT	DROP FAULT								CHANNEL FAULT (Transmission Loss)								PROGRAM HALTED DROP See Notes			
			FAILED DROP				OPERATIONAL DROP				FAILED DROP				OPERATIONAL DROP				HALTED OPERATION DROP			
			LOCAL IMAGE		REMOTE DROP		LOCAL IMAGE		REMOTE DROP		LOCAL IMAGE		REMOTE DROP		LOCAL IMAGE		REMOTE DROP		LOCAL IMAGE		REMOTE DROP	
			INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
0	0	HALT	CLEAR	CLEAR	–	TURN OFF	CLEAR	CLEAR	–	TURN OFF	CLEAR	CLEAR	–	TURN OFF	CLEAR	CLEAR	–	TURN OFF	UPDATE	CLEAR		TURN OFF
0	1	HALT	CLEAR	CLEAR		TURN OFF	LAST STATE	LAST STATE		LAST STATE	LAST STATE	LAST STATE	–	LAST STATE	LAST STATE	LAST STATE	–	LAST STATE	UPDATE	CLEAR	–	TURN OFF
1	0	RUN	CLEAR	CLEAR	–	TURN OFF	UPDATE LADDER	UPDATE LADDER	-	UPDATE LADDER	CLEAR	CLEAR	–	TURN OFF	UPDATE	UPDATE LADDER		UPDATE LADDER	UPDATE	CLEAR	–	TURN OFF
1	1	RUN	CLEAR	CLEAR	–	TURN OFF	UPDATE LADDER	UPDATE LADDER	-	UPDATE LADDER	LAST STATE	LAST STATE	–	LAST STATE	UPDATE	UPDATE LADDER		UPDATE LADDER	UPDATE	CLEAR	–	TURN OFF

NOTES:

1. LI HALT Bit refers to bits 1 to 8 of the LI channel control data register.
2. Regardless of how outputs on a drop get frozen, if communication is re-established, the drop will reset, clear all outputs and local image table information for that drop, and stay in the halted mode until restarted.
3. Restarting the system may be done in any of the following ways.

   A. Toggling the CPU keyswitch.
   B. Power cycling the local (CPU) rack.
   C. Auto Restart function of the LI/RI system.
   D. Pushing the LI Restart button.

   For more detailed information, refer to Section 5.6, LI/RI Communications Restart (Push Button).
4. If the CPU halts its execution due to an error, turning the keyswitch to HALT will not reset frozen outputs on any of the remote drops even if valid LI/RI communication is present.

Figure 5.4 - CPU and LI/RI Response to I/O Faults

1. Toggling the CPU keyswitch out of HALT.
2. Power cycling the power to the local CPU racks while the CPU is in RUN or DISABLE OUTPUTS.
3. Power cycling the remote drops while the Failure Override Bit is ON.
4. Pushing the LI restart push button while the Failure Override Bit is ON and the CPU is in RUN or DISABLE OUTPUTS.

The RESTART button is operational when all the following exists:

1. CPU must be running.
2. Communications error must have originated on one of the LI channels.
3. Failure Override Bit must be ON.
4. Valid communications must be able to be established to the affected racks, or else no change of state will occur.

NOTE: The RESTART button will only restart drops which are shutdown due to communications errors. It will have no effect if a local (CPU) rack error exists.

WARNING: Pressing the RESTART (RESET) button on the front of the LI module may cause outputs to turn ON or OFF.

5.7.1. FROZEN DROP RESET

An operational drop with frozen outputs may be reset by:

1. Power cycling the remote drop.
2. Setting the drop HALT bit ON while the Failure Override Bit is ON and CPU are operational. For more information on how to apply these bits, refer to Appendix D, LI Control/Status Registers.
3. Turning keyswitch to HALT providing the CPU rack is operational, no errors exist.

5.8 CPU and LI/RI Response to Faults

Figure 5.4 depicts how a system will respond to a detected fault condition within the LI/RI portion of the system.

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5.9 Obtaining Additional Assistance

If additional assistance is needed, the following must be available.

1. A concise statement of the problem. Also, determine what the system is actually doing.
2. A physical description of the system indicating the quantities and types of the following:
   A. Inputs and outputs.
   B. Channels.
   C. Drops.
   D. Registers per drop.
   E. I/O per drop.
3. Is this a start-up of a new system or an addition or repair to a previously operable system?
4. How long has the system been operational?
5. Have any overriding control register bits been set?
6. What is the rack addressing as seen on the CRT screen?
7. Check contents of the following registers:
   A. CPU ERROR CODE
   B. LI ERROR CODE
   C. LI CHANNEL CONTROL/STATUS
8. Describe the equipment involved:

	Qty.	Serial Number	Class	Type	Series	Revision
Processor						
Local Interface(s)						
Remote Interface(s)						
Bus Expander(s)						
Rack Assembly(s)						
Register Module(s)						
Communication Module(s)						
CRT Programmer						
Loader/Recorder						
Other Equipment						

Figure 5.5 - Equipment List

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APPENDIX A

A.0 LI/RI UPDATE TIME

A.1 General Information

This appendix provides equations for calculation of the LI/RI update time.

Update time refers to the time required to pass information in either direction between the LI image table and the RI image table.

Update time should not be confused with throughput time. Throughput time is the time required from the actuation of an input until an output action occurs. Throughput time also includes I/O module response time as well as CPU processing time. Further information regarding throughput (overall system response) is covered in the Planning and Installation Guide Instruction Bulletin, 30598-175.

A.2 Channel Update Time

Channel update time is dependent on the update time of the drop with the greatest number of registers assigned to it and the total number of registers on the channel. Therefore, by calculating the update time of that particular drop, the worst case channel update time may be determined.

A.3 Drop Update Time

One of two equations are used to calculate drop update time. For the purpose of these equations, drops will be put into two categories, digital and register. The digital drop is a pure digital drop (8 or less registers*) with no register modules. While the register drop will contain register modules or a combination of register and digital modules.

* For 9 or more registers, use register drop equations.

A.4 Update Time Equation Variables

D = Total digital drops on the channel. (0-8)
R = Total register drops (or digital/register drops) on the channel. (1-8)
DR = Total register addresses assigned to all digital drops. (0-64)
RR = Total register addresses assigned to all register drops. (1-255)
X = Register addresses assigned to the drop being evaluated. (1-8) If more than 8 registers are assigned, use X = 8.

Note that actual performance times may be better than calculations for channels with many registers.

A.5 Drop Update Time Equations

Use this equation for a channel with only digital drops.

Digital Channel Drop Update Time (ms)
$= 2.31D + DR + X + 0.79$

Use this equation for all other remote I/O channels.

Register Channel Drop Update Time (ms)
$= 2.31D + DR + 3.15R + 1.24(RR + X) + 1.52$

A.6 Example #1

This example works out the drop update time for a purely digital channel. This example has the following relevant attributes.

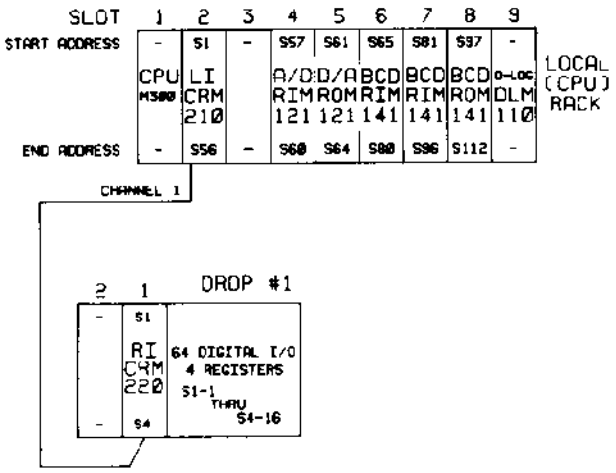


Figure A.1 - Digital Channel

CHANNEL 1 Consists of one drop and 4 registers.
DROP #1 Consists of 4 registers used for digital I/O.
CHANNEL 2 Not used.

Channel 1 Digital Drop Update Time
$= 2.31D + DR + X + 0.79$
$= 2.31(1) + (4) + (4) + 0.79$
$= 11.1$ ms

A.7 Example #2

This example works out the drop update time equation for a combinational (register) channel.

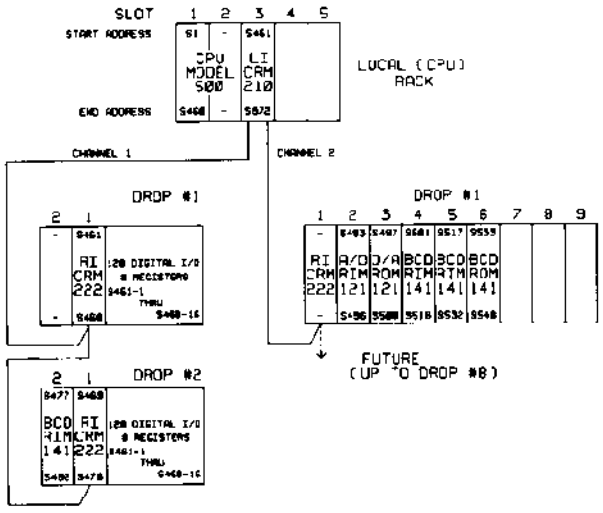


Figure A.2 - Register Channel

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CHANNEL 1 Consists of two drops and 32 registers.

DROP #1 Consists of 8 registers used for digital I/O.
DROP #2 Consists of 24 registers, some used for data storage.
CHANNEL 2 Consists of one drop and 56 registers

DROP #1 Consists of 56 registers used for data storage.

Note that only the register drop update time equations can be used since neither channel has only digital drops.

Channel 1 Drop Update Time

$$= 2.31D + DR + 3.15R + 1.24(RR + X) + 1.52$$
$$= 2.31(1) + (8) + 3.15(1) + 1.24(24 + 8) + 1.52$$
$$= 54.7\text{ms.}$$

Channel 2 Drop Update Time

$$= 2.31D + DR + 3.15R + 1.24(RR + X) + 1.52$$
$$= 2.31(0) + (0) + 3.15(1) + 1.24(56 + 8) + 1.52$$
$$= 84.0\text{ms.}$$

A.8 Register Optimization

By allocating only the number of registers which will be used by a register module, channel update time can be minimized. For example, if only five of the 16 registers of a RIM 141 BCD Output Module are actually needed, assign only five. This register reduction of 16 to 5 will result in a 15ms channel update time savings.

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APPENDIX B — ERROR CODES

B.1 Introduction And Description

B.1.1 GENERAL INFORMATION

Errors detected by the processor and error codes annunciated on the CRT provide the operator with information useful in isolating problems.

Some errors are indicated as messages on the screen display while other error indications involve error code numbers. Since the messages are self explanatory, this appendix deals directly with the numbered error codes.

These error code numbers can be broken into two general categories and are indicated in different locations on the CRT screen.

In the first category are the **peripheral to PC system** interaction errors of which 3 classifications of error codes exist. These errors are indicated at the bottom of the screen display or for some special cases, in the status register of a communications rung.

In the second category are the **PC system operational errors** which are errors detected within the processor or any one of the modules contained in a programmable controller system. These errors are indicated in the STATUS Mode display next to the label ERROR NUMBER. The number displayed is also the number contained in the error code control register 8175 or possibly in a Local Interface Module error code control register (when using remote I/O).

B.1.2 PERIPHERAL TO PC SYSTEM INTERACTION ERRORS

These types of errors are associated with attempts to perform illegal operations with the processor or the communication hardware is not functioning properly. This category of error will only be generated when using the keyboard to command processor operations or when the processor is attempting communication with other responding devices.

The three classifications of peripheral to PC system interaction error codes are: Processor, Transmission, and Tape. When an error occurs while a programmer is connected to the processor, one of these messages will be shown on the display along with a number. Should an error occur during the execution of a processor communication rung a Processor Error will be used to indicate the fault. The number code will be shown when the status register of the communication rung is displayed.

Processor Errors

These errors indicate that the operation attempted was not successfully completed. The error code numbers range from 01 thru 99. To resolve the error situation, check the error code description in the following table, use the CLEAR key to clear the error indication if the error has been displayed on a programmer, and take the appropriate recourse action. Error codes indicated by an asterisk (*) in the following Error Code Table, may also be displayed in the status register of a communications rung.

PROCESSOR ERROR CODE TABLE

Error Code No	Error Description
01*	Illegal protocol opcode, the device does not recognize the instruction. Reenter the desired operation.
02	Illegal intermediate code format. Reenter the desired operation.
03*	An illegal address has been attempted.
04	Illegal rack addressing has been attempted.
05*	An instruction has been attempted which is not allowed in the processor. (Example: Square root in Model 300 processor.)
06	Item being searched for cannot be found.
07*	An attempt has been made to alter data in a protected register. Check Control Register 8176.
08	An attempt has been made to access protected memory. Check Control Register 8176.
09*	An attempt has been made to alter data in a READ only register or a register containing external inputs.
10	An attempt has been made to exceed memory limitations.
11*	Communications error (receiver overflow). Reenter the desired operation.
12	Illegal CPU rack addressing; Register assignments must be divisible by four.
13*	Communications error (link error). This error is generated by the processor. Check Control Register 8175 or the status register of the communication rung. Check cable connections between devices.
14	The operation that has been attempted is not allowed in RUN.
15*	Communication overflow. Check the baud rate for compatibility between communicating devices. Reenter the desired operation.
16	The register count in a communication rung is too large for the processor.
17*	The remote device is inactive. This error code is generated by the Network Interface Module. Check cable connections between devices.
18	The rung number used is not allowed.
19*	An illegal READ parameter has been assigned.
20	An illegal channel number, or no channel number has been assigned.
21*	Trying to change a forced bit or WRITE to an external output while the processor is in HALT.
22	The forcing function is inhibited from the processor COMM port.
23*	An attempt has been made to alter data in a fenced register.
24	An attempt has been made to force a nonforceable register.

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25*	CPU error, check Control Register 8175. Refer to the following section on CPU/LI errors.
26	Rack Addressing and user memory overlap.
27*	Memory error. A CLEAR ALL operation is required.
28	An illegal baud rate was selected.
29*	An attempt has been made to send a message with an illegal route.
30	An attempt has been made to alter PROM memory after the PROM inhibit coil was entered in memory.
31*	See **Tape Errors**
32	Operation is not allowed in PROM memory (such as inserting, deleting, or replacing a rung).
33*	See **Tape Errors**
34	For UVPROM processors only: Read after Write error; parity error; or security jumper was removed and no UVPROM inhibit coil was programmed into memory.
35*	See **Tape Errors**
36	Replace rung operations are not allowed on this rung. Use delete and insert operations only.
37*	See **Tape Errors**
38	Unused
39*	Alarm already set within the D-LOG Module.
40	Unused
41*	An illegal register WRITE. The D-LOG module does not accept a register WRITE into certain registers.
42	Unused
43*	An illegal operation has been attempted. D-LOG Module protected.
44	Unused
45*	Operation is not allowed. D-LOG Module tape operation is in progress.
46	Unused
47*	Operation is not allowed due to keyswitch position.
48	Programming of an MCR in subroutine area is not allowed.
49	I/O, Register or Channel is safeguarded; used in Type SCP-544 RAM/PROM Processor — see Appendix E.
50	Rack Addressing is not alterable when forcing is active.
51*	A module is not seated properly or missing, or no rack address assigned to the module, or the address exceeds the capability of the processor.
52	Unused
53*	See **Tape Errors**
54	Illegal MARK number.
55	See **Tape Errors**
56	Unused
57	Unused
58	Unused
59	Unused
60	Illegal MARK number. GOTO or GOSUB with numbers above 8189 not allowed.
61	MARK ST. SUB rung cannot be inserted-append only allowed.
62	RTN (return) rungs are not allowed in ladder area.
63	MARK number previously used in the program. Each MARK instruction must have a unique number assigned.
64	Operation is not allowed while the processor is in RUN. Cannot delete a RTN if any GOSUB contains the same MARK number.
65	Operation is not allowed. Cannot delete MARK ST. SUB rung unless all subroutines are deleted.
66	Operation is not allowed — cannot delete MARK having an associated RTN (return).
67	Operation is not allowed — RTN rungs must have an associated MARK number.
68	Operation is not allowed — only one RTN per MARK number is allowed.
69	Operation is not allowed while the processor is in RUN — GOSUB cannot invoke a subroutine having no RTN.
70	Operation is not allowed while the processor is in RUN — GOTO rung cannot jump to a MARK having an associated RTN.
71	Operation is not allowed while the processor is in RUN — cannot delete MARK until all GOSUBs or GOTOs with the same number are deleted.
72	Operation is not allowed while the processor is in RUN — rung cannot have unused MARK number. A GOTO or GOSUB with an undefined MARK is not allowed. The MARK must be programmed before the GOTO or GOSUB is programmed.
73	Unused
74	Unused
75	Unused
76	Unused
77	Unused
78	Unused
79	Operation is not allowed when the processor is in RUN while the Timed Interrupt is enabled.

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Tape Errors

These errors are generated when performing tape operations. When the processor is operating with a Loader/Recorder through the use of communications rungs, the status register of that rung can be checked for the presence of an error condition.

Error Code No.	Error Description
31*	The end of the tape was encountered before the operation could be completed.
33*	Tape Data Error detected, the block of data involved in the Read or Write operation was faulty.
35*	The tape cartridge is not seated properly or is missing, or the "Record" tab on the cartridge has been set to the Write Inhibit position.
37*	An attempt to Skip or Read a file was made when already past the last file on the tape.
53*	Illegal Tape Format — Erase Track Required.
55*	Tape operation has been aborted. Retry the operation.

Transmission Errors

Communication errors due to hardware problems are annunciated on the CRT screen by the message "Transmission Error" followed by a number.

The error code numbers that appear are the numbers 1, 72, and 74. When an error such as this occurs, check all cable connections and BAUD rates (Register 8169), then use the CLEAR key to clear the error indication. When all connections are secure, retry the operation.

B.1.3 PC SYSTEM OPERATIONAL ERRORS

These error codes indicate PC system operational errors and consist of a five digit decimal value. These error codes or (ERROR NUMBERS) are the contents of the Control Register 8175 data field (bits 1-16). Seven possible classifications of operational error codes exist and they are:

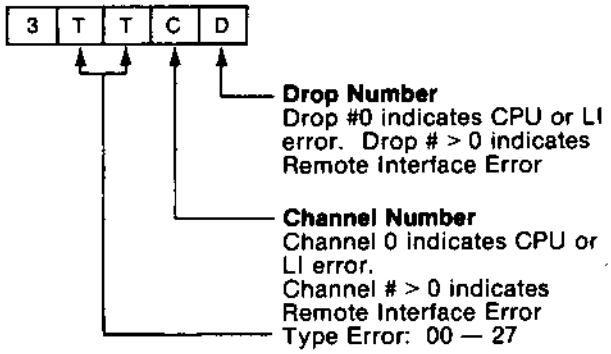
ERROR NUMBER	TYPE OF ERROR
30000-32700	CPU/LI ERROR
29000-29999	MISCELLANEOUS ERROR
20000-28192	SLOT REGISTER ERROR
19000-19016	SLOT ERROR
10000-18192	READ AFTER WRITE ERROR
01000-09999	PROCESSOR COMMUNICATION PORT ERROR
00001-00999	GENERAL ERROR

When an error condition occurs, the appropriate error code is loaded into Control Register 8175 only if the register contains zero of ir it presently contains an error code of lower priority (a smaller number). The previous error code is then lost (if a Model 300) or moved to Register 8183 (if a Model 500 or 700).

The same operational errors are used by the Local/Remote Interface systems to indicate errors in devices under its control. In this case, Register 8175 or the ERROR NUMBER in the CRT Status display will indicate the slot of the Local Interface having the problem. Once located, inspection of the error control register inside the Local Interface will reveal which of the remote devices contains the error. Refer to Section B.2 for greater detail on using the error codes to isolate system faults.

CPU/LI Error (30000-32700)

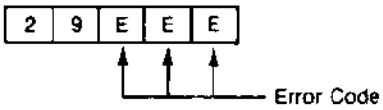
This error indicates a problem with either the processor (CPU) or Local Interface Module.



TT	ERROR DESCRIPTION
00	Status Register Read/Write Parity Error
01	Image RAM Read/Write-Parity Error
02	Internal Register Data Error
03	Illegal PROM Format
04	Illegal Opcode Encountered in RUN
05	Bus Error Signal Error
06	Software Watchdog Error
07	Not Used
08	Not Used
09	User Memory Read/Write-Parity Error
10	Illegal Data in User Memory
11	PROM Memory Corrupted
12	Illegal Addressing Map Code
13	Transmission Error Exceeds Tolerance
14	Loss of Transmission
15	More External I/O Registers Assigned Than Module Can Handle
16	Too Many Registers Assigned to the Drop
17	Addressing More than 8 Drops per Channel
18	Addressing Number of Channels Exceeded Module Capabilities
19	Addressing Map Checksum Error
20	Bus Error — Watchdog Time Out
21	BPU Diagnostic Error
22	Parity Circuit non-functional
23	Clear Line Error
24	Executive Scratch RAM Error
25	Watchdog Tolerance Error
26	Hardware Diagnostic Error
27	Module Inactive

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Miscellaneous Errors (29000-29999)



EEE	Error Description
000	Subroutine Nesting Error.•
100	Time to Process the Timed Interrupt Subroutine has Exceeded the Time Base.•
101	Timed Interrupt Routine Missing.
102	Time to Solve a Rung has Exceeded the Tolerance Set Within a Timed Interrupt.•
201	MCU Software Mismatch with LCU.
202	LCU Software Mismatch with MCU.
300	Mixed Primary-Backup LTIs in CPU Rack.*
301	LTI Timeout on EOS Transfer. ■
302	LTI Timeout on Start-Up Transfer.■
500	Number of Assigned Local Transfer Interface Registers must be at least 8 for 1 defined channel, 12 for 2 defined channels.
501	Insufficient Local Transfer Interface Control.
510	RTI Wired Improperly - Channels A and B are mixed.
511	LTIs in CPU racks A and B have equal states of operation and no primary determination can be made in HALT.
512	Backup Transfer System cannot be in RUN when Primary Transfer System is in DISABLE OUTPUTS.
513	Rack Addressing between LTIs in racks A and B (Primary and Backup) are not the same.
514	Backup cannot be in run with Test bit set when Primary goes to HALT. Backup must also go to HALT.
515	Backup cannot become Primary until synchronization has occurred and Primary goes to HALT.
516	Backup unable to become Primary because remote bus error exists. Also error generated by Primary to allow transfer to Backup when Primary keyswitched to HALT.
517	Backup has lost synchronization and does not have RTC FAILURE OVERRIDE bit set.
518	Two Primary processors were found in RUN; this processor was halted with a bus error.

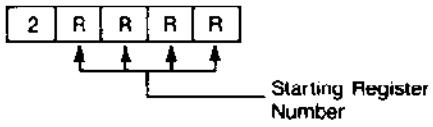
- Control Register 8184 will contain the rung number where the error took place. If 8184 equals zero, check Rack Addressing.

* The data field of Control Register 8184 contains the bit table of primary or back-up status (bit set indicates primary) while the status field of Control Register 8175 identifies the slots which contain LTIs (bit set indicates LTI present).

■ The data field of Control Register 8184 identifies the first register assigned to the LTI that caused the error while the status field of Control Register 8175 contains the elapsed time (in msec.) that the scan was held.

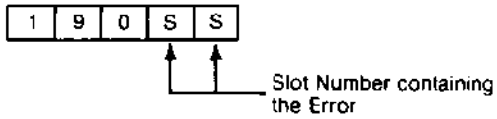
Slot Register Error (20000-28192)

In the event of a Slot Register Error, the ERROR NUMBER (last four digits) will point out the first register number assigned to the slot containing a faulty register module. Further inspection of that register's status field will provide additional diagnostics.



Slot Error (19000-19016)

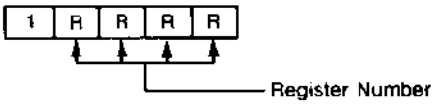
In the event of a Slot Error, the ERROR NUMBER will point out the slot number experiencing the error.



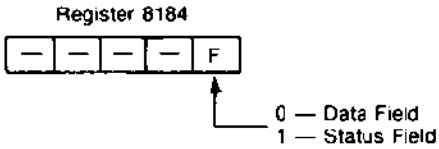
NOTE: ERROR 19000 same as ERROR 32000.

Register Read After Write Error (10000-18192)

A read after write error indicates a particular bit in a register has not maintained the condition written to it by the processor. The error number (last four digits) will point out which register encountered the problem.



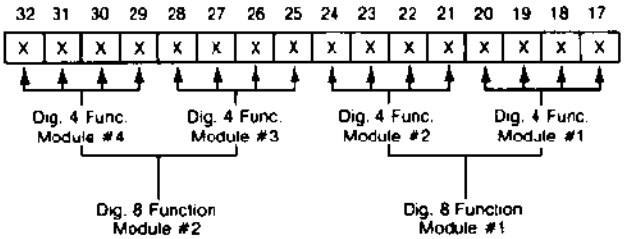
By displaying the status field (bits 17-32) of the control register containing the error code, the bit or bits causing the malfunction will be indicated (by a 1). Since each register contains both a status field and a data field, control register 8184 is used to indicate which set of bits contains the problem.



If the faulty register is used to control outputs and control register 8184 indicates the bad bits are contained in the data field, most likely, an output module has caused the problem. Following is a diagram which can be used to isolate the output module having the problem.

In addition, note that a parity error can also be detected in a register and is indicated by a zero in all bit positions.

Status Field of Control Register 8175 or of Local Interface Error Code Control Register



Checks:

a. If X=0, Bit was read correctly.

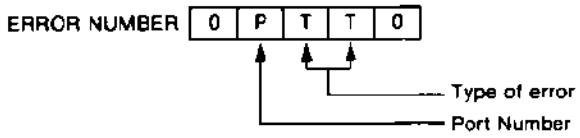
b. If X=1, Bit was read incorrectly.

c. If all X's=0, Parity error was detected.

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Processor Communication Port Error (01000-09999)

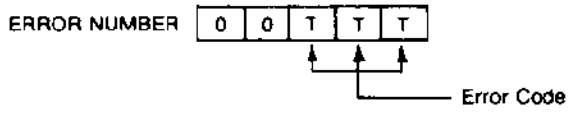
To clear a communication port error, toggle the processor keyswitch from HALT to RUN, or Clear S8175. If this does not clear the error, cycle power to the processor. These errors can be seen in the STATUS Mode Display by the ERROR NUMBER. Also check remote device and cable connections.



TT	ERROR DESCRIPTION
11	Communications overflow.
12	Buffer overflow.
13	Illegal data.
14	Wrong reply (odd/even).
15	Checksum error.
16	Framing error.
17	Parity error.
18	Inability to communicate thru Port #P.
19	Retry timeout.

General Errors (00001-00999)

The ERROR NUMBER in the Status Display indicates the problem.



TTT Error Code	Error Description
900	Control registers corrupted.*
901	Data registers corrupted.*
902	Undervoltage lockout is engaged.
960	HALT or HALT/RUN bit set.
962	Tolerance equal to or greater than the rate.
963	Timed Interrupt time base is less than 3.
964	GOTO and GOSUB to same MARK.***
965	Illegal Internal Error Code.
966	User Subroutine Stack Error.***
967	A MARK rung with the same reference number is required.***
968	GOTO to MARK with RTN (return).***
969	GOSUB to MARK with no RTN (return).***
970	Scan Time of processor is greater than 1 second or scan limit in S8167 has been exceeded.**
971	Scan Time limit of processor has been exceeded due to long LTI start-up transfer. (Check register 8184 for elapsed time in msec.)
979	Rack Addressing missing.
980	Keyswitch in RUN and no program in memory.
981	PROM inhibit coil not in memory (PROM processor).
983	Safeguarding rung not in memory or programmed incorrectly.
984	Undefined register programmed in user memory.**

* Control registers are normalized and data registers are cleared. Toggling keyswitch will allow CPU to run.

** S8184 will contain the rung number being executed when the error occurs.

*** S8184 will contain the MARK number.

B.2 Using Error Codes To Isolate P.C. System Faults

B.2.1 GENERAL CONCEPT

When a P.C. system, which was once operating correctly malfunctions, one of three situations can arise: either the whole P.C. system shuts down, one or more drops shut down, or a run time communication port error is detected. Once the malfunction is identified as existing in one of these three categories, the P.C. SYSTEM OPERATIONAL ERROR CODES can be used to isolate the fault. Recognition of the first category is obvious however, the second category can exist only when the P.C. system incorporates remote I/O and the override bit is set in the Local Interface Module.

The third category of malfunction deals with communications to external devices and requires that control register 8175 be monitored by the program for errors in the range 01000 to 09999. These types of errors are different from those described in the "Processor Errors" section in that they are generated by the processor itself and not by the external device.

B.2.2 WHEN THE SYSTEM SHUTS DOWN

When the processor halts, register 8175 should be the first point of interrogation. The error code indicated will be one in the following number ranges:

ERROR CODE	DESCRIPTION
30000-32700	CPU/LI Error
29000-29999	Miscellaneous Error
20000-28192	Slot Register Error
10000-18192	Read After Write Error
00001-00999	General Errors

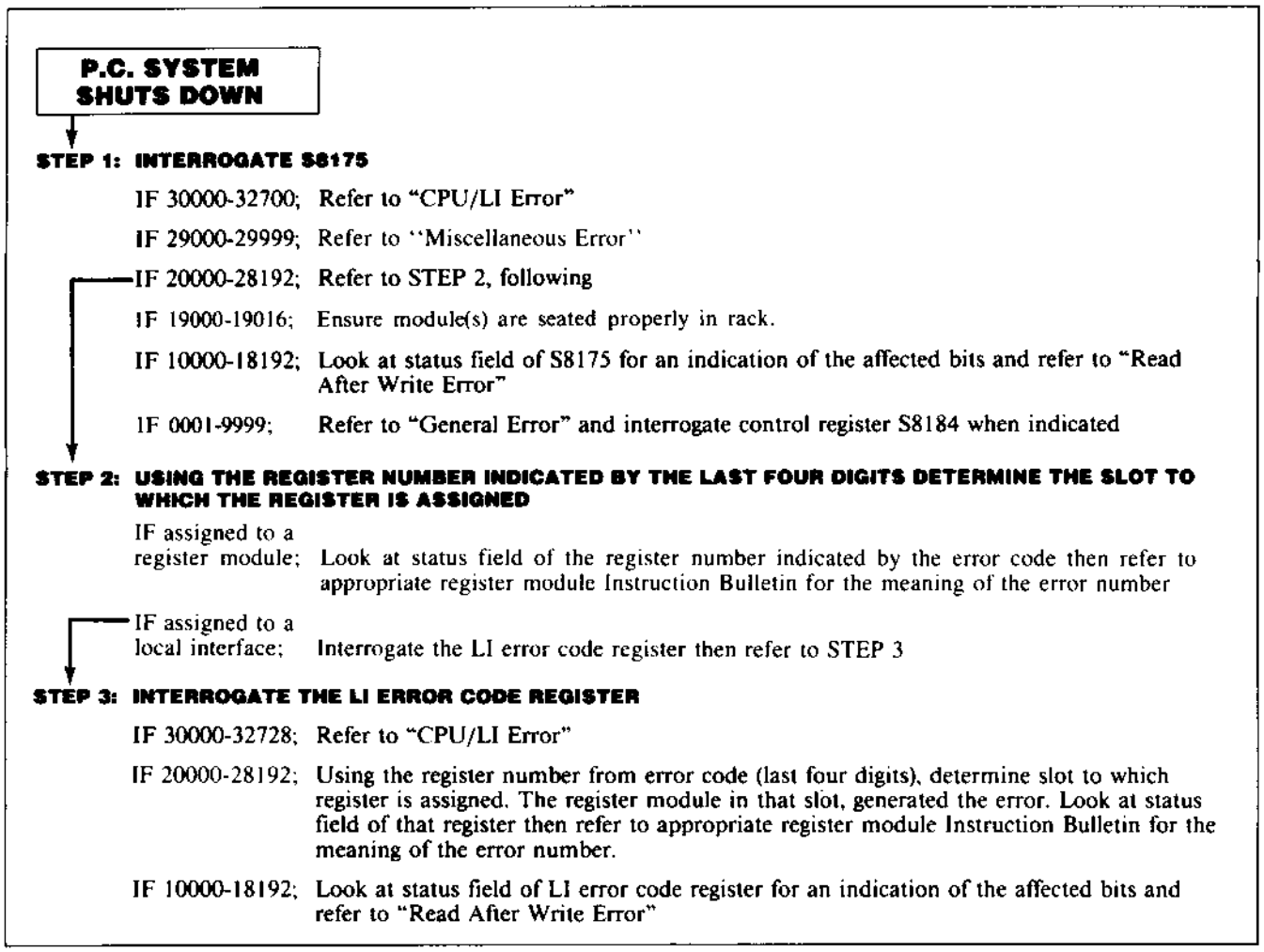
In the case of the 20000-28192 Slot Register Errors two courses of action may be taken depending on the register number indicated by the last four digits. If the register is the first assigned to a register module, interrogating the status field of that register will indicate the error. (Refer to appropriate register module Instruction Bulletin.) If the register number is the first assigned to a Local Interface Module (when using remote I/O), then further interrogation of the LI error code register is required. (Refer to Appendix D to determine the address of the LI error code register/s.) When the LI error code register is interrogated, the number will be in the following ranges:

LI ERROR CODE	DESCRIPTION
30000-32728	CPU/LI Error
20000-28192	Slot Register Error
10000-18192	Read After Write Error

In the case of the 10000-18192 Read After Write Errors, the affected bit or bits are indicated in the status field of the LI error code register.

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Following is a flow chart which illustrates the previously described procedure.



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EXAMPLES:

Shown is an arbitrary P.C. system configuration with four different fictitious malfunctions (which are not the only ones possible) marked by numbers. Following are the steps one would go through to isolate each type of problem (based on the previous flow chart). The four problem areas are the:

— CPU
— Local Register Module
— Remote Register Module
— Remote I/O Module

FOUR P.C. SYSTEM MALFUNCTIONS

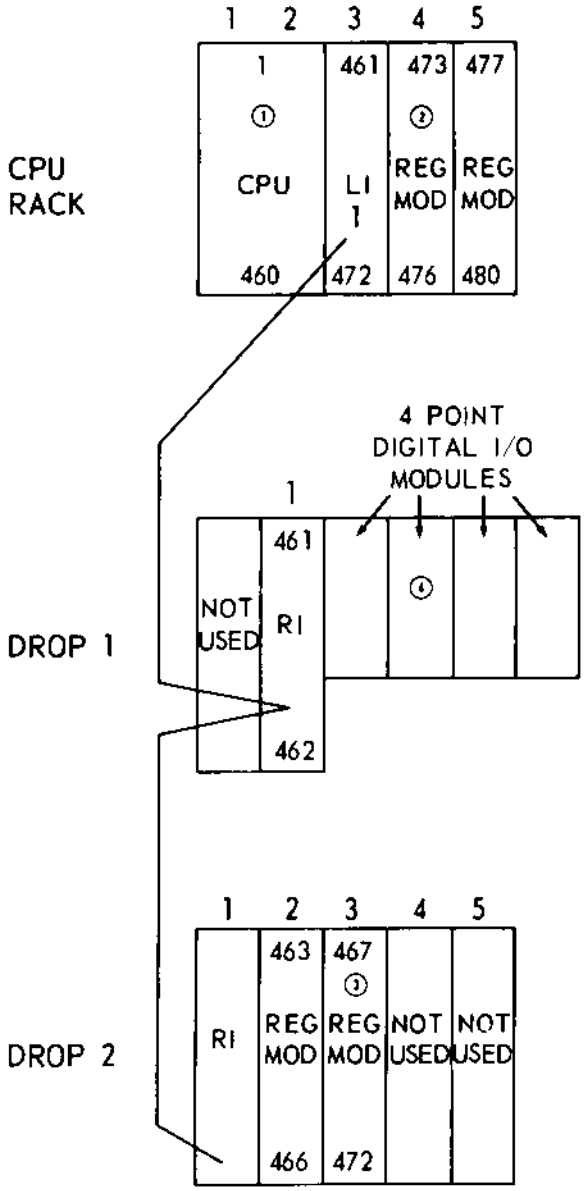


Figure B.1 — A Typical P.C. System

*NOTE: Arbitrary register assignments have been added to this diagram to aid in the following explanation.

1. Malfunction in CPU

   A malfunction in the CPU would cause the system to shut down therefore the "P.C. System Shuts Down" flow chart should be used.

Result of STEP 1: Since a malfunction in the CPU itself, caused the system to shut, interrogating control register 8175 would result in an error code in the range of 30000-32700. By referring to the "CPU/LI Error" section the specific error can be determined.

2. Malfunction in a Local Register Module (Located in CPU Rack)

   A major malfunction in a register module located in the CPU rack would cause the system to shut down, therefore the "P.C. System Shuts Down" flow chart should be used.

Result of STEP 1: Interrogating control register 8175 would result in a 20473 error code.

Result of STEP 2: The error code indicates the register module in slot four of the CPU rack has malfunctioned since it is the module containing register 473 as the first register address. By looking at the status field of register 473 and then referring to the appropriate register module Instruction Bulletin, the specific error can be determined.

3. Malfunction in a Remote Register Module

   A malfunction in a register module located in a remote rack will cause the total system to shut down if the override bit in the local interface module (LI) is **not** set. If this is the case, the "P.C. System Shuts Down" flow chart should be used.

Result of STEP 1: Interrogating control register 8175 would result in a 20461 error code.

Result of STEP 2: The register number indicated in the error code is 461, which is the first register in the LI. Interrogating the LI error code register (in this case 8163) will provide additional information as to which module in the remote I/O system caused the shut down.

Result of STEP 3: Interrogating the LI error code register (8163 in this case) would result in a 20467. Since the register module in DROP two SLOT three contains register 467, that module is responsible for the system shut down. By looking at the status field of register 467 and then referring to the appropriate register module Instruction Bulletin, the specific error can be determined.

4. Malfunction in a Remote I/O Module

   A malfunction in an output module located in a remote rack will cause the total system to shut down if the override bit in the local interface module (LI) is **not** set. If this is the case, the "P.C. System Shuts Down" flow chart should be used.

Result of STEP 1: Interrogating control register 8175 would result in a 20461 error code.

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Result of STEP 2: The register number indicated in the error code is 461, which is the first register in the LI. Interrogating the LI error code register (in this case 8163) will provide additional information as to which module in the remote I/O system caused the shut down.

Result of STEP 3: Interrogating the LI error code register (8163 in this case) would result in a 10461. Looking at the status field of 8163 will provide the bit mask, indicating which output module associated with register 461 caused the failure.

B.2.3 WHEN A REMOTE RACK SHUTS DOWN

When the P.C. system incorporates remote I/O and a remote rack or racks halts without causing the rest of the system to halt, the error code register of the Local Interface module controlling that drop will contain the error number of the fault. When the LI error code register is interrogated, the number will be in the following ranges:

LI ERROR CODE	DESCRIPTION
30011-32728	CPU/LI Error
20000-28192	Slot Register Error
10000-18192	Read After Write Error

In the case of the 10000-18192 Read After Write Errors, the affected bits are indicated in the LI error code register.

Following is a flow chart which illustrates the previously described procedure.

EXAMPLES:

Using the malfunctions three and four in Figure B.1 as examples, following are the steps one would go through to isolate each type of problem (based on the previous flow chart). The two problem areas are the:

— Remote Register Module
— Remote I/O Module

1. Malfunction in a Remote Register Module

   A malfunction in a register module located in a remote rack will cause just that rack (drop) to shut down only if the override bit in the local interface module (LI) is set. If this is the case, the "Remote Rack/s Shuts Down" flow chart should be used.

   Result of STEP 1: Interrogating the LI error code register (8163 in this case) would result in a 20467. Since the register module in DROP two slot three contains register 467, that module is responsible for the system shut down. By looking at the status field of register 467 and then referring to the appropriate register module Instruction Bulletin, the specific error can be determined.

2. Malfunction in a Remote I/O Module

   A malfunction in an output module located in a remote rack will cause just the rack (drop) to shut down only if the failure override bit in the interface module (LI) is set. If this is the case, the "Remote Rack/s Shuts Down" flow chart should be used.

   Result of STEP 1: Interrogating the LI error code register (8163 in this case) would result in a 10461. Looking at the status field of 8163 will provide the bit mask indicating which output module associated with register 461 caused the failure.

B.2.4 PROCESSOR COMMUNICATION PORT ERROR DETECTED

These errors are different from those Processor Errors associated with communications listed earlier in this appendix. The difference is that Processor Communication Port Errors are detected by the processor rather than the external communicating device. The only Processor Error that has any relationship to Processor Communication Port Errors (01000-09999) is Processor Error code 13. When error 13 is indicated in a status register of a communication rung, interrogation of control register 8175 will result in the display of one of the Processor Communication Port Errors (01000-09999).

These errors can also be detected when an external device is asking for information from the local processor. In this case, there is no communication rung status register to indicate the fault. Therefore, it is up to the user to implement the means to annunciate these types of errors.

REMOTE RACK(S) SHUTS DOWN

↓

STEP 1: INTERROGATE APPROPRIATE LOCAL INTERFACE ERROR CODE REGISTER

IF 30000-32728; Refer to "CPU/LI Error"

IF 20000-28192; Using the register number from error code (last four digits), determine slot to which register is assigned. The register module in that slot, generated the error. Look at status field of that register then refer to appropriate register module Instruction Bulletin for the meaning of the error number.

IF 10000-18192; Look at status field of LI error code register for an indication of the affected bits and refer to "Read After Write Error"

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APPENDIX C

C.0 CHANNEL EXPANSION

C.1 General Information

This appendix provides information to expand an LI/RI system. Expansion may be accomplished in two ways. The first consists of adding to an existing drop, while the second is to add an additional drop.

Regardless of what type of expansion method is used, the user must develop and enter the ladder logic program for the newly added I/O points. For the specific programming procedures, refer to the CRT Programmer Instruction Bulletin.

C.2 I/O Expansion Considerations

1. The additional I/O must fit within the processor (CPU) addressing capability.

2. The additional I/O must be able to be supported by the existing LI, if not, an additional LI module(s) will be required.

   Note: Model 300 can support 1 LI only.

3. Expansion of a physical drop requires that external registers are available for use at that location by either a result of:

   A. Previously allocated address assignments.

   B. A reallocation of addresses.

4. The addition of more registers on a channel will increase the LI/RI update time. However, if the register(s) were previously on that channel, the LI/RI update time should not be significantly increased by additional drops.

The following is a brief description of the two basic expansion alternatives, drop expansion and drop addition.

C.3 Drop Expansion

Drop expansion by a mere addition of hardware alone can be accomplished if, and only if, the previously entered rack addressing allows for it. Therefore, the current system configuration and the defined rack addressing has to be reviewed when contemplating expansion of an existing PC system.

Expansion can be accomplished in one of two ways:

1. Replace the existing rack with a larger assembly.

2. With a four function digital I/O rack assembly, an expander module (class 8030 Type CRM-115/116) may be used to add a second Digital I/O rack to the drop.

C.4 Drop Addition

Adding a drop can be performed at any time within the limitations of the CPU and LI(s) being used.

The mere addition of the hardware to support a drop to an existing LI channel alone will not make a drop operational.

Alteration of the existing rack addressing assignments and associated ladder program most likely will be required.

WARNING: Care must be taken when altering existing rack addressing. Automatic shifting of addresses will occur from the point of alteration. Registers may be changed to locations which were not intended by the designer to be used as I/O points, thus possibly causing unexpected control action to occur.

Once hardware and software modifications are started, complete and verify that they are correct before putting the system into Run or Disable Outputs.

For information on how to alter rack addressing assignments, refer to the CRT Programmer Instruction Bulletin.

When adding a drop or changing rack addressing for a specific channel, the LI/RI update time may be altered. Refer to Appendix A, LI/RI Update Time for more detailed information.

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APPENDIX D

D.0 LI CONTROL/STATUS REGISTERS

D.1 General Information

Control registers 8001 through 8163 (contained in the processor) are used to monitor, and in some cases, control the Local/Remote Interface (LI) system. Not only is the condition of the LI system reflected in these control registers, but information pertaining to register modules and I/O modules is also located in these registers.

The CRM-210 and CRM-211 are two channel LI modules in which three registers are used to communicate directly with the processor (CPU). The first register is an error code control register. The second is a control register for channel 1 and the third is a control register for channel 2.

The number of control registers used to monitor a particular LI system is based on the number of local interfaces used in the system and the number of channels included in each local interface. Each register consists of two parts known as the status field and data field. The data field can be programmed by the user for control functions. The status field, as the name implies, is used just to monitor status of specific system conditions.

D.2 Register Allocation

For the first LI Module in a system, the error code control register is S8163. The channel control registers are S8162 for channel 1 and S8161 for channel 2.

The following is a listing of the error control and channel registers for systems using both channels on each LI up to 7 LI modules.

The contents of the error code control registers are discussed in greater detail in Appendix B, Error Codes. The format for the control data and status follow.

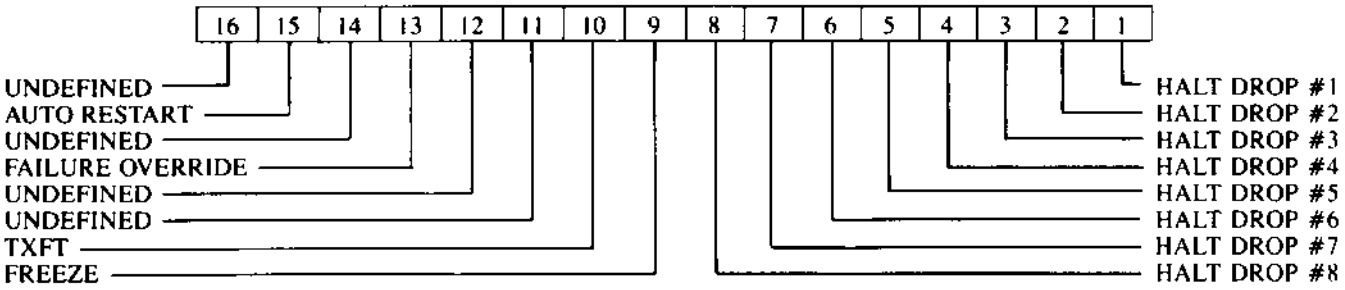
REGISTER	L.I.	LOCATION	FUNCTION
S8163	First	(Right of	Error Code
S8162	First	CPU)	Channel 1 Control Data and Status
S8161	First*		Channel 2 Control Data and Status
S8160	Second*	(Right of	Error Code
S8159	Second*	first LI	Channel 1 Control Data and Status
S8158	Second*	module)	Channel 2 Control Data and Status
S8157	Third*	(Right of	Error Code
S8156	Third*	second LI	Channel 1 Control Data and Status
S8155	Third*	module)	Channel 2 Control Data and Status
S8154	Fourth*	(Right of	Error Code
S8153	Fourth*	third LI	Channel 1 Control Data and Status
S8152	Fourth*	module)	Channel 2 Control Data and Status
S8151	Fifth*	(Right of	Error Code
S8150	Fifth*	fourth	Channel 1 Control Data and Status
S8149	Fifth*	LI module)	Channel 2 Control Data and Status
S8148	Sixth*	(Right of	Error Code
S8147	Sixth*	fifth LI	Channel 1 Control Data and Status
S8146	Sixth*	module)	Channel 2 Control Data and Status
S8145	Seventh*	(Right of	Error Code
S8144	Seventh*	sixth LI	Channel 1 Control Data and Status
S8143	Seventh*	module)	Channel 2 Control Data and Status

* Indicated LI register assignments may vary, dependent upon LI position and rack addressing assignments. Control registers are dynamically assigned in accordance with rack addressing and not solely based upon LI count. For more information, refer to Section 4.3.3, LI Control Register Allocation.

Figure D.1 - LI Control/Status Register Assignments

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D.3 Local Interface Module Control Data Register

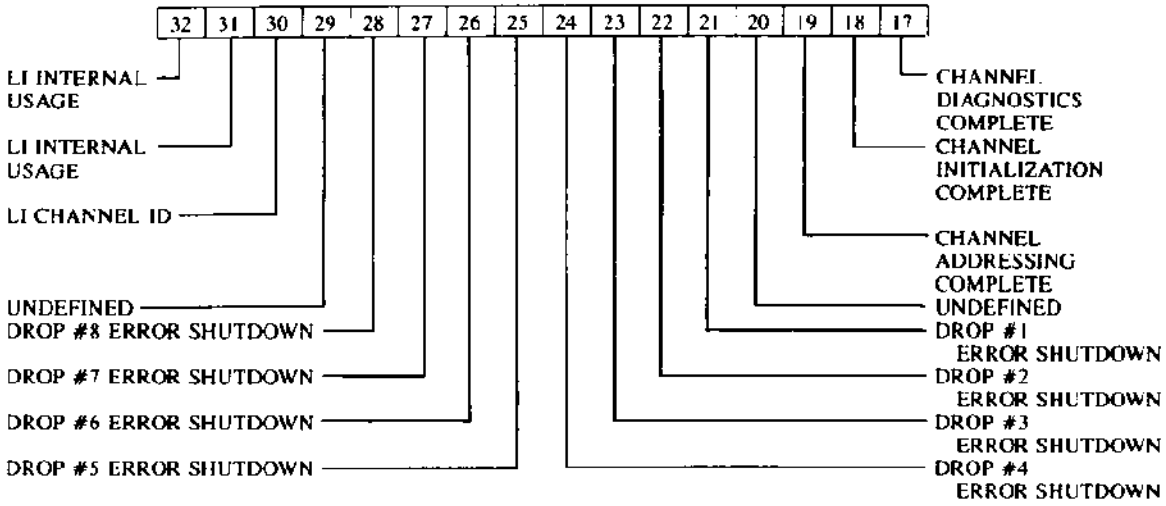


Channel Control Register Bit	Name	Description
1 2 3 4 5 6 7 8	HALT DROP #1 HALT DROP #2 HALT DROP #3 HALT DROP #4 HALT DROP #5 HALT DROP #6 HALT DROP #7 HALT DROP #8	When OFF (0) the drop will operate as the ladder logic indictates. When ON (1) the drop will be shutdown. 1. Input status still valid 2. Outputs turn OFF 3. Register I/O clear (depending upon module type)
9	FREEZE	When ON (1) and a loss of transmission or transmission error or local rack error occurs, all outputs are maintained in their last state.
10	TXFT	Transmission Fault Tolerance determines whether 3 or 10 consecutive transmission errors occur before a channel error is acknowledged. OFF(0) = 3 errors ON(1) = 10 errors
11	Undefined	
12	Undefined	
13	FAILURE OVERRIDE	When ON (1) allows the channel to continue operating if a drop error on the channel occurs. When OFF (0) and drop error is present, channel will shutdown and processor will halt.
14	Undefined	
15	AUTO RESTART	When ON (1) allows the channel to attempt to re-establish valid communications with any drop shutdown due to transmission errors. (Bit 13 must be set to enable bit 15 to be recognized.) This control bit accomplishes a similar function as the restart button on the LI module.
16	Undefined	

Figure D.2 - LI Control Data Register

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D.4 Local Interface Module Control Status Register (Read Only)



Channel Control Register Bit	Name	Description
17	Channel Diagnostics Complete	When ON (1) LI channel completed its diagnostics.
18	Channel Initialization Complete	When ON (1) 1. RIs have completed their diagnostics 2. Valid LI/RI communication 3. Image table updating sequence complete
19	Channel Addressing Complete	When ON (1), indicates the CPU has loaded valid rack addressing information into the LI.
20	Undefined	
21 22 23 24 25 26 27 28	DROP #1 ERROR SHUTDOWN DROP #2 ERROR SHUTDOWN DROP #3 ERROR SHUTDOWN DROP #4 ERROR SHUTDOWN DROP #5 ERROR SHUTDOWN DROP #6 ERROR SHUTDOWN DROP #7 ERROR SHUTDOWN DROP #8 ERROR SHUTDOWN	If drop has been rack addressed: When OFF (0) drop is operating When ON (1) drop is shutdown due to error. If drop has NOT been rack addressed: When OFF (0) no drop exists When ON (1) drop exists without addressing
29	Undefined	
30	LI Channel ID	When OFF (0), indicates a 1 channel LI.
31	LI Internal Usage	
32	LI Internal Usage	

Figure D.3 - LI Control Status Register

D.5 Detailed Description of Control Data/Status Bits

The LI channel control register, bits 1-16, are initially reset OFF (0) when the LI is installed. Once altered by programming equipment, data entry, or by the ladder program, these bits will retain their state until altered again.

Halt Bit(s) (1-8)

CAUTION: Do not use the DROP HALT bit function of the CRM-210/211 Local Interface Modules until you understand the following operational characteristic and the CAUTION below. The status of inputs reported in the ladder program for a drop shut down with the DROP HALT bit function, is not as described in the Instruction Bulletin.

Any drop on a channel may be programmed to HALT, that is, turning OFF all its associated outputs. This is done by setting its respective LI channel DROP HALT bit to ON (1).

CAUTION: All inputs assigned to a drop that has halted because of the DROP HALT bit function momentarily show an OFF (0) status in the processor. Within 5 seconds, all inputs are again updated and valid input data is contained within the processor.

A drop programmed to halt will have valid updated input status contained within the LI image table.

Freeze Bit (9)

When the FREEZE BIT (bit 9) is set ON (1) by the user, all the outputs on all the drops of a particular channel will retain their last state, ON or OFF when any of the following exist:

1. A communication error at a drop (ie. cut cable)
2. The CPU HALT BIT (S8176-1) is set ON (1). (i.e. CPU error or programmed Halt).

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3. Power loss at the local (CPU) rack.

Note: Although the freeze bit may be set on (1), the operation of the freeze function depends upon the detected error.

In the following cases, the drops will not be frozen, but set OFF (0).

1. Drop with internal error (ie. power loss, faulty RI, read after write error) will have its outputs reset OFF (0).

2. CPU turned into HALT via keyswitch or S8176-3 will cause all drops to reset OFF (0).

CAUTION: Do not use the FREEZE BIT function of the CRM-210/211 Local Interface Modules until you have read and understand the following series related operational differences. The status of inputs and outputs for a failed drop, as reported in the ladder program, will be different depending on the series module being used.

General Information

When using the CRM-210/211 Local Interface Modules, series L through N1, the freeze bit function operates in a manner different from other series modules. This errata sheet details those operational differences.

The operation of the freeze function is as follows:

Pre Series L

The freeze bit function operates as described previously in Section D.5 and as shown in the LI/RI fault status table in Section 5.7.

Series L through N1

If a loss of communication occurs to a remote drop, the operation of the CRM-210/211 Module with Failure Override ON and the freeze bit set on is as follows:

1. All outputs in the remote rack will hold their last state.

2. While communication with the remote rack is interrupted, the ladder diagram program will show all Input/Output points associated with the frozen drops 1-4 as being off. The I/O points in the ladder program associated with the frozen drops 5-8 will reflect their last state.

3. Once communication is reestablished with the remote rack, the ladder diagram program will again accurately reflect the state of all I/O in the remote rack.

Series N2 and later

The freeze bit function operates as described in Section D.5 and as shown in the LI/RI fault status table in Section 5.7.

Turning Off Frozen Drops

1. Power cycling a drop with frozen outputs will reset, turn OFF all the outputs, regardless of the processor state.

2. When valid communications exist, setting a particular LI halt bit ON (1) will result in turning off frozen outputs.

Note that if the CPU is halted due to an error, turning the key switch to halt *will not reset* frozen drops.

Restarting Frozen Drops

1. Placing the CPU in either Run or Disable Outputs, by either turning the CPU keyswitch or setting the appropriate control register bits (S8176), will allow all drops with valid communications to restart in accordance with the user program.

2. Power cycling the CPU when it is in either Run or Disable Outputs.

3. To automatically restart all drops, the CPU must be running. Also, the Failure Override Bit (bit 13) and the Auto Restart Bit (bit 15) must be previously set ON (1). This will function provided valid communications exist between the operational CPU and drop(s).

4. Pushing the RESTART (RESET) button on the LI, if and only if, the CPU and communications are fully operational. (Failure Override must be set ON (1).

Transmission Fault Tolerance Bit (10)

In harsh electromagnetically noisy environments, the possibility of nuisance system shutdowns could occur. If communications are disrupted, the LI/RI system is designed to establish a valid data transmission 3 times before acknowledging these errors to the processor.

Transmission Error Detection

Two types of data transmission error detection methods are used in the LI/RI communications link.

The first detection method counts the number of times a specific block of data is determined to be invalid. The second detection method counts the number of consecutive blocks of data which are determined to be invalid

The accumulative values for each type of transmission error on each of the independent channels is kept internally by the LI and RI module. When any one good transmission occurs on a channel, the respective transmission error counters for that channel are reset to zero.

The user has the option of increasing the transmission fault tolerance level from 3 to 10 transmission errors. This is done by setting the Transmission Fault Tolerance Bit ON (1). Be aware that by setting the number of transmission errors to 10 will require additional time for the system to recognize a transmission error and cause a shutdown.

Note that the transmission fault tolerance only affects the operation of the system when invalid data is detected. In the event that data is lost due to cable damage, hardware malfunctions transmission acknowledgements will not be present in the LI/RI full duplex communication link, the system will shutdown immediately.

When the LI acknowledges excessive transmission errors, the entire system will shutdown unless the Failure Override Bit, (Bit 13) is set ON (1).

Failure Override Bit (13)

The LI is designed so that upon recognizing any drop error, it will signal the CPU to terminate ladder program processing and shutdown.

Each channel has a Failure Override Bit. The Failure Override Bit provides a means of preventing the drop error signal

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from affecting the CPU. With the Failure Override Bit set ON (1), a detected drop error will shutdown that drop, but will allow the rest of the channel to operate.

CAUTION: 1. Care must be taken whenever the Failure Override Bit is set ON (1), because the system will continue to operate when drop errors occur. However, it is still possible to halt drops thru ladder programming by setting ON (1) selected Drop Halt Bits.

2. If Failure Override Bit has been set ON (1) and a drop error shutdown occurs, followed by the Failure Override Bit being turned OFF (0), the channel will shutdown. The channel shutdown will in turn cause the system to shutdown.

This bit allows for more system flexibility, therefore improving troubleshooting and start-up capabilities.

Auto Restart Bit (15)

If a drop has been shutdown due to transmission error, setting bit 15 ON (1) will allow the LI to automatically attempt to re-establish valid communication to that drop. It should be noted, however, that the processor must be operating in Run or Disable Outputs. In order to keep the processor running under error conditions, the Failure Override Bit (Bit 13) must be ON (1).

This bit acts in the same manner as does the RESTART (RESET) button on the front of the respective LI module. The AUTO RESTART BIT has the advantage of attempting to bring a drop back on line as soon as possible without requiring personnel to push the LI RESTART button. For more information on the RESTART button, refer to Section 5.6 LI/RI Communication Restart (Pushbutton).

Drop Error Shutdown Bit(s) (21-28)

Drop Error Shutdown bits are used for diagnostic purposes. They are also used to initiate control functions when the Failure Override Bit is set ON (1).

The Drop Error Shutdown bit of a non-existent or an undefined drop will be displayed as ON (1)*, because the LI is not communicating with the drop. The drop error bit of an undefined drop being ON (1)* will not affect the shutdown operation of the system.

Note that these bits will be extremely useful when implementing applications which use ladder control programs to affect conditional failure overriding and programmed shutdowns.

* Some programmers are capable of displaying information which is relevant only to the present system configuration. For additional information, refer to a programming instruction bulletin.

APPENDIX E

E.0 LI/RI POWER-UP SEQUENCE

E.1 General Information

This appendix will describe the power-up sequence for the LI/RI I/O system.

E.2 LI Light Sequence

The following sequence of events occurs when the LI is energized, or the processor keyswitch goes from HALT to RUN or DISABLE OUTPUTS:

1. The MODULE ERROR LED blinks ON, OFF, ON, OFF, and remains OFF if no detected error* exists within the LI.

2. The CHANNEL ERROR and HALT LED's are ON and turn OFF when all the self-diagnostic routines are completed.

3. The green channel RUN LED will turn ON when the LI is communicating.

*The MODULE ERROR LED will turn ON if this module has initiated a rack error condition, thus halting the system when:

1. A self-diagnostic error is detected.

2. Missing defined racks (unless the Failure Override Bit is ON (1)).

3. An illegal rack addressing map is detected.

E.3 RI Light Sequence

The following sequence of events occurs when the RI is energized:

1. All red LED's turn ON and then OFF.

2. The red HALT LED will turn OFF when the green RUN LED turns ON.

3. The green RUN LED turns ON when the RI is communicating to its rack assembly and the CPU is in Run or Disabled Outputs.

When the processor keyswitch goes from HALT to RUN or DISABLE OUTPUTS, only steps 2 and 3 occur.

The MODULE ERROR LED will remain ON only when a self-diagnostic error is detected.

E.4 LI/RI Initialization

1. When power is applied, self-diagnostic routines are initiated and verified within the LI, RI, CPU, and other register modules. Completion of the self-diagnostics insures that these modules are operational.

2. The LI then verifies communications with all of its drops.

3. The CPU will initiate the loading of the user defined rack addressing map into the LI.

If valid LI/RI communications cannot be established, an error will be generated by the LI module. This error will halt the processor unless the failure override bit of that LI channel control register has been set ON (1).

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APPENDIX F

F.0 LI/RI ADDRESSING WITH MODEL 300

F.1 General Information

The following two examples are used to illustrate the concept of the Model 300 local and remote address assignments. The first utilizes a Model 300 housed in a digital I/O rack. The second has the Model 300 in a register rack. In both examples, there are 256 digital I/O and 6 register modules.

When examining these Model 300 examples, observe the following points:

1. Since the Model 300 can support only one LI and address a maximum of 112 registers, adding an LI *does not* increase the number of useable registers, but does permit the use of remote I/O.

2. Assign as many registers as possible to the LI. This type of register assignment allows for flexible remote I/O configurations.

3. The register assignments are distributed in an equitable manner between the two channels of the LI. This method allows for a uniform LI/RI update time.

4. The digital I/O are assigned to the first 16 registers because these are the forcible registers within the Model 300's 112 useable registers.

F.2 Local (Model 300 CPU) Digital Rack Assignments

This first example demonstrates the use of a Model 300 being housed in a digital rack to support local I/O while also supporting remote I/O. The local (CPU) rack is supporting 64 digital I/O points and a 2 channel LI module with remote drops. 192 digital I/O points and 6 register modules are assigned to the drops among the two channels.

The maximum update time for any drop on channel 1 is 54.7ms. The maximum update time for the drop on channel 2 is 84.0ms. For more information, refer to Appendix A, LI/RI Update Time.

F.2.1 LOCAL (CPU) RACK

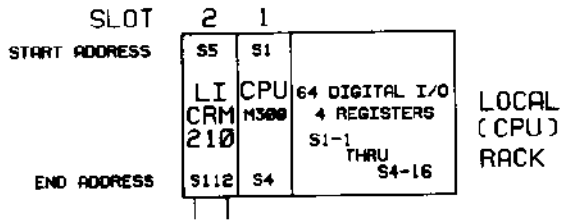


Figure F.1 - Local (Model 300 CPU) Digital Rack Address Assignments

Slot 1- Four registers have been assigned to the Model 300 for the 64 local digital I/O. (S1-1 thru S4-16)

Note that in a digital rack, addresses for digital I/O are always assigned to slot 1.

Slot 2- The remaining 108 registers are assigned to the LI module (CRM-210) so the CPU may access and use them as either external or internals. (S5 thru S112)

F.2.2 CHANNEL 1, DROP #1 RACK ADDRESS ASSIGNMENTS

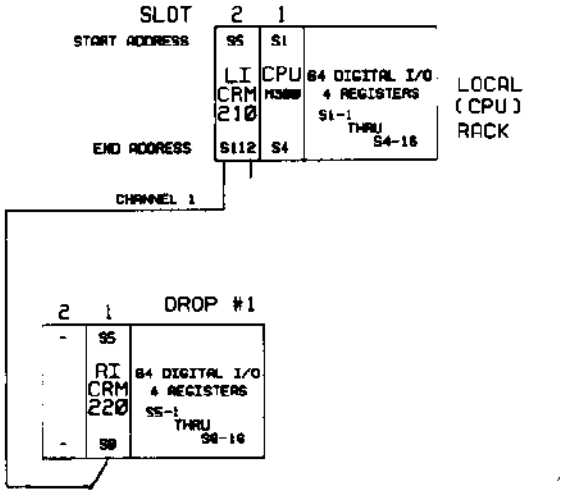


Figure F.2 - Channel 1, Drop #1 Rack Address Assignments

A total of 64 digital I/O points are assigned to this remote drop. Note that this drop uses a low profile RI (Class 8030 Type CRM-220) which is designed to fit into four function I/O rack assemblies only. This same addressing scheme can be used if a Type CRM-222 were used.

Slot 1- The RI module (CRM-220) has been assigned four registers for the 64 remote digital I/O. (S5-1 thru S8-16)

Slot 2- No address assignments required.

F.2.3 CHANNEL 1, DROP #2 RACK ADDRESS ASSIGNMENTS

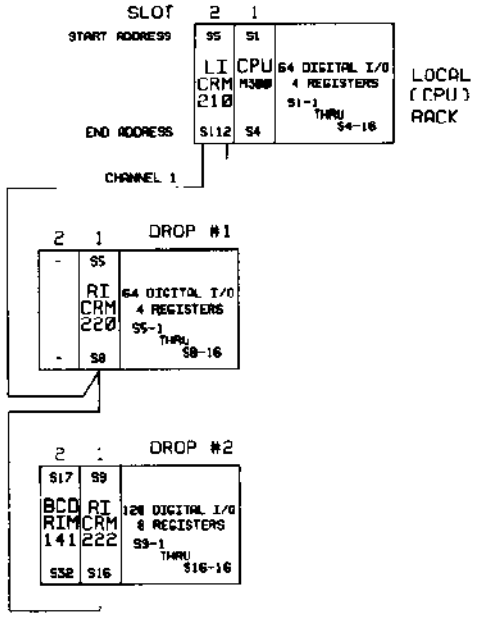


Figure F.3 - Channel 1, Drop #2 Rack Address Assignments

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The second drop is similar to the first in that it has digital I/O. However, this drop has double the digital I/O points and is also using a BCD input module.

Slot 1- The RI module (CRM-222) has been assigned 8 registers for the 128 remote digital I/O. (S9-1 thru S16-16)

Slot 2- 16 registers have been assigned for the BCD input module. (S17 thru S32)

F.2.4 CHANNEL 2, DROP #1 RACK ADDRESS ASSIGNMENTS

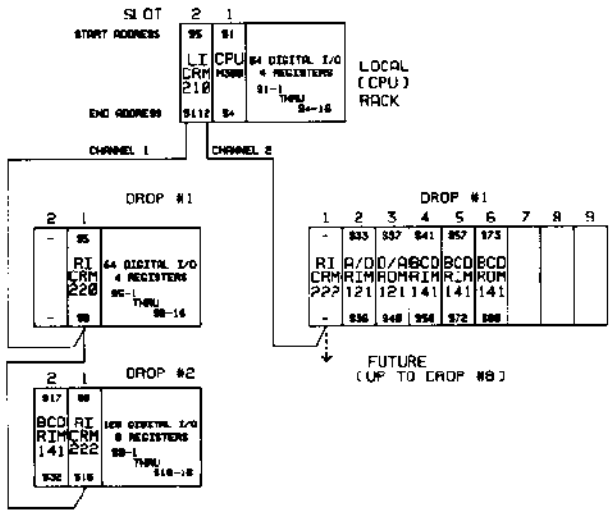


Figure F.4 - Channel 2, Drop #1
Rack Address Assignments

For this next drop, a 9 slot register rack is connected to channel 2. Note that the addresses for channel 2 start at one greater than the ending address for channel 1. In other words, when channel 1 ends, channel 2 begins.

Requirements for register modules vary. As an example, a 4 channel analog module requires 4 registers for complete addressing. A BCD I/O module requires 16 registers.

Slot 1- No address registers are required since there are no digital I/O points.

Slot 2- Four registers are assigned to a 4 channel analog input module. (S33 thru S36)

Slot 3- Four registers are assigned to a 4 channel analog output module. (S37 thru S40)

Slot 4- 16 registers are assigned to a 16 (4 digit) BCD input module. (S41 thru S56)

Slot 5- 16 registers are assigned to a 16 (4 digit) BCD input module. (S57 thru S72)

Slot 6- 16 registers are assigned to a 16 (4 digit) BCD output module. (S73 thru S88)

Slot 7-9*- No address assignments required.

* Slot 9 and above cannot be addressed by the Model 300. (These slots may be used to power any register module which require only power and does not require registers such as a D-LOG or SY/NET module).

F.3 Local (Model 300 CPU) Register Rack Address Assignments

This second example demonstrates the use of a Model 300 in a register rack. The local (CPU) rack will house the processor, LI and 5 additional register modules.

Note how the addresses are assigned in very much the same manner as the previous example and specifically the digital I/O and register modules.

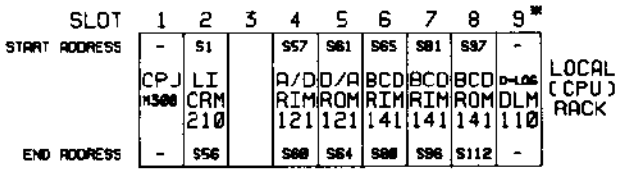
The first 16 of the 112 total addressable registers of the Model 300 are used for digital I/O since they may be forced.

The Model 300 Processor can support one LI module. The addition of a LI module *does not* increase the number of additional registers, however, it does permit the use of remote I/O.

In order to maximize the number of registers available to the LI, and facilitate for easier future expansion, the ending addresses are calculated for the slots by subtracting the number of registers required for each module in the CPU rack from the available registers. (i.e. The ending address for the last addressed slot, in this case slot 8, is 112 and the preceding slot's ending address should be 112 minus the number of registers required for this module.)

The maximum update time for any drop on channel 1 is 17.4ms. The maximum update time for the drop on channel 2 is 44.4ms. For more information on how to calculate LI/RI update times, refer to Appendix A, LI/RI Update Time.

F.3.1 LOCAL CPU RACK



* SLOT 9 CANNOT BE ADDRESSED BY THE MODEL 300. (THIS SLOT MAY BE USED TO POWER A D-LOG OR SY/NET MODULE)

Figure F.5 - Local (Model 300 CPU)
Register Rack Address Assignments

Slot 1- No address registers are required since there are no digital I/O points.

Slot 2- 56 registers are assigned to the LI (CRM-210) for the 2 remote I/O channels and future expansion. (S1 thru S56)

Slot 3- No register assignments required. (Spare slot for future expansion.)

Slot 4 4 registers are assigned to a 4 point analog input module. (S57 thru S60)

Slot 5- 4 registers are assigned to a 4 point analog output module. (S61 thru S64)

Slot 6- 16 registers are assigned to a BCD input module. (S65 thru S80)

Slot 7- 16 registers are assigned to a 16 (4 digit) BCD input module. (S81 thru S96)

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Slot 8- 16 registers are assigned to a 16 (4 digit) BCD output module. (S97 thru S112)

Slot 9- This slot is not addressable by the Model 300. (This slot can be used to support a module which only requires power. For example, a D-LOG (DLM-110) or SY/NET (CRM-510).)

F.3.2 CHANNEL 1, DROP #1 RACK ADDRESS ASSIGNMENTS

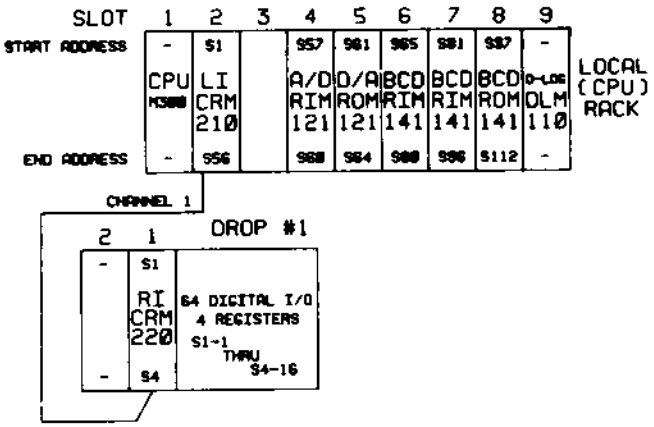


Figure F.6 - Channel 1, Drop #1
Rack Address Assignments

This drop will support 64 I/O. It uses a Type CRM-220 RI module which means that the drop must use 4 function I/O rack assemblies.

Slot 1- Four registers are required for the 64 digital I/O. (S1-1 thru S4-16)

Slot 2- No address assignments required.

F.3.3 CHANNEL 1, DROP #2 RACK ADDRESS ASSIGNMENTS

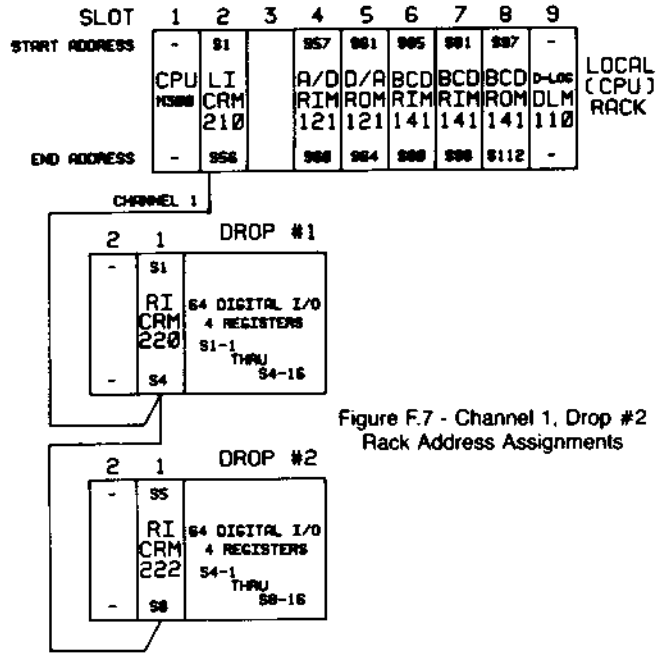


Figure F.7 - Channel 1, Drop #2
Rack Address Assignments

This drop is identical to Drop #1 in that it has 64 digital I/O and differs in only that a Type CRM-222 is used. The Type CRM-222 RI can be used in any type of rack assembly, 4 or 8 function I/O rack as well as register rack assemblies.

Slot 1- 4 registers are required for the 64 digital I/O. (S5-1 thru S8-16)

Slot 2- No address assignments required.

F.3.4 CHANNEL 2, DROP #1 RACK ADDRESS ASSIGNMENTS

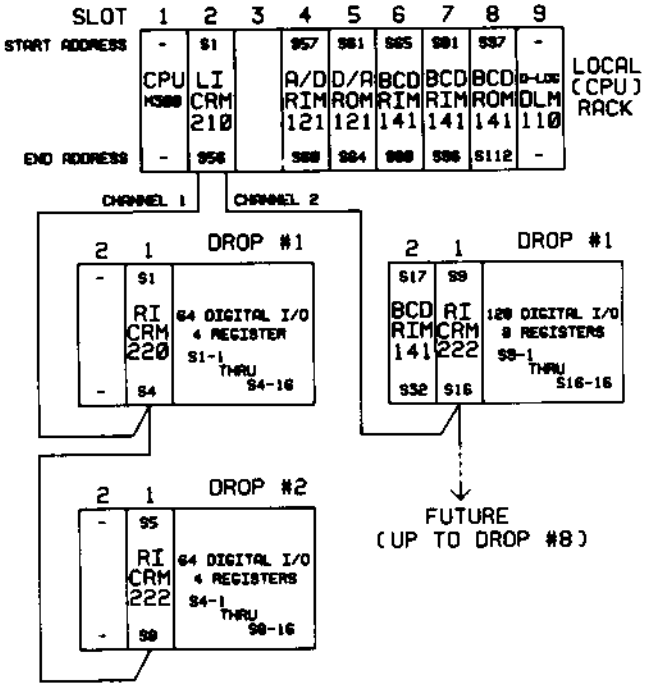


Figure F.8 - Channel 2, Drop #1
Rack Address Assignments

This drop supports 128 digital I/O and a BCD input module.

Slot 1- 8 registers are assigned to support the 128 digital I/O. (S9-1 thru S16-16)

Slot 2- 16 registers are assigned to the BDC input module. (S17 thru S32)

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APPENDIX G ADDITIONAL DATA LINE PROTECTION

For outdoor communication cable, or indoor cable that is subject to severe electrical disturbances, overvoltage transient protection is required. This protection is to guard both modules and cable from damage. To accomplish this, a device that suppresses transients caused by lightning, inductive switching and electrostatic discharge must be used. This device is called a *data line protector (DLP).*

The recommended DLP is the Square D Class 8030 CBP-310.

IMPORTANT INSTALLATION CONSIDERATIONS

1. Cable runs between the CRM-2XX Interface Modules and panel DLPs should be kept as short as possible. The shield in the cable can be connected to the DLP's "N/C" screw; the portion of the unshielded cable must be kept as short as possible. The Interface Module wiring is standard.

2. A *panel* DLP should be solidly grounded, via its ground lead, directly to the panel.

3. *Building* DLPs are suggested for outdoor runs of cable to provide primary level protection against lightning-induced transients. The DLPs should preferably be installed at the point of building entry to keep all transients outside the building, otherwise it may be necessary to electromagnetically shield the cable so that the high voltage transients aren't coupled into cables within the building. Shielding the cable can be done with a separate, properly grounded, steel conduit.

4. *Building* DLPs must be solidly grounded, via their GND lead, directly to building steel or to the power ground.

5. The load of each DLP is equal to 200 feet of cable.

6. Each SY/MAX rack and power supply must be solidly grounded. Refer to the "Planning and Installation Guide," Instruction Bulletin #30598-175-XX.

7. See Instruction Bulletin #30598-518-01 for further details on the Data Line Protector.

8. The CRM-210/211 Modules Series 0 and later have this isolation built into the module and they do not require a DLP.

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