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CPCI2PMC

CompactPCI® 2-Slot PMC Module Carrier Hardware Reference

Document No. B-T-MR-CPCI2PMC-A-0-A4

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for the Curtiss-Wright Controls CPCI2PMC 6U CompactPCI two-slot PMC Module Carrier herein referred to as the CPCI2PMC board, part number BHAS-CPCI2PMC-2.

1.1.2 Scope

This reference manual contains a physical and operational description of the CPCI2PMC. To benefit from the manual you should have a general understanding of computer software and hardware applications, and be familiar with PMC modules.

1.1.3 Style Conventions

- Called functions are italicized: *OpenConnect()*
- Data types are italicized: *int*
- Function parameters are bolded: **Action**
- Path names are italicized: *utility/sw/cfg*
- File names are bolded: **config.c**
- Path file names are italicized and bolded: ***utility/sw/cfg/config.c***
- Hexadecimal values are written with an "0x" preceding the value (e.g. 0xFB000)
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that is bolded represent user input. Text that the computer displays on the screen is not bolded.

```
ls
file1           file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/): /SYNC

1.2 Related Publications

- *PCI Local Bus Specification Rev. 2.1*- PCI Special Interest Group
- *PCI Local Bus PCI to PCI Bridge Architecture Specification Rev. 1.0* - PCI Special Interest Group
- CompactPCI Specification, PICMG 2.0 R2.1, Sept. 1997 by the PCI Industrial Computer Manufacturer's Group
- Draft Standard for a Common Mezzanine Card Family: CMC, P1368/Draft 2.0, April 4, 1995 by Bus Architecture Standards Committee of the IEEE Computer Society
- Additional information about the Intel 21152-PCI-to-PCI bridge chip can be obtained from the vendor:

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- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

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2. PRODUCT OVERVIEW

2.1 Overview

The Curtiss-Wright Controls CPCI2PMC two-slot PMC Module Carrier board is a 6U CompactPCI add-in board that supports one doublewide or two singlewide 32-bit PMC cards. The CPCI2PMC supports +5 V and +3.3 V signaling PMC modules and optionally supports the mapping of 128 user I/O signals out to the CompactPCI J3/P3 and J4/P4 backplane connectors. The I/O signal mapping is compliant with the PMC on CompactPCI specification PICMG 2.3 R1.0, August 7, 1998. The CPCI2PMC's PCI interface design is compliant with the PCI bus specification V2.1 and the PCI-to-PCI Bridge function is compliant with the PCI Local Bus "PCI to PCI Bridge Architecture Specification", Rev. 1.0.

The bus connector interface and board physical layout are in accordance with the CompactPCI specification PICMG 2.0 R2.1.

NOTE: In this manual CompactPCI is referred to as CPCI. Also, the acronym "CPCI" refers to any mechanically-based characteristics of the CPCI2PMC, including the J1 connector for interfacing to the host via a backplane. The acronym "PCI" is used when relating to electrical characteristics of the board or relating to signals that are covered in the PCI specification separate from CompactPCI.

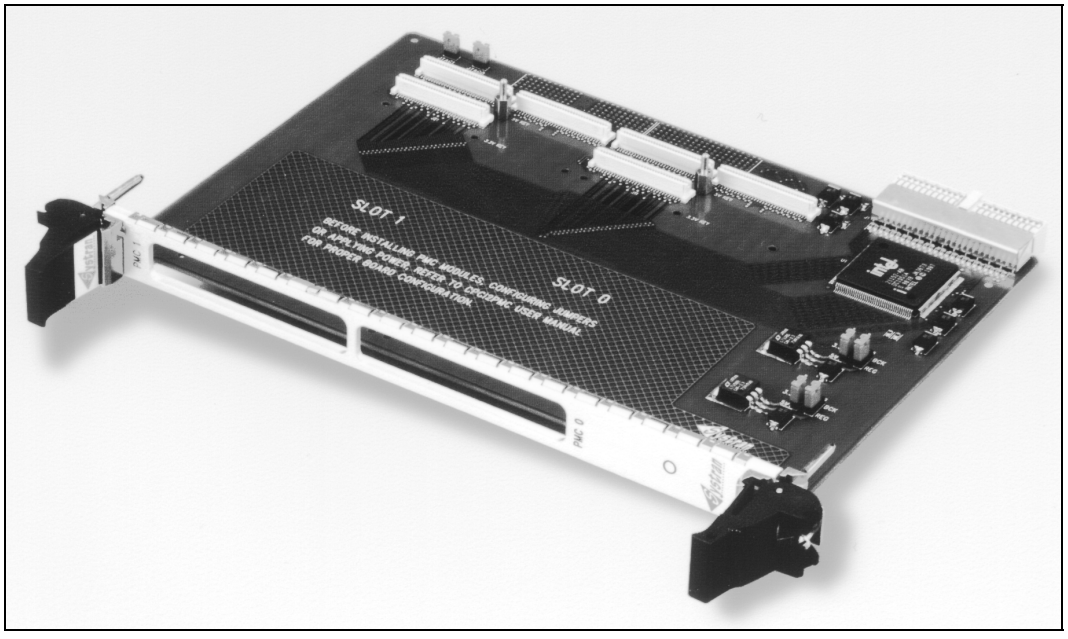


Figure 2-1 CPCI2PMC-2 Board

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2.1.1 Features

The CPCI2PMC board provides the following features/functions:

- 6U board, connector, faceplate, and ejectors per CompactPCI Specification, Rev. 2.1
- 32-bit PCI bus implementation per the PCI Local Bus Specification, Rev. 2.1
- PCI-to-PCI Bridge function is compatible with PCI Local Bus "PCI to PCI Bridge Architecture Specification", Rev. 1.0
- Two CMC/PMC Slots and associated connectors per the CMC Draft Standard, IEEE P1386/Draft 2.0 and the PMC Draft Standard, P1386.1/Draft 2.0
- Faceplate cutouts for two CMC modules per the CMC Draft Standard, IEEE P1386/Draft 2.0
- +5 V and +3.3 V signaling voltage for each CMC Slot
- Jumper-selectable +3.3 V source from either CompactPCI system power supply (via backplane) or on-board regulators
- On-board +3.3 V regulators capable of providing a minimum of 2.5 Amps continuous current per slot
- 128 optional user I/O signals
- Supports both +5 V and +3.3 V signaling on both CompactPCI and PMC buses

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3. INSTALLATION

3.1 Unpack the CPCI2PMC

Table 3-1 lists the contents of the CPCI2PMC shipping packages.

Table 3-1 Contents of CPCI2PMC Shipping Packages

Qty	Description
1	CPCI2PMC Printed Circuit Assembly
1	CPCI2PMC Hardware Reference *

One manual is shipped for each board ordered. Extra manuals may be purchased by calling Curtiss-Wright Controls, Inc. or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g., BTMR-CPCI2PMC).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Inspect the CPCI2PMC

Examine the CPCI2PMC to determine if any damage occurred during shipping.

3.3 Configure and Install the CPCI2PMC

NOTE: The CPCI2PMC is an Electrostatic Sensitive Device (ESD). Use an anti-static mat connected to a wrist band when handling or installing the board.

3.3.1 JTAG Jumpers

Figure 3-1 shows the locations of the JTAG jumpers (J2) and (J5). Each of these items and their settings are described in their respective sections. JTAG0 is installed if a PMC module is not found in Slot 0. JTAG1 is installed if no PMC module is found in Slot 1.

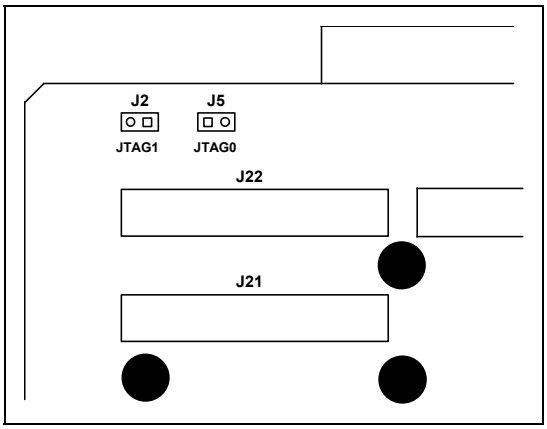


Figure 3-1 JTAG Jumper Locations

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3.3.2 +3.3 V and +5 V Signaling Jumpers

NOTE: The bridge chip's primary PCI bus (CompactPCI) is automatically configured to the signaling level (+5 V or +3.3 V) of the backplane.

Jumpers J6 and J7 provide the appropriate signaling voltage (+3.3 V or +5 V) to CMC/PMC slot 0 and CMC/PMC slot 1 as shown in Figure 3-2.

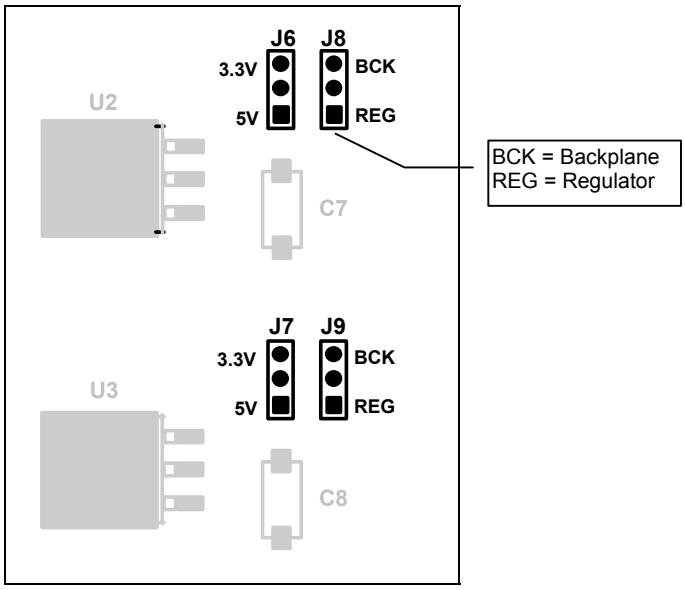


Figure 3-2 PMC Power Jumper Locations

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+3.3 V CONFIGURATION

Figure 3-3 shows the proper jumper configuration when +3.3 V signaling PMC Modules are installed. This configuration should only be used when both PMC modules signal at +3.3 V or a single +3.3 V PMC module is installed.

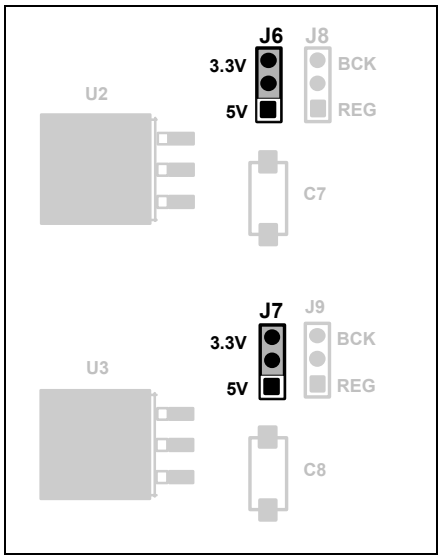


Figure 3-3 +3.3 V Power Jumper Configuration

+5 V CONFIGURATION

Figure 3-4 shows the proper jumper configuration when any +5 V signaling PMC Modules are installed. This includes two +5 V signaling PMC modules or one +5 V signaling PMC module.

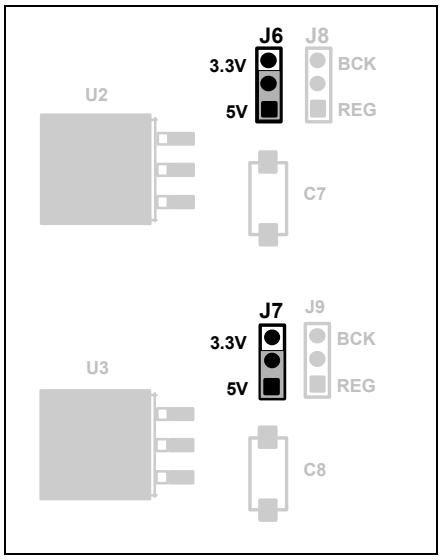


Figure 3-4 +5 V Power Jumper Configuration



CAUTION: J6 and J7 must be configured the same for the board to operate properly.

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3.3.3 +3.3 V Power Jumpers

Jumpers J8 and J9 are used to select the source of the +3.3 V power. This power can be provided by the CompactPCI backplane, if available, or by the two +5 V to +3.3 V regulators that are present on the CPCI2PMC board. Figure 3-5 shows the proper jumper configuration for the CompactPCI backplane source option and Figure 3-6 shows the configuration for the regulator source option.

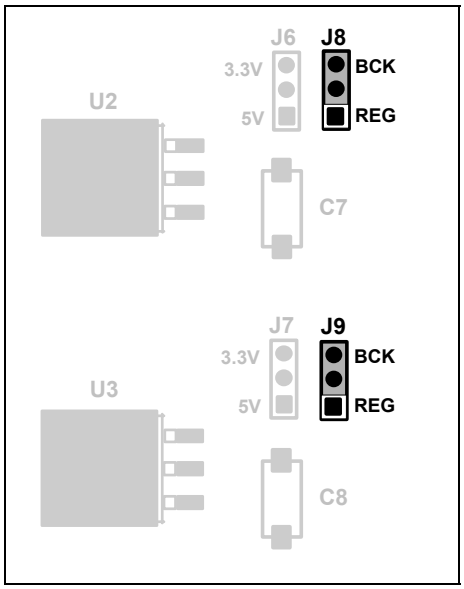


Figure 3-5 +3.3 V Power from CompactPCI Backplane

CAUTION: J8 and J9 determine the source of power and must be configured the same to prevent possible damage.

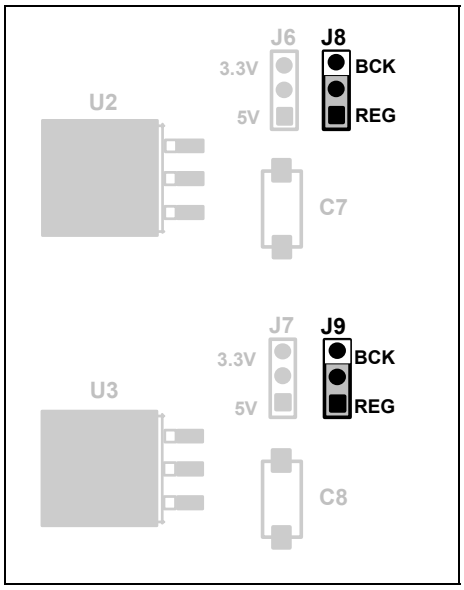


Figure 3-6 +3.3 V Power from CPCI2PMC board regulators

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3.3.4 CMC/PMC Slot Voltage Keys

Place the voltage keys in their proper locations depending on what type of PMC cards are to be installed. (+3.3 V or 5 V)

3.3.5 Installation of PMC Modules on the CPCI2PMC

Figure 3-7 shows the model with the optional I/O connectors installed.

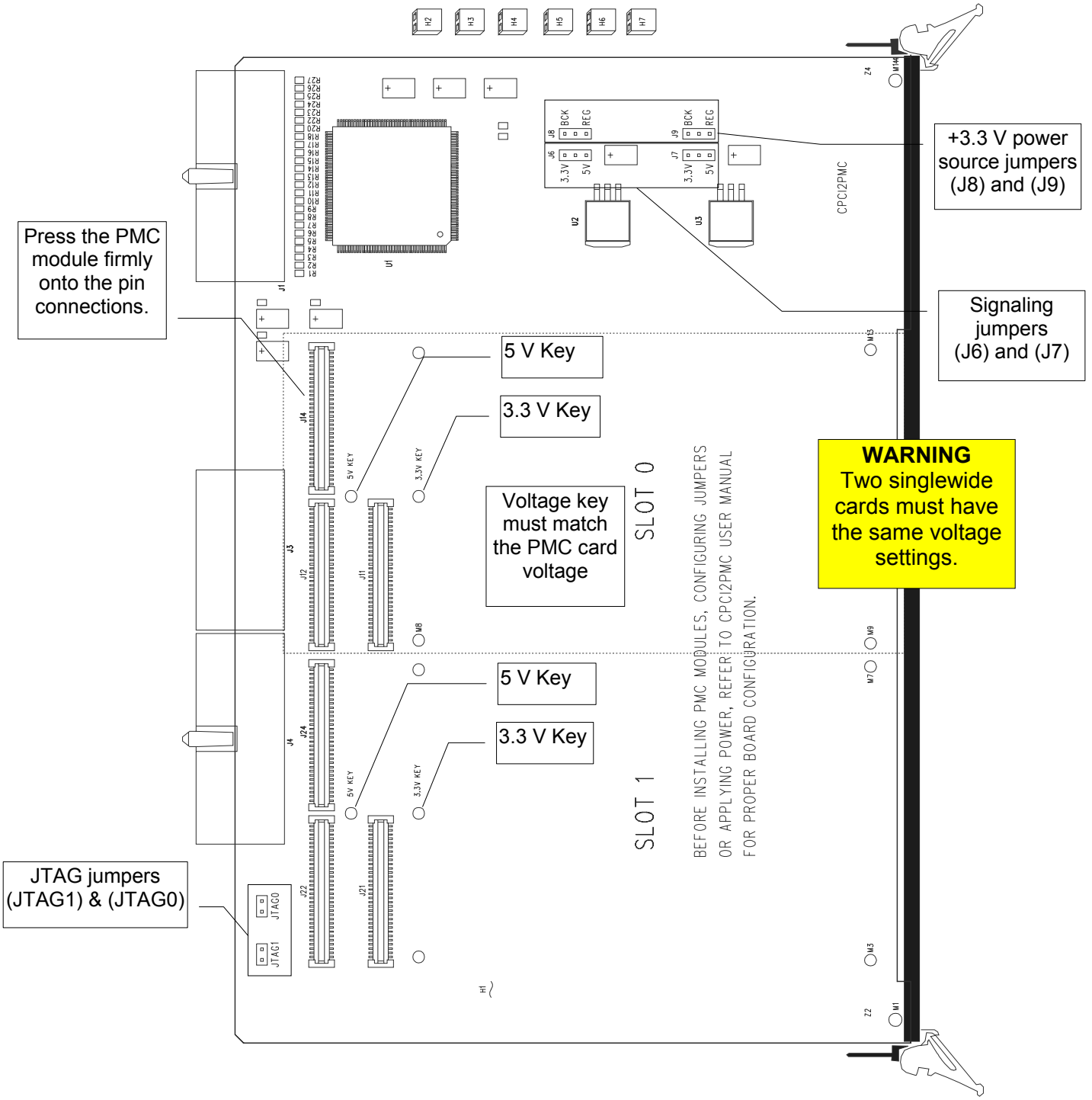


Figure 3-7 Installation of a PMC Module on the CPCI2PMC-1

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Referring to the appropriate figures and table described below, perform the following steps in removing the CPCI2PMC from its shipping container (or from an existing installation) and installing PMC Modules. The asterisk (*) denotes optional items.

1. Turn off all power to the CPCI backplane.
2. Remove the CPCI2PMC from its shipping container and move it to the ESD-controlled area where the installation of the PMC Module(s) can be made.

*2a. Remove the CPCI2PMC from the CPCI backplane if modifications are necessary, and move it to an ESD controlled area where the installation or changing of PMC Modules can be made.

3. Place Voltage Keys in proper locations.
4. Set the PMC signaling jumpers (J6) and (J7) and the +3.3V power-source jumpers (J8) and (J9) to the desired positions.
5. Install the PMC Module(s) onto the carrier board by applying adequate and equal pressure to the PMC Module(s) on the CPCI2PMC board.
6. Install four PMC mounting screws that should have been included with the PMC modules.



WARNING: Before installing CPCI2PMC with optional 128 user I/O signals (part number BHAS-CPCI2PMC-1) into the CPCI backplane, verify that the backplane pinout for P3 and P4 are pin-for-pin compatible with Table 2-1 and Table 2-2.

7. Slide the CPCI2PMC into a desired peripheral slot of a CPCI backplane while applying enough force to ensure a tight fit into the backplane connector. After insertion, use a standard Phillips-head screwdriver to secure the CPCI2PMC panel onto the frame of the CPCI chassis.

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3.3.6 Connector Pin Assignments

Table 3-2 contains the pin assignments for the PCI signals, power, ground and other pertinent connections made to the J1 connector which interfaces to the CPCI backplane. Note that the J1 connector has six columns of pin positions labeled A through F with column F providing connections for a shield ground. There are twenty-five rows of pins with rows 12 through 14 not used since this area of the connector is designated for the voltage key.

Table 3-2 CompactPCI Bus Pin Assignments

Pin	A	B	C	D	E	F	
25	5 V	REQ64#	ENUM#	3.3 V	5 V	GND	
24	AD[1]	5 V	V(I/O)	AD[0]	ACK64#	GND	
23	3.3 V	AD[4]	AD[3]	5 V	AD[2]	GND	
22	AD[7]	GND	3.3 V	AD[6]	AD[5]	GND	
21	3.3 V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	J
19	3.3 V	AD[15]	AD[14]	GND	AD[13]	GND	1
18	SERR#	GND	3.3 V	PAR	C/BE[1]#	GND	
17	3.3 V	SDONE	SBO#	GND	PERR#	GND	
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	3.3 V	FRAME#	IRDY#	GND	TRDY#	GND	C
12-14	**KEY AREA**						O
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	AD[21]	GND	3.3 V	AD[20]	AD[19]	GND	N
9	C/BC[3]#	IDSEL	AD[23]	GND	AD[22]	GND	E
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	C
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	T
6	REQ#	GND	3.3 V	CLK	AD[31]	GND	O
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	R
4	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	INTA#	INTB#	INTC#	5 V	INTD#	GND	
2	TCK	5 V	TMS	TDO	TDI	GND	
1	5 V	-12 V	TRST#	+12 V	5 V	GND	
Pin	**A**	**B**	**C**	**D**	**E**	**F**	

The CMC/PMC slot connectors J11, J12, J21 and J22 pin assignments conform to CMC P1386/Draft 2.0 and PMC P1386.1/Draft 2.0

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4. OPERATION

4.1 Overview

This section describes the function of the CPCI2PMC. The CPCI2PMC is compliant with multiple industry standards and specifications. As such, the descriptions contained herein are not intended to provide comprehensive descriptions of the function/protocol of buses, registers, etc., that are more completely described in their respective specification(s). The reader may refer to those specifications which take precedence over the descriptions provided in this manual.

4.2 Functional Description

Figure 4-1 is a block diagram of the CPCI2PMC. The remaining subsections describe elements of the block diagram.

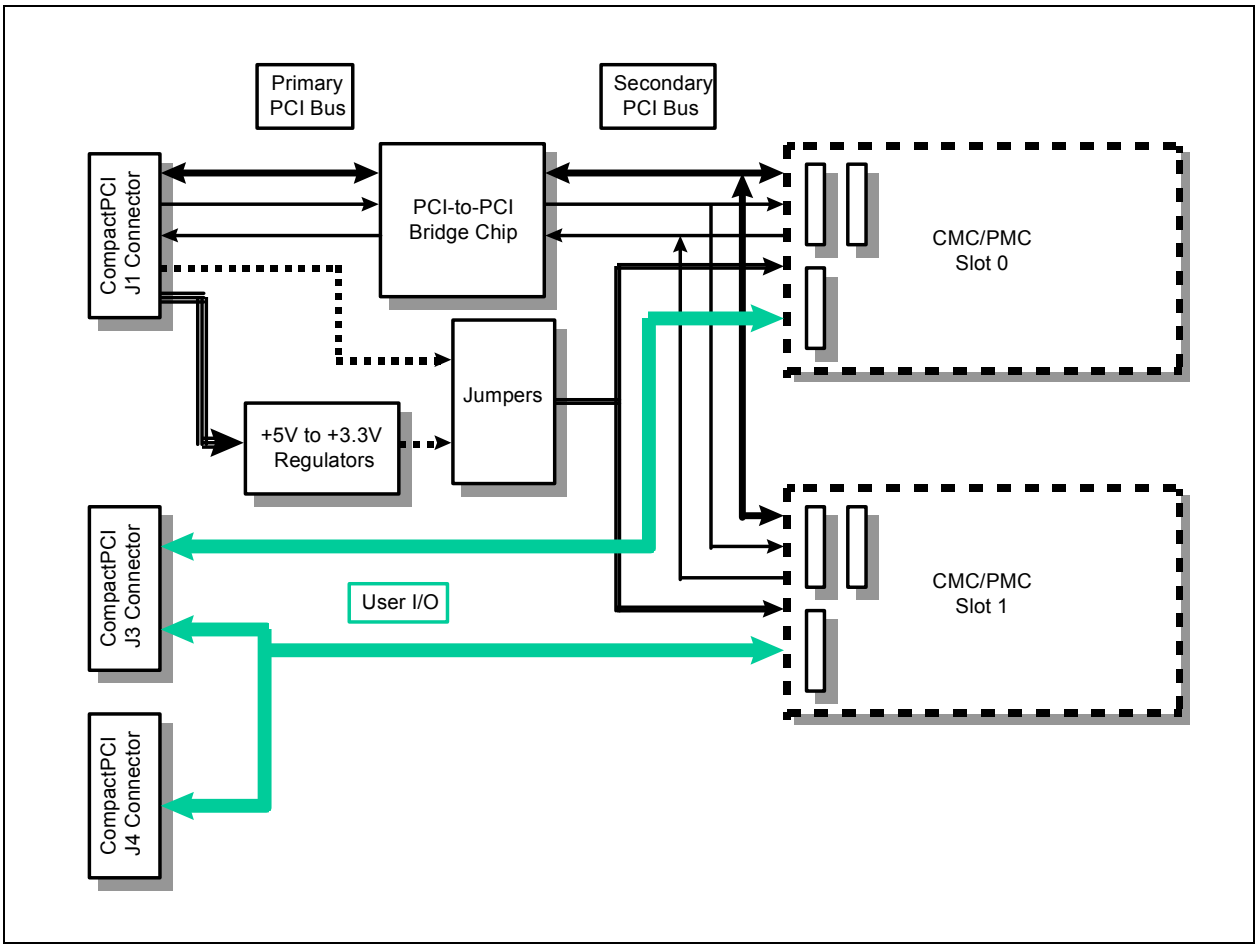


Figure 4-1 CPCI2PMC Block Diagram

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4.2.1 PCI-to-PCI Bridge Chip Function

The CPCI2PMC essentially provides a bridge between the Primary PCI bus on the CompactPCI backplane and the Secondary PCI bus on the CPCI2PMC board. The Secondary PCI bus provides the interface to up to two PMC modules that can be installed on the board. The bridge function is accomplished entirely by the Intel 21152 PCI-to-PCI bridge chip. The Intel 21152 is fully compliant with the following PCI specifications:

- PCI Local Bus Specification, Revision 2.1
- PCI-to-PCI Bridge Architecture Specification, Revision 1.1

USER ACCESSIBLE REGISTERS

The 21152 has no registers that should be accessed by the user under normal circumstances. The 21152 has configuration registers which are initialized by the system BIOS.



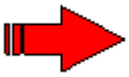
WARNING: Reliable operation cannot be guaranteed if these registers are altered in any way.

However, these registers may be altered if necessary. See section 1.3 for more information on contacting the vendor.

4.2.2 +5 V to +3.3 V Regulators and Jumpers

Two +5 V to +3.3 V regulators are present on the CPCI2PMC board. The purpose of these regulators is to provide +3.3 V power to the CMC/PMC slots if +3.3 V power is not available from the CompactPCI system/backplane. One regulator is dedicated to each slot and can provide up to 3.0 Amps to the slot (although the CMC specification only allows for a maximum power dissipation of 7.5 Watts). The Slot 0 regulator, U2, also provides a small amount of +3.3 V power to the PCI-to-PCI bridge chip, U1. Jumpers J8 and J9 provide the means of bypassing the regulators if +3.3 V power is available from the CompactPCI backplane.

The regulators also can provide the +3.3 V signaling power to the Secondary PCI Bus VIO (S_VIO_0 and S_VIO_1) pins for the PCI-to-PCI bridge chip and the PMC modules PCI interface chip. (If the regulators are bypassed, the +3.3 V will come from the CompactPCI backplane.) VIO will be either +3.3 V or +5 V dependent upon user requirements. The voltage source for S_VIO_0 and S_VIO_1 can be chosen via jumpers J6 and J7 however, both must be set to the same voltage.



NOTE: Connectors J3, J4, J14, and J24 are present only on BHAS-CPCI2PMC-1. They are not present on BHAS-CPCI2PMC-2.

More details on jumper setting are provided in Chapter 3.

4.2.3 CMC/PMC Slots

Two slots are provided which meet the physical and electrical requirements of the CMC and PMC specifications. Electrically, these slots implement the 32-bit PCI bus at 33 MHz on the J11/J12 and J21/J22 connectors. Sixty-four (128 total) user I/O signals are available on each connector (more on this in a later section).

For PCI Type 1 cycles on the Primary PCI bus, the PCI-to-PCI bridge chip will convert these cycles to Type 0 Configuration cycles on the Secondary PCI bus. The IDSEL line is

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asserted to the appropriate PMC during these cycle types. The CPCI2PMC is configured such that PMC Slot 0 is IDSEL 0x4 and PMC Slot 1 is IDSEL 0x5.

4.2.4 Interrupt Routing

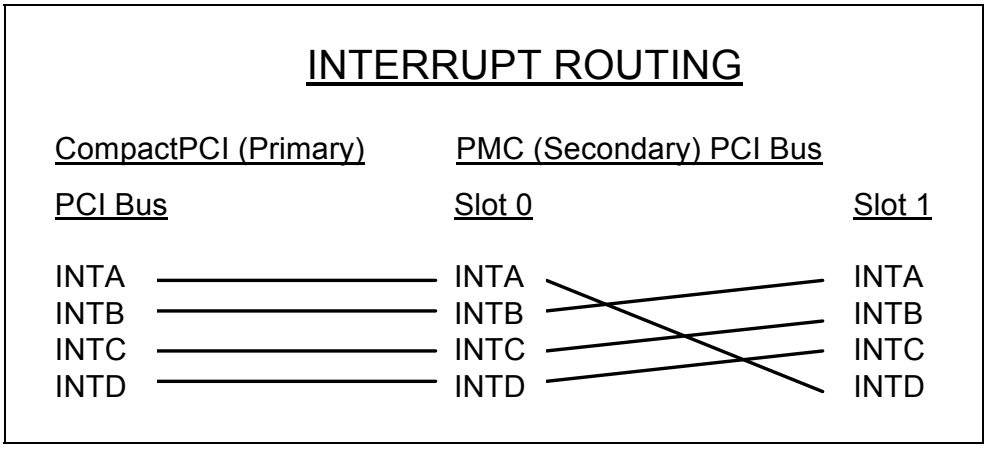


Figure 4-2 Secondary to Primary PCI Interrupt Routing

Four possible Secondary PCI bus interrupts can originate from each PMC slot. These interrupts are designated A, B, C, and D. These interrupts are not routed through the bridge chip but are hard-wired to the Primary PCI bus interrupts on the CompactPCI backplane. According to the *PCI Local Bus PCI-to-PCI Bridge Architecture Specification*, these interrupts must adhere to a specific mapping to the Primary PCI bus as shown in Figure 4-2. This mapping ensures the proper association between the PMC device, its IDSEL and PCI INT, the system Interrupt Controller, and the Interrupt Handler S/W. Refer to the *PCI Local Bus PCI-to-PCI Bridge Architecture Specification* for additional information.

4.2.5 JTAG Signals and Jumpers

The five JTAG signals (TDI, TDO, TCK, TMS, and TRST) are supported by the CompactPCI bus and the PMC bus and by the CPCI2PMC. All signals are routed to each of the PMC slots for use by the user's PMC modules if required. TDI and TDO are handled in a special way because they are daisy-chained signals. TDI from the CompactPCI backplane goes to PMC Slot 0 and TDO comes from PMC Slot 1 to the CompactPCI backplane. The TDO output from PMC Slot 0 is routed to TDI of PMC Slot 1. Two jumpers, J5 and J2, are provided to bypass TDI to TDO for Slot 0 and Slot 1, respectively. The jumper would be in place if no PMC card was installed in a given slot so that the JTAG daisy-chain can be maintained.

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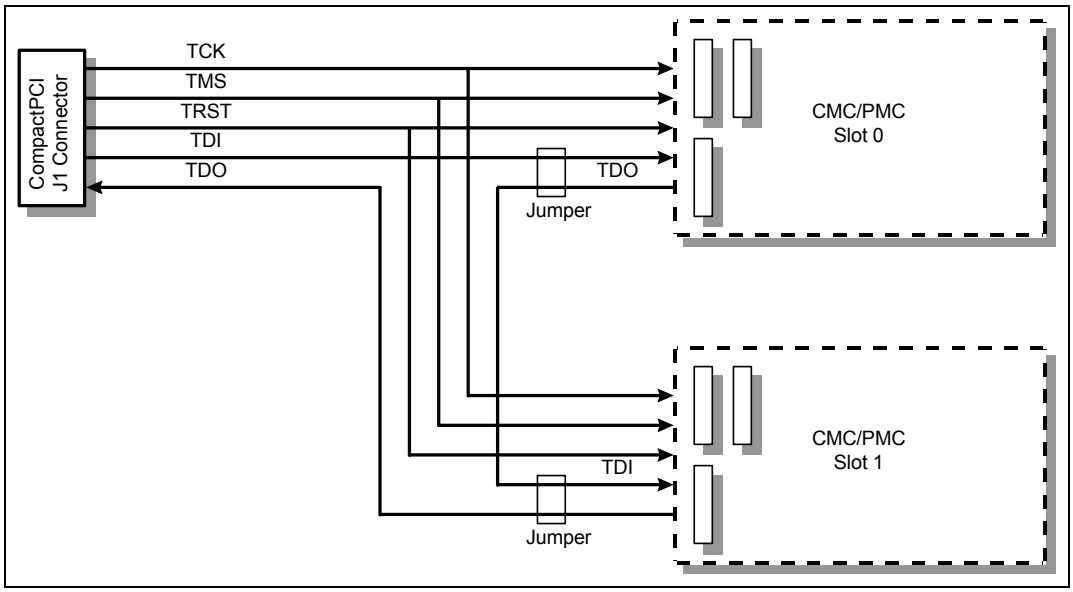


Figure 4-3 JTAG Signals

4.2.6 User I/O (BHAS-CPCI2PMC-1 Only)

A total of 128 signals are routed from the PMC slots' J14 and J24 connectors and are mapped to the CompactPCI J3 and J4 connectors as shown in the following tables:

Table 4-1 PMC Slot 1 J24 Connector Mapped to the 6U CompactPCI J3 and J4 Connectors Row

Connector	Pos.	F	E	D	C	B	A
J4	9	GND	GND	GND	GND	GND	GND
J4	8	GND	1	2	3	4	5
J4	7	GND	6	7	8	9	10
J4	6	GND	11	12	13	14	15
J4	5	GND	16	17	18	19	20
J4	4	GND	21	22	23	24	25
J4	3	GND	26	27	28	29	30
J4	2	GND	31	32	33	34	35
J4	1	GND	36	37	38	39	40
J3	19	GND	41	42	43	44	45
J3	18	GND	46	47	48	49	50
J3	17	GND	51	52	53	54	55
J3	16	GND	56	57	58	59	60
J3	15	GND	61	62	63	64	VI/O
J3	14	GND	+5V	+5V	+3.3V	+3.3V	+3.3V

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Table 4-2 PMC Slot 0 J14 Connector Mapped to the 6U CompactPCI J3 Connectors Row

Connector	Pos.	F	E	D	C	B	A
J3	14	GND	+5V	+5V	+3.3V	+3.3V	+3.3V
J3	13	GND	1	2	3	4	5
J3	12	GND	6	7	8	9	10
J3	11	GND	11	12	13	14	15
J3	10	GND	16	17	18	19	20
J3	9	GND	21	22	23	24	25
J3	8	GND	26	27	28	29	30
J3	7	GND	31	32	33	34	35
J3	6	GND	36	37	38	39	40
J3	5	GND	41	42	43	44	45
J3	4	GND	46	47	48	49	50
J3	3	GND	51	52	53	54	55
J3	2	GND	56	57	58	59	60
J3	1	GND	61	62	63	64	VI/O

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APPENDIX A

SPECIFICATIONS

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A.2 Dimensions A-2

FIGURES

Figure A-1 CPCI2PMC-1 Dimensions A-2

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A.1 Specifications

The CPCI2PMC board's physical and operating characteristics are:

MECHANICAL

Measurements:	Length: 9.187 inches (233.35 mm) Width: 6.299 inches (160 mm)
Weight:	240 grams; 8.416 oz (includes faceplate)
Board Thickness:	0.0635 inches, 0.16 cm, nominally, (8 layers)

ELECTRICAL

Power (No modules installed)	+12 Vdc @ 0.0 Amps, -12 Vdc @ 0.0 Amps
Power (Intel 21152)	P_{WC} = 1.2 W @ 33 MHz
Power (for each regulator)	P_{WC} = 4.57 W (calculated using 7.5 W maximum allowable power dissipation for each PMC per CMC Draft Standard) I_{WC} = 2.27 A (provided by 5 V backplane)

RECOMMENDED OPERATING SUPPLY RATINGS

Supply Voltage with respect to ground:	+4.75 Vdc to +5.25 Vdc

ENVIRONMENTAL SPECIFICATIONS

Temperature:

Operating:	0°C to +70°C
Storage:	-40°C to +85°C
Humidity (Noncondensing)	5% to 95%

MEAN TIME BETWEEN FAILURE

*MTBF	1,447,720 hours per MIL-HDBK-217F
Bellcore Issue 6	2,226,633

* The MTBF numbers below are based on calculations using MIL-HDBK-217F Appendix A, for a ground benign environment.

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A.2 Dimensions

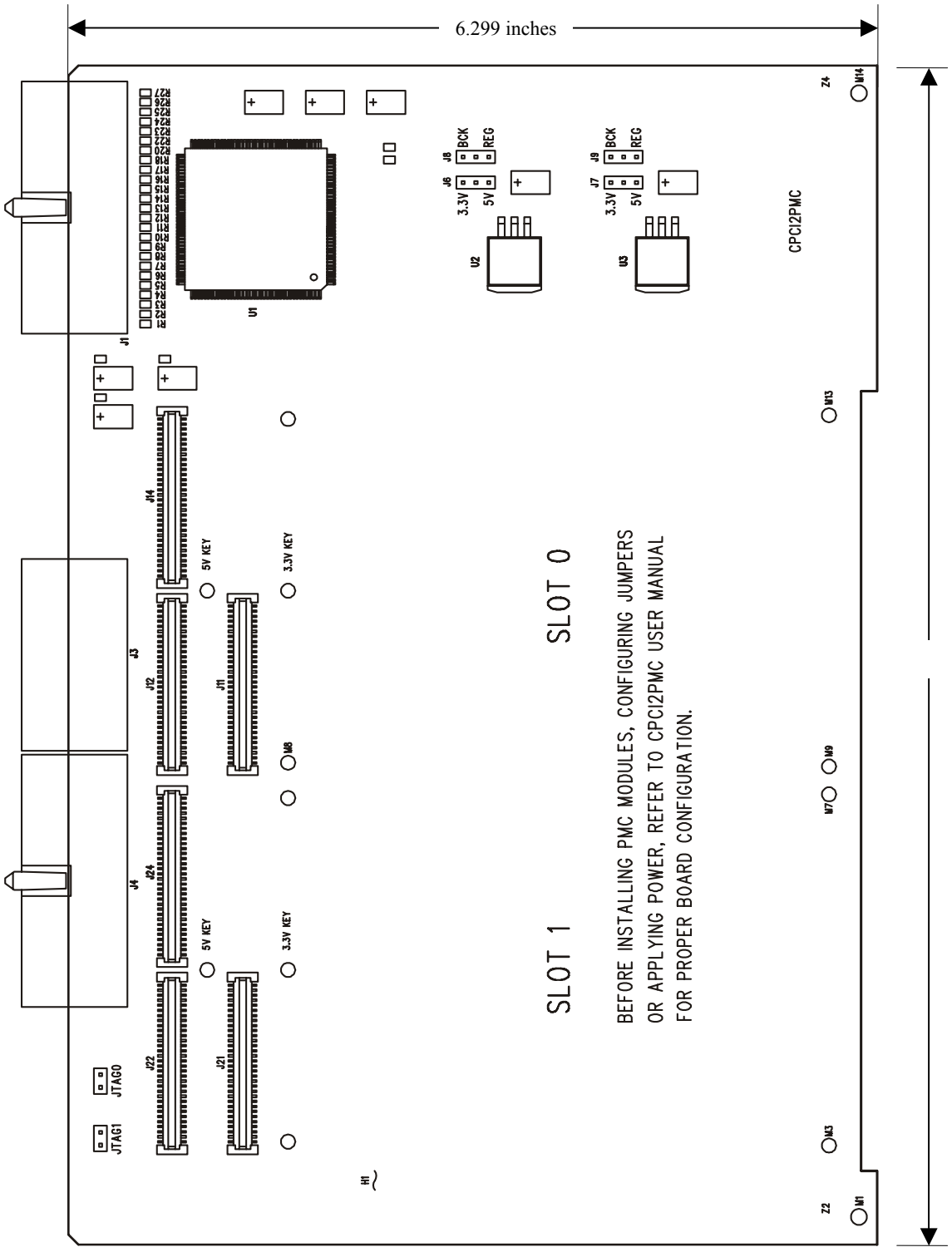


Figure A-1 CPCI2PMC-1 Dimensions

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APPENDIX B

TYPICAL APPLICATIONS

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B.1 Overview

Curtiss-Wright Controls, Inc. extends an open invitation to all users to freely submit their applications that might, or do, use the CPCI2PMC Slave Carrier to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Curtiss-Wright team, while simultaneously publishing your ideas. Submission constitutes permission to publish without additional consent or compensation, and Curtiss-Wright Controls, Inc. reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 COTS PMC Modules

The CPCI2PMC is a two-slot, PMC Module Carrier board to be used as a PMC-to-CompactPCI adapter that will accept any 32-bit 5 V/3.3 V standard length singlewide or doublewide Commercial Off The Shelf (COTS) PMC module that adheres to the design specifications listed below:

- PCI Local Bus Specification, Revision 2.1
- Draft standard for a common mezzanine card family: CMC (IEEE P1386/Draft 2.0)
- Draft standard physical and environmental layers for PCI Mezzanine Cards: PMC (IEEE P1386.1/Draft 2.0)

B.3 Curtiss-Wright PMC Modules

Curtiss-Wright Controls, Inc. offers a wide range of networking-solution PMC modules that can be used with the CPCI2PMC carrier board.

B.3.1 SCRAMNet SC150e PMC

SCRAMNet (Shared Common Random Access Memory Network) is a real-time applications communications network based on a replicated, shared-memory concept.

The SCRAMNet SC150e PMC board is mounted on any PMC-compliant carrier board in the computer chassis.

The on-board shared memory can be 2 MB, or 4 MB random access memory (RAM). Memory is installed at the factory.

PMC BOARD FEATURES

- General Purpose Counter.
- Error Interrupt Mask.
- Dynamic shared-memory addressing.
- Virtual paging for Shared Memory (CSR selectable).
- Variable-length message packet capability.
- Dual-port memory.
- Dual memory and error interrupt.

PMC SPECIFICATION LEVEL

The SCRAMNet SC150e PMC board was designed in accordance with the PCI Local Bus Specification 2.1.

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HARDWARE

- 32-bit PMC compliant
- Supports bus level interrupt INTA#
- Maximum bus clock speed is 33 MHz
- Less than 1.5 amps @ 5 volts
- V3 Byte Swapping

B.3.2 FibreXpress PMC

The FibreXpress (FX) Network is a standards-based Fibre Channel (FC) network designed to meet the requirements of the real-time computing industry. The superior communication and interconnect capabilities of the FC standard are maximized by the design of the FX Network.

Curtiss-Wright Controls' FibreXpress PCI and PMC boards, also called Host Bus Adapters (HBA), are ANSI-Standard boards for Fibre Channel communications on host nodes. The FX PCI and FX PMC boards mount into any PCI or PMC compliant carrier, respectively.

FX boards provide interconnection for a wide range of popular bus architectures and for other FC products that comply with ANSI FC standard revision 4.3.
FX software device drivers, which provide support for numerous protocols under a variety of popular operating environments, are continually under development at Curtiss-Wright Controls. Please refer to the appropriate software driver manual for information on installation and use of the software drivers.

The interface between the FX PCI or PMC board and the PCI Local Bus is provided by a V3 PCI Local Bus Controller ASIC. This interface supports both master and slave operations and has a complete interrupt capability built into it.

Other FX boards have the interface to the network incorporated as an integral part of the board to accommodate height restrictions and cost effectiveness. The versatile FX board can operate in any topology specified by the Fibre Channel standard. These topologies are: point-to-point, switched fabric, and arbitrated loop.
There are two interfaces on the FX board:

- A host bus interface used for communication with a host computer
- A physical media or Fibre Channel interface used for communication with other Fibre Channel entities

NETWORK FEATURES

Fibre Channel communication provides a practical, inexpensive, yet expandable method for achieving high-speed data transfer among workstations, mainframes, supercomputers, desktop computers, storage devices, and display devices. Processors can connect to other processors or to peripherals over distances of up to 10 km per link.

Some network features are listed below:

- Includes all the protocol necessary to effect end-to-end communications in the physical layer. These protocols are implemented in hardware.
- Supports a switched topology that provides a bandwidth that is linearly scaleable to the number of nodes connected.
- Supports a low-cost loop architecture with full functionality and connectivity to the switched architecture.

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- Supports a switched point-to-point architecture that insures deterministic performance.
- Supports a loop architecture that offers fairness and deterministic performance.
- Supports a variety of baud rates (266, 531, and 1062 megabits per second) in both copper and optic media. This versatility results in a vast cost performance matrix that enables solutions to be cost effectively tailored to the problem space.
- Supports an architecture that in turn supports a flow control, which allows stations operating at different baud rates to communicate with each other through a fabric.
- Minimizes implementation cost and enhances throughput by using a simple protocol.
- Isolates transmission medium from the control protocol so that implementation of point-to-point links, loops, crosspoint switches, or other special requirements may be made in a technology best suited to the application environment of the user.
- Has a framing protocol that allows several other protocols—such as TCP/IP, SCSI, HIPPI, and others—to be easily ported.
- Has a built-in protocol that aids the management of link operation, performs error recovery, and provides link and port status information.

HOST BUS INTERFACE

The FX board occupies a piece of PCI memory space. The board can be either a PCI Local Bus master or slave:

- The bus master function is used for optional DMA (Direct Memory Access) transfers between on-board memory and host memory.
- The slave function is used for programming on-board resources and, in some cases, for accessing on-board buffer memory.

PHYSICAL MEDIA INTERFACE

The physical media interface for the FX board can be either optical fiber or copper twinax. This multi-functionality is accomplished through a built-in link interface.

BOARD FEATURES

Both the FX PCI and PMC boards have the following features:

- Offers Fibre Channel data transfer rate of 1062 megabits per second (Mbps)
- On-board (Static Random Access Memory or SRAM) buffer memory sizes of 1 megabyte (MB)
- Supports the Fibre Channel Systems Initiative (FCSI) IP profile
- Supports the FCSI SCSI FCP profile
- Supports optical or twinaxial media
- Has Fibre Channel service support for Classes 1, 2, and 3
- Has an interrupt controller to report link failure, transaction completion, or buffer space request
- Has status LED that reports link stability
- Has an intelligent Fibre Channel ASIC with multi-channel DMA engine and queue management
- Is configured through configuration and operations registers
- Is capable of generating a PCI Local Bus interrupt

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- Has a PCI target/slave interface capable of 132 megabytes per second (MBps) throughput
- Has a programmable Little- (PCI) to Big- (FC) Endian byte swapper

PCI LOCAL BUS SPECIFICATION LEVEL

The FX PCI and PMC boards were designed in accordance with the PCI Local Bus specification Revision 2.1.

OPTIONS

Curtiss-Wright Controls, Inc. offers the following options:

- Data rate of 1062 Mbps
- Memory size of 1 MB (FX)
- Software Driver
- LinkXchange Network Transparent Switch
- Cables

B.3.3 1553 Solutions PMC

The GLD+PMC and GLD+PMC/S provide a powerful and convenient interface between a host computer and a MIL-STD-1553 data bus. The GLD+PMC is capable of operating in Bus Controller (BC), Multiple Remote Terminal (MRT), and Chronological Monitor (CM) modes simultaneously or independently. The GLD+PMC/S operates singularly as a BC, MRT or CM. All MIL-STD-1553A or B protocol communication between emulated devices occurs over the 1553 bus, rather than through a local bus. The three operating modes provide extensive bus protocol error detection, such as parity error and no response. The GLD+PMC also has the ability to inject protocol and/or electrical errors into the 1553 bus traffic. The single-function GLD+PMC/S does not support error injection.

The GLD+PMC and GLD+PMC/S are offered in a single-channel (1A and 1B bus) configuration. The boards contain 64 K of 16-bit dual-port Random Access Memory (RAM) which is mapped into the PCI memory space. They use a high-speed controller in conjunction with the RAM to provide a complete, intelligent 1553 emulation system. Using on-board data structures located in the dual-port RAM, the board is capable of sustaining operation on the bus without host intervention. In addition, the CM stores commands, status responses, gap times and time tags within the same buffer.

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GLOSSARY

arbitrated loop ----------Fibre Channel topology where L_Ports use arbitration to establish a point-to-point circuit without hubs or switches.

ASIC ----------Application-Specific Integrated Circuit.

BC ----------Bus Controller (1553 bus).

CPCI ----------CompactPCI. Also refers to any mechanically-based characteristics of the CPCI2PMC, including the J1 connector for interfacing to the host via a backplane.

CM ----------Chronological Monitor (1553 bus)

CSR ----------Control and Status Registers.

COTS ----------Commercial, Off The Shelf products.

DMA ----------Direct Memory Access.

fabric ----------A self-managed, active, intelligent switching mechanism that handles routing in Fibre Channel Networks.

FCSI ----------Fibre Channel Systems Initiative.

FibreXpress (FX) Network ------A standards-based Fibre Channel (FC) network which meets the requirements of the real-time computing industry and maximizes the superior communication and interconnect capabilities of the FC standard.

HBA----------Host Bus Adapter.

HIPPI ----------High Performance Parallel Interface. An 800 Mbps interface to supercomputer networks (previously called high-speed channel) developed by ANSI.

LED ----------Light Emitting Diode.

LinkXchange ----------Logo/name of the Systran Network Transparent Switch.

MRT ----------Multiple Remote Terminal (1553 bus).

PIO ----------Programmed I/O.

RAM ----------Random Access Memory.

SCRAMNet ----------Shared Common Random Access Memory Network is a real-time applications communications network based on a replicated, shared-memory concept.

SCSI ----------Small Computer System Interface.

SRAM ----------Static Random Access Memory.

switched fabric ----------(see the definition for “fabric”).

TCP/IP ----------Transmission Control Protocol/Internet Protocol.

MTBF ----------Mean Time Between Failures

ns, µs, ms ----------Nanoseconds, microseconds, and milliseconds, respectively.

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