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10089 Hardware/Software Manual

Buffered VMEbus DR11-W Emulator

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10089 Hardware/Software Manual

Buffered VMEbus DR11-W Emulator

Ikon Corporation

1. Introduction

This manual contains programming and hardware set-up information for the etched-board version of the IKON Model 10089 VMEbus DR11-W emulator. The Model 10089 is an emulation of a Digital Equipment Corporation DR11-W and will support any device or application supported by the DEC product with the exception of the "exotic" addressing modes controlled by the WC INC ENB, BA INC ENB, C0 CNTL, and A00 input signals.

The 10089 is a software-transparent replacement for the older Model 10084. (Use the 10084 for applications requiring the "exotic" addressing modes.) The '89 incorporates a 32 bit data path and FIFO buffers in its DMA output logic and double-buffering in its DMA input logic for increased throughput and bus efficiency when compared with the 10084. It can do DR11-W external DMA handshakes in as little as 300ns, with a maximum throughput of 6M+ bytes/second for output and 4M+ bytes/second for input transfers.

The DR11-W emulator is a high-speed parallel DMA interface which may be used in interprocessor links based on cross-coupled DR11-Ws or emulators. Linkable systems include VAX, LSI-11, PDP-11, Gould/Sel, Data General, Prime Harris, Perkin-Elmer, and IBM using other manufacturer's DR11-Ws, and Multibus, VERSAbus and VMEbus systems using IKON's family of DR11-W emulators.

The 10089 can also be used to connect the VMEbus to almost any peripheral device, network node, mainframe channel interface, or workstation with a DR11-W type interface -- including a wide variety of graphics equipment made by several manufacturers.

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NOTE: The following registered trademarks are used in this manual for descriptive purposes to identify compatibility:

VERSAbus - Motorola, Inc.

Multibus - Intel Corporation

DEC, PDP-11, VAX, LSI-11 - Digital Equipment Corporation

2. General Specifications

Slave Mode Access

16 bit I/O map or 24 bit standard map with switch-selectable address.

PAL-selectable address modifier decode. Standard factory PAL responds to hex modifier codes of 29 and 2D in the I/O map and 39, 3A, 3D, and 3E in the standard map.

Interrupts

Jumper-selected interrupt level with software-selected vector.

DMA

32 bit linear address generation with 16 or 24 bit range (word) counter for up to 32M byte DMA blocks anywhere in VME address space.

DMA logic is all-bipolar with a 20MHz clock for maximum speed and bus efficiency.

Jumper-selectable bus priority.

Multiple word or longword per arbitration in output mode. Single word per arbitration in input mode. Early BBSY* release in either mode--allowing concurrent arbitration for maximum bus efficiency.

External Interface

All DR11-W I/O modes supported, except external address and range counter incrementation control, transfer direction control, and byte mode DMA.

Input de-skew and output settling times jumper selectable.

Cycle request (CRQA & B) and BUSY polarities jumper

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selectable.

I/O connectors and pin-out identical to DEC format.

All input signals received with high-hysteresis unified bus type recievers. All output signals driven with high current (70mA) unified bus type open-collector drivers (transceivers).

Optional byte swapping to and from the external device with separate switches for p-I/O and DMA.

Power and Environmental

Power consumption - 3.9A

Commercial temperature range and humidity to 90% non-condensing.

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3. Detailed Hardware Specifications

All timings are typical.

Slave Mode

DS0* and DS1* L.E. to DTACK* L.E.	700ns
D00-D15 driven to DTACK* L.E.	400ns
D00-D15 released to DTACK* T.E.	30ns
DS0* or DS1* T.E. to DTACK* T.E.	80ns
DS0* or DS1* L.E. to A01-23, IACK, WRITE* latched	100ns
DS0* or DS1* L.E. to D00-15 latched	450ns

Interrupts

DS0* and IACKIN* L.E. to DTACK*	700ns
D00-D07 driven to DTACK* L.E.	100ns
D00-D07 released to DTACK* T.E.	30ns
DS0* T.E. to DTACK* T.E.	80ns
DS0* and IACKIN* L.E. to IACKOUT* L.E.	300ns
AS* T.E. to IACKOUT* T.E.	40ns

DMA - Data Transfer Timing

internal grant and bus available to bus driven	50ns
A01-A23, WRITE*, IACK*, LWORD* driven to AS* L.E.	75ns
D00-D15 driven to DS0* or DS1* L.E.	75ns
AS* L.E. to DS0* or DS1* L.E. (memory read)	5ns
AS* L.E. to DS0* or DS1* L.E. (memory write)	50ns
DTACK* L.E. to A01-A23 released	50ns
DTACK* L.E. to D00-D15 released	50ns
DTACK* L.E. to DSTB* T.E. (memory read)	130ns
DTACK* L.E. to DSTB* T.E. (memory write)	50ns
DS0* or DS1* T.E. to WRITE* released	50ns
All bus and strobe signals released to AS* T.E.	0ns
AS* T.E. to AS* released	5ns

DMA - Bus Arbitration

BGxIN* L.E. to internal grant	70ns
BGxIN* L.E. to BBSY* asserted	70ns
BBSY* asserted to BRQx* released (min)	50ns

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BBSY* asserted (min)	150ns
AS* asserted to BBSY* released	50ns
BGxIN* to BGxOUT*	75ns

Bus Interface

All bus and strobe receivers 74LS245 or equivalent.

All bus transceivers (data bus only) 74ALS646-1 or equivalent.

All bus drivers 74LS645-1 or equivalent.

All strobe drivers 74F241 or equivalent.

All open collector drivers 74S38 or equivalent.

External Interface

All external signals terminated with 180 ohms to vcc and 390 ohms to ground.

All external input signals received with 8T37 type hex receivers with 1v hysteresis (1v and 2v thresholds).

All external output signals driven with 8T38 type open-collector transceivers with 70mA sink capability.

Input de-skew (cycle request - CRQA or B - to input data latched) jumper-selectable 100, 150, 200, or 300ns.

Output settling time (data valid to BUSY trailing edge) jumper-selectable 40,90,140, 240ns.

END CYCLE H pulse 100ns.

ACLO FNCT2 H, INIT H, GO H pulses 300ns.

FNCT1, 2, 3 signals change with the leading edge of GO H (these bits may also be changed without pulsing GO H).

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4. On-Board Registers

The Model 10089 on-board registers occupy a 32 byte block of addresses which may be located anywhere in the VME standard map or short I/O map. Address and map selection is via switches. The address modifier codes recognized for each map are PAL determined and may be modified if necessary. See the general specifications for standard modifier codes supported.

The low order five bits of the system address (actually 4 bits + two data strobes on the bus) are used to determine which on-board register is being accessed. The remaining address bits and the address modifier codes are examined to determine when the board is being addressed.

All on-board registers may be read as bytes or words. Only word writes are allowed, with the exception of the modifier and interrupt vector register which may be written as two separate bytes, and the High DMA Range Count register which is only 8 bits wide and may be written as a word or byte. Longword accesses to these registers are not allowed.

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4.1. On-Board Register Addressing

xxxx + 4 bits switch selectable -- all values in hex

Address	Write	Read
xxxx00	Control	Status
xxxx02	Data Out	Data In
xxxx04	Modifier+Vector	Modifier+Vector
xxxx04	(byte) Modifier	(byte) Modifier
xxxx05	(byte) Vector	(byte) Vector
xxxx06	Pulse Command	
xxxx08		
xxxx0A		
xxxx0C		
xxxx0E		
xxxx10		
xxxx12	DMA Address Low	
xxxx14	DMA Range Low	DMA Range Low
xxxx16		DMA Address Low
xxxx18		
xxxx1A	DMA Address High	
xxxx1C	DMA Range High	DMA Range High
xxxx1E		DMA Address High

Note that the DMA Address registers have different read and write addresses. A value written to the DMA Address Low register at offset xxxx12 will be read back at xxxx16. This is done to preserve software compatibility with IKON's other DR11-W emulators.

The DMA Range High register is enabled by a jumper option. This 8-bit register may be written and read, but has no

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effect unless enabled.

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4.2. Register Formats

For all 16 bit registers, bit 15 is the most significant bit. Bit 7 is the MSB for all 8 bit registers.

Control

Bit	Name-Signal	Function
15	RDMA	reset DMAF and BERR flags
14	RATN	reset ATTF flag
13	RPER	reset PERR flag
12	MCLR	master clear board and pulse INIT H
11		
10		
09		
08	CYCL	force DMA cycle
07	TERM	terminate DMA
06	IENB	enable-disable interrupts
05		
04	SDIR	software direction control
03	FCN3	FNCT3 H signal
02	FCN2	FNCT2 H signal
01	FCN1	FNCT1 H signal
00	GO	pulse GO H signal & enable DMA

RDMA Writing a 1 to this bit resets the DMA end of range flag and associated interrupt, if set. It also clears the bus error flag.

RATN Resets the attention flag bit and its associated interrupt.

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RPER Resets the parity error flag if set.

MCLR Resets all latched functions and flags in the interface, terminates DMA, and pulses the INIT H signal to the external device. Produces the same effect as SYSRESET* from the VMEbus.

CYCL Forces an immediate DMA cycle if DMA is enabled. This bit is the software equivalent of an external cycle request.

TERM Writing a one to this bit terminates DMA if active and sets REDY without sending an INIT H pulse to the external device.

IENB This is the master interrupt enable bit for the interface. If it is a 1, the interface will place an interrupt request on the bus whenever ATTF or DMAF is set. Interrupts may be disabled by setting this bit to 0. Note that IENB is reset during an interrupt acknowledge sequence, or by MCLR or SYSRESET* from the VMEbus.

SDIR This bit is an optional DMA data transfer direction control bit. This board requires that the direction of data transfer be known prior to issuing the GO pulse--unlike the DEC DR11-W which can change transfer direciton on a word-by-word basis. If the external device can't meet this requirement the SDIR bit can be used instead of the C1 CNTL or FNCT1 signals to determine the direction of data transfer. Setting this bit to ONE sets the board up for DMA input to memory. Setting this bit to ZERO sets the board up for DMA output. See the Hardware Switch and Jumper Options section of this manual for further details.

FCNx The three function bit latches drive the FNCTx H signals to the external device. They may be set to 0 or 1, and are reset to 0 by MCLR or SYSRESET* on the VMEbus. FCN1 may optionally be used to control DMA transfer direction. FCN2 also drives the ACLO FNCT2 H signal.

GO The go bit pulses GO H to the external device and enables DMA transfers. Whether DMA transfers actually occur depends on the external device and the FIFO pre-load jumper option, and whether the software issues a cycle request.

The above functions which are pulses--GO, CYCL, MCLR, TERM, RPER, RATN, RDMA, and pulsed forms of IENB and FCN2--are also available in the Pulse Command register.

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Status

Bit	Name-Signal	Function
15	DMAF	DMA end-of-range flag
14	ATTF	attention flag
13	ATTN	state of ATTENTION H
12	PERR	parity error flag
11	STTA	state of STATUS A input
10	STTB	state of STATUS B input
09	STTC	state of STATUS C input
08	0	
07	REDY	interface ready indication
06	IENB	interrupt enable latch
05	BERR	bus error flag
04	SDIR	state of SDIR latch
03	FCN3	state of FCN3 latch
02	FCN2	state of FCN2 latch
01	FCN1	state of FCN1 latch
00	DFLG	device flag

DMAF — DMA end-of-range flag. Set by last transfer in block, or when DMA is terminated by ATTENTION H. Causes an interrupt if IENB is true (1). Reset by MCLR, RDMA, or SYSRESET* from the VMEbus.

ATTF — Set by a false-to-true transition on the ATTENTION H input. ATTF will cause an interrupt if IENB is true. Reset by MCLR, RATN, or SYSRESET* from the VMEbus.

ATTN — This bit follows the state of the ATTENTION H input.

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PERR — The parity error flag is set by an external (DR11-W) parity error during a DMA input or p-I/O read. It is reset by MCLR, RPER, or SYSRESET* from the VME-bus, but otherwise will stay true once set by an error. Note that parity is an IKON-only enhancement to the DR11-W specification and will work properly only when this interface is connected to a device which implements parity on the DR11-W I/O signals. A bad parity indication will not halt transfers. This is only a status bit and does not affect the board's data transfer logic. In general, when connected to a device that does not implement IKON's DR11 cable parity, this bit will set frequently, and should be ignored by the software. Alternatively, parity reporting may be disabled with jumpers. (See the Hardware Options section of this manual)

STTx — The STTx bits follow the state of the STATUS x inputs.

REDY — This bit reflects the state of the READY H output and indicates that the interface is ready for another command, such as GO. When REDY is false it indicates that the interface has been enabled to do DMA (by GO) and that the external device may issue cycle requests. REDY is reset by GO and set by MCLR, TERM, SYSRESET* from the VMEbus, DMA end-of-range, or ATTENTION H.

IENB — This bit reflects the state of the interrupt enable latch.

BERR — This bit is set by a VMEbus error during DMA. It is reset by MCLR, RDMA, or SYSRESET* from the VMEbus.

SDIR — This bit reflects the state of the SDIR latch.

FCNx — These bits indicate the states of the function bit latches, and are primarily diagnostic in nature.

DFLG — May be used to indicate to the software that this board is a 10089 rather than a 10084. The older 10084 always shows a zero in this bit position. The state of this bit is jumper-selectable in the 10089.

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Data Out

Data written to this register is latched and presented to the external device via the DO00-DO15 output signals. This register is also used during DMA output and should not be written when REDY is false for output.

Odd parity over 17 bits is maintained for output data. The 17th bit (POXX H) replaces a GROUND pin in the DEC DR11-W specification. Its use is optional.

NOTE: The Data Out Register is un-available to the program during DMA output, and any time that REDY (and READY H) is false for a non-dma command. If a GO-initiated command, whether involving DMA or not, is not terminated by DMA end-of-range or ATTENTION, it should be terminated with TERM in the Control or Pulse Command Registers, or later writes to the Data Out Register may not function correctly.

See also the FIFO Pre-load jumper option in the Hardware Switch and Jumper Options section of this manual.

Data In

This register contains the current state of the DI00-DI15 input signals from the external device. It is used during DMA input and should not be read when REDY is false for input. Parity is checked whenever this register is read by the program or by DMA input.

Odd parity over 17 bits is checked on input data and PIXX H.

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Address Modifier and Interrupt Vector

Address Modifier -- High byte of combined register

15	14	13	12	11	10	09	08
x	x	AM5	AM4	AM3	AM2	AM1	AM0

Interrupt Vector -- Low byte of combined register

07	06	05	04	03	02	01	00
D07	D06	D05	D04	D03	D02	D01	D00

This is a pair of 8 bit registers that may be written and read separately or combined as a 16 bit word. The Address Modifier is the bit pattern that will be applied to the address modifier lines of the VMEbus when the interface is the bus master (DMA). There are several possible address modifier values; all are somewhat system dependent. Consult documentation for the target system, and the VMEbus technical specification for appropriate values. Note that there are only 6 address modifier lines on the VMEbus, and that they correspond to the low order 6 bits of the 8 bit address modifier register.

On most systems, an address modifier of (hex) 3D will work for 24 bit addressing, and a value of (hex) 0D will work for 32 bit extended addressing.

The 8 bit value in the interrupt vector register is applied to the low order byte of the VMEbus during an interrupt acknowledge cycle. The VMEbus specification refers to this byte as the status-id byte. Its use is system dependent; typically it is multiplied by four (by the interrupt handler) and used as an index into a dispatch table. Consult the appropriate target system documentation for suitable values for this register.

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Pulse Command

Bit	Name-Signal	Function
15	RDMA	reset DMAF and BERR flags
14	RATN	reset ATTF flag
13	RPER	reset PERR flag
12	MCLR	master clear board and pulse INIT H
11		
10		
09		
08	CYCL	force DMA cycle
07	TERM	terminate DMA
06	SMSK	set IENB
05	RMSK	reset IENB
04		
03		
02	FCN2	pulse ACLO FNCT2 H
01		
00	GO	pulse GO H signal & enable DMA

All bits in the Pulse Command register are pulsed functions which only affect interface and device functions when written as 1s. Writing a 0 to any of these bits has no effect. They are included as a convenience to allow the programmer to generate pulses without having to worry about the static, latched functions in the Control register. This eliminates always having to carry a copy of the Control register and 'or' in the pulse bits. It also allows pulsing the ACLO FNCT2 H (typically used to interrupt the external device) without having to set FCN2 to 1 and then 0.

SMSK This bit does a pulsed set of the interrupt enable latch. Writing a 1 to this bit sets the latch. Writing a 0 has no effect.

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RMSK Writing a 1 to this bit clears the interrupt enable latch. Writing a 0 has no effect.

FCN2 Writing a 1 to this bit pulses the ACLO FNCT2 H output. Writing a 0 has no effect. Note that the ACLO signal is the 'or' of this pulse and the FCN2 latch in the Control register.

See the Control register section of this manual for a description of the other bits in this register.

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DMA Address

The DMA address register is a 31 bit counter that is accessed by the program as a pair of 16 bit registers. Note that register bit 00 maps onto address bus bit 01, and so on. Any address value in this register is effectively multiplied by 2 before being applied to the bus. Prior to enabling the DMA mechanism, this register is loaded with the buffer starting address divided by 2 (right-shifted one place). After each DMA transfer the register is incremented by 1. This counter may be as many as 48 words ahead of the external device in output mode, and 1 word behind the device in input mode, but will be in synch with the device at end-of-range.

DMA address register to VMEbus address bus correspondence

DMA Address Low

07	06	05	04	03	02	01	00
A08	A07	A06	A05	A04	A03	A02	A01

15	14	13	12	11	10	09	08
A16	A15	A14	A13	A12	A11	A10	A09

DMA Address High

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

15	14	13	12	11	10	09	08
x	A31	A30	A29	A28	A27	A26	A25

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DMA Range Count

The DMA range counter is a 16 bit register that controls the number of words transferred to the external device during a DMA block transfer. Prior to starting the DMA mechanism, this counter is set to the number of words to be transferred minus 1. During each DMA transfer the counter is decremented by one. When the range counter goes negative, further DMA transfers are inhibited, the READY H output and REDY bit are asserted, the DMAF flag is set, and an interrupt is generated if enabled. This counter may be as many as 48 words ahead of the external device in output mode, but will be in synch with the device at end-of-range.

An on-board jumper option allows the range count register to be expanded from 16 to 24 bits, providing a maximum block size of 32M bytes to be transferred in a single operation. If the 24 bit range counter option is enabled, the upper 8 bits of the 24 bit counter are accessed as the DMA Range Count High register and MUST be set to an appropriate value before enabling DMA transfers.

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5. External Signals

It is important to understand the pin-numbering convention used by the IKON family of DR11-W emulators, and how this convention relates to the DEC scheme.

The 10089 external connectors correspond exactly--both electrically and physically to the DEC connectors. This means that the pin labelled on the connector as pin 1 (usually by an arrow or equivalent) corresponds to the DEC pin designated VV. The fact that DEC numbers (letters!) their pins in reverse order when compared to the physical connectors used has caused all kinds of grief to the customer trying to install DR11-W compatible products in a computer system. Some designers have chosen to make pin 1 correspond to DEC pin A which produces a connector that is physically backward from the DEC product--and only adds to the confusion.

A further confusing factor is that the preferred cables are assembled with a stripe on the pin 40 end! This is necessary since the cable's internal ground plane drain wire is at the striped end of the cable and must be terminated to pin 40.

Customers using this or any other DR11-W compatible product must determine from their various suppliers which pin numbering convention is used, and whether the cables need a half-twist between the connected devices. IKON cables are keyed, and can only be plugged in correctly at the IKON end.

It is strongly recommended that IKON's ground-plane cables or their equivalent be used for DR11-W applications. Ordinary ribbon cables have unsuitable impedance control and cross-talk characteristics when used with the DR11-W pin-out and may adversely affect data integrity.

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Signals to External Device

All signals asserted when high

DO00-DO15 H	Output data lines. DO15 H is the msb. These lines follow the state of the Output Data register which is written by the program or by DMA output.
POXX H	This is the IKON-specified optional output parity signal. Odd parity is maintained over 17 bits (DOxx and POXX).
INIT H	Initialize signal to the external device. Asserted whenever the bus initialize signal SYSRESET* is true. Pulsed true for 250ns by writing a 1 to the MCLR bit in the Control or Pulse Command register.
FNCT1,2,3 H	User-defined function bits sent to the external device. Set by writing to the FCNx bits in the Control register. These bits change with the leading edge of GO H (if it is written--it is not necessary to pulse GO to change these bits).
READY H	Corresponds to the REDY bit in the Status register. When false it indicates that the DMA mechanism has been enabled and that the external device may issue cycle requests. It is set false by GO in the Control register and is set true by MCLR, TERM, system reset, DMA end-of-range, or ATTENTION H. At end-of-range it will be true at approximately the same time that the data would become stable in output mode, or at approximately the same time as the input data latch time in input mode. These timings are affected by the DMA timing jumper settings in the same way as the input and output data timings. There is a jumper option that causes the READY H signal to go high at the leading of the END CYCLE H pulse in both input and output mode. This is provided for compatibility with some DR11-B applications.
BUSY H	Indicates that the 10089 has received a valid cycle request and is doing a DMA cycle. The trailing edge of BUSY H indicates that the DMA cycle is complete and that the device may read the DOxx lines (if an output cycle) and issue another cycle request. The delay from stable output data to the trailing edge of BUSY H is jumper selectable.

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BUSY H is normally asserted high. Its polarity is jumper selectable. In interprocessor link applications it is asserted low so that its trailing edge causes a cycle request at the other end of the link. Many external devices also require that BUSY H be asserted low. The device documentation should be consulted for correct BUSY H polarity.

ACLO FNCT2 H — This signal is set by writing to FCN2 in the Control register or pulsed for 300ns by writing to FCN2 in the Pulse Command register. It is typically used to pulse ATTENTION H or its equivalent in the external device.

GO H — A 300ns pulse caused by writing a 1 to GO in the Control or the Pulse Command register. The leading edge of GO H occurs simultaneously with the true-to-false transition of READY H. It may be used to indicate to the external device that DMA has been enabled, or may be used as a strobe to indicate that the FNCTx H lines should be read by the external device. In DMA output mode, the FIFOs will start to fill as soon as the the GO H pulse is issued. Some applications require that the GO H pulse be used for functions other than DMA. There is an on-board jumper option that inhibits FIFO loading unitl the external device or the software issues a cycle request. This avoids starting DMA accesses with every GO pulse.

END CYCLE H — This is a 100ns pulse that is simultaneous with the trailing edge of BUSY H. It may be used to strobe output data into the external device or instead of BUSY H as a handshake signal.

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Signals from External Device

All signals true when high.

Input terminations will hold floating inputs high.

All data inputs are latched following each cycle request. The latch delay (input de-skew) is jumper selectable in normal input mode, and system dependent in double buffered input mode.

DI00-DI15 H — Input data from the external device. DI15 is the MSB. The state of these lines may be read in the Data In register, or by doing DMA input. During normal DMA input these lines are latched a jumper-selectable delay after the cycle request is issued. During double buffered input mode, the input de-skew is system dependent, and requires that the external device keep the data inputs stable until the trailing edge of BUSY H.

The IKON-specified optional input parity line. Odd parity is tested for over 17 bits (DIxx and PIXX).

Not supported. The 10089 does not support byte addressable DMA inputs or read-modify-write sequences.

This input signal controls the direction of DMA data transfer. It must be stable prior to the trailing edge of GO H. This timing requirement will probably be met in most interprocessor link applications, since C1 CNTL H is looped back by the link cable and is actually driven by the local FNCT1 H signal. Jumper options on the board allow deriving the direction control signal directly from the outgoing FNCT1 H signal, or from the SDIR software direction bit in the Control Register if C1 CNTL H cannot be guaranteed to be stable in a given application.

CYCLE RQ A,B H — A 0-to-1 transition on either of these lines while the other is held low, or a simultaneous 0-to-1 transition on both inputs will request a DMA cycle. If READY H is high, or if BUSY H is true, cycle requests will be ignored. The end of the DMA cycle will be indicated by the END CYCLE H pulse and by the trailing edge of BUSY H. The input data and parity lines are latched a jumper-selectable

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delay after cycle request in normal input mode, and a system-dependent time after cycle request in double-buffered input mode.

The polarity of the cycle request inputs may be reversed (they will be falling edge active) by jumpers on the board. This may be useful when connecting to devices intended to interface to the DR11-B. With either polarity, the inactive input (typically CYCLE RQ B) should be held low. There is a jumper available on the 10089 to accomplish this if for some reason it is not possible for the external device to control CYCLE RQ B H.

ATTENTION H — The ATTENTION input signal can be used by the external device to terminate the DMA block (if DMA is in progress) and/or interrupt the CPU. ATTENTION H sets READY H and the REDY flag bit true and sets the ATTF flag bit in the Status Register. If ATTENTION H is used to halt DMA transfers, it should not be ussued from the time the device issues a cycle request until the end of the associated busy indication. If ATTENTION H is held true it inhibits the starting of further DMA blocks and holds the ATTN bit in the Status register true. Any input data in the input buffer when ATTENTION is received in double-buffered input mode will be input correctly as long as ATTENTION H is not issued while the last BUSY H is asserted.

STATUS A,B,C H — User defined input signals. They may be read as STTA, B, C in the Status register.

WC INC ENB H — Not supported.

BA INC ENB H — Not supported.

A00 H — Not supported.

BURST RQ L — Not directly supported. The 10089 will function correctly in DR11-W style burst mode, but will not actually be "hogging" the bus as requested by the external device. This will not be apparent to the device.

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Connector Pin-Out

J1 Pin-Out

IKON	DEC	Signal		DEC	IKON
1	VV	DO15 H	DO00 H	UU	2
3	TT	DO14 H	DO01 H	SS	4
5	RR	DO13 H	DO02 H	PP	6
7	NN	DO12 H	DO03 H	MM	8
9	LL	DO11 H	DO04 H	KK	10
11	JJ	DO10 H	DO05 H	HH	12
13	FF	DO09 H	DO06 H	EE	14
15	DD	DO08 H	DO07 H	CC	16
17	BB	POXX H	GROUND	AA	18
19	Z	CYCLE RQ B H	GROUND	Y	20
21	X	END CYCLE H	GROUND	W	22
23	V	STATUS C H	GROUND	U	24
25	T	STATUS C H	GROUND	S	26
27	R	STATUS B H	GROUND	P	28
29	N	INIT H	GROUND	M	30
31	L	STATUS A H	BURST RQ L	K	32
33	J	WC INC ENB H	GROUND	H	34
35	F	READY H	GROUND	E	36
37	D	ACLO FNCT2 H	GROUND	C	38
39	B	CYCLE RQ A H	GROUND	A	40

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J2 Pin-Out

IKON	DEC	Signal		DEC	IKON
1	VV	DI15 H	DI00 H	UU	2
3	TT	DI14 H	DI01 H	SS	4
5	RR	DI13 H	DI02 H	PP	6
7	NN	DI12 H	DI03 H	MM	8
9	LL	DI11 H	DI04 H	KK	10
11	JJ	DI10 H	DI05 H	HH	12
13	FF	DI09 H	DI06 H	EE	14
15	DD	DI08 H	DI07 H	CC	16
17	BB	PIXX H	GROUND	AA	18
19	Z	GROUND	GROUND	Y	20
21	X	GO H	GROUND	W	22
23	V	FNCT1 H	GROUND	U	24
25	T	C1 CNTL H	GROUND	S	26
27	R	FNCT2 H	GROUND	P	28
29	N	C0 CNTL H	GROUND	M	30
31	L	FNCT3 H	FNCT3 H	K	32
33	J	BA INC ENB H	GROUND	H	34
35	F	A00 H	GROUND	E	36
37	D	ATTN H	GROUND	C	38
39	B	BUSY H	GROUND	A	40

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6. Loopback Testing

The IKON model 10089, like most DR11-Ws and emulators is capable of extensive self-test. All programmed I/O, interrupt, and DMA features may be exercised and tested by 'looping back' the J2 connector to the J1 connector. This is done with a 40-conductor ribbon cable connected pin-for-pin between two 40-pin idc sockets. One of the standard IKON-supplied cables may be used for this purpose.

The signals connected in this way are shown below:

DO00-15 H	>	DI00-15 H
FNCT 1,2,3 H	>	STATUS C,B,A H
FNCT 1 H	>	C1 CNTL H
ACLO FNCT2 H	>	ATTENTION H
BUSY H	>	CYCLE RQ A H
POXX H	>	PIXX H

The loopback connection also causes (by virtue of the way the connector pin-outs line up) WC INC ENB H and BA INC ENB H to be asserted, and C0 CNTL H and CYCLE RQ B H to be held false. CYCLE RQ B H is the only one of these signals used by the 10089.

BUSY H should be jumpered for low-assertion.

When set up for loopback, the 10089's various features may be tested as follows:

Programmed I/O is tested by writing a value to the Data Out register and verifying that the value appears in the Data In register.

Function and Status bits are tested by writing the FCNx bits in the Control register and reading the resulting STTx bits in the Status register. Note that FCN1 corresponds to STTC, and that FCN2 will also cause the ATTN, and ATTF Status bits to change.

Interrupts and various pulse commands are tested by setting up the board's interrupt mask, and then generating an ATTENTION interrupt by pulsing ACLO FNCT2 H by writing a 1 to FCN2 in the Pulse Command register.

DMA output is tested by setting up the range and address registers, setting FCN1 to 0, and then pulsing GO and CYCL in the Control register or Pulse Command register. GO enables DMA, and CYCL actually initiates the first transfer. The end of the first, and later transfers cause BUSY H to go from low to high, which

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causes another cycle request, continuing the handshake until the range counter has been exhausted. End-of-range sets the REDY and DMAF flags in the Status register, and causes an interrupt, if enabled.

If the data buffer has been previously set to a known pattern, the last word of that pattern should appear in the Data In register when the DMA block transfer is complete.

DMA input is tested in the same way except that FCN1 is set to one before starting DMA. If a known value has been previously written to the Data Out register, it should be repeated in every word of the input buffer.

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7. Interprocessor Links

The IKON model 10089 may be used in a high-speed parallel interprocessor link with other IKON DR11-W emulators, or those made by DEC or other manufacturers. This technique of linking processors and systems produces very high transfer rates -as high as 4Mbytes/second- and can usually be implemented with a simple, efficient protocol.

The physical interprocessor link connection is made by connecting the J1 connector of each DR11-W to the J2 connector of the other DR11-w, and jumpering for BUSY H asserted low and Cycle Request rising edge active.

The signal connection accomplished is similar to loop-back, and is shown below.

DR11-W #1		DR11-W #2
DO00-15 H	>	DI00-15 H
POXX H	>	PIXX H
DI00-15 H	<	DO00-15 H
PIXX H	<	POXX H
BUSY H	>	CYCLE RQ A H
CYCLE RQ A H	<	BUSY H
FNCT 1,2,3 H	>	STATUS C,B,A H
STATUS C,B,A H	<	FNCT 1,2,3 H
FNCT1 H	>	(loop back
C1 CNTL H	<	to #1)
(loop back	<	FNCT1 H
to #2)	>	C1 CNTL H
FNCT3 H	>	BURST RQ L
BURST RQ L	<	FNCT3 H
ACLO FNCT 2 H	>	ATTENTION H
ATTENTION H	<	ACLO FNCT 2 H
CYCLE RQ B H	<	0
C0 CNTL H	<	0
A00 H	<	0
WC INC ENB H	<	1
BA INC ENB H	<	1
0	>	CYCLE RQ B H
0	>	C0 CNTL H
0	>	A00 H
1	>	WC INC ENB H
1	>	BA INC ENB H

Note that each device's C1 CNTL H (direction control) is derived from its own FNCT 1 H output. If the device sets its FNCT 1 H output, it will be doing an input into its associated memory.

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The exact software link protocol chosen is customer and application dependent, but most are based on the link protocol suggested by DEC in its DR11-W user's guide. This protocol involves exchanging single word messages via ATTENTION H interrupts to set up word count and data direction, and synchronize the start of DMA transfers. Block mode DMA accomplishes the actual data transfer. An example of an enhanced version of this protocol used by several of IKON's customers is available on request.

When ATTENTION H is used as part of a DMA protocol (typically driven by ACLO FNCT2 H as a clear-to-send indicator), it must be a pulse rather than a level. If the program that received the ATTENTION H signal attempts to start DMA while ATTENTION H is still asserted, DMA operation will be inhibited, and will not start when ATTENTION H is de-asserted. The end of the link generating the ATTENTION H signal should use a pulse that is as short as practical--which may be relatively long if more than one operating system call is required--and the end of the link receiving the ATTENTION H pulse should wait until it is removed before starting DMA.

The IKON Model 10089 Pulse Command register may be used to generate a 300ns ACLO FNCT2 H pulse at the IKON end of the link.

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8. Hardware Switch/Jumper Options

The options controlled by jumpers are listed below. The options set by switches are listed later under Board Address Selection.

jumpers connected	effect
W1-2	normal CYCLE REQ B
W2-3	CYCLE REQ B grounded
W4-5	parity errors reported in PERR
W5-6	PERR always 0
W7-8	BUSY asserted high
W8-9	BUSY asserted low
W10-11	READY true at BUSY T.E.
W11-12	READY true during BUSY
W13-14	CYCLE REQ falling edge active
W14-15	CYCLE REQ rising edge active
W16-17	no FIFO load until 1st CYCLE REQ
W17-18	FIFO loading starts with GO
W19-20	DFLG status bit = 1
W20-21	DFLG = 0
W22-23	16 bit range counter
W23-24	24 bit range counter
W25 through W34	FIFO burst length
W35 through W50	bus grant level
W51 through W58	bus request level
W59 through W72	interrupt request level
W73 through W86	interrupt ack level
W87-88	DMA direction set by SDIR bit
W89-90	DMA direction set by FCN1
W91-92	DMA direction set by C1CNTL

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Board Address Selection

The location of the 10089's on-board register set in the system memory map(s) is determined by switches at U55, U56, and U57.

U55		U56		U57	
1	A23	1	A15	1	A07
2	A22	2	A14	2	A06
3	A21	3	A13	3	A05
4	A20	4	A12	4	off=mem map, on=i-o map
5	A19	5	A11	5	off=16 bit DMA, on=32 bit
6	A18	6	A10	6	on=input dbl bfr enb
7	A17	7	A09	7	on=swap DMA bytes
8	A16	8	A08	8	on=swap p-i-o bytes

Note that the address selection switches are complemented. Any address switch set to on will decode a zero in that address bit position.

Switches U57-5 through 8 are not associated with address selection.

Address map selection is done with switch U57-4. If that switch is off, the board will respond to any of the four standard map address modifier codes: 39, 3A, 3D, and 3E. If switch U57-4 is on, the board will respond to either of the short I/O map address modifier codes: 29 and 2D.

DFLG Polarity

DFLG is a do-nothing bit in the LSB of the Status Register. It may be used to indicate to the software that the board is a 10089 rather than a 10084. If jumper pins W19 and 20 are connected, DFLG will be read as a 1. If jumper pins W20 and 21 are connected, DFLG will be read as a 0. This bit will always read as a 0 (zero) in the 10084 status register.

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Interrupt Level Selection

The bus interrupt level of the board is controlled by jumpers W59-72 and W73-86. The jumpers must be set to the same level.

W	INT RQ	W	INT ACK
71-72	IR1	73-74	IA1
69-70	IR2	75-76	IA2
67-68	IR3	77-78	IA3
65-66	IR4	79-80	IA4
63-64	IR5	81-82	IA5
61-62	IR6	83-84	IA6
59-60	IR7	85-86	IA7

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DMA Options

Bus Priority Selection

The bus priority level used by the board during DMA transfers is selected by jumpers W35-49 And W51-58.

The bus levels selected must agree!

Bus Request Selection

W	Bus Level
51-52	BR0
53-54	BR1
55-56	BR2
57-58	BR3

Bus Grant Matrix

Bus Grant	W	W	Internal Grant
BG0IN	36	35	BGIN
BG0OUT	38	37	BGOUT
BG1IN	40	39	BGIN
BG1OUT	42	41	BGOUT
BG2IN	44	43	BGIN
BG2OUT	46	45	BGOUT
BG3IN	48	47	BGIN
BG3OUT	50	49	BGOUT

The bus level to be used by this board is selected by jumpering the appropriate BGxIN pin to the adjacent BGIN pin, and the corresponding BGxOUT pin to the adjacent BGOUT pin. The three remaining bus levels are passed through the board by jumpering each level's BGxIN pin to its BGxOUT pin.

A board set up to use bus level 3 would have the following jumpers in place:

W36-38, W40-42, W44-46, W47-48, W49-50, and W57-58.

Consult target system documentation for information on selecting the appropriate priority level for this board.

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DMA Burst Length

The number of words per arbitration that are loaded into the fifos during a DMA output burst is set by jumpers W25-34.

W	Burst Length
25-26	16 Words per burst
27-28	8 Words per burst
29-30	4 Words per burst
31-32	2 Words per burst
33-34	1 Word per burst

The number of words per output burst will be as selected above, except that the first burst may be any number of words up to 1+ the number selected, and the last burst of a DMA block may be less than the number selected if the range counter underflows. (end-of-range is reached) If one word per burst is selected, exactly one word per burst will be transferred in all cases.

In input mode, only one word is transferred per arbitration regardless of the burst length selected.

32 Bit DMA Output

The 10089 is capable of reading data from VMEbus accessible memory 32 bits at a time. If Switch U57-5 is off, output data width on the bus will be 16 bits. If Switch U57-5 is on, output data width will be 32 bits, doubling bus efficiency. If this option is to be used, the VMEbus accessible memory must be capable of honoring 32 bit (longword) requests.

Dma input data width will be 16 bits regardless of the setting of this switch.

FIFO Pre-Load

For most applications, it is desirable for the board to begin loading its FIFO buffers as soon as a GO H is generated for DMA output. For some applications this may not be appropriate -- when the application doesn't do DMA after each GO H for instance. If jumper pins W17 and 18 are connected, the FIFOs will start to load as soon as a GO H for output is generated. If jumper pins W16 and 17 are connected, FIFO pre-load will be inhibited until the first CYCLE REQ A or B H is received from the device, or until a software cycle request is made.

Range Counter Extension

If jumper pins W22 and 23 are connected, the range counter

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will be 16 bits long. If jumper pins W23 and 24 are connected, the range counter will be 24 bits long, and the upper 8 bits must be set to an appropriate value prior to starting DMA.

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External Device I/O Options

Byte Swap

Switches at U57 control the byte ordering of data to and from the external device.

U57 switch	7	8
swap DMA data	ON	X
no DMA swap	OFF	X
swap P-I/O data	X	ON
no P-I/O swap	X	OFF

Parity

This hardware option is an extension of the DEC DR11-W specification. It replaces a ground pin with a parity signal which provides parity checking and generation (odd parity over 16 data bits + 1 parity bit) for all P-I/O and DMA data to and from the external device. It applies only the the external cable and does not involve VMEbus parity!!!!! The external device or other DR11-W must have matching parity logic to take advantage of this enhancement. All IKON DR11-W emulators support matching parity generation and detection circuitry, making them particularly useful in high speed interprocessor links where data integrity is important.

Outgoing parity is generated and latched whenever data is written to the Output Data register by P-I/O or DMA. Incoming parity is checked during P-I/O and DMA reads of the Input Data register. Any read parity error causes the PERR flag in the Status register to set and remain set until cleared by MCLR or RPER.

Jumper pins W4,5, and 6 control whether parity errors are reported in the status register. If jumper pins W4 and 5 are connected, external parity errors will be reported in the PERR bit in the Status Register. If jumper pins W5 and 6 are connected errors will not be reported and PERR will always be 0.

BUSY H Polarity

The jumper pins W7,8, and 9 control the polarity of the outgoing BUSY H signal. BUSY H is asserted LOW for interprocessor link operation and most general applications. It is asserted HIGH for what DEC calls 'device mode'. Consult target device documentation for appropriate polarity selection.

If jumper pins W8 and 9 are connected BUSY H will be

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asserted low. If jumper pins W7 and 8 are connected, BUSY H will be asserted high.

CYCLE RQ Polarity

Jumper pins W13,14, and 15 determine the active edge of the incoming CYCLE REQ A and B signals. The normal setting for DR11-W emulation is CYCLE RQ rising edge active.

If jumper pins W14 and 15 are connected, cycle requests will be rising edge active. If jumper pins W13 and 14 are connected, cycle requests will be falling edge active.

CYCLE REQ B Inhibit

If for some reason the device connected to the 10089 does not control CYCLE REQ B H, there is a jumper that may be used to ground this signal (it must be held low if CYCLE REQ A is to operate properly). If jumper pins W1 and 2 are connected, CYCLE REQ B H operates normally, and must be controlled by the device. If jumper pins W2 and 3 are connected, CYCLE REQ B H is grounded. This may be of use in DR11-B applications, where a special cable must be fabricated, and it is inconvenient to ground CYCLE REQ B H externally.

Transfer Direction Control

Unlike the DEC DR11-W, and some other DR11-W emulators, the 10089 requires that the direction of transfer be known by the DMA logic prior to the trailing edge of the GO H pulse. Normally the transfer direction is determined by the incoming C1 CNTL control line. If it is not possible for the external device to guarantee that this input will be stable prior to the end of GO H, there are two other options which may be used to determine transfer direction: direction may be controlled by the outgoing FNCT1 H signal (useful in link mode applications) or may be controlled by the SDIR software direction bit in the Control register. The direction option used is controlled by jumpers W87-92.

If jumper pins W91 and 92 are connected, direction is determined by the C1 CNTL H input. If jumper pins W89 and 90 are connected, direction is determined by FCN1 H. If jumper pins W87 and 88 are connected, direction is determined by the SDIR bit in the Control Register.

If the selected control signal/bit is asserted/set to 1, the transfer direction will be FROM the external device TO VME-bus memory.

Double-Buffered Input

The DEC DR11-W and IKON's other emulators require only that

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input data be stable at the active edge of CYCLE RQ, and be held for approximately 250ns. The 10089 complies with this specification in normal DMA input mode. It also incorporates a double-buffered input option that allows almost twice the input transfer rate. In double-buffered mode the imput data must be stable at the active edge of CYCLE RQ, and must be held until the trailing edge of BUSY H. The input data will be latched no sooner that 200ns after the active edge of CYCLE RQ.

Double-buffered input is enabled when switch U57-6 is ON.

In double-buffered input mode, the highest throughput will be achieved when the input de-skew time is set to its shortest setting with the input de-skew timing jumpers.

Output Data Settling Time

External data transfer timing is controlled by jumpers in the I/O timing matrix -- located between the J1 and J2 connectors, and labelled T0 through T3, IN A B and OUT A B. Output data settling time is determined by jumpers OUT A and OUT B. The OUT A and OUT B settings must match (T0 through T3 selection must be the same). The output settling time (data stable to BUSY H trailing edge) options are shown below.

Jumpers A&B	Settling Time
T0	40ns
T1	90ns
T2	140ns
T3	240ns

Input De-skew Timing

In normal DMA input mode the input de-skew time (CYCLE RQ active edge to input data latched) is determined by jumpers IN A and IN B. The IN A and IN B settings must match (t0 through T3 selection must be the same). The input timing options are shown below.

Jumpers A&B	Input De-Skew
T0	100ns
T1	150ns
T2	200ns
T3	300ns

The longer de-skew times may be appropriate when the application involves poor quality cables or under-specified line drivers or terminations in the external device.

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When double-buffered input operation is enabled, the shortest input de-skew time should be selected, for maximum throughput.

READY H Timing

In output mode, the READY H signal will go true during the last word of the block at approximately the same time that the data becomes stable -- as determined by the output timing jumpers. In normal input mode, READY H will go true prior to the trailing edge of the last BUSY H cycle of the block by an ammount of time approximately equal to the input de-skew time selected. In double-buffered input mode, READY H will go true approximately 40ns prior to the trailing edge of the last BUSY H.

If it is necessary to increase the separation between the rise of READY H and the trailing edge of BUSY (the device is not recognizing the rise of READY H - for instance) the output and input timing jumpers may be adjusted accordingly. Using an input timing setting other than the one recommended for double buffered input will reduce the maximum transfer rate somewhat, but may be appropriate if necessary to increase the READY to BUSY T.E. separation. The timing change will be approximately that listed for normal input mode.

It is also possible to delay the rise of READY H for DR11-B applications that require this. If jumper pins W11 and 12 are connnected, the READY H timing will be as described above. If jumper pins W10 and 11 are connected, the rise of READY H in all DMA modes will be approximately simultaneous with the leading edge of the END CYCLE H pulse.

It should be noted that the IKON DR11 emulators differ from the DEC DR11-W in one respect: in the IKON products, the trailing edge of BUSY H is simultaneous with the leading edge of END CYCLE H. For the DEC product, the trailing edge of BUSY H is simultaneous with the trailing edge of END CYCLE H. This should not prove to be a problem, as all known applications use either BUSY H, or END CYCLE H, but not both.

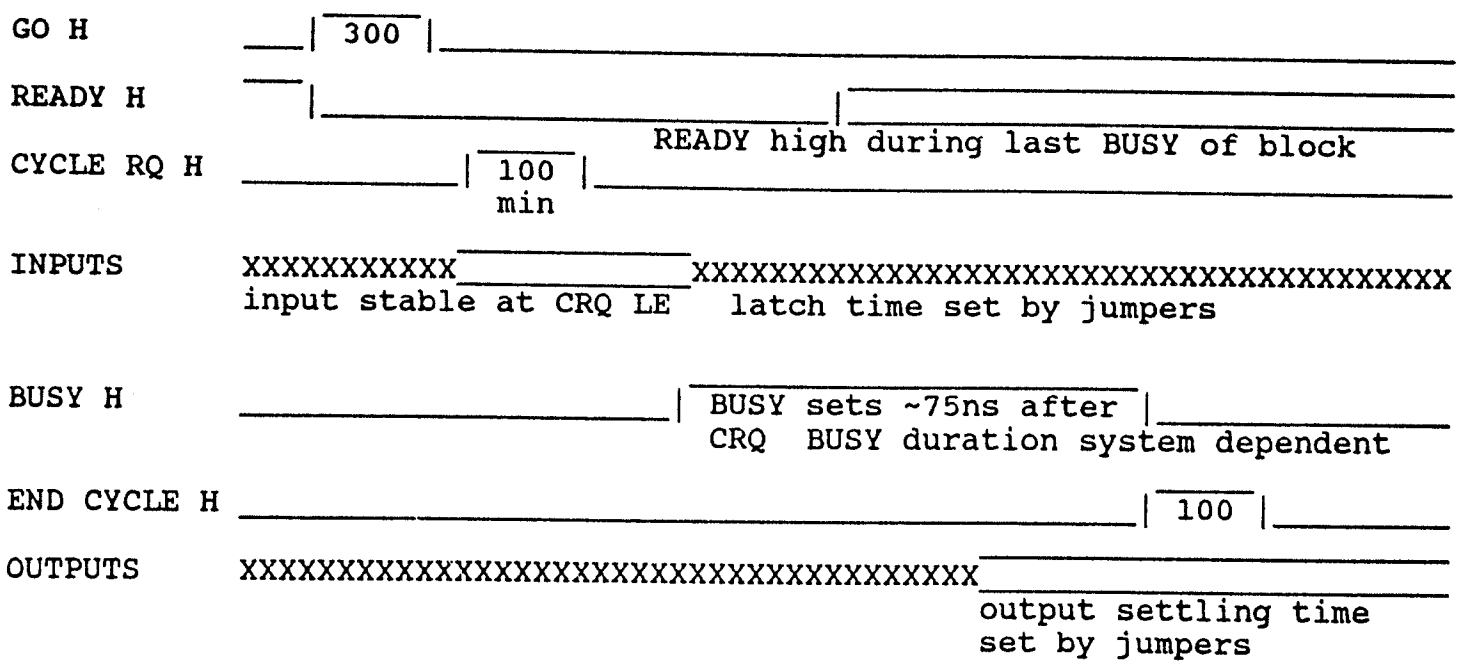
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APPENDIX A

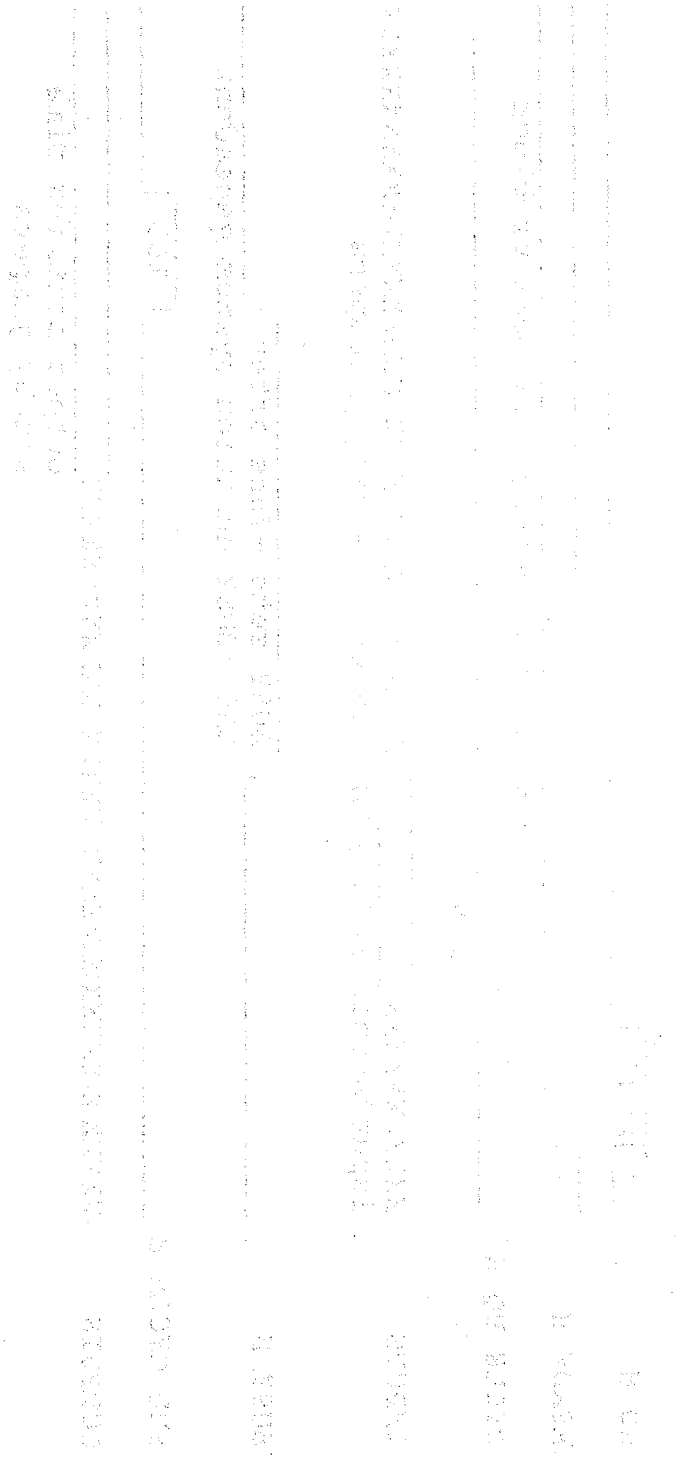
I/O Timing

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