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REFERENCE MANUAL

Talon Instruments™

SR105

16-Channel TTL Stimulus/Response Module



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Instrument Part Number: SR105

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This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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DOCUMENT CHANGE HISTORY

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1 Introduction

Talon's SR192 digital test module is a modular VXI stimulus/response system. The SR192 motherboard is a two slot, "C" size module which houses up to 12 I/O modules. I/O modules are designed to provide either 8 or 16 stimulus/response channels for a total of 96 or 192 channels. Modules provide many logic options such as fixed voltage TTL, ECL, RS485/422 or variable voltages of +/- 15V or +5/-2. The I/O channels may also be single-ended or double-ended (differential) logic.

Multiple SR192's may be linked in a master/slave configuration to provide up to 1152 channels in a single VXI 13-slot chassis.

This manual is for the SR105 I/O module. The SR105 is a 16 channel, dynamic, single-ended TTL I/O module. The 16 I/O channels are bi-directional using a tristate memory to control direction on a per pin basis. Each SR105 operates as two 8 channel groups allowing up to twenty-four 8 channel groups in a single SR192. Driver enable signals are assigned in groups of 8. Input strobe signals are assigned in groups of 16. This manual will describe the operation of a single 8 channel group of the SR105.

The SR105 utilizes a five memory architecture, OUTPUT, TRISTATE, EXPECT, MASK and RECORD. This architecture allows the user to perform real-time error detection and recording. Each memory is 128K bits per channel.

The layout of this manual is in five sections described below:

1. Introduction	This section
2. Specifications	SR105 electrical and environmental specifications
3. Jumpers/Installation	Description of the jumpers and installation of the SR105
4. Functional Description	SR105 functional description
5. Memory Data Mapping	Memory to channel mapping

In addition, five appendices are included:

A. Glossary of Terms	Definition of terms used in this manual
B. Function Code Map	Hardware register descriptions
C. Programming Examples	SR105 stimulus/response programming examples
D. SR192 Clock Timing	SR192 clock timing specifications.
E. SR105 Block Diagram	SR192/SR105 system block diagram.

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2 Specifications

The following sections list the specifications of the SR105 I/O module.

2.1 I/O Module

Number of channels	16
Number of Stimulus Memories	2
OUTPUT, TRISTATE	
Number of Response Memories	3
Memory depth per channel	131072
Maximum stimulus data rate parallel (16 channels)	25 MHz
Stimulus group enable signal (common to 8 channels)	4
Internal (TSENABLE1, TSENABLE2)	2
External (FCNTL1, FCNTL2)	2
Stimulus group enable resolution	one TS_CLK
Maximum response data rate (16 channels)	25 MHz
Response input strobe signal (common to 8 channels)	4
Internal (TSSTROBE1, TSSTROBE2)	2
External (FCNTL1,FCNTL2, CSTROBE)	2
Response input strobe resolution	one TS_CLK
Output Driver/Input Receiver	74AS240

2.2 Electrical

High Level Output Voltage	2.4V min
High Level Source Current	50 mA
Low Level Output Voltage	0.4V max
Low Level Sink Current	50 mA
Output Impedance (with 47Ω series terminator)	55Ω typ
Short Circuit Protected	Yes [2]
High Input Threshold	2.0V
Low Input Threshold	0.8V
Input Impedance	>10KΩ

Note 2: With the 47Ω series terminator installed

2.3 Timing Characteristics

In order to specify the timing characteristics of the SR105, the TS_CLK signal generated by the timing module will be used as the reference signal. Appendix D of this manual gives the timing relationship between the external input clocks (EXCLK1 and EXCLK2), TS_CLK and external output clocks (CLOCKA and CLOCKB).

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Table 2-1 lists the typical timing characteristics of the SR105's stimulus/response logic.

Parameter and Description	From	To	Typ (ns)	Note
Stimulus Specifications				
Data Propagation	TS_CLK	CH OUTPUT	10-12	-
Tristate Propagation enabled	TS_CLK	CH OUTPUT	17-19	-
Tristate Propagation disabled	TS_CLK	CH OUTPUT	17-19	-
Internal clock to group enable true	TS_CLK	GROUP ENABLE	15-19	1
Internal clock to group enable false	TS_CLK	GROUP ENABLE	13-17	1
Field control one to group enable true.	FCNTL1-TTL	GROUP ENABLE	17-26	1
	FCNTL1-PROG		24-32	1
	FCNTL1-DIFF		49-62	1
Field control one to group enable false.	FCNTL1-TTL	GROUP ENABLE	14-21	1
	FCNTL1-PROG		23-30	1
	FCNTL1-DIFF		49-56	1
Field control two to group enable true.	FCNTL2	GROUP ENABLE	20-28	1
Field control two to group enable false.	FCNTL2	GROUP ENABLE	16-22	1
Card strobe to group enable true.	CSTROBE	GROUP ENABLE	13-16	1
Card strobe to group enable false.	CSTROBE	GROUP ENABLE	8-11	1
Group enable to valid data.	GROUP ENABLE	CH OUTPUT valid	12-14	-
Group enable to invalid data.	GROUP ENABLE	CH OUTPUT invalid	12-14	-
Response Specifications				
Receiver propagation	CH INPUT	RESP VALID	5-7	-
Internal clock to response strobes.	TS_CLK	INPUT/STROBE	12-16	1
Field control one to response strobes.	FCNTL1-TTL	INPUT/STROBE	14-23	1
	FCNTL1-PROG		21-29	1
	FCNTL1-DIFF		46-57	1
Field control two to response strobe.	FCNTL2	INPUT STROBE	17-25	1
Card strobe to response strobe.	CSTROBE	INPUT STROBE	7-10	1
Data valid setup to input strobe.	RESP VALID	INPUT/STROBE	5	-

Note 1: The range of delay accounts for the number of modules installed and their position in the SR192 system.

Table 2-1 Stimulus/Response Timing Characteristics

2.4 Environmental

Temperature Range

Operating .....0° C to +50° C
Storage .....-40° C to +71° C (RH not controlled)

Altitude

Operating .....Sea level to 10,000 ft.
Storage .....Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C .....not controlled
+11°C to +30°C .....95+/-5%RH
+31°C to +40°C .....75+/-5%RH
+41°C to +50°C .....45+/-5%RH

2.5 Size

Dimension

4.93 cm x 22.61 cm (1.94" x 8.9")

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Weight

.074 kg (2.6 oz)

2.6 Power Requirements

The power requirements listed in table 2-2 are for a single SR105 with the drivers unloaded.

Voltage	Peak Current	Dynamic Current	Note
+5V	1A	.3A	1
-5.2V	0	0	-
-2V	0	0	-
+12V	0	0	-
-12V	0	0	-
+24V	0	0	-
-12V	0	0	-
V+	0	0	1
V-	0	0	-

Note 1: The +5V can be supplied either from the Backplane or from V+ on front panel J10 connector, see Section 3.2.

Table 2-2 SR105 Voltage Requirements

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3 Jumpers/Installation

The SR105 I/O module requires firmware revision 1.28 or later for proper operation. Contact Talon Instruments for information on firmware upgrades.

Figure 3-1 below is a locator diagram for test points and jumpers located on the SR105.

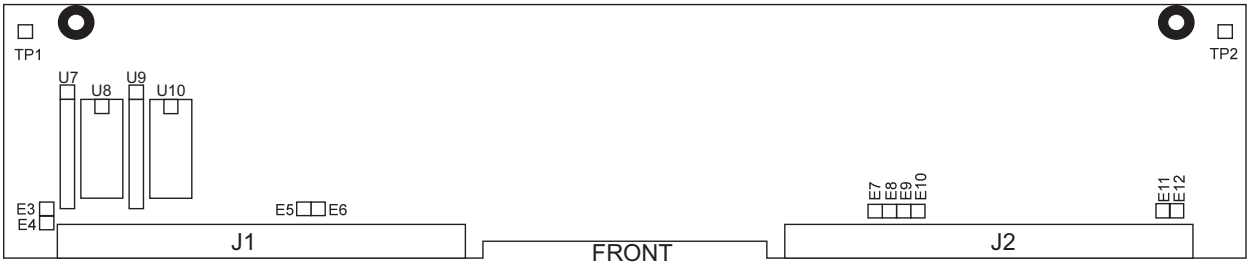


Figure 3-1 Test Point/Jumper Locations

3.1 Test Point Description

Table 3-1 describes the test points on the SR105 I/O module.

Test Point	Mnemonic	Description
TP1	GND1	Signal ground
TP2	GND2	Signal Ground

Table 3-1 SR105 Test Point Description

3.2 Jumper Description

The following sections describe the SR105 jumper options.

3.2.1 Factory Jumpers (E5, E6, E7, E8, E9, E10)

These jumpers are reserved and are used to enable the reprogrammable logic on the SR105. For normal operation connect E5-E6 and E7-E10.

3.2.2 Backplane +5V Select (E3, E4, E5, E6, E11, E12)

This jumper block connects the VXI Backplane +5V to the SR105's +5V Vcc plane. E3-E4, E5-E6 and E11-E12 installed connects +5V to the VXI Backplane (factory default).

3.2.3 Front Panel +5V Select (E7, E8, E9, E10)

This jumper block connects the V+ front panel J10 signal to the SR105's +5V Vcc plane. E7-E8 and E9-E10 installed connects +5V to the front panel.

This setting would be used if the VXI chassis +5V power supply cannot provide sufficient power to the SR105's.

CAUTION

Make sure the J10 power is applied prior to VXI chassis power.

WARNING

Make sure the Backplane +5V jumpers E3-E4, E5-E6 and E11- E12 are disconnected. A trace may be present (factory default) which connects E3-E4, E5-E6 and E11-E12.

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3.3 Installation

Each SR192 motherboard can house up to 12 I/O modules. I/O modules are installed in motherboard slots DRA1 through DRA6 and DRB1 through DRB6, see Figure 3-2.

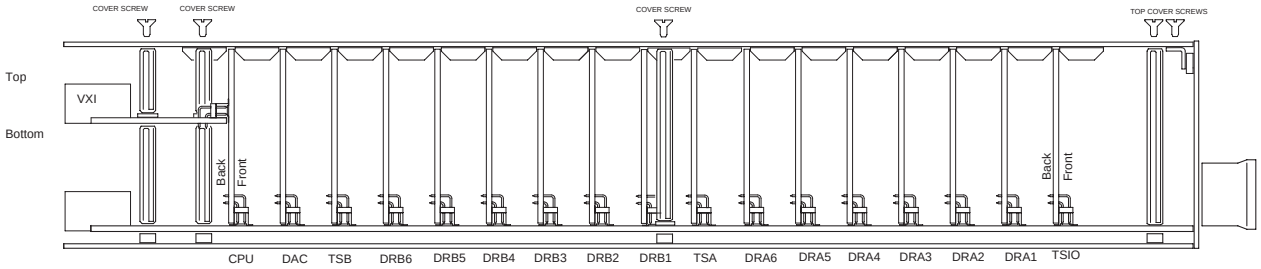


Figure 3-2 SR192 Motherboard Side View

Perform the following steps to add or replace an I/O module:

Step 1. Using ESD protocols remove the SR192 from the VXI chassis.

Step 2. Remove the top cover screws, refer to Figure 3-2.

Step 3. If replacing an I/O module, remove it by grasping at each corner and gently rocking forward and back while pulling it away from the motherboard.

Step 4. Insert the I/O module in the desired DRA or DRB module slot, Figure 3-2, by lining up the J1 and J2 connectors with the motherboard connectors and gently pushing down. All SR192 modules are keyed along the associated mating connector. If the module cannot be inserted, make sure you are inserting the module into the correct slot, check for bent pins and make certain the pins are aligned with the mating connector on the motherboard.

CAUTION

Although the modules and the associated mating connectors have been keyed, it is possible to force a module into an incorrect slot.

3.4 Termination Options

The following sections describe the output/input termination options of the SR105.

3.4.1 Output Termination

The SR105 is shipped from the factory with 47Ω series termination resistors on each channel. These 16 resisters are installed in U8 and U10, see figure 3-1.

U8 and U10 are sixteen pin dip resister packages, Bourns part number 4116R-001-470. The resistor packs can be removed or changed by the user.

U8 is connected to the lower 8 channels and U10 is connected to the upper 8 channels.

3.4.2 Input Termination

The SR105 has two ten pin sip pads (U7 and U9) where parallel termination resisters can be installed.

Pin one of both pads are connected to signal ground and pin ten is connected to Vcc (+5V).

U7 is connected to the lower 8 channels and U9 is connected to the upper 8 channels.

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4 Functional Description

The SR105, along with all the other I/O modules, is controlled through the SR192 timing modules. Control signals are generated by the timing module which allow the SR105 to output stimulus data and record response data while the timing module is running. When the timing module is not running, idle, the CPU module or VXI controller can program or query the stimulus/response memories on the SR105.

Figure 4-1 depicts an SR105 module in relation to other components of the SR192.

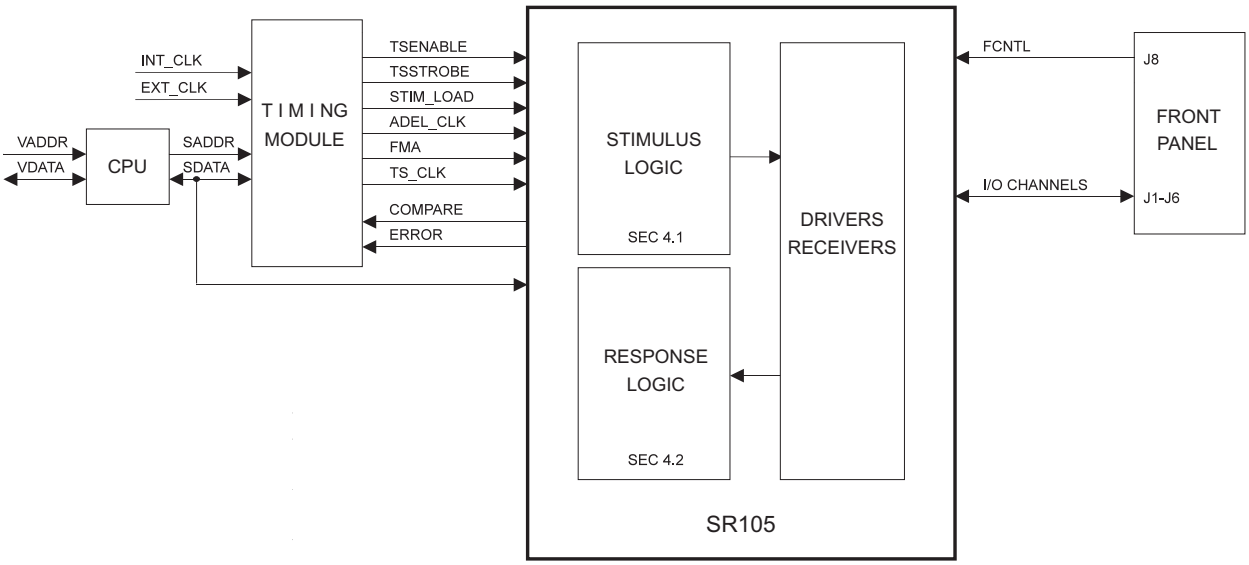


Figure 4-1 SR105 Block Diagram

The following list describes the functional blocks shown in figure 4-1 above.

1.	CPU	The SR192 CPU module selects whether the local processor or VXI Backplane has control of the system bus, SADDR and SDATA.
2.	TIMING MODULE	One of two SR192 timing modules, SR100 or SR101.
3.	STIMULUS LOGIC	The memories, registers and control bits that generate UUT input data.
4.	RESPONSE LOGIC	The memories, registers and control bits that record UUT output data.
5.	DRIVERS/RECEIVERS	The driver/receiver ICs and terminators that connect the STIMULUS/RESPONSE logic to the UUT.
6.	FRONT PANEL	The mating connectors through which a physical connection is made to the UUT.

The following list describes the signals shown in figure 4-1 above.

1.	INT_CLK	Selected internal timing module clock from the motherboard (10MHz, 20MHz, 50MHz or programmable from SR210).
2.	EXT_CLK	Selected external clock from the front panel J8 connector (EXCLK1 or EXCLK2)
3.	VADDR	The address bus from the VXI Backplane.
4.	VDATA	The data bus from the VXI Backplane.
5.	SADDR	Either the local microprocessor or VADDR bus.
6.	SDATA	Either the local microprocessor or VDATA bus.
7.	TSENABLE	Two timing module signals which can be selected as the group enable for the stimulus data.
8.	TSSTROBE	Two timing module signals which can be selected to strobe response data.
9.	STIM_LOAD	Timing module signalthat 1) - enables data from the output and tristate memories into the stimulus register and 2) - clocks an input address delay register.
10.	ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
11.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word.
12.	TS_CLK	The timing module clock (EXT_CLK or INT_CLK).

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13.	COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
14.	ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
15.	FCNTL	Two front panel input signals that can be selected to either enable stimulus or strobe response data.
16.	I/O CHANNELS	16 bi-directional data channels.

The following sections describe the three major logic elements of the SR105 (Stimulus, Response and Driver/Receiver).

4.1 Stimulus Logic

Figure 4-2 shows the stimulus logic block diagram (lower group shown).

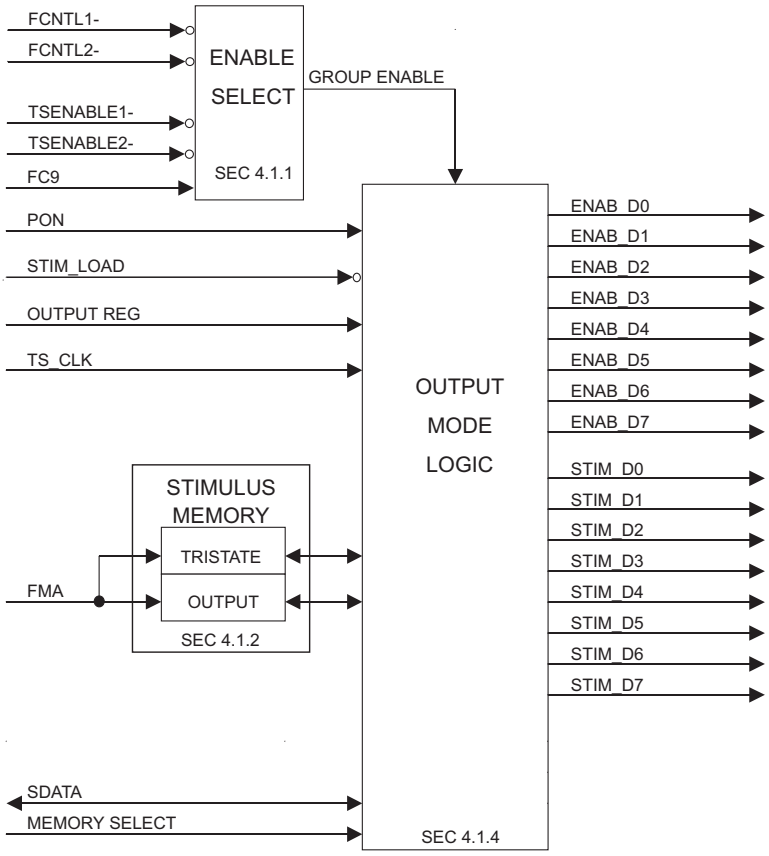


Figure 4-2 Stimulus Logic Block Diagram

The following list describes the functional blocks of figure 4-2.

1.	ENABLE SELECT	Used to select the group enable signal. The group enable signal allows the operator to enable all eight drivers for a portion of the timing cycle.
2.	STIMULUS MEMORY	Two 128K by 16 memories allows the operator to define the logic level and enable any of the 16 drivers during an output word.
3.	OUTPUT MODE LOGIC	Hardware that performs the selected channel output function..

The following list describes the signals shown in figure 4-2 above.

1.	FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
2.	FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
3.	TSENABLE1	Timing Set Enable 1 from the timing module.
4.	TSENABLE2	Timing Set Enable 2 from the timing module.
5.	PON	Power on signal routed to all the I/O modules. Set by the “OUTPUT:CHANNEL:STATE (ON | OFF) command.

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6.	STIM_LOAD	Timing module signal that: 1. Enables data from the output and tristate memories to the stimulus registers in output register mode. 2. Clocks an input address delay register in output register mode (not shown).
7.	OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
8.	TS_CLK	The selected timing module clock.
9.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word.
10.	SDATA	The selected data bus used to program and query the stimulus memories.
11.	MEMORY SELECT	This signal allows the user to program or query the tristate or output memory.
12.	GROUP ENABLE	Group enable signal. This signal can be used to enable a group of I/O channels.
13.	ENAB_D0-ENAB_D7	Registered enable signals to the output drivers.
14.	STIM_D0-D7	Data to the output driver.

4.1.1 Enable Select

The enable logic allows the user to select the GROUP ENABLE signal.

The GROUP ENABLE signal must be true (low) to enable output drivers. This functionality is required for simulating channels which are enabled and disabled as a synchronous group. Selected in groups of 8 channels.

4.1.2 Stimulus Memories

The Stimulus memories on the SR105 consist of two 128K x 16 bit static RAM's. The first memory contains the TRISTATE data and the second contains the OUTPUT data. Bit 0 - 15 of word "n" of the tristate memory corresponds to and enables bits 0 - 15 of word "n" of the output data.

Both of the output memories are addressed by the FMA bus generated by the timing module. Each FMA value causes a new output and tristate word.

4.1.3 Output Mode Logic

The SR105 output mode logic unit, in figure 4-2, between the stimulus memories and the output drivers is illustrated in figure 4-3 below.

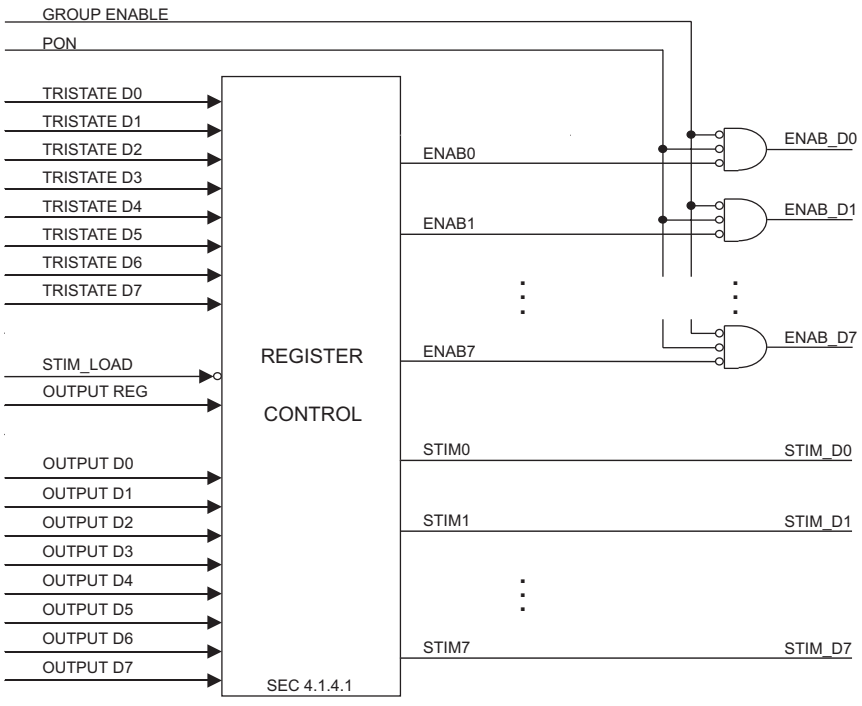


Figure 4-3 Output Mode Logic Block Diagram (One of two 8 channel groups)

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The following list describes the functional blocks of figure 4-3.

1. REGISTER CONTROL — Used to select the data source for the stimulus registers.
2. OUTPUT REGISTERS — These registers contain the enable and data values for the output drivers.

The following list describes the signals shown in figure 4-3 above.

1. GROUP ENABLE — Group enable signal. This signal can be used to enable a group of 8 I/O channels.
2. PON — Power on signal routed to all the I/O modules. Set by the "OUTPUT:CHANNEL:STATE (ON | OFF) command.
3. TRISTATE D0-D7 — Tristate driver data from the stimulus memory.
4. STIM_LOAD — Timing module signal that:
   1. Enables the data from the output and tristate memories to the output registers in output register mode.
   2. Clocks an input address delay register in output register mode.
5. OUTPUT REG — Signal used to indicate if the output register mode is enabled or disabled.
6. OUTPUT D0-D7 — Data from the output memory.
7. TS_CLK — The timing module clock.
8. ENAB0-ENAB7 — Selected enable signal from the register control block.
9. ENAB_D0-ENAB_D7 — Registered enable signals to the output drivers.
10. STIM0-STIM7 — Selected data signal from the register control block.
11. STIM_D0-STIM_D7 — Registered data signal.

4.1.3.1 Driver Enable Logic

Table 4-1 below illustrates the affects of the PON and GROUP ENABLE signals along with the tristate and output memory data on the driver output.

PON	GROUP ENABLE	TRISTATE MEMORY	OUTPUT MEMORY	DRIVER OUTPUT
HIGH	X	X	X	High Z
LOW	HIGH	X	X	High Z
LOW	LOW	1	X	High Z
LOW	LOW	0	0	Logic Zero
LOW	LOW	0	1	Logic One

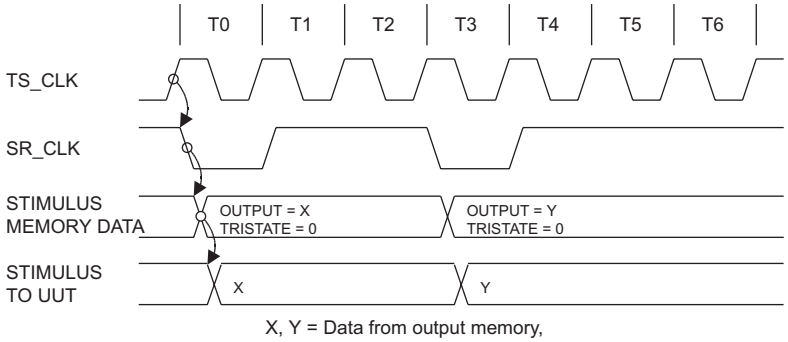
Table 4-1 Stimulus Memory Description

As shown in table 4-1 above, three conditions must be true in order to enable the output driver:

1. The power-up register (PON) must be set true (LOW).
2. The selected group enable signal must be true (LOW).
3. The respective bit from the tristate memory must be true (LOW).

4.1.4 Unregistered Output Mode Timing (Default)

The timing is defined by the SR_CLK control signal programmed in the timing set. Figure 4-4 shows unregistered output signal timing.



X, Y = Data from output memory,

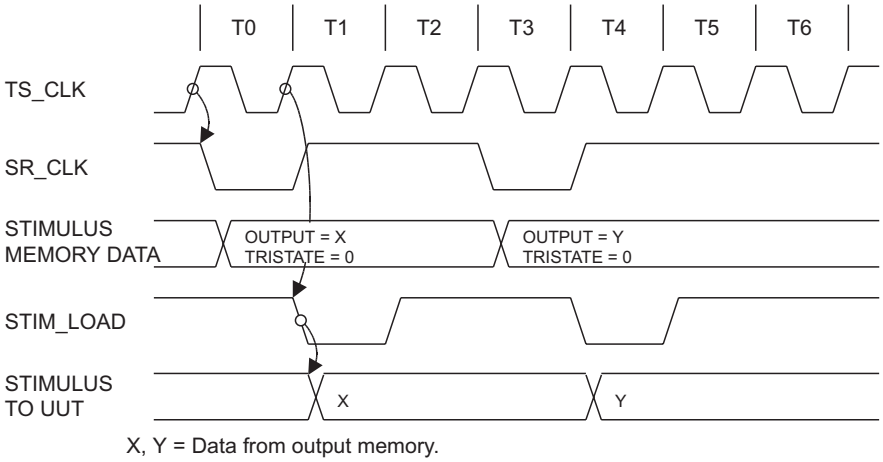
Figure 4-4 Unregistered Output Signal Timing

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The stimulus data to the UUT is generated from the OUTPUT and TRISTATE memory. The SR_CLK signal increments the stimulus address (FMA) to the OUTPUT and TRISTATE memories.

4.1.5 Registered Output Mode Timing

The timing is defined by the SR_CLK and STIM_LOAD control signals programmed in the timing set. Figure 4-5 shows unregistered output signal timing.



X, Y = Data from output memory.

Figure 4-5 Registered Output Signal Timing

The data to the UUT is registered by the falling edge of the STIM_LOAD control signal.

Output timing restrictions:

1. If STIM_LOAD is in the same cell as SR_CLK then the registered data will be from the previous FMA address, i.e., pipelined.

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4.2 Response Logic

Figure 4-6 shows the response logic block diagram.

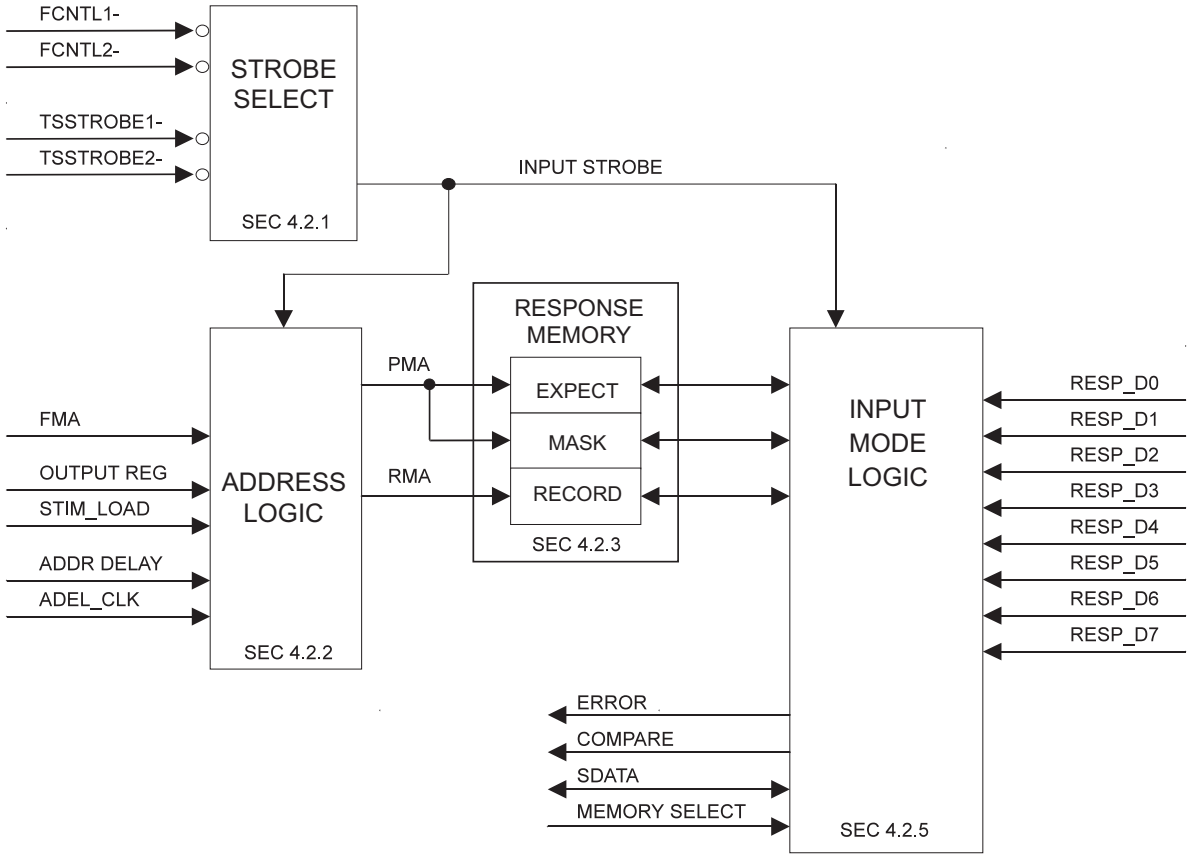


Figure 4-6 Response Logic Block Diagram

The following list describes the functional blocks of figure 4-6.

1.	STROBE SELECT	Used to select the input strobe.
2.	ADDRESS LOGIC	A series of registers used to delay the FMA in order to generate a synchronous address to the response memories.
3.	EXPECT MEMORY	128K by 16 memory allows the user specify an expected result for each response bit for real time compare.
4.	MASK MEMORY	128K by 16 memory allows the user to mask on or off any response bit for real time compare.
5.	RECORD MEMORY	128K by 16 memory stores the result of the real time compare for every INPUT STROBE signal.
6.	INPUT MODE LOGIC	Hardware that performs the selected function mode and real time compare.

The following list describes the signals shown in figure 4-6 above.

1.	FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
2.	FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
3.	TSSTROBE1	Timing Set Strobe 1 from the timing module.
4.	TSSTROBE2	Timing Set Strobe 2 from the timing module.
5.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
6.	OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
7.	STIM_LOAD	Timing module signal that latches the response address bus (FMA) when the output register mode is enabled.
8.	ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
9.	ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
10.	PMA	Present Memory Address. Delayed FMA bus. Refer to section 4.2.2

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11.	RMA	Record Memory Address. Delayed PMA bus. Refer to section 4.2.2
12.	INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
13.	COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
14.	ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
15.	SDATA	The selected data bus used to program and query the response memories.
16.	MEMORY SELECT	This signal allows the user to program or query the expect, mask or record memory. Two virtual memories can also be selected (error and response) that are derived from the data stored in the other three memories.
17.	RESP_D0-D7	Response signals from the input receivers.

4.2.1 Strobe Select

The strobe select allows the user to select the INPUT STROBE.

The falling edge of INPUT STROBE causes the data from the input receivers to be compared to the data programmed in the EXPECT and MASK memories. The result of the comparison for each channel is then stored in the RECORD memory. Refer to section 4.2.3 for a description of the response memories.

4.2.2 Address Logic

Figure 4-7 illustrates the SR105 address logic.

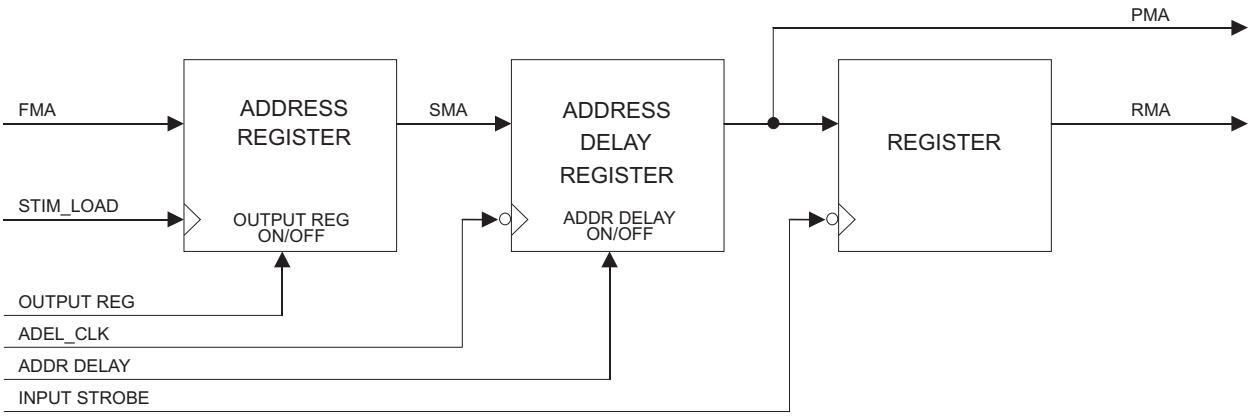


Figure 4-7 Input Address Logic Block Diagram

The following list describes the signals shown in figure 4-7 above.

1.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
2.	STIM_LOAD	Timing module signal that latches the response address bus (FMA) when the output delay mode is enabled.
3.	OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
4.	ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
5.	ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
6.	INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
7.	SMA	Stimulus Memory Address. Delayed FMA bus.
8.	PMA	Present Memory Address. Delayed SMA bus.
9.	RMA	Record Memory Address. Registered PMA bus.

The address logic is used to delay the FMA bus to the PMA and RMA bus.

As shown in figure 4-7 above there are two register delay blocks. The combination of these two registers defines four input modes described in section 4.2.5.

These input modes can be used in stimulus/response applications to keep the stimulus data synchronized with the response data.

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4.2.3 Response Memories

The response memories on the SR105 consist of three 128K x 16 bit static RAM's. The first two, EXPECT and MASK contain the data that is used by the input comparator. The third memory, RECORD, is used to store the results of the input comparator. Bit 0 of the EXPECT is compared with bit 0 of registered response data from the input receiver and the result is stored in bit 0 of the RECORD memory as the "unmasked" error.

The MASK and EXPECT memories are addressed by the PMA bus. The RECORD memory is addressed by the registered PMA bus called the RMA bus.

From the contents of the EXPECT, MASK and RECORD memory, two additional "virtual" memories are created, ERROR and RESPONSE.

Table 4-2 below illustrates the real time compare results of the MASK and EXPECT memories for each state of the response data (logic 0 and logic 1).

COMPARE FUNCTION	MASK MEMORY	EXPECT MEMORY	RESPONSE DATA	RECORD MEMORY	ERROR MEMORY	RESPONSE MEMORY
Test for logic 0	0	0	Logic 0	0	0	0
			Logic 1	1	1	1
Test for logic 1	0	1	Logic 0	1	1	0
			Logic 1	0	0	1
Mask off ERROR	1	0	Logic 0	0	0	0
			Logic 1	1	0	1
Not Used	1	1	Logic 0	1	1	0
			Logic 1	1	1	0

Table 4-2 Expect, Mask, Record, Error and Response Memory Description

The RESPONSE memory is the logical "exclusive or" of the RECORD and EXPECT memories.

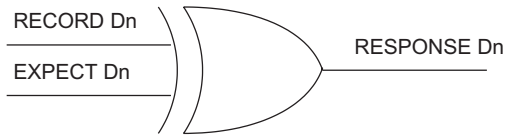


Figure 4-8 Response Memory Logic

The ERROR memory is generated by the logical "and" of the RECORD memory with the logical "or" of the EXPECT and the complimented MASK memory.

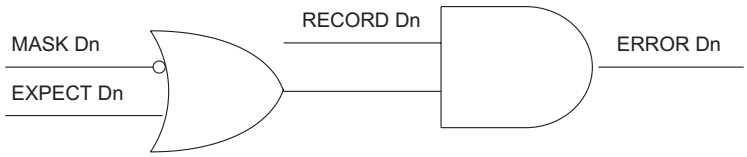


Figure 4-9 Error Memory Logic

4.2.4 Input Mode Logic

The mode of operation for the response logic is the same as the stimulus logic. The channels record data in parallel.

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Figure 4-10 below is the block diagram for the input mode logic.

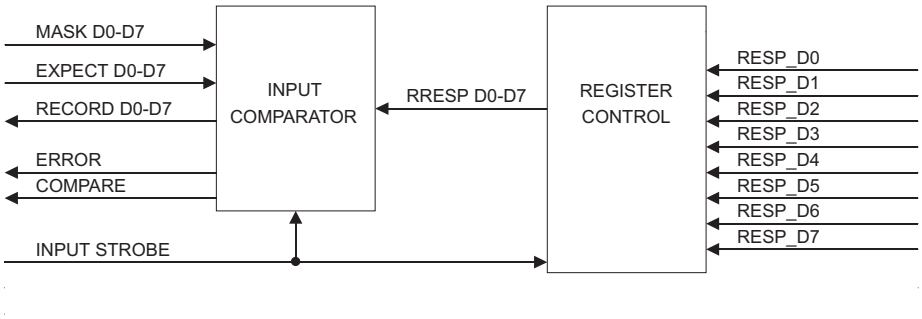


Figure 4-10 Input Mode Logic

The following list describes the functional blocks of figure 4-10.

1. INPUT COMPARATOR — On the falling edge of the INPUT STROBE signal this logic will compare the registered response data with the mask and expect memory data.
2. REGISTER CONTROL — This logic routes the response data from the receivers to the appropriate register based on the selected function mode and registers the data.

The following list describes the signals shown in figure 4-10 above.

1. MASK D0-D7 — Data from the mask memory.
2. EXPECT D0-D7 — Data from the expect memory.
3. RECORD D0-D7 — Data to the record memory.
4. ERROR — Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
5. COMPARE — Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
6. INPUT STROBE — This signal registers the input data, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
7. RRESP D0-D7 — Registered response data.
8. RESP_D0-D7 — Response signals from the input receivers.

4.2.4.1 Input Comparator

The input comparator generates the data for the record memory as well as the ERROR and COMPARE signals.

Table 4-3 below illustrates the input comparator results for the ERROR and COMPARE signal.

COMPARE FUNCTION	MASK DATA	EXPECT DATA	REGISTERED RESPONSE	ERROR	COMPARE
Test for logic 0	0	0	Logic 0	0	1
			Logic 1	1	0
Test for logic 1	0	1	Logic 0	1	0
			Logic 1	0	1
Mask off ERROR	1	0	Logic 0	0	1
			Logic 1	0	1
Not Used	1	1	Logic 0	1	0
			Logic 1	1	0

Table 4-3 Input Comparator Results

The input comparator generates the data that will be recorded in the record memory. It also generates the real time ERROR and COMPARE signals that can be tested by the timing modules.

The error signal for each channel is registered with the falling edge of the INPUT STROBE signal. The ERROR signal for the module is the “OR” of the error signals of the individual channels. Note from table 4-3 that a channel error signal is not generated if the compare is masked off.

The compare signal for each channel is not registered. The COMPARE signal for the module is the “AND” of the compare signals from the individual channels.

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CAUTION

Since COMPARE is not registered, logic switching noise may produce an inadvertent compare of sufficient duration to be recognized by the timing module as a valid compare. Also in TSA/TSB linked mode, the response data must be synchronized with CLOCKA in order to prevent TSA/TSB from becoming unsynchronized.

4.2.4.2 Input Register Control

The input register control logic is used to register the response data from the input receivers.

The falling edge of INPUT STROBE is used to control the data.

In order to record the UUT response data in the same memory address that generated the UUT stimulus data, the user must do two things:

1. Determine where the input strobe signal needs to be positioned to accommodate the UUT delay.
2. Select an input addressing mode that will retrieve the Expect/Mask data with respect to his input strobe.

The input strobe must be placed far enough over from the cell which generated the stimulus data to allow for the UUT delay (D), as well as the SR105's internal input and output delay. The number of cells (N) required to accommodate these delays for the SR105 are shown in the following formula:

$$N = (D+12)F/1000$$

Where D = users UUT delay in ns

F = SR192 TS_CLK rate in MHz

If the response data can be recorded within the same cycle and, therefore before the next stimulus word, then input mode 1 or 3 should be selected.

If the response data has to be recorded during the next stimulus word, then the expect and mask data must be delayed using addressing mode 2 or 4.

If the response data has to be recorded after the next stimulus word then the expect and mask data must be pipelined, i.e., the response data generated by stimulus word at address "n" will be recorded in address "n + 1" or later.

4.2.5 Input Mode Timing

The following sections describe the timing of the four input modes described in section 4.2.2.

4.2.5.1 Input Mode 1 Timing

This mode is set by enabling the output registers and disabling the address delay reigister.

In this mode the field memory address bus (FMA) is registered by the falling and stimulus data edge of the STIM_LOAD signal before addressing the response memories (MASK, EXPECT and RECORD).

This mode can be used in most stimulus/response applications where the response to a stimulus word can be strobed prior to the output of the next stimulus word.

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The following timing restrictions apply to addressing mode 1:

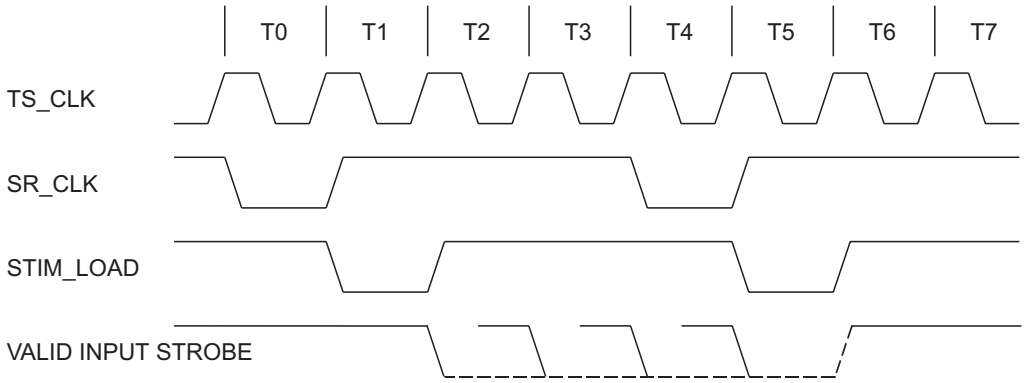


Figure 4-12 Input Mode 1 Timing Restrictions

Timing Set restrictions:

1. Do not have the falling edge of STIM_LOAD at the same time as the falling edge of SR_CLK.

Figure 4-11 below illustrates mode 1 input timing.

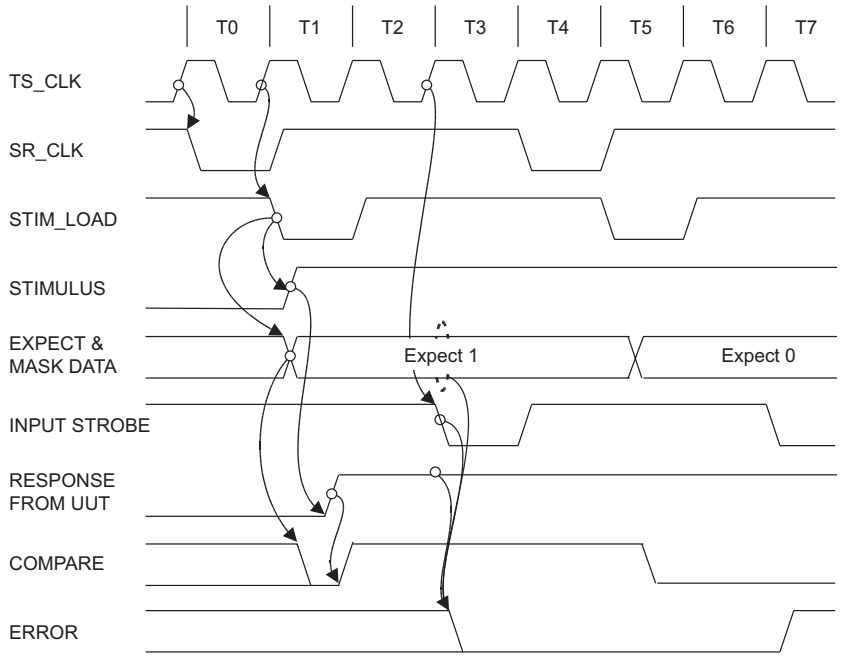


Figure 4-11 Input Mode 1 Timing

The example above illustrates recording data that generates a compare/no error followed by a non-compare/error.

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The following table 4-4 describes the timing sequence in figure 4-11.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory.
T1	STIM_LOAD	Falling Edge	Loads stimulus data into the output registers (a logic one in the example). Retrieves expect and mask data from memory (expect 1 in example).
T3	INPUT STROBE	Falling Edge	Compare the UUT response data with the expect and mask data then store results into the record memory.
T4	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
T5	STIM_LOAD	Falling Edge	Loads stimulus data into the output registers (a logic one in the example). Retrieves new expect and mask data from memory (expect 0 in example).
T7	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.

Table 4-4 Input Mode 1 Timing Description

4.2.5.2 Input Mode 2 Timing

This mode is set by enabling the output registers and the address delay reigister.

In this mode the field memory address bus (FMA) is registered first by the falling edge of STIM_LOAD and then by the falling edge of ADEL_CLK before addressing the response memories (MASK, EXPECT and RECORD).

This is used in applications where the response to a stimulus word cannot be strobed prior to the end of the stimulus word cycle.

The following timing restrictions apply to input mode 2:

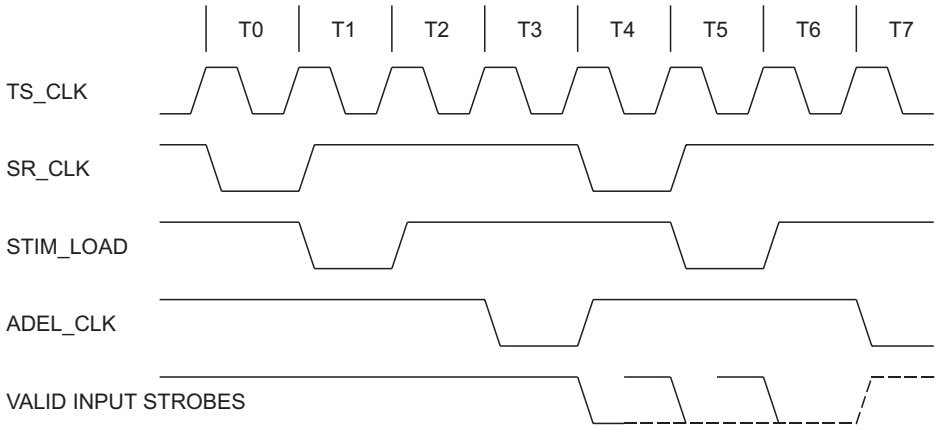


Figure 4-13 Input Mode 2 Timing Restrictions

Timing Set restrictions:

1. Do not have the falling edge of STIM_LOAD at the same time as the falling edge of SR_CLK.
2. Do not have the falling edge of INPUT STROBE at the same time as the falling edge of ADEL_CLK.

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Figure 4-14 below illustrates the input mode 2 timing.

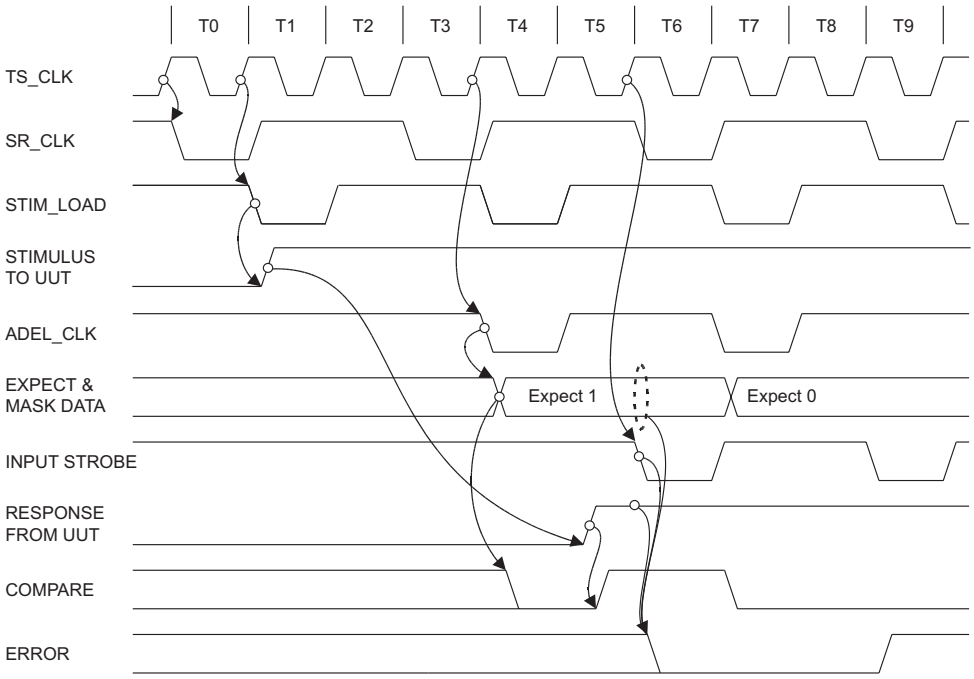


Figure 4-14 Input Mode 2 Timing

The example above illustrates recording data that generates a compare/no error followed by a non-compare/error.

The following table describes the timing sequence in figure 4-14

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory.
T1	STIM_LOAD	Falling Edge	Loads stimulus data into the output registers (a logic one in the example). Stimulus Memory Address (SMA) registered, see figure 4-7.
T3	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
T4	STIM_LOAD	Falling Edge	Loads stimulus data into the output registers (a logic one in the example). Stimulus Memory Address (SMA) registered, see figure 4-7.
	ADEL_CLK	Falling Edge	Retrieves expect and mask data from memory (expect 1 in example).
T6	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.
T7	STIM_LOAD	Falling Edge	Loads stimulus data into the output registers (a logic one in the example). Stimulus Memory Address (SMA) registered, see figure 4-7.
	ADEL_CLK	Falling Edge	Retrieves new expect and mask data from memory (expect 0 in example).
T9	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.

Table 4-5 Input Mode 2 Timing Description

4.2.5.3 Input Mode 3 Timing

This mode is set by disabling the output registers and the address delay reigister.

In this mode the field memory address bus (FMA) is passed through directly to the response memories (MASK, EXPECT and RECORD).

This is used in applications where the response to a stimulus word can be strobed prior to the end of the stimulus word cycle.

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The following timing restrictions apply to input mode 3:

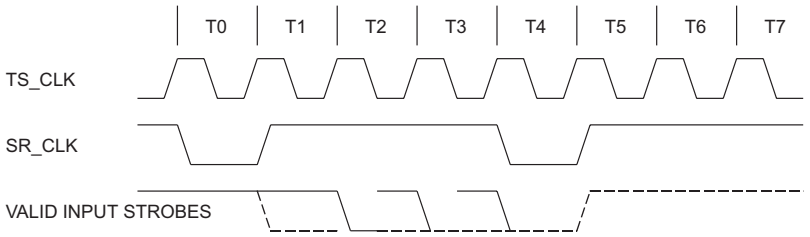


Figure 4-16 Input Mode 3 Timing Restrictions

Timing Set restrictions:

1. The INPUT STROBE must occur at least one cell later than SR_CLK (in stimulus response applications).

Figure 4-15 below illustrates the input mode 3 timing.

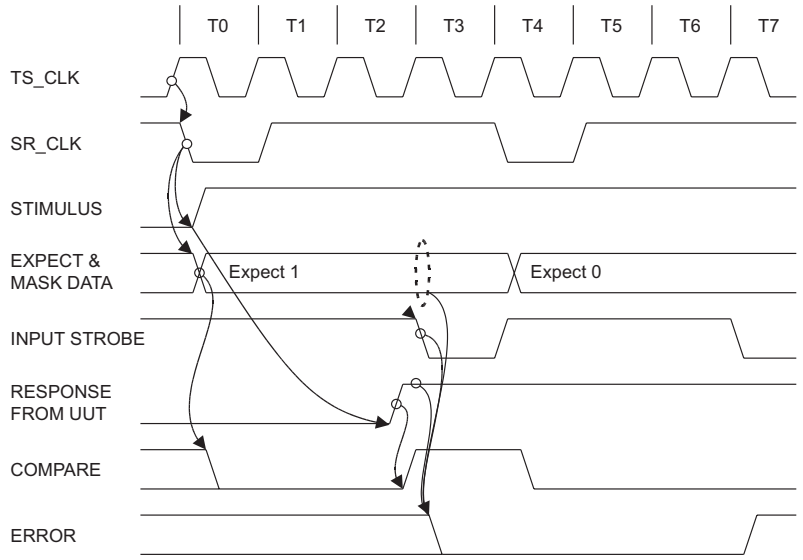


Figure 4-15 Input Mode 3 Timing

The example above illustrates recording data that generates a compare/no error followed by a non-compare/error.

The following table describes the timing sequence in figure 4-15.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus (a logic one in the example), expect and mask data from memory (expect 1 in example).
T3	INPUT STROBE	Falling Edge	Compare the response input with the expect and mask data then store results into the record memory.
T4	SR_CLK	Falling Edge	Retrieves stimulus (a logic one in the example), expect and mask data from memory (expect 0 in example).
T7	INPUT STROBE	Falling Edge	Compare the response input with the expect and mask data then store results into the record memory.

Table 4-6 Input Mode 3 Timing Description

4.2.5.4 Input Mode 4 Timing

This mode is set by disabling the output registers and enabling the address delay reigister.

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In this mode the bus that addresses the stimulus memory (FMA) is registered by the falling edge of the ADEL_CLK signal before addressing the response memories (MASK, EXPECT and RECORD).

The following timing restrictions apply to input mode 4:

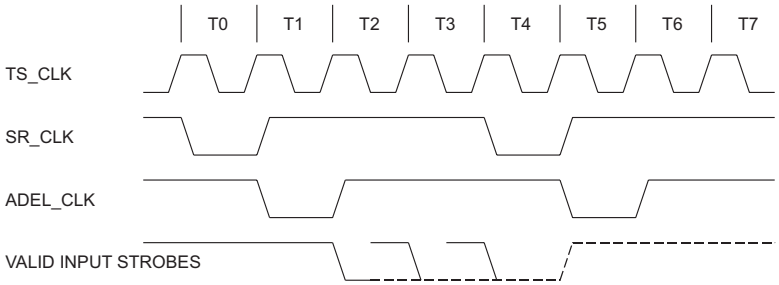


Figure 4-17 Input Mode 4 Timing Restrictions

Timing Set restrictions:

1. Do not have the falling edge of INPUT STROBE at the same time as the falling edge of ADEL_CLK..
2. The INPUT STROBE must occur at least one cell later than SR_CLK (in stimulus response applications).

Figure 4-18 below illustrates the input mode 4 timing.

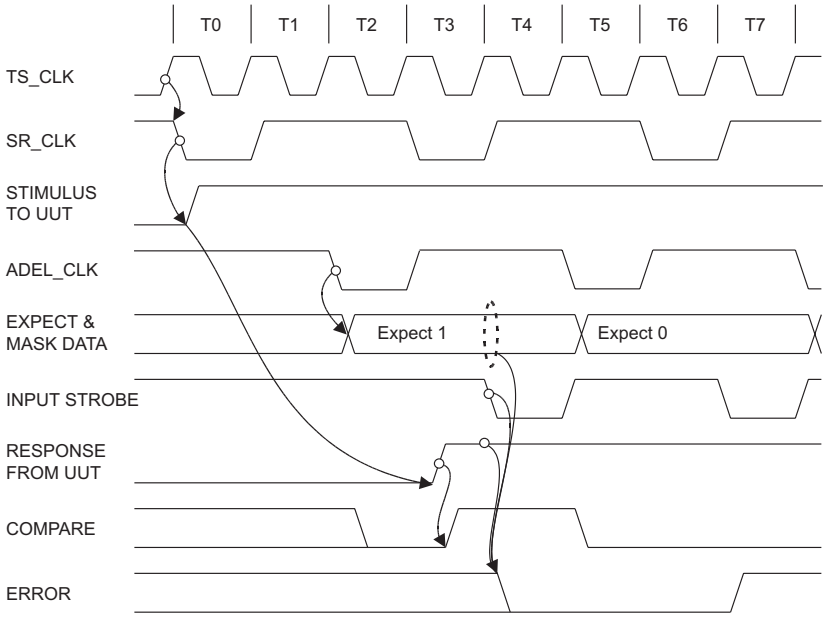


Figure 4-18 Input Mode 4 Timing

The example above illustrates recording data that generates a compare/no error followed by a non-compare/error.

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The following table describes the timing sequence in figure 4-18

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (a logic one in the example).
T2	ADEL_CLK	Falling Edge	Retrieves expect and mask data from memory (expect 1 in example).
T3	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (a logic one in the example).
T4	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.
T5	ADEL_CLK	Falling Edge	Retrieves expect and mask data from memory (expect 0 in example).
T6	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (a logic one in the example).
T7	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.

Table 4-7 Input Mode 4 Timing Description

4.3 Driver/Receiver Logic Description

Figure 4-19 below illustrates the SR105's driver/receiver logic.

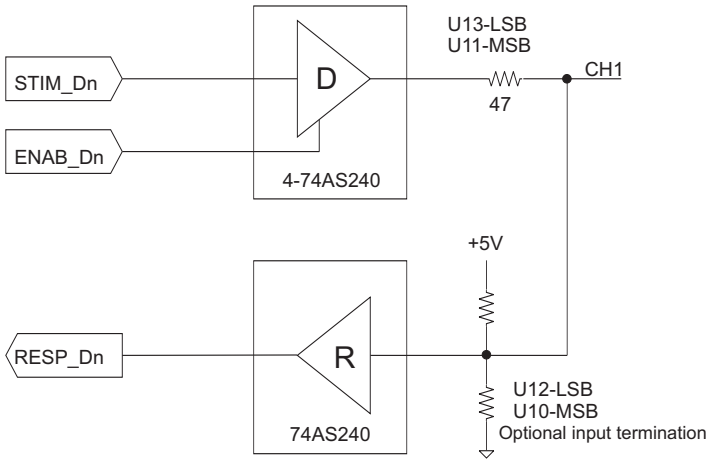


Figure 4-19 Driver/Receiver Configuration

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5 Memory Data Mapping

The following table 5-1 shows the memory data to front panel mapping.

Bit	DRA1	DRAB	DRAB	DRA4	DRA5	DRA6	DRB1	DRB2	DRB3	DRB4	DRB5	DRB6
0	CH1	CH17	CH33	CH49	CH65	CH81	CH97	C113	CH129	CH145	CH161	CH177
1	CH2	CH18	CH34	CH50	CH66	CH82	CH98	CH114	CH130	CH146	CH162	CH178
2	CH3	CH19	CH35	CH51	CH67	CH83	CH99	CH115	CH131	CH147	CH163	CH179
3	CH4	CH20	CH36	CH52	CH68	CH84	CH100	CH116	CH132	CH148	CH164	CH180
4	CH5	CH21	CH37	CH53	CH69	CH85	CH101	CH117	CH133	CH149	CH165	CH181
5	CH6	CH22	CH38	CH54	CH70	CH86	CH102	CH118	CH134	CH150	CH166	CH182
6	CH7	CH23	CH39	CH55	CH71	CH87	CH103	CH119	CH135	CH151	CH167	CH183
7	CH8	CH24	CH40	CH56	CH72	CH88	CH104	CH120	CH136	CH152	CH168	CH184
8	CH9	CH25	CH41	CH57	CH73	CH89	CH105	CH121	CH137	CH153	CH169	CH185
9	CH10	CH26	CH42	CH58	CH74	CH90	CH106	CH122	CH138	CH154	CH170	CH186
10	CH11	CH27	CH43	CH59	CH75	CH91	CH107	CH123	CH139	CH155	CH171	CH187
11	CH12	CH28	CH44	CH60	CH76	CH92	CH108	CH124	CH140	CH156	CH172	CH188
12	CH13	CH29	CH45	CH61	CH77	CH93	CH109	CH125	CH141	CH157	CH173	CH189
13	CH14	CH30	CH46	CH62	CH78	CH94	CH110	CH126	CH142	CH158	CH174	CH190
14	CH15	CH31	CH47	CH63	CH79	CH95	CH111	CH127	CH143	CH159	CH175	CH191
15	CH16	CH32	CH48	CH64	CH80	CH96	CH112	CH128	CH144	CH160	CH176	CH192

Table 5-1 Stimulus Memory Data To Front Panel Mapping

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Appendix A Glossary of Terms

A16/A24/A32	VXI Register Based Programming Mode.
ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
CSTROBE-	Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data.
ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
EXT_CLK	Selected external clock from the front panel J8 connector (EXCLK1 or EXCLK2)
FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
FUNCTION CODE(FC)	Each module in a SR192 is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
GROUP ENABLE	Group enable signal. This signal can be used to enable a group of I/O channels.
INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
INT_CLK	Selected internal timing module clock from the motherboard (10MHz, 20MHz or 50MHz).
I/O CHANNELS	Sixteen bi-directional TTL data channels.
I/O MODULE	Any of Talons Stimulus/Response modules for the SR192.
OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.

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RESPONSE	The response data of the SR192 is comprised of EXPECT, MASK and RECORD memory in five memory I/O modules and just RECORD memory in three memory I/O modules.
SEQUENCE	A sequence is the link between the timing sets and the tables.
STIM_LOAD	Timing module control signal that latches (on falling edge) the data from the stimulus memory in the output register mode. The falling edge of this control signal also registers the stimulus address (FMA) when the output register delay is enabled.
STIMULUS	The stimulus data of the SR192 is comprised of OUTPUT and TRISTATE memory located on the I/O modules.
SR_CLK	Stimulus/Response Clock. This signal, generated by the timing generator, clocks the word generator.
SUBSEQUENCE	A subsequence is a single element of a sequence. A subsequence selects a timing set, table, loop count, jump condition and control flags.
TABLE	A table is the structure that defines a FMA range for the subsequence. The FMA range is broadcast to all the I/O modules connected to the timing module.
TIMING MODULE	Any of Talons Timing Modules for the SR192.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Four pages of sixteen timing sets can be defined.
TRANSFER	See WORD.
TRISTATE Dn	Tristate driver data from the stimulus memory.
TS_CLK	Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK.
TSENABLE1	Timing Set Enable One. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight.
TSENABLE2	Timing Set Enable Two. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight.
TSINPUT1	Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT1A is routed to TSA INPUT1, TSINPUT1B is routed to TSB INPUT1.
TSINPUT2	Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT2A is routed to TSA INPUT2, TSINPUT2B is routed to TSB INPUT2.
TSOUT1	Timing Set Output One. General purpose output signal generated by the timing module.
TSOUT2	Timing Set Output Two. General purpose output signal generated by the timing module.
TSOUT3	Timing Set Output Three. General purpose output signal generated by the timing module.
TSOUT4	Timing Set Output Four. General purpose output signal generated by the timing module.

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TSOUT5	Timing Set Output Five. General purpose output signal generated by the timing module. Also used as a strobe for the SR121/SR210 probe.
TSSTROBE1	Timing Set Strobe One. This signal, generated by the timing generator, can be selected as the input strobe.
TSSTROBE2	Timing Set Strobe Two. This signal, generated by the timing generator, can be selected as the input strobe.
VADDR	The address bus from the VXI Backplane.
VDATA	The data bus from the VXI Backplane.
VECTOR	See WORD.
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192.

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Appendix B Function Code Map

Address Location:

Driver/Receiver modules are each given a 256K word address space starting at 0x200000.

Specifications:

The SR105 is a five memory D/R module.

- Output
- Tristate
- Expect
- Mask
- Record
- Masked error (virtual)
- Response (virtual)

Sixteen input/output (TTL) 128K per channel, algorithmic.

Function Code Assignments:

FC0 Read/write OUTPUT data memory.
128K x 16 word and byte access. 1- outputs a high level.

FC1 Read/write TRISTATE memory.
128K x 16 word and byte access. 1- disables driver output.

FC2 Read/write EXPECT memory.
128K x 16 word and byte access. See table below.

FC3 Read/write MASK memory.
128K x 16 word and byte access.

MASK	EXPECT	Result Condition
0	0	Expect logic zero '0'
0	1	Expect logic one '1'
1	0	Masked off (Record as expect zero) 'M'
1	1	NU

FC4 Read/write RECORD memory.
128K x 16 word and byte access.

DATA RECEIVED	EXPECT CODE FROM ABOVE		
	'0'	'1'	'M'
'0'	0	1	0
'1'	1	0	1

FC5 Read ERROR data.
128K x 16 word and byte access.

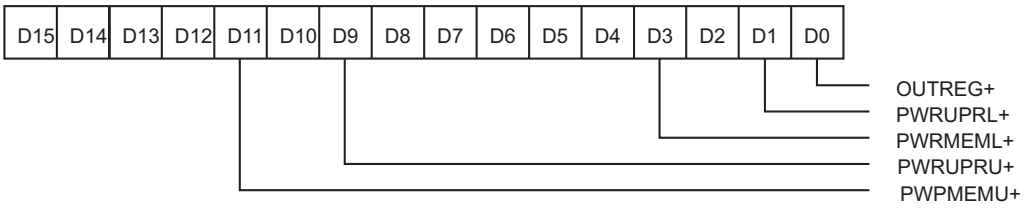
DATA RECEIVED	EXPECT CODE FROM ABOVE		
	'0'	'1'	'M'
'0'	0	1	0
'1'	1	0	0

FC6 Read RESPONSE data (unmasked error & expect low).
128K x 16 word and byte access.

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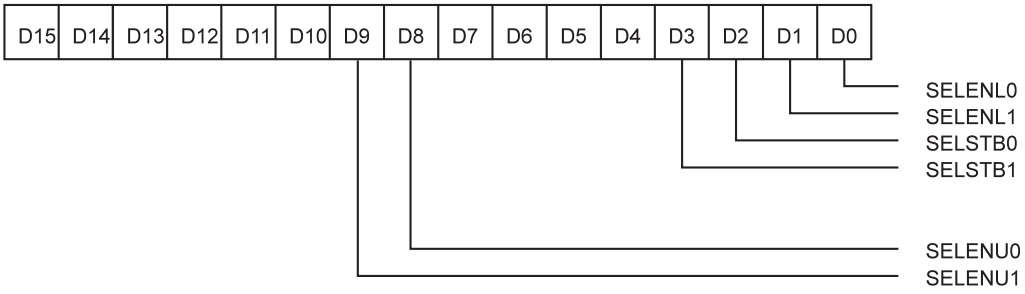
DATA RECEIVED	EXPECT CODE FROM ABOVE		
	'0'	'1'	'M'
'0'	0	0	0
'1'	1	1	1

FC8 Write output/power management register.
The output/power management register programs the output register setting as well as power saving modes.



OUTREG+	Output Register Enable (1-Enable output register all 16 channels)
PWRUPRL+	Driver Power Enable LSB (1-Turns on all eight LSB drivers)
PWRMEML+	Turn on Driver/Receiver Memory Power LSB (1-Turns on LSB memory power
PWRUPRU+	Driver Power Enable MSB (1-Turns on all eight MSB drivers)
PWRMEMU+	Turn on Driver/Receiver Memory Power MSB (1-Turns on MSB memory power)

FC9 Write I/O control register.
The I/O control register programs the group enable and input strobe selectors.



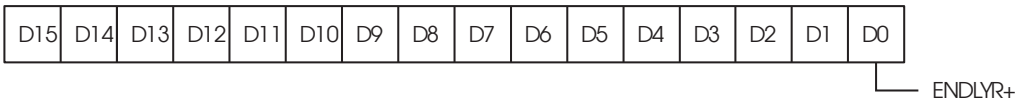
SELEN(L/U)1	SELEN(L/U)0	Selected Enable (LSB/MSB)
0	0	TSENable1
0	1	TSENable2
1	0	FCNTl1
1	1	FCNTl2/CARDS

SELSTB1	SELSTB0	Selected Input Strobe (all 16 channels)
0	0	TSSTrobe2
0	1	FCNTL2
1	0	CSTROBE
1	1	TSSTrobe1 (Rev D or later)

FC10 Write card control register

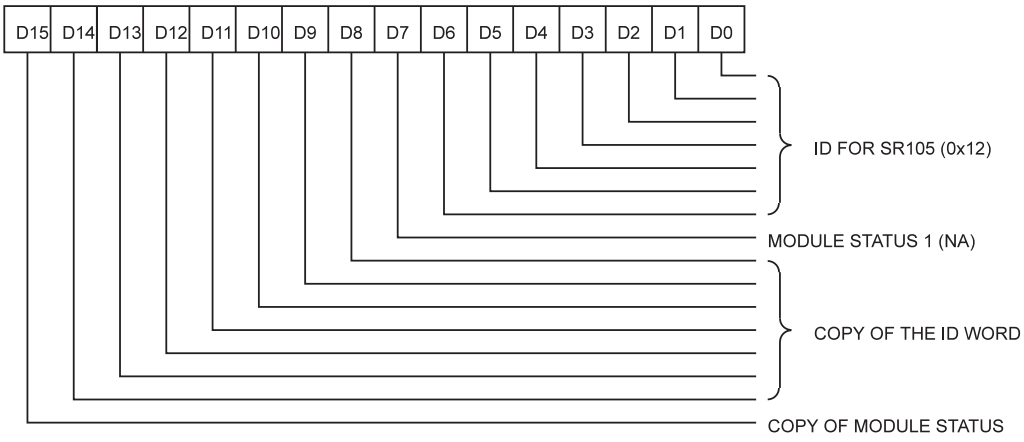
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This register enables/disables the input address delay register, 1-enables the delay register.



FC11 Write drive fault latch reset.
This decode resets the drive fault signal for this module.

FC15 Read status/ID register.



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Appendix C SR192 Clock Timing

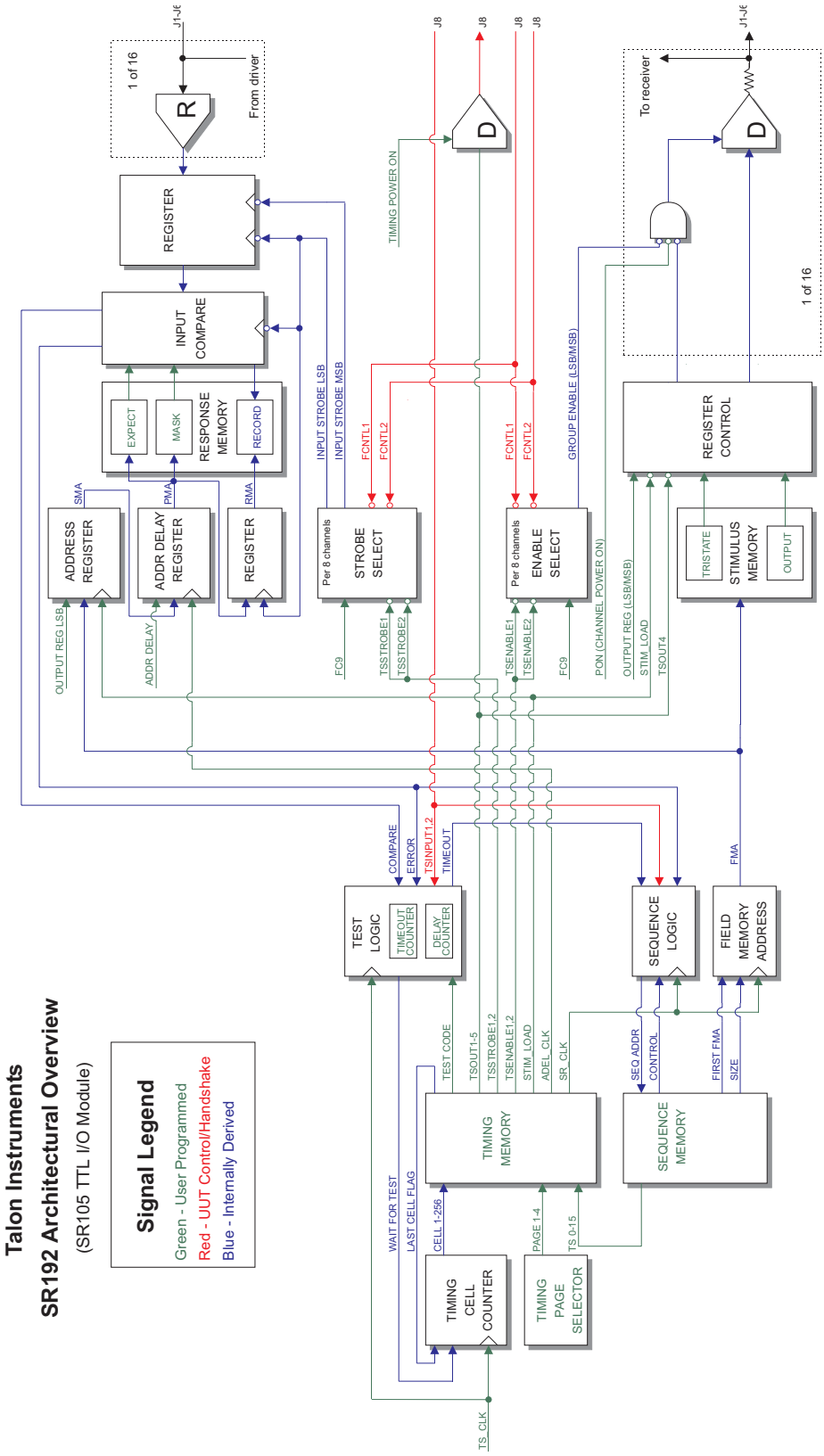
This appendix gives the SR192 clock timing relationships.

Description	From	To	Typ (AS)
External Clock One Propagation TTL Setting.	EXCLK1	TS_CLK	27-A 31-B
External Clock One Propagation Programmable Setting.	EXCLK1	TS_CLK	32-A 36-B
External Clock One Propagation Differential Setting.	EXCLK1	TS_CLK	54-A 57-B
External Clock Two Propagation.	EXCLK2	TS_CLK	22
Internal Clock to TSA Output Clock Propagation TTL Setting.	TS_CLK	CLOCKA	8
Internal Clock to TSA Output Clock Propagation Programmable Setting.	TS_CLK	CLOCKA	11
Internal Clock to TSA Output Clock Propagation Differential Setting.	TS_CLK	CLOCKA	17
Internal Clock to TSB Output Clock Propagation.	TS_CLK	CLOCKB	4

Programmable measurements were made with VOH set to +5V, VOL set to 0V, VISR set to +2V and VIL set to +2.5V.

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Appendix D Block Diagram



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