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REFERENCE MANUAL

Talon Instruments™

SR114

8-Channel Variable Voltage Stimulus/Response Module

EADS NORTH AMERICA

Publication Date: 04/24/06
Publication Number: SRMM912 Rev. A
Instrument Part Number: SR114

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If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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1 Introduction

Talon's SR192 digital test module is a modular VXI stimulus/response system. The SR192 motherboard is a two slot, "C" size module which houses up to 12 I/O modules. I/O modules are designed to provide either 8 or 16 stimulus/response channels for a total of 96 or 192 channels. Modules provide many logic options such as fixed voltage TTL, ECL, RS485/422 or variable voltages. The I/O channels may also be single-ended or double-ended (differential) logic.

Multiple SR192's may be linked in a master/slave configuration to provide up to 1152 channels in a single VXI 13-slot chassis.

This manual is for the SR114 I/O module. The SR114 is an 8 channel, dynamic, single-ended variable voltage I/O module. Each SR114 has a single 8 channel group allowing up to 12 groups in a single SR192. The 8 I/O channels are bi-directional using a tristate memory to control direction on a per pin basis. A jumper block on the SR114 allows the channels to be split into 8 outputs and 8 inputs. The output enable and input strobe signals are assigned in groups of 8 channels. The output high and low levels along with the input high and low thresholds are all user programmable from -15V to +15V.

The SR114 utilizes a five memory architecture, OUTPUT, TRISTATE, EXPECT, MASK and RECORD. This architecture allows the user to perform real-time error detection and recording. Each memory is 128K bits per channel.

The SR114 is a multi-function I/O module. Talon's multi-function I/O modules provide several operating modes in addition to the normal parallel stimulus/response operation. These special operating modes are:

Multiplex	This mode allows the user to program one or more 8 channel groups to operate as 4 channels with double the memory and twice the data rate.
Serial	This mode allows the user to send and receive data through a single channel of the 8 channel group. Adjacent 8 channel groups may be linked to provide for 16, 32, etc., bit words. This mode provides the user with the ability to easily emulate serial busses as well as increasing the memory depth.
Algorithmic	This mode provides a bit shift function that operates on the data stored in the output register. Using this mode an engineer can easily generate incremented data such as addresses for RAM or ROM testing without using I/O memory. The 8 channel groups may be linked to provide wider data words.
Data Format	This operating mode provides the standard formatting modes, RTO, RTC, RTZ and HOLD. Each 8 channel group may be assigned the same or a different format from the other groups.

The layout of this manual is in five sections described below:

1. Introduction	This section
2. Specifications	SR114 electrical and environmental specifications
3. Jumpers/Installation	Description of the jumpers and installation of the SR114
4. Functional Description	SR114 functional description
5. Memory Data Mapping	Memory to channel mapping

In addition, five appendices are included:

A. Glossary of Terms	Definition of terms used in this manual
B. Function Code Map	Hardware register descriptions
C. Programming Examples	SR114 stimulus/response programming examples
D. SR192 Clock Timing	SR192 clock timing specifications.
E. SR114 Block Diagram	SR192/SR114 system block diagram.

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2 Specifications

The following sections list the specifications of the SR114 I/O module.

2.1 I/O Module

Number of channels	8 bi-directional or 8 stimulus & 8 response
Number of Stimulus Memories	2
OUTPUT, TRISTATE	
Number of Response Memories	3
EXPECT, MASK, RECORD	
Data Format Channel Modes	
Non Return	HOLD
Return to Zero	RTZ
Return to One	RTO
Return to Compliment	RTC
Algorithmic Increment Channel Modes	
Increment by one	INCREMENT1
Increment by two	INCREMENT2
Increment by four	INCREMENT4
Increment by eight	INCREMENT8
Data Shift Channel Modes	
Shift by one	SERIAL
Shift by four	MULTIPLEX
Memory depth per channel (Data format and increment modes)	131072
Memory depth per channel (MULTIPLEX)	262144
Memory depth per channel (SERIAL)	1048576
Maximum stimulus data rate parallel (8 channels)	25 MHz (TTL Levels)
Maximum stimulus data rate multiplexed (4 channels)	50 MHz (TTL Levels)
Stimulus group enable signal (common to all channels)	4
Internal (TSENABLE1, TSENABLE2)	2
External (FCNTL1, FCNTL2[1] or CSTROBE[1])	2
Stimulus group enable resolution	one TS_CLK
Maximum response data rate parallel (8 channels)	25 MHz (TTL Levels)
Maximum response data rate multiplexed (4 channels)	50 MHz (TTL Levels)
Response input strobe signal (common to all channels)	4
Internal (TSSTROBE1, TSSTROBE2)	2
External (FCNTL2, CSTROBE)	2
Response input strobe resolution	one TS_CLK
Response shift strobe signal (MULTIPLEX/SERIAL mode)	2
Internal (TSSTROBE1)	1
External (FCNTL1)	1
Response shift strobe resolution	one TS_CLK
Output Driver	Elantec EL1056
Input Receiver	Elantec EL2252

Note 1: Jumper selectable

2.2 Electrical

High Level Output Voltage	-5V to +15V
High Level Source Current	50 mA max
Low Level Output Voltage	+5V to -15V
Low Level Sink Current	50 mA max
Voltage Swing	20V max
AC Current (200 nsec max)	200 mA
Output Impedance (with 47Ω series termination)	50Ω typ
Output Slew Rate	0.7V/nsec typ[2]
Short Circuit Protected	Yes
High Input Threshold	-5V to +15V
Low Input Threshold	+5V to -15V
Input Impedance (Bi-directional)	>26KΩ
Input Impedance (Uni-directional)	30KΩ

Note 2: User programmable (default values given)

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2.3 Timing Characteristics

In order to specify the timing characteristics of the SR114, the TS_CLK signal generated by the timing module will be used as the reference signal. Appendix D of this manual gives the timing relationship between the external input clocks (EXCLK1 and EXCLK2), TS_CLK and external output clocks (CLOCKA and CLOCKB).

Table 2-1 lists the typical timing characteristics of the SR114's stimulus/response logic.

Parameter and Description	From	To	Typ (ns)	Note
Stimulus Specifications				
Data Propagation	TS_CLK	CH OUTPUT	16-18	2,4
Tristate Propagation enabled	TS_CLK	CH OUTPUT	18-22	4
Tristate Propagation disabled	TS_CLK	CH OUTPUT	18-22	4
Internal clock to group enable true	TS_CLK	GROUP ENABLE	15-19	1
Internal clock to group enable false	TS_CLK	GROUP ENABLE	13-17	1
Field control one to group enable true.	FCNTL1-TTL	GROUP ENABLE	17-26	1
	FCNTL1-PROG		25-33	1
	FCNTL1-DIFF		49-62	1
Field control one to group enable false.	FCNTL1-TTL	GROUP ENABLE	14-21	1
	FCNTL1-PROG		23-30	1
	FCNTL1-DIFF		49-56	1
Field control two to group enable true.	FCNTL2	GROUP ENABLE	20-28	1
Field control two to group enable false.	FCNTL2	GROUP ENABLE	16-22	1
Card strobe to group enable true.	CSTROBE	GROUP ENABLE	13-16	1
Card strobe to group enable false.	CSTROBE	GROUP ENABLE	8-11	1
Group enable to valid data.	GROUP ENABLE	CH OUTPUT valid	13-16	4
Group enable to invalid data.	GROUP ENABLE	CH OUTPUT invalid	13-16	4
Receiver Specifications				
Receiver propagation	CH INPUT	RESP VALID	8-14	3,4
Internal clock to response strobes.	TS_CLK	INPUT/SHIFT STROBE	12-16	1
Field control one to response strobes.	FCNTL1-TTL	INPUT/SHIFT STROBE	14-23	1
	FCNTL1-PROG		21-29	1
	FCNTL1-DIFF		46-57	1
Field control two to response strobe.	FCNTL2	INPUT STROBE	17-25	1
Card strobe to response strobe.	CSTROBE	INPUT STROBE	7-10	1
Data valid setup to input strobe.	RESP VALID	INPUT/SHIFT STROBE	5	-

Note 1: The range of delay accounts for the number of modules installed and their position in the SR192 system.
Note 2: VOL = 0, VOH = 5, VISR = 2
Note 3: 0 to 5V input, VIH, VIL = 20 to 80% of swing
Note 4: The range of delay accounts for the position of the SR114 in the SR192 system.

Table 2-1 Stimulus/Response Timing Characteristics

2.4 Environmental

Temperature Range

Operating ..... 0° C to +50° C
Storage ..... -40° C to +71° C (RH not controlled)

Altitude

Operating ..... Sea level to 10,000 ft.
Storage ..... Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C ..... not controlled

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+11°C to +30°C ..... 95+/-5%RH
+31°C to +40°C ..... 75+/-5%RH
+41°C to +50°C ..... 45+/-5%RH

2.5 Size

Dimension

4.93 cm x 22.61 cm (1.94" x 8.9")

Weight

.091 kg (3.2 oz)

2.6 Power Requirements

The current requirements listed in table 2-2 are for a single SR114 with the drivers unloaded.

Voltage	Peak Current	Dynamic Current	Note
+5V	1.0 A	0.34A	-
-5.2V	0	0	-
-2V	0	0	-
+12V	0	0	-
-12V	0	0	-
+24V	0	0	-
-12V	0	0	-
V+	1.04A	0.55A	-
V-	1.06A	0.57A	-

Table 2-2 SR114 Voltage Requirements

The following specifications list the front panel J10 V+ and V- voltage requirements.

V+ maximum ..... +20V
V+ minimum ..... +7V
V- maximum ..... -7V
V- minimum ..... -20V
V+ to V- maximum 32V
V+ minimum headroom from VOH/VIH ..... +4V
V- minimum headroom from VOL/VIL ..... -4V

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3 Jumpers/Installation

The SR114 I/O module requires firmware revision 1.28 or later for proper operation. Contact Talon Instruments for information on firmware upgrades.

Figure 3-1 below is a locator diagram for test points and jumpers located on the SR114.

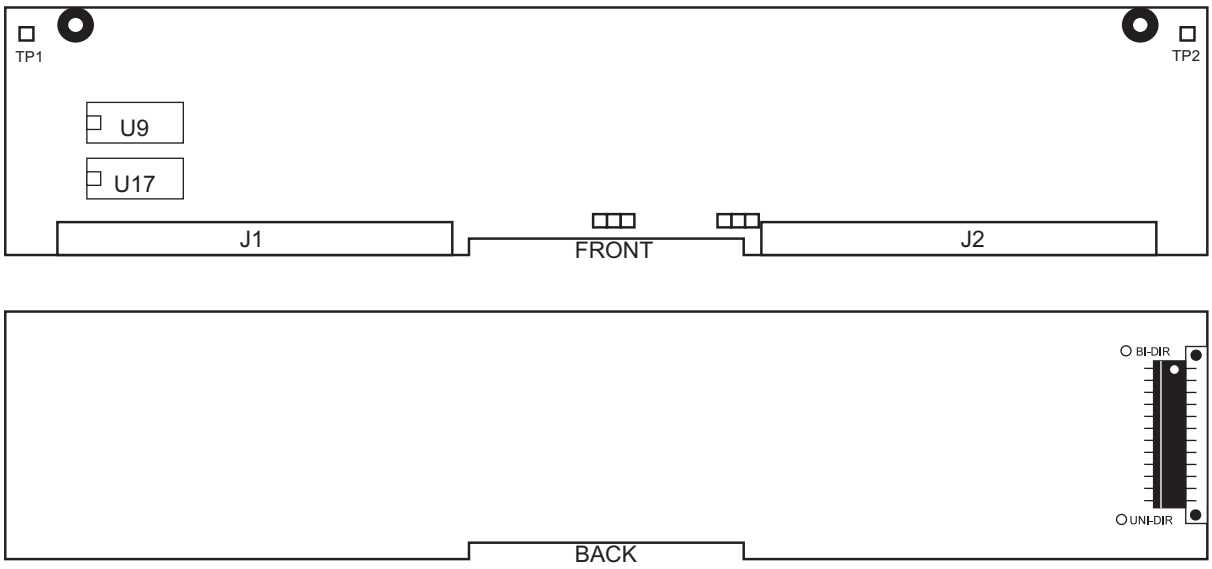


Figure 3-1 Test Point/Jumper Locations

3.1 Test Point Description

Table 3-1 describes the test points on the SR114 I/O module.

Test Point	Mnemonic	Description
TP1	GND1	Signal ground
TP2	GND2	Signal Ground

Table 3-1 SR114 Test Point Description

3.2 Jumper Description

The following sections describe the SR114 jumper options.

3.2.1 External Group Enable Select (E1, E2, E3)

This jumper block is used to select between CSTROBE and FCNTL2 for the group enable input assigned to FCNTL2. Connect E2-E3 for FCNTL2 (factory default). Connect E1-E2 for CSTROBE.

CAUTION

A small trace may be present (factory default) which connects E2-E3. Cut this trace before jumpering E1-E2.

3.2.2 Bi-directional vs. Uni-Directional Select (J101)

This jumper choice selects the setting of the I/O channels as bi-directional or uni-directional. When bi-directional is selected, the 8 I/O channels will be connected to channels 1-8, 17-24, 33-40, etc. When

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uni-directional is selected, the output drivers will be connected to channels 1-8, 17-24, 33-40, etc., while the input receivers will be connected to channels 9-16, 25-32, 41-48, etc.

3.2.3 Factory Jumpers (E4, E5, E6)

These jumpers are reserved and are used to enable the reprogrammable logic on the SR114. For normal operation, connect E4-E5.

3.3 Installation

Each SR192 motherboard can house up to 12 I/O modules. I/O modules are installed in motherboard slots DRA1 through DRA6 and DRB1 through DRB6, see Figure 3-2.

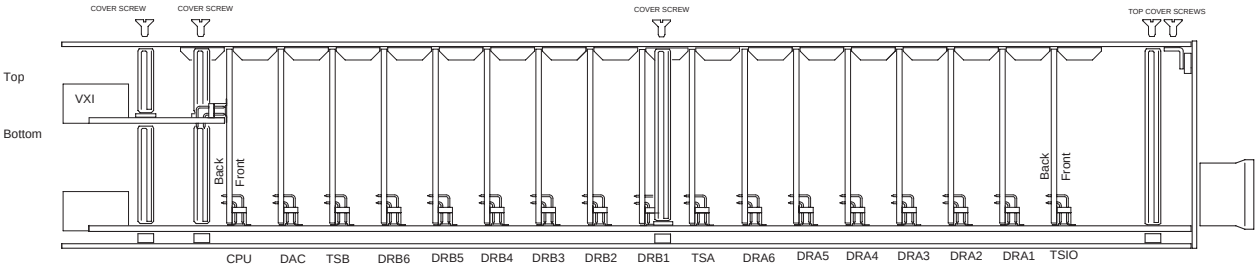


Figure 3-2 SR192 Motherboard Side View

Perform the following steps to add or replace an I/O module:

Step 1. Using ESD protocols remove the SR192 from the VXI chassis.

Step 2. Remove the top cover screws, refer to Figure 3-2.

Step 3. If replacing an I/O module, remove it by grasping at each corner and gently rocking forward and back while pulling it away from the motherboard.

Step 4. Insert the I/O module in the desired DRA or DRB module slot, Figure 3-2, by lining up the J1 and J2 connectors with the motherboard connectors and gently pushing down. All SR192 modules are keyed along the associated mating connector. If the module cannot be inserted, check for bent pins and make certain the pins are aligned with the mating connector on the motherboard.

CAUTION

Although the modules and the associated mating connectors have been keyed, it is possible to force a module into an incorrect slot.

3.3.1 Voltage Group Positioning

The SR192 provides 3 voltage groups which are determined by the physical location of an installed SR114. Group one is comprised of modules located in slots DRA1 through DRA6. Group two uses slots DRB1 through DRB3 with optionally jumpered DRB4. Group Three uses slots DRB5 and DRB6 with optionally jumpered DRB4.

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Figure 3-3 illustrates the SR192 motherboard voltage group routing.

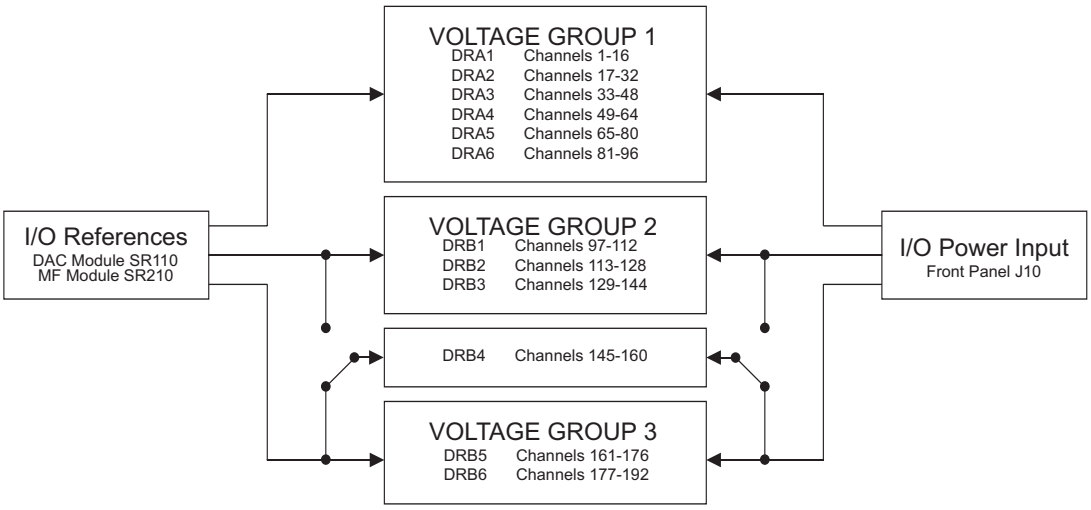


Figure 3-3 SR192 Motherboard Voltage Groups

3.4 Termination Options

The SR114 is shipped from the factory with 47Ω series termination resistors on each channel. These 8 resisters are installed in U9, see figure 3-1. Additional series termination resistors may be added in paralleled with these in U17.

U9 and U17 are sixteen pin dip resister packages, Bourns part number 4116R-001-470. The resistor packs can be removed or changed by the user.

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4 Functional Description

The SR114, along with all the other I/O modules, is controlled through the SR192 timing modules. Control signals are generated by the timing module which allow the SR114 to output stimulus data and record response data while the timing module is running. When the timing module is not running, idle, the CPU module or VXI controller can program or query the stimulus/response memories on the SR114.

Figure 4-1 depicts an SR114 module in relation to other components of the SR192.

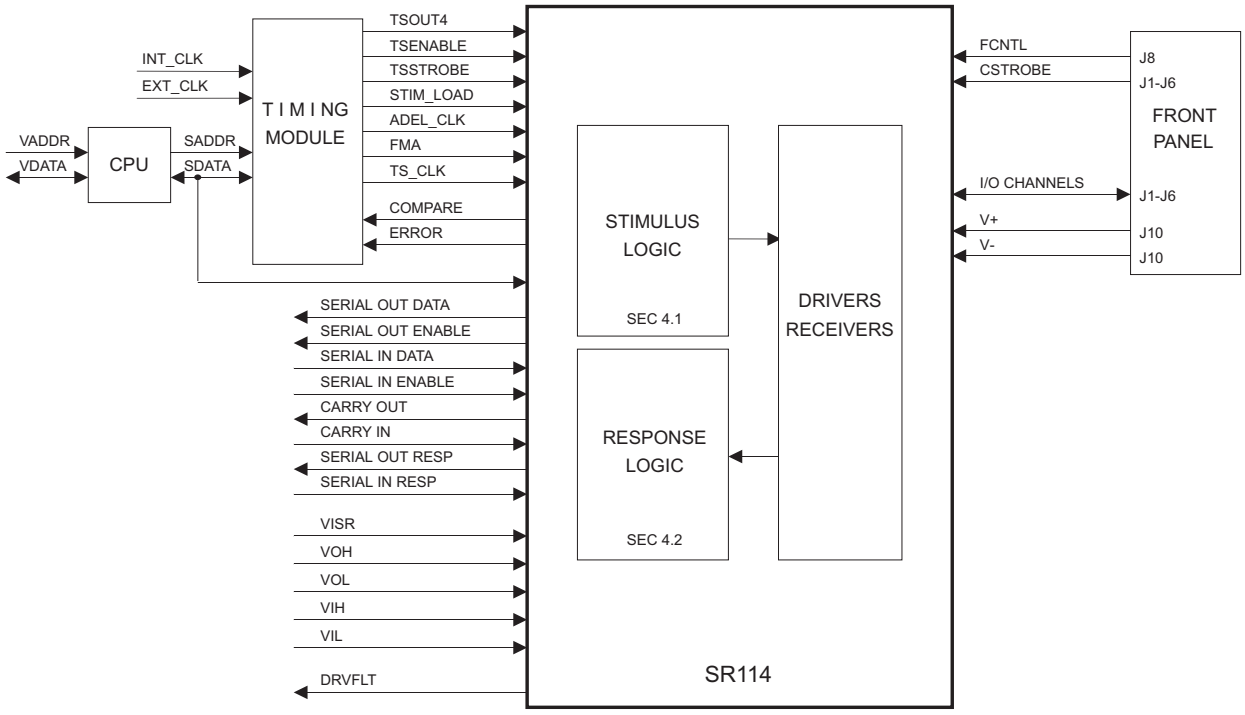


Figure 4-1 SR114 Block Diagram

The following list describes the functional blocks shown in figure 4-1 above.

1.	CPU	The SR192 CPU module selects whether the local processor or VXI Backplane has control of the system bus, SADDR and SDATA.
2.	TIMING MODULE	One of two SR192 timing modules, SR100 or SR101.
3.	STIMULUS LOGIC	The memories, registers and control bits that generate UUT input data.
4.	RESPONSE LOGIC	The memories, registers and control bits that record UUT output data.
5.	DRIVERS/RECEIVERS	The driver/receiver ICs and terminators that connect the STIMULUS/RESPONSE logic to the UUT.
6.	FRONT PANEL	The mating connectors through which a physical connection is made to the UUT.

The following list describes the signals shown in figure 4-1 above.

1.	INT_CLK	Selected internal timing module clock from the motherboard (10MHz, 20MHz or 50MHz).
2.	EXT_CLK	Selected external clock from the front panel J8 connector (EXCLK1 or EXCLK2)
3.	VADDR	The address bus from the VXI Backplane.
4.	VDATA	The data bus from the VXI Backplane.
5.	SADDR	Either the local microprocessor or VADDR bus.
6.	SDATA	Either the local microprocessor or VDATA bus.
7.	TSOUT4	Timing module signal used to enable the selected channel mode function.
8.	TSENABLE	Two timing module signals which can be selected as the group enable for the stimulus data.
9.	TSSTROBE	Two timing module signals which can be selected to strobe response data.

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10.	STIM_LOAD	Timing module signal used to enable data from the output and tristate memories into the stimulus register and clock an input address delay register.
11.	ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
12.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word.
13.	TS_CLK	The timing module clock (EXT_CLK or INT_CLK).
14.	COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
15.	ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
16.	SERIAL OUT DATA	Stimulus output signal to adjacent lower SR114, 8 channel group for SERIAL function mode.
17.	SERIAL OUT ENABLE	Stimulus enable signal to adjacent lower SR114, 8 channel group for SERIAL function mode.
18.	SERIAL IN DATA	Stimulus input data from adjacent higher SR114, 8 channel group for SERIAL function mode.
19.	SERIAL IN ENABLE	Stimulus input enable signal from adjacent higher SR114, 8 channel group for SERIAL function mode.
20.	CARRY OUT	Carry output signal to adjacent higher SR114, 8 channel group for INCREMENT function modes.
21.	CARRY IN	Carry input signal from adjacent lower SR114, 8 channel group for INCREMENT function mode.
22.	SERIAL OUT RESP	Response output to adjacent lower SR114, 8 channel group for SERIAL function mode.
23.	SERIAL IN RESP	Response input from adjacent higher SR114, 8 channel group for SERIAL function mode.
24.	VISR	Output driver slew rate voltage set by the internal DACs (SR110 or SR210) or external reference inputs from the front panel connector J9.
25.	VOH	High output voltage references set by the internal DAC's (SR110 or SR210) or external reference inputs from front panel connector J9.
26.	VOL	Low output voltage references set by the internal DAC's (SR110 or SR210) or external reference inputs from front panel connector J9.
27.	VIH	High input voltage references set by the internal DAC's (SR110 or SR210) or external reference inputs from front panel connector J9.
28.	VIL	Low input voltage references set by the internal DAC's (SR110 or SR210, or external reference inputs from front panel connector J9.
29.	DRVFLT	Driver signal generated when the output current exceeds 60mA for greater than 1ns.
30.	FCNTL	Two front panel input signals that can be selected to either enable stimulus or strobe response data.
31.	CSTROBE	Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data.
32.	I/O CHANNELS	Eight bi-directional or 8 output/8 input data channels.
33.	V+	Positive input voltage from J10 used to supply power to the variable voltage driver/receiver I/O modules.
34.	V-	Negative input voltage from J10 used to supply power to the variable voltage driver/receiver I/O modules.

The following sections describe the three major logic elements of the SR114 (Stimulus, Response and Driver/Receiver).

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4.1 Stimulus Logic

Figure 4-2 shows the stimulus logic block diagram.

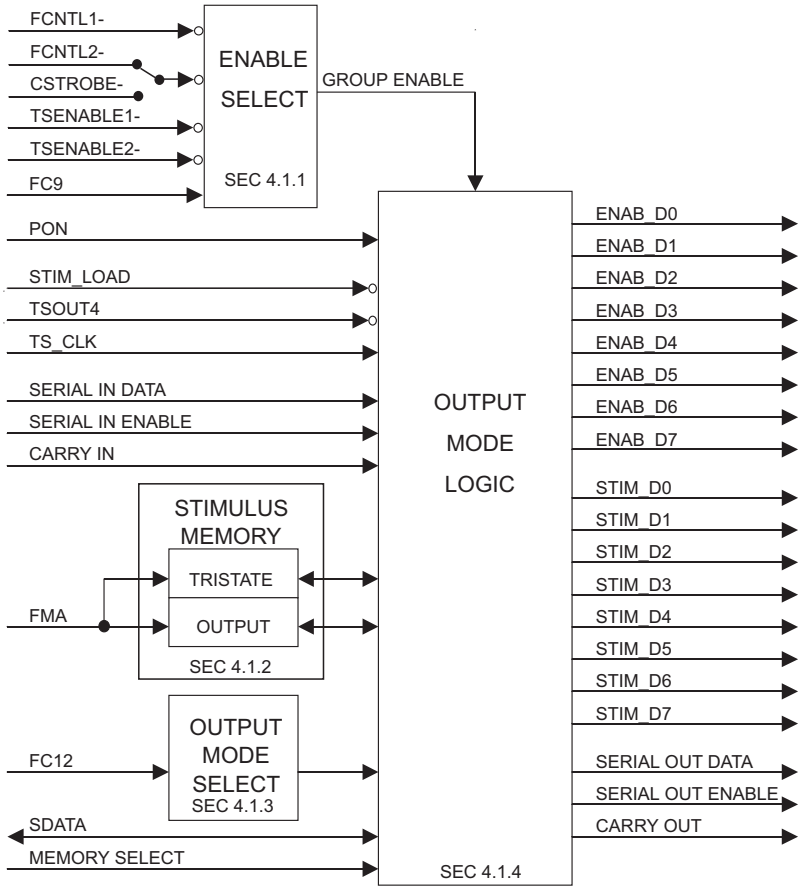


Figure 4-2 Stimulus Logic Block Diagram

The following list describes the functional blocks of figure 4-2.

1.	ENABLE SELECT	Used to select the group enable signal. The group enable signal allows the operator to enable all eight drivers for a portion of the timing cycle.
2.	STIMULUS MEMORY	Two 128K by 8 memories allows the operator to define the logic level and enable any of the 16 drivers during an output word.
3.	OUTPUT MODE SELECT	Allows the operator to program the channel mode function.
4.	OUTPUT MODE LOGIC	Hardware that performs the selected channel function mode.

The following list describes the signals shown in figure 4-2 above.

1.	FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
2.	FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
3.	CSTROBE-	Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data. The enable selection is jumpered on the SR114 and replaces FCNTL2 when selected.
4.	TSENABLE1	Timing Set Enable 1 from the timing module.
5.	TSENABLE2	Timing Set Enable 2 from the timing module.
6.	FC9	Control signals used to program the strobe/group enable selector. Refer to Appendix B.
7.	PON	Power on signal routed to all the I/O modules. Set by the "OUTPUT:CHANNEL:STATE (ON | OFF) command.
8.	STIM_LOAD	Timing module signal that enables data from the output and tristate memories to the stimulus registers and clock an input address delay register.
9.	TSOUT4	Timing module signal that causes the selected channel mode function to be loaded into the mode logic registers.
10.	TS_CLK	The selected timing module clock.

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11.	SERIAL IN DATA	Stimulus data input signal from adjacent higher SR114 8 channel group for SERIAL function mode.
12.	SERIAL IN ENABLE	Stimulus enable input signal from adjacent higher SR114 8 channel group for SERIAL function mode.
13.	CARRY IN	Carry input signal from adjacent lower SR114 8 channel group for INCREMENT function mode.
14.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word.
15.	FC12	Control signals used to program the channel function mode. Refer to appendix B.
16.	SDATA	The selected data bus used to program and query the stimulus memories.
17.	MEMORY SELECT	This signal allows the user to program or query the tristate or output memory.
18.	GROUP ENABLE	Group enable signal. This signal can be used to enable a group of I/O channels.
19.	ENAB_D0-ENAB_D7	Registered enable signals to the output drivers.
20.	STIM_D0-D7	Data to the output driver.
21.	SERIAL OUT DATA	Stimulus data signal to adjacent lower SR114 8 channel group for SERIAL function mode.
22.	SERIAL OUT ENABLE	Stimulus enable signal to adjacent lower SR114 8 channel group for SERIAL function mode.
23.	CARRY OUT	Carry output signal to adjacent higher SR114 8 channel group for INCREMENT function modes.

4.1.1 Enable Select

The enable logic allows the user to select the GROUP ENABLE signal.

The GROUP ENABLE signal must be true (low) to enable output drivers. This functionality is required for simulating channels which are enabled and disabled as a synchronous group.

4.1.2 Stimulus Memories

The Stimulus memories on the SR114 consist of two 128k x 8 bit static RAM's. The first memory contains the TRISTATE data and the second contains the OUTPUT data. Bits 0-7 of word "n" of the tristate memory corresponds to and enable bits 0-7 of word "n" of the output data.

Both of the output memories are addressed by the FMA bus generated by the timing module. Each FMA value causes a new output and tristate word.

4.1.3 Output Mode Select

For each SR114 I/O module, the CPU must first define the function which is to be performed by the mode logic.

The following functions may be selected for each module.

Data Format Functions:

1. HOLD — Load the present data back into the output register
2. RTZ — Return to zero: set all bits of the output register to the logic 0 state.
3. RTO — Return to one: set all bits of the output register to the logic 1 state.
4. RTC — Return to compliment: set all bits of the output register to the compliment of its present state.

Algorithmic Increment Functions:

1. INCR1 — Increment by one: clock the output register to its present value plus 1.
2. INCR2 — Increment by two: clock the output register To its present value plus 2.
3. INCR4 — Increment by four: clock the output register to its present value plus 4.
4. INCR8 — Increment by eight: clock the output register to its present value plus 8.

Shift Functions:

1. SERIAL — Shift by one: clock the output register data from bit n into bit n-1 (i.e. Data shifted out the least significant channel (LSN)). Bit 0 of a higher 8 channel group is clocked into bit 7 of the adjacent lower 8 channel group.
2. MULTIPLEX — Shift by 4: clock the output register data from bits 7 through 4 into bits 3 through 0 (i.e. Data shifted out the least significant nibble (LSN)).

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CAUTION

Each I/O module may select a different function, however, modules programmed as serial must be assigned to the lower channels to avoid a signal conflict between adjacent modules.

4.1.4 Output Mode Logic

The SR114 output mode logic unit, in figure 4-2, between the stimulus memories and the output drivers is illustrated in figure 4-3 below.

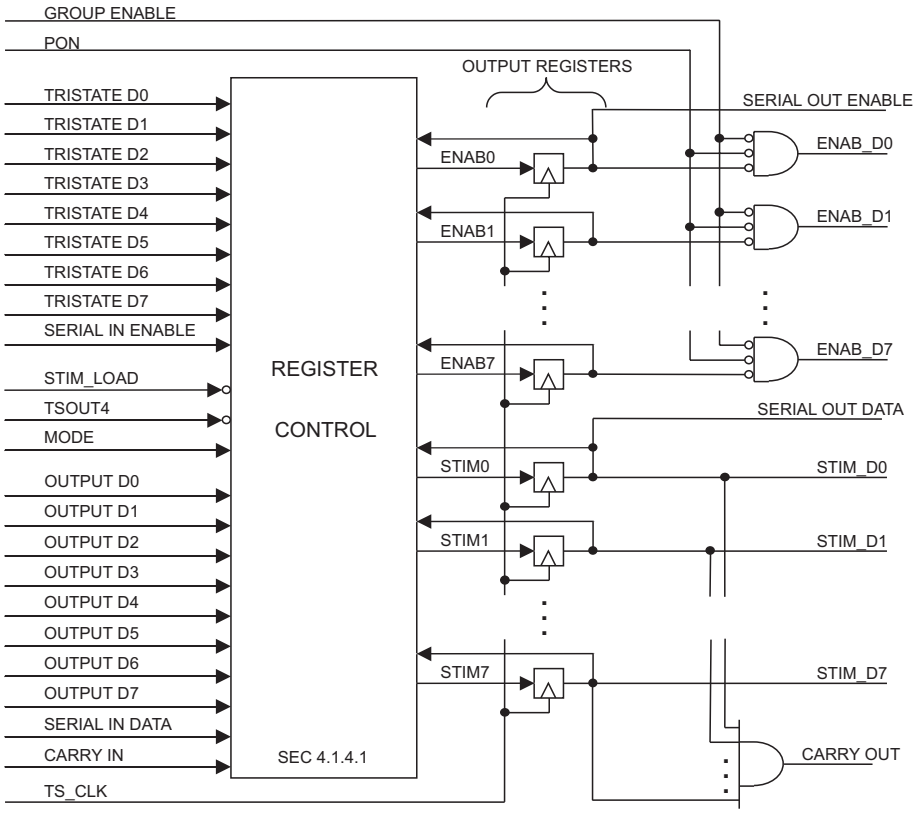


Figure 4-3 Output Mode Logic Block Diagram

The following list describes the functional blocks of figure 4-3.

1.	REGISTER CONTROL	Used to select the data source for the stimulus registers.
2.	OUTPUT REGISTERS	These registers contain the enable and data values for the output drivers.

The following list describes the signals shown in figure 4-3 above.

1.	GROUP ENABLE	Group enable signal. This signal can be used to enable a group of 8 I/O channels.
2.	PON	Power on signal routed to all the I/O modules. Set by the "OUTPUT:CHANNEL:STATE (ON | OFF) command.
3.	TRISTATE D0-D7	Tristate driver data from the stimulus memory.
4.	SERIAL IN ENABLE	Enable input signal from adjacent higher SR114 8 channel group for SERIAL function mode.
5.	STIM_LOAD	Timing module signal that enables the data from the output and tristate memories to the output registers and clock an input address delay register.
6.	TSOUT4	Timing module signal that selects the function data as the output register inputs.
7.	MODE	Selected function mode from mode select, refer to section 4.1.3.
8.	OUTPUT D0-D7	Data from the output memory.
9.	SERIAL IN DATA	Data input signal from adjacent higher SR114 8 channel group for SERIAL function mode.
10.	CARRY IN	Carry input signal from adjacent lower SR114 8 channel group for INCREMENT function mode.

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11.	TS_CLK	The timing module clock.
12.	SERIAL OUT ENABLE	Enable signal output to adjacent lower SR114 8 channel group for SERIAL function mode.
13.	ENAB0-ENAB7	Selected enable signal from the register control block.
14.	ENAB_D0-ENAB_D7	Registered enable signals to the output drivers.
15.	SERIAL OUT DATA	Data signal output to adjacent lower SR114 8 channel group for SERIAL function mode.
16.	STIM0-STIM7	Selected data signal from the register control block.
17.	STIM_D0-STIM_D7	Registered data signal.
18.	CARRY OUT	Carry output signal to adjacent higher SR114 8 channel group for INCREMENT function modes.

4.1.4.1 Driver Enable Logic

Table 4-1 below illustrates the affects of the PON and GROUP ENABLE signals along with the tristate and output memory data on the driver output.

PON	GROUP ENABLE	TRISTATE MEMORY	OUTPUT MEMORY	DRIVER OUTPUT
HIGH	X	X	X	High Z
LOW	HIGH	X	X	High Z
LOW	LOW	1	X	High Z
LOW	LOW	0	0	VOL
LOW	LOW	0	1	VOH

Table 4-1 Stimulus Memory Description

As shown in table 4-1 above, three conditions must be true in order to enable the output driver:

1. The power-up register (PON) must be set true (LOW).
2. The selected group enable signal must be true (LOW).
3. The respective bit from the tristate memory must be true (LOW).

4.1.4.2 Output Register Control

The register control logic selects the data source for the output registers. Each rising edge of the TS_CLK signal loads the output registers with one of the following three data signals:

- Stimulus Memory Data
- Function Mode Data
- Present Data

The timing module signals STIM_LOAD and TSOUT4 along with the selected function mode control which one of the three data signals is enabled.

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Table 4-2 illustrates how STIM_LOAD and TSOUT4 affects the output registers.

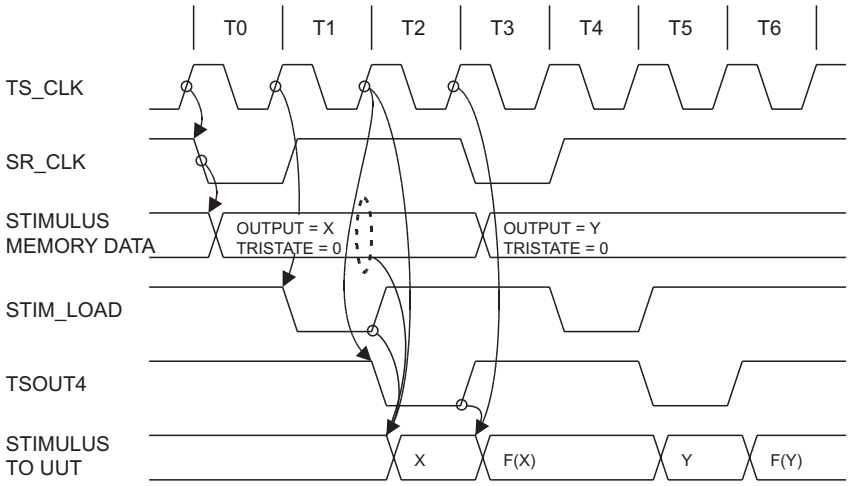
STIM LOAD	TSOUT4	Mode	Output Register Input							
			D7	D6	D5	D4	D3	D2	D1	D0
FALSE (high)	FALSE (high)	X	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
TRUE (low)	X	X	MEMORY D7	MEMORY D6	MEMORY D5	MEMORY D4	MEMORY D3	MEMORY D2	MEMORY D1	MEMORY D0
FALSE	TRUE (low)	HOLD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
FALSE	TRUE	RTO	1	1	1	1	1	1	1	1
FALSE	TRUE	RTZ	0	0	0	0	0	0	0	0
FALSE	TRUE	RTC	$\overline{RD7}$	$\overline{RD6}$	$\overline{RD5}$	$\overline{RD4}$	$\overline{RD3}$	$\overline{RD2}$	$\overline{RD1}$	$\overline{RD0}$
FALSE	TRUE	INCR1	If CARRY IN is true then the RD7-RD0 are incremented by the selected amount, i.e., 1, 2, 4 or 8. CARRY OUT Generation: INCR1 CARRY IN and RD7-RD0 all high. INCR2 CARRY IN and RD7-RD1 all high. INCR4 CARRY IN and RD7-RD2 all high. INCR8 CARRY IN and RD7-RD3 all high.							
FALSE	TRUE	INCR2								
FALSE	TRUE	INCR4								
FALSE	TRUE	INCR8								
FALSE	TRUE	SERIAL	SERIAL IN	RD7	RD6	RD5	RD4	RD3	RD2	RD1
FALSE	TRUE	MULTI-PLEX	X	X	X	X	RD7	RD6	RD5	RD4

Dn = Register Input Bit n RDn = Register Output Bit n MEMORY Dn = OUTPUT or TRISTATE data

Table 4-2 TSOUT4/STIM_LOAD Register Control

4.1.5 Output Mode Timing

The timing is defined by the FMA bus and three control signals, TS_CLK, STIM_LOAD and TSOUT4. Figure 4-4 shows output signal timing.



X, Y = Data from output memory, F(X), F(Y) = Function mode data.

Figure 4-4 Output Signal Timing

The stimulus data to the UUT is generated from the OUTPUT and TRISTATE memory. The SR_CLK signal increments the address (FMA) to the OUTPUT and TRISTATE memories. The output registers between the stimulus memory and the output drivers are clocked by the rising edge of TS_CLK. TS_CLK is selected from either an internal clock or from one of the two external clocks, EXCLK1 or EXCLK2.

The data to the output registers are enabled by two control signals, STIM_LOAD and TSOUT4. When both of these signals are not true (”high” state), the output registers maintain their present value. When the STIM_LOAD signal is true (”low” state) the data from the stimulus memories is routed to the output registers and will be loaded on the next rising edge of TS_CLK. When the TSOUT4 signal is true (”low”

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state), the function mode data is routed to the output registers and will be loaded on the next rising edge of TS_CLK.

Output timing restrictions:

1. STIM_LOAD cannot be in the same cell as SR_CLK if the Timing Set clock is greater than 30 MHz.

4.1.6 Output Mode Timing Examples

The following sections illustrates the timing signal requirements for the SR114 data format, algorithmic increment, serial and multiplex output modes.

4.1.6.1 Output Data Format Timing

A data format function timing is illustrated in figure 4-5 below using RTC as an example.

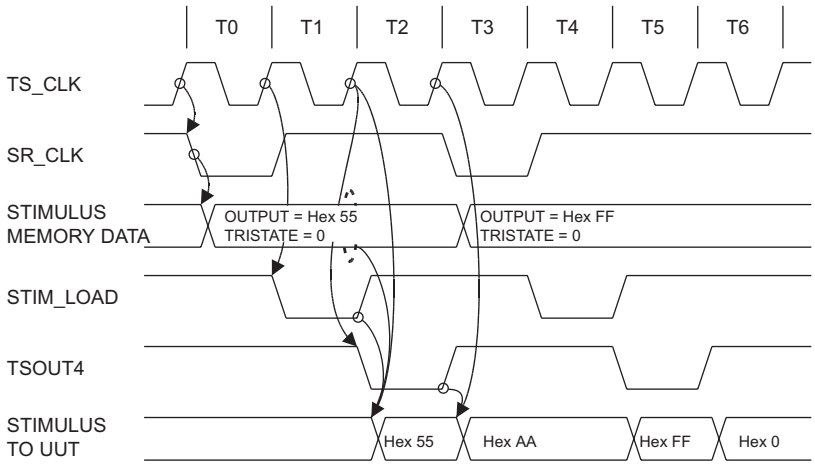


Figure 4-5 RTC Timing Example

The following table 4-3 describes the timing sequence of figure 4-5.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (Hex 55 output, 0 tristate in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (Hex 55 in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For RTC, output data Hex 55 becomes Hex AA. Tristate data does not change.
T3	TS_CLK	Rising Edge	Loads function data into the output registers (Hex AA in example).
	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (Hex FF output, 0 tristate in example).
T4	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T5	TS_CLK	Rising Edge	Loads stimulus data into the output registers (Hex FF output in example)..
	TSOUT4	True (low)	Function mode data routed to the output registers. For RTC, output data Hex FF becomes 0. Tristate data does not change.
T6	TS_CLK	Rising Edge	Loads function data into the output registers (0 in example)..

Table 4-3 Output Data Format Timing Description

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4.1.6.2 Output Algorithmic Increment Function

The timing for all the algorithmic increment functions operate in a similar fashion. Figure 4-6 illustrates the channel mode INCREMENT2 timing.

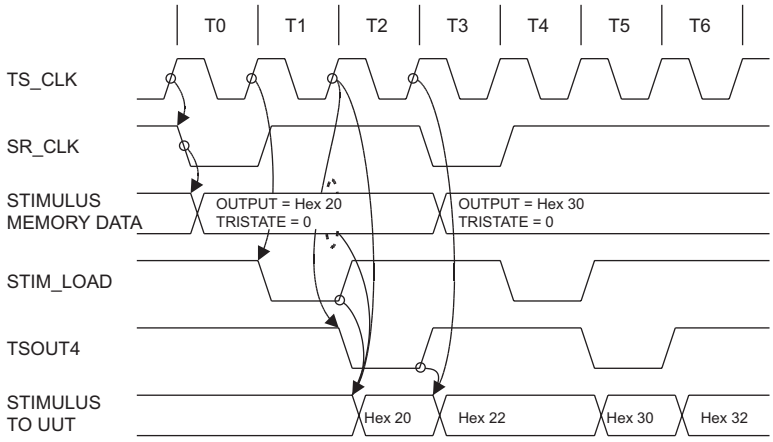


Figure 4-6 INCREMENT2 Timing Example

The following table 4-4 describes the timing sequence of figure 4-6.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (Hex 20 output, 0 tristate in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (Hex 20 in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For INCR2, output data Hex 20 becomes Hex 22. Tristate data does not change.
T3	TS_CLK	Rising Edge	Loads function data into the output registers (Hex 22 in example).
	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (Hex 30 output, 0 tristate in example).
T4	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T5	TS_CLK	Rising Edge	Loads stimulus data into the output registers (Hex 30 in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For INCR2, output data Hex 20 becomes Hex 22. Tristate data does not change.
T6	TS_CLK	Rising Edge	Loads function data into the output registers (Hex 32 in example).

Table 4-4 Output Algorithmic Timing Description

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4.1.6.3 Output Serial Shift Function

The serial shift timing is illustrated in figure 4-7 below.

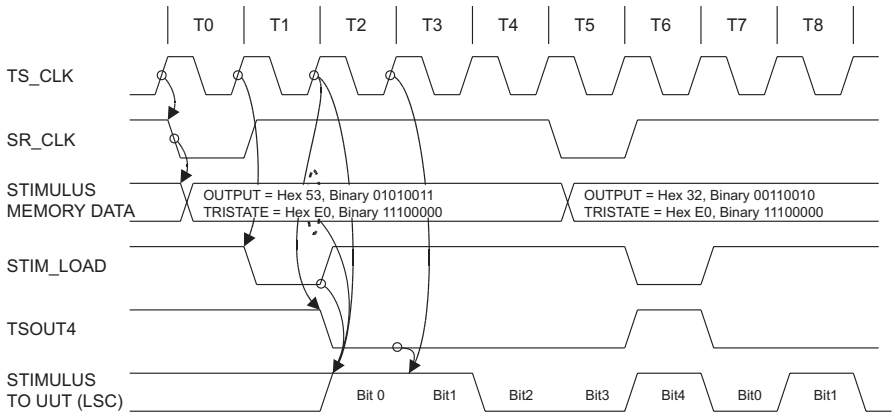


Figure 4-7 Serial Shift Timing

The following table 4-5 describes the timing sequence of figure 4-7.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (Hex 53 output, E0 tristate in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (LSC high in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For SER, output data Hex 53 becomes Hex 29. Tristate data Hex E0 becomes Hex 70.
T3	TS_CLK	Rising Edge	Loads function data into the output registers (LSC high in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For SER output data Hex 29 becomes Hex 14. Tristate data Hex 70 becomes Hex 38.
T4	TS_CLK	Rising Edge	Loads function data into the output registers (LSC low in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For SER output data Hex 14 becomes Hex A. Tristate data Hex 38 becomes Hex 1C.
T5	TS_CLK	Rising Edge	Loads function data into the output registers (LSC low in example).
	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (Hex 32 output, E0 tristate in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For SER output data Hex A becomes Hex 5. Tristate data Hex 1C becomes Hex E.
T6	TS_CLK	Rising Edge	Loads function data into the output registers (LSC high in example).
	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T7	TS_CLK	Rising Edge	Loads stimulus data into the output registers (LSC low in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For SER, output data Hex 32 becomes Hex 19. Tristate data Hex E0 becomes Hex 70.
T8	TS_CLK	Rising Edge	Loads function data into the output registers (LSC high in example).

Table 4-5 Output Serial Shift Timing Description

NOTE: The serial shift example above has been programmed to output only five bits from each stimulus word instead of all eight.

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4.1.6.4 Output Multiplex Shift Function

Figure 4-8 depicts the multiplex shift mode timing.

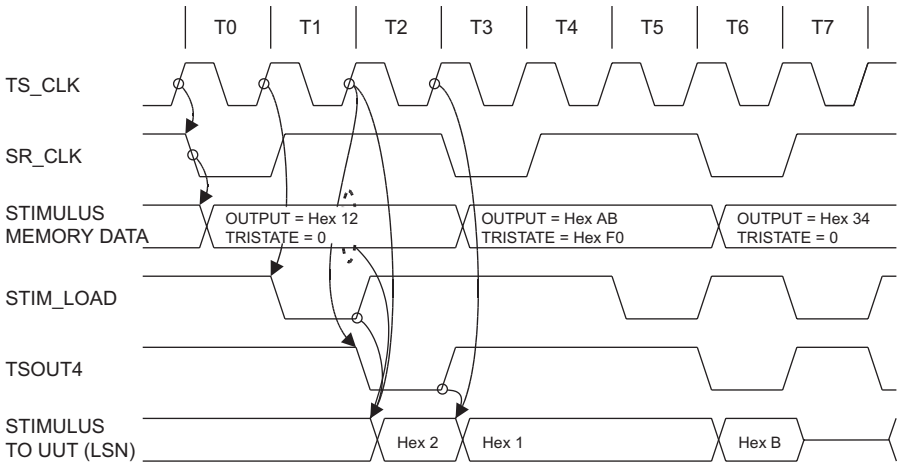


Figure 4-8 Multiplex Shift Timing

The following table 4-6 describes the timing sequence of figure 4-8.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (Hex 12 output, 0 tristate in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (Hex 2 in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For MULT, output data Hex 12 becomes Hex 1. Tristate data remains 0.
T3	TS_CLK	Rising Edge	Loads function data into the output registers (Hex 1 in example).
	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (Hex AB output, F0 tristate in example).
T4	TS_CLK	Rising Edge	Loads present data into the output registers (Hex 1 in example).
T5	TS_CLK	Rising Edge	Loads present data into the output registers (Hex 1 in example).
	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T6	TS_CLK	Rising Edge	Loads stimulus data into the output registers (Hex B in example).
	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (Hex 34 output, 0 tristate in example).
	TSOUT4	True (low)	Function mode data routed to the output registers. For MULT output data Hex AB becomes Hex A. Tristate data Hex F0 becomes Hex F.
T7	TS_CLK	Rising Edge	Loads function data into the output registers (Hi-Z in example).
	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.

Table 4-6 Output Multiplex Timing Description

NOTE: In the above multiplex example, the UUT data during T4 and T5 holds its present value (hex 1) because both control signals (TSOUT4 and STIM_LOAD) are false (high). Refer to table 4-2.

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4.2 Response Logic

Figure 4-9 shows the response logic block diagram.

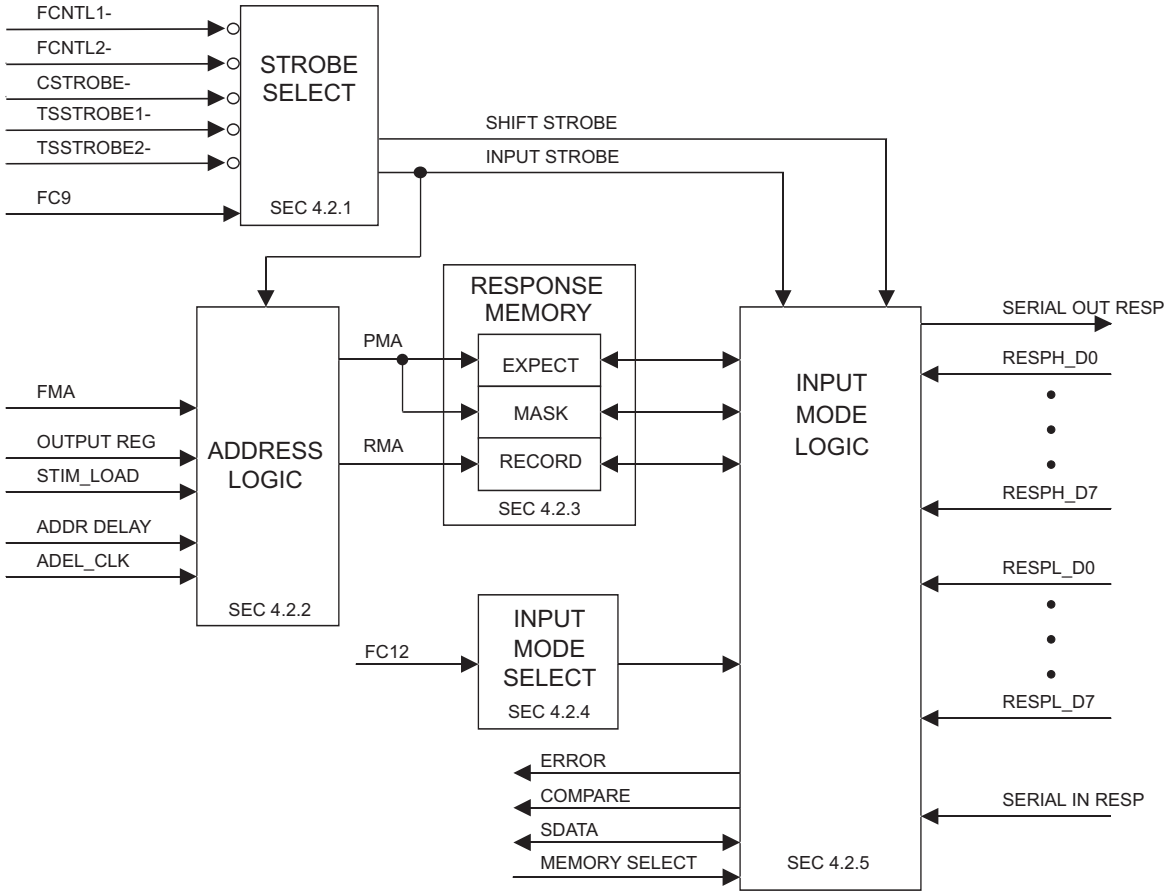


Figure 4-9 Response Logic Block Diagram

The following list describes the functional blocks of figure 4-9.

1.	STROBE SELECT	Used to select the input strobe as well as the shift strobe.
2.	ADDRESS LOGIC	A series of registers used to delay the FMA in order to generate a synchronous address to the response memories.
3.	EXPECT MEMORY	128K by 8 memory allows the user specify an expected result for each response bit for real time compare.
4.	MASK MEMORY	128K by 8 memory allows the user to mask on or off any response bit for real time - compare.
5.	RECORD MEMORY	128K by 8 memory stores the result of the real time compare for every INPUT STROBE signal.
6.	INPUT MODE SELECT	Allows the operator to program the channel mode function.
7.	INPUT MODE LOGIC	Hardware that performs the selected function mode and real time compare.

The following list describes the signals shown in figure 4-9 above.

1.	FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
2.	FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
3.	CSTROBE-	Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data.
4.	TSSTROBE1	Timing Set Strobe 1 from the timing module.
5.	TSSTROBE2	Timing Set Strobe 2 from the timing module.
6.	FC9	Control signals used to program the strobe/group enable selector. Refer to appendix B.

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7.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
8.	OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
9.	STIM_LOAD	Timing module signal that latches the stimulus address bus (FMA) when the output register mode is enabled.
10.	ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
11.	ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
12.	PMA	Present Memory Address. Delayed FMA bus. Refer to section 4.2.2
13.	RMA	Record Memory Address. Delayed PMA bus. Refer to section 4.2.2
14.	FC12	Control signals used to program the channel function mode. Refer to appendix B.
15.	SHIFT STROBE	This signal is used to record intermediate data from the UUT for the shift function modes (serial or multiplex).
16.	INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
17.	COMPARE	Unregistered signal from the response comparator that indicates that the current response data matches the expect and mask data.
18.	ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
19.	SDATA	The selected data bus used to program and query the response memories.
20.	MEMORY SELECT	This signal allows the user to program or query the expect, mask or record memory. Two virtual memories can also be selected (error and response) that are derived from the data stored in the other three memories.
21.	SERIAL OUT RESP	Response data output signal to adjacent lower SR114, 8 channel group for SERIAL function mode.
22.	RESPH_D0-D7	Response high signals from the input receivers.
23.	RESPL_D0-D7	Response low signals from the input receivers.
24.	SERIAL IN RESP	Response data input signal from adjacent higher SR114, 8 channel group for SERIAL function mode.

4.2.1 Strobe Select

The strobe select allows the user to select the INPUT STROBE and the SHIFT STROBE signals.

The falling edge of INPUT STROBE causes the data from the input receivers to be compared to the data programmed in the EXPECT and MASK memories. The result of the comparison for each channel is then stored in the RECORD memory. Refer to section 4.2.3 for a description of the response memories.

The SHIFT STROBE is used for the Serial and Multiplex shift modes to record the intermediate data.

Table 4-7 below describes the input and shift strobe functions for the various channel modes.

Function Mode	Shift Strobe Action	Input Strobe Action
HOLD, RTO, RTC, RTZ	NA	Strobe in all eight input registers, then record the comparison results from all eight input register bits.
INCR1,2,4,8	NA	
Serial Shift	Strobe most significant channel (MSC) of the channel group into the MSB of the input register, then shift down by one.	Strobe MSC of the channel group into the MSB of the input register, then record the comparison results from all eight input register bits.
Multiplex Shift	Strobe least significant nibble (LSN) of the channel group into the LSN of the input register.	Strobe in LSN of the channel group into the MSN of the input register, then record the comparison results from all eight input register bits.

Table 4-7 Input/Shift Strobe Functions

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4.2.2 Address Logic

Figure 4-10 illustrates the SR114 address logic.

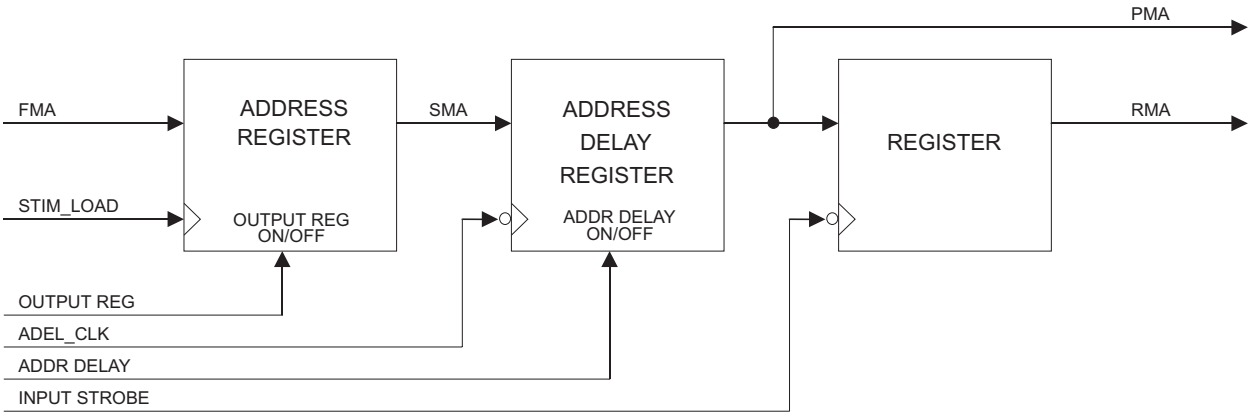


Figure 4-10 Input Address Logic Block Diagram

The following list describes the signals shown in figure 4-10 above.

1.	FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
2.	STIM_LOAD	Timing module signal that latches the stimulus address bus (FMA) when the output delay mode is enabled.
3.	OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
4.	ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
5.	ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
6.	INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
7.	SMA	Stimulus Memory Address. Delayed FMA bus.
8.	PMA	Present Memory Address. Delayed SMA bus.
9.	RMA	Record Memory Address. Registered PMA bus.

The address logic is used to delay the FMA bus to the PMA and RMA bus.

As shown in figure 4-10 above there are two register delay blocks. The combination of these two registers defines four input modes described in the following table 4-8.

Input Mode	Description	Required Timing Signals
Mode 1 (default)	Output register mode enabled and the input address delay mode disabled.	STIM_LOAD rising edge.
Mode 2	Both Output register mode and input address delay mode enabled	STIM_LOAD rising edge, ADEL_CLK falling edge.
Mode 3	Both output register mode and address delay mode disabled.	NA

Table 4-8 Addressing Mode Descriptions

These input modes can be used in stimulus/response applications to keep the stimulus data synchronized with the response data.

4.2.3 Response Memories

The response memories on the SR114 consist of three 128K x 16 bit static RAM's. The first two, EXPECT and MASK contain the data that is used by the input comparator. The third memory, RECORD, is used to store the results of the input comparator. Bit 0 of the EXPECT and MASK is compared with bit 0 of registered response data from the input receiver and the result is stored in bit 0 of the RECORD memory.

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The mask and expect memories are addressed by the PMA bus. The record memory is addressed by the registered PMA bus called the RMA bus.

From the contents of the expect, mask and record memory, two additional “virtual” memories are created, error and response.

Table 4-9 below illustrates the real time compare results of the mask and expect memories for each state of the response data (logic 0 and logic 1).

COMPARE FUNCTION	MASK MEMORY	EXPECT MEMORY	RESPONSE DATA	RECORD MEMORY	ERROR MEMORY	RESPONSE MEMORY
Test for < VIL	0	0	< VIL	0	0	0
			> VIL	1	1	1
Test for > VIH	0	1	< VIH	1	1	0
			> VIH	0	0	1
Mask off ERROR	1	0	< VIL	0	0	0
			> VIH	1	0	1
			> VIL and < VIH	1	0	1
Test for > VIL and < VIH	1	1	< VIL	1	1	0
			> VIH	1	1	0
			> VIL and < VIH	0	0	1

Table 4-9 Expect, Mask, Record, Error and Response Memory Description

The response memory is the logical “exclusive or” of the record and expect memories.

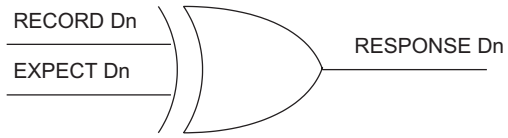


Figure 4-11 Response Memory Logic

The error memory is generated by the logical “and’ of the record memory with the logical “or” of the expect and the complimented mask memory.

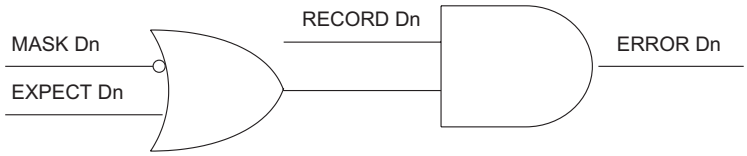


Figure 4-12 Error Memory Logic

4.2.4 Input Mode Logic

The mode of operation for the response logic is the same as the stimulus logic. The data formatting and algorithmic increment modes all record data in parallel. The serial shift function records data only from the most significant channel. The multiplex shift function records data from the four least significant nibble of the channel group. Refer to section 4.1.3.

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4.2.5 Input Mode Logic

Figure 4-13 below is the block diagram for the input mode logic.

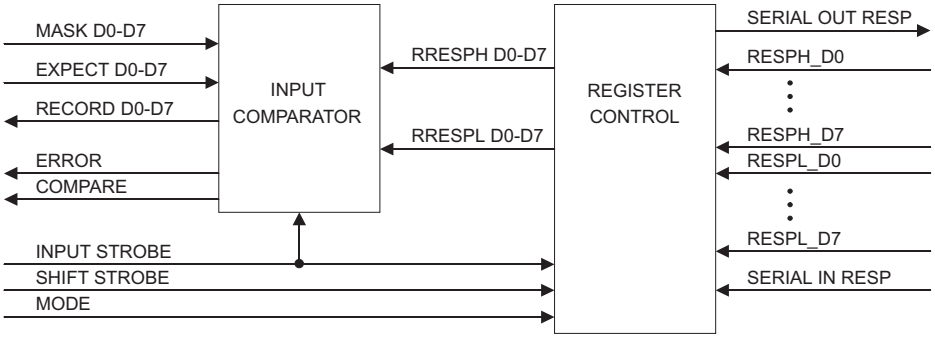


Figure 4-13 Input Mode Logic

The following list describes the functional blocks of figure 4-13.

1.	INPUT COMPARATOR	On the falling edge of the INPUT STROBE signal this logic will compare the registered response data with the mask and expect memory data.
2.	REGISTER CONTROL	This logic routes the response data from the receivers to the appropriate register based on the selected function mode and registers the data.

The following list describes the signals shown in figure 4-13 above.

1.	MASK D0-D7	Data from the mask memory.
2.	EXPECT D0-D7	Data from the expect memory.
3.	RECORD D0-D7	Data to the record memory.
4.	ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
5.	COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
6.	INPUT STROBE	This signal registers the input data, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
7.	SHIFT STROBE	This signal is used to record intermediate data from the UUT for the shift function modes.
8.	RRESPH D0-D7	Registered response high data.
9.	RRESPL D0-D7	Registered response low data.
10.	SERIAL OUT RESP	Response data output signal to adjacent lower SR114, 8 channel group for SERIAL function mode.
11.	RESPH_D0-D7	Response low signals from the input receivers.
12.	RESPL_D0-D7	Response high signals from the input receivers.
13.	SERIAL IN RESP	Response data input signal from adjacent higher SR114, 8 channel group for SERIAL function mode.
14.	MODE	Selected function mode from Input Mode Select logic.

4.2.5.1 Input Comparator

The input comparator generates the data for the record memory as well as the ERROR and COMPARE signals.

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Table 4-11 below illustrates the input comparator results for the ERROR and COMPARE signal.

COMPARE FUNCTION	MASK DATA	EXPECT DATA	REGISTERED RESPONSE	ERROR	COMPARE
Test for < VIL	0	0	< VIL	0	1
			> VIH	1	0
			> VIL and < VIH	1	0
Test for > VIH	0	1	< VIL	1	0
			> VIH	0	1
			> VIL and < VIH	1	0
Mask off ERROR	1	0	< VIL	0	1
			> VIH	0	1
			> VIL and < VIH	0	1
Test for > VIL and < VOH	1	1	< VIL	1	0
			> VIH	1	0
			> VIL and < VIH	0	1

Table 4-11 Input Comparator Results

The input comparator generates the data that will be recorded in the record memory. It also generates the real time ERROR and COMPARE signals that can be tested by the timing modules.

The error signal for each channel is registered with the falling edge of the INPUT STROBE signal. The ERROR signal for the module is the “OR” of the error signals of the individual channels. Note from table 4-11 that a channel error signal is not generated if the compare is masked off.

The compare signal for each channel is not registered. The COMPARE signal for the module is the “AND” of the compare signals from the individual channels.

CAUTION

Since COMPARE is not registered, logic switching noise may produce an inadvertent compare of sufficient duration to be recognized by the timing module as a valid compare. Also in TSA/TSB linked mode, the response data must be synchronized with CLOCKA in order to prevent TSA/TSB from becoming unsynchronized.

4.2.5.2 Input Register Control

The input register control logic is used to register the response data from the input receivers.

The falling edge of INPUT STROBE and SHIFT STROBE are used to control the data.

Table 4-10 shows how INPUT STROBE and SHIFT STROBE affect the input registers.

SHIFT STROBE	INPUT STROBE	MODE	Input Register Response Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Falling Edge	FALSE (high)	SERIAL	RESP_D7	RD7	RD6	RD5	RD4	RD3	RD2	RD1
FALSE (high)	Falling Edge		RESP_D7	RD7	RD6	RD5	RD4	RD3	RD2	RD1
Falling Edge	FALSE (high)	MULTI-PLEX	X	X	X	X	RESP_D3	RESP_D2	RESP_D1	RESP_D0
FALSE (high)	Falling Edge		RESP_D3	RESP_D2	RESP_D1	RESP_D0	RD3	RD2	RD1	RD0
Falling Edge	FALSE (high)	DATA FORMAT ALGO INCR	X	X	X	X	X	X	X	X
FALSE (high)	Falling Edge		RESP_D7	RESP_D6	RESP_D5	RESP_D4	RESP_D3	RESP_D2	RESP_D1	RESP_D0

Dn = Register Input Bit n RDn = Register Output Bit n RESP_Dn = RESPH_Dn or RESPL_Dn

Table 4-10 Input Register Control Signals

In order to record the UUT response data in the same memory address that generated the UUT stimulus data, the user must do two things:

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1. Determine where the input strobe signal needs to be positioned to accommodate the UUT delay.
2. Select an input addressing mode that will retrieve the Expect/Mask data with respect to his input strobe.

The input strobe must be placed far enough over from the cell which generated the stimulus data to allow for the UUT delay (D), as well as the SR114's internal input and output delay. The number of cells (N) required to accommodate these delays for the SR114 are shown in the following formula:

$$N=(D+27)F/1000$$

Where D = users UUT delay in ns

F = SR192 clock rate in MHz

If the response data can be recorded within the same cycle and, therefore before the next stimulus word, then input mode 1 or 3 should be selected.

If the response data has to be recorded during the next stimulus word, then the expect and mask data must be delayed using addressing mode 2 or 4.

If the response data has to be recorded after the next stimulus word, then the expect and mask data must be pipelined (i.e. The response data generated by stimulus word at address "n" will be recorded in address "n + 1" or later).

4.2.6 Input Mode Timing

The following sections describe the timing of the four input modes described in section 4.2.2.

4.2.6.1 Input Mode 1 Timing

In this mode the field memory address bus (FMA) is registered by the rising edge of the STIM_LOAD signal before addressing the response memories (MASK, EXPECT and RECORD).

This is the default addressing mode and can be used in most stimulus/response applications where the response to a stimulus word can be strobed prior to the output of the next stimulus word.

The following timing restrictions apply to addressing mode 1:

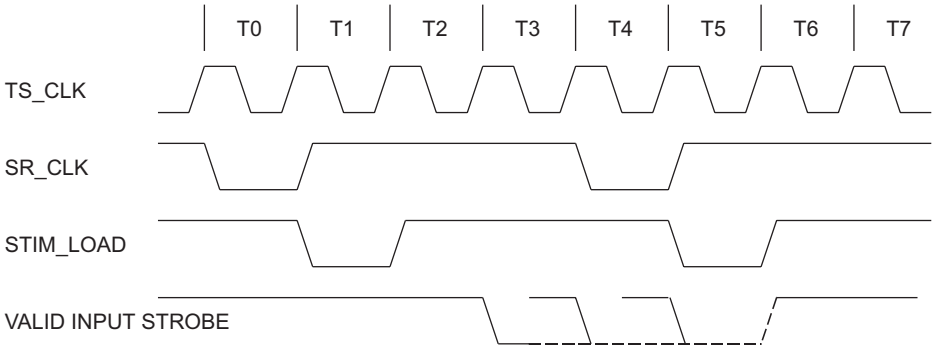


Figure 4-14 Input Mode 1 Timing Restrictions

Timing Set restrictions:

1. Do not have the rising edge of STIM_LOAD at the same time as the falling edge of SR_CLK.
2. Do not have the falling edge of INPUT STROBE at the same time as the rising edge of STIM_LOAD.

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Figure 4-15 below illustrates mode 1 input timing.

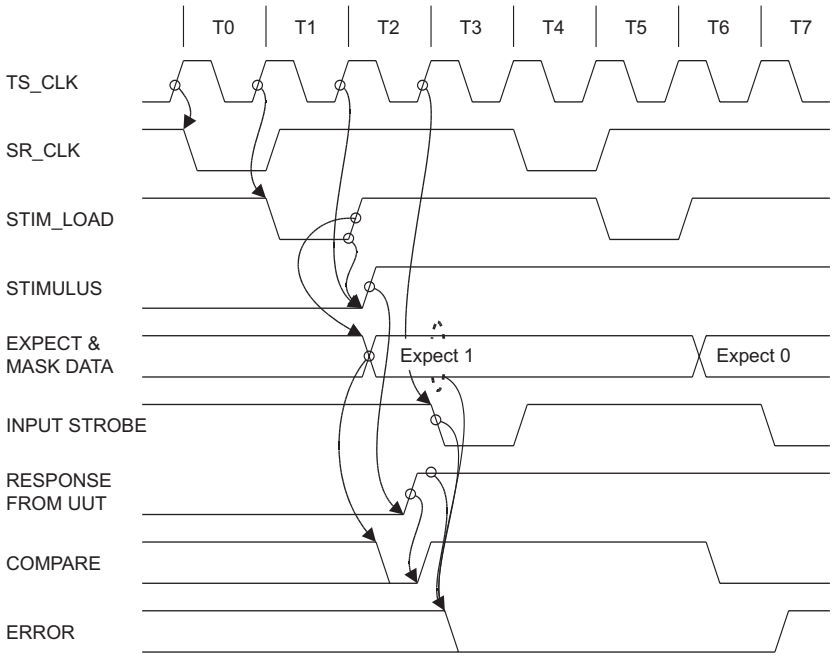


Figure 4-15 Input Mode 1 Timing

The following table 4-12 describes the timing sequence in figure 4-15.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory.
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	STIM_LOAD	Rising Edge	Retrieves expect and mask data from memory (Expect 1 in example).
T3	INPUT STROBE	Falling Edge	Compare the UUT response data with the expect and mask data then store results into the record memory.
T4	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
T5	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T6	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	STIM_LOAD	Rising Edge	Retrieves new expect and mask data from memory (Expect 0 in example).
T7	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.

Table 4-12 Input Mode 1 Timing Description

4.2.6.2 Input Mode 2 Timing

In this mode the field memory address bus (FMA) is registered first by both the rising edge of STIM_LOAD and then by the falling edge of ADEL_CLK before addressing the response memories (MASK, EXPECT and RECORD).

This is used in applications where the response to a stimulus word cannot be strobed prior to the end of the stimulus word cycle.

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The following timing restrictions apply to input mode 2:

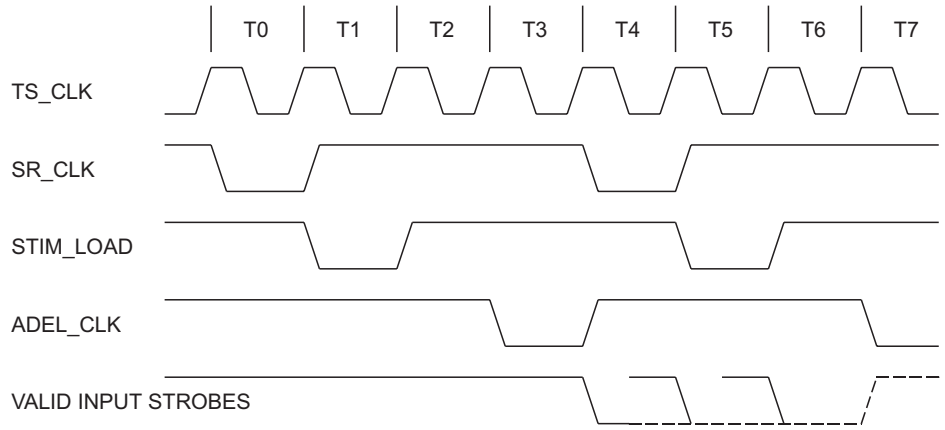


Figure 4-17 Input Mode 2 Timing Restrictions

Timing Set restrictions:

1. Do not have the rising edge of STIM_LOAD at the same time as the falling edge of SR_CLK.
2. Do not have the falling edge of INPUT STROBE at the same time as the falling edge of ADEL_CLK.

Figure 4-16 below illustrates the input mode 2 timing.

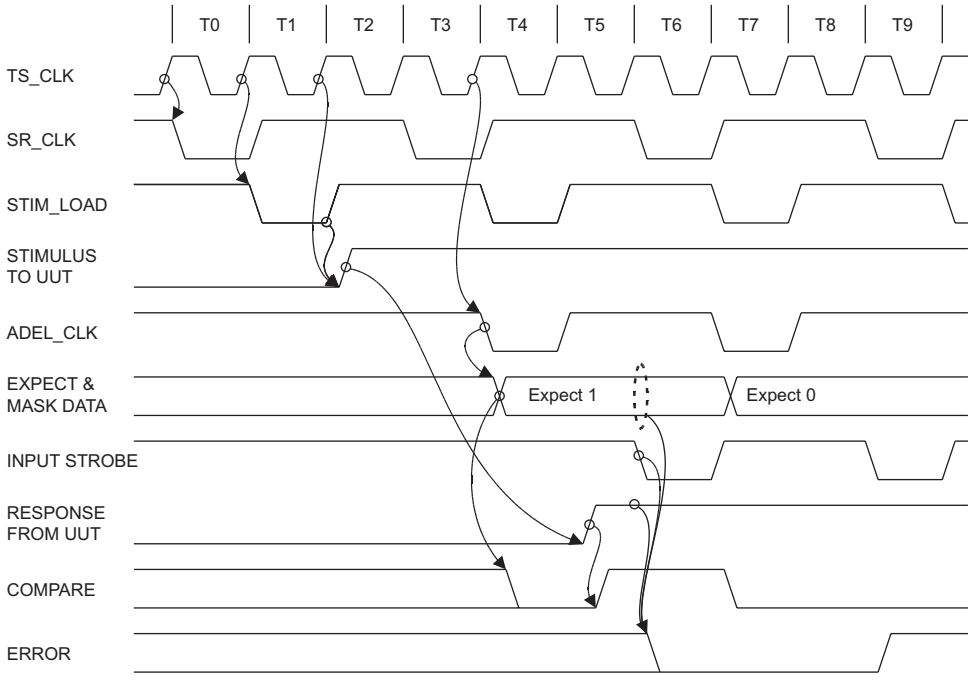


Figure 4-16 Input Mode 2 Timing

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The following table describes the timing sequence in figure 4-16

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory.
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	STIM_LOAD	Rising Edge	Stimulus Memory Address (SMA) registered, see figure 4-10.
T3	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
T4	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
	ADEL_CLK	Falling Edge	Retrieves expect and mask data from memory (expect 1 in example).
T5	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	STIM_LOAD	Rising Edge	Stimulus Memory Address (SMA) registered, see figure 4-10.
T6	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.
T7	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
	ADEL_CLK	Falling Edge	Retrieves new expect and mask data from memory (expect 0 in example).
T8	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	STIM_LOAD	Rising Edge	Stimulus Memory Address (SMA) registered, see figure 4-10.
T9	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.

Table 4-13 Input Mode 2 Timing Description

4.2.6.3 Input Mode 3 Timing

In this mode the field memory address bus (FMA) is passed through directly to the response memories (MASK, EXPECT and RECORD).

This is used in applications where the response to a stimulus word can be strobed prior to the end of the stimulus word cycle.

The following timing restrictions apply to input mode 3:

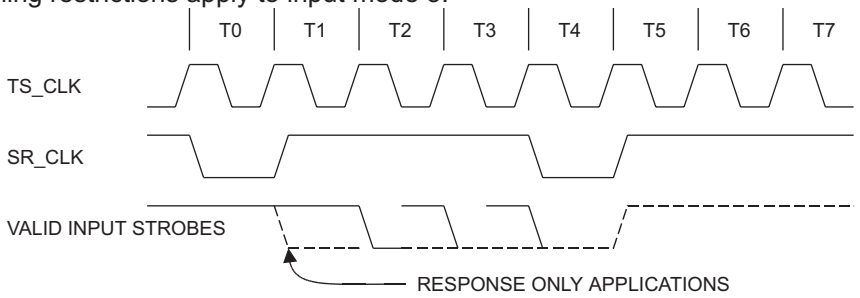


Figure 4-18 Input Mode 3 Timing Restrictions

Timing Set restrictions:

1. The INPUT STROBE must occur at least two cells later than STIM_LOAD (in stimulus response applications).

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Figure 4-19 below illustrates the input mode 3 timing.

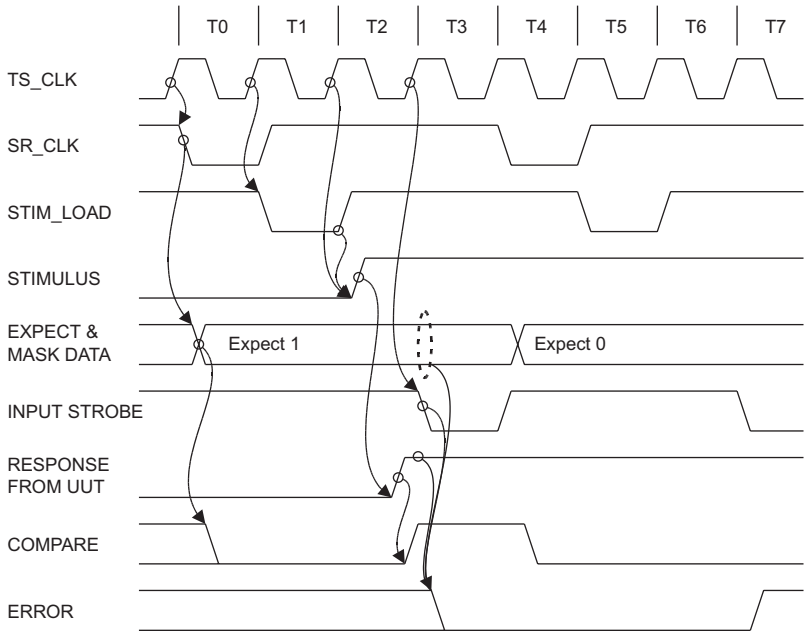


Figure 4-19 Input Mode 3 Timing

The following table describes the timing sequence in figure 4-19.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus, expect and mask data from memory (expect 1 in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
T3	INPUT STROBE	Falling Edge	Compare the response input with the expect and mask data then store results into the record memory.
T4	SR_CLK	Falling Edge	Retrieves stimulus, expect and mask data from memory (expect 0 in example).
T5	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers (a logic one in the example).
T6	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
T7	INPUT STROBE	Falling Edge	Compare the response input with the expect and mask data then store results into the record memory.

Table 4-14 Input Mode 3 Timing Description

4.2.6.4 Input Mode 4 Timing

In this mode the bus that addresses the stimulus memory (FMA) is registered by the falling edge of the ADEL_CLK signal before addressing the response memories (MASK, EXPECT and RECORD).

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The following timing restrictions apply to input mode 4:

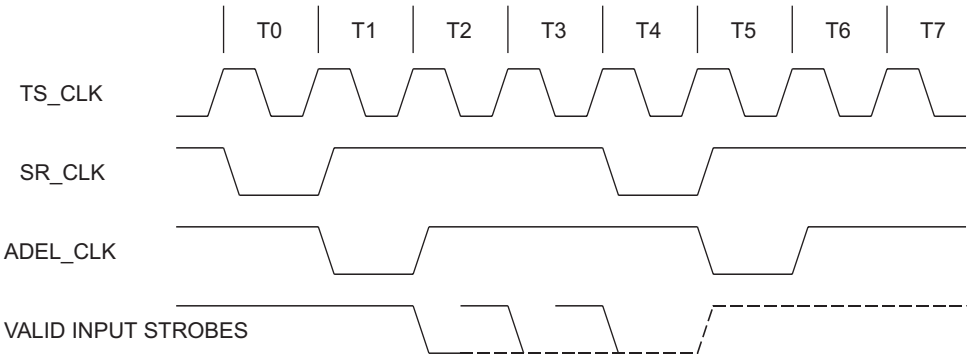


Figure 4-21 Input Mode 4 Timing Restrictions

Timing Set restrictions:

1. Do not have the falling edge of INPUT STROBE at the same time as the falling edge of ADEL_CLK.
2. The INPUT STROBE must occur at least one cell later than STIM_LOAD (in stimulus response applications).

Figure 4-20 below illustrates the input mode 4 timing.

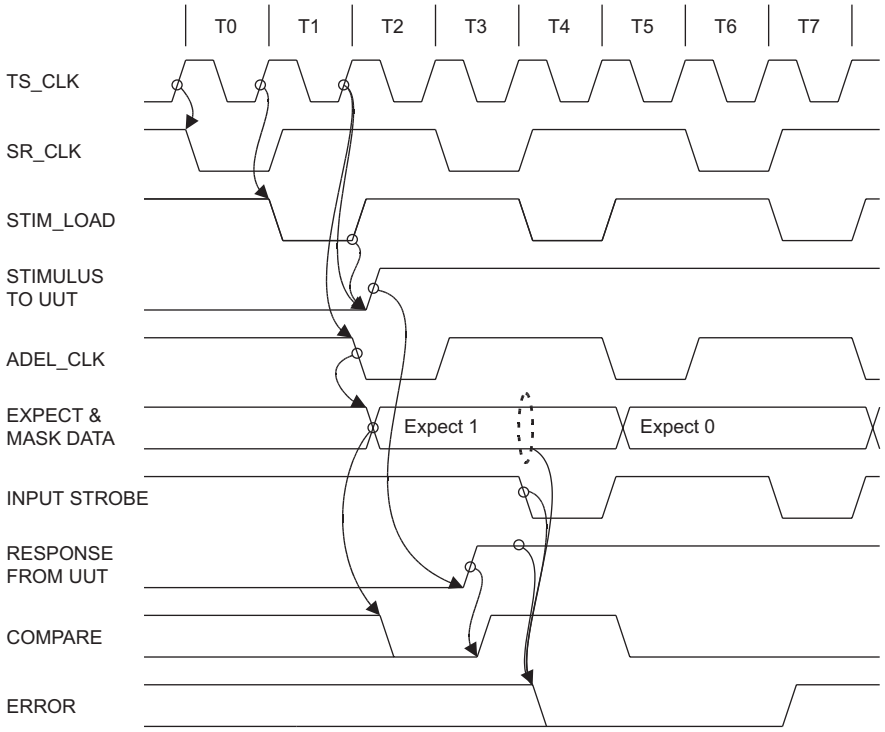


Figure 4-20 Input Mode 4 Timing

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The following table describes the timing sequence in figure 4-20

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory.
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	ADEL_CLK	Rising Edge	Retrieves expect and mask data from memory (expect 1 in example).
T3	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
T4	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.
T5	TS_CLK	Rising Edge	Loads stimulus data into the output registers (a logic one in the example).
	ADEL_CLK	Falling Edge	Retrieves expect and mask data from memory (expect 0 in example).
T6	SR_CLK	Falling Edge	Retrieves new stimulus data from memory.
T7	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
	INPUT STROBE	Falling Edge	Compare the response data with the expect and mask data then store results into the record memory.

Table 4-15 Input Mode 4 Timing Description

4.2.7 Input Mode Timing Examples

The following sections illustrates the timing signal requirements for the SR114 serial and multiplex input modes.

4.2.7.1 Input Serial Shift Timing

The serial shift mode allows the operator to input UUT response data as a serial stream. The serial input comes from the most significant channel and is shifted towards the least significant memory bit.

The following example uses input mode 1 timing.

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Figure 4-22 below illustrates the serial mode response timing.

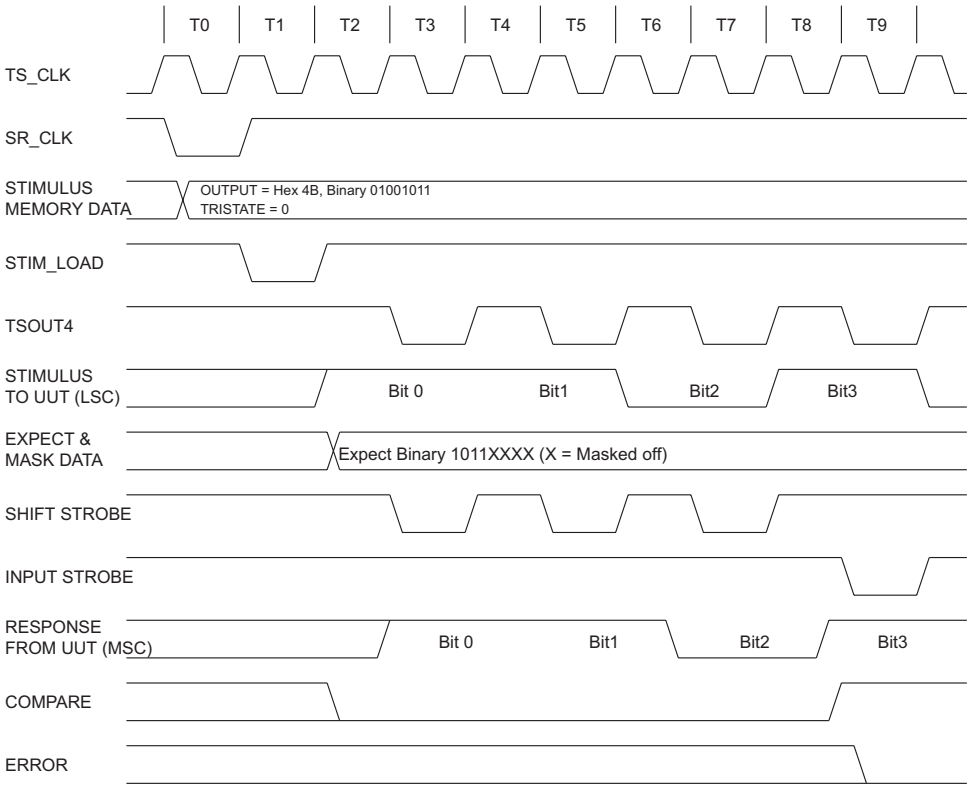


Figure 4-22 Serial Mode Input Timing Example

The following table describes the timing sequence in figure 4-22.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (Hex 4B output, 0 tristate in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (LSC high in example).
	STIM_LOAD	Rising Edge	Retrieves expect and mask data from memory (Expect binary 1011XXXX in example).
T3	TSOUT4	True (low)	Function mode data routed to the output registers, SER (Hex 4B) = Hex 25.
	SHIFT STROBE	Falling Edge	Strobe in MSC (high in example) and shift. Input reg = X1XXXXXX
T4	TS_CLK	Rising Edge	Loads function data into the output registers (LSC high in example).
T5	TSOUT4	TRUE (low)	Function mode data routed to the output registers, SER (Hex 25) = Hex 12.
	SHIFT STROBE	Falling Edge	Strobes in MSC (high in example) and shift. Input reg = X11XXXXX
T6	TS_CLK	Rising Edge	Loads function data into the stimulus registers (LSC low in example).
T7	TSOUT4	True (low)	Function mode data routed to the output registers, SER (Hex 12) = Hex 9.
	SHIFT STROBE	Falling Edge	Strobes in MSC (low in example) and shift. Input reg = X011XXXX
T8	TS_CLK	True (low)	Loads function data into the output registers (LSC high in example).
T9	INPUT STROBE	Falling Edge	Strobes MSC (high in example) . Input reg = 1011XXXX. Compares the input register data with the expect and mask data then store the results into the record memory.

Table 4-16 Serial Mode Input Timing Description

4.2.7.2 Input Multiplex Shift Timing

The multiplex shift mode allows the operator to input UUT response data as a multiplex stream. The multiplexed input comes from the four least significant channels. The shift strobe temporarily stores the

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lower nibble of data into the “shift” register. The input strobe stores the input data into the upper nibble of the input register and appends the lower nibble of data which was temporarily stored in the “shift” register.

The following example uses input mode 1 timing.

Figure 4-23 illustrates the multiplex mode response timing.

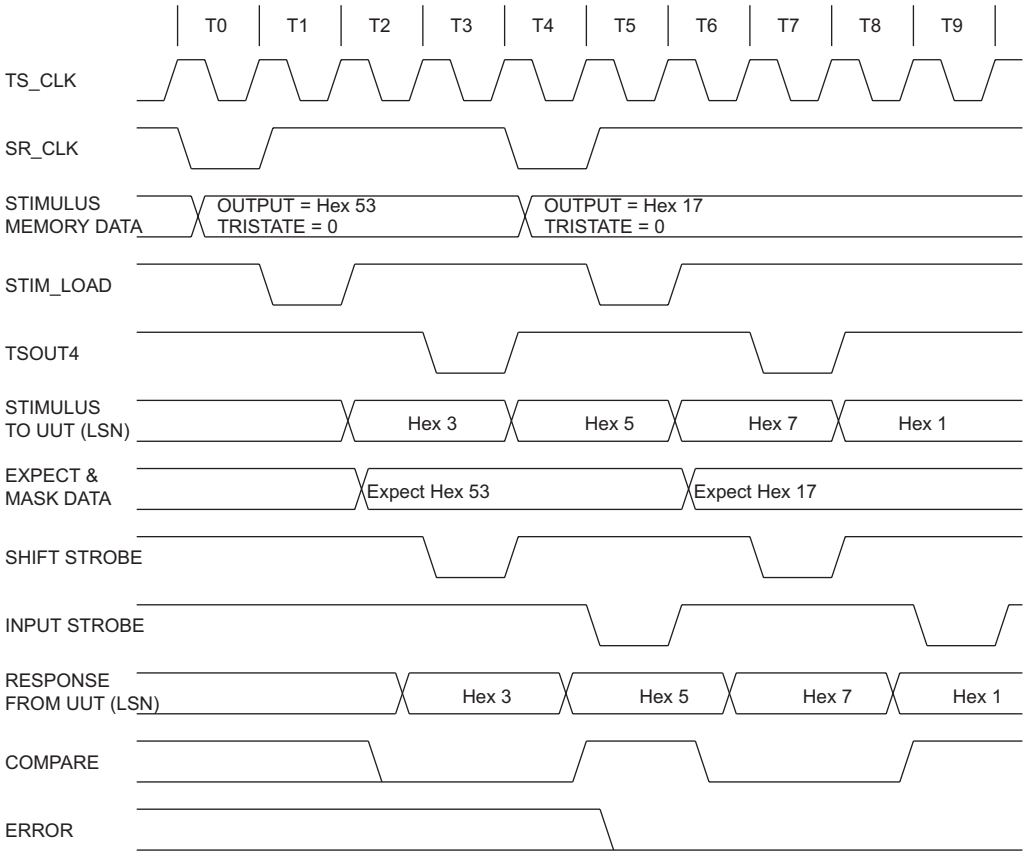


Figure 4-23 Multiplex Mode Input Timing Example

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Table 4-17 describes the timing sequence in figure 4-23.

Time	Signal	Condition	Action
T0	SR_CLK	Falling Edge	Retrieves stimulus data from memory (Hex 53 output, 0 tristate in example).
T1	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
T2	TS_CLK	Rising Edge	Loads stimulus data into the output registers (LSN Hex 3 in example).
T3	TSOUT4	True (low)	Function mode data routed to the output registers, MULT(hex53) = Hex 5.
	SHIFT STROBE	Falling Edge	Strobes in LSN (Hex 3 in example). Input reg = X3
T4	TX_CLK	Rising Edge	Loads function data into the output register (LSN Hex 5 in example).
	SR_CLK	Falling Edge	Retrieves new stimulus data from memory (Hex 17 output, 0 tristate in example).
T5	STIM_LOAD	True (low)	Stimulus memory data routed to the output registers.
	INPUT STROBE	Falling Edge	Strobes in LSN (Hex 5 in example). Input reg = Hex 53. Compare the response data with the expect and mask data then store it into record memory.
T6	TS_CLK	Rising Edge	Loads stimulus data into the output registers (LSN Hex 7 in example).
T7	TSOUT4	True (low)	Function mode data routed to the output registers, MULT(Hex17) = Hex 1.
	SHIFT STROBE	Falling Edge	Strobes in LSN Hex 7 in example). Input reg = X7.
T8	TX_CLK	True (low)	Loads function data into the output registers (Hex 1 in example).
T9	INPUT STROBE	Falling Edge	Strobes in LSN (Hex 1 in example). Input reg = Hex 17. Compare the response data with the expect and mask data then store results into the record memory.

Table 4-17 Multiplex Mode Input Timing Description

4.3 Driver/Receiver Logic Description

Figure 4-24 below illustrates the SR114's driver/receiver logic.

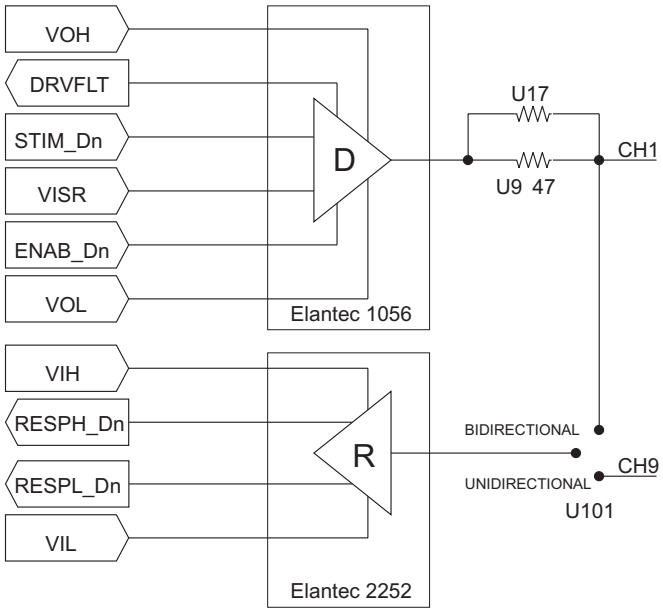


Figure 4-24 Driver/Receiver Configuration

4.3.1 Short Circuit Protection

Each driver incorporates a circuit which monitors excessive current. When sustained currents greater than 60mA are detected, the protection circuit will latch a power down signal to all 8 drivers. The front panel "OVERDRIVE" LED will illuminate and the SR192 CPU will be triggered. The power down signal is reset prior to the run sequence command to the SR192.

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4.3.2 Output Slew Rate

The default output driver slew rate is approximately 0.70 V/ns. The slew rate can be programmed faster or slower by means of the VISR (Voltage Input Slew Rate) input. The VISR is sourced by either the SR110/SR210 module or the front panel, J9 connector.

On power-up, the VISR voltage for all drivers are set to 2.0 volts. The VISR can be set from 0 to 5 volts with higher voltages yielding faster slew rates, see table 4-18 below. Since the cables, test fixture and UUT can affect the slew rate, it is recommended that the user place a scope (200 MHz bandwidth minimum) on the output signals and program VISR for the desired slew rate.

VISR	Driver Slew Rate (20% to 80% no load)	Notes
5V	1.25V/ns	2,3
4V	1.10V/ns	2,3
3V	0.83V/ns	2,3
2V (default)	0.54V/ns	3
1V	0.24V/ns	3
0.5V	0.10V/ns	1,3

Note 1: A VISR voltage of less than 0.5 volt may turn off the drivers.

Note 2: As the VISR voltage increases above 2 volts, the required current for V- and V+ will increase. The current for V+ and V- for each SR114 module will increase by approximately 150 mA with VISR = 5 volts.

Note 3: Slew rate shown for a +/- 10V swing (it will decrease for smaller swings).

Table 4-18 Driver Slew Rate vs. VISR

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5 Memory Data Mapping

The following table 5-1 shows the memory data to front panel mapping.

Bi-Dir Bit	Uni-Dir Bit	DRA1	DRA3	DRA3	DRA4	DRA5	DRA6	DRB1	DRB2	DRB3	DRB4	DRB5	DRB6
0	0 stim	CH1	CH17	CH33	CH49	CH65	CH81	CH97	C113	CH129	CH145	CH161	CH177
1	1 stim	CH2	CH18	CH34	CH50	CH66	CH82	CH98	CH114	CH130	CH146	CH162	CH178
2	2 stim	CH3	CH19	CH35	CH51	CH67	CH83	CH99	CH115	CH131	CH147	CH163	CH179
3	3 stim	CH4	CH20	CH36	CH52	CH68	CH84	CH100	CH116	CH132	CH148	CH164	CH180
4	4 stim	CH5	CH21	CH37	CH53	CH69	CH85	CH101	CH117	CH133	CH149	CH165	CH181
5	5 stim	CH6	CH22	CH38	CH54	CH70	CH86	CH102	CH118	CH134	CH150	CH166	CH182
6	6 stim	CH7	CH23	CH39	CH55	CH71	CH87	CH103	CH119	CH135	CH151	CH167	CH183
7	7 stim	CH8	CH24	CH40	CH56	CH72	CH88	CH104	CH120	CH136	CH152	CH168	CH184
	0 resp	CH9	CH25	CH41	CH57	CH73	CH89	CH105	CH121	CH137	CH153	CH169	CH185
	1 resp	CH10	CH26	CH42	CH58	CH74	CH90	CH106	CH122	CH138	CH154	CH170	CH186
	2 resp	CH11	CH27	CH43	CH59	CH75	CH91	CH107	CH123	CH139	CH155	CH171	CH187
	3 resp	CH12	CH28	CH44	CH60	CH76	CH92	CH108	CH124	CH140	CH156	CH172	CH188
	4 resp	CH13	CH29	CH45	CH61	CH77	CH93	CH109	CH125	CH141	CH157	CH173	CH189
	5 resp	CH14	CH30	CH46	CH62	CH78	CH94	CH110	CH126	CH142	CH158	CH174	CH190
	6 resp	CH15	CH31	CH47	CH63	CH79	CH95	CH111	CH127	CH143	CH159	CH175	CH191

Table 5-1 Stimulus Memory Data To Front Panel Mapping

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Appendix A Glossary of Terms

A16/A24/A32	VXI Register Based Programming Mode.
ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
CSTROBE-	Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data.
DRVFLT	Driver signal generated when the output current exceeds 60mA for greater than 1ns. When a “drive fault” condition occurs all eight drivers will be shut down and the front panel “OVERDRIVE” LED will illuminate.
ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
EXT_CLK	Selected external clock from the front panel J8 connector (EXCLK1 or EXCLK2) or the programmable clock from the SR121/SR210 module.
FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
FUNCTION CODE(FC)	Each module in a SR192 is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
GROUP ENABLE	Group enable signal. This signal can be used to enable a group of I/O channels.
INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
INT_CLK	Selected internal timing module clock from the motherboard (10MHz, 20MHz or 50MHz).
I/O CHANNELS	Eight bi-directional variable voltage data channels.

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I/O MODULE	Any of Talons Stimulus/Response modules for the SR192.
OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
RESPONSE	The response data of the SR192 is comprised of EXPECT, MASK and RECORD memory in five memory I/O modules and just RECORD memory in three memory I/O modules.
SEQUENCE	A sequence is the link between the timing sets and the tables.
SHIFT STROBE	This signal is used to record intermediate data from the UUT for the shift function modes.
STIM_LOAD	Timing module control signal that routes the data from the stimulus memory to the output registers. The rising edge of this control signal also registers the stimulus address (FMA) when the output register delay is enabled.
STIMULUS	The stimulus data of the SR192 is comprised of OUTPUT and TRISTATE memory located on the I/O modules.
SR_CLK	Stimulus/Response Clock. This signal, generated by the timing generator, clocks the word generator.
SUBSEQUENCE	A subsequence is a single element of a sequence. A subsequence selects a timing set, table, loop count, jump condition and control flags.
TABLE	A table is the structure that defines a FMA range for the subsequence. The FMA range is broadcast to all the I/O modules connected to the timing module.
TIMING MODULE	Any of Talons Timing Modules for the SR192.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Four pages of sixteen timing sets can be defined.
TRANSFER	See WORD.
TRISTATE Dn	Tristate driver data from the stimulus memory.
TS_CLK	Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK.
TSENABLE1	Timing Set Enable One. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight.
TSENABLE2	Timing Set Enable Two. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight.
TSINPUT1	Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT1A is routed to TSA INPUT1, TSINPUT1B is routed to TSB INPUT1.
TSINPUT2	Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT2A is routed to TSA INPUT2, TSINPUT2B is routed to TSB INPUT2.
TSOUT1	Timing Set Output One. General purpose output signal generated by the timing module.
TSOUT2	Timing Set Output Two. General purpose output signal generated by the timing module.

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TSOUT3	Timing Set Output Three. General purpose output signal generated by the timing module.
TSOUT4	Timing Set Output Four. General purpose output channel generated by the timing module. Also used to enable the selected channel mode function.
TSOUT5	Timing Set Output Five. General purpose output channel generated by the timing module. Also used as a strobe for the SR121/SR210 probe.
TSSTROBE1	Timing Set Strobe One. This signal, generated by the timing generator, can be selected as the input strobe or shift strobe.
TSSTROBE2	Timing Set Strobe Two. This signal, generated by the timing generator, can be selected as the input strobe.
V+	Positive input voltage from I/O used to supply power to the variable voltage driver/receiver I/O modules.
V-	Negative input voltage from I/O used to supply power to the variable voltage driver/receiver I/O modules.
VADDR	The address bus from the VXI Backplane.
VDATA	The data bus from the VXI Backplane.
VECTOR	See WORD.
VISR	Output driver slew rate voltage set by the internal DACs (SR110 or SR210) or external reference inputs from the front panel connector J9.
VIH	High input voltage references set by the internal DAC's (SR110 or SR210) or external reference inputs from front panel connector J9.
VIL	Low input voltage references set by the internal DAC's (SR110 or SR210, or external reference inputs from front panel connector J9.
VOH	High output voltage references set by the internal DAC's (SR110 or SR210) or external reference inputs from front panel connector J9.
VOL	Low output voltage references set by the internal DAC's (SR110 or SR210) or external reference inputs from front panel connector J9.
VOLTAGE GROUP	Voltage groups refer to the physical assignment of reference signals and voltage inputs supplied to the variable voltage I/O modules.
VOLTAGE REFERENCES	See VOH, VOL, VIH and VIL
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192.

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Appendix B Function Code Map

Address Location:

Driver/Receiver modules are each given a 256K word address space starting at 0x200000.

Specifications:

The SR114 is a five memory D/R module.

- Output
- Tristate
- Expect
- Mask
- Record
- Masked error (virtual)
- Response (virtual)

Eight output (-15 to +15), eight input (dual threshold) 128K per channel, algorithmic.

Function Code Assignments:

FC0 Read/write OUTPUT memory.
128K x 8 word and byte access. 1- outputs a high level.
Word read/writes access two consecutive transfer locations.

FC1 Read/write TRISTATE memory.
128K x 8 word and byte access. 1- disables driver output.
Word read/writes access two consecutive transfer locations.

FC2 Read/write EXPECT memory.
128K x 8 word and byte access. See table below.
Word read/writes access two consecutive transfer locations.

FC3 Read/write MASK memory.
128K x 8 word and byte access.
Word read/writes access two consecutive transfer locations.

MASK	EXPECT	Result Condition
0	0	Expect < VIL, '0'
0	1	Expect > VIH, '1'
1	0	Masked off (Record as expect zero), 'M'
1	1	Expect > VIL and < VIH, 'T''

FC4 Read/write RECORD memory.
128K x 8 word and byte access.
Word read/writes access two consecutive transfer locations.

DATA RECEIVED	EXPECT CODE FROM ABOVE			
	'0'	'1'	'M'	'T'
< VIL	0	1	0	1
> VIH	1	0	1	1
> VIL and < VIH	1	1	1	0

FC5 Read masked error (unmasked error & expect low & expect high).
128K x 8 word and byte access.

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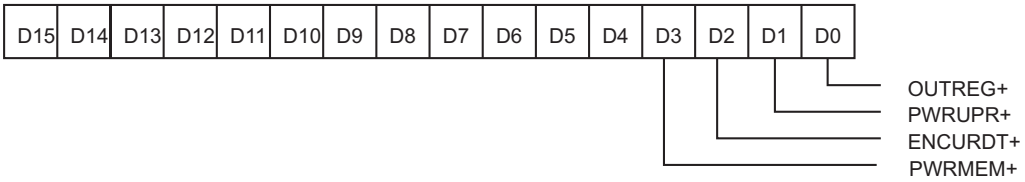
Word reads access two consecutive transfer locations.

DATA RECEIVED	EXPECT CODE FROM ABOVE			
	'0'	'1'	'M'	'T'
< VIL	0	1	0	1
> VIH	1	0	0	1
> VIL and < VIH	1	1	0	0

FC6 Read RESPONSE data (unmasked error & expect low).
128K x 8 word and byte access.

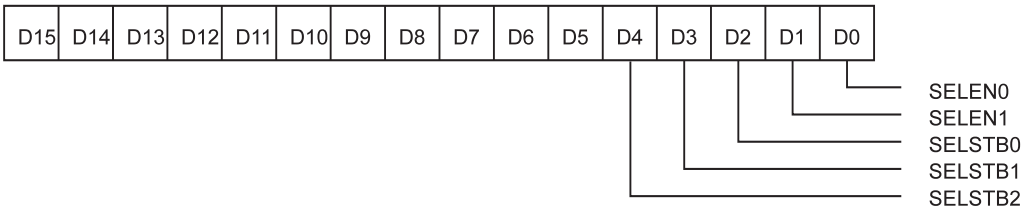
DATA RECEIVED	EXPECT CODE FROM ABOVE			
	'0'	'1'	'M'	'T'
< VIL	0	0	0	0
> VIH	1	1	1	0
> VIL and < VIH	1	0	1	1

FC8 Write output/power management register.
The output/power management register programs the output register setting as well as power saving modes.



OUTREG+	Output Register Enable (1-Enable output register all eight channels)
PWRUPR+	Driver Power Enable (1-Turns on all eight drivers).
ENCURDT+	Over Current Detect Enable (1-Enables over current detect logic).
PWRMEM+	Turn on Driver/Receiver Memory Power (1-Turns on memory power).

FC9 Write I/O control register.
The I/O control register programs the output enable and input strobe selectors for all eight channels..



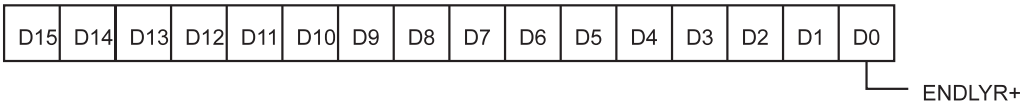
SELEN1	SELEN0	Selected Enable (all 8 channels)
0	0	TSENable1
0	1	TSENable2
1	0	FCNTL1
1	1	FCNTL2

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SELSTB0	Selected Shift Strobe (all 8 channels)
0	TSSTrobe1
1	FCNTL1

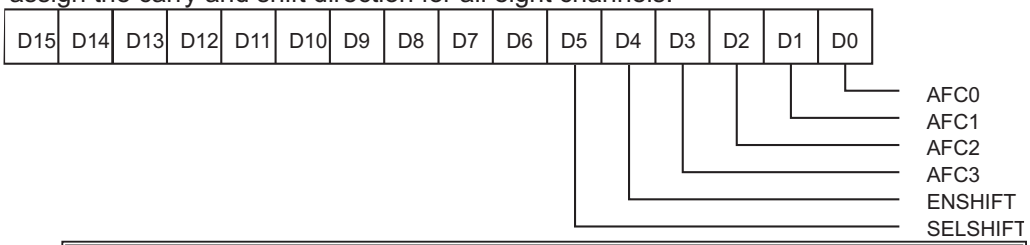
SELSTB2	SELSTB1	Selected Input Strobe (all 8 channels)
0	0	TSSTrobe2
0	1	FCNTL2
1	0	CSTROBE
1	1	TSST1

FC10 Write card control register
This register enables/disables the input address delay register, 1-enables the delay register.



FC11 Write drive fault latch reset.
This decode resets the drive fault signal for this module.

FC12 Algorithm select and control register.
This register is used to program the driver/receiver algorithm as well as assign the carry and shift direction for all eight channels.



AFC3	AFC2	AFC1	AFC0	Algorithm
0	0	0	1	Multiplex
0	0	1	0	Serial
1	0	0	0	Hold
1	0	0	1	RTZ
1	0	1	0	RTO
1	0	1	1	RTC
1	1	0	0	Increment 1
1	1	0	1	Increment 2
1	1	1	0	Increment 4
1	1	1	1	Increment 8

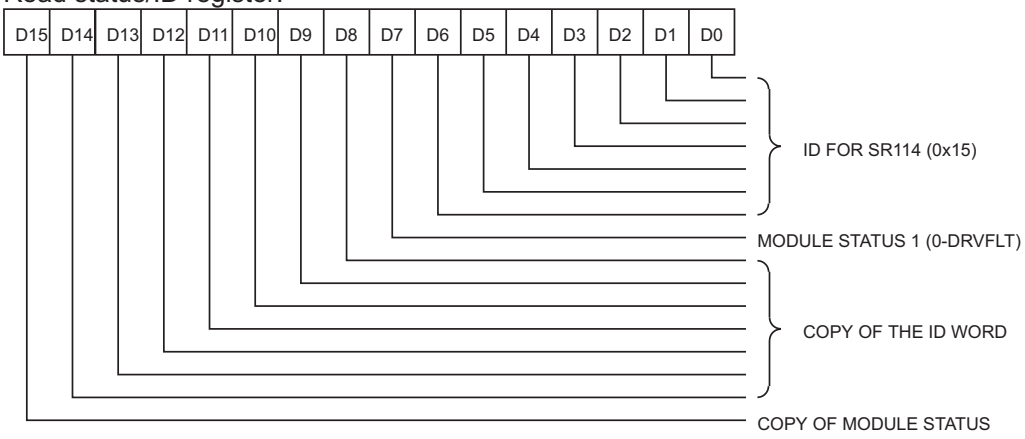
ENSHIFT — A one programmed in the bit position enables the serial mode on the SR114 for input and output. Bits are shifted from the most significant channel to the least significant channel. A zero disables the serial mode and enables the SR114 for all other modes..

SELSHIFT — For the outputs a one sets the carry in to always be true. A zero sets the carry in to be the carry out of the most significant channel of the next lower I/O module.
For the inputs a one sets the serial in to be the serial out of the next higher I/O module (serial out is the least significant channel). A zero sets the serial in to come from the most significant channel from the front panel for the specific I/O module.

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Note: The carry out/in and serial out/in signals that connect adjacent I/O modules are common, therefore the order of programming is critical in order to prevent two outputs from driving at the same time (i.e. Serial mode shifts from most to least significant channel and increment carries from least to most significant channel). ENSHIFT 0 to 1 (non shift to shift) must be programmed from the least significant I/O module to the most significant I/O module. ENSHIFT 1 to 0 (shift to non shift) must be programmed from the most significant I/O module to the least significant I/O module..

FC15 Read status/ID register.



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Appendix C SR192 Clock Timing

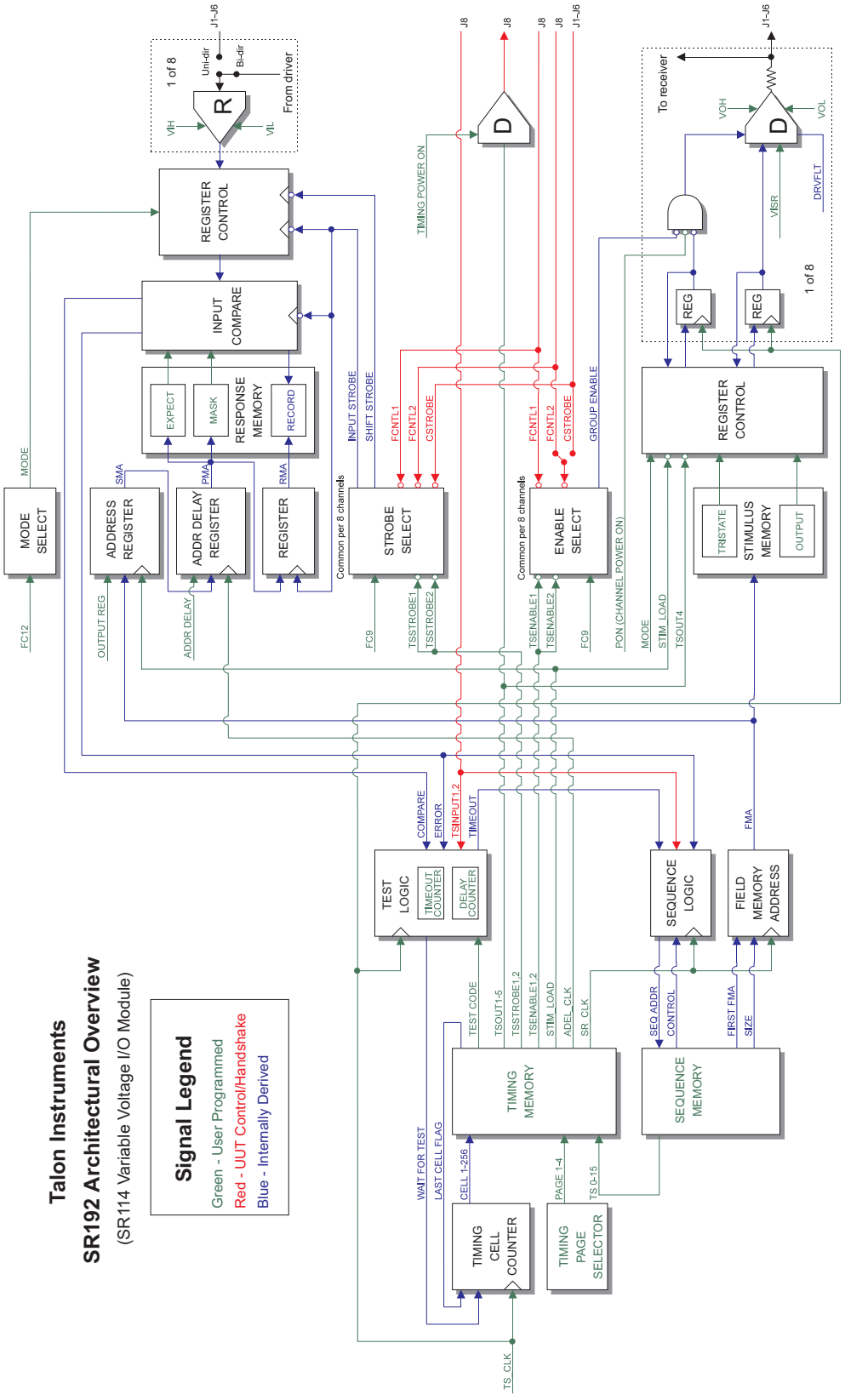
This appendix gives the SR192 clock timing relationships.

Description	From	To	Typ
External Clock One Propagation TTL Setting.	EXCLK1	TS_CLK	27-A 31-B
External Clock One Propagation Programmable Setting.	EXCLK1	TS_CLK	32-A 36-B
External Clock One Propagation Differential Setting.	EXCLK1	TS_CLK	54-A 57-B
External Clock Two Propagation.	EXCLK2	TS_CLK	22
Internal Clock to TSA Output Clock Propagation TTL Setting.	TS_CLK	CLOCKA	8
Internal Clock to TSA Output Clock Propagation Programmable Setting.	TS_CLK	CLOCKA	11
Internal Clock to TSA Output Clock Propagation Differential Setting.	TS_CLK	CLOCKA	17
Internal Clock to TSB Output Clock Propagation.	TS_CLK	CLOCKB	4

Programmable measurements were made with VOH set to +5V, VOL set to 0V, VISR set to +2V and VIL set to +2.5V.

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Appendix D Block Diagram



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