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OPERATOR'S MANUAL

# Talon Instruments™

# SR101

## Timing Set Module




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Instrument Part Number: SR101


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Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.




This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.




Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.


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# Table of Contents

1 Introduction . . . . . 1-1

2 Specifications . . . . . 2-1

2.1 Timing Generator . . . . . 2-1

2.2 Word Generator . . . . . 2-1

2.3 Electrical . . . . . 2-1

2.4 Environmental . . . . . 2-2

3 Jumpers/Installation . . . . . 3-1

3.1 Test Point Description . . . . . 3-1

3.2 Jumper Description . . . . . 3-1

3.2.1 Select ISP Block (E1, E2, E3) . . . . . 3-1

3.2.2 Select INPUT2 Source (E4, E5, E6) . . . . . 3-1

3.2.3 Select INPUT1 Source (E7, E8, E9, E10) . . . . . 3-2

3.2.4 ISPDI/WAIT - Select (E11, E12, E13) . . . . . 3-2

3.3 Installation . . . . . 3-2

4 Functional Description . . . . . 4-1

4.1 Timing Generator Logic . . . . . 4-1

4.2 Word Generator Logic . . . . . 4-3

5 SR101 Operation . . . . . 5-1

5.1 Timing Generator Programming . . . . . 5-1

5.1.1 Configuring SR101 Modules . . . . . 5-1

5.1.1.1 Programming SR101 Configuration Using the Development Editor . . . . . 5-1

5.1.1.2 Programming SR101 Configuration Using SCPI Commands . . . . . 5-1

5.1.1.3 Programming SR101 Configuration Using the Plug and Play Driver . . . . . 5-2

5.1.2 Timing Generator Global Settings . . . . . 5-2

5.1.2.1 Programming SR101 Global Settings Using the Development Editor . . . . . 5-3

5.1.2.2 Programming SR101 Global Settings Using SCPI Commands . . . . . 5-3



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5.1.2.3 Programming SR101 Global Settings Using the Plug and Play Driver . . . . . 5-4
5.1.3 Programming the Timing Cell Memory . . . . . 5-4
5.1.3.1 Creating and Programming Timing Sets Using the Development Editor . . . . . 5-4
5.1.3.2 Creating and Programming Timing Sets Using SCPI Command . . . . . 5-5
5.1.3.3 Creating and Programming Timing Sets Using the Plug & Play Driver . . . . . 5-7
5.2 Timing Generator Execution . . . . . 5-9
5.2.1 Timing Generator Execution Modes . . . . . 5-10
5.2.1.1 Programming the Execution Mode Using SCPI Commands . . . . . 5-10
5.2.1.2 Programming the Execution Mode Using the Plug and Play Driver . . . . . 5-11
5.2.2 Timing Generator Execution . . . . . 5-11
5.2.2.1 Timing Generator Execution Using SCPI Commands . . . . . 5-11
5.2.2.2 Timing Generator Execution Using the Plug and Play Driver . . . . . 5-13
5.3 Word Generator Programming . . . . . 5-13
5.3.1 Creating Word Generator Tables . . . . . 5-13
5.3.1.1 Creating Word Generator Tables Using SCPI Commands . . . . . 5-14
5.3.1.2 Creating Word Generator Tables Using the Plug and Play Driver . . . . . 5-14
5.3.2 Creating and Programming Sequences . . . . . 5-14
5.3.2.1 Multiple Subsequence Definition . . . . . 5-16
5.3.2.2 Sequence Looping . . . . . 5-16
5.3.2.3 Subsequence Looping . . . . . 5-17
5.3.2.4 Unconditional Sequence Jumping . . . . . 5-17
5.3.2.5 Conditional Sequence Branching . . . . . 5-19
5.3.2.6 Stopping a Subsequence . . . . . 5-20
5.3.2.7 Editing a Subsequence . . . . . 5-20
6 SR192 Timing Module Applications . . . . . 6-1
61 SR101 Module Status . . . . . 6-1
62 Synchronizing Timing Set A and Timing Set B . . . . . 6-1
63 Linking Multiple SR192's . . . . . 6-2



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Appendix A Glossary of Terms . . . . . A-1

Appendix B SR101 Function Code Map . . . . . B-1

Appendix C SR101 Worksheets . . . . . C-1



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# List of Figures

Figure 3-1 Test Point/Jumper Locations . . . . . 3-1
Figure 3-2 Test Input1 Source . . . . . 3-2
Figure 3-4 SR192 Motherboard Side View . . . . . 3-3
Figure 4-1 SR101 State Machine . . . . . 4-1
Figure 4-2 Timing Generator Block Diagram . . . . . 4-1
Figure 4-3 Word Generator Block Diagram . . . . . 4-3
Figure 5-1 Development Editor-Edit SR Module Panel . . . . . 5-1
Figure 5-2 Plug & Play Configure Timing Module Panel . . . . . 5-2
Figure 5-3 Development Editor-Edit SR Module Timing Generator Tab Panel . . . . . 5-3
Figure 5-4 Plug & Play Timing Module Global Parameters . . . . . 5-4
Figure 5-5 Development Editor Timing Set Menu . . . . . 5-5
Figure 5-6 Development Editor Edit->Add->Timing Set . . . . . 5-5
Figure 5-7 Timing Set Worksheet Example . . . . . 5-6
Figure 5-8 Plug & Play Timing Define . . . . . 5-7
Figure 5-9 Plug & Play Program Timing Set . . . . . 5-8
Figure 5-10 SR101 States . . . . . 5-9
Figure 5-11 Plug & Play Timing Cell Test . . . . . 5-9
Figure 5-12 Plug & Play Execution Mode . . . . . 5-11
Figure 5-13 Timing Set Example, With Wait . . . . . 5-12
Figure 5-14 Timing Set Example, No Wait . . . . . 5-12
Figure 5-15 Plug & Play Execute Timing Set . . . . . 5-13
Figure 5-16 Plug & Play Define Table . . . . . 5-14
Figure 5-17 Plug & Play Define Sequence . . . . . 5-15
Figure 5-18 Sequence Example . . . . . 5-15
Figure 5-19 Multi Subsequence Sequence . . . . . 5-16
Figure 5-20 Sequence Looping . . . . . 5-16



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Figure 5-21 Unconditional Sequence JUMP . . . . . 5-17
Figure 5-22 Subsequence Looping . . . . . 5-17
Figure 5-23 Unconditional Sequence GOSUB . . . . . 5-18
Figure 5-24 Plug & Play Sequence Branch . . . . . 5-19
Timing Set Memory Pages . . . . . B-1
Timing Set Memory Bits . . . . . B-1
Loop Count Register . . . . . B-2
Timing Set Sequence Memory . . . . . B-3
Function Code Eight Memory . . . . . B-4
Timing Set Control Register Two . . . . . B-4
Timing Set Control Register One . . . . . B-4
Timeout Register . . . . . B-5
LASTWD, SYNC, TESTEN and GOOD0, GOOD1 Memory . . . . . B-5
Function Code 15 Write . . . . . B-6
Function Code 15 Write . . . . . B-6
Function Code 15 Read . . . . . B-6



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# List of Tables

Table 3-1 SR101 Test Point Description. . . . . 3-1

Table 6-1 SR101 Status Register Description . . . . . 6-1



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# 1 Introduction

Talon's SR192 digital test module is a modular VXI stimulus/response system. The SR192 motherboard is a two slot, "C" size module which houses up to 12 I/O modules. I/O modules are designed to provide either 8 or 16 stimulus/response channels for a total of 96 or 192 channels. Modules provide many logic options such as fixed voltage TTL, ECL, RS485/422 or variable voltages of +/- 15V or +5/-2. The I/O channels may also be single-ended or double-ended (differential) logic.

Multiple SR192's may be linked in a master/slave configuration to provide up to 1152 channels in a single VXI 13-slot chassis.

This manual is for the SR101 Timing module. The function of the SR101 Timing Set Module is to provide all the timing and control for the SR192 I/O modules when executing a stimulus/response operation or emulating a bus interface. After being programmed and commanded to start, the SR101 can generate output signals to the UUT, test input signals from the UUT (i.e. Handshake or test input), generate memory address and control signals for the SR192 I/O modules, and finally test the results from the I/O modules.

Each SR192 may have one or two SR101 modules, nomenclated TSA and TSB. TSA controls up to six I/O modules, channels 1-96. TSB controls up to six I/O modules, channels 97-192. The Timing Sets may operate independently or may be synchronized with one another. Additionally, timing sets from different SR192's may be synchronized together through the J7 master/slave front panel connector.

The layout of this manual is in five sections described below:

| | |
|---|---|
| 1. Introduction | This section |
| 2. Specifications | SR101 electrical and environmental specifications |
| 3. Jumpers/Installation | Description of the jumpers and installation of the SR105 |
| 4. Functional Description | SR101 functional description |
| 5. Operation | SR101 Operation |

In addition, five appendices are included:

| | |
|---|---|
| A. Glossary of Terms | Definition of terms used in this manual |
| B. Function Code Map | SR101 Function Code |
| C. Worksheets | SR101 Worksheets |



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# 2 Specifications

The following sections list the specifications of the SR101 I/O module.

## 2.1 Timing Generator

### Timing Cycles

Number of Static Pages.....4
Number per Page .....16

### Number of Cells

Maximum .....256
Minimum Non IDLE .....2
Minimum IDLE .....4

### Test Input Wait Conditions

TSINPUT1.....High/Low Level
TSINPUT2 .....High/Low Level/Edge
ERROR .....True/False
RAW_ERROR.....True/False
Delay Minimum .....0 TS_CLKs
Delay Maximum.....32768 TS_CLKS

Note: Test Conditions can be programmed in any cell except TSINPUT2 edge in last cell and two consecutive TSINPUT2 edge same level.

### Wait Timeout

Minimum .....0-Disabled
Maximum .....32768 TS_CLKS

Note: Timeout disabled for Delay and RAW_ERROR tests.

## 2.2 Word Generator

### Sequence

Number of Subsequences Minimum .....1
Number of Subsequences Maximum .....131071
Sequence Loop Minimum .....1 (Single)
Sequence Loop Maximum.....32768
Continuous Execution .....Yes

### Subsequence

Number of Timing Cycles .....1
Number of I/O Transfers Minimum .....1
Number of I/O Transfers Maximum .....131072
Subsequence Loop Minimum.....1
Subsequence Loop Maximum.....32768

### Subsequence Conditional Jump/Gosub Test Conditions

TSINPUT1.....High/Low Level
TSINPUT2.....High/Low Level
ERROR .....True
Jump Enable .....True
Timeout .....True

## 2.3 Electrical

### Timing/Sequence Clock (TS_CLK)

Maximum Frequency .....50 MHZ
Minimum Frequency.....10 Hz



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### TSINPUT Test Signal Delay

Linked or Master Mode .....3 TS_CLKs
Unlinked Independent Mode .....2 TS_CLKs
Note: One TS_CLK delay can be eliminated via hardware jumpers. Refer to section 2.2.2 and 2.2.3 of this manual.

### TSINPUT Signal Pulse Width

Level Test Minimum Pulse Width.....1 TS_CLK period
Edge Test Minimum Pulse Width.....10ns

### Subsequence Conditional Clock (SR_CLK)

Setup to end of cycle .....35ns
3 cells min 25ns from begin. One cell before last cell.

### Power

+5V .....2.3A

## 2.4 Environmental

### Temperature Range

Operating .....0°C to 50°C
Storage .....-10°C to 70°C

### Altitude

Operating.....Sea level to 10,000 ft.
Storage .....Sea level to 40,000 ft.

### Relative Humidity

Operating.....0 to 95% non-condensing



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# 3 Jumpers/Installation

The SR101 Timing module requires firmware revision 1.14 or later for proper operation. Contact Talon Instruments for information on firmware upgrades.

Figure 3-1 is a locator diagram for the test points and jumper blocks of an SR101.

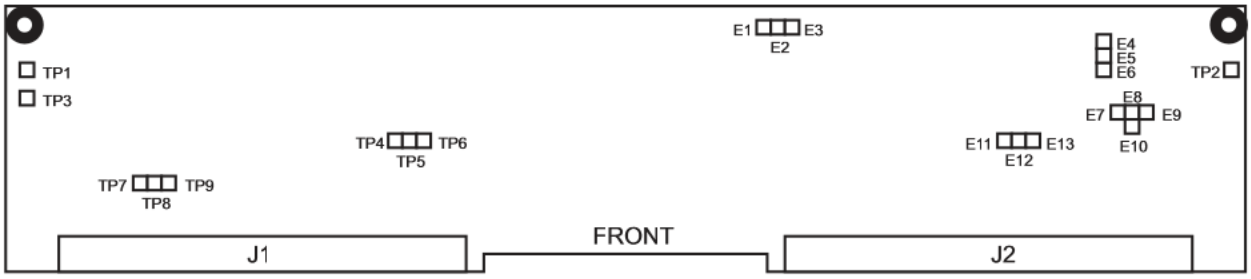



Figure 3-1 Test Point/Jumper Locations

## 3.1 Test Point Description

Table 3-1 describes the test points and jumper locations on the SR101 Timing Module.

| Test Point | Mnemonic | Description |
|---|---|---|
| TP1 | GND | Logic ground |
| TP2 | GND | Logic Ground |
| TP3 | SEQACT- | Low Indicates non-idle sequence running |
| TP4 | SNSEQ- | Low selects next sequence |
| TP5 | SPSEQ- | Low selects present sequence |
| TP6 | LSTHSMA- | Low indicates next TS_CLK is last cell |
| TP7 | LPSEQ- | Low loads present sequence |
| TP8 | LSTWD- | Low indicates last word of table |
| TP9 | TESTJ- | Low indicates a branch condition is true |

Table 3-1 SR101 Test Point Description

## 3.2 Jumper Description

The following sections describe each jumper block on the SR101.

### 3.2.1 Select ISP Block (E1, E2, E3)

This jumper block is used for programming the in-circuit-programmable devices.

E1 to E2 selects U109, U108, U106, U107, U105, U103 and U118 for programming.

E2 to E3 selects U17, U14, U22, U21, U116, U101 and UU112 for programming.

### 3.2.2 Select INPUT2 Source (E4, E5, E6)

Each timing module can test two externally generated signals, INPUT1 and INPUT2. INPUT2's source is normally TSINPUT2 from the front panel sampled using TS_CLK to guarantee correct setup and hold



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times. The raw TSINPUT2 signal can be jumpered in reducing the number of WAIT delays by one TS_CLK. Figure 3-3 describes the INPUT2 source jumper.

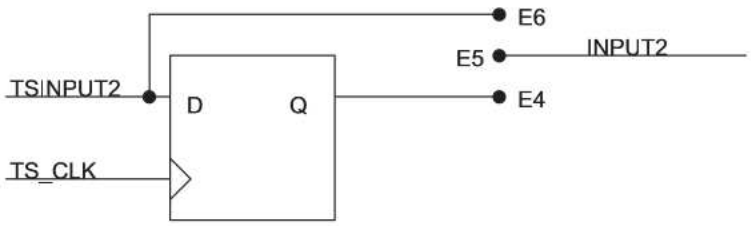



Figure 3-3 Test Input2 Source

Factory Default: Trace connecting E4 to E5 on back side.

### 3.2.3 Select INPUT1 Source (E7, E8, E9, E10)

Each timing module can test two externally generated signals, INPUT1 and INPUT2. INPUT1's source is normally TSINPUT1 or TSINPUTM from the front panel sampled using TS_CLK to guarantee correct setup and hold times. TSINPUTM is selected to guarantee correct operation when two timing modules are linked for synchronous operation. The raw TSINPUT1 or TSINPUTM signal can be jumpered in reducing the number of WAIT delays by one TS_CLK. Figure 3-2 describes the INPUT1 source jumper.

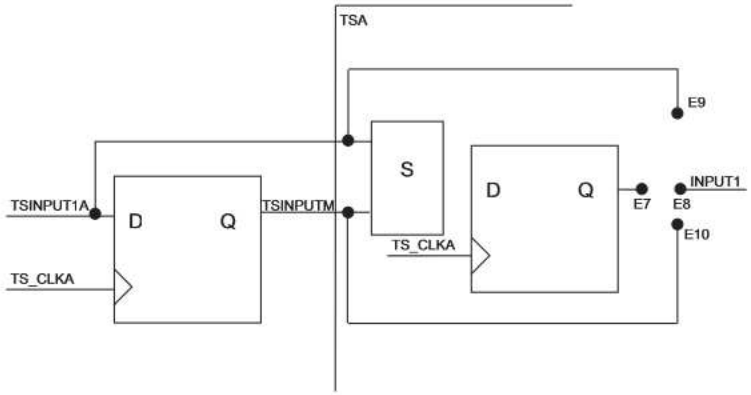



Figure 3-2 Test Input1 Source

Factory Default: Trace connecting E7 to E8 on back side.

### 3.2.4 ISPDI/WAIT - Select (E11, E12, E13)

This jumper block is used for programming the in-circuit-programmable devices.

E11 to E12 enables U117 and U118 for programming. E12 to E13 Normal operation.

## 3.3 Installation

Each SR192 motherboard can house up to two timing modules. Timing modules are installed in motherboard slots TSA and TSB. See Figure 3-4.

Follow the following steps to add or replace a timing module:

| | |
|---|---|
| Step 1. | Remove SR192 from the chassis and take to an ESD safe area. |
| Step 2. | Remove top cover screws, refer to figure 3. |
| Step 3. | If replacing a timing module, remove it by grasping at each corner and gently rocking forward and back while pulling it away from the motherboard. |
| Step 4. | Insert the new timing module in the TSA or TSB slots, Figure 3-4, by lining up the J1 and J2 connectors with the motherboard connectors and gently pushing down. All SR192 modules are keyed along with the asso- |



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ciated motherboard connectors. If the module cannot be inserted, check for bent pins and make sure the module is installed in the proper mother-board slot.

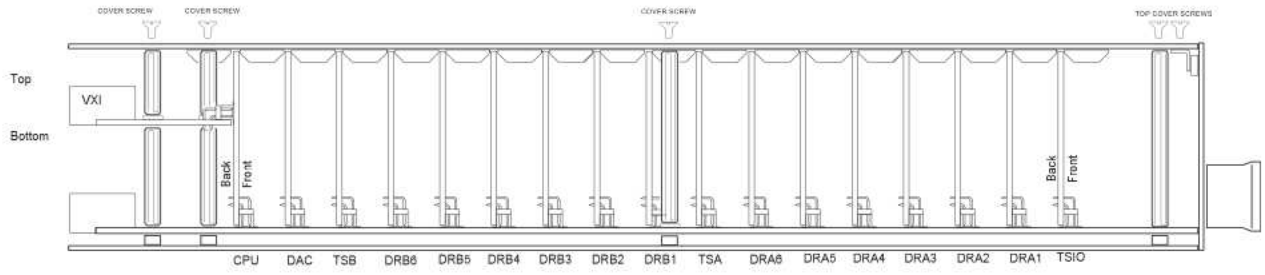



Figure 3-4 SR192 Motherboard Side View

**CAUTION**

**Although the modules and the associated mating connectors have been keyed, it is possible to force a module into an incorrect slot.**



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# 4 Functional Description

The SR101, like the SR100, is a programmable state machine. Figure 4-1 illustrates that the SR101 state machine is comprised of two synchronous state machines referred to as the TIMING GENERATOR and the WORD GENERATOR.

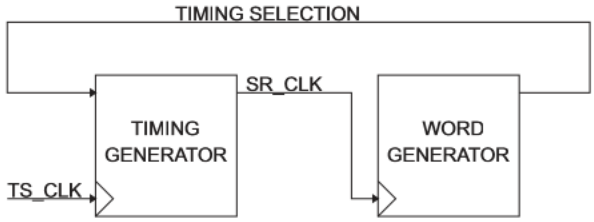



Figure 4-1 SR101 State Machine

The timing generator controls the clock signal for the word generator. The word generator selects the timing for each word.

The following sections describe the timing generator and the word generator logic.

## 4.1 Timing Generator Logic

Figure 4-2 shows the block diagram of the timing generator logic.

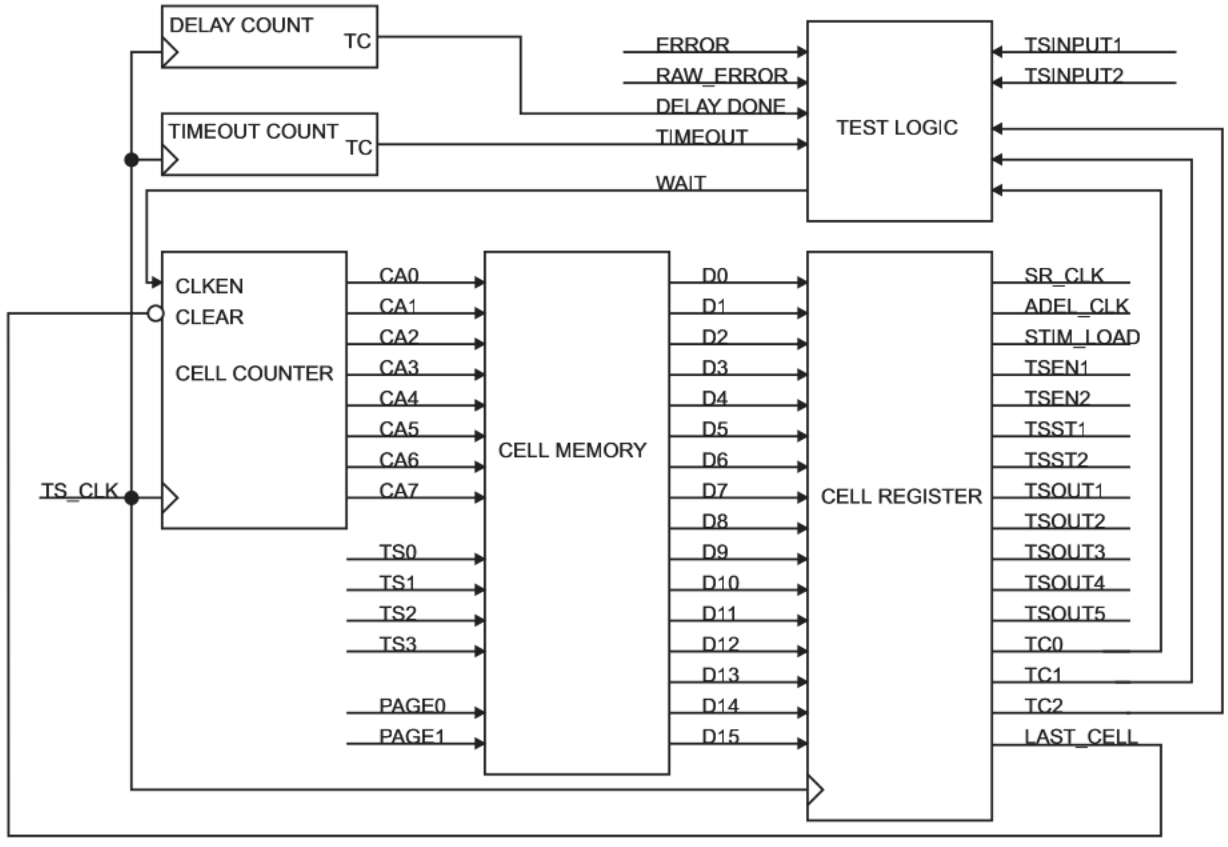



Figure 4-2 Timing Generator Block Diagram



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The following text describes the major elements of Figure 2.

TS_CLK: This signal is the timing generator system clock. Every rising edge of the TS_CLK causes a new timing generator state, called a CELL. The minimum resolution of a timing generator cell is the period of the TS_CLK.

Cell Counter: The cell counter generates the lower eight address lines (CA0-CA7) to the cell memory. The counter is cleared to zero by a feedback signal programmed into the cell memory called LAST_CELL. The counter can be stopped by a signal generated by the test logic called WAIT.

Cell Memory: The contents of the cell memory controls the timing generator state machine as well as the word generator clock, SR192 I/O module control signals and user defined timing outputs. Each memory location is a timing generator state. The cell memory is segmented into the following address groups:

1. PAGE0,PAGE1: Four timing pages selected by a static register
2. TS0-TS3: Sixteen timing sets selected by the word generator
3. CA0-CA7: 256 timing cells

Cell Register: The contents of the cell memory are registered and clocked by the same signal that generates the lower eight addresses. The signals are described below:

| | |
|---|---|
| SR_CLK: | Word generator clock |
| ADEL-CLK: | I/O Module Response Delay Clock |
| STIM_LOAD: | I/O Module Stimulus Load Clock |
| TSEN1: | I/O Module Driver Enable |
| TSEN2: | I/O Module Driver Enable |
| TSST1: | I/O Module Response Clock |
| TSST2: | I/O Module Response Clock. |
| TSOUT1-TSOUT5: | User Defined Outputs |
| TC0-TC2: | Test Logic Control Code |
| LAST_CELL: | Cell Counter Clear Control |

Test Logic: Within each cell, a test code can be programmed to test one of seven conditions. The result of the test can cause the timing state machine to either stop (WAIT) or continue to the next timing cell. The seven conditions are described below:

| | |
|---|---|
| 1, TSINPUT1 LOW: | Front panel signal test for low level |
| 2. TSINPUT1 HIGH: | Front panel signal test for high level |
| 3. TSINPUT2 LOW: | Front panel signal test for low level/edge |
| 4. TSINPUT2 HIGH: | Front panel signal test for high level/edge |
| 5. ERROR: | I/O Module latched real time error. |
| 6. RAW_ERROR: | I/O Module unlatched real time error |
| 7. DELAY: | Delay counter done signal. |

Delay Count: This is a counter that is loaded at the beginning of each new cell. The cell memory can be programmed to remain in the current cell until the counter has reached its terminal count. The delay is counted as the number of additional TS_CLK's.

Timeout Count: This es a counter that can be used to terminate a WAIT condition from the test logic after a programmed number of TS_CLK's have occurred.



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## 4.2 Word Generator Logic

Figure 4-3 is the block diagram for the word generator.

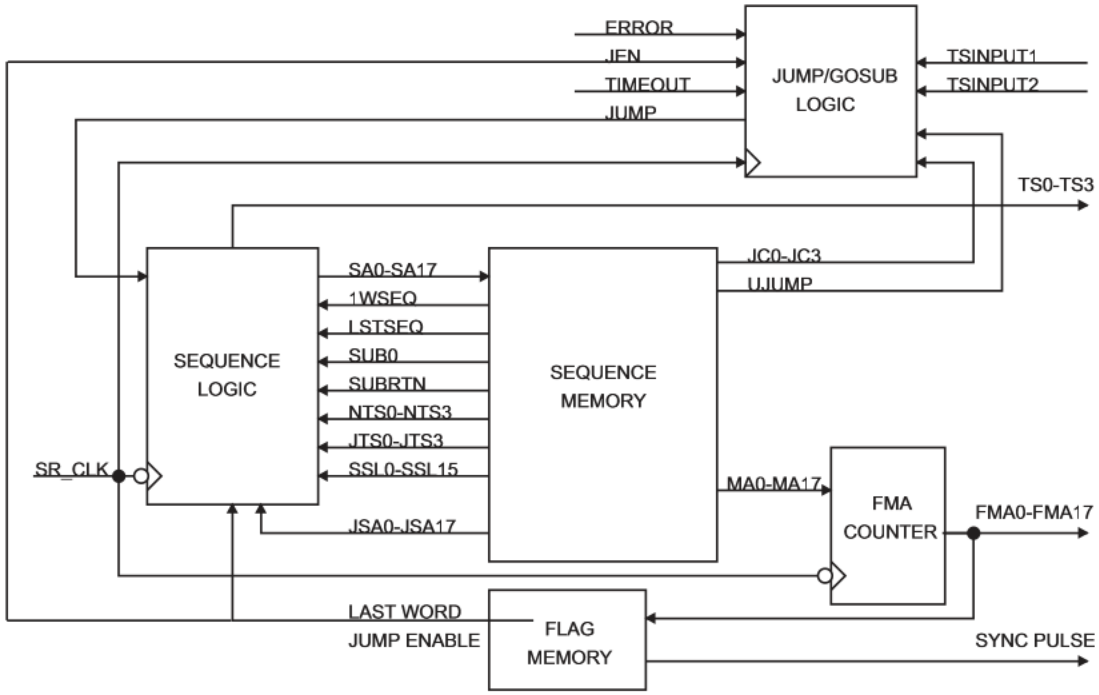



Figure 4-3 Word Generator Block Diagram

The following text describes the major elements of Figure 3.

SR_CLK: This signal is the word generator system clock. The falling edge of the SR_CLK causes one of two functions to occur:

1. Increment the subsequence address (SSA0-SSA17) if LAST WORD is true.

Or

2. Increment the field memory address (FMA0-FMA17) to the next address.

Subsequence Memory: The sequence memory is a 68 bit by 128K memory array that controls the word generator state machine. The sequence memory is addressed by a 17 bit counter generated by the sequence logic. The 68 bits are described below:

| | |
|---|---|
| 1WSEQ (1 bit): | 1 word sequence flag |
| LSTSEQ (1 bit): | Last sequence flag |
| SUB0 (1 bit): | Return to IDLE flag |
| SUBRTN (1 bit): | Subroutine sequence flag |
| NTS0-NTS3 (4 bits): | Next timing set address |
| JTS0-JTS3 (4 bits): | Jump/Gosub timing set address |
| SSL0-SSL15 (16 bits): | Subsequence loop count |
| JC0-JC2 (3 bits): | Jump/Gosub code |
| UJUMP (1 bit): | Unconditional Jump/Gosub flag |
| MA0-MA17 (18 bits): | Field Memory Address (FMA) |
| JSA0-JSA17 (18 bits): | Jump/Gosub Sequence address |



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Flag Memory: The flag memory is addressed by the FMA bus and contains two flags used by the sequence logic (LAST WORD and JUMP ENABLE) and one flag that is routed to the front panel (SYNC PULSE).

FMA Counter: The Field Memory Address (FMA) is broadcast to all the I/O modules being controlled by this timing module. The FMA bus addresses the stimulus/response memory (i.e. Every FMA address generates a new stimulus vector and response memory location). The FMA counter is loaded when a new sequence address is generated by the sequence logic otherwise it is incremented by one every SR_CLK. The FMA counter is cleared to zero when the timing module is idle.

Jump/Gosub Logic: The Jump/Gosub logic receives a jump code for every sequence address. The jump code allows the user to program both conditional and unconditional branches. Conditional Jump/Gosub codes are sampled on the rising edge of SR_CLK and exist for the following events:

1. TSINPUT1 LOW: Front panel signal test for low level
2. TSINPUT1 HIGH: Front panel signal test for high level
3. TSINPUT2 LOW: Front panel signal test for low level
4. TSINPUT2 HIGH: Front panel signal test for high level
5. JENABEE: Table Jump Enable Qualifier
6. ERROR: I/O Module latched real time error true
7. TIMEOUT: Timeout signal true

Sequence Logic: The sequence logic evaluates the current sequence state through external flags (LAST WORD, JUMP and LSTSEQ) and internal counters (subsequence loop and sequence loop) to determine the address of the next subsequence. In addition, the sequence logic also selects the timing for the current sequence through the TS0-TS3 which are fed back to the timing generator.



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# 5 SR101 Operation

The timing/word generator view of the SR101 also extends to the operation of the SR101. The first stip in using the SR101 is to program the timing generator. The word generator is then programmed.

## 5.1 Timing Generator Programming

The timing generator is programmed in three steps:

1. Configure the Timing Module(s)
2. Global Parameters
3. Timing Cell Memory

The timing module can be programmed using any of the following methods:

1. SR192 Development Editor
2. SR192 SCPI commands
3. SR192 Plug and Play Driver
4. A32/A24 VXI Memory

Examples of the first three methods will be given in the following sections.

### 5.1.1 Configuring SR101 Modules

A Single SR192 system can house one or two SR101 timing modules that can be programmed to run synchronously or independent. In addition, multiple SR192 systems can be run in a master/slave configuration where one SR192 (master) is providing the clock, start, stop and sync signals to other SR192's (slaves).

Each module in an SR192 system is selected by a predefined keyword. The two timing modules are referred to as TSA and TSB.

The following assignments can be made:

1. Operation (Independent, Master or Slave).
2. Timing Gen. A/B (Not Linked or Linked).

#### 5.1.1.1 Programming SR101 Configuration Using the Development Editor

The SR101 configuration is programed from the top of the "**Edit->SR Module**" panel.

Figure 5-1 illustrates the "**Edit->SR Module**" panel.

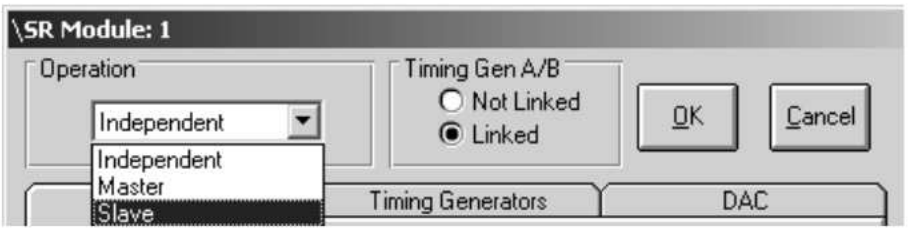



Figure 5-1 Development Editor-Edit SR Module Panel

#### 5.1.1.2 Programming SR101 Configuration Using SCPI Commands

The following SCPI commands configure the "**Operation**" setting:

1. Independant
   MODULE:SELECT TSA
   MODULE:LINK OFF
   OUTPUT:MASTER OFF
2. Master
   MODULE:SELECT TSA
   MODULE:LINK OFF
   OUTPUT:MASTER ON



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3. Slave

```
OUTPUT:MASTER OFF
MODULE:SELECT TSA
MODULE:LINK ON
```

The following SCPI commands configure the "**Timing Gen A/B**" setting:

1. Not Linked (power up default)

```
MODULE:SELECT TSB
MODULE:LINK OFF
```

2. Linked

```
MODULE:SELECT TSB
MODULE:LINK ON
```

#### 5.1.1.3 Programming SR101 Configuration Using the Plug and Play Driver

Figure 5-2 is the Plug & Play panel for configuring the timing modules.

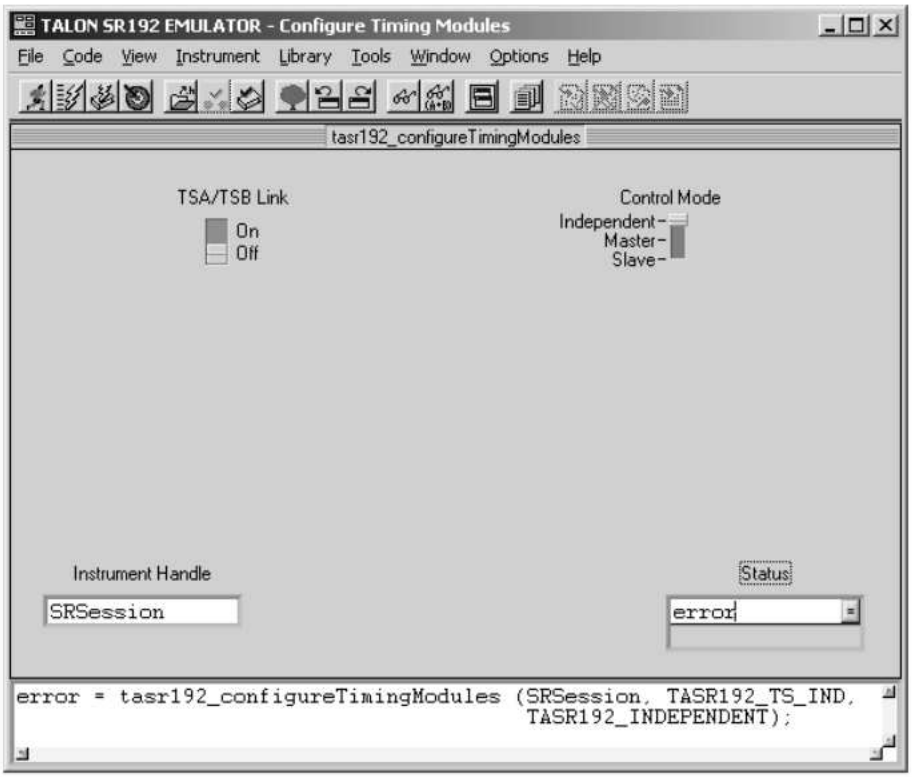



Figure 5-2 Plug & Play Configure Timing Module Panel

### 5.1.2 Timing Generator Global Settings

The following list is the parameters that are global for the entire SR101 module.

1. Clock Source — The TS_CLK can be programmed to the following:
    1. Internal 10 MHz
    2. Internal 20 MHz
    3. Internal 50 MHz
    4. Front Panel EXTCLK1
    5. Front Panel EXTCLK2
2. Delay Count — The delay value for the delay counter can be set between 0 and 32768. A count of zero disables all delay test cells.
3. Timout Count — The cycle timeout counter can be set between 0 and 32768. A setting of zero disables the timeout counter.
4. Test Input 2 — The front panel signals TSINPUT2A and TSINPUT2B can both be programmed as either a level test input or an edge test input.



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#### 5.1.2.1 Programming SR101 Global Settings Using the Development Editor

The "**Timing Generator**" tab from the "**Edit->SR Module**" panel allows the user to program the SR101 global settings.

Figure 5-3 illustrates the "**Timing Generator**" tab panel:

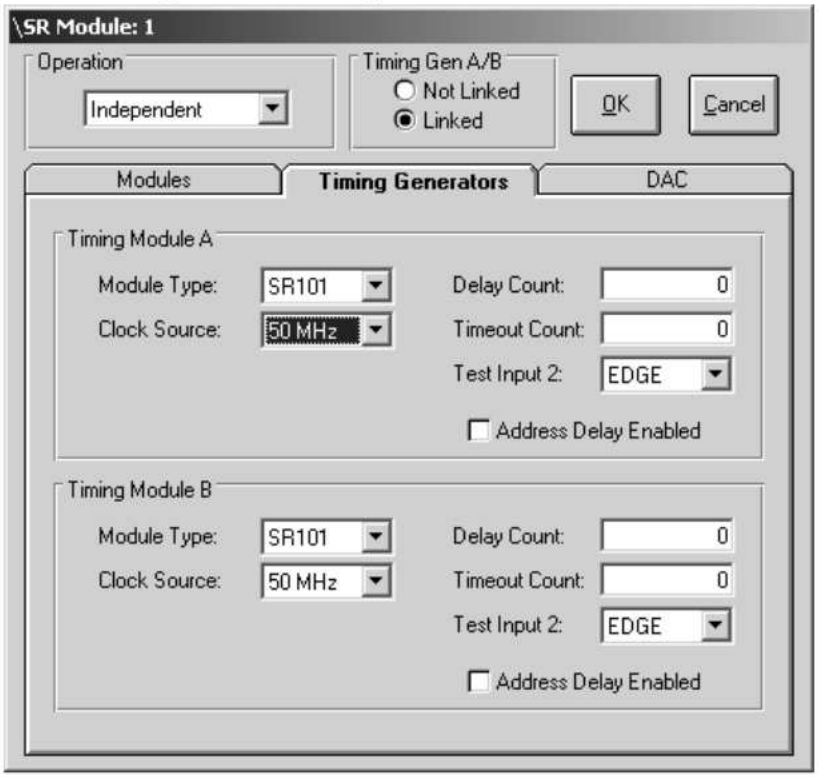



Figure 5-3 Development Editor-Edit SR Module Timing Generator Tab Panel

#### 5.1.2.2 Programming SR101 Global Settings Using SCPI Commands

The following SCPI commands configure TSA and TSB timing modules:

| | |
|---|---|
| 1. Clock Source set to 10 Mhz | TIMING:SETUP:CLOCK 10 |
| 2. Timeout Set to 10 TS_CLKS | TIMING:SETUP:CTIMEOUT 10 |
| 3. Delay Value Set to 100 TS_CLKS | TIMING:SETUP:DELAY 100 |
| 4. TSINPUT2 Mode Set to edge | TIMING:SETUP:TSINPUT2 EDGE |



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#### 5.1.2.3 Programming SR101 Global Settings Using the Plug and Play Driver

Figure 5-4 shows the SR192 Plug and Play driver panel for programming the global parameters.

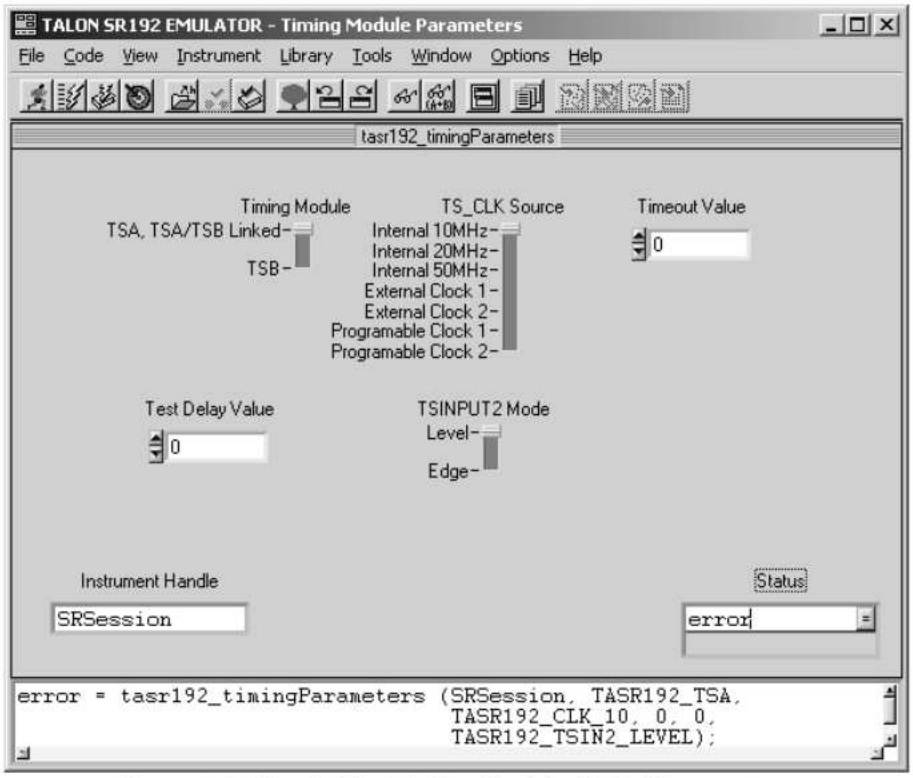



Figure 5-4 Plug & Play Timing Module Global Parameters

### 5.1.3 Programming the Timing Cell Memory

From the previous sections we know that the timing cell memory is segmented into four pages of sixteen timing sets. Prior to programming any timing cell, the timing page must be selected and then a timing set must be defined.

#### 5.1.3.1 Creating and Programming Timing Sets Using the Development Editor



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Figures 5-6 and 5-5 show the Development Editor menu after a timing set called “WRITE” has been defined and the size set to 6 cells.

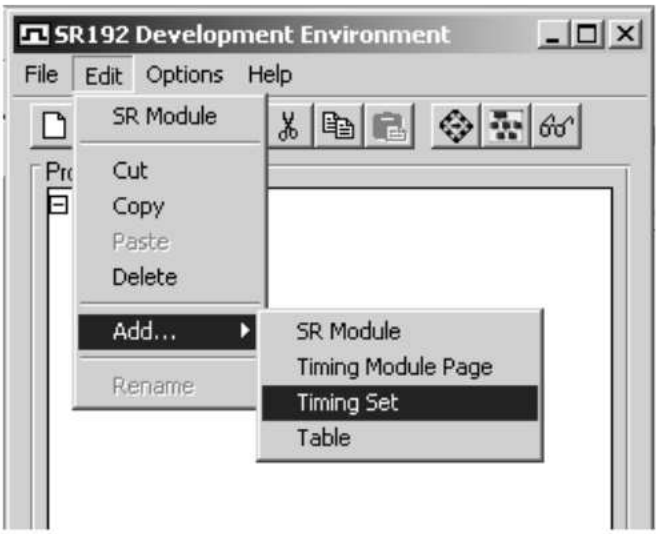



Figure 5-6 Development Editor Edit->Add->Timing Set

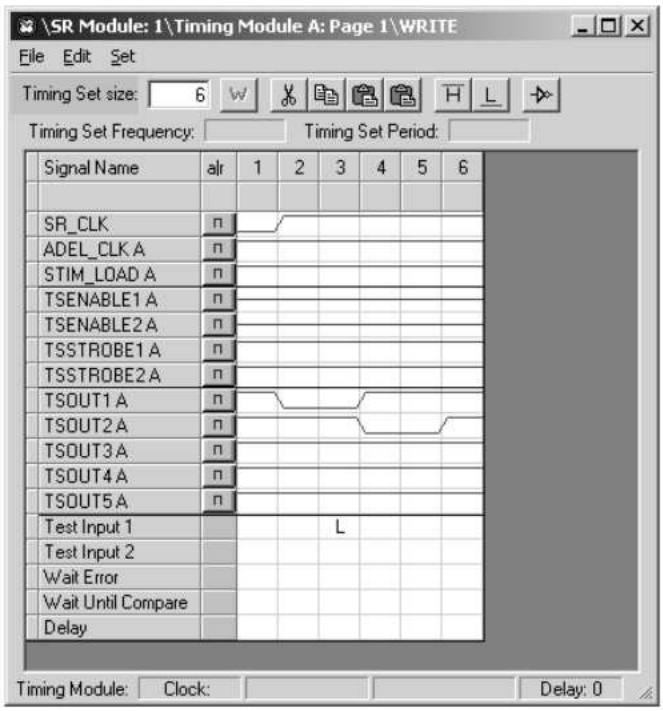



Figure 5-5 Development Editor Timing Set Menu

Up to sixteen timing sets can be programmed per page.

### 5.1.3.2 Creating and Programming Timing Sets Using SCPI Command



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When programming the timing memory using SCPI commands a timing set worksheet is used like the one shown below.

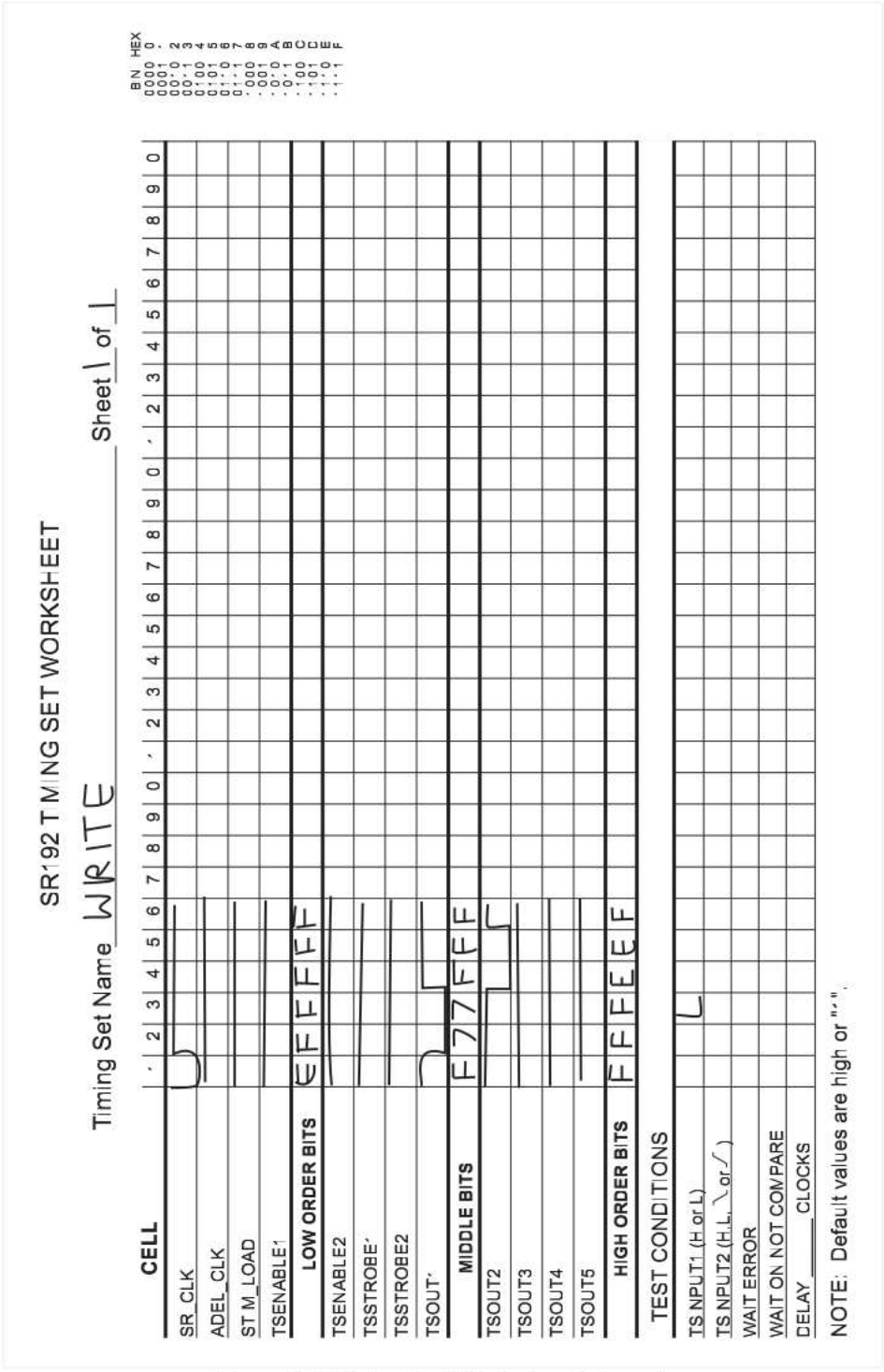



Figure 5-7 Timing Set Worksheet Example

The following SCPI commands program TSA timing cell memory:

| | |
|---|---|
| 1. Select TSA | MODULE:SELECT TSA |
| 2. Reset the selected Timing Module | EXECUTE:MODE RESET |



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| | | |
|---|---|---|
| 3. | Define the "WRITE" Timing Set as 6 Cells | TIMING:DEFINE WRITE,6 |
| 4. | Program the First Cell | TIMING:CELL WRITE,1,#hF7F |
| 5. | Program the Second Cell | TIMING:CELL WRITE,2,#hF7F |
| 6. | Program the Third Cell | TIMING:CELL WRITE,3,#hF7F |
| 7. | Program the Fourth Cell | TIMING:CELL WRITE,4,#hEFF |
| 8. | Program the Fifth Cell | TIMING:CELL WRITE,5,#hEFF |
| 9. | Program the Sixth Cell | TIMING:CELL WRITE,6,#hFFF |
| 10. | Program the TSINPUT1 Test | TIMING:TEST:LEV WRITE,TSINPUT1,3,LOW |

#### 5.1.3.3 Creating and Programming Timing Sets Using the Plug & Play Driver

It takes three Plug & Play driver calls to program the timing set shown in Figure 5-7. The first driver shown in Figure 5-8 defines the timing set.

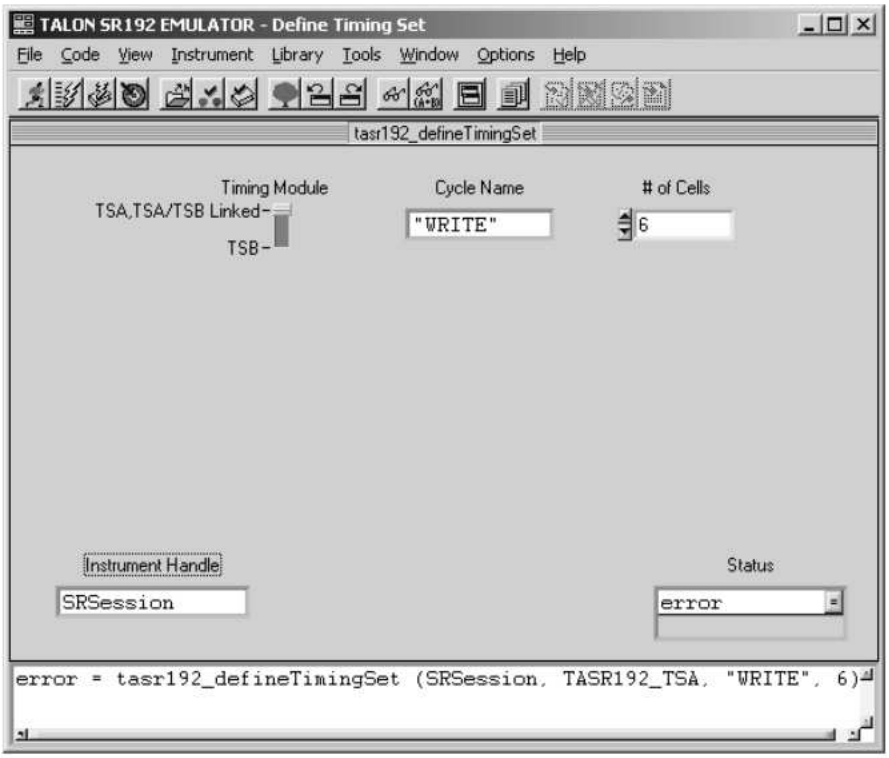



Figure 5-8 Plug & Play Timing Define



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The second driver shown in Figure 5-9 programs the timing cell memory.

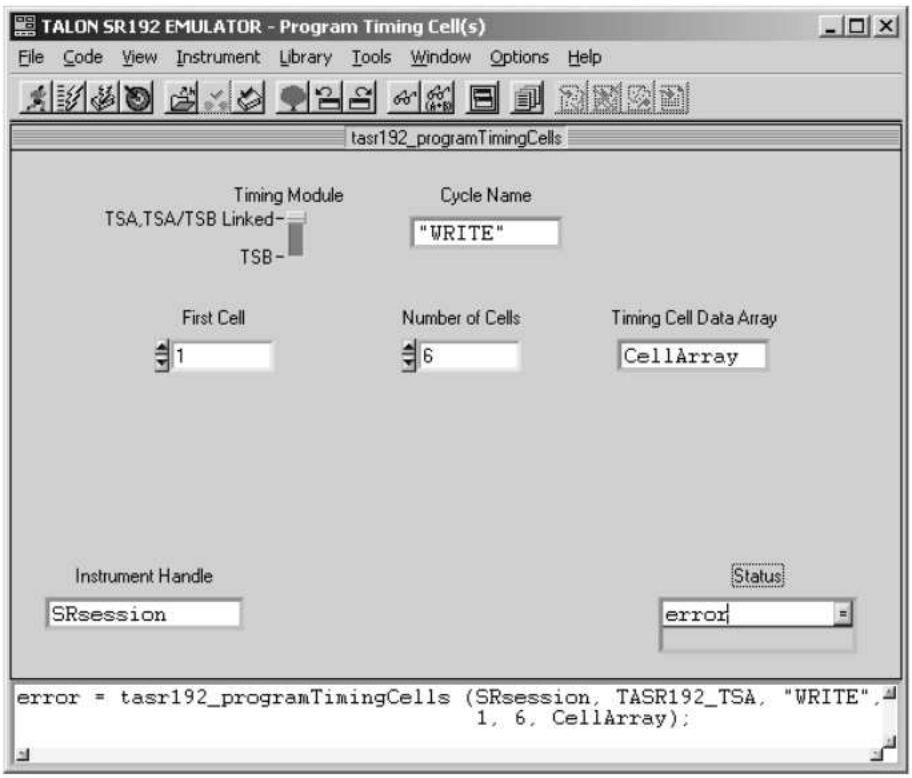



Figure 5-9 Plug & Play Program Timing Set



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The third driver programs the test cell and is shown in Figure 5-11.

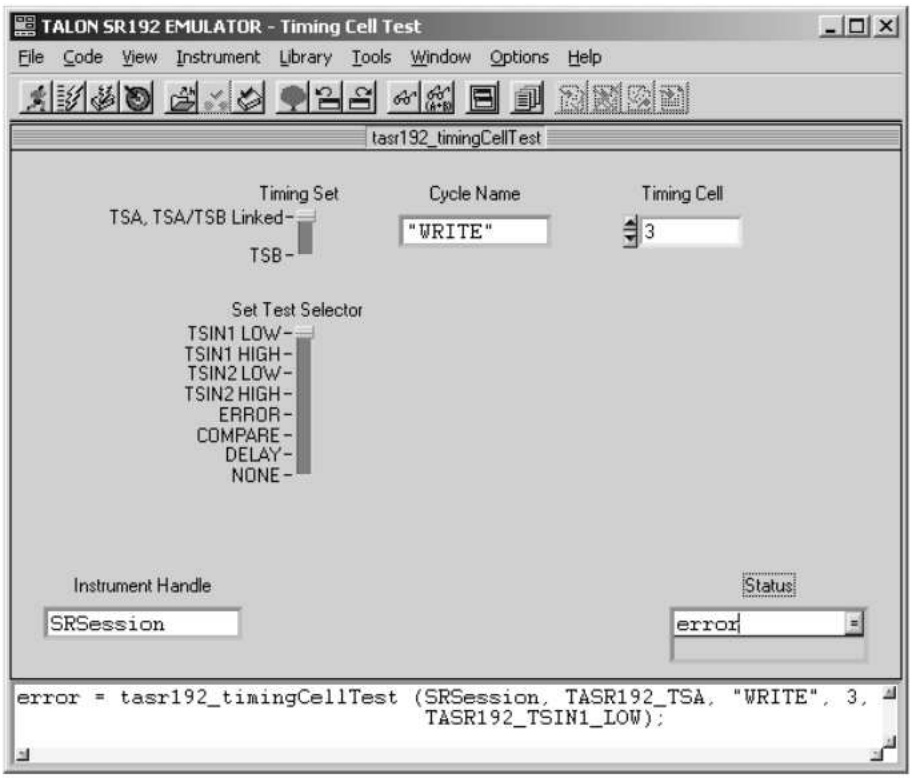



Figure 5-11 Plug & Play Timing Cell Test

## 5.2 Timing Generator Execution

Once the timing generator has been programmed with one or more timing sets, the next step would be to execute the timing set

While the SR101 can be viewed as a synchronous timing generator and word generator it is, in reality, a single state machine. Figure 5-10 shows the three states of the SR101.

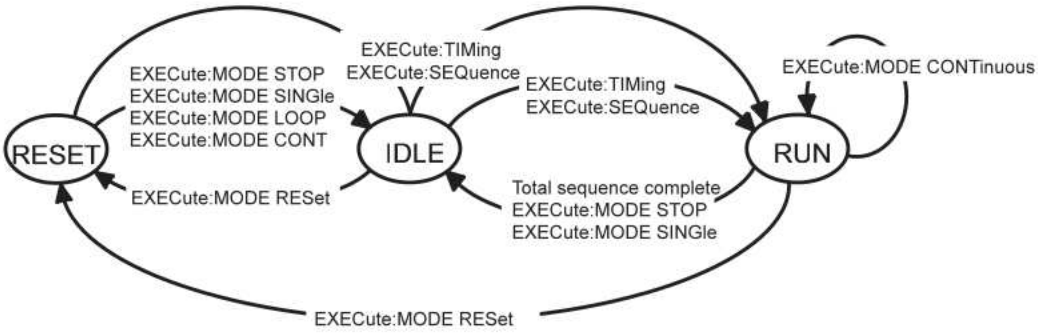



Figure 5-10 SR101 States

The three SR101 states are described below:

**Reset** The reset state is the power up default of the SR101. The reset state is active when the front panel LED labeled RUN is not illuminated. The module status register contains and IDLE bit for software queries. The following programming steps can be done while in the reset state.

1. Edit/query timing cell memory



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2. Edit/query I/O module stimulus/response memory
3. Edit/query sequence memory.

IDLE: The first timing set in each page is reserved and called IDLE. During the idle state, the IDLE timing set continuously runs. As shown in Figure 5-10, the only way to enter the run state is through the idle state. The idle state is active when the front panel LED labeled RUN is illuminated green. The module status register contains an IDLE bit for software queries. The following programming steps can be done while in the idle state.

1. Edit/query I/O module stimulus/response memory
2. Edit/query sequence memory

RUN: During the run state, the SR192 is either outputting stimulus data, recording response data or both. The run state is entered when a start signal is sent to the sequence logic. The sequence logic waits until the last cell of the IDLE cycle and then starts the specified sequence. The run state is active when the front panel LED labeled RUN is illuminated red. The module and instrument status register both contain a BUSY bit for software queries.

### 5.2.1 Timing Generator Execution Modes

Programming the execution mode can be done either by SCPI commands or by the Plug & Play driver. The Development Editor is an offline tool to configure, setup and define one or more SR192 Modules. The Execution Manager, included in the Development System package, is used to load the Development Editor file (called a project) to the hardware and then execute.

#### 5.2.1.1 Programming the Execution Mode Using SCPI Commands

The following SCPI commands program TSA execution mode:

1. Select TSA MODULE:SELECT TSA
2. Set the Single Mode EXECUTE:MODE SINGLE
3. Set the Continuous Mode EXECUTE:MODE CONTINUOUS
4. Set the Loop Mode EXECUTE:MODE LOOP,10

The previous example shows the three “RUN” modes (SINGLE< CONTINUOUS and LOOP), i.e., modes that define how the timing generator will run. The following examples illustrate the two stop modes:

1. Set the Stop Mode EXECUTE:MODE STOP
2. Set the Reset Mode EXECUTE:MODE RESET

The two stop modes stop the timing generator from running. STOP issues a stop pulse to the hardware which forces the timing generator to stop at the end of the next word.



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#### 5.2.1.2 Programming the Execution Mode Using the Plug and Play Driver

Figure 5-12 shows the Plug & Play driver for setting the execution mode.

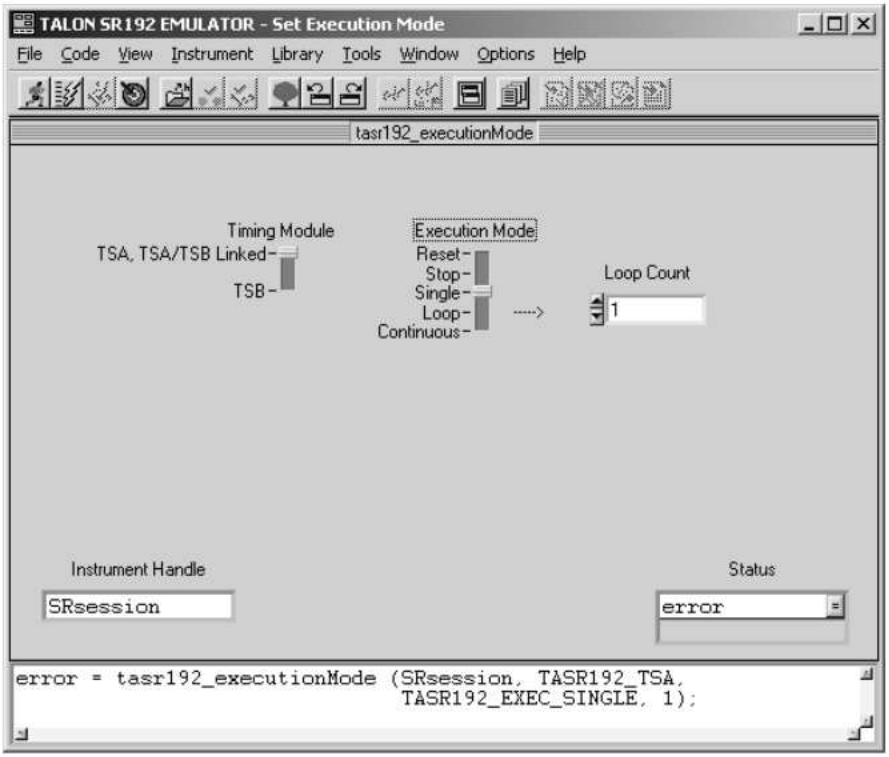



Figure 5-12 Plug & Play Execution Mode

### 5.2.2 Timing Generator Execution

The timing generator is executed by specifying a timing set and a range of Field Memory Addresses (FMA). The timing set will cycle for each FMA specified.

The FMA range can be specified as an absolute starting address and a size or as a pre-defined table. Table definition will be discussed in the section covering word generator programming.

#### 5.2.2.1 Timing Generator Execution Using SCPI Commands

The following SCPI commands program TSA execution mode:

1. Select TSA — MODULE:SELECT TSA
2. Set the Single Mode — EXECUTE:MODE SINGLE
3. Execute the Timing Set — EXECUTE:TIMING WRITE,1,1



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Using the timing set we defined in section 5.1.3, the following pattern, Figure 5-14 would be seen:

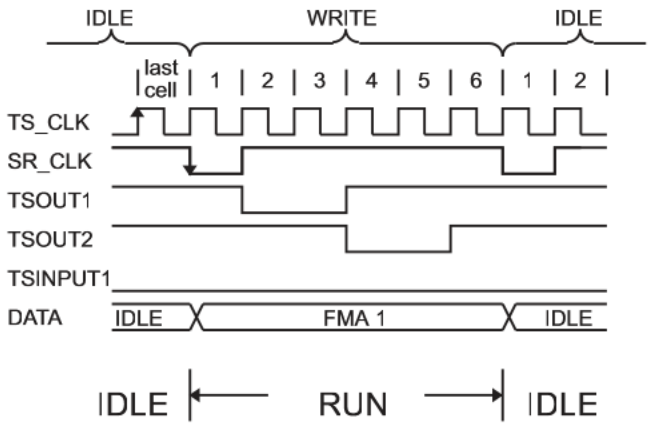



Figure 5-14 Timing Set Example, No Wait

Figure 5-14 shows the WRITE timing cycle with the TSINPUT1 signal always low. The following SCPI command will generate the pattern shown in Figure 5-13 where TSINPUT1 is not always low.

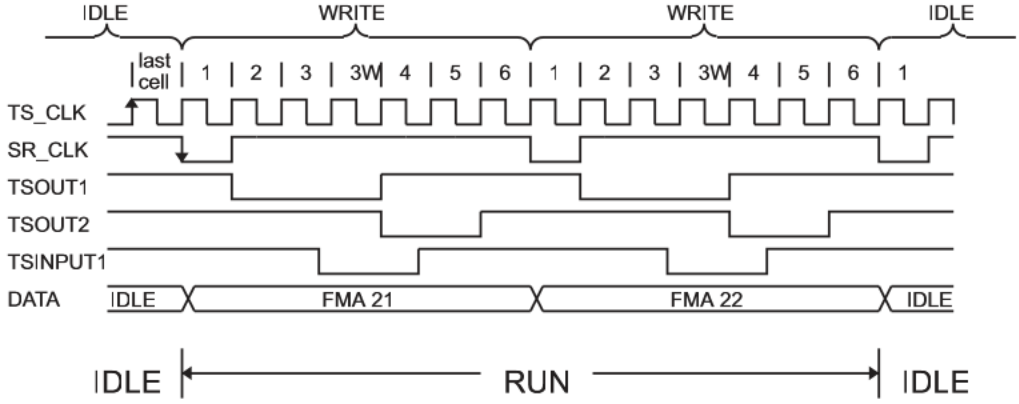



Figure 5-13 Timing Set Example, With Wait

Notice that in Figure 5-14 the FMA starts as one, and only one, cycle was executed. Figure 13 illustrates two cycles starting at FMA 21. The FMA address will increment by one, every falling edge of SR_CLK.



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#### 5.2.2.2 Timing Generator Execution Using the Plug and Play Driver

Figure 5-15 shows the Plug & Play driver used to execute a timing set.

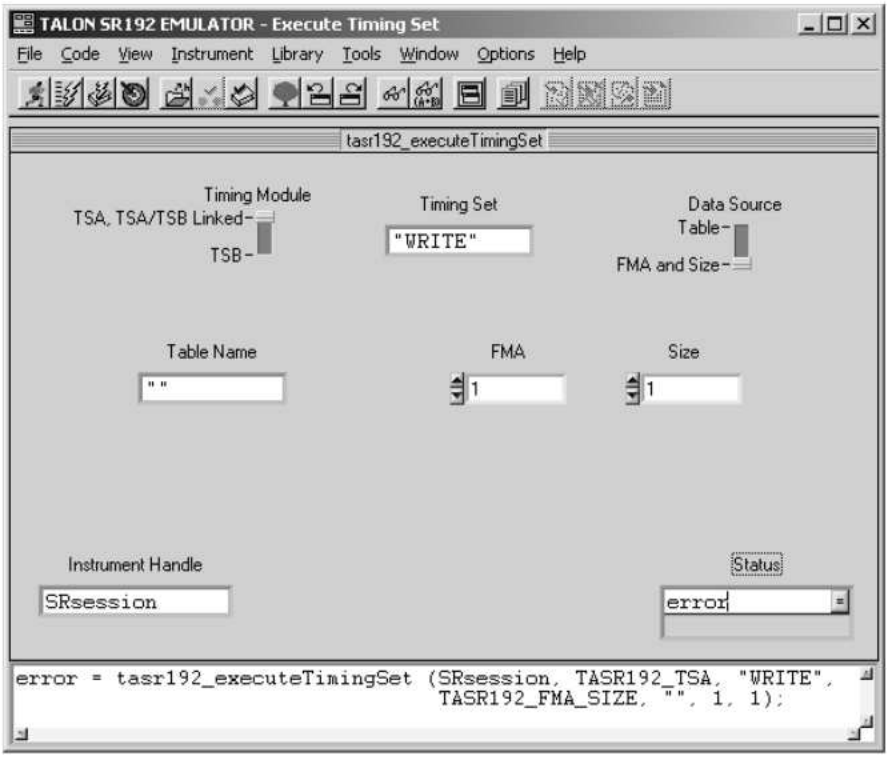



Figure 5-15 Plug & Play Execute Timing Set

## 5.3 Word Generator Programming

The word generator allows the user to output stimulus data, record response data or both.

The word generator is programmed into structures called a **SEQUENCE**. Each sequence is given a name and address into the sequence memory where that specific sequence begins. Each element of the sequence memory is called a **SUBSEQUENCE**. A sequence can be from 1 to 131071 subsequences, as long as the total number of subsequences does not exceed 131071.

Each subsequence is comprised of the following elements:

1. Timing Set Address
2. Table FMA
3. Subsequence Loop Count
4. Jump Code/Timing Set Address
5. Jump Subsequence Address
6. Control Flags

At a minimum, a timing set and a table are required to program a word generator sequence. Timing set programming was covered in Section 5.1. The following sections first describe creating a table followed by creating a sequence and programming the sequence memory.

### 5.3.1 Creating Word Generator Tables

A word generator table specifies a FMA (Field Memory Address) range. Each FMA element is referred to as a **WORD**. The FMA is broadcast to every I/O module and it addresses the stimulus/response memory. Multiple tables can be defined as long as the total number of words does not exceed 131072.



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Talon offers a program called the Table Editor that can be used to define word generator tables; however, the primary use of the Table Editor is to program the contents of the I/O modules memory. The following sections will provide examples using SCPI commands and Plug & Play drivers.

#### 5.3.1.1 Creating Word Generator Tables Using SCPI Commands

The following SCPI commands create a word generator table called DUMP that has sixteen words:

1. Select TSA — MODULE:SELECT TSA
2. Define the table — TABLE:DEFINE SUMP,16

The FMA range is assigned starting as zero. If DUMP is the first table defined, then FMA range is from 0 to 15. The next table defined will have a range starting at 16.

During the IDLE state, the data in the stimulus memory of each I/O module at FMA 0 is registered so that the I/O module stimulus memory can be modified without causing noise to the UUT.

#### 5.3.1.2 Creating Word Generator Tables Using the Plug and Play Driver

Figure 5-16 shows the Plug & Play driver used to create a table.

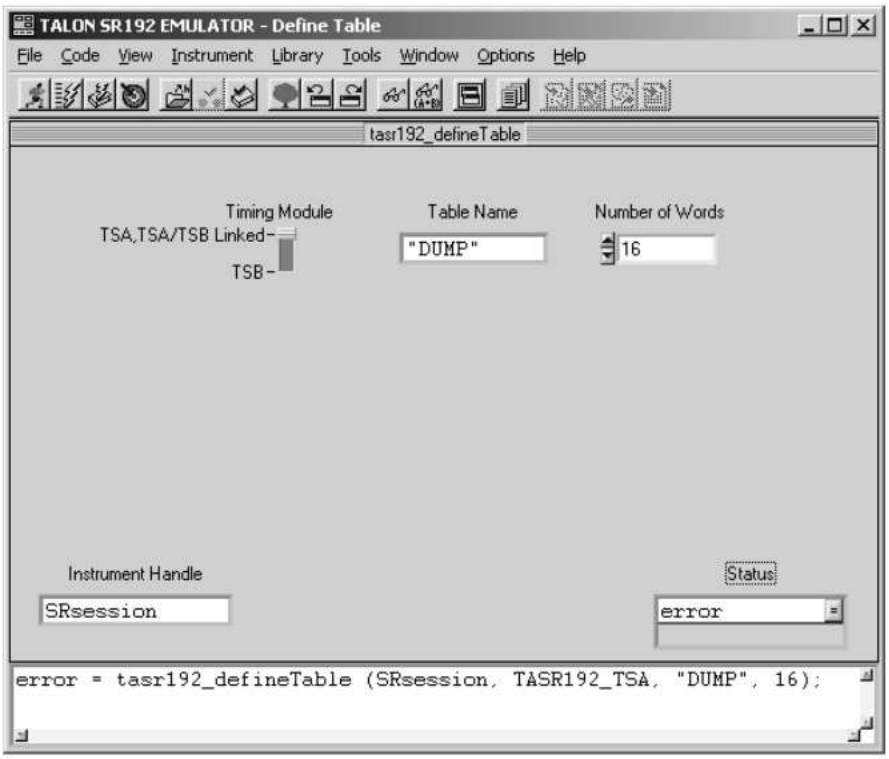



Figure 5-16 Plug & Play Define Table

### 5.3.2 Creating and Programming Sequences

Once a timing set and table have been programmed, a sequence can then be defined that associates the two structures together.



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Figure 5-18 defines and executes an SR101 execution sequence using a timing set with three cells and a table with five words using SCPI commands.

```
TIMING:DEFINE T1,3
TABLE:DEFINE D1,5
SEQUENCE:DEFINE S1,T1,D1
EXECUTE:SEQUENCE S1
```

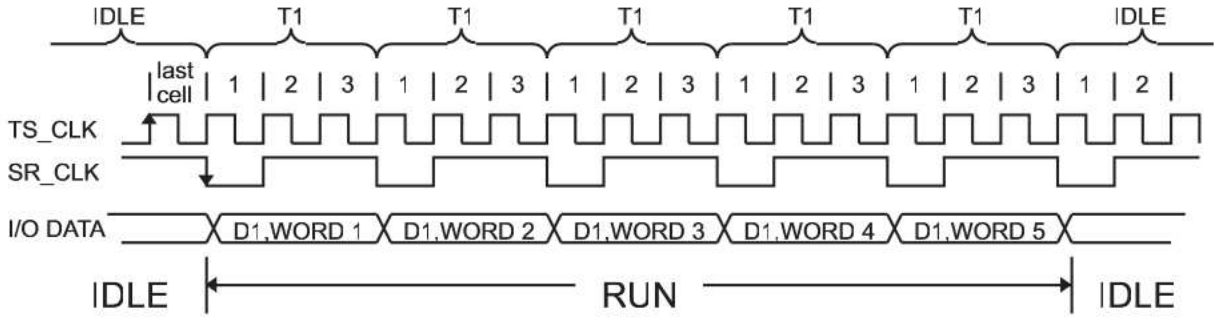



Figure 5-18 Sequence Example

The complete timing set will cycle from the first cell to the last cell for each word of the table. Figure 5-17 illustrates the Plug & Play driver for defining a sequence.

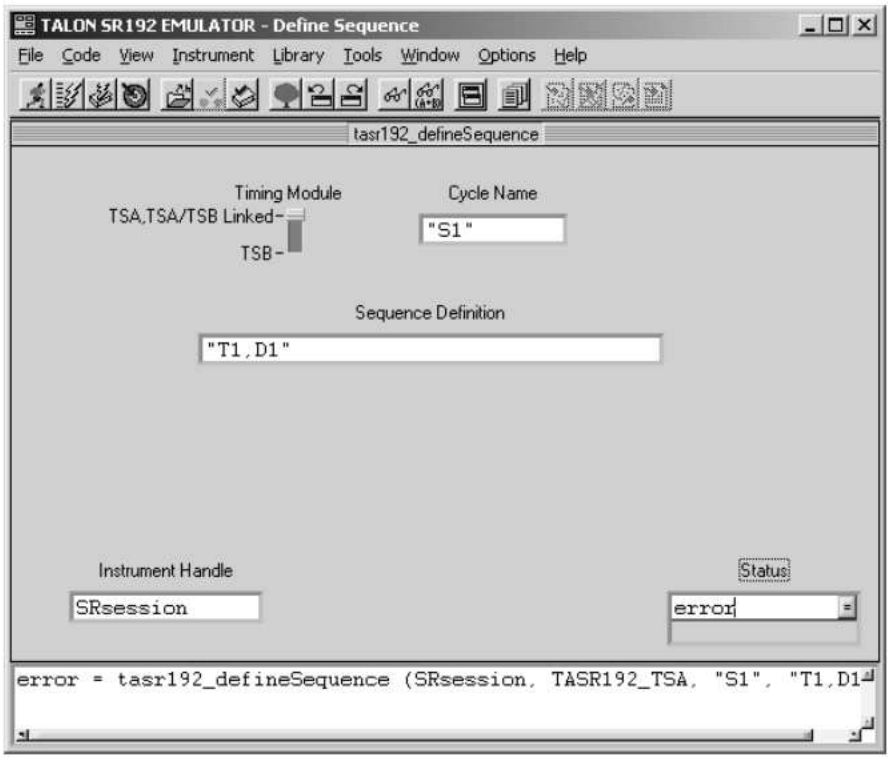



Figure 5-17 Plug & Play Define Sequence



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#### 5.3.2.1 Multiple Subsequence Definition

A sequence is not restricted to a single timing set and table. Multiple timing sets and tables can be defined and programmed into a sequence with multiple subsequences.

Figure 5-19 illustrates a sequence with three subsequences.

```
TIMING:DEFINE T1,5
TIMING:DEFINE T2,3
TIMING:DEFINE T3,4
TABLE:DEFINE D1,1
TABLE:DEFINE D2,2
TABLE:DEFINE D3,1
SEQUENCE:DEFINE S1,T1,D1,T2,D2,T3,D3
EXECUTE:SEQUENCE S1
```

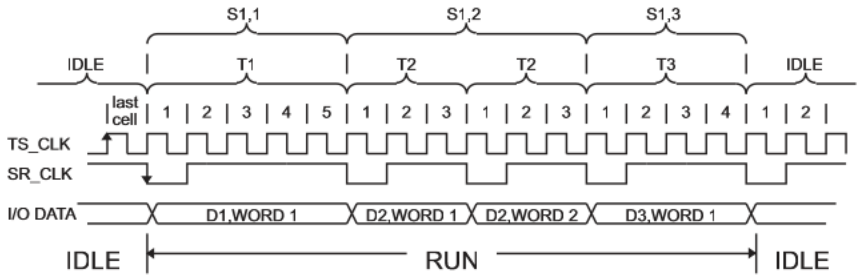



Figure 5-19 Multi Subsequence Sequence

Each transition from subsequence to subsequence is on the rising edge of TS_CLK.

#### 5.3.2.2 Sequence Looping

The entire sequence can be looped from 1 to 32768 times.

Figure 5-20 illustrates sequence looping.

```
TIMING:DEFINE T1,5
TIMING:DEFINE T2,3
TIMING:DEFINE T3,4
TABLE:DEFINE D1,1
TABLE:DEFINE D2,2
TABLE:DEFINE D3,1
SEQUENCE:DEFINE S1,T1,D1,T2,D2,T3,D3
EXECUTE:MODE LOOP,10
EXECUTE:SEQUENCE S1
```

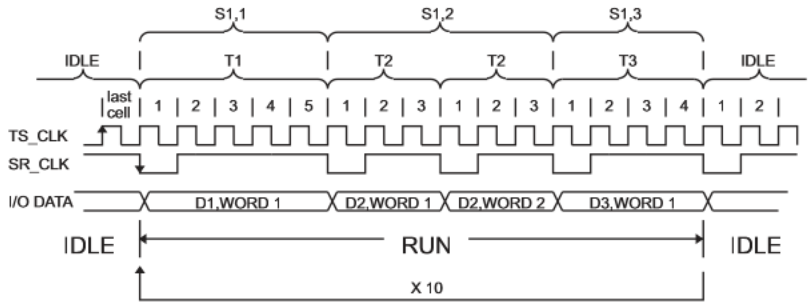



Figure 5-20 Sequence Looping

The sequence loops from the last word of the last subsequence to the first word of the first subsequence.



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### 5.3.2.3 Subsequence Looping

Subsequences can also be looped from 1 to 32768 times. Figure 5-22 illustrates subsequence looping.

```
TIMING:DEFINE T1,5
TIMING:DEFINE T2,3
TIMING:DEFINE T3,4
TABLE:DEFINE D1,1
TABLE:DEFINE D2,2
TABLE:DEFINE D3,1
SEQUENCE:DEFINE S1,T1,D1,T2,D2,T3,D3
SEQUENCE:LOOP S1,2,5
EXECUTE:SEQUENCE S1
```

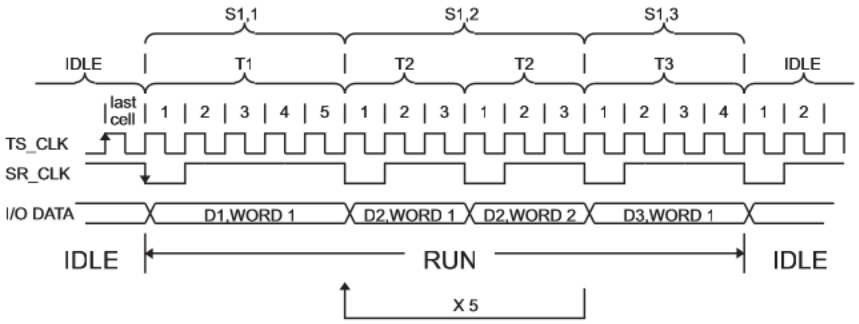



Figure 5-22 Subsequence Looping

The subsequence loop can also be specified when the sequence is defined. The following SCPI command defines the same sequence as shown in Figure 22:

SEQUENCE:DEFINE S1,T1,D1,1,T2,D2,5,T3,D3,1

Subsequences, as shown in Figure 22 are specified by giving the sequence name followed by an index starting at one. Subsequences are assigned consecutive addresses in the sequence memory.

### 5.3.2.4 Unconditional Sequence Jumping

The SR101 word generator normally transitions from subsequence to subsequence sequentially. Each subsequence can be programmed with a code that allows the user to program unconditional jumping from subsequence to subsequence. In addition, a control flag is available that allows each jump code to branch with return (**GOSUB**) or branch without return (**JUMP**).

A JUMP causes the first table word of the current subsequence to be executed and then the jump subsequence will become the current subsequence. Figure 5-21 shows an example of an unconditional jump.

```
TIMING:DEFINE T1,4
TIMING:DEFINE T2,3
TABLE:DEFINE D1,2
TABLE:DEFINE D2,2
SEQUENCE:DEFINE S1,T1,D1
SEQUENCE:DEFINE S2,T2,D2
SEQUENCE:JUMP S1,1,S2,1
EXECUTE:SEQUENCE S1
```

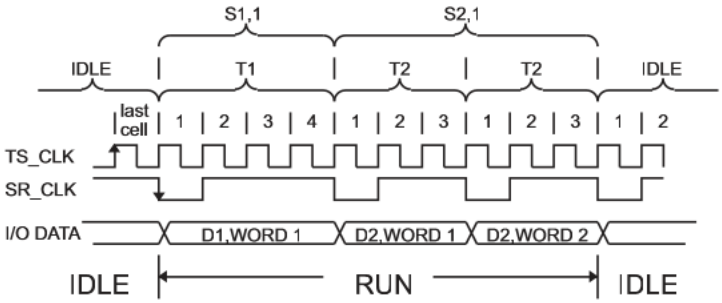



Figure 5-21 Unconditional Sequence JUMP



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A GOSUB causes the first table word of the current subsequence to execute. The gosub subsequence then executes. After the GOSUB subsequence executes its entire table, the next word of the current subsequence is executed. The GOSUB subsequence will be executed after every word of the current sequence. Figure 5-23 shows an example of an unconditional GOSUB.

```
TIMING:DEFINE T1,4
TIMING:DEFINE T2,3
TABLE:DEFINE D1,2
TABLE:DEFINE D2,2
SEQUENCE:DEFINE S1,T1,D1
SEQUENCE:DEFINE S2,T2,D2
SEQUENCE:GOSUB S1,1,S2,1
EXECUTE:SEQUENCE S1
```

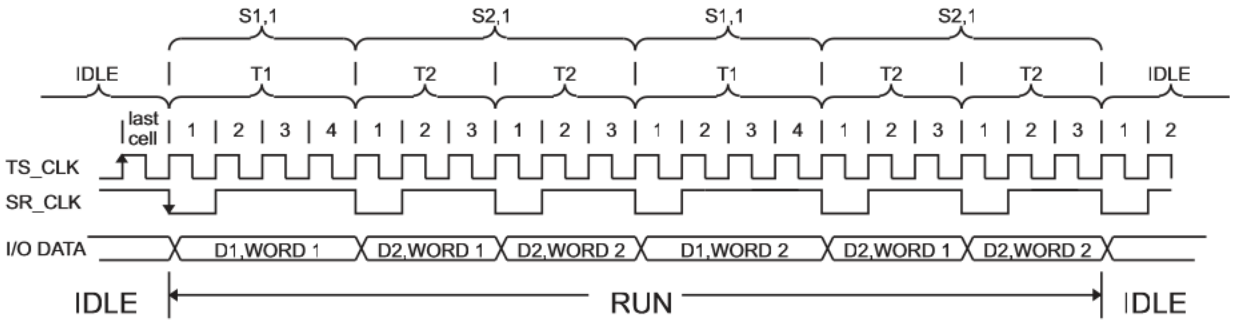



Figure 5-23 Unconditional Sequence GOSUB

A JUMP is performed at the end of the current table word, in the case where the return flag is set true (GOSUB), the specified JUMP subsequence is executed and then returns to the next word of the current subsequence.



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Figure 5-24 shows the Plug & Play Sequence Branch driver.

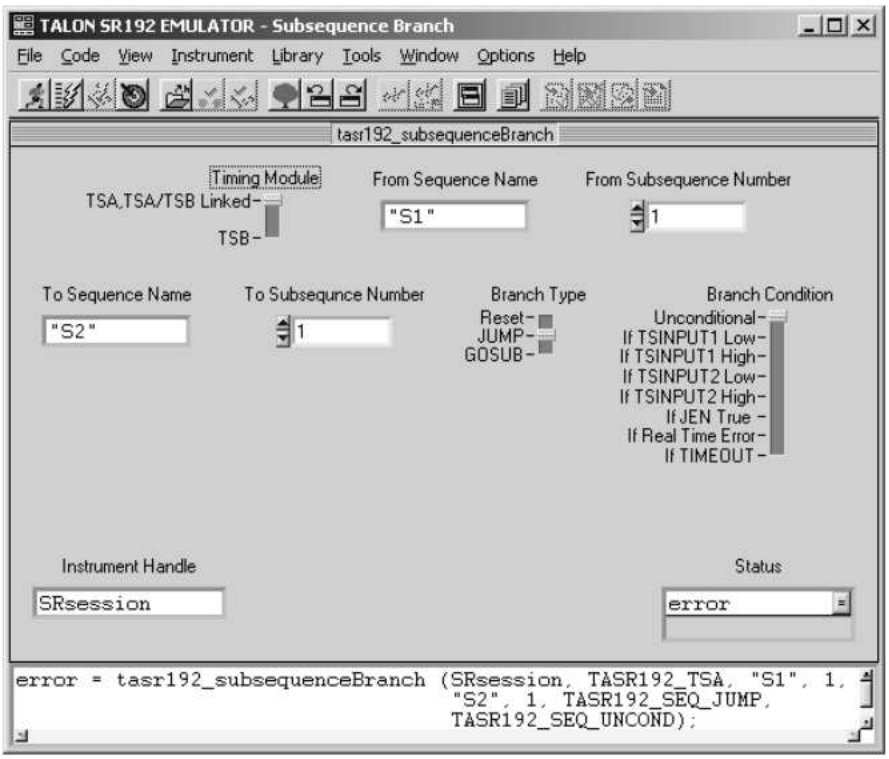



Figure 5-24 Plug & Play Sequence Branch

### 5.3.2.5 Conditional Sequence Branching

Conditional sequence branching works exactly the same as unconditional sequence branching except that the decision to jump is based on the following two events being true:

1. Jump Enable Bit Set True
2. Specified Test Condition is True

The jump enable bit can be set on or off for every word in a table. When a table is defined, all jump enable bits are set off. The following SCPI commands show an example of programming all the jump enable bits of a table on:

1. Define a table with 1024 words — TABLE:DEFINE TEST1,1024
2. Enable all Jump enable bits — TABLE:JENABLE TEST1,ALL

The following SCPI commands show an example of programming the jump enable bit for only the last word true:

1. Define a table with 10000 words — TABLE:DEFINE TEST2,10000
2. Disable all Jump enable bits — TABLE :JENABLE TEST2,NONE
3. Enable jump enable bit for the last word — TABLE:JENABLE TEST2,10000,ON

The test signal for conditional branching is sample on the rising edge of SR_CLK. A minimum of 40ns is required from the rising edge of SR_CLK to the end of the timing set for proper operations.

**Conditional testing with the timing generator running 50MHz requires a minimum of four cells.**

THE FOLLOWING EVENTS CAN BE TESTED:

1. TSINPUT1 Level
2. TSINPUT2 Level



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3. Raw Error Level
4. Cycle Timeout Status
5. Response Error

The jump code will be sample for every word in the subsequence whose jump enable bit is set true.

#### 5.3.2.6 Stopping a Subsequence

Each subsequence has a stop flag that can be on or off. Setting the stop flag on causes the subsequence to execute one word and the return to the IDLE state. The flag is used for trouble shooting sequence execution. The following SCPI commands program the stop flag:

1. Define a sequence with 3 Subsequences — SEQUENCE:DEFINE S1,T1,D1,T2,D2,T3,D3
2. Enable the stop flag for subsequence 2 — SEQUENCE:STOP S1,2,ON

#### 5.3.2.7 Editing a Subsequence

Once a sequence is defined with one or more subsequences, the user can redefine any of the subsequence parameters (Timing Set, Table, Loop Count) using the following commands:

1. Define a sequence with 2 subsequences — SEQUENCE:DEFINE S1,T1,D1,3,T2,D2,1
2. Edit the table for subsequence 2 to D3 — SEQUENCE:TABLE S1,2,D3
3. Edit the timing set for subsequence 1 to T3 — SEQUENCE:TIMING S1,1,T3
4. Edit the loop for subsequence 2 to 1000 — SEQUENCE:LOOP S1,2,1000

The jump code for a subsequence can be set to another code or reset using the following commands:

1. Define a sequence with 2 subsequences — SEQUENCE:DEFINES1,T1,D1,3,T2,D2,1
2. Define a sequence with 1 subsequences — SEQUENCE:DEFINE S2,T3,D3
3. Program a jump from S1,2 to S2,1 — SEQUENCE:JUMP S1,2,S2,1
4. Re-program jump to gosub — SEQUENCE:GOSUB S1,2,S2,1
5. Reset to no jump — SEQUENCE:RESET S1,2



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# 6 SR192 Timing Module Applications

The following sections describe common applications involving SR192 Timing Modules.

## 61 SR101 Module Status

Every Timing and I/O module returns a status word using the following commands:

1. Select the timing module — MODULE:SELECT TSA
2. Query the status — MODULE:STATUS?

The following table describes the returned data:

| Bits | Description |
|---|---|
| Bit 0 | Power on/self test pass/fail bit. 1-pass, 0-fail |
| Bit 1 | Idle Flag. 1-not idle stata, 0-idle state |
| Bit 2 | Run Flag. 1-not run state, 0-run state |
| Bit 3 | Wait Flag. 1-not waiting, 0-waiting |
| Bit 4 | Timeout Flag. 1-timeout true, 0-timeout false |
| Bit 5 | Real Time Error Flag. 1-error, 0-no error |
| Bit 6 | Not Used |
| Bit 7 | Synchronous Command Fail. 1-fail, 0-pass |
| Bits 8-15 | ID byte, SR1-ID=hex 9 |

Table 6-1 SR101 Status Register Description

## 62 Synchronizing Timing Set A and Timing Set B

When it is required to synchronize channels 1 through 96 with channels 97 through 192, the timing sets must be synchronized. This is accomplished by executing the following SCPI commands:

1. Select TSB — MODULE:SELECT TSB
2. Link TSB to TSA — MODULE:LINK ON

TSB must be linked to TSA prior to any table or timing sets being defined or timing generator parameters being programmed.

After linking TSB to TSA, TSA is automatically selected.

When linked, the two timing modules operate under the following rules:

1. SR101 modules cannot be linked to SR100 modules.
2. Both timing modules use the same clock source.
3. Timing sets will have the exact same number of cells.
4. The DELAY COURT will have the same delay value.
5. The CYCLE TIMEOUT will have the same value.
6. Timing test cells will have the same test code in the same test cell.
7. Tables will be defined for both timing modules.
8. Sequences will be defined for both timing modules.

When both timing sets test TSINPUT1, the input is guaranteed to meet the setup time to both timing modules.



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**WARNING**
**When the timing modules are linked, TSINPUT1A is synchronized with the timing set clock and connected to both TSA and TSB. TSINPUT1B is not used. TSINPUT2A and TSINPUT2B are not synchronized and could cause the timing modules to become unsynchronized if not synchronized externally with CLOCKA or CLOCKB.**

Each timing set may test its respective TSINPUT2 test signal, with the following restrictions.

1. The TSINPUT2A and TSINPUT2B signals must be tied together externally.
2. The TSINPUT2 common signal must be stable 2 cells (2 TS_CLK's) prior to the test cell.

The synchronize command "ANDs" the ERROR and RAW ERROR signals from the I/O modules to create a 192 channel ERROR and RAW ERROR signal. When the linked timing modules test the ERROR or RAW ERROR signal, they are actually testing the compare results of all 192 input channels.

In general, when TSA and TSB are linked, they can be thought of as a single timing module.

## 63 Linking Multiple SR192's

Multiple SR192's can be linked together in a master/slave mode where one SR192 generates the control signals for one or more additional SR192's.

The following SCPI commands setup the SR192 as a master:

1. Set the master mode on — OUTPUT:MASTER ON

The following SCPI commands setup the SR192 as a slave:

1. Select TSA — MODULE:SELECT TSA
2. Set link mode on — MODULE:LINK ON

The SR192 master generates the following signals to the SR192 slaves through the front panel J7 connector:

1. EXCLKM — TS_CLK selection
2. STARTM — Sequence start pulse
3. STOPM — Sequence stop pulse
4. SYNCM — Sequence sync pulse
5. TSINPUTM — Synchronized test input signal

All the SR192's are connected to the following two open collector signals through the front panel J7 connector:

1. ERROR — I/O module real time error signal
2. COMPARE — I/O module raw compare signal

When master/slave mode is enabled, the SR192's operate under the following rules:

1. Timing modules of all SR192's must be the same.
2. Only one master SR192 in the master/slave chain.
3. The master SR192 must be enabled prior to programming the slave SR192's.
4. Timing sets of all SR192's must be defined identical to each other.
5. The DELAY COUNT will have the same delay value.
6. The CYCLE TIMEOUT will have the same value.
7. Timing test cells will have the same test code in the same test cell.
8. Tables of all SR192's must have the exact same number of words.
9. Sequences of all SR192's must be identical.
10. All slaves must be executed (armed) prior to master execution.
11. Slaves can only be stopped by the master.



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12. All slaves must be armed prior to the master going into the idle state.

**WARNING**

**When the master/slave mode is enabled, TSINPUT1A of the master SR192 is synchronized with the timing set clock and broadcast to the slave SR192's. All other TSINPUTS are not synchronized and could cause the master/slave system to become unsynchronized.**



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# Appendix A Glossary of Terms

| | |
|---|---|
| A16/A24/A32 | The VXI address is segmented into three separate areas by a group of VXI signals called the address modifiers (AM0-AM5). These three areas are called A16, A24 and A32. Every VXI module is mapped into 64 bytes of the A16 memory. VXI modules, in addition, may request additional memory map space in the A24 or A32 space. The SR192 maps all the Timing and I/O modules registers into the A24/A32 space. |
| ADEL_CLK | Address Delay Clock. This signal, generated by the timing generator, clocks the response address delay register on the I/O modules. |
| CELL | A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK. |
| FMA | Field Memory Address. This group of signals is generated by the word generator and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word. |
| FUNCTION CODE(FC) | Each module in a SR192 is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module. |
| I/O MODULE | Any of Talon's Stimulus/Response modules for the SR192. |
| RESPONSE | The response data of the SR192 is comprised of EXPECT, MASK and RECORD memory in five memory I/O modules and just RECORD memory in three memory I/O modules. |
| SEQUENCE | A sequence is the link between the timing sets and the tables. |
| SR_CLK | Stimulus/Response Clock. This signal, generated by the timing generator, clocks the word generator. |
| STIM_LOAD | Stimulus Load. This signal, generated by the timing generator, loads data from the output and tristate memories into the output registers on the I/O modules. |
| STIMULUS | The stimulus data of the SR192 is comprised of OUTPUT and TRISTATE memory located on the I/O modules. |
| SUBSEQUENCE | A subsequence is a single element of a sequence. A subsequence selects a timing set, table, loop count, jump condition and control flags. |
| TABLE | A table is the structure that defines a FMA range for the subsequence. The FMA range is broadcast to all the I/O modules connected to the timing module. |
| TIMING MODULE | Any of Talon's Timing Modules for the SR192. |
| TIMING SET | A timing set is the structure that is created that defines the stimulus/response timing. Four pages of sixteen timing sets can be defined. |
| TRANSFER | See WORD. |



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| | |
|---|---|
| TS_CLK | Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK. |
| TSENABLE1 | Timing Set Enable One. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight. |
| TSENABLE2 | Timing Set Enable Two. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight. |
| TSINPUT1 | Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT1A is routed to TSA INPUT1, TSINPUT1B is routed to TSB INPUT1. |
| TSINPUT2 | Front panel test input signal input. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT2A is routed to TSA INPUT2, TSINPUT2B is routed to TSB INPUT2. |
| TSOUT1 | Timing Set Output One. General purpose output channel generated by the timing generator. |
| TSOUT2 | Timing Set Output Two. General purpose output channel generated by the timing generator. |
| TSOUT3 | Timing Set Output Three. General purpose output channel generated by the timing generator. |
| TSOUT4 | Timing Set Output Four. General purpose output channel generated by the timing generator. |
| TSOUT5 | Timing Set Output Five. General purpose output channel generated by the timing generator. |
| TSSTROBE1 | Timing Set Strobe One. This signal, generated by the timing generator, can be selected to strobe the response data into the input registers in groups of eight.. |
| TSSTROBE2 | Timing Set Strobe Two. This signal, generated by the timing generator, can be selected to strobe the response data into the input registers in groups of eight. |
| VECTOR | See WORD. |
| WORD | A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192. |



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# Appendix B SR101 Function Code Map

Module ID:

Hex 9

Address Location:

Timing Module TSA base address is located at hex 0x100000

Timing Module TSB base address is located at hex 0x180000

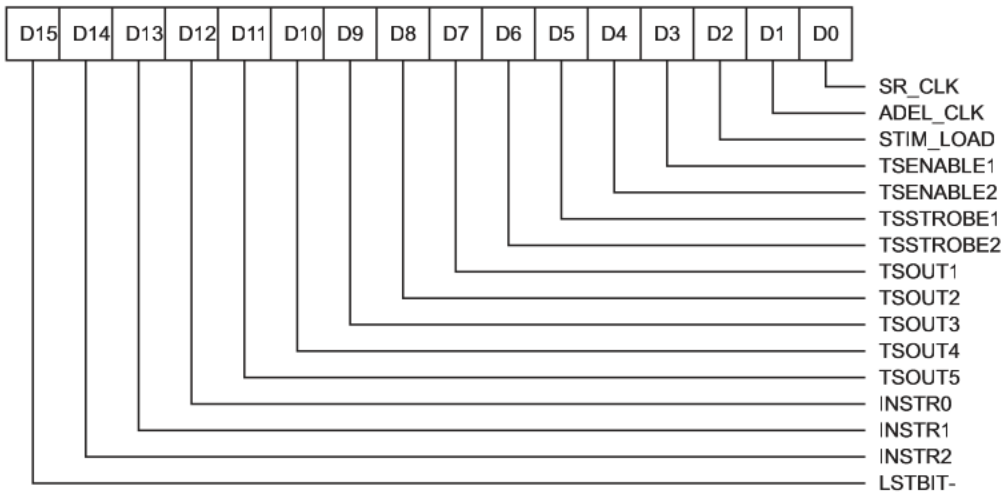
Function Code Assignments:

FC0 Read/write timing set memory.
The timing set memory is organized in an 8K by 16 bit array. Each timing set is programmed from 1 to 256 cells. Word access only. The timing memory is split into 4 pages.

Each memory location is referred to as a cell.

| PAGE1 | | PAGE2 | | PAGE3 | | PAGE4 | |
|---|---|---|---|---|---|---|---|
| TS0 | BASE + 0x0 | TS0 | BASE + 0x0 | TS0 | BASE + 0x0 | TS0 | BASE + 0x0 |
| TS1 | BASE + 0x200 | TS1 | BASE + 0x200 | TS1 | BASE + 0x200 | TS1 | BASE + 0x200 |
| TS2 | BASE + 0x400 | TS2 | BASE + 0x400 | TS2 | BASE + 0x400 | TS2 | BASE + 0x400 |
| TS3 | BASE + 0x600 | TS3 | BASE + 0x600 | TS3 | BASE + 0x600 | TS3 | BASE + 0x600 |
| TS4 | BASE + 0x800 | TS4 | BASE + 0x800 | TS4 | BASE + 0x800 | TS4 | BASE + 0x800 |
| TS5 | BASE + 0xA00 | TS5 | BASE + 0xA00 | TS5 | BASE + 0xA00 | TS5 | BASE + 0xA00 |
| TS6 | BASE + 0xC00 | TS6 | BASE + 0xC00 | TS6 | BASE + 0xC00 | TS6 | BASE + 0xC00 |
| TS7 | BASE + 0xE00 | TS7 | BASE + 0xE00 | TS7 | BASE + 0xE00 | TS7 | BASE + 0xE00 |
| TS8 | BASE + 0x1000 | TS8 | BASE + 0x1000 | TS8 | BASE + 0x1000 | TS8 | BASE + 0x1000 |
| TS9 | BASE + 0x1200 | TS9 | BASE + 0x1200 | TS9 | BASE + 0x1200 | TS9 | BASE + 0x1200 |
| TS10 | BASE + 0x1400 | TS10 | BASE + 0x1400 | TS10 | BASE + 0x1400 | TS10 | BASE + 0x1400 |
| TS11 | BASE + 0x1600 | TS11 | BASE + 0x1600 | TS11 | BASE + 0x1600 | TS11 | BASE + 0x1600 |
| TS12 | BASE + 0x1800 | TS12 | BASE + 0x1800 | TS12 | BASE + 0x1800 | TS12 | BASE + 0x1800 |
| TS13 | BASE + 0x1A00 | TS13 | BASE + 0x1A00 | TS13 | BASE + 0x1A00 | TS13 | BASE + 0x1A00 |
| TS14 | BASE + 0x1C00 | TS14 | BASE + 0x1C00 | TS14 | BASE + 0x1C00 | TS14 | BASE + 0x1C00 |
| TS15 | BASE + 0x1E00 | TS15 | BASE + 0x1E00 | TS15 | BASE + 0x1E00 | TS15 | BASE + 0x1E00 |

Timing Set Memory Pages




Timing Set Memory Bits

SR_CLK Sequence Address Clock (inverted)

ADEL_CLK Input Address Delay Register Clock (inverted)



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| | |
|---|---|
| STIM_LOAD | Internal Output Clock (inverted) |
| TSENABLE1 | Internal Output Enable 1 (inverted) |
| TSENABLE2 | Internal Output Enable 2 (inverted) |
| TSSTROBE1 | Internal Input Strove 1 (inverted) |
| TSSTROBE2 | Internal Input Strobe 2 (inverted) |
| TSOUT1 | General Purpose Timing Output Bit 1 |
| TSOUT2 | General Purpose Timing Output Bit 2 |
| TSOUT3 | General Purpose Timing Output Bit 3 |
| TSOUT4 | General Purpose Timing Output Bit 4 |
| TSOUT5 | General Purpose Timing Output Bit 5 |
| INSTR0 | Test Instruction Code Bit 1 |
| INSTR1 | Test Instruction Code Bit 2 |
| INSTR2 | Test Instruction Code Bit 3 |
| LSTBIT- | Last Timing Cell Flag |

| SELTST2 FC5 | SELTST1 FC5 | INSTR2 | INSTR1 | INSTR0 | TEST DESCRIPTION |
|---|---|---|---|---|---|
| X | 0 | 0 | 0 | 0 | WAIT UNTIL TSINPM LOW |
| X | 1 | 0 | 0 | 0 | WAIT UNTIL TSINP1 LOW |
| X | 0 | 0 | 0 | 1 | WAIT UNTIL TSINPM HIGH |
| X | 1 | 0 | 0 | 1 | WAIT UNTIL TSINP1 HIGH |
| 0 | X | 0 | 1 | 0 | WAIT UNTIL TSINP2 FALLING EDGE |
| 1 | X | 0 | 1 | 0 | WAIT UNTIL TSINP2 LOW |
| 0 | X | 0 | 1 | 1 | WAIT UNTIL TSINP2 RISING EDGE |
| 1 | X | 0 | 1 | 1 | WAIT UNTIL TSINP2 HIGH |
| X | X | 1 | 0 | 0 | WAIT IF ERROR |
| X | X | 1 | 0 | 1 | WAIT UNTIL COMPARE |
| X | X | 1 | 1 | 0 | WAIT UNTIL DELAY DONE |
| X | X | 1 | 1 | 1 | NO WAIT |

FC1 Read/Write subsequence Field Memory Address (FMA). 128K by 16

Up to 128K subsequences can be programmed. Each FMA is eighteen bits, FMA0 through FMA17. FMA0 through FMA15 are programmed at this function code. FMA16 and FMA17 are programmed using function code eight.

FC2 Write sequence loop count

The timing sequence can be looped from 1 to 32768 times. The sequence can also be looped continuously. The LSW defines the loop count. Loop > 1 (two's compliment + 1 with bit 15 set low), loop = 1 (0xFFFF). Bit zero of the MSW is the continuous bit, 0= continuous.

FC3 Read/Write subsequence timing set/test code register. 128K by 16

| | |
|---|---|
| LOOP LSW | BASE + 0x0 |
| LOOP MSW | BASE + 0x2 |

Loop Count Register

Each subsequence will execute one of the sixteen timing sets within the current page. In addition each subsequence can branch to another subsequence unconditionally or conditionally.

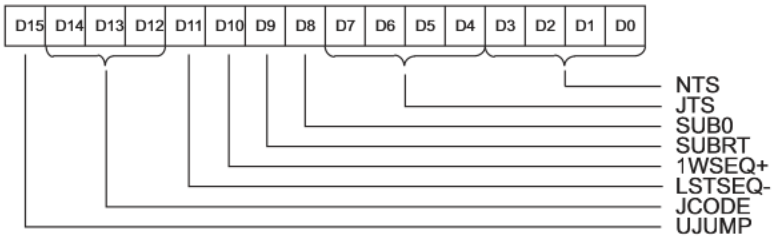
NTS Timing set number for next subsequence

JTS Timing set number for jump subsequence



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| | |
|---|---|
| LSTSEQ- | Last subsequence flag |
| SUB0 | Return to idle |
| SUBRT | Jump with return |
| 1WSEQ+ | This sequence is only one word |
| LSTSEQ- | Last Sequence Flag |
| JCODE | Sequence jump code (see table below) |
| UJUMP | Unconditional jump flag |




Timing Set Sequence Memory

| SELTST1F C5 | TESTEN FC13 | UJUMP | JUMP CODE | | | TEST DESCRIPTION |
|---|---|---|---|---|---|---|
| | | | TEST2 | TEST1 | TEST0 | |
| 0 | 1 | 0 | 0 | 0 | 0 | JUMP IF TSINPM LOW |
| 1 | 1 | 0 | 0 | 0 | 0 | JUMP IF TSINP1 LOW |
| 0 | 1 | 0 | 0 | 0 | 1 | JUMP IF TSINPM HIGH |
| 1 | 1 | 0 | 0 | 0 | 1 | JUMP IF TSINP1 HIGH |
| X | 1 | 0 | 0 | 1 | 0 | JUMP IF TSINP2 LOW |
| X | 1 | 0 | 0 | 1 | 1 | JUMP IF TSINP2 HIGH |
| X | 1 | 0 | 1 | 0 | 0 | JUMP IF ERROR |
| X | 1 | 0 | 1 | 0 | 1 | JUMP IF NOT ERROR |
| X | 1 | 0 | 1 | 1 | 0 | JUMP IF ERROR (NOT COMPARE) |
| X | 1 | 0 | 1 | 1 | 1 | JUMP IF TIMEOUT |
| X | X | 1 | X | X | X | UNCONDITIONAL JUMP |
| X | 0 | 0 | X | X | X | NO JUMP |

FC4 Read/Write jump subsequence register. 128K x 16

The jump subsequence register defines the sequence address (0-128K) for jumps, SA0 through SA17. SA0 through SA15 are programmed with this function code. SA16 and SA17 are programmed using function code eight.

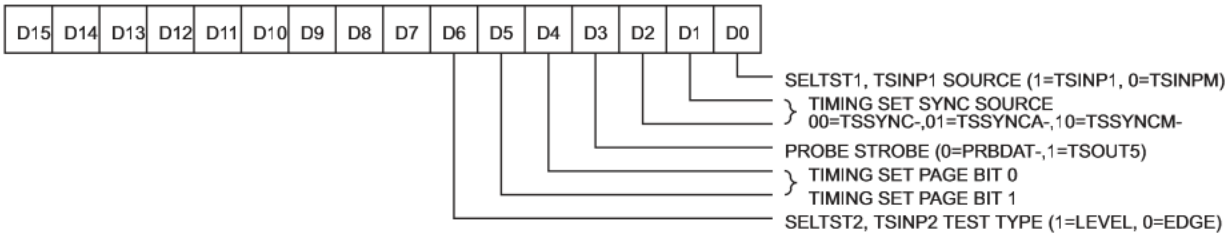
FC5 Write control register one.

Control register one has five program functions, program the TSINPUT1 source, program the timing set sync source, program the probe strobe



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source, program the timing page number and program the TSINPUT2 test type.




Timing Set Control Register One

FC6 Generate reset timing set (RESTS-)

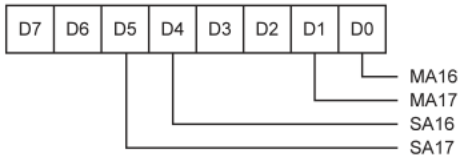
Unsynchronized command register clear (RES-T, RES-B). The power up reset, RESET-, also generates a TESTS- register clear.

FC7 Generate initialize clock (INITCK-)

Initialize command selects the internal 10MHz clock, generates a RES-B and at least one CLK+.

FC8 Set upper bits of FC1 and FC4 (128K x 8)

This memory is used in conjunction with FC1 and FC4 to program MA16 and MA17 for function code 1 and SA16 and SA17 for function code 4.

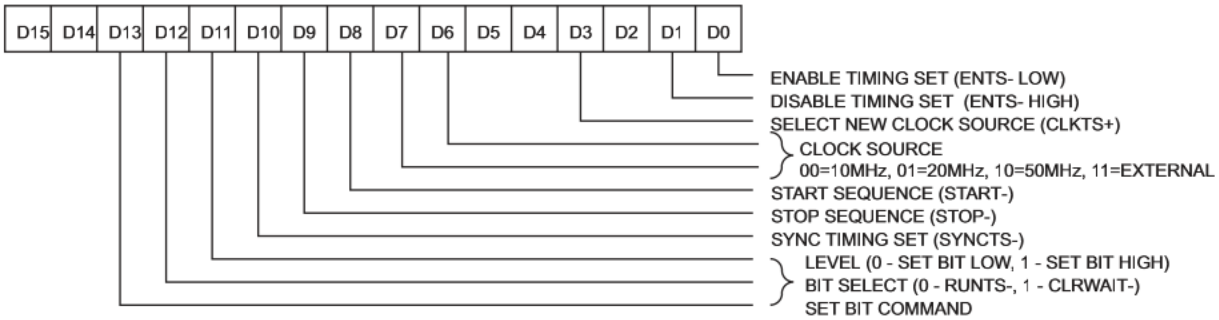



Function Code Eight Memory

FC9 Write control register two (SELCKT-)

Control register two is the sequence and timing set command register. These commands are synchronous with the selected timing set clock. Control register two is written with a single command at a time. The current command is cleared at the end of the command. Bit seven of the status/id register will be set to a one at the completion of any of the synchronous commands.

FC10 Generate prime timing set (IRPRIME-)




Timing Set Control Register Two

FC11 Write delay count (LDDLY-)



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The delay register is a sixteen bit counter and can be programmed from 0, no delay, to 32768 delay clocks. Delay>=1 (2's compliment), if delay >1). Bit fifteen low disables the delay function.

FC12 Write timeout count (LDTMOUT-)

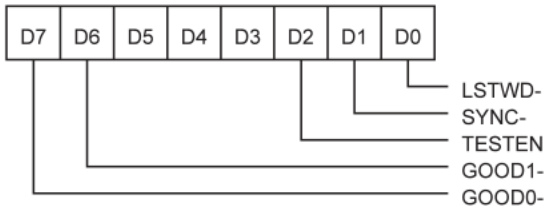
The timeout register is a sixteen bit register and can be programmed from 0 to 32768 clocks before a timeout is generated during a WAIT on input. The timeout can also be disabled. The LSW defines the timeout count. Timeout>1 (two's compliment + 1 with bit 15 set low), timeout = 1 (0xFFFF). Bit zero of the MSW is the disable bit, 0=disabled.

| | |
|---|---|
| TIMEOUT LSW | BASE + 0x0 |
| TIMEOUT MSW | BASE + 0x2 |

Timeout Register

FC13 Read/Write last word, sync, test enable and probe memory

The LSTWD-, SYNC- and TESTEN memory is located in an 4 by 128K memory that is set to output when RUN- is low. GOOD0-/GOOD1- probe memory is located in an 4 by 128K memory chip that is set to input when RUN- is low. Both memories are addressed by the FMA bus during RUN-.




LASTWD, SYNC, TESTEN and GOOD0, GOOD1 Memory

FC14 Read/Write subsequence loop counter (128K x 16)

Each subsequence can be looped from 1 to 32768 times.

FC15 Read status/ID-Write First Sequence register

The status/ID register is unique for each module and is described below.

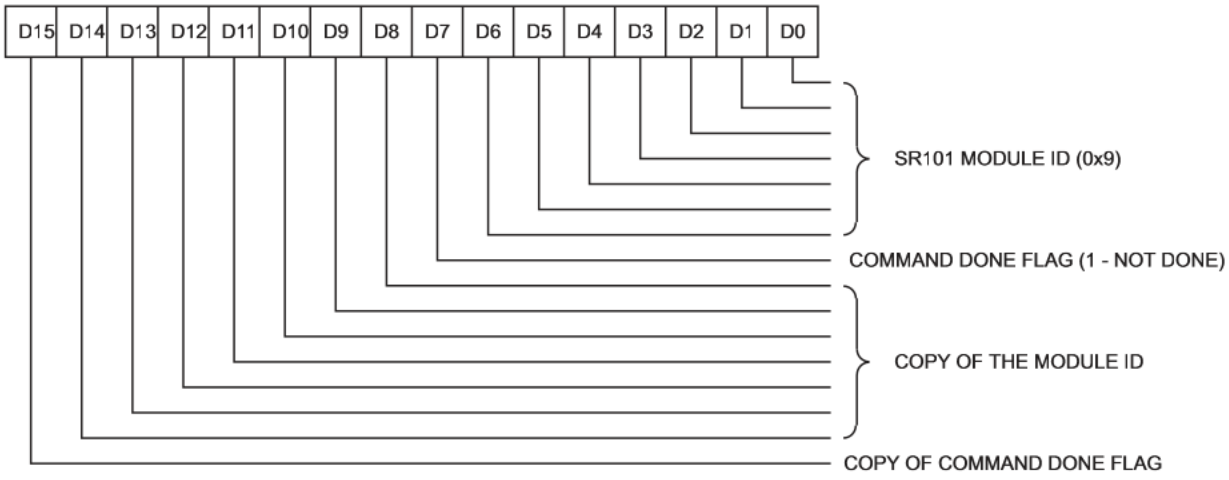
The first sequence register is a 22 bit register that holds the address and timing set number of the first sequence to be executed. The 22 bits are programmed with two 16 bit words.

FSA<0:17> First Sequence Address



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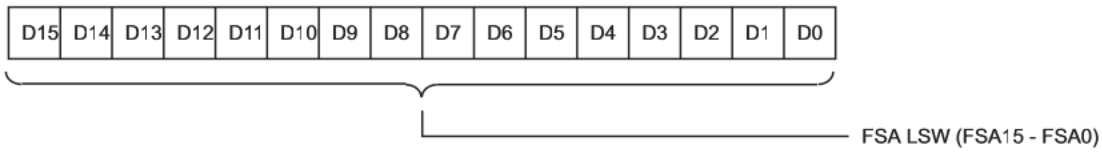
FTS First Timing Set

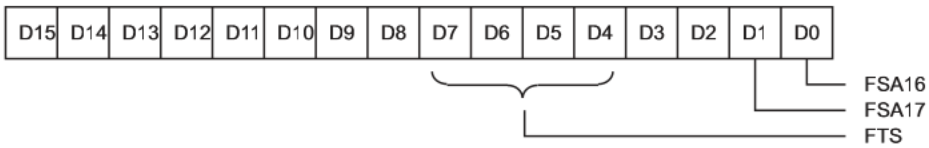



Function Code 15 Read

| | |
|---|---|
| FSA LSW | BASE + 0x0 |
| FSA MSW | BASE + 0x2 |

Function Code 15 Write




Function Code 15 Write



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# Appendix C SR101 Worksheets

The following worksheets are included:

1. Unlinked Timing Set
2. Linked Timing Set



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# SR192 TIMING SET WORKSHEET

Timing Set Name_____ Sheet__of___

| CELL | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | ' | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR_CLK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ADEL_CLK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| STIM_LOAD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSENABLE' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **LOW ORDER BITS** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSENABLE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSSTROBE1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSSTROBE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSOUT' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **MIDDLE BITS** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSOUT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSOUT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSOUT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSOUT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **HIGH ORDER BITS** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| BIN | HEX |
|---|---|
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |
| 1000 | 8 |
| 1001 | 9 |
| 1010 | A |
| 1011 | B |
| 1100 | C |
| 1101 | D |
| 1110 | E |
| 1111 | F |

TEST CONDITIONS

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSINPUT1 (H or L) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSINPUT2 (H,L, \ or /) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| WAIT ERROR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| WAIT ON NOT COMPARE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DELAY _____ CLOCKS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

NOTE: Default values are high or "1".

10/96



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## SR192 LINKED TIMING SET WORKSHEET

Timing Set Name _____

| CELL | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR_CLK | | | | | | | | | | | | | | | |
| ADEL_CLKA | | | | | | | | | | | | | | | |
| ADEL_CLKB | | | | | | | | | | | | | | | |
| STIM_LOADA | | | | | | | | | | | | | | | |
| STIM_LOADB | | | | | | | | | | | | | | | |
| TSENABLE1A | | | | | | | | | | | | | | | |
| TSENABLE2A | | | | | | | | | | | | | | | |
| TSENABLE1B | | | | | | | | | | | | | | | |
| **BYTE 1** | | | | | | | | | | | | | | | |
| TSENABLE2B | | | | | | | | | | | | | | | |
| TSSTROBE1A | | | | | | | | | | | | | | | |
| TSSTROBE2A | | | | | | | | | | | | | | | |
| TSSTROBE1B | | | | | | | | | | | | | | | |
| TSSTROBE2B | | | | | | | | | | | | | | | |
| TSOUT1A | | | | | | | | | | | | | | | |
| TSOUT2A | | | | | | | | | | | | | | | |
| TSOUT3A | | | | | | | | | | | | | | | |
| **BYTE 2** | | | | | | | | | | | | | | | |
| TSOUT4A | | | | | | | | | | | | | | | |
| TSOUT5A | | | | | | | | | | | | | | | |
| TSOUT1B | | | | | | | | | | | | | | | |
| TSOUT2B | | | | | | | | | | | | | | | |
| TSOUT3B | | | | | | | | | | | | | | | |
| TSOUT4B | | | | | | | | | | | | | | | |
| TSOUT5B | | | | | | | | | | | | | | | |
| NU | | | | | | | | | | | | | | | |
| **BYTE 3** | | | | | | | | | | | | | | | |

TEST CONDITIONS

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSINPUT1 (H or L) | | | | | | | | | | | | | | | |
| TSINPUT2 (H,L, ↘ or ↗) | | | | | | | | | | | | | | | |
| WAIT ON ERROR | | | | | | | | | | | | | | | |
| WAIT FOR COMPARE | | | | | | | | | | | | | | | |
| DELAY _____ CLOCKS | | | | | | | | | | | | | | | |



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