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REFERENCE MANUAL

Talon Instruments™

SR192

192-Channel Modular Digital Resource Module



Publication Date: 04/24/06
Publication Number: SROM114 Rev. A
Instrument Part Number: SR192

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This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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1 Introduction

The SR192 integrates both bus emulation and traditional stimulus/response capability in a single package. The SR192 provides the following features:

VERSATILE ARCHITECTURE....The SR192 is message based with A32 addressing for high speed downloading and retrieving of test data. In bus emulation mode channels are grouped in 8 pin groups as fields of 8, 16, 32, etc. In stimulus/response mode, each of the channels can be input or output (per pin architecture).

DENSITY....VXI space is at a premium, thus the SR192 was designed to pack the most dynamic digital capability in the smallest possible space.192 I/O channels with 128K bits per channel plus 20 additional timing and control signals are housed in a dual slot “C” size VXI module.

MODULARITY....The SR192 was designed as a motherboard/daughterboards arrangement. With this concept the user purchases the number and type of I/O channels needed for his test requirements. The system can easily be upgraded at a later time as test requirements change. Multiple SR192’s may be installed in a VXI chassis and linked in a master/slave configuration up to 1152 I/O channels.

DRIVER/RECEIVER VOLTAGE FAMILIES....The SR192 offers a variety of I/O daughterboards with options such as, TTL single-ended, 422/485 and ECL differential, variable voltage modules with ranges from +15V to -15V or +7V to -5V. Most modules can be mixed in a single SR192 to provide more flexibility for the user.

PROGRAMMING....The SR192 is a message based SCPI compatible module with A32 addressing capability. It is shipped with VXI Plug&Play drivers and soft front panel. Graphical editor software packages are available as options allowing an easy means of programming timing and stimulus data.

SR211 PROBE....The SR211 probe is 25MHz dual threshold data probe. It consists of an external pod, which houses all probe related electronics, and a standard X10 scope probe. This eliminates the high cost of maintenance and service associated with custom digital probes. Real time node status is visually shown via 5 LEDs located on the pod, (“Good One’, “Good Zero”, Tristate, Contact or Pulse signals are indicated). The SR211 features +/- 10Vdc threshold setting with 20mV resolution, static voltage reading and 128K bits of memory for data capture. The SR211 may be used in a manual mode with data capture initiated via a scope probe button or with the Millennia III prober in a fully automated mode.

1.1 Manual Layout

This manual contains technical information on the SR192 and all of its components.

The layout of this manual is in five sections described below:

1. Introduction	This section.
2. Specifications	Electrical and environmental specifications of the SR192.
3. Jumpers/Installation	Description of the jumpers and installation of the SR192.
4. Front Panel Connectors	Description and pin out of the front panel connectors.
5. Functional Description	Functional description of the SR192 hardware.

In addition, five appendices are included:

A. Glossary of Terms	Description of terms used in this manual.
B. Function Code Map	Hardware register description.
C. Power & Cooling	Power and cooling requirements and cable worksheets.
D. Signal Description	Front panel signal and termination descriptions.
E. SR192 Block Diagram	SR192 system block diagram.

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1.2 SR192 System

The SR192 system is comprised of the following components; front panel, motherboard, digital resource A and digital resource B as well as the following modules; TSIO, DAC/MFC and CPU/VXI.

1.2.1 Front Panel

The SR192 front panel provides the hardware interface to the UUT.

Section 4 lists the pinouts for the SR192 front panel connectors.

1.2.2 Motherboard

The motherboard PCB is a “C” sized VXI board which contains the connectors and headers required for routing signals to/from SR192 components. The motherboard also contains logic for recording real-time error data from digital resource A.

1.2.3 Digital Resource A

Digital resource A is comprised of the following module slots on the motherboard:

TSA	Timing module slot that generates the address and control signals for the I/O modules installed in slots DRA1 through DRA6.
DRA1	I/O module slot that contains the driver, receivers and memory for the front panel channels 1 through 16.
DRA2	I/O module slot that contains the driver, receivers and memory for the front panel channels 17 through 32.
DRA3	I/O module slot that contains the driver, receivers and memory for the front panel channels 33 through 48.
DRA4	I/O module slot that contains the driver, receivers and memory for the front panel channels 49 through 64.
DRA5	I/O module slot that contains the driver, receivers and memory for the front panel channels 65 through 80.
DRA6	I/O module slot that contains the driver, receivers and memory for the front panel channels 81 through 96.

1.2.4 Digital Resource B

Digital resource B is comprised of the following module slots on the motherboard:

TSB	Timing module slot that generates the address and control signals for the I/O modules installed in slots DRB1 through DRB6.
DRB1	I/O module slot that contains the driver, receivers and memory for the front panel channels 97 through 112.
DRB2	I/O module slot that contains the driver, receivers and memory for the front panel channels 113 through 128.
DRB3	I/O module slot that contains the driver, receivers and memory for the front panel channels 129 through 144.
DRB4	I/O module slot that contains the driver, receivers and memory for the front panel channels 145 through 160.
DRB5	I/O module slot that contains the driver, receivers and memory for the front panel channels 161 through 176.
DRB6	I/O module slot that contains the driver, receivers and memory for the front panel channels 177 through 192.

1.2.5 TSIO Module

The TSIO module is an L shaped assembly which is installed in the P35 connector of the motherboard. This board is used to convert timing set signals TSOUTA1, TSOUTA2, TSINPA1, TSINPA2, CLOCKA, EXCLK1 and FCNTL1 to various logic family levels that are compatible with Talon’s family of I/O modules.

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1.2.6 DAC/MFC Modules

The DAC module provides the following support logic for the SR192 system:

1. Reference levels for the variable voltage I/O modules.

The MFC module provides the following support logic for the SR192 system:

1. Reference levels for the variable voltage I/O modules.
2. Interface logic for the SR211 Probe Pod.
3. User programmable clocks routed to the digital resources and front panel.

1.2.7 CPU/VXI Modules

The CPU module resides in the last slot of the motherboard and communicates with the VXI backplane through the VXI module. It contains a Motorola 68HC000 microprocessor, FLASHRAM, system RAM, VXI interface logic and SR192 address map decoding logic. The CPU provides a SCPI format compatible parser to control data flow to/from the VXI controller and communication registers for the VXI protocol requirements. Many of the SR192 functions can also be programmed through VXI A32/A24 register access.

The FLASHRAM contains the SR192 operating system. Used in tandem with static memory it allows the operating system to be field upgradeable without hardware modification.

The SR192 operating system conforms to SCPI Version 1994.0 and IEEE-488.2 standard mandated commands.

The CPU communicates with the various modules via the address and data bus of the SR192 motherboard. The upper addresses form a module decode for each module slot. Along with the module decodes each slot has four function code lines F0 through F3. These function code lines enable each module to define 16 unique function codes. These codes are used to pass module ID, operating status and commands to/from the CPU or VXI bus.

The VXI module is a small daughter board which mates with the CPU module and connects to the VXI system backplane . This module is the link to the SR192 for all VXI communication. In addition to providing the hardware link to the VXI bus, it houses the system RAM for downloading operating system changes to the CPU FLASHRAM.

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2 Specifications

The following sections list the specifications of the SR192 module.

2.1 SR192 Motherboard

Number of digital I/O module slots 12
DRA1, DRA2, DRA3, DRA4, DRA5, DRA6, DRB1, DRB2, DRB3, DRB4, DRB5, DRB6
Number of timing module slots 2
TSA, TSB
Number of accessory module slots 1
DAC/MFC
VXI Bus
Message Based
A16/D16 Slave
A24/A32 Required Memory[1] 8M
IEEE-488.2 Instrument (I4)
Event Generation (EG)
Interrupter
Static/Dynamic Configuration[1]
TTLTRG Drive TSOUT3A
Digital I/O Slot Signals
Maximum number of I/O channels 192
I/O channel Termination .....See specific I/O module manual
Memory depth per I/O channel .....See specific I/O module manual
Number of control channels .....See specific I/O module manual
Control channel Termination .....See specific I/O module manual
Timing Slot Signals
Number of output trigger, handshake lines (TSOUT1-TSOUT5, SYNC) .....6 per slot
Output trigger, handshake termination[2] .....See section 3.6
Number of input trigger, handshake lines (TSINPUT1,TSINPUT2) .....2 per slot
Input trigger, handshake termination[3] .....See section 3.6
External I/O control inputs (FCNTL1, FCNTL2)[4] 2
External I/O control input termination[4] .....See section 3.6
External clock inputs (EXCLK1, EXCLK2)[5] 2
External clock input termination[2] .....See section 3.6
Selected clock output (CLOCKA, CLOCKB)[6] .....1 per slot
Selected clock output termination[6] .....See section 3.6
Busy flag output (TSABUSY, TSBBUSY) .....1 per slot
Busy flag output termination .....None
DAC/MFC Accessory Module Signals .....See specific accessory module manual
VXI Backplane Signals
Output Low Sink Current (TTLTRG0 - TTLTRG7, IRQ1 - IRQ7) .....24 mA

Note 1: Switch Selection
Note 2: TSOUTA1 and TSOUTA2 routed through TSIO, see section 3.4 and 5.7.1
Note 3: TSINPUTA1 and TSINPUTA2 routed through TSIO, see section 3.4 and 5.7.2
Note 4: FCNTL1 routed through TSIO, see section 3.4, 5.6, and 5.9
Note 5: EXCLK1 routed through TSIO, see section 3.4 and 5.5
Note 6: CLOCKA routed through TSIO, see section 3.4 and 5.5

2.2 Electrical

The following lists the electrical characteristics of the SR192 motherboard driver/receivers

TTL Signals
High Level Output Voltage .....2.4V min
High Level Source Current .....15 mA
Low Level Output Voltage .....0.4V max
Low Level Sink Current .....25 mA
Output Impedance (with 47Ω series terminator) .....80Ω typ
Short Circuit Protected .....Yes[1]
High Input Threshold .....2.0V min
Low Input Threshold .....0.8V max
Input Impedance .....82Ω typ

The following lists the electrical characteristics of the SR192 TSIO driver/receivers

TTL Signals
High Level Output Voltage .....2.4V min
High Level Source Current .....15 mA
Low Level Output Voltage .....0.4V max
Low Level Sink Current .....25 mA
Output Impedance (with 47Ω series terminator) .....80Ω typ
Short Circuit Protected .....Yes[1]
High Input Threshold .....2.0V min

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Low Input Threshold.....0.8V max
Input Impedance (Variable Voltage TSIO, V+/V- Applied).....> 10KΩ
Input Impedance (Variable Voltage TSIO, V+/V- Not Applied).....900Ω @ 3V typ
Input Impedance (Differential TSIO).....82Ω typ

RS-422 Differential Signals

Differential Driver Output Voltage (Unloaded).....5V max
Differential Driver Output Voltage (Loaded 27 ohm, RS-485).....1.5V min
Differential Driver Output Voltage (Loaded 50 ohm, RS-422).....2V min
Differential Receiver Threshold.....-2V min, +2V max
Differential Receiver Hysteresis.....70mV typ
Differential Receiver common mode range.....-7V to +12V
Input/Output Impedance.....120Ω

Variable Voltage Signals

High Level Output Voltage.....-5V to +15V[3]
High Level Source Current.....50 mA max
Low Level Output Voltage.....+5V to -15V[3]
Low Level Sink Current.....50 mA max
Voltage Swing.....20V max
AC Current (200 nsec max).....200 mA
Output Impedance (with 47Ω series termination).....50Ω typ
Output Slew Rate.....0.7V/ns typ[2]
Short Circuit Protected.....Yes
High Input Threshold.....-5V to +15V[3]
Low Input Threshold.....+5V to -15V[3]
Input Impedance.....30KΩ

Note 1: With 47Ω series terminator installed.
Note 2: User programmable (default values given).
Note 3: Range dependant on the V1+ and V1-

2.3 Timing Characteristics

Table 2-1 lists the timing characteristics of the SR192's timing module clock and control logic.

Description	Logic	From	To	Typ ns	Note
External Clock One Propagation.	TTL	EXCLK1	TS_CLKA	27	-
			TS_CLKB	31	-
	Variable Voltage	EXCLK1	TS_CLKA	32	-
			TS_CLKB	36	-
	Differential	EXCLK1	TS_CLKA	54	-
			TS_CLKB	57	-
External Clock Two Propagation.	TTL	EXCLK2	TS_CLK	22	-
Internal Clock to Timing Control Signals	TTL	TS_CLK	ADEL_CLK STIM_LOAD TSENABLE TSSTROBE	5-10	1
Internal Clock to New Pattern Address.	TTL	TS_CLK	FMA	12-15	1
Internal Clock to TSA Output Clock.	TTL	TS_CLK	CLOCKA	8	-
	Variable Voltage	TS_CLK	CLOCKA	11	-
	Differential	TS_CLK	CLOCKA	17	-
Internal Clock to TSB Output Clock.	TTL	TS_CLK	CLOCKB	4	-
External Field Control One Propagation.	TTL	FCNTL1	DRA/DRB	8-20	1
	Variable Voltage	FCNTL1	DRA/DRB	14-23	1
	Differential	FCNTL1	DRA/DRB	40-54	1
External Field Control Two Propagation	TTL	FCNTL2	DRA/DRB	8-20	1
TSA Input Handshake/Trigger Signals	TTL	TSINPUT1/2A	TSA	5-7	1
	Variable Voltage	TSINPUT1/2A	TSA	12-13	1
	Differential	TSINPUT1/2A	TSA	39-43	1
TSB Input Handshake/Trigger Signals	TTL	TSINPUT1/2B	TSB	12-20	1
TSA Output Handshake/Trigger Signals	TTL	TS_CLKA	TSOUTA	10	-
	Variable Voltage	TS_CLKA	TSOUTA	16	-
	Differential	TS_CLKA	TSOUTA	20	-
TSB Output Handshake/Trigger Signals	TTL	TS_CLKB	TSOUTB	10	-

Note 1: Range of delay accounts for the number of modules installed and edge variations.

Table 2-1 SR192 Motherboard Clock Timing

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2.4 Environmental

Temperature Range

Operating .....0° C to +50° C
Storage .....-40° C to +70° C (RH not controlled)

Altitude

Operating .....Sea level to 10,000 ft.
Storage .....Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C.....not controlled
+11°C to +30°C.....95+/-5%RH
+31°C to +40°C.....75+/-5%RH
+41°C to +50°C.....45+/-5%RH

2.5 Size

Dimension

Dual slot, “C” size VXI module. Approx. 26.22 cm x 6.09cm x 36.63 cm (10.325” x 2.4” x 14.42”)

Weight

< 1.81kg (4.0 lbs.)

2.6 Power Requirements

The power requirements listed in table 2-2 are for the SR192 motherboard with a TSIO, CPU and VXI modules.

Voltage	Peak Current	Dynamic Current	Note
+5V	2.2A	20mA	-
-5.2V	0	0	-
-2V	0	0	-
+12V	2mA	N/A	-
-12V	0	0	-
+24V	40mA	0	-
-24V	40mA	0	-
V+	200mA	100mA	1
V-	200mA	100mA	1

Note 1. Variable voltage TSIO setting only.

Table 2-2 Backplane Power Requirements

The following lists the front panel J10 V+ and V- voltage requirements for the variable voltage TSIO module with +15/-15 variable voltage I/O modules installed in any DRA<n> slot..

V1+ maximum .....+20V
V1+ minimum .....+7V
V1- maximum .....-7V
V1- minimum .....-20V
V1+ to V1- maximum 32V
V1+ minimum headroom from VOH/VIH .....+4V
V1- minimum headroom from VOL/VIL .....-4V

The following lists the front panel J10 V+ and V- voltage requirements for the variable voltage TSIO module with +7/-5 variable voltage I/O modules installed in any DRA<n> slot..

V1+ maximum .....+12.5V
V1+ minimum .....+9.5V
V1- maximum .....-7.5V
V1- minimum .....-12.5V

2.7 Cooling Requirements

The cooling requirements for an SR192 system requires that the total power used by the system must first be calculated (refer to Appendix C).

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3 Jumpers/Installation

The following sections describe the jumpers and installation procedure for the SR192 including the CPU, VXI and TSIO modules.

3.1 Motherboard Jumpers, Test Points, Fuses and SW1

Figure 3-1 below is a locator diagram for test points, jumpers, fuses and SW1 located on the SR192 motherboard, part number 20231 (S/N 1000 and up).

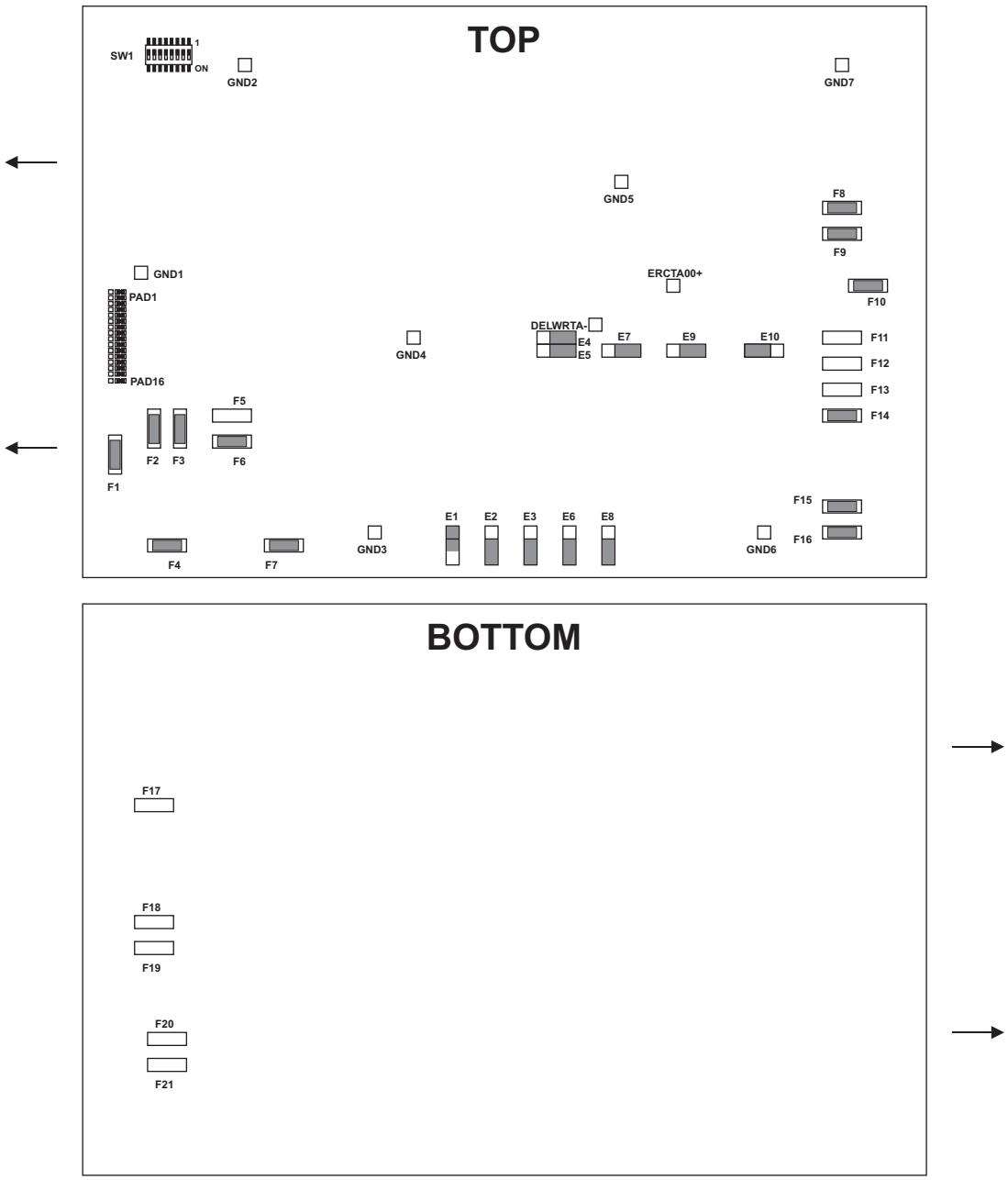


Figure 3-1 SR192 Motherboard Test Points, Jumpers, Fuses and SW1 Location

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3.1.1 Motherboard Test Point Description

Table 3-1 describes the test points on the SR192 motherboard.

Mnemonic	Description
GND1	Signal ground
GND2	Signal ground
GND3	Signal ground
GND4	Signal ground
GND5	Signal ground
GND6	Signal ground
GND7	Signal ground
DELWRTA-	Write enable signal to the error address memory.
ERCTA00+	Least significant address bit to the error address memory.

Table 3-1 SR192 Motherboard Test Point Description

3.1.2 Motherboard Jumper Description

The following sections describe the motherboard jumper options.

3.1.2.1 Probe/Reference Select (PAD1 through PAD16)

This set of sixteen jumper pads routes either the DAC reference or the SR211 probe control signals to the J9 front panel connector. The DAC references are selected by installing a zero ohm resistor between the two pads closer to the front panel. The SR211 Probe is selected (factory default) by installing a zero ohm resistor between the two pads furthest from the front panel. See figure 3-2 below.

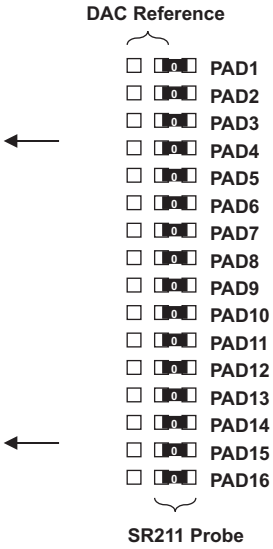


Figure 3-2 SR192 Motherboard J9 SR211/DAC Selection

3.1.2.2 TSINPUTMB Handshake Source (E1)

This jumper block selects the source for the TSINPUTMB handshake signal. Pin 1 to Pin 2 (factory default) connects the synchronized TSINPUT1A signal, pin 2 to pin 3 connects the buffered J7 TSINPUTM signal.

The pin 2 to pin 3 setting would only be used in all units of a multiple SR192 master/slave configured system.

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3.1.2.3 TSA Input2 Handshake Source (E2)

This jumper block selects the source for the TSA input2 signal. Pin 2 to Pin 3 (factory default) connects the front panel buffered TSINPUT2A signal, pin 1 to pin 2 connects the selected TTLTRG signal from the VXI backplane. See TTLTRG- register in appendix B.

The pin 1 to pin 2 setting would only be used to trigger TSA using the VXI backplane.

WARNING

A trace may be present (factory default) that connects pin 2 to pin 3 and must be cut prior to connecting pins 1 and 2.

3.1.2.4 DRB4 Voltage Group Select (E3,E4,E5,E6,E7,E8,E9)

These jumper blocks selects the voltage group for the DRB4 module. Pin 2 to pin 3 on all jumpers (factory default) connects DRB4 to voltage group 3, pin 1 to pin 2 connects voltage group 2.

Each voltage group is made up of 7 signals listed below along with the jumper that selects it:

Jumper (Signal)	DRB4 Slot Voltage Group	
	Pin 1 to Pin 2	Pin 2 to Pin 3 (Factory Default)
E3 (VIH)	VGRP2 (VIH2)	VGRP3 (VIH3)
E4 (V+)	VGRP2 (V2+)	VGRP3 (V3+)
E5 (V-)	VGRP2 (V2-)	VGRP3 (V3-)
E6 (VOH)	VGRP2 (VOH2)	VGRP3 (VOH3)
E7 (VIL)	VGRP2 (VIL2)	VGRP3 (VIL3)
E8 (VOL)	VGRP2 (VOL2)	VGRP3 (VOL3)
E9 (VISR)	VGRP2 (VISR2)	VGRP3 (VISR3)

3.1.2.5 TSB Input2 Handshake Source (E10)

This jumper block selects the source for the TSB input2 signal. Pin 2 to Pin 3 (factory default) connects the front panel buffered TSINPUT2B signal, pin 1 to pin 2 connects the selected TTLTRG signal from the VXI backplane. See TTLTRG- register in appendix B.

The pin 1 to pin 2 setting would only be used to trigger TSB using the VXI backplane.

WARNING

A trace may be present (factory default) that connects pin 2 to pin 3 and must be cut prior to connecting pins 1 and 2.

3.1.2.6 V1+ Source Select (F1, F17)

The V1+ source is selected by installing one of two fuses. F1-7A installed (factory default) connects V1+ to the front panel J10 connector, F17 (2A max) installed connects V1+ to the VXI backplane +12V.

3.1.2.7 V1- Source Select (F5, F6, F13)

The V1- source is selected by installing one of three fuses. F6-7A installed (factory default) connects V1- to the front panel J10 connector, F5 (2A max) installed connects V1- to the VXI backplane -12V, F13 (7A max) installed connects V1- to VXI backplane -5.2V.

3.1.2.8 V2+ Source Select (F4, F18)

The V2+ source is selected by installing one of two fuses. F4-7A installed (factory default) connects V2+ to the front panel J10 connector, F18 (2A max) installed connects V2+ to the VXI backplane +12V.

3.1.2.9 V2- Source Select (F2, F12, F21)

The V2- source is selected by installing one of three fuses. F2-7A installed (factory default) connects V2- to the front panel J10 connector, F21 (2A max) installed connects V1- to the VXI backplane -12V, F12 (7A max) installed connects V2- to VXI backplane -5.2V.

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3.1.2.10 V3+ Source Select (F7, F19)

The V3+ source is selected by installing one of two fuses. F7-7A installed (factory default) connects V3+ to the front panel J10 connector, F19 (2A max) installed connects V3+ to the VXI backplane +12V.

3.1.2.11 V3- Source Select (F3, F11, F20)

The V3- source is selected by installing one of three fuses. F3-7A installed (factory default) connects V3- to the front panel J10 connector, F20 (2A max) installed connects V3- to the VXI backplane -12V, F11 (7A max) installed connects V3- to VXI backplane -5.2V.

3.1.3 Motherboard Fuse Description

Table 3-2 describes the fuses on the motherboard for VXI backplane voltages used by the SR192.

Fuse	Signal, Amps
F8	+12V, 2A
F9	-12V, 2A
F10	+5V, 15A
F14	-5.2V, 15A
F15	+24V, 2A
F16	-24V, 2A

Table 3-2 SR192 Motherboard Fuse Description

3.1.4 Motherboard SW1 Description

SW1 is used to terminate or pull-up the front panel J7 signals. All switches on (factory default) connects the termination and pull-up resistors to the front panel J7 connector, all switches off isolates the termination and pull-up resisters from the J7 connector.

SW1 is used in a master/slave SR192 system. All SR192's in the chassis except for the last SR192 slave should set all SW1 switches off.

3.2 CPU Jumpers, Test Points and Switches

Figure 3-3 below is a locator diagram for test points, jumpers and switches located on the SR192 CPU module, part number 10510.

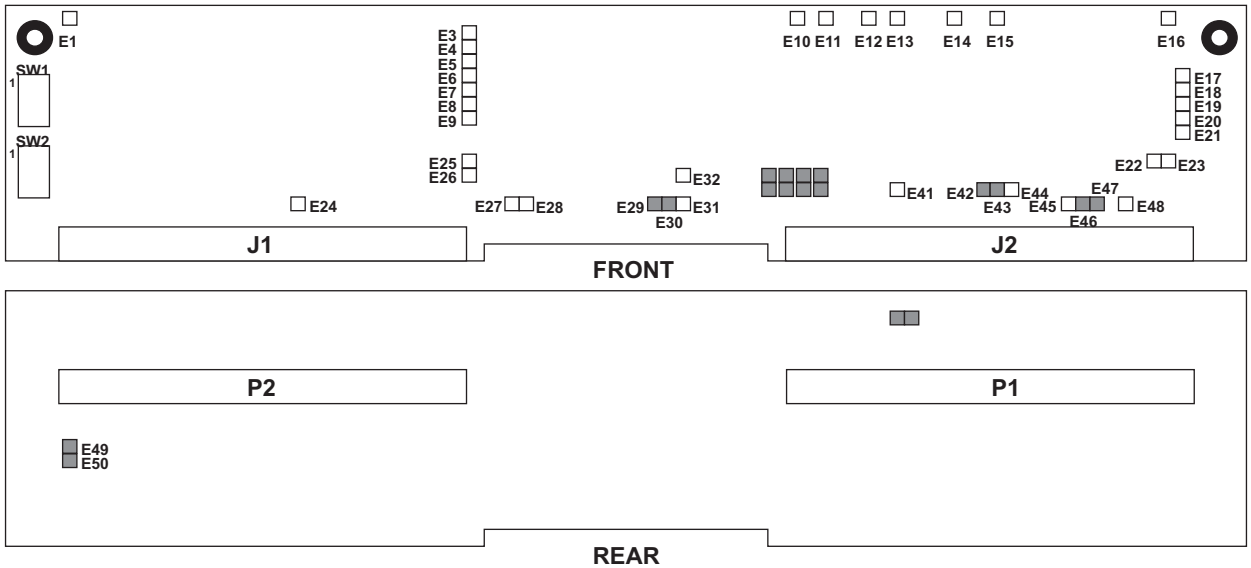


Figure 3-3 SR192 CPU Module Test Points, Jumpers and Switch Location

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3.2.1 CPU Test Point Description

Table 3-3 describes the test points on the SR192 CPU module.

Mnemonic	Description
E1	Signal ground
E2	Signal ground
E3	+5V
E4	Signal Ground
E5	CCLK1
E6	DONE1
E7	DIN1
E8	PROG1
E9	LA19/INIT-
E10	UAS-
E11	CPU-
E12	Signal ground
E13	+5V
E14	Signal ground
E15	VXI-
E16	Signal ground
E17	+5V
E18	Signal Ground
E19	CCLK2
E20	DONE2
E21	DIN2
E22	PROG2-
E23	Signal Ground
E24	BS8-
E25	PROG1-
E26	Signal Ground
E27	UIPL2-
E28	UIPL1-
E32	UIPL0-
E41	GALIO1
E48	VAS-

Table 3-3 SR192 CPU Test Point Description

3.2.2 CPU Jumper Description

The following sections describe the CPU module jumper options.

3.2.2.1 U21 FPGA Cable Load (E42,E43,E44; E45,E46,E47; E49,E50)

U21 can be programmed through either a serial PROM or by a cable download. E42 connected to E43, E46 connected to E47 and E49 connected to E50 enables U21 to be loaded by the serial PROM (factory default). E43 connected to E44, E45 connected to E46 and E49 disconnected from E50 enables U21 to be loaded from the cable.

These jumpers are factory reserved and should not be modified.

WARNING

A trace may be present (factory default) that connects E49 to E50.

3.2.2.2 U6 FPGA Cable Load (E29,E30,E31; E51,E52)

U6 can be programmed through either a serial PROM or by a cable download. E30 connected to E31 and E51 connected to E52 enables U6 to be loaded by the serial PROM (factory default). E29 connected to E30 and E51 disconnected from E52 enables U6 to be loaded from the cable.

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These jumpers are factory reserved and should not be modified.

WARNING

A trace may be present (factory default) that connects E51 to E52.

3.2.2.3 General Purpose SRIO (E33,E34; E35,E36)

Two general purpose I/O signals (SRIO1 and SRIO2) can be isolated from the SR192 motherboard. E33 connected to E34 and E35 connected to E36 connects the SRIO signals to the motherboard (factory default). E33 disconnected from E34 and E35 disconnected from E36 isolates the SRIO signals.

These jumpers are factory reserved and should not be modified.

3.2.2.4 CPWAIT Signal (E37,E38)

The CPWAIT signal can be isolated from the SR192 motherboard. E37 connected to E38 connects the CPWAIT signal to the SR192 motherboard (factory default). E37 disconnected from E38 isolates CPWAIT from the SR192 motherboard.

These jumpers are factory reserved and should not be modified.

3.2.2.5 UUTRST Signal (E39,E40)

The UUTRST signal can be isolated from the SR192 motherboard. E39 connected to E40 connects the UUTRST signal to the SR192 motherboard (factory default). E39 disconnected from E40 isolates UUTRST from the SR192 motherboard.

These jumpers are factory reserved and should not be modified.

3.2.3 CPU Switch Description

The following sections describe the CPU module switches.

3.2.3.1 Logical Address Switch Selection (SW1)

The following figure 3-4 below shows a logical address setting of 2.

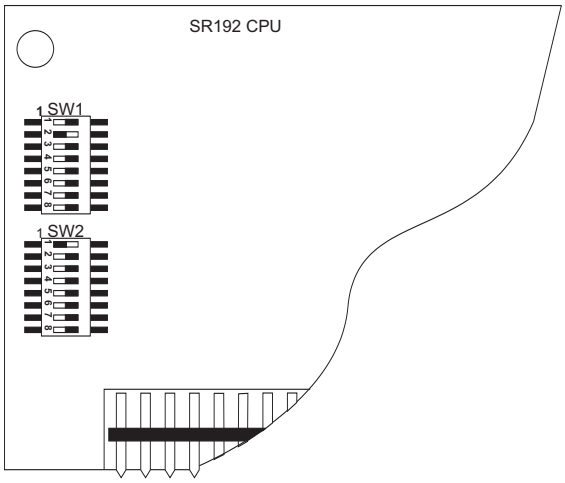


Figure 3-4 SR192 CPU Module Switch Settings

SW1							
8	7	6	5	4	3	2	1
LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0

Switch position definitions:

Position 1 through 8 corresponds to bits 0 through 7 of the logical address. The “ON” setting sets the corresponding bit of the logical address to a one (1).

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A logical address setting of 255 (factory default), all positions set “ON”, sets the SR192 into dynamic addressing mode. A logical address setting between 1 and 254 sets the SR192 into static mode. A logical address of zero is reserved for the slot 0 controller and is invalid.

3.2.3.2 Interrupt Level, A32/A24 Switch Selection (SW2)

SW2							
8	7	6	5	4	3	2	1
Reserved				A24/A32	Interrupt Level		

Switch position definitions:

The binary encoded value of the first three switch positions of SW2 are used to assign the VXI interrupt level.

Position 3	Position 2	Position 1	VXI Interrupt Level
OFF	OFF	OFF	Disabled (none)
OFF	OFF	ON	Level One Selected (factory default)
OFF	ON	OFF	Level Two Selected
OFF	ON	ON	Level Three Selected
ON	OFF	OFF	Level Four Selected
ON	OFF	ON	Level Five Selected
ON	ON	OFF	Level Six Selected
ON	ON	ON	Level Seven Selected

Switch position 4 is used to select A32/A24 register mapping.

Position 4	Register Mapping
OFF	A32 Register Mapping (factory default)
ON	A24 Register Mapping

Positions 5 through 8 are factory reserved and should be set to off.

Figure 3-4 shows a interrupt level setting of one (factory default). A setting of zero disables the VXI interrupt generation.

3.3 VXI Test Points and Fuses

Figure 3-5 below is a locator diagram for test points and fuses located on the SR192 VXI module, part number 10532.

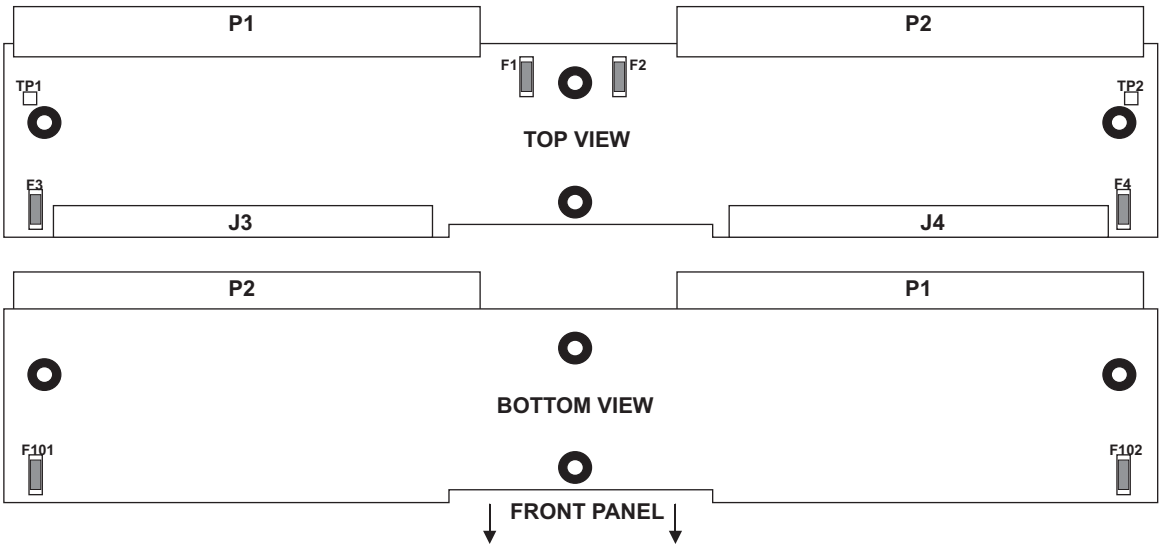


Figure 3-5 SR192 VXI Module Test Points and Fuses

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3.3.1 VXI Test Point Description

Table 3-4 below describes the test points on the SR192 VXI module.

Mnemonic	Description
TP1	Signal ground
TP2	Signal ground

Table 3-4 SR192 VXI Module Test Points

3.3.2 VXI Fuse Description

Table 3-5 below describes the fuses on the VXI module for VXI backplane voltages used by the SR192.

Fuse	Signal, Amps
F1	+5V, 10A
F2	+5V, 10A
F3	+12V, 2A
F4	+24V, 2A
F101	-24V, 2A
F102	-12V, 2A

Table 3-5 SR192 VXI Module Fuse Description

3.4 TSIO Jumper Description

The following sections describes the jumper selections for both types of SR192 TSIO modules, variable voltage/TTL (part number 10545-003) and differential/TTL (part number 10500-003).

3.4.1 TSIO Variable Voltage Jumper Description

Figure 3-6 shows the factory default jumper settings for both revisions of the variable voltage TSIO PCB.

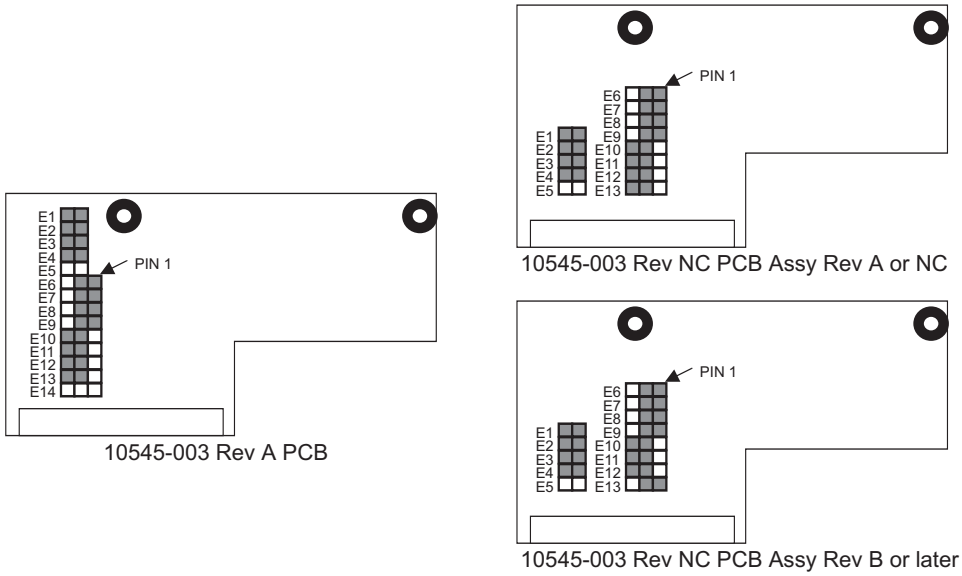


Figure 3-6 TSIO Variable Voltage/TTL Jumper Locations

The assembly revision for the revision NC PCB is located on the opposite side of the board.

3.4.1.1 TSINPUTA1 Receiver Source (E1, E10)

The receiver for the TSINPUTA1 handshake signal is selected using jumpers E1 and E10. The TTL receiver is selected by installing a jumper in E1 and E10 pin 2 to pin 3 (factory default). The Variable Voltage receiver is selected by removing the E1 jumper and installing a jumper in E10 pin 1 to pin 2.

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3.4.1.2 TSINPUTA2 Receiver Source (E2, E11)

The receiver for the TSINPUTA2 handshake signal is selected using jumpers E2 and E11. The TTL receiver is selected by installing a jumper in E2 and E11 pin 2 to pin 3 (factory default). The Variable Voltage receiver is selected by removing the E2 jumper and installing a jumper in E11 pin 1 to pin 2.

3.4.1.3 EXCLK1 Receiver Source (E3, E12)

The receiver for the EXCLK1 external clock signal is selected using jumpers E3 and E12. The TTL receiver is selected by installing a jumper in E3 and E12 pin 2 to pin 3 (factory default). The Variable Voltage receiver is selected by removing the E3 jumper and installing a jumper in E12 pin 1 to pin 2.

3.4.1.4 FCNTL1 Receiver Source (E4, E13, E14)

The receiver for the FCNTL1 control signal is selected using jumpers E4 and E13. E14 is also used on the Rev A PCB.

For the Rev A PCB the TTL receiver is selected by installing a jumper in E4 and E13 pin 2 to pin 3 (factory default). The Variable Voltage receiver is selected by removing the E4 and E13 jumpers and installing a jumper in E14 pin 1 to pin 2.

For the Rev NC PCB assembly revisions A and NC, the TTL receiver is selected by installing a jumper in E4 and E13 pin 2 to pin 3 (factory default). The Variable Voltage receiver is selected by removing the E4 jumper and installing a jumper in E13 pin 1 to pin 2.

For the Rev NC PCB assembly revisions B or later, the TTL receiver is selected by installing a jumper in E4 and E13 pin 1 to pin 2 (factory default). The Variable Voltage receiver is selected by removing the E4 jumper and installing a jumper in E13 pin 2 to pin 3.

3.4.1.5 Variable Voltage Receiver Reference Source (E6)

The reference source for the Variable Voltage receivers can be selected by using the E6 jumper. E6 pin 1 connected to pin 2 selects VIL1 signal (factory default). E6 pin 2 to pin 3 uses a 1.4V fixed reference.

3.4.1.6 TSOUTA1 Driver Source (E7)

The driver for the TSOUTA1 signal is selected by using the E7 jumper. E7 pin 1 to pin 2 selects the TTL driver (factory default). E7 pin 2 to pin 3 selects the Variable Voltage driver.

3.4.1.7 CLOCKA Driver Source (E8)

The driver for the CLOCKA signal is selected by using the E8 jumper. E8 pin 1 to pin 2 selects the TTL driver (factory default). E8 pin 2 to pin 3 selects the Variable Voltage driver.

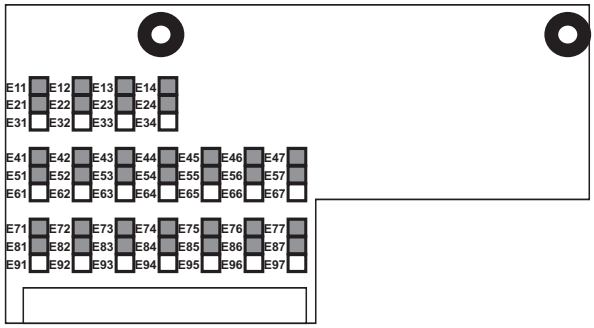
3.4.1.8 TSOUTA2 Driver Source (E9)

The driver for the TSOUTA2 signal is selected by using the E9 jumper. E9 pin 1 to pin 2 selects the TTL driver (factory default). E9 pin 2 to pin 3 selects the Variable Voltage driver.

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3.4.2 TSIO Differential/TTL Jumper Description

Figure 3-7 shows the factory default jumper settings for the differential/TTL TSIO PCB.



10550-003

Figure 3-7 TSIO Differential/TTL Jumper Locations

3.4.2.1 TSINPUTA1 Receiver Source (E14,E24,E34,E44,E54,E64,E74,E84,E94)

The receiver for the TSINPUTA1 handshake signal is selected using jumpers E14 through E94. The TTL receiver is selected by installing jumpers between E14 and E24, E44 and E54, E74 and E84 (factory default). The differential receiver is selected by installing jumpers between E24 and E34, E54 and E64, E84 and E94.

3.4.2.2 TSINPUTA2 Receiver Source (E13,E23,E33,E43,E53,E63,E73,E83,E93)

The receiver for the TSINPUTA2 handshake signal is selected using jumpers E13 through E93. The TTL receiver is selected by installing jumpers between E13 and E23, E43 and E53, E73 and E83 (factory default). The differential receiver is selected by installing jumpers between E23 and E33, E53 and E63, E83 and E93.

3.4.2.3 EXCLK1 Receiver Source (E12,E22,E32,E42,E52,E62,E72,E82,E92)

The receiver for the EXCLK1 external clock signal is selected using jumpers E12 through E92. The TTL receiver is selected by installing a jumper between E12 and E22, E42 and E52, E72 and E82 (factory default). The differential receiver is selected by installing jumpers between E22 and E32, E52 and E62, E82 and E92.

3.4.2.4 FCNTL1 Receiver Source (E11,E21,E31,E41,E51,E61,E71,E81,E91)

The receiver for the FCNTL1 control signal is selected using jumpers E11 through E91. The TTL receiver is selected by installing a jumper between E11 and E21, E41 and E51, E71 and E81 (factory default). The differential receiver is selected by installing jumpers between E21 and E31, E51 and E61, E81 and E91.

3.4.2.5 TSOUTA1 Driver Source (E46,E56,E66,E76,E86,E96)

The driver for the TSOUTA1 signal is selected by using E46 through E96 jumpers. Jumpers between E46 and E56, E76 and E86 selects the TTL driver (factory default). Jumpers between E56 and E66, E86 and E96 selects the differential driver.

3.4.2.6 CLOCKA Driver Source (E47,E57,E67,E77,E87,E97)

The driver for the CLOCKA signal is selected by using E47 through E97 jumpers. Jumpers between E47 and E57, E77 and E87 selects the TTL driver (factory default). Jumpers between E57 and E67, E87 and E97 selects the differential driver.

3.4.2.7 TSOUTA2 Driver Source (E45,E55,E65,E75,E85,E95)

The driver for the TSOUTA2 signal is selected by using E45 through E95 jumpers. Jumpers between E45 and E55, E75 and E85 selects the TTL driver (factory default). Jumpers between E55 and E65, E85 and E95 selects the differential driver.

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3.5 Module Installation

Along with the CPU, VXI and TSIO modules, each SR192 motherboard can optionally house up to two timing modules, twelve I/O modules and one DAC/MFC Accessory module.

Figure 3-8 below illustrates the slot positions of the SR192 and their reference designators.

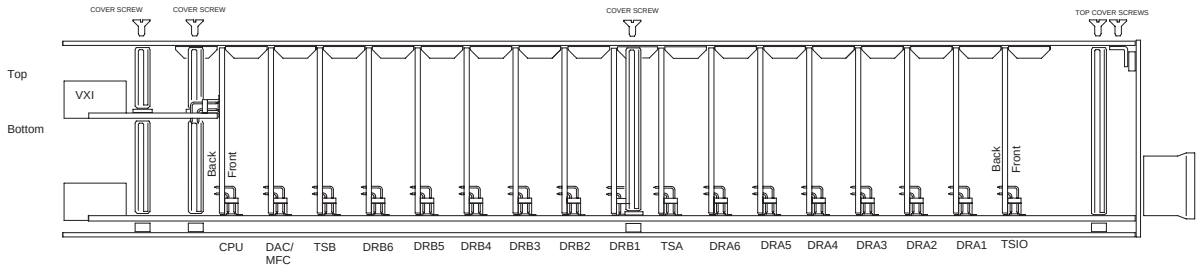


Figure 3-8 SR192 Slot Position Side View

Perform the following steps to add or replace an SR192 module:

Step 1. Using ESD protocols remove the SR192 from the VXI chassis.

Step 2. Remove the top cover black anodized screws, refer to Figure 3-8.

Step 3. If replacing either the CPU or VXI module, remove the spacers that hold the VXI module.

Step 4. Remove the module by grasping at each corner and gently rocking forward and back while pulling it away from the motherboard.

Step 5. Insert the module in the desired slot by lining up the connectors and gently pushing down. All SR192 modules except the VXI and TSIO are keyed along the associated mating connector. If the module cannot be inserted, check for bent pins and make certain the pins are aligned with the mating connector on the motherboard.

WARNING

Make sure the connectors are aligned and in the proper slot position. It is possible to mis-align or force even a keyed module into the wrong slot or pin number.

Step 6. Reinstall spacers and washers if applicable.

Step 7. Reinstall top cover.

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3.6 Termination Options

Table 3-6 below list the termination value and location of each resistor for the front panel signals.

Connector	Signal	Logic	Termination	Location
J1-J6	CH1-CH192	I/O Module Specific		I/O Module
J7	System master/slave connector, see section 3.1.4			
J8	**Variable Voltage/TTL TSIO Signals**			
	TSOUTA1	Variable Voltage/TTL	Series 47Ω	TSIO, R18[1], R23[2]
	TSOUTA2	Variable Voltage/TTL	Series 47Ω	TSIO, R17[1], R22[2]
	CLOCKA	Variable Voltage/TTL	Series 47Ω	TSIO, R19[1], R24[2]
	TSINPUTA1	Variable Voltage/TTL	Parallel to GND	TSIO, Not Installed, R2
	TSINPUTA2	Variable Voltage/TTL	Parallel to GND	TSIO, Not Installed R1[1], R5[2]
	EXCLK1	Variable Voltage/TTL	Parallel to GND	TSIO, Not Installed R3[1], R1[2]
	FCNTL1	Variable Voltage/TTL	Parallel to GND	TSIO, Not Installed R4
	Differential/TTL TSIO Signals			
	TSOUTA1	TTL	Series 47Ω	TSIO, R5
		Differential	None	NA
	TSOUTA2	TTL	Series 47Ω	TSIO, R3
		Differential	None	NA
	CLOCKA	TTL	Series 47Ω	TSIO, R7
		Differential	None	NA
	TSINPUTA1	TTL	82Ω to GND	TSIO, R6
		Differential	120Ω parallel	TSIO, R11
	TSINPUTA2	TTL	82Ω to GND	TSIO, R4
		Differential	120Ω parallel	TSIO, R10
	EXCLK1	TTL	82Ω to GND	TSIO, R2
		Differential	120Ω parallel	TSIO, R9
	FCNTL1	TTL	82Ω to GND	TSIO, R1
		Differential	120Ω parallel	TSIO, R8
	Motherboard Signals			
	TSOUTA3-5 TSOUTB1-5	TTL	Series 47Ω	MB, U2
	TSINPUTB1	TTL	82Ω to GND	MB, R42
	TSINPUTB2	TTL	82Ω to GND	MB, R41
	EXCLK2	TTL	82Ω to GND	MB, R83
	TSABUSY	TTL	NONE	NA
	TSBBUSY	TTL	NONE	NA
	SYNCA	TTL	NONE	NA
	SYNCB	TTL	NONE	NA
	FCNTL2	TTL	82Ω to GND	MB, R65
	CLOCKB	TTL	Series 47Ω	MB, R67
	PRBDAT	TTL	NONE	NA
	UUTRST	TTL	Series 47Ω	MB, R79
	CLKRSTE	TTL	NONE	NA
SMA	EXCLK1	See J8 EXCLK1 above		
	EXCLK2	See J8 EXCLK2 above		
	CLKA	TTL	Series 47Ω	SR210, U5
	CLKB	TTL	Series 47Ω	SR210, U5
	CLKC	Variable Voltage	Series 47Ω	SR210, U5
	CLKREF	TTL	82Ω to GND	SR210, R113

Note 1: Variable Voltage/TTL TSIO rev NC.

Table 3-6 Front Panel Signal Termination Location and Values

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3.7 SR192 Installation

The following sections discuss the installation procedure for the SR192 system.

WARNING

Use ESD protocols whenever handling the SR192 or any of its modules.

3.7.1 Receiving Inspection

Check the shipment at the time of delivery and inspect each box for damage. Describe any box damage and list any shortages on the delivery invoice.

1. **Unpack the boxes.** Unpack the boxes in a clean and dry environment. Save all the packing material in case the instrument must be returned for service.
2. **Check for damage.** Inspect the equipment carefully for any signs of physical damage regardless of the condition of the shipping boxes. In the case of physical damage, call the shipper immediately and start the claim process. Call a Customer Service representative (800-722-2528) to inform them that the shipment arrived damaged. Please be prepared to provide a detailed damage report.

3.7.2 Returning Equipment

Follow these steps when you return equipment to Talon:

1. **Save the packing material.** Always return equipment in its original packing material and boxes. If you use inadequate material, you'll be responsible for any shipping damage repair as carriers won't accept responsibility on incorrectly packed equipment.
2. **Call Talon's Customer Service and ask for a return authorization.** The Customer Service representative (800-722-2528) will ask for your name, telephone number, company name, equipment type, model number, serial number, and a description of your problem.
3. **Pack and ship the equipment to:**

   Talon Instruments
   4 Goodyear
   Irvine, CA 92618

3.7.3 Preparation for Storage

The SR192 should be stored in a clean, dry environment. In high humidity environments, protect the SR192 from temperature variations that could cause internal condensation. The following environmental conditions apply to both shipping and storage:

Temperature	-40°C to +70°C
Relative Humidity	Not controlled, non-condensing
Altitude	<40000 ft. (12192 m)
Vibration	<2g
Shock	<40g

3.7.4 Preparation for Use

The following sections covers the following topics:

- Logical Address Selection
- VXI Interrupt Level Selection

3.7.4.1 Logical Address Selection

The VXI chassis Resource Manager identifies units in the system by the unit's logical address. The VXI logical address can range from 0 to 255. The exceptions are addresses 0 and 255. Address 0 is reserved for the Resource Manager. Address 255 is used for dynamic configuration.

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The logical address of the SR192 can be statically or dynamically configured. An eight position DIP switch (SW1) located on the CPU module, see section 3.2.3.1, is used to assign the logical address. A switch setting between 1 and 254 will establish a static logical address of the same value. A switch setting of 255 will place the SR192 in a dynamic logical address mode where the final logical address is assigned by the resource manager. Talon ships the SR192 in the dynamic configuration.

3.7.4.2 VXI Interrupt Selection

The first three switch positions of SW2 is used to assign the VXI interrupt level, see section 3.2.3.2. A value of zero disables VXI interrupt generation by the SR192. Values between one and seven select the interrupt of the same value, i.e., if SW2 position 2 and 3 are on and position one is off then VXI interrupt level 6 will be used by the SR192. VXI level one is set at the factory prior to shipment.

3.7.5 Installation

The SR192 must be installed in a VXI mainframe in any slot except slot 0 (zero), which is reserved for the Resource Manager. Always check P1 and P2 for bent pins prior to installation. When inserting the SR192 into the mainframe, it should be gently rocked back and forth to seat the connectors into the backplane receptacles.

3.7.5.1 Initial Power-On

With the SR192 properly installed in a VXI chassis, turn on the external power supplies, if required, followed by the chassis power. Refer to the appropriate I/O module reference manual for external power requirements.

The SR192 will immediately conduct a self-test which tests memory, registers, communication with the host, etc. The red FAIL indicator will come on and the SYSFAIL- line on the VXI backplane will be driven true. The other indicators may or may not flash during the self-test. After about four seconds, if the SR192 passes the VXI register configuration self-test, then the FAIL indicator will go off, all the other indicators will be off, and the SYSFAIL- line will no longer be driven by the SR192. The SR192 is now ready for use.

If the SR192 fails the VXI register configuration self test, then the FAIL indicator will stay on and the SYSFAIL- line will continue to be driven. Should this happen, turn the chassis power off, make certain the SR192 is properly installed, and turn the chassis power back on. Should the SR192 continue to fail, then call Talon's Customer Service representative (800-722-2528) for assistance.

If the FAIL indicator flashes after power-up then one or more of the SR192's modules have failed the module self test. To locate the failing module either run the Plug & Play Soft Front Panel shipped with the instrument driver or send the following SCPI commands:

for each <module> send

MODule:SELect <module>

MODule:STATus?

The response returned from the STATus query should have bit one set high for all modules that passed the self test. After identifying any failing modules turn off the chassis power, remove the SR192 and inspect the failing module to see if there is a good connection to the SR192 motherboard. Re-install the SR192 and turn the chassis power back on. Should the module(s) continue to fail, call Talon's Customer Service representative for assistance.

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4 SR192 Front Panel

The SR192 front panel provides the hardware interface to the UUT. Figure 4-1 illustrates the front panel and its connectors:

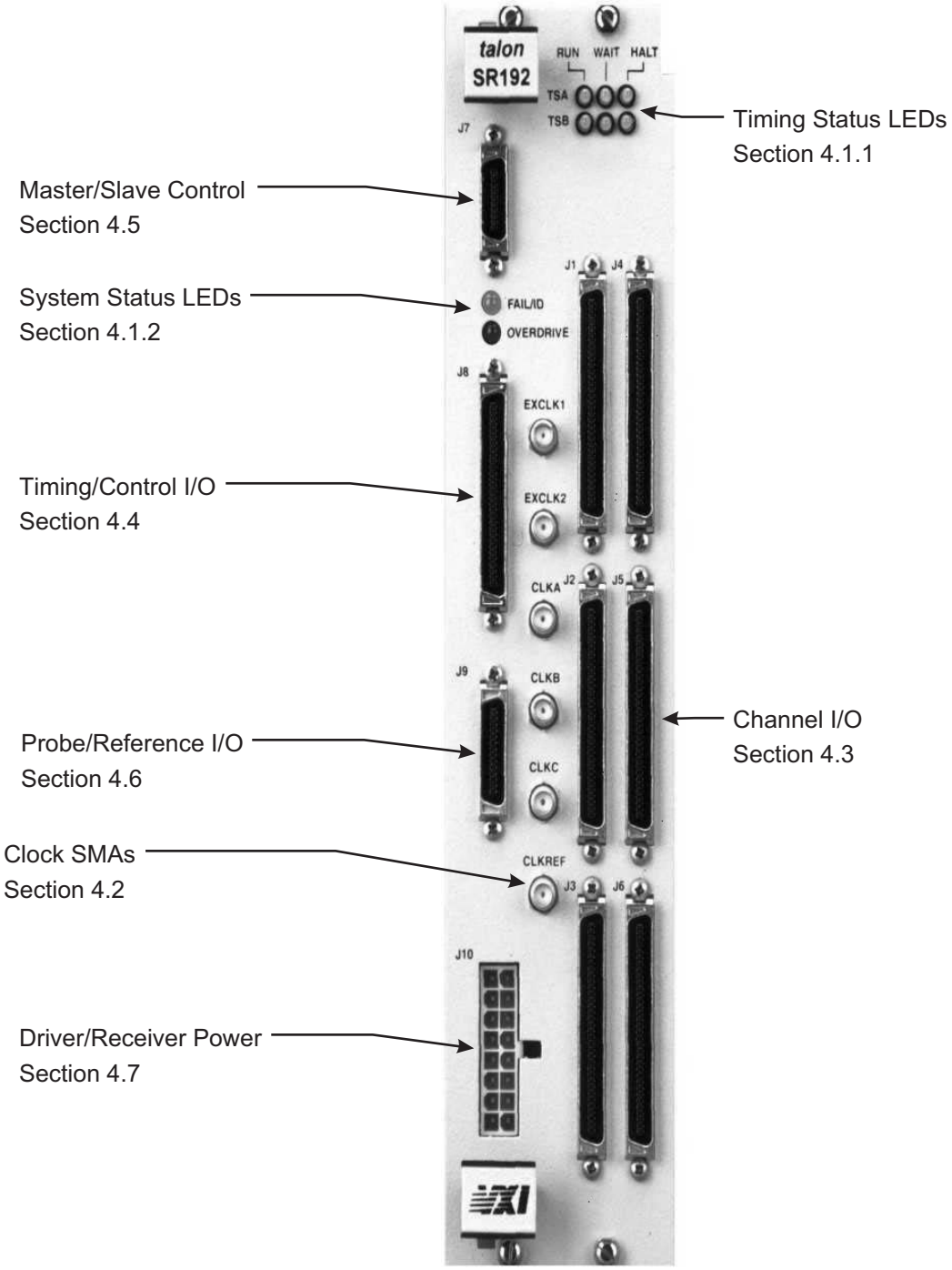


Figure 4-1 SR192 Front Panel

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4.1 LED Indicators

The following sections describe all of the front panel indicators and connectors. Appendix G gives a detailed description of all the SR192 signals including drive and termination information.

4.1.1 Timing Set LED Indicators

The timing set LEDs, located in the top right corner of the front panel, are used to indicate the operating status of the Timing Sets A & B. The color codes are:

RUN	Off - IDLE cycle not active, i.e., RESET mode.
	Green - IDLE cycle is active.
	Red - Sequence cycles are executing.
WAIT	Off - no timeouts have occurred.
	Green - waiting for a test cell to complete.
	Red - A test cell timed out.
HALT	Off - No tests for compare or error.
	Green - waiting on a test for a compare cell.
	Red - A test for error cell is true.

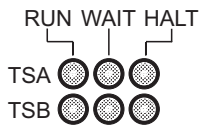


Figure 4-2 Timing Module Status LEDs

4.1.2 System LED Indicators

The System LED Indicators are used to communicate system information to the user. Illuminated LEDs indicate:

FAIL/ID	Off - normal operation.
	Solid Red - CPU power-up self test failed.
	Flashing Red - Command/Module error.
	Green - VXI MODID asserted.
	Amber - both FAIL and MODID are asserted.
OVERDRIVE	One of the Variable Voltage drivers on the TSIO or I/O modules was over-driven and has shut-off.



Figure 4-3 System Status LEDs

4.2 SMA Connectors

SMAs are provided to allow the user access to programmable clock outputs as well a providing a shielded connector for clock inputs.

EXCLK1	External timing module input clock one (also available on J8 connector).
EXCLK2	External timing module input clock two (also available on J8 connector).
CLKA	Delayed programmable output clock one from SR210.
CLKB	Delayed programmable output clock two from SR210.
CLKC	Variable voltage programmable output clock two from SR210.
CLKREF	Programmable reference input clock to SR210.

CLKA, CLKB, CLKC and CLKREF are only available when the optional SR210 MFC accessory module is installed.



Figure 4-4 Clock SMAs

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4.3 I/O Signal Connectors, J1-J6

There are 6 I/O channel connectors labeled J1-J6. One side of each connector is designated for each I/O module.

4.3.1 J1 I/O Connector

Table 4-1 lists the I/O channels assigned to J1.

Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic	Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic
J1-1A	CH1	CH1+	J1-1B	CH17	CH17+
J1-2A	GND	CH1-	J1-2B	GND	CH17-
J1-3A	CH2	CH2+	J1-3B	CH18	CH18+
J1-4A	GND	CH2-	J1-4B	GND	CH18-
J1-5A	CH3	CH3+	J1-5B	CH19	CH19+
J1-6A	GND	CH3-	J1-6B	GND	CH19-
J1-7A	CH4	CH4+	J1-7B	CH20	CH20+
J1-8A	GND	CH4-	J1-8B	GND	CH20-
J1-9A	CH5	CH5+	J1-9B	CH21	CH21+
J1-10A	GND	CH5-	J1-10B	GND	CH21-
J1-11A	CH6	CH6+	J1-11B	CH22	CH22+
J1-12A	GND	CH6-	J1-12B	GND	CH22-
J1-13A	CH7	CH7+	J1-13B	CH23	CH23+
J1-14A	GND	CH7-	J1-14B	GND	CH23-
J1-15A	CH8	CH8+	J1-15B	CH24	CH24+
J1-16A	GND	CH8-	J1-16B	GND	CH24-
J1-17A	CH9	GND	J1-17B	CH25	GND
J1-18A	GND	GND	J1-18B	GND	GND
J1-19A	CH10	GND	J1-19B	CH26	GND
J1-20A	GND	GND	J1-20B	GND	GND
J1-21A	CH11	GND	J1-21B	CH27	GND
J1-22A	GND	GND	J1-22B	GND	GND
J1-23A	CH12	NC	J1-23B	CH28	NC
J1-24A	GND	NC	J1-24B	GND	NC
J1-25A	CH13	NC	J1-25B	CH29	NC
J1-26A	GND	NC	J1-26B	GND	NC
J1-27A	CH14	NC	J1-27B	CH30	NC
J1-28A	GND	NC	J1-28B	GND	NC
J1-29A	CH15	NC	J1-29B	CH31	NC
J1-30A	GND	NC	J1-30B	GND	NC
J1-31A	CH16	NC	J1-31B	CH32	NC
J1-32A	GND	NC	J1-32B	GND	NC
J1-33A	CSTROBE (DRA1)	CSTROBE[1] (DRA1)	J1-33B	CSTROBE (DRA2)	CSTROBE[1] (DRA2)
J1-34A	GND	NC	J1-34B	GND	NC

Note 1. Signal is single ended TTL.

Table 4-1 J1 I/O Connector Assignments

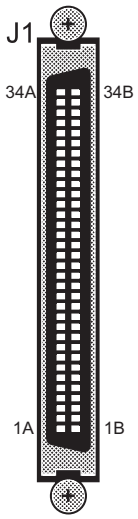


Figure 4-5 J1 Connector

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4.3.2 J2 I/O Connector

Table 4-2 lists the I/O channels assigned to J2.

Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic	Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic
J2-1A	CH33	CH33+	J2-1B	CH49	CH49+
J2-2A	GND	CH33-	J2-2B	GND	CH49-
J2-3A	CH34	CH34+	J2-3B	CH50	CH50+
J2-4A	GND	CH34-	J2-4B	GND	CH50-
J2-5A	CH35	CH35+	J2-5B	CH51	CH51+
J2-6A	GND	CH35-	J2-6B	GND	CH51-
J2-7A	CH36	CH36+	J2-7B	CH52	CH52+
J2-8A	GND	CH36-	J2-8B	GND	CH52-
J2-9A	CH37	CH37+	J2-9B	CH53	CH53+
J2-10A	GND	CH37-	J2-10B	GND	CH53-
J2-11A	CH38	CH38+	J2-11B	CH54	CH54+
J2-12A	GND	CH38-	J2-12B	GND	CH54-
J2-13A	CH39	CH39+	J2-13B	CH55	CH55+
J2-14A	GND	CH39-	J2-14B	GND	CH55-
J2-15A	CH40	CH40+	J2-15B	CH56	CH56+
J2-16A	GND	CH40-	J2-16B	GND	CH56-
J2-17A	CH41	GND	J2-17B	CH57	GND
J2-18A	GND	GND	J2-18B	GND	GND
J2-19A	CH42	GND	J2-19B	CH58	GND
J2-20A	GND	GND	J2-20B	GND	GND
J2-21A	CH43	GND	J2-21B	CH59	GND
J2-22A	GND	GND	J2-22B	GND	GND
J2-23A	CH44	NC	J2-23B	CH60	NC
J2-24A	GND	NC	J2-24B	GND	NC
J2-25A	CH45	NC	J2-25B	CH61	NC
J2-26A	GND	NC	J2-26B	GND	NC
J2-27A	CH46	NC	J2-27B	CH62	NC
J2-28A	GND	NC	J2-28B	GND	NC
J2-29A	CH47	NC	J2-29B	CH63	NC
J2-30A	GND	NC	J2-30B	GND	NC
J2-31A	CH48	NC	J2-31B	CH64	NC
J2-32A	GND	NC	J2-32B	GND	NC
J2-33A	CSTROBE (DRA3)	CSTROBE[1] (DRA3)	J2-33B	CSTROBE (DRA4)	CSTROBE[1] (DRA4)
J2-34A	GND	NC	J2-34B	GND	NC

Note 1. Signal is single ended TTL.

Table 4-2 J2 I/O Connector Assignment

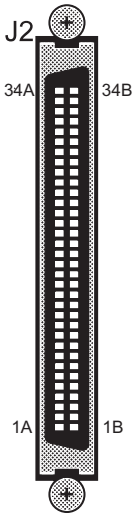


Figure 4-6 J2 Connector

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4.3.3 J3 I/O Connector

Table 4-3 lists the I/O channels assigned to J3.

Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic	Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic
J3-1A	CH65	CH65+	J3-1B	CH81	CH81+
J3-2A	GND	CH65-	J3-2B	GND	CH81-
J3-3A	CH66	CH66+	J3-3B	CH82	CH82+
J3-4A	GND	CH66-	J3-4B	GND	CH82-
J3-5A	CH67	CH67+	J3-5B	CH83	CH83+
J3-6A	GND	CH67-	J3-6B	GND	CH83-
J3-7A	CH68	CH68+	J3-7B	CH84	CH84+
J3-8A	GND	CH68-	J3-8B	GND	CH84-
J3-9A	CH69	CH69+	J3-9B	CH85	CH85+
J3-10A	GND	CH69-	J3-10B	GND	CH85-
J3-11A	CH70	CH70+	J3-11B	CH86	CH86+
J3-12A	GND	CH70-	J3-12B	GND	CH86-
J3-13A	CH71	CH71+	J3-13B	CH87	CH87+
J3-14A	GND	CH71-	J3-14B	GND	CH87-
J3-15A	CH72	CH72+	J3-15B	CH88	CH88+
J3-16A	GND	CH72-	J3-16B	GND	CH88-
J3-17A	CH73	GND	J3-17B	CH89	GND
J3-18A	GND	GND	J3-18B	GND	GND
J3-19A	CH74	GND	J3-19B	CH90	GND
J3-20A	GND	GND	J3-20B	GND	GND
J3-21A	CH75	GND	J3-21B	CH91	GND
J3-22A	GND	GND	J3-22B	GND	GND
J3-23A	CH76	NC	J3-23B	CH92	NC
J3-24A	GND	NC	J3-24B	GND	NC
J3-25A	CH77	NC	J3-25B	CH93	NC
J3-26A	GND	NC	J3-26B	GND	NC
J3-27A	CH78	NC	J3-27B	CH94	NC
J3-28A	GND	NC	J3-28B	GND	NC
J3-29A	CH79	NC	J3-29B	CH95	NC
J3-30A	GND	NC	J3-30B	GND	NC
J3-31A	CH80	NC	J3-31B	CH96	NC
J3-32A	GND	NC	J3-32B	GND	NC
J3-33A	CSTROBE (DRA5)	CSTROBE[1] (DRA5)	J3-33B	CSTROBE (DRA6)	CSTROBE[1] (DRA6)
J3-34A	GND	NC	J3-34B	GND	NC

Note 1. Signal is single ended TTL.

Table 4-3 J3 I/O Connector Assignments

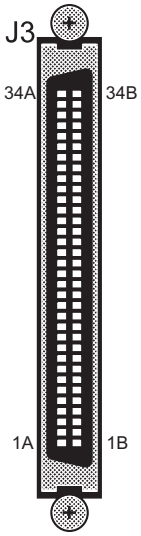


Figure 4-7 J3 Connector

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4.3.4 J4 I/O Connector

Table 4-4 lists the I/O channels assigned to J4.

Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic	Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic
J4-1A	CH97	CH97+	J4-1B	CH113	CH113+
J4-2A	GND	CH97-	J4-2B	GND	CH113-
J4-3A	CH98	CH98+	J4-3B	CH114	CH114+
J4-4A	GND	CH98-	J4-4B	GND	CH114-
J4-5A	CH99	CH99+	J4-5B	CH115	CH115+
J4-6A	GND	CH99-	J4-6B	GND	CH115-
J4-7A	CH100	CH100+	J4-7B	CH116	CH116+
J4-8A	GND	CH100-	J4-8B	GND	CH116-
J4-9A	CH101	CH101+	J4-9B	CH117	CH117+
J4-10A	GND	CH101-	J4-10B	GND	CH117-
J4-11A	CH102	CH102+	J4-11B	CH118	CH118+
J4-12A	GND	CH102-	J4-12B	GND	CH118-
J4-13A	CH103	CH103+	J4-13B	CH119	CH119+
J4-14A	GND	CH103-	J4-14B	GND	CH119-
J4-15A	CH104	CH104+	J4-15B	CH120	CH120+
J4-16A	GND	CH104-	J4-16B	GND	CH120-
J4-17A	CH105	GND	J4-17B	CH121	GND
J4-18A	GND	GND	J4-18B	GND	GND
J4-19A	CH106	GND	J4-19B	CH122	GND
J4-20A	GND	GND	J4-20B	GND	GND
J4-21A	CH107	GND	J4-21B	CH123	GND
J4-22A	GND	GND	J4-22B	GND	GND
J4-23A	CH108	NC	J4-23B	CH124	NC
J4-24A	GND	NC	J4-24B	GND	NC
J4-25A	CH109	NC	J4-25B	CH125	NC
J4-26A	GND	NC	J4-26B	GND	NC
J4-27A	CH110	NC	J4-27B	CH126	NC
J4-28A	GND	NC	J4-28B	GND	NC
J4-29A	CH111	NC	J4-29B	CH127	NC
J4-30A	GND	NC	J4-30B	GND	NC
J4-31A	CH112	NC	J4-31B	CH128	NC
J4-32A	GND	NC	J4-32B	GND	NC
J4-33A	CSTROBE (DRB1)	CSTROBE[1] (DRB1)	J4-33B	CSTROBE (DRB2)	CSTROBE[1] (DRB2)
J4-34A	GND	NC	J4-34B	GND	NC

Note 1. Signal is single ended TTL.

Table 4-4 J4 I/O Connector Assignment

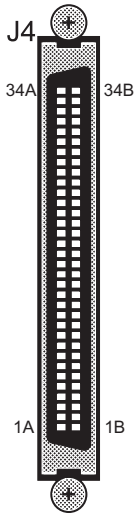


Figure 4-8 J4 Connector

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4.3.5 J5 I/O Connector

Table 4-5 lists the I/O channels assigned to J5.

Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic	Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic
J5-1A	CH129	CH129+	J5-1B	CH145	CH145+
J5-2A	GND	CH129-	J5-2B	GND	CH145-
J5-3A	CH130	CH130+	J5-3B	CH146	CH146+
J5-4A	GND	CH130-	J5-4B	GND	CH146-
J5-5A	CH131	CH131+	J5-5B	CH147	CH147+
J5-6A	GND	CH131-	J5-6B	GND	CH147-
J5-7A	CH132	CH132+	J5-7B	CH148	CH148+
J5-8A	GND	CH132-	J5-8B	GND	CH148-
J5-9A	CH133	CH133+	J5-9B	CH149	CH149+
J5-10A	GND	CH133-	J5-10B	GND	CH149-
J5-11A	CH134	CH134+	J5-11B	CH150	CH150+
J5-12A	GND	CH134-	J5-12B	GND	CH150-
J5-13A	CH135	CH135+	J5-13B	CH151	CH151+
J5-14A	GND	CH135-	J5-14B	GND	CH151-
J5-15A	CH136	CH136+	J5-15B	CH152	CH152+
J5-16A	GND	CH136-	J5-16B	GND	CH152-
J5-17A	CH137	GND	J5-17B	CH153	GND
J5-18A	GND	GND	J5-18B	GND	GND
J5-19A	CH138	GND	J5-19B	CH154	GND
J5-20A	GND	GND	J5-20B	GND	GND
J5-21A	CH139	GND	J5-21B	CH155	GND
J5-22A	GND	GND	J5-22B	GND	GND
J5-23A	CH140	NC	J5-23B	CH156	NC
J5-24A	GND	NC	J5-24B	GND	NC
J5-25A	CH141	NC	J5-25B	CH157	NC
J5-26A	GND	NC	J5-26B	GND	NC
J5-27A	CH142	NC	J5-27B	CH158	NC
J5-28A	GND	NC	J5-28B	GND	NC
J5-29A	CH143	NC	J5-29B	CH159	NC
J5-30A	GND	NC	J5-30B	GND	NC
J5-31A	CH144	NC	J5-31B	CH160	NC
J5-32A	GND	NC	J5-32B	GND	NC
J5-33A	CSTROBE (DRB3)	CSTROBE[1] (DRB3)	J5-33B	CSTROBE (DRB4)	CSTROBE[1] (DRB4)
J5-34A	GND	NC	J5-34B	GND	NC

Note 1. Signal is single ended TTL.

Table 4-5 J5 I/O Connector Assignments

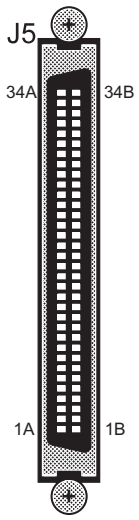


Figure 4-9 J5 Connector

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4.3.6 J6 I/O Connector

Table 4-6 lists the I/O channels assigned to J6.

Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic	Connector Pin No.	Standard IO Mnemonic	Differential IO Mnemonic
J6-1A	CH161	CH161+	J6-1B	CH177	CH177+
J6-2A	GND	CH161-	J6-2B	GND	CH177-
J6-3A	CH162	CH162+	J6-3B	CH178	CH178+
J6-4A	GND	CH162-	J6-4B	GND	CH178-
J6-5A	CH163	CH163+	J6-5B	CH179	CH179+
J6-6A	GND	CH163-	J6-6B	GND	CH179-
J6-7A	CH164	CH164+	J6-7B	CH180	CH180+
J6-8A	GND	CH164-	J6-8B	GND	CH180-
J6-9A	CH165	CH165+	J6-9B	CH181	CH181+
J6-10A	GND	CH165-	J6-10B	GND	CH181-
J6-11A	CH166	CH166+	J6-11B	CH182	CH182+
J6-12A	GND	CH166-	J6-12B	GND	CH182-
J6-13A	CH167	CH167+	J6-13B	CH183	CH183+
J6-14A	GND	CH167-	J6-14B	GND	CH183-
J6-15A	CH168	CH168+	J6-15B	CH184	CH184+
J6-16A	GND	CH168-	J6-16B	GND	CH184-
J6-17A	CH169	GND	J6-17B	CH185	GND
J6-18A	GND	GND	J6-18B	GND	GND
J6-19A	CH170	GND	J6-19B	CH186	GND
J6-20A	GND	GND	J6-20B	GND	GND
J6-21A	CH171	GND	J6-21B	CH187	GND
J6-22A	GND	GND	J6-22B	GND	GND
J6-23A	CH172	NC	J6-23B	CH188	NC
J6-24A	GND	NC	J6-24B	GND	NC
J6-25A	CH173	NC	J6-25B	CH189	NC
J6-26A	GND	NC	J6-26B	GND	NC
J6-27A	CH174	NC	J6-27B	CH190	NC
J6-28A	GND	NC	J6-28B	GND	NC
J6-29A	CH175	NC	J6-29B	CH191	NC
J6-30A	GND	NC	J6-30B	GND	NC
J6-31A	CH176	NC	J6-31B	CH192	NC
J6-32A	GND	NC	J6-32B	GND	NC
J6-33A	CSTROBE (DRB5)	CSTROBE[1] (DRB5)	J6-33B	CSTROBE (DRB6)	CSTROBE[1] (DRB6)
J6-34A	GND	NC	J6-34B	GND	NC

Note 1. Signal is single ended TTL.

Table 4-6 J6 I/O Connector Assignments

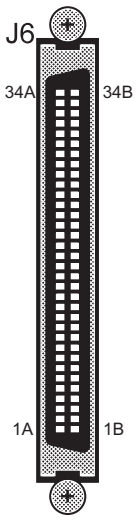


Figure 4-10 J6 Connector

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4.4 J8 Timing and Control Connector

This connector contains the timing and control signals that connects external control logic with timing sets TSA & TSB. Refer to appendix G for a detailed signal description.

The A and B designations of the J7, J8 and J9 connectors are reversed from the J1 through J6 connectors.

Table 4-7 lists the timing and control signals assigned to J8.

Connector	Mnemonic	Connector	Standard IO Mnemonic	Differential IO Mnemonic
J8-1B	TSOUTB1	J8-1A	TSOUTA1	TSOUTA1+
J8-2B	GND	J8-2A	GND	TSOUTA1-
J8-3B	TSOUTB2	J8-3A	TSOUTA2	TSOUTA2+
J8-4B	GND	J8-4A	GND	TSOUTA2-
J8-5B	TSOUTB3	J8-5A	TSOUTA3	TSOUTA3
J8-6B	GND	J8-6A	GND	GND
J8-7B	TSOUTB4	J8-7A	TSOUTA4	TSOUTA4
J8-8B	GND	J8-8A	GND	GND
J8-9B	TSOUTB5	J8-9A	TSOUTA5	TSOUTA5
J8-10B	GND	J8-10A	GND	GND
J8-11B	TSINPUTB1	J8-11A	TSINPUTA1	TSINPUTA1+
J8-12B	GND	J8-12A	GND	TSINPUTA1-
J8-13B	TSINPUTB2	J8-13A	TSINPUTA2	TSINPUTA2+
J8-14B	GND	J8-14A	GND	TSINPUTA2-
J8-15B	EXCLK2+	J8-15A	EXCLK1+	EXCLK1+
J8-16B	GND	J8-16A	GND	EXCLK1-
J8-17B	TSBBUSY-	J8-17A	TSABUSY-	TSABUSY-
J8-18B	GND	J8-18A	GND	GND
J8-19B	SYNCB-	J8-19A	SYNCA-	SYNCA-
J8-20B	GND	J8-20A	GND	GND
J8-21B	FCNTL2-	J8-21A	FCNTL1-	FCNTL1+
J8-22B	GND	J8-22A	GND	FCNTL1-
J8-23B	PROBDAT-	J8-23A	TCNTL1	TCNTL1
J8-24B	GND	J8-24A	GND	GND
J8-25B	UUTRST	J8-25A	TCNTL2	TCNTL2
J8-26B	GND	J8-26A	GND	GND
J8-27B	CLOCKB-	J8-27A	CLOCKA-	CLOCKA-
J8-28B	GND	J8-28A	GND	CLOCKA+
J8-29B	RCVRIN	J8-29A	TCNTL3	TCNTL3
J8-30B	GND	J8-30A	GND	GND

Table 4-7 J8 Connector Assignments

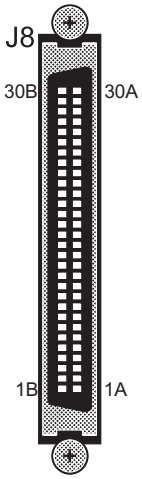


Figure 4-11 J8 Connector

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4.5 J7 Master/Slave Daisy Chain Connector

The Daisy Chain connector contains the signals necessary to synchronize multiple SR192's. Refer to appendix G for a detailed signal description. The cable assembly for master/slave SR192 operation is included when a master/slave SR192 configuration is ordered.

Table 4-8 lists the signals assigned to J7.

Connector	Mnemonic	Connector	Mnemonic
J7-1B	ERRORM-	J7-1A	EXCLKM+
J7-2B	GND	J7-2A	GND
J7-3B	COMPAREM-	J7-3A	SYNCTSM-
J7-4B	GND	J7-4A	GND
J7-5B	Reserved	J7-5A	STARTM-
J7-6B	GND	J7-6A	GND
J7-7B	Reserved	J7-7A	STOPM-
J7-8B	GND	J7-8A	GND
J7-9B	Reserved	J7-9A	TSINPUTM
J7-10B	GND	J7-10A	GND

Table 4-8 J7 Connector Assignments

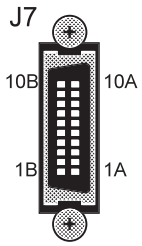


Figure 4-12 J7 Connector

4.6 J9 Probe/Reference Connector

The probe/reference I/O connector is used to either control the SR211 Probe Pod or monitor the reference signals from the SR110/SR210 DAC logic. The J9 factory default is set to the SR211 probe control signals. Refer to section 3.1.2.1 for details on changing the J9 signals to the reference signals. Refer to appendix G for a detailed signal description.

Table 4-9 lists the J9 signals.

Connector	SR211	Reference	Connector	SR211	Reference
J9-1B	PRBDO6	VOL2	J9-1A	PRBD00	VOL1
J9-2B	ODS-	VOL3	J9-2A	GND	GND
J9-3B	PRBD07	VOH2	J9-3A	PRBD01	VOH1
J9-4B	-24VSAFE	VOH3	J9-4A	GOOD0_IN	GND
J9-5B	DIR-	VIL2	J9-5A	PRBD02	VIL1
J9-6B	-24VSAFE	VIL3	J9-6A	GND	GND
J9-7B	DOR+	VIH2	J9-7A	PRBD03	VIH1
J9-8B	+24VSAFE	VIH3	J9-8A	GOOD1_IN	GND
J9-9B	IDS-	VISR2	J9-9A	PRBD04	VISR1
J9-10B	+24VSAFE	VISR3	J9-10A	GND	GND
J9-11B	GND	GND	J9-11A	NC	NC
J9-12B	GND	GND	J9-12A	GND	GND
J9-13B	GND	GND	J9-13A	PRBD05	GND
J9-14B	GND	GND	J9-14A	GND	GND

Table 4-9 J9 Connector Assignment

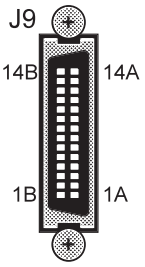


Figure 4-13 J9 Connector

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4.7 J10 Power Connector

The power connector is used to supply power to the driver chips. Refer to appendix G for a detailed signal description.

Table 4-10 lists the J10 signals.

Connector	Mnemonic	Connector	Mnemonic
J10-1	V1+	J10-9	V2+
J10-2	V1+	J10-10	GND
J10-3	GND	J10-11	V2-
J10-4	GND	J10-12	GND
J10-5	V1-	J10-13	V3+
J10-6	V1-	J10-14	GND
J10-7	GND	J10-15	V3-

Table 4-10 J10 Connector Assignments

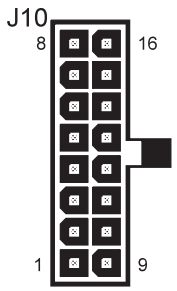


Figure 4-14 J10 Connector

4.8 SR192 Front Panel Mating Connectors

The following table lists the manufacturer part number and Talon order number for the front panel mating connectors.

Table 4-11 lists the manufacturers part numbers and Talons part numbers for the SR192 mating connectors.

Connector	Manufacturer Part Number	Talon Order Number
J1-J6	Robinson/Nugent P50-68-MDS-TG	SR305 (Qty. 2), SR301 (Qty. 6)
J7	Robinson/Nugent P25-20-S-TG	NA
J8	Robinson/Nugent P50-60-MDS-TG	SR301 (Qty 1)
J9	Robinson/Nugent P50-28-MDS-TG	SR301 (Qty 1)
J10	Molex 39-01-2160	SR301 (Qty 1)

Table 4-11 Mating Connector Part Numbers

Contact Talon for current pricing and availability on mating connectors and cable assemblies.

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5 Functional Description

The SR192 System is a “C” size, dual slot, VXI module. It was designed to be a modular system housing digital I/O modules, timing control modules and the VXI system circuitry. The Motherboard System is comprised of the front panel, motherboard and the CPU/VXI modules. The I/O modules plug into connectors located on the motherboard and are field replaceable.

Figure 5-1 depicts the major logic elements of the SR192 system.

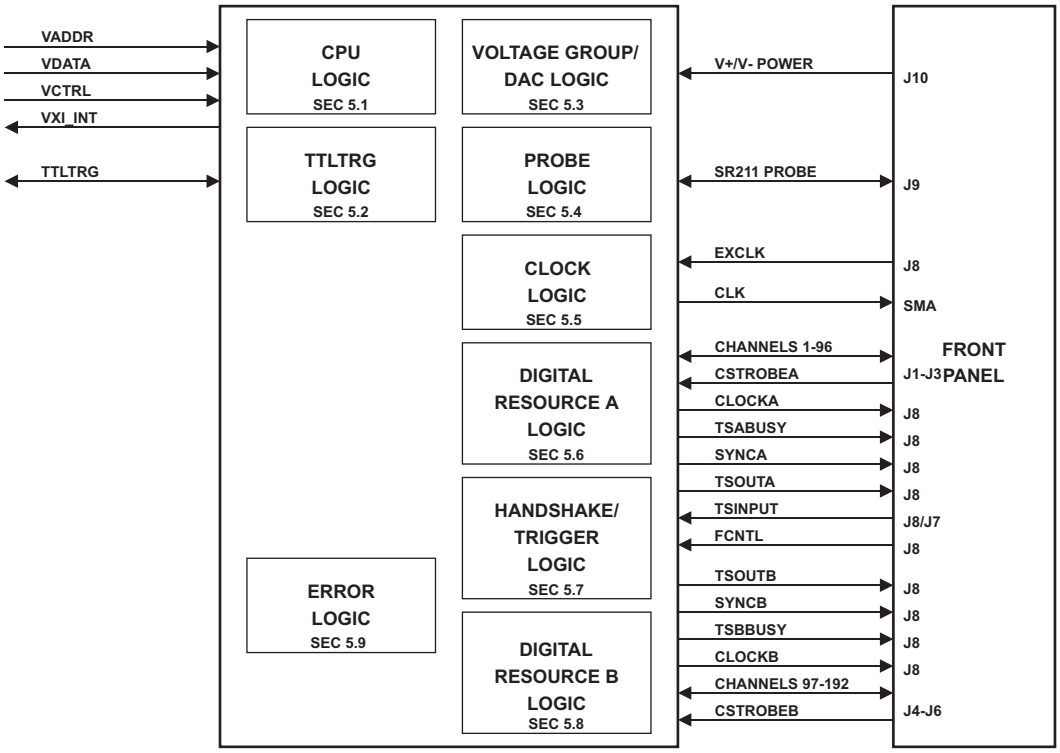


Figure 5-1 SR192 Block Diagram

The following list describes the functional blocks shown in figure above.

1. CPU logic — This logic controls the VXI backplane interface as well as the local CPU interface which is used to program the SR192 and its components.
2. TTLTRG logic — This logic allows the user to enable/disable SR192 signals to/from the VXI TTLTRG bus.
3. Voltage group/DAC logic — This logic distributes the external power inputs and internal reference levels to the Digital Resource and TSIO LOGIC.
4. Probe logic — This logic routes the SR211 probe signals to the FRONT PANEL.
5. Clock logic — This logic generates clock signals for the digital resources and also interfaces to the front panel.
6. Digital Resource A logic — This logic which consists of the TSA timing module and DRA1 through DRA6 I/O modules provides the stimulus/response logic for channels 1 through 96.
7. Handshake/trigger logic — This logic is used to distribute and synchronize the handshake signals to both Digital Resource blocks.
8. Digital Resource B logic — This logic which consists of the TSB timing module and DRB1 through DRB6 I/O modules provides the stimulus/response logic for channels 97 through 192.
9. Error logic — This logic monitors the real time error bits from Digital Resource A and records response error data.

The following list describes the signals shown in figure 5-1.

1. VADDR — The address bus from the VXI bus backplane.
2. VDATA — The data bus from the VXI bus backplane.
3. VCTRL — The control bus from the VXI bus backplane.
4. VXI_INT — Selected VXI interrupt signal from SW1.
5. TTLTRG — The TTL Trigger bus from the VXI bus backplane.

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6.	V+/V- POWER	The positive and negative input voltage used to supply power to the variable voltage driver/receiver modules.
7.	SR211 PROBE	The signals used to control the SR211 probe pod.
8.	EXCLK	Two external clocks routed to both timing modules.
9.	CLK	The three programmable clock outputs (CLKA, CLKB and CLKC) as well as the external clock reference input (CLKREF).
10.	CHANNELS 1-96	96 I/O signals routed to DRA1 through DRA6 I/O module slots.
11.	CSTROBEA	6 input signals. One signal routed to each I/O module DRA slot.
12.	CLOCKA	Selected clock for digital resource A.
13.	TSABUSY	Active low signal that indicates that digital resource A is running.
14.	SYNCA	Programmable output trigger from the TSA timing module.
15.	TSOUTA	General purpose output handshake/trigger signals from the TSA timing module.
16	TSINPUT	Five general purpose trigger/handshake inputs, two routed to TSA and two routed to TSB. The fifth routed to both for synchronous triggering in linked and master/slave mode.
17.	FCNTL	Two external I/O control signals routed to all I/O modules and error logic.
18.	TSOUTB	General purpose output handshake/trigger signals from the TSB timing module.
19.	SYNCB	Programmable output trigger from the TSB timing module.
20.	TSBBUSY	Active low signal that indicates that digital resource B is running.
21.	CLOCKB	Selected clock for digital resource B.
22.	CHANNELS 97-192	96 I/O signals routed to DRB1 through DRB6 I/O module slots.
23.	CSTROBEB	6 input signals. One signal routed to each I/O module DRB slot.

The following sections describe the nine logic elements of the SR192.

5.1 CPU Logic

The CPU logic performs the VXI interface management as well as the SCPI command language control.

The VXI interface management involves the A16 registers and the Word Serial (WS) commands that the SR192 supports. The SR192 programming manual describes the WS commands that the SR192 responds to.

The SCPI command language control includes the command parser as well as the execution control software. The SR192 programming manual lists all the SCPI commands of the SR192.

Figure 5-2 shows the CPU logic block diagram.

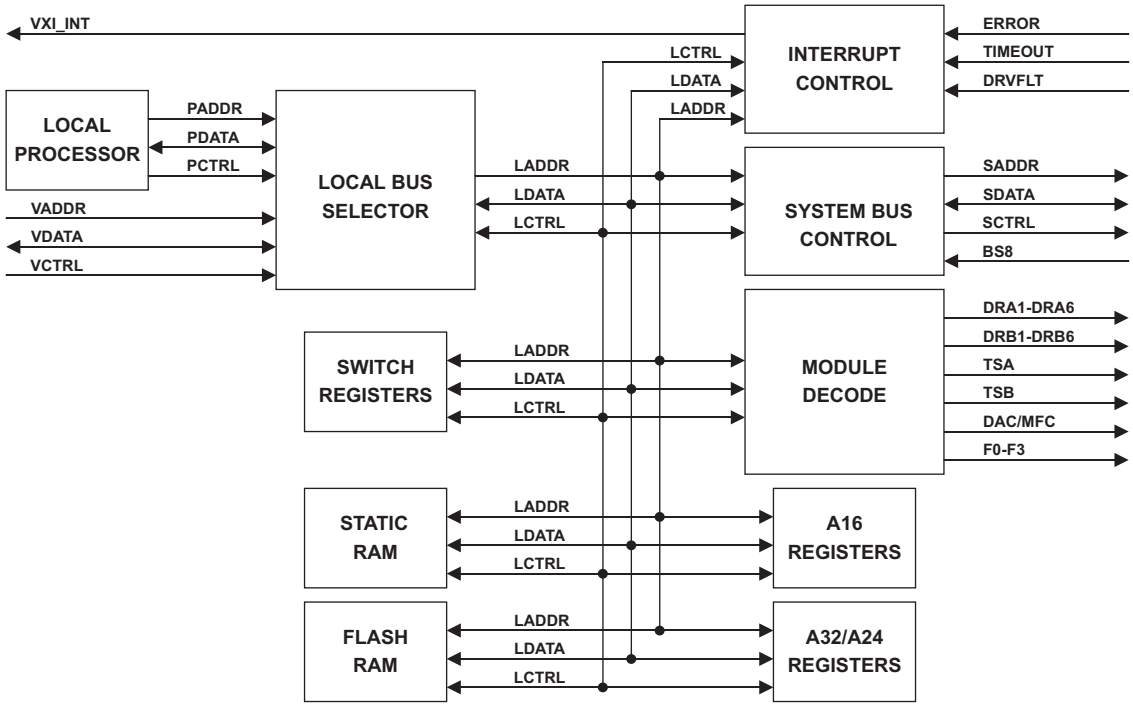


Figure 5-2 CPU Logic Block Diagram

The following list describes the functional blocks above.

1.	Local processor	The local processor manages the VXI interface as well as SCPI command parser.
2.	Local bus selector	This logic controls the local bus arbitration between the VXI bus and the processor bus.

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3. Switch registers — The switch register are read by the CPU on power-up in order to assign the logical address and VXI interrupt level.
4. Static RAM — The static RAM is used by the SCPI parser and execution firmware as allocable heap memory. The static RAM is also used to update the flash firmware.
5. Flash RAM — The flash RAM contains the local processor code and SCPI parser.
6. Interrupt control — VXI interrupts can be generated by real time events or by the local processor.
7. System bus control — This logic manages byte/word data sent to or read from any of the I/O of timing modules.
8. Module decode — The module decodes along with the function code (F0-F3) identifies a specific module and register page.
9. A16 registers — The A16 registers are defined by the VXI standard, see appendix B.
10. A32/A24 registers — The A32/A24 registers are defined in appendix B.

The following list describes the signals from figure 5-2.

1. VXI_INT — Selected VXI interrupt line.
2. PADDR — Processor address bus.
3. PDATA — Processor data bus.
4. PCTRL — Processor control bus.
5. VADDR — VXI address bus.
6. VDATA — VXI data bus.
7. VCTRL — VXI control bus.
8. LADDR — Local address bus.
9. LDATA — Local data bus.
10. LCTRL — Local control bus.
11. ERROR — Real time error from the Digital Resources.
12. TIMEOUT — Input trigger timeout from the Digital Resources.
13. DRVFLT — Variable Voltage drivers over current flag.
14. SADDR — Selected address bus to the timing modules.
15. SDATA — Selected data bus to the timing and I/O modules.
16. SCTRL — Selected control bus to the timing and I/O modules.
17. BS8 — Module bus size flag from the timing and I/O modules.
18. DRA1-DRA6 — Digital Resource A I/O module decodes.
19. DRB1-DRB6 — Digital Resource B I/O module decodes.
20. TSA — Digital Resource A timing module decode.
21. TSB — Digital Resource B timing module decode.
22. DAC/MFC — Reference/multifunction module decode.
23. F0-F3 — Module function code select signals.

5.2 TTLTRG Logic

The TTLTRG bus from the VXI backplane is an open collector, daisy chained bus used for cross-triggering multiple instruments.

Figure 5-3 shows the TTLTRG logic block diagram.

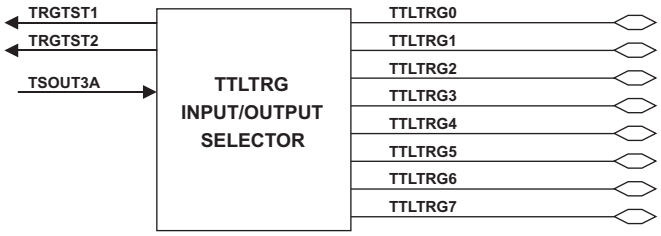


Figure 5-3 TTLTRG Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. TTLTRG input/output select — This logic selects routs signals to and from the VXI TTLTRG bus.

The following list describes the signals listed in figure 5-3.

1. TRGTST1 — Input trigger sourced by one of the VXI TTLTRG lines that is routed to the timing module of digital resource A (TSA). Refer to section 5.7.2.
2. TRGTST2 — Input trigger sourced by one of the VXI TTLTRG lines that is routed to the timing module of digital resource B (TSB). Refer to section 5.7.2.
3. TSOUT3A — One of the five output triggers from the TSA timing module.
4. TTLTRG0-TTLTRG7 — Eight TTL trigger lines to/from the VXI backplane.

5.3 Voltage Group/DAC Logic

Several of Talon's SR192 I/O modules contain Variable Voltage drivers/receivers. These Variable Voltage driver/receivers require reference signals to define input and output levels.

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Figure 5-4 shows the voltage group logic of the SR192 motherboard.

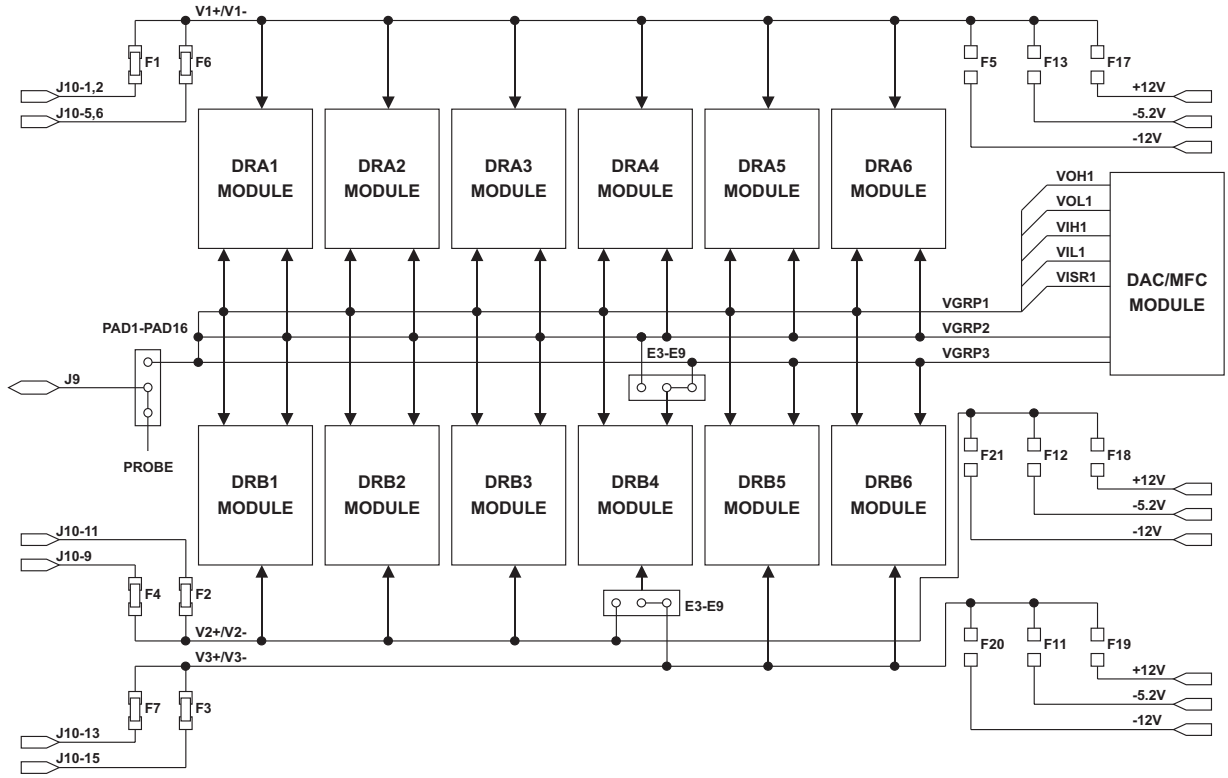


Figure 5-4 Voltage Group Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. PAD1-PAD16 — 16 surface mount PCB pads used to select the front panel J9 signals. See section 3.1.2.1.
2. DRA1 module — The logic and memories for I/O channels 1-16.
3. DRA2 module — The logic and memories for I/O channels 17-32.
4. DRA3 module — The logic and memories for I/O channels 33-48.
5. DRA4 module — The logic and memories for I/O channels 49-64.
6. DRA5 module — The logic and memories for I/O channels 65-80.
7. DRA6 module — The logic and memories for I/O channels 81-96.
8. DRB1 module — The logic and memories for I/O channels 97-112.
9. DRB2 module — The logic and memories for I/O channels 113-128.
10. DRB3 module — The logic and memories for I/O channels 129-144.
11. DRB4 module — The logic and memories for I/O channels 145-160.
12. DRB5 module — The logic and memories for I/O channels 161-176.
13. DRB6 module — The logic and memories for I/O channels 177-192.
14. DAC/MFC module — The logic that generates the three voltage group references.

The following list describes the signals shown in figure 5-4.

1. J10-<n> — External voltage inputs from the J10 front panel connector.
2. F<n> — Motherboard fuses used for selecting the voltage source of the variable voltage modules.
3. V1+/V1- — Voltage group one positive and negative input voltages.
4. +12V — +12 volt signal from the VXI backplane.
5. -5.2V — -5.2 volt signal from the VXI backplane.
6. -12V — -12 volt signal from the VXI backplane.
7. VOH1 — Output high level for VGRP1.
8. VOL1 — Output low level for VGRP1.
9. VIH1 — Input high threshold for VGRP1.
10. VIL1 — Input low threshold for VGRP1.
11. VISR1 — Driver slew rate voltage for VGRP1.
12. VGRP1 — Voltage group one levels and thresholds.
13. VGRP2 — Voltage group two levels and thresholds.
14. VGRP3 — Voltage group three levels and thresholds.
15. J9 — Front panel connector I/O.
16. PROBE — Signals used for the SR211 data probe.
17. E3-E9 — Jumpers used to select the voltage group and input voltage source for DRB4.
18. V2+/V2- — Voltage group two positive and negative input voltages.
19. V3+/V3- — Voltage group three positive and negative input voltages.

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Talon has developed two types of variable voltage I/O modules, single and dual reference. Table 5-1 below explains how the voltage groups are routed to both types of modules.

Reference	Voltage Group Assignment					
	DRA1-DRA6		DRB1-DRB3		DRB4-DRB6	
	Single	Dual	Single	Dual	Single	Dual
REFA	VGRP1	VGRP1	VGRP2	VGRP1	VGRP3[1]	VGRP1
REFB	NA	VGRP2	NA	VGRP2	NA	VGRP3[1]

Note 1: DRB4 Can be jumpered to select either VGRP3 (default) or VGRP2, see section 3.1.2.4

Table 5-1 Single and Dual Reference Voltage Group Assignments

5.4 Probe Logic

Talons SR210 DAC/MFC Accessory module contains interface logic for the SR211 Probe Pod. Figure 5-5 shows the probe logic of the SR192 motherboard.

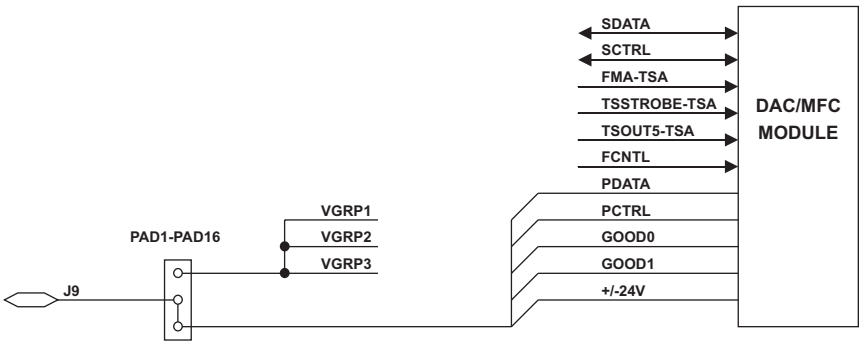


Figure 5-5 Probe Logic Block Diagram

The following list describes the functional blocks listed above.

1. PAD1-PAD16 — 16 surface mount PCB pads used to select the front panel J9 signals. See section 3.1.2.1.
2. DAC/MFC — The logic and drivers for SR211 probe pod interface.

The following list describes the signals shown in figure 5-5.

1. J9 — Front panel connector I/O.
2. VGRP1 — Voltage group one levels and thresholds.
3. VGRP2 — Voltage group two levels and thresholds.
4. VGRP3 — Voltage group three levels and thresholds.
5. SDATA — Selected data bus to the timing and I/O modules.
6. SCTRL — Selected control bus to the timing and I/O modules.
7. FMA-TSA — Memory address bus from the TSA timing module.
8. TSSTROBE-TSA — Two input strobe signals from the TSA timing module that can be selected as the probe data clock.
9. TSOUT5-TSA — General purpose output signal from the TSA timing module that can be selected as the probe data clock.
10. FCNTL — Two external I/O control signals. routed to all I/O modules that can be selected as the probe data strobe.
11. PDATA — Probe data bus used to send/receive commands or data to the SR211 pod.
12. PCTRL — Probe control bus used to send/receive commands or data to the SR211 pod.
13. GOOD0 — Input signal from the SR211 pod that indicates a valid low signal.
14. GOOD1 — Input signal from the SR211 pod that indicates a valid high signal.
15. +/-24V — Fused +24V and -24V from the VXI backplane.

5.5 Clock Logic

The timing modules on the SR192 operate using a single clock to which the stimulus/response addresses and control signals are synchronized. This clock, called TS_CLK, can be selected from several sources.

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Figure 5-6 shows the clock logic of the SR192 motherboard.

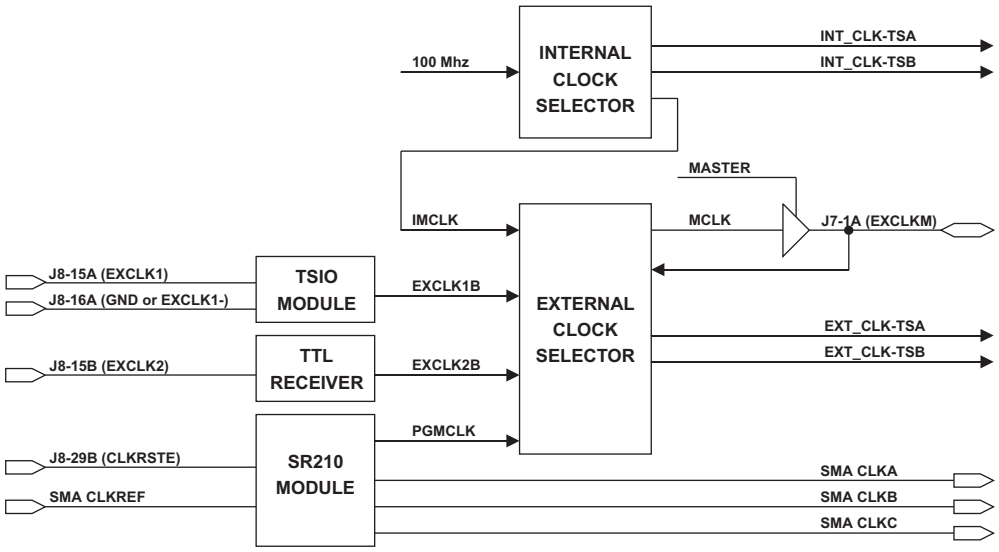


Figure 5-6 Clock Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. TSIO module — Receiver for EXCLK1 for the timing modules.
2. TTL receiver — Receiver for EXCLK2 for the timing modules.
3. SR210 module — SR210 accessory module.
4. Internal clock selector — This logic generates the internal 10, 20 or 50 MHz clock frequency for both TSA and TSB timing modules.
5. External clock selector — This logic selects the external clock source for both TSA and TSB timing modules.

The following list describes the signals shown in the figure 5-6.

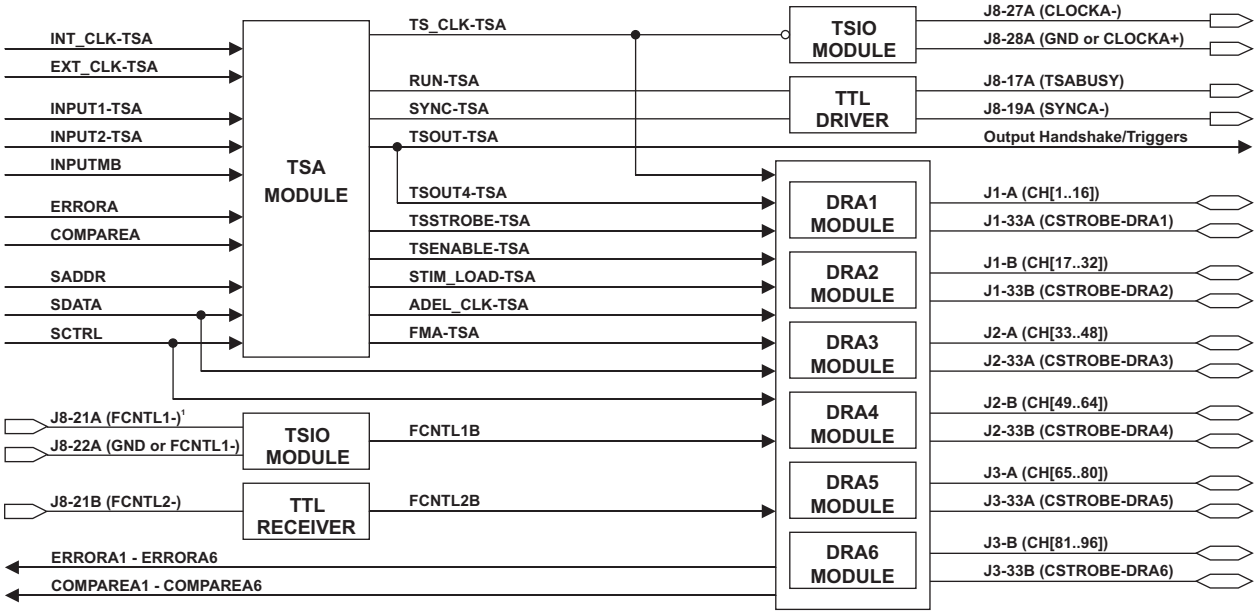
1. J8-15A (EXCLK1) — TTL, Variable Voltage or differential clock one from the front panel.
2. J8-16A (GND or EXCLK1-) — Differential compliment of EXCLK1 or signal ground for TTL and Variable Voltage.
3. J8-15B (EXCLK2) — TTL clock two from the front panel.
4. J8-29B (CLKRSTE) — TTL clock reset signal for the programmable clock logic.
5. SMA CLKREF — TTL clock generator reference signal for the programmable clock logic.
6. 100 MHz — Internal clock used to generate the 50/20/10 MHz clocks to the timing modules.
7. IMCLK — Internal J7 master bus clock (EXCLKM) setting.
8. EXCLK1B — Buffered external clock one signal.
9. EXCLK2B — Buffered external clock two signal.
10. PGMCLK — Programmable clock signal from the SR210 installed in the DAC/MFC slot.
11. MASTER — Signal used to enable the driver for the synchronized clock routed to the J7 connector.
12. MCLK — Selected master clock signal. Valid choices are EXCLK1, EXCLK2, 10MHz, 20MHz, 50MHz or PGMCLK.
13. INT_CLK-TSA — Selected TSA internal clock signal. Valid choices are 10MHz, 20MHz or 50MHz.
14. INT_CLK-TSB — Selected TSB internal clock signal. Valid choices are 10MHz, 20MHz or 50MHz.
15. J7-1A (EXCLKM) — Synchronized clock for master/slave functions.
16. EXT_CLK-TSA — Selected TSA external clock signal. Valid choices are EXCLK1, EXCLK2, EXCLKM or PGMCLK.
17. EXT_CLK-TSB — Selected TSB external clock signal. Valid choices are EXCLK1, EXCLK2, EXCLKM or PGMCLK.
18. SMA CLKA — TTL PGMCLK1 output.
19. SMA CLKB — TTL PGMCLK2 output.
20. SMA CLKC — Variable Voltage +8V to -8V PGMCLK2 output.

5.6 Digital Resource A Logic

The SR192 can contain two independent Digital Resources which are comprised of a timing module and one or more I/O modules. Digital Resource A can be synchronized to an external source through the J7 master/slave connector.

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Figure 5-7 shows the Digital Resource A logic of the SR192.



Note 1: FCNTL1 differential input inverted.

Figure 5-7 Digital Resource A Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	TSA module	Timing module that generates the word address and control signals for I/O channels 1 through 96.
2.	TSIO module	Receiver for FCNTL1 for the I/O modules.
3.	TTL Receiver	Receiver for FCNTL2 for the I/O modules.
4.	TTL driver	Driver for SYNCA from TSA.
5.	DRA1 module	The logic and memories for I/O channels 1-16.
6.	DRA2 module	The logic and memories for I/O channels 17-32.
7.	DRA3 module	The logic and memories for I/O channels 33-48.
8.	DRA4 module	The logic and memories for I/O channels 49-64.
9.	DRA5 module	The logic and memories for I/O channels 65-80.
10.	DRA6 module	The logic and memories for I/O channels 81-96.

The following list describes the signals shown in figure 5-7

1.	INTCLK-TSA	Selected internal clock.
2.	EXTCLK-TSA	Selected external or J7 master bus clock.
3.	INPUT1-TSA	Test input one for TSA.
4.	INPUT2-TSA	Test input two for TSA.
5.	INPUTMB	Synchronized test input.
6.	ERRORA	Error flag from the error logic, see section 5.9
7.	COMPAREA	Compare flag from the error logic, see section 5.9.
8.	SADDR	Selected address bus to the timing modules.
9.	SDATA	Selected data bus to the timing and I/O modules.
10.	SCTRL	Selected control bus to the timing and I/O modules.
11.	J8-21A (FCNTL1-)	TTL, Variable Voltage or differential strobe/enable one to the I/O modules. Differential input inverted.
12.	J8-22A (GND or FCNTL1-)	Differential compliment of FCNTL1 or signal ground for TTL and Variable Voltage.
13.	J8-21B (FCNTL2-)	TTL I/O strobe/enable two to the I/O modules.
14.	ERRORA1 - ERRORA6	Real time error flag from each I/O module.
15.	COMPAREA1 - COMPAREA6	Real time compare flag from each I/O module.
16.	TS_CLK-TSA	Selected TSA timing clock.
17.	RUN-TSA	TSA running signal.
18.	SYNC-TSA	Programmable output sync.
19.	TSOUT-TSA	TSOUT handshake/trigger signals, see section 5.7.1.
20.	TSOUT4-TSA	I/O module algorithm enable.
21.	TSSTROBE-TSA	Two internal response strobe signals.
22.	TSENABLE-TSA	Two internal stimulus enable signals.
23.	STIM_LOAD-TSA	I/O module control signal used to load stimulus memory and latch the response address.
24.	ADEL_CLK-TSA	I/O module control signal used to latch the response address.
25.	FMA-TSA	I/O module stimulus/response memory address bus.
26.	FCNTL1B	Buffered FCNTL1 signal.

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27.	FCNTL2B	Buffered FCNTL2 signal.
28.	J8-27A (CLOCKA-)	TTL, Variable Voltage or differential output of CLOCK-TSA.
29.	J8-28A (GND or CLOCKA+)	Differential compliment of CLOCK-TSA or signal ground for TTL and Variable Voltage.
30.	J8-17A (TSABUSY)	TSA running signal
31.	J2-19A (SYNCA-)	Programmable output sync.
32.	J1-A (CH[1..16])	I/O channels 1-16.
33.	J1-33A (CSTROBE-DRA1)	CSTROBE for DRA1.
34.	J1-B (CH[17..32])	I/O channels 17-32.
35.	J1-33B (CSTROBE-DRA2)	CSTROBE for DRA2
36.	J2-A (CH[33..48])	I/O channels 33-48.
37.	J2-33A (CSTROBE-DRA3)	CSTROBE for DRA3
38.	J2-B (CH[49..64])	I/O channels 49-64.
39.	J2-33B (CSTROBE-DRA4)	CSTROBE for DRA4.
40.	J3-A (CH[65..80])	I/O channels 65-80.
41.	J3-33A (CSTROBE-DRA5)	CSTROBE for DRA5.
42.	J3-B (CH[81..96])	I/O channels 81-96.
43.	J3-33B (CSTROBE-DRA6)	CSTROBE for DRA6

5.7 Handshake/Trigger Logic

The SR192 routes output and input handshake/trigger signals to the two timing modules, TSA and TSB. Each timing module has five general purpose output signals (TSOUT1 through TSOUT5) and two test input signals (TSINPUT1 and TSINPUT2). The following sections describes the motherboard routing logic for these signals.

5.7.1 Output Handshake/Trigger Logic (TSOUT)

Figure 5-8 shows the output logic of the SR192 motherboard.

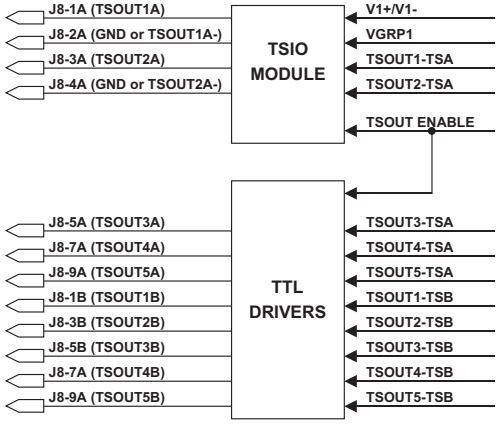


Figure 5-8 Output Trigger Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	TSIO module	Drivers for TSOUT1 and TSOUT2 from the TSA timing module.
2.	TTL drivers	Drivers for TSOUT3 through TSOUT5 from TSA and TSOUT1 through TSOUT5 from TSB.

The following list describes the signals shown in figure 5-8.

1.	J8-1A (TSOUT1A)	TTL, Variable Voltage or differential output of TSOUT1-TSA.
2.	J8-2A (GND or TSOUT1A-)	Differential compliment of TSOUT1-TSA or signal ground for TTL and Variable Voltage.
3.	J8-3A (TSOUT2A)	TTL, Variable Voltage or differential output of TSOUT2-TSA.
4.	J8-4A (GND or TSOUT2A-)	Differential compliment of TSOUT2-TSA or signal ground for TTL and Variable Voltage.
5.	J8-5A (TSOUT3A)	TTL output of TSOUT3-TSA.
6.	J8-7A (TSOUT4A)	TTL output of TSOUT4-TSA.
7.	J8-9A (TSOUT5A)	TTL output of TSOUT5-TSA.
8.	J8-1B (TSOUT1B)	TTL output of TSOUT1-TSB.
9.	J8-3B (TSOUT2B)	TTL output of TSOUT2-TSB.
10.	J8-5B (TSOUT3B)	TTL output of TSOUT3-TSB.
11.	J8-7B (TSOUT4B)	TTL output of TSOUT3-TSB.
12.	J8-9B (TSOUT5B)	TTL output of TSOUT4-TSB.
13.	V1+/V1-	Voltage group one input supply for TSOUT1A and TSOUT2A Variable Voltage outputs.
14.	VGRP1	Voltage group one reference signals for TSOUT1A and TSOUT2A Variable Voltage outputs.
15.	TSOUT1-TSA	TSOUT1 signal from the TSA timing module.
16.	TSOUT2-TSA	TSOUT2 signal from the TSA timing module.
17.	TSOUT ENABLE	User controlled output enable signal.
18.	TSOUT3-TSA	TSOUT3 signal from the TSA timing module.

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19. TSOUT4-TSA — TSOUT4 signal from the TSA timing module.
20. TSOUT5-TSA — TSOUT5 signal from the TSA timing module.
21. TSOUT1-TSB — TSOUT1 signal from the TSB timing module.
22. TSOUT2-TSB — TSOUT2 signal from the TSB timing module.
23. TSOUT3-TSB — TSOUT3 signal from the TSB timing module.
24. TSOUT4-TSB — TSOUT4 signal from the TSB timing module.
25. TSOUT5-TSB — TSOUT5 signal from the TSB timing module.

5.7.2 Test Input Handshake/Trigger Logic (TSINPUT)

Figure 5-9 shows the test input logic of the SR192 motherboard.

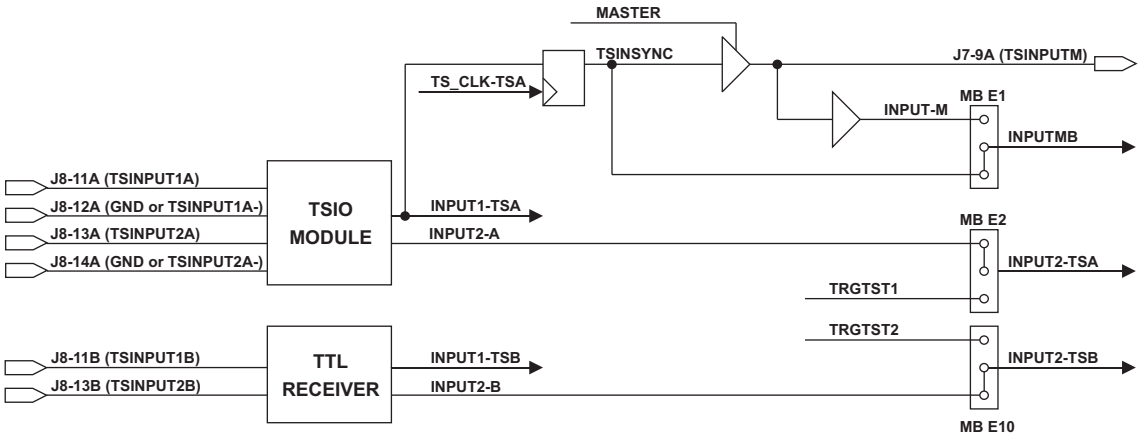


Figure 5-9 Input Trigger Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. TSIO module — Receivers for TSINPUT1A and TSINPUT2A for the TSA timing module.
2. TTL receiver — Receivers for TSINPUT1B and TSINPUT2B for the TSB timing module.
3. MB E1 — Motherboard jumper block E1, see section 3.1.2.2.
4. MB E2 — Motherboard jumper block E2, see section 3.1.2.3.
5. MB E10 — Motherboard jumper block E10, see section 3.1.2.5.

The following list describes the signals shown in the figure 5-9 above.

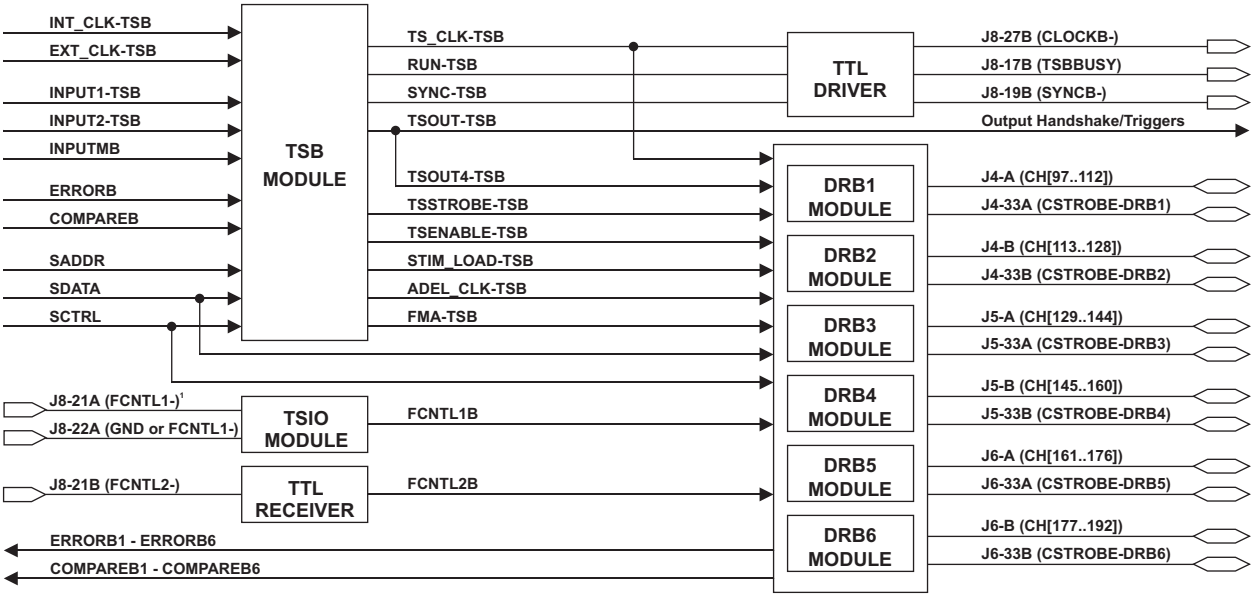
1. J8-11A (TSINPUT1A) — TTL, Variable Voltage or differential test input one to the TSA timing module.
2. J8-12A (GND or TSINPUT1A-) — Differential compliment of TSINPUT1A or signal ground for TTL and Variable Voltage.
3. J8-13A (TSINPUT2A) — TTL, Variable Voltage or differential test input two to the TSB timing module.
4. J8-14A (GND or TSINPUT2A-) — Differential compliment of TSINPUT2A or signal ground for TTL and Variable Voltage.
8. J8-11B (TSINPUT1B) — TTL test input one to the TSB timing module.
9. J8-13B (TSINPUT2B) — TTL test input two to the TSB timing module.
10. TS_CLK-TSA — Timing set clock from the TSA timing module used to synchronize the INPUT1-TSA signal.
11. INPUT1-TSA — Test input one routed to the TSA timing module.
12. INPUT2-A — Front panel test input two for the TSA timing module.
13. INPUT1-TSB — Test input one routed to the TSB timing module.
14. INPUT2-B — Front panel test input two for the TSB timing module.
15. MASTER — Signal used to enable the driver for the synchronized input trigger routed to the J7 connector.
16. TSINSYNC — Synchronized test input.
17. J7-9A (TSINPUTM) — Master/slave test input.
18. INPUT-M — Buffered test input from the master/slave connector.
19. INPUTMB — Synchronized test input routed to both TSA and TSB timing modules.
20. INPUT2-TSA — Test input two routed to the TSA timing module.
21. TRGTST1 — Selected TTL trigger from the VXI backplane, see section 5.2.
22. TRGTST2 — Selected TTL trigger from the VXI backplane, see section 5.2.
23. INPUT2-TSB — Test input two routed to the TSB timing module.

5.8 Digital Resource B Logic

Digital resource B can be synchronized to either digital resource A or an external source through the J7 master/slave connector.

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Figure 5-10 shows the Digital Resource B logic of the SR192.



Note 1: FCNTL1 differential input inverted.

Figure 5-10 Digital Resource B Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	TSB module	Timing module that generates the word address and control signals for I/O channels 1 through 96.
2.	TSIO module	Receiver for FCNTL1 for the I/O modules.
3.	TTL Receiver	Receiver for FCNTL2 for the I/O modules.
4.	TTL driver	Drivers for CLOCKB and SYNCB from TSB.
5.	DRB1 module	The logic and memories for I/O channels 97-112.
6.	DRB2 module	The logic and memories for I/O channels 113-128.
7.	DRB3 module	The logic and memories for I/O channels 129-144.
8.	DRB4 module	The logic and memories for I/O channels 145-160.
9.	DRB5 module	The logic and memories for I/O channels 161-176.
10.	DRB6 module	The logic and memories for I/O channels 177-192.

The following list describes the signals shown in figure 5-10.

1.	INT_CLK-TSB	Selected internal clock.
2.	EXTCLK-TSB	Selected external or J7 master bus clock.
3.	INPUT1-TSB	Test input one for TSB.
4.	INPUT2-TSB	Test input two for TSB.
5.	INPUTMB	Synchronized test input.
6.	ERRORB	Error flag from the error logic, see section 5.9
7.	COMPAREB	Compare flag from the error logic, see section 5.9.
8.	SADDR	Selected address bus to the timing modules.
9.	SDATA	Selected data bus to the timing and I/O modules.
10.	SCTRL	Selected control bus to the timing and I/O modules.
11.	J8-21A (FCNTL1-)	TTL, Variable Voltage or differential strobe/enable one to the I/O modules. Differential input inverted.
12.	J8-22A (GND or FCNTL1-)	Differential compliment of FCNTL1 or signal ground for TTL and Variable Voltage.
13.	J8-21B (FCNTL2-)	TTL I/O strobe/enable two to the I/O modules.
14.	ERRORB1 - ERRORB6	Real time error flag from each I/O module.
15.	COMPAREB1 - COMPAREB6	Real time compare flag from each I/O module.
16.	TS_CLK-TSB	Selected TSB timing clock (TS_CLK).
17.	RUN-TSB	TSB running signal.
18.	SYNC-TSB	Programmable output sync.
19.	TSOUT-TSB	TSOUT trigger signals, see section 5.7.1.
20.	TSOUT4-TSB	I/O module algorithm enable.
21.	TSSTROBE-TSB	Two internal response strobe signals.
22.	TSENABLE-TSB	Two internal stimulus enable signals.
23.	STIM_LOAD-TSB	I/O module control signal used to load stimulus memory and latch the response address.
24.	ADEL_CLK-TSB	I/O module control signal used to latch the response address.
25.	FMA-TSB	I/O module stimulus/response memory address bus.
26.	FCNTL1B	Buffered FCNTL1 signal.

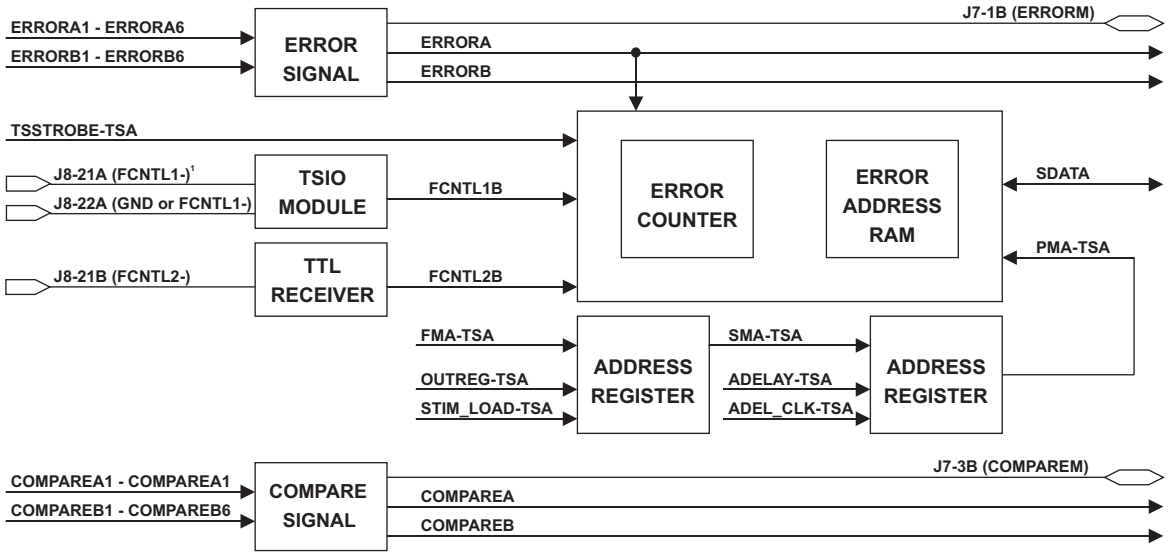
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27.	FCNTL2B	Buffered FCNTL2 signal.
28.	J8-27B (CLOCKB-)	TTL output of TS_CLK-TSB.
29.	J8-17B (TSBBUSY)	TSB running signal.
30.	J2-19B (SYNCB-)	Programmable sync trigger.
31.	J4-A (CH[97-112])	I/O channels 97-112 .
32.	J4-33A (CSTROBE-DRB1)	CSTROBE for DRB1.
33.	J4-B (CH[113..128])	I/O channels 113-128 .
34.	J4-33B (CSTROBE-DRB2)	CSTROBE for DRB2
35.	J5-A (CH[129..144])	I/O channels 129-144 .
36.	J5-33A (CSTROBE-DRB3)	CSTROBE for DRB3
37.	J5-B (CH[145..160])	I/O channels 145-160 .
38.	J5-33B (CSTROBE-DRB4)	CSTROBE for DRB4.
39.	J6-A (CH[161..176])	I/O channels 161-176 .
40.	J6-33A (CSTROBE-DRB5)	CSTROBE for DRB5.
41.	J6-B (CH177..192])	I/O channels 177-192 .
42.	J6-33B (CSTROBE-DRB6)	CSTROBE for DRA6

5.9 Error Logic

The error logic monitors the real time error signals from both timing modules and counts the number of errors during a Digital Resource A pattern sequence. In addition the pattern address of each error is recorded in a static RAM that can be queried by the user.

Figure 5-11 shows the error logic of the SR192.



Note 1: FCNTL1 differential input inverted.

Figure 5-11 Error Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	Error signal	Logic that 'OR's the error signals from all the I/O modules and the J7 connector into separate error flags for TSA and TSB.
2.	TSIO module	Receiver for FCNTL1 for the I/O modules.
3.	TTL Receiver	Receiver for FCNTL2 for the I/O modules.
4.	Compare signal	Logic that 'AND's the compare signals from all the I/O modules and the J7 connector into separate compare flags for TSA and TSB.
5.	Error counter	This logic samples the TSA error flag and increments by one when an error is recorded.
6.	Error address RAM	The FMA address of the response word that generated an error is stored when an error is recorded.
7.	Address register	These registers duplicate the address logic on the I/O modules in order to synchronize the stimulus address with the response address.

The following list describes the signals shown in figure 5-11.

1.	ERRORA1 - ERRORA6	Real time error flag from each TSA I/O module.
2.	ERRORB1 - ERRORB6	Real time error flag from each TSB I/O module.
3.	TSSTROBE-TSA	Two internal response strobe signals.
4.	J8-21A (FCNTL1-)	TTL, Variable Voltage or differential strobe/enable one to the I/O modules. Differential input inverted.
5.	J8-22A (GND or FCNTL1-)	Differential compliment of FCNTL1 or signal ground for TTL and Variable Voltage.
6.	J8-21B (FCNTL2-)	TTL I/O strobe/enable two to the I/O modules.

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7. COMPAREA1-COMPAREA6 Real time compare flag from each TSA I/O module.
8. COMPAREB1-COMPAREB6 Real time compare flag from each TSB I/O module.
7. ERRORM Error flag (open collector 'OR') to/from the J7 master/slave connector.
8. ERRORA Error flag to the TSA timing module and error counter/RAM logic.
9. ERRORB Error flag to the TSB timing module.
10. FCNTL1B Buffered FCNTL1 signal.
11. FCNTL2B Buffered FCNTL2 signal.
12. FMA-TSA Stimulus/response address bus from the TSA timing module.
13. OUTREG-TSA Output register mode control from the TSA timing module.
14. STIM_LOAD-TSA STIM_LOAD control signal from the TSA timing module.
15. COMPAREM Compare flag (open collector 'AND') to/from the J7 master/slave connector.
16. COMPAREA Compare flag to the TSA timing module.
17. COMPAREB Compare flag to the TSB timing module.
18. SMA-TSA Registered/buffered FMA address.
19. ADELAY-TSA Address delay mode control from the TSA timing module.
20. ADEL_CLK-TSA ADEL_CLK control signal from the TSA timing module.
21. PMA-TSA Registered/buffered SMA address.
22. SDATA Selected data bus.

5.9.1 Error Signal Generation

The error signals from both digital resources as well as the front panel master/slave connector (J7) can be programmed to generate a single error flag that can be tested. Table 5-2 illustrates how the error flags are generated.

SR192 Setting	ERRORA TRUE if	ERRORB TRUE if	ERRORM TRUE if
SR192 Independent, TSA/TSB not linked	Any ERRORA<n> signal true.	Any ERRORB<n> signal true.	N/A
SR192 Independent, TSA/TSB linked	Any ERRORA<n> or ERRORB<n> signal true.		N/A
SR192 Master/slave, TSA/TSB not linked	Any ERRORA<n> or ERRORM signal true.	Any ERRORB<n> signal true.	Any ERRORA<n> signal true.
SR192 Master/slave, TSA/TSB linked	Any ERRORA<n> or ERRORB<n> or ERRORM signal true.		Any ERRORA<n> or ERRORB<n> signal true.

Table 5-2 Error Signal Generation

5.9.2 Compare Signal Generation

The compare signals from both digital resources as well as the front panel master/slave connector (J7) can be programmed to generate a single compare flag that can be tested. Table 5-3 illustrates how the error flags are generated.

SR192 Setting	COMPAREA TRUE if	COMPAREB TRUE if	COMPAREM TRUE if
SR192 Independent, TSA/TSB not linked	All COMPAREA<n> signals true.	All COMPAREB<n> signals true.	N/A
SR192 Independent, TSA/TSB linked	All COMPAREA<n> and COMPAREB<n> signals true.		N/A
SR192 Master/slave, TSA/TSB not linked	All COMPAREA<n> and COMPAREM signals true.	All COMPAREB<n> signals true.	All COMPAREA<n> signals true.
SR192 Master/slave, TSA/TSB linked	All COMPAREA<n> and COMPAREB<n> and COMPAREM signals true.		All COMPAREA<n> and COMPAREB<n> signals true.

Table 5-3 Compare Signal Generation

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Appendix A Glossary of Terms

A16/A24/A32	VXI Register Based Programming Mode.
ADEL_CLK	Timing module signal used to delay the memory address to the record memory.
ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
COMPARE	Unregistered signal from the response comparator which indicates that the current response data matches the expect and mask data.
CSTROBE-	Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data.
DAC/MFC	SR192 motherboard accessory module slot mnemonic.
DRA1-DRA6	SR192 motherboard digital resource A I/O module slot mnemonic.
DRB1-DRB6	SR192 motherboard digital resource B I/O module slot mnemonic.
ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
EXTCLK	Selected external clock from the front panel J8 connector (EXCLK1 or EXCLK2)
FCNTL1-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FCNTL2-	Front panel input signal (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
FUNCTION CODE(FC)	Each module in a SR192 is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
GROUP ENABLE	Group enable signal. This signal can be used to enable a group of I/O channels.
INPUT STROBE	This signal records data into the compare register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
INTCLK	Selected internal timing module clock from the motherboard (10MHz, 20MHz or 50MHz).
I/O CHANNELS	Sixteen bi-directional TTL data channels.

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I/O MODULE	Any of Talons Stimulus/Response modules for the SR192.
OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
RESPONSE	The response data of the SR192 is comprised of EXPECT, MASK and RECORD memory in five memory I/O modules and just RECORD memory in three memory I/O modules.
SCPI	(Standard Commands for Programmable Instruments) Remote command language format standard the SR192 utilizes.
SEQUENCE	A sequence is the link between the timing sets and the tables.
SHIFT STROBE	This signal is used to record intermediate data from the UUT for the shift function modes.
STIM_LOAD	Timing module control signal that routes the data from the stimulus memory to the output registers. The rising edge of this control signal also registers the stimulus address (FMA) when the output register delay is enabled.
STIMULUS	The stimulus data of the SR192 is comprised of OUTPUT and TRISTATE memory located on the I/O modules.
SR_CLK	Stimulus/Response Clock. This signal, generated by the timing generator, clocks the Digital Resource.
SUBSEQUENCE	A subsequence is a single element of a sequence. A subsequence selects a timing set, table, loop count, jump condition and control flags.
TABLE	A table is the structure that defines a FMA range for the subsequence. The FMA range is broadcast to all the I/O modules connected to the timing module.
TIMING MODULE	Any of Talons Timing Modules for the SR192.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Four pages of sixteen timing sets can be defined.
TRANSFER	See WORD.
TRISTATE Dn	Tristate driver data from the stimulus memory.
TS_CLK	Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK.
TSA	SR192 motherboard digital resource A timing module mnemonic.
TSB	SR192 motherboard digital resource B timing module mnemonic.
TSENABLE1	Timing Set Enable One. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight.
TSENABLE2	Timing Set Enable Two. This signal, generated by the timing generator, can be selected to enable the stimulus drivers in groups of eight.
TSINPUT1	Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT1A is routed to TSA INPUT1, TSINPUT1B is routed to TSB INPUT1.

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TSINPUT2	Front panel test input signal. Each timing module has two test input signals available, INPUT1 and INPUT2. TSINPUT2A is routed to TSA INPUT2, TSINPUT2B is routed to TSB INPUT2.
TSIO	(Timing Set Input Output) used as the name for the SR192 timing signal translator module.
TSOUT1	Timing Set Output One. General purpose output signal generated by the timing module.
TSOUT2	Timing Set Output Two. General purpose output signal generated by the timing module.
TSOUT3	Timing Set Output Three. General purpose output signal generated by the timing module.
TSOUT4	Timing Set Output Four. General purpose output signal generated by the timing module. Also used to enable the selected channel mode function.
TSOUT5	Timing Set Output Five. General purpose output signal generated by the timing module. Also used as a strobe for the SR121/SR210 probe.
TSSTROBE1	Timing Set Strobe One. This signal, generated by the timing generator, can be selected as the input strobe or shift strobe.
TSSTROBE2	Timing Set Strobe Two. This signal, generated by the timing generator, can be selected as the input strobe.
VADDR	The address bus from the VXI Backplane.
VDATA	The data bus from the VXI Backplane.
VECTOR	See WORD.
VXI	(VME Extensions for Instrumentation), also used as the name for the SR192 backplane interface board.
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192.

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Appendix B Address Map

SR192 addressing is split into two sections, A16 and A24/A32. The two sections are selected by six signals on the VXI backplane called the address modifiers.

The SR192 will respond to the following A16 address modifier settings: hex 29 and 2D.

If the SR192 is set to A24 addressing (section 3.2.3.2) then it will respond to the following address modifier settings: hex 39, 3A, 3B, 3D, 3E and 3F.

If the SR192 is set to A32 addressing (section 3.2.3.2) then it will respond to the following address modifier settings: hex 39, 3A, 3B, 3D, 3E and 3F.

1 A16 Map

The A16 registers and their function are defined by the VXI standard.

Register	Offset	R/W	Description
ID	0x0	read	Instrument ID Register
LA	0x0	write	Logical Address Register
DEVICE	0x2	read	Device Register
STATUS	0x4	read	Status Register
CONTROL	0x4	write	Control Register
OFFSET	0x6	read/write	A32/A24 Offset Register
PROTOCOL	0x8	read	Protocol Register
RESPONSE	0xA	read	Response Register
DATA LOW	0xE	read/write	Data Low

Table B-1 A16 Address Map

The following sections describes the registers listed above.

1.1 ID Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Class		Address Space		Manufacturer ID											

Field/Bit Description:

Device Class	Specifies the VXI device classification: SR192 = hex 2 (message based).
Address Space	Device address mode; SR192 = hex 1 (A16/A32) or hex 0 (A16/A24) based on the CPU switch setting, see section .3.2.3.2
Manufacturer ID	Unique ID; Talon Instruments = hex 909.

1.2 LA Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Address															

Field/Bit Description:

Logical Address	Specifies the logical address if dynamic configuration is enabled, see section 3.2.3.1.

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1.3 Device Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Required Memory				Device Type											

Field/Bit Description:

Required Memory — Specifies the amount of A24/A32 memory addressing required; SR192 = 8388K
Device Type — Unique device identifier; SR192 = hex 101.

1.4 Status Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/A32 Active	MODID	NU										Ready	Passed	NU	

Field/Bit Description:

A24/A32 Active — Indicates whether the A24/A32 memory space is enabled (1) or disabled (0).
MODID — A zero in this field indicates that the SR192 is selected by a high state on the P2 MODID line.
Ready — A zero in this field indicates that the SR192 is still in the self test/initialize state during power up. A one in this field with a zero in the “passed” field indicates the SR192 failed register initialization. A one in this field along with a one in the “passed“ field indicates the SR192 is operational.
Passed — A zero in this field indicates the SR192 is either executing or has failed self test. A one indicates the SR192 has passed self test and is ready for operation.

1.5 Control Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/A32 Enable	NU													Sysfail Inhibit	Reset

Field/Bit Description:

A24/A32 Enable — A one (1) enables access to the A24/A32 registers of the SR192. A zero (0) disables access.
Sysfail Inhibit — A one (1) in this field disables the SR192 from driving the SYSFAIL line.
Reset — A one (1) in this field forces the SR192 into the reset state.

1.6 Offset Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24 MSA	NU														
A32 MSA									NU						

Field/Bit Description:

A24 MSA — This bit is mapped to the most significant bit of the A24 address decoder.
A32 MSA — These 9 bits are mapped to the upper 9 bits of the A32 address decoder.

1.7 Protocol Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMDR	Signal Register	Master	Interrupter	FHS	Shared Memory	Reserved						NU			

Field/Bit Description:

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CMDR	Always 1, this field indicates that the SR192 is a servant only.
Signal Register	Always 1, this field indicates that the SR192 does not have a signal register.
Master	Always 1, this field indicates that the SR192 does not have VMEbus Master capability.
Interrupter	Always 1, this field indicates that the SR192 has interrupter capability.
FHS	Always 1, this field indicates that the SR192 supports the normal transfer mode.
Shared Memory	Always 1, this field indicates that the SR192 does not support the shared memory protocol.
Reserved	All ones (hex 3F) will be returned.

1.8 Response Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved	DOR	DIR	Err	Read Ready	Write Ready	NU								

Field/Bit Description:

Bit 15	Always zero (0)
Reserved	Always one (1)
DOR	Data Output Ready; A one (1) in this field indicates that the SR192 is ready to output data to the commander using the byte transfer protocol.
DIR	Data Input Ready; A one indicates that the SR192 is ready to accept data from the commander using the byte transfer protocol.
Err	A zero (0) indicates that a word serial error has occurred.
Read Ready	A one (1) indicates that the SR192's DATA LOW register contains data to be read.
Write Ready	A one (1) indicates that the SR192 is ready for data to be written to the DATA LOW register.

1.9 DATA LOW Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command/Data															

Field/Bit Description:

Command/Data	Commands and data are passed between the SR192 and the commander by reads and writes to this register.

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2 A32 Map

The SR192 requests approximately 8M of address memory from the resource manager on power up. This address memory allows the SR192 user to directly access the stimulus/response memory as well as control/status registers.

The 8M of address memory is segmented into sections listed below.. Along with the module decodes

Section	Base Address	Function Code	Description	Section
SYSTEM	0	0-4	System Memory	2.1
STATUS/CONTROL	40000	NU	VXI A32 Decodes,	2.2
DAC/MFC	70000	0-F	DAC/MFC Module	2.3
ERAMA	80000	0,1,2	Error Address Ram, TSA	2.4
PROBE	C0000	NU	Probe GOOD0/GOOD1	2.5
TSA	100000	0-F	Timing Set A Module	2.6
TSB	180000	0-F	Timing Set B Module	2.6
DRA1	200000	0-F	Driver/Receiver Module	2.7
DRA2	280000	0-F	Driver/Receiver Module	2.7
DRA3	300000	0-F	Driver/Receiver Module	2.7
DRA4	380000	0-F	Driver/Receiver Module	2.7
DRA5	400000	0-F	Driver/Receiver Module	2.7
DRA6	480000	0-F	Driver/Receiver Module	2.7
DRB1	500000	0-F	Driver/Receiver Module	2.7
DRB2	580000	0-F	Driver/Receiver Module	2.7
DRB3	600000	0-F	Driver/Receiver Module	2.7
DRB4	680000	0-F	Driver/Receiver Module	2.7
DRB5	700000	0-F	Driver/Receiver Module	2.7
DRB6	780000	0-F	Driver/Receiver Module	2.7

Table B-2 SR192 A24/A32 Section Map

Each section can be further divided into sixteen pages using four function code signals (F0 through F3) to generate a function code.

Function code 15 (FC15) for each of the module sections is used to identify the module type. ID's 0 - 7 are reserved for DAC/MFC modules, 8 - 15 are reserved for timing modules and 16 - 128 are reserved for I/O modules.

The following sections describe each A24/A32 section listed above.

2.1 SYSTEM MEMORY

The SR192 System Memory is comprised of up to 5 banks of memory located at address 0-0x3FFFF. Each bank is addressed using the function code bits.

Commands are available to do the following functions:

1. Restart using upper RAM1 as new system.
2. Reprogram flash RAMs using the data in upper RAM1.

Function Code Assignments:

FC0 Read Flash RAM (contains the system firmware).

FC1 Read/write bank one RAM. This bank can be swapped with flash for firmware updates.

FC2 Read/write bank 2 RAM.

FC3 Read/write bank 3 RAM.

FC4 Read/write bank 4 RAM.

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2.2 Status/Control

The SR192 A24/A32 status/control registers are listed below.

Register	Offset	R/W	Register Description
WSEXCLK	0x40000	write	Programs external clock source, master mode and error memory address mode.
WRTMRST	0x40002	write	Clear error counter, reset timing module error and time-out
RDTMSTA	0x40002	read	Timing module status register
RD1617A	0x40004	read	Upper Error Memory Address Bit Register
ERREG	0x40006	write	Error Control Register
DRVRRD	0x40008	read	Variable Voltage Driver Status Register
VXIFC	0x40010	write	VXI Function Code Register
TTLTRG-	0x40012	write	TTLTRG Control Register

Table B-3 A24/A32 Status/Control Registers

2.2.1 WSEXCLK (0x40000)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Factory Reserved (must program high)							Master Enable	Error memory address mode		EXCLKM source		EXCLK-TSB source		EXCLK-TSA, ICLKM source	

Bit Description:

Bit 0 and 1 selects the EXCLK-TSA source when the SR192 is not in the master mode. If the SR192 is in the master mode then bit 0 and 1 selects the internal clock source of EXCLKM. ICLKM = master bus clock source.

Bit 1	Bit 0	Master Mode	EXCLK-TSA
X	X	ON	EXCLKM
0	0	OFF	EXCLK1
0	1	OFF	EXCLK2
1	0	OFF	EXCLKM
1	1	OFF	PGMCLK

Bit 1	Bit 0	Master Mode	ICLKM
X	X	OFF	N/A
0	0	ON	10MHz
0	1	ON	20MHz
1	0	ON	50MHz
1	1	ON	PGMCLK

Bit 2 and 3 selects the EXCLK-TSB source.

Bit 3	Bit 2	EXCLK-TSB
0	0	EXCLK1
0	1	EXCLK2
1	0	EXCLKM
1	1	PGMCLK

Bit 4 and 5 selects the EXCLKM source.

Bit 5	Bit 4	EXCLKM
0	0	EXCLK1
0	1	EXCLK2
1	X	ICLKM

Bit 6 and 7 selects the error memory address register mode.

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Bit 7	Bit 6	EMA register mode
0	0	OUTREG and ADDRESS DELAY enable.
0	1	OUTREG disabled and ADDRESS DELAY enabled.
1	0	OUTREG enabled and ADDRESS DELAY disabled.
1	1	OUTREG and ADDRESS DELAY disabled.

Bit 8 enables the master mode.

Bit 8	Master Mode
0	ON
1	OFF

Bits 9 through 15 are factory reserved and must be programmed high.

2.2.2 WRTMRST (0x40002)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used											Clear error counter	Reset TSB timeout	Reset TSA timeout	Reset TSB halt	Reset TSA halt

Bit 0 clears the TSA halt LED.

Bit 0	TSA halt LED
0	OFF
1	No change

Bit 1 clears the TSB halt LED.

Bit 1	TSB halt LED
0	OFF
1	No change

Bit 2 clears the TSA timeout LED.

Bit 2	TSA timeout LED
0	OFF
1	No change

Bit 3 clears the TSB timeout LED.

Bit 3	TSB timeout LED
0	OFF
1	No change

Bit 4 clears the error counter.

Bit 4	Error counter
0	0
1	No change

2.2.3 RDTMSTA (0x40002)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		TSB timing module status						NU		TSA timing module status					

Bit definitions:

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Bit #	Level	TSA Status
0 IDLE-	High (1)	TSA in reset state
	Low (0)	TSA in idle or run state, see bit 1.
1 RUN-	High (1)	TSA not running, idle or reset.
	Low (0)	TSA running.
2 WAIT-	High (1)	TSA not waiting for input trigger/handshake.
	Low (0)	TSA waiting for input trigger/handshake.
3 TIMEOUT	High (1)	TSA input trigger/handshake timed out.
	Low (0)	No TSA timeout.
4 HALT	High (1)	TSA halt on error occurred.
	Low (0)	No TSA halt.
5 COMPARE	High (1)	TSA waiting for compare.
	Low (0)	TSA not waiting for compare.

Bit #	Level	TSB Status
0 IDLE-	High (1)	TSB in reset state
	Low (0)	TSB in idle or run state, see bit 1.
1 RUN-	High (1)	TSB not running, idle or reset.
	Low (0)	TSB running.
2 WAIT-	High (1)	TSB not waiting for input trigger/handshake.
	Low (0)	TSB waiting for input trigger/handshake.
3 TIMEOUT	High (1)	TSB input trigger/handshake timed out.
	Low (0)	No TSB timeout.
4 HALT	High (1)	TSB halt on error occurred.
	Low (0)	No TSB halt.
5 COMPARE	High (1)	TSB waiting for compare.
	Low (0)	TSB not waiting for compare.

2.2.4 RD1617a (0x40004)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														ERRAMA Bit 16 and Bit 17	

When any word of the error memory address is read the upper two bits are automatically registered. The data can then be read back and the complete address can be determined. This data is only valid for the previous read of the current address, error address memory, or error count which is determined by function code, see section A.2.4.

Bit definitions:

Bit #	TSA Status
0	Value of bit 16 for the previous read/write of ERRAMA register.
1	Value of bit 17 for the previous read of ERRAMA register.

2.2.5 ERREG (0x40006)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU			EMA strobe delay			EMA strobe source		NU	TSIO DRVFLT irq mask	Timing channel enable	TSIO DRVFLT reset	COMPARE source		ERROR source	

Bit definitions:

Bit 0 and 1 selects the error flag source.

Bit 1	Bit 0	ERRORA Source	ERRORB Source	ERRORM Source
0	0	DRA1-DRA6	DRB1-DRB6	NONE

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0	1	DRA1-DRB6	DRA1-DRB6	NONE
1	0	DRA1-DRB6,ERRORM	DRA1-DRB6,ERRORM	DRA1-DRB6
1	1	DRA1-DRA6,ERRORM	DRB1-DRB6	DRA1-DRA6

Bit 2 and 3 selects the error flag source.

Bit 3	Bit 2	COMPAREA Source	COMPAREB Source	COMPAREM Source
0	0	DRA1-DRA6	DRB1-DRB6	NONE
0	1	DRA1-DRB6	DRA1-DRB6	NONE
1	0	DRA1-DRB6,COMPAREM	DRA1-DRB6,COMPAREM	DRA1-DRB6
1	1	DRA1-DRA6,COMPAREM	DRB1-DRB6	DRA1-DRA6

Bit 4 clears the TSIO drive fault flag.

Bit 4	TSIO DRVFLT
0	Set TSIO drive fault flag.
1	Reset TSIO drive fault flag.

Bit 5 enables/disables the drivers for TSOUTA1-TSOUTA5, TSOUTB1-TSOUTB5, and CLOCKA.

Bit 5	Output Drivers
0	Enabled.
1	Disabled.

Bit 6 masks the motherboard drive fault flag (MB DRVFLT).

Bit 6	TSIO DRVFLT Irq Mask
0	Enable TSIO drive fault irq.
1	Disable TSIO drive fault irq.

Bit 8 and 9 selects the error memory address strobe.

Bit 9	Bit 8	EMA Strobe
0	0	FCNTL1
0	1	FCNTL2
1	0	TSSTROBEA1
1	1	TSSTROBEA2

Bit 10, 11 and 12 selects the error memory strobe delay.

Bit 12	Bit 11	Bit 10	EMA Strobe Delay
0	0	0	0
0	0	1	5ns
0	1	0	10ns
0	1	1	15ns
1	0	0	20ns
1	0	1	25ns
1	1	0	30ns
1	1	1	35ns

2.2.6 DRVRRD (0x40008)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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NU	EMA strobe source	TSIO DRVFLT flag	TSIO DRVFLT irq mask	DRVFLT flag	OVERDRIVE LED	NU

Bit definitions:

Bits 4 through 7 return the Variable Voltage driver status.

Bit #	Level	Description
4	High (1)	OVERDRIVE LED off.
	Low (0)	OVERDRIVE LED on.
5	High (1)	I/O and TSIO driver fault flag false.
	Low (0)	I/O or TSIO driver fault flag true.
6	High (1)	TSIO driver fault irq mask enabled.
	Low (0)	TSIO driver fault irq mask disabled.
7	High (1)	TSIO driver fault false.
	Low (0)	TSIO driver fault true.

Bits 8 and 9 return the EMA strobe setting.

Bit 9	Bit 8	EMA Strobe Setting
0	0	FCNTL1 selected
0	1	FCNTL2 selected
1	0	TSSTROBEA1 selected
1	1	TSSTROBEA2 selected

2.2.7 VXIFC (0x40010)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU												Function Code			

Bit definitions:

Bit 0 through 3 sets the function code value.

Bit 3	Bit 2	Bit 1	Bit 0	Function Code
0	0	0	0	FC0
0	0	0	1	FC1
0	0	1	0	FC2
0	0	1	1	FC3
0	1	0	0	FC4
0	1	0	1	FC5
0	1	1	0	FC6
0	1	1	1	FC7
1	0	0	0	FC8
1	0	0	1	FC9
1	0	1	0	FC10
1	0	1	1	FC11
1	1	0	0	FC12
1	1	0	1	FC13
1	1	1	0	FC14
1	1	1	1	FC15

2.2.8 TTLTRG (0x40012)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								TTLTRG input enable	TTLTRG input select			TTLTRG output enable	TTLTRG output select		

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Bit definitions:

Bit 0, 1 and 2 selects the TTLTRG output selection.

Bit 2	Bit 1	Bit 0	TTLTGR Selection
0	0	0	TTLTRG0
0	0	1	TTLTRG1
0	1	0	TTLTRG2
0	1	1	TTLTRG3
1	0	0	TTLTRG4
1	0	1	TTLTRG5
1	1	0	TTLTRG6
1	1	1	TTLTRG7

Bit 3 enables/disables the output TTLTRG driver.

Bit 3	TTLTRG Output Driver
0	OFF
1	ON

Bit 4, 5 and 6 selects the TTLTRG input selection.

Bit 6	Bit 5	Bit 4	TTLTGR Selection
0	0	0	TTLTRG0
0	0	1	TTLTRG1
0	1	0	TTLTRG2
0	1	1	TTLTRG3
1	0	0	TTLTRG4
1	0	1	TTLTRG5
1	1	0	TTLTRG6
1	1	1	TTLTRG7

Bit 7 enables/disables the input TTLTRG receiver.

Bit 7	TTLTRG Input Receiver
0	OFF
1	ON

2.3 DAC/MFC

Refer to the specific reference manual of the module installed in the DAC/MFC slot.

2.4 ERAMA MEMORY

The SR192 Error Ram Memory is comprised of 1 bank of memory located at address hex 80000 to BFFFF and two registers located at address hex 80000. Both registers and the memory are selected using the function code bits.

Function Code Assignments:

FC0 — Read/Write lower 16 bits of error address memory, see section B.2.2.4 to read the upper two bits.

FC1 — Read lower 16 bits of the error counter, see section B.2.2.4 to read the upper two bits.

FC2 — Read lower 16 bits of the timing generator memory address, see section 2.2.4 of this appendix to read the upper two bits.

2.5 PROBE

See the SR210 reference manual.

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2.6 TSA/TSB

Refer to the specific timing module reference manual.

2.7 DRAn/DRBn

Refer to the specific I/O module reference manual.

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Appendix C Power & Cooling

Appendix C will guide the user through the necessary steps for calculating the total cooling requirements for any SR192 unit configuration. Part 1 of Appendix C will provide the user with the appropriate formulas and typical module power dissipation values to determine the total power dissipation of the SR192. Part 2 will use the total SR192 power dissipation value to calculate the VXI chassis cooling requirements (i.e., required airflow). Finally, Part 3 uses a graph to determine the optimal Back pressure for the required airflow.

1 Calculating the Total Power Dissipation

The total power dissipated by the SR192 is equal to the sum of the individual power dissipations of its modular components. Each of these components will be addressed separately and they consist of the Motherboard Assembly, the I/O Module(s), the Timing Module(s) and the Accessory Module.

The first step before attempting to calculate the total power dissipation is to document the configuration of the SR192. In table C-1 below, list the installed modules under the “Module Type” column and in their respective “Slot” positions:

Slot	Module Type	Typical Power (W)
n/a	Motherboard	
DRA1		
DRA2		
DRA3		
DRA4		
DRA5		
DRA6		
TSA		
DRB1		
DRB2		
DRB3		
DRB4		
DRB5		
DRB6		
TSB		
DAC		
Total Power (W)		

Table C-1 SR192 Power Table

The “Typical Power (W)” and “Total Power (W)” values will be filled-in later.

Now that the SR192 unit configuration has been defined, proceed through the appropriate sections that follow and enter the resultant power dissipation values into the “Typical Power (W)” column of table C-1. After entering-in all the pertinent power dissipation values, calculate the “TOTAL SR192 POWER (W)” by simply adding all of these separate values together. Once this is done, proceed to section 2 to calculate the VXI chassis airflow requirements.

Notes for the following formulas:

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1. For calculations involving programmable-voltage I/O, variables “V+” and “V-” must be substituted with the appropriate V+/V- rail voltage values (supplied externally via connector J10).
2. “| |“ = the absolute value of.
3. All “No-Load Current” values are listed in table C-2 below.
4. The Load Factor = average “enable” time of 50% X average ratio of driving channels/non-driving channels.
   Example: for an average of 8 SR105 channels driving, Load Factor = .5 X 8/16 = .25.

	VXI BACKPLANE (Amps)							EXTERNAL INPUT J10 (Amps)	
	+5	-5.2	-2	+12	-12	+24	-24	+V	-V
MB,CPU,VXI,TSIO	2.2	0	0	0.002	0	0.04	0.04	0.2	0.2
SR100/SR101	2.3	0	0	0	0	0	0	0	0
SR103/SR103C	1.1	0	0	0	0	0	0	0	0
SR105,SR105C	1.4	0	0	0	0	0	0	0	0
SR107	0.5	0	0	0	0	0	0	0	0
SR115,SR115C	2	0	0	0	0	0	0	0	0
SR112	1	0	0	0	0	0	0	0	0
SR122	1.35	0	0	0	0	0	0	0	0
SR123	1	1	0	0	0	0	0	0	0
SR210	0.475	0	0	0.1	0.09	0.21	0.12	0	0
SR211	0.7	0	0	0	0	0.16	0.12	0	0
SR102	0.52	0	0	0	0	0	0	0.64	0.64
SR104	0.86	0	0	0	0	0	0	0.64	0.64
SR106	0.4	0	0	0	0	0	0	0.64	0.64
SR114	0.95	0	0	0	0	0	0	0.64	0.64
SR214	2	0	0	0	0	0	0	0.8	0.8

Table C-2 SR192 No Load Current Chart

1.1 Motherboard Assembly Power Dissipation

The SR192 Motherboard Assembly consists of the SR192 Motherboard, the TSIO board and the CPU/VXI assembly. The power dissipation of the Motherboard Assembly is calculated by using the following formula:

(+5V X 2.2A) + (+12V X 2mA) + (+24V X 40mA) + (|-24V| X 40mA) + (V+ X 200mA) + (V- X 200mA)
= 12.94W + (V+ X 200mA) + (V- X 200mA)

NOTE: if V+/V- are not used, then 12.94W is the total Motherboard Assembly power dissipation **

Enter the calculated power dissipation in the “Motherboard Assembly” row of table C-1 under the “Typical Power (W)” column.

1.2 I/O Module Power Dissipation

Depending upon the types of I/O modules installed (i.e., TTL, CMOS, Programmable, etc…), use the appropriate “Typical Total Power Dissipation Values” from the following section and enter them in the appropriate “DRAn”/”DRBn” row(s) of table C-1 under the “Typical Power (W)” column. For reference, the basic formula for calculating I/O module power dissipation is:

Total Power Dissipation per I/O Module (W) = No-Load Power + Average Load Power

1.2.1 TTL I/O Modules (SR103, SR105, SR107, SR115)

Formulas Used:

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No-Load Power (W):

+5V X No-Load Current (value is from the “+5” column of table C-2)

Average Load Power (W):

{(+5V - +3.5V) + 0.3V}/2 X Load Current X # of channels per module X Load Factor

Typical Current/Load Factor Parameters:

Load Current	10mA
Load Factor	0.25

Calculated Typical Power:

SR103: 5.54W

SR105: 7.04W

SR107: 2.54W

SR115: 10.04W

1.2.2 CMOS I/O Modules (SR103/C, SR105/C, SR115/C)

Formulas Used:

No-Load Power (W):

+5V X No-Load Current value is from the “+5” column of table C-2)

Average Load Power (W):

{(+5V - +3.5V) + 0.3V}/2 X Load Current X # of channels per module X Load Factor

Typical Current/Load Factor Parameters:

Load Current	10mA
Load Factor	0.25

Calculated Typical Power:

SR103/C: 5.54W

SR105/C: 7.04W

SR115/C: 10.04W

1.2.3 TTL Differential I/O Modules (SR112, SR122)

Formulas Used:

No-Load Power (W):

+5V X No-Load Current (value is from the “+5” column of table C-2)

Average Load Power (W):

{(+5V - +3.5V) + 0.3V} X Load Current X # of channels per module X Load Factor

Typical Current/Load Factor Parameters:

Load Current	10mA
Load Factor	0.25

Calculated Typical Power:

SR103/C: 5.54W

SR112: 5.04W

SR122: 6.79W

1.2.4 ECL Differential I/O Modules (SR123)

Formulas Used:

No-Load Power (W):

(+5V X No-Load Current) + (|-5.2V| X No-Load Current) (values are from table C-1)

Average Load Power (W):

{(0.9V X Load Current) + (3.1V X Load Current)} X # of channels per module X Load Factor

Typical Current/Load Factor Parameters:

Load Current	10mA
Load Factor	0.25

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Calculated Typical Power

SR123: 10.28W

1.2.5 Programmable-Voltage I/O Modules (SR102, SR104, SR106, SR114, SR214)

Formulas Used:

No-Load Power (W):

(+5V X No-Load Current) + (V+ X No-Load Current) + (|V-| X No-Load Current) (values are from table C-2)

Average Load Power (W):

{(V+ – VOH) + (|V-| - VOL)}/2 X Load Current X # of channels per module X Load Factor

Typical Voltage/Current/Load Factor Parameters:

V+	10V
V-	-10V
VOH	+5V
VOL	0V
Load Current	10mA
Load Factor	0.25

Calculated Typical Power:

SR102: 15.55W

SR104: 17.25W

SR106: 14.95W

SR114: 17.7W

SR214: 26.3W

1.3 Timing Module Power Dissipation

The TSA and TSB slots of the SR192 can accommodate either of 2 types of Timing Modules – the SR100 and the SR101. The calculated power dissipation for each of these modules is:

SR100/SR101 Power Dissipation (W) = +5V X 2.3A = 11.5W

For each installed Timing Module, enter 11.5W in the “TSA”/“TSB” row(s) of table C-1 under the “Typical Power (W)” column.

1.4 Accessory Module Power Dissipation

The SR210 Accessory Module resides in the DAC slot of the SR192 and provides the voltage references for the programmable-voltage I/O modules (if any are installed). The SR210 also supplies a programmable-frequency clock source to the TSA/TSB Timing Modules and an interface to the SR211 Data Probe. The calculated power dissipation for the SR210 is:

(+5V X 47.5mA) + (+12V X 100mA) + (|-12V| X 90mA) + (+24V X 210mA) + (|-24V| X 120mA) = 10.44W

If an SR210 Accessory Module is installed, enter 10.44W in the “DAC” row of table C-1 under the “Typical Power (W)” column.

2 Calculating the VXI Chassis Airflow Requirements

Now that the total power dissipation for the SR192 has been determined, use one of the following formulas to calculate the Required Airflow to give a maximum 10C or 20C temperature rise:

Required Airflow for 10C rise (liters/sec) = (P/2) X 0.083

or

Required Airflow for 20C rise (liters/sec) = (P/2) X 0.0415

“P” is “TOTAL SR192 POWER (W)” from the SR192 POWER TABLE.

“0.083” and “0.0415” are airflow in liters/sec per Watt (W).

3 Determining the Optimal Back pressure

Use the following SR192 Back pressure Chart and the calculated Required Airflow value from Part 2 (above) to determine the optimal chassis Back pressure. The Back pressure is determined by drawing an upward vertical line from the horizontal x-axis at the calculated airflow value. At the point where this

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vertical line intersects the curve on the chart, draw a horizontal line left to the y-axis. The point where this horizontal line intersects the y-axis is the optimal Back pressure value, represented in mmH2O.

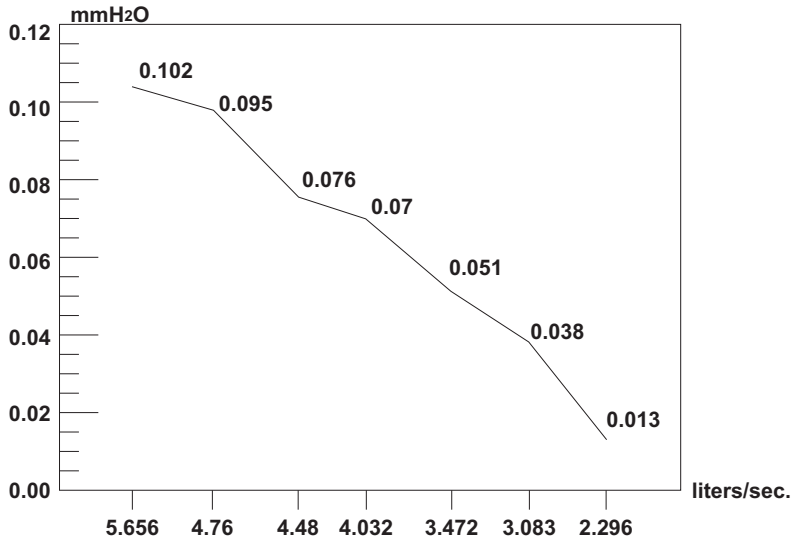


Figure C-1 SR192 Back pressure Chart

For example lets assume the calculated power (P) is 125W. Plugging this into our equation gives us:

A = (125W/2) x 0.083 ls/W

A = 62.5W x 0.083 ls/W

A = 5.1875 l/s

Pressure from the chart above is ~0.1mmH_2O

The cooling requirement is:

5.188 l/s @ 0.1mmH_2O

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Appendix D Signal Description

The following sections describe the SR192 front panel signals and terminations.

1 I/O Channels (J1 through J6)

Single ended I/O modules connect the I/O channel to the odd pin numbers and signal ground to all the even pin numbers.

Double ended (differential) I/O modules connect the I/O signal to the odd pin numbers and the compliment to the corresponding even pin numbers.

CH1-CH16	[J1-1A through J1-32A, I/O] Channel data from DRA1 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRA1	[J1-33A, Input] Card strobe signal routed to DRA1 module. See specific reference manual for driver/receiver and termination data.
CH17-CH32	[J1-1B through J1-32B, I/O] Channel data from DRA2 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRA2	[J1-33B, Input] Card strobe signal routed to DRA2 module. See specific reference manual for driver/receiver and termination data.
CH33-CH48	[J2-1A through J2-32A, I/O] Channel data from DRA3 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRA3	[J2-33A, Input] Card strobe signal routed to DRA3 module. See specific reference manual for driver/receiver and termination data.
CH49-CH64	[J2-1B through J2-32B, I/O] Channel data from DRA4 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRA4	[J2-33B, Input] Card strobe signal routed to DRA4 module. See specific reference manual for driver/receiver and termination data.
CH65-CH80	[J3-1A through J3-32A, I/O] Channel data from DRA5 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRA5	[J3-33A, Input] Card strobe signal routed to DRA5 module. See specific reference manual for driver/receiver and termination data.
CH81-CH96	[J3-1B through J3-32B, I/O] Channel data from DRA6 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRA6	[J3-33B, Input] Card strobe signal routed to DRA6 module. See specific reference manual for driver/receiver and termination data.
CH97-CH112	[J4-1A through J4-32A, I/O] Channel data from DRB1 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRB1	[J4-33A, Input] Card strobe signal routed to DRB1 module. See specific reference manual for driver/receiver and termination data.
CH113-CH128	[J4-1B through J4-32B, I/O] Channel data from DRB2 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRB2	[J4-33B, Input] Card strobe signal routed to DRB2 module. See specific reference manual for driver/receiver and termination data.
CH129-CH144	[J5-1A through J5-32A, I/O] Channel data from DRB3 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRB3	[J5-33A, Input] Card strobe signal routed to DRB3 module. See specific reference manual for driver/receiver and termination data.
CH145-CH160	[J5-1B through J5-32B, I/O] Channel data from DRB4 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRB4	[J5-33B, Input] Card strobe signal routed to DRB4 module. See specific reference manual for driver/receiver and termination data.
CH161-CH176	[J6-1A through J6-32A, I/O] Channel data from DRB5 module slot. See specific reference manual for driver/receiver and termination data.
CSTROBE-DRB5	[J6-33A, Input] Card strobe signal routed to DRB5 module. See specific reference manual for driver/receiver and termination data.
CH177-CH192	[J6-1B through J6-32B, I/O] Channel data from DRB6 module slot. See specific reference manual for driver/receiver and termination data.

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CSTROBE-DRB6 [J6-33B, Input] Card strobe signal routed to DRB6 module. See specific reference manual for driver/receiver and termination data.

2 Master/Slave Signals (J7)

All signals from the J7, master/slave connector have a selectable termination through SW1 on the SR192 motherboard. The following list shows the termination settings of the signals when enabled.

EXCLKM [J7-1A, I/O] TTL clock used by all the timing modules linked to the master/slave bus. 82Ω to GND, 74AS244 driver, GAL22V10 receiver.

SYNCTSM [J7-3A, I/O] TTL sync signal used to synchronize all the timing modules linked to the master/slave bus. 82Ω to GND, 74AS244 driver, 74HC244 receiver.

STARTM [J7-5A, I/O] TTL start signal used to begin execution of all the timing modules linked to the master/slave bus. 82Ω to GND, 74AS244 driver, 74HC244 receiver.

STOPM [J7-7A, I/O] TTL stop signal used to stop all the timing modules linked to the master/slave bus. 82Ω to GND, 74AS244 driver, 74HC244 receiver.

TSINPUTM [J7-9A, I/O] TTL input trigger/handshake signal used by the timing modules linked to the master/slave bus instead of TSINPUT1A and TSINPUT1B. 82Ω to GND, 74AS244 driver, 74HC244 receiver.

ERRORM [J7-1B, I/O] Open collector real-time error flag used by all the timing modules linked to the master/slave bus. 100Ω to +5V, 74AS1035 driver, GAL22V10 receiver.

COMPAREM [J7-3B, I/O] Open collector real-time compare flag used by all the timing modules linked to the master/slave bus. 100Ω to +5V, 74AS1035 driver, GAL22V10 receiver.

3 Timing and Control Signals (J8)

Single ended signals are connected to the odd pin number and signal ground to the corresponding even pin number.

Double ended (differential) signals are connected to the odd pin number and the compliment to the corresponding even pin number.

3.1 Trigger/Handshake Outputs

TSOUTA1,2 (two signals)[J8-(1A,3A), Output] Driver selectable trigger/handshake signals from TSA module. TTL selection: 47Ω series, 74AS244. Variable voltage selection: 47Ω series, EL1056. Differential selection: None, DS3695.

TSOUTA3-5 (three signals)[J8-(5A,7A,9A), Output] TTL user trigger/handshake signals from TSA module. 47Ω series, 74AS244.

TSOUTB1-5 (five signals)[J8-(1B,3B,5B,7B,9B), Output] TTL user trigger/handshake signals from TSB module. 47Ω series, 74AS244.

SYNCA- [J8-19A] TTL word trigger from TSA module. None, 74FCT827

SYNCB - [J8-19B] TTL word trigger from TSB module. None, 74FCT827

3.2 Trigger/Handshake Test Inputs

TSINPUTA1,2 (two signals)[J8-(11A,13A), Input] Receiver selectable trigger/handshake signals to TSA module. TTL selection variable voltage TSIO: Parallel to GND not installed, 74AS244. TTL selection differential TSIO: 82Ω to GND, 74AS244. Variable voltage selection: Parallel to GND not installed, EL2252. Differential selection: 120Ω parallel, DS3695.

TSINPUTB1,2 (two signals)[J8-(11B,13B), Input] TTL trigger/handshake signals to TSB module. 82Ω to GND, 74HC244.

3.3 Clock Inputs

EXCLK1 [J8-15A and SMA, Input] Receiver selectable external clock to both timing modules. TTL selection variable voltage TSIO: Parallel to GND not installed, 74AS244. TTL selection differential TSIO: 82Ω to GND, 74AS244. Variable volt-

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age selection: Parallel to GND not installed, EL2252. Differential selection: 120Ω parallel, DS3695.

EXCLK2 [J8-15B and SMA, Input] TTL external clock to both timing modules. 82Ω to GND, 74AS1004.

CLKREF [SMA, Input] TTL external programmable clock reference to the DAC/MFC module. 82Ω to GND, isplsi2032.

3.4 Clock Outputs

CLOCKA [J8-27A, Output] Driver selectable TSA clock. TTL selection: 47Ω series, 74AS244. Variable voltage selection: 47Ω series, EL1056. Differential selection: None, DS3695.

CLOCKB [J8-27B, Output] TTL TSB clock. 47Ω series, 74AS1004.

CLKA [SMA, Output] TTL programmable clock output one, PGMCLK1. 47Ω series, 74FCT240.

CLKB [SMA, Output] TTL programmable clock output two, PGMCLK2. 47Ω series, 74FCT240.

CLKC [SMA, Output] Variable voltage programmable clock output two, PGMCLK2. 47Ω series, EL1056.

3.5 I/O Control Inputs

FCNTL1- [J8-21A, Input] Receiver selectable external output enable/input strobe to all I/O modules. TTL selection variable voltage TSIO: Parallel to GND not installed, 74AS244. TTL selection differential TSIO: 82Ω to GND, 74AS244. Variable voltage selection: Parallel to GND not installed, EL2252. Differential selection: 120Ω parallel, DS3695.

FCNTL2- [J8-21B, Input] TTL external output enable/input strobe to all I/O modules. 82Ω to GND, 74AS1004.

PROBDAT- [J8-23B, Input] TTL probe data input strobe to DAC/MFC module. None, PALCE26V12.

3.6 Miscellaneous I/O

CLKRSTE [J8-29B, Input] TTL programmable clock reset signal to DAC/MFC module. None, isplsi2032.

UUTRST [J8-25B, Output] TTL operator programmable output pulse signal. 47Ω series, 74HC244.

TSABUSY [J8-17A, Input] TTL signal that indicates that a TSA sequence is running when low. None, 74AS1034.

TSBBUSY [J8-17B, Input] TTL signal that indicates that a TSB sequence is running when low. None, 74AS1034.

4 Probe/DAC Reference (J9)

The factory default for the SR192 J9 connector is set to the probe signals. The following sections describe the reference signals option, see section 3.1.2.1.

4.1 Voltage Group One

VOL1 [J9-1A, Output] Variable voltage output low reference for group one.

VOH1 [J9-3A, Output] Variable voltage output high reference for group one.

VIL1 [J9-5A, Output] Variable voltage input low reference for group one.

VIH1 [J9-7A, Output] Variable voltage input low reference for group one.

VISR1 [J9-9A, Output] Variable voltage output low reference for group one.

4.2 Voltage Group Two

VOL2 [J9-1B, Output] Variable voltage output low reference for group two.

VOH2 [J9-3B, Output] Variable voltage output high reference for group two.

VIL2 [J9-5B, Output] Variable voltage input low reference for group two.

VIH2 [J9-7B, Output] Variable voltage input low reference for group two.

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VISR2 [J9-9B, Output] Variable voltage output low reference for group two.

4.3 Voltage Group One

VOL3 [J9-2B, Output] Variable voltage output low reference for group three.
VOH3 [J9-4B, Output] Variable voltage output high reference for group three.
VIL3 [J9-6B, Output] Variable voltage input low reference for group three.
VIH3 [J9-6B, Output] Variable voltage input low reference for group three.
VISR3 [J9-10B, Output] Variable voltage output low reference for group three.

5 Power Connector (J10)

The J10 connector supplies both positive and negative power to the variable voltage I/O modules. The external power supply requirements are I/O module dependent, refer to the reference manual for each I/O module installed in the SR192 for the external power requirements and specifications.

GND (eight signals)[J10-(3,4,7,8,10,12,14,16)] Ground return for all positive and negative supply voltages.

5.1 Voltage Group One

V1+ (two signals)[J10-(1,2), Input] Positive supply for the I/O modules installed in slots DRA1 through DRA6 as well as TSIO-PROG. Fuse: F1, 7 Amps.
V1- (two signals)[J10-(5,6), Input] Negative supply for the I/O modules installed in slots DRA1 through DRA6 as well as TSIO-PROG. Fuse: F6, 7 Amps.

5.2 Voltage Group Two

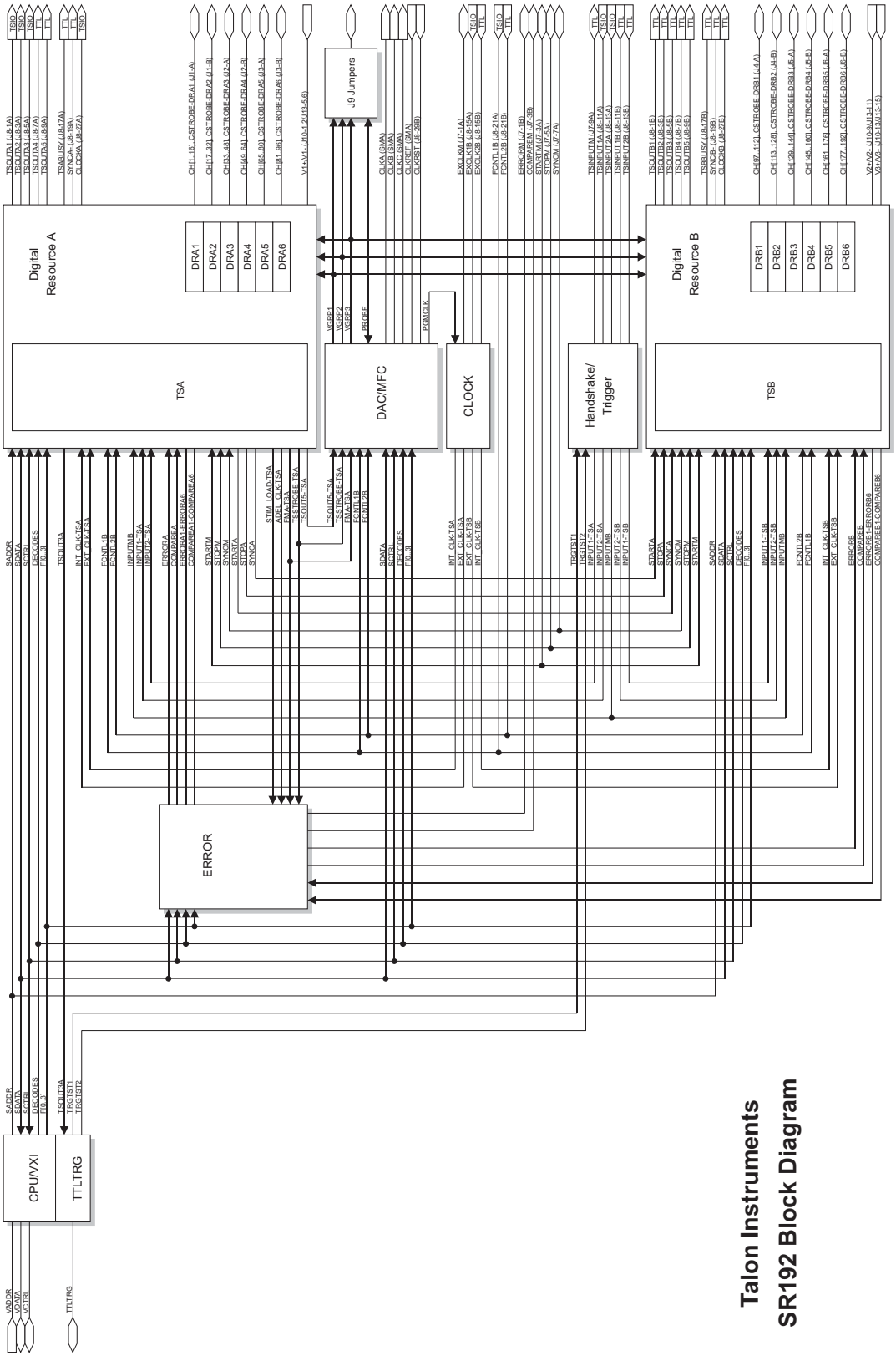
V2+ [J10-9, Input] Positive supply for the I/O modules installed in slots DRB1 through DRB3. Fuse: F4, 7 Amps.
V2- [J10-11, Input] Negative supply for the I/O modules installed in slots DRB1 through DRB3. Fuse: F2, 7 Amps.

5.3 Voltage Group Three

V3+ [J10-13, Input] Positive supply for the I/O modules installed in slots DRB4 through DRB6. Fuse: F7, 7 Amps.
V3- [J10-15, Input] Negative supply for the I/O modules installed in slots DRB4 through DRB6. Fuse: F3, 7 Amps.

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Appendix E Block Diagram



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