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TECHNICAL DESCRIPTION

Talon Instruments™

SR192

Bus Emulator/Word Generator

Publication Date: 06/1996
Publication Number: SRTD406 Rev. A
Instrument Part Number: SR192

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This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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DOCUMENT CHANGE HISTORY

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MODEL SR192 TECHNICAL DESCRIPTION

192 I/O CHANNELS

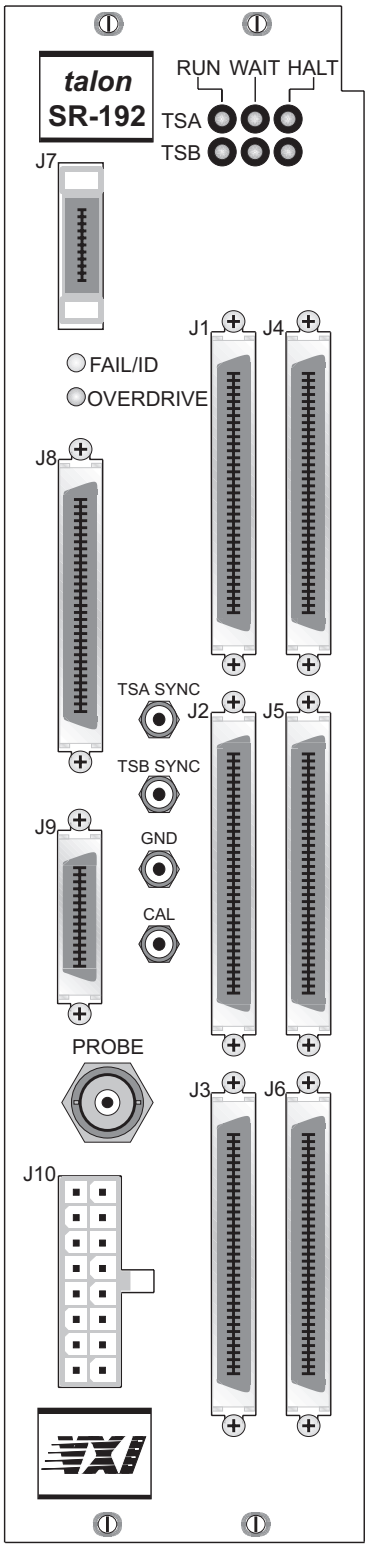
STIMULUS/RESPONSE

PER PIN ARCHITECTURE

PROGRAMMABLE I/O LEVELS

DUAL BUS EMULATOR

50 MHZ TIMING



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1 INTRODUCTION

For years the test engineer faced less than desirable alternatives when selecting a digital test resource. Digital products offered in the early eighties were basic stimulus response architectures. These products were expensive, consumed abundant real estate and were power hungry. They also required extensive programming to emulate a relatively simple digital interface.

In the mid eighties, Talon developed the first digital bus emulator product with the introduction of the Model 6000 Digital Test System. In the early nineties, Talon introduced bus emulation in a VXI format with Talon's BE-64. For many applications, these bus emulation products significantly reduced cost, real estate, power and programming requirements. However, the BE-64 posed another question for the test engineer: Does his test system require bus emulation or a traditional stimulus response digital resource?

Talon's SR192 solves this dilemma by integrating both a bus emulator architecture and a stimulus response architecture into a single VXI resource. The SR192 provides the following features:

ARCHITECTURE Figure 1 represents the Block Diagram of the SR192. As seen, the SR192 is actually two independent 96 channel digital resources which can operate independent and asynchronous from one another, or can be synchronized together to be one 192 channel device. Each 96 channels can operate in bus emulator mode or stimulus/response mode independently.

DENSITY VXI space is at a premium, thus the SR192 was designed to pack the most dynamic digital capability in the smallest possible space. 192 I/O channels plus 20 timing and control signals are housed in a dual slot VXI card. This is approximately three times denser than presently available VXI products.

MODULARITY To meet each customer's requirements, the SR192 offers a modular architecture. The user need only purchase the I/O modules which meet his testing requirements. Naturally, he may upgrade his SR192 as his test requirements mature. Additionally, several SR192's can be synchronized yielding test systems with up to 1152 I/O channels within a single 13 slot chassis.

MULTIPLE I/O LEVELS The SR192 offers the option of selecting TTL, RS485 differential or programmable driver/receivers, programmed from +/- 15 volts with 20 mV resolution. Optional built in DACS offer three voltage groups.

PROGRAMMING The SR192 is a message based SCPI format compatible VXI card. The SR192 uses the same SCPI commands as Talon's BE-64. The memories can be accessed via message based commands or directly via the A24 or A32 space. Also available are Timing Set and Data Table Editor window driven packages which output compatible SR192 SCPI commands.

COST Integrating 192 channels into a dual slot VXI card reduces much of the physical and electrical overhead costs associated with competitive units. This, in conjunction with extensive use of high density mechanical and electrical components, yields a digital resource which is typically 60% the cost of presently available VXI products.

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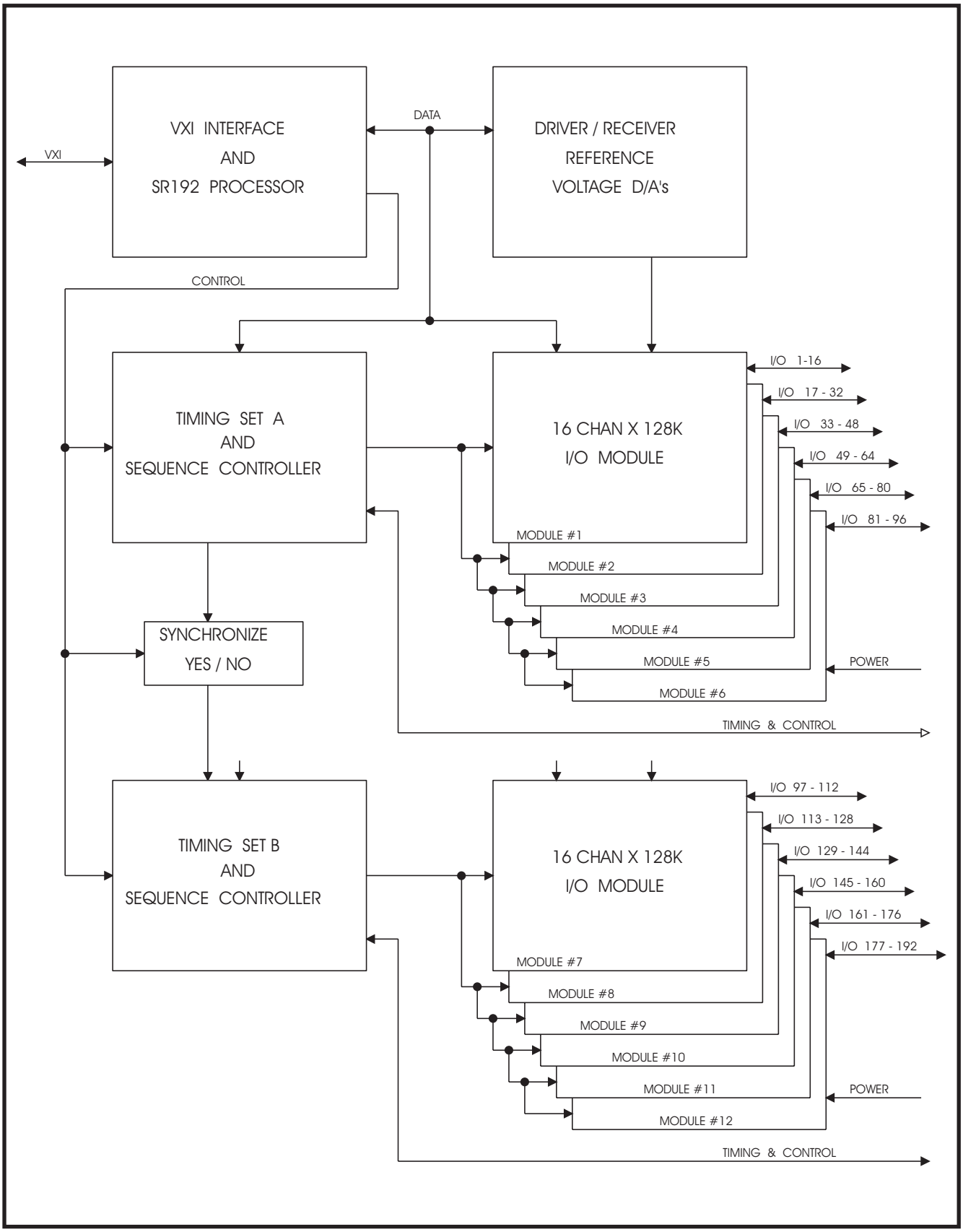


Figure 1 SR192 Block Diagram

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2 MODULAR CONSTRUCTION

Since each user's test requirements may vary significantly, the SR192 has been designed with modular I/O and timing cards. To match user's requirements, he may install up to twelve I/O modules, two timing set modules and one D/A module, figure 2.

Moreover, the user may choose from a variety of I/O modules, depicted in Figure 3. A wide variety of modules have been designed to offer significant cost savings for users who don't require programmable I/O levels or 128K memory depth. Additionally, the user may mix and match the I/O modules to generate the most cost effective and versatile system which matches his needs.

For systems with 6 I/O modules or less, a minimum of one timing set module is required. For systems with 7 I/O modules or more, two timing set modules are required. These timing set modules are nearly identical to Talon's BE-64 timing sets. They include handshake control signals, programmable cell delay, and a programmable time-out function. They may be clocked at frequencies to 50MHZ, yielding 20 nsec resolution for UUT control signals, bus enable signals, input sample signals, etc. The two timing set modules may operate completely independent and asynchronous from one another, yielding two independent interfaces, each having up to 96 I/O channels. Conversely, the timing sets can be synchronized, both within an SR192 card as well as among several SR192 cards, yielding systems from 192 to 1152 I/O channels

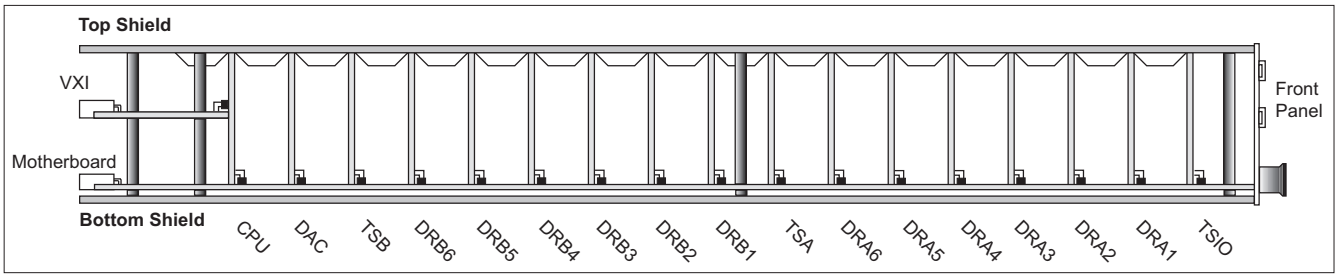
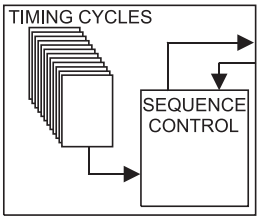


Figure 2 SR192 Modular Construction

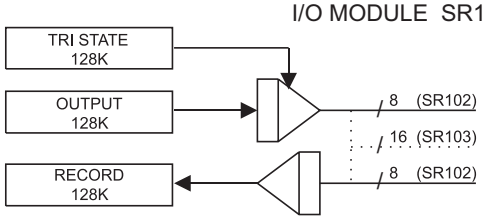
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TIMING MODULE SR100, SR101



FEATURES	MODULE	
	SR100	SR101
# OF SUBSEQUENCES	4	128K
SUBSEQUENCE BRANCHING	NO	YES
SUBSEQUENCE SUBROUTINE	NO	YES, 1 LEVEL
SEQUENCE LOOP	1-64K	1-32K
SUBSEQUENCE LOOP	NO	1-32K
# OF CELLS	128	256
# OF TIMING CYCLES	64	
SPEED	50 MHZ	
# OF TIMING OUTPUTS	5	
# OF TEST INPUTS	2	

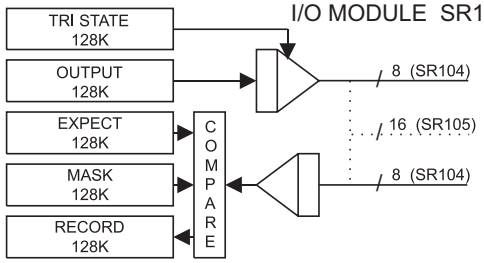
I/O MODULE SR102, SR103



FEATURES	MODULE	
	SR102	SR103
# OF CHANNELS	*16	16
OUTPUT LEVELS	PROG +/- 15V	TTL
INPUT THRESHOLD	DUAL +/- 15V	SINGLE, TTL
SPEED	25 MHZ	
MEMORY DEPTH	128K	
# MEMORIES / CHAN	3	
CHAN GROUPING	PER CHAN	
BUS EMULATION CONTROL	PER BYTE	

*SR102'S 16 CHANNELS ARE DEDICATED 8 OUTPUT AND 8 INPUT INTERNAL JUMPER FOR 8 BI-DIRECTIONAL

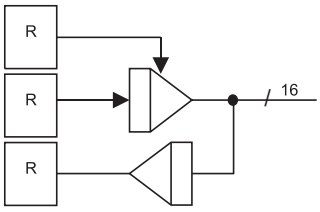
I/O MODULE SR104, SR105



FEATURES	MODULE	
	SR104	SR105
# OF CHANNELS	*16	16
OUTPUT LEVELS	PROG +/- 15V	TTL
INPUT THRESHOLD	DUAL +/- 15V	SINGLE, TTL
SPEED	25 MHZ	
MEMORY DEPTH	128K	
# MEMORIES / CHAN	5	
CHAN GROUPING	PER CHAN	
BUS EMULATION CONTROL	PER BYTE	
REAL TIME COMPARE	YES	

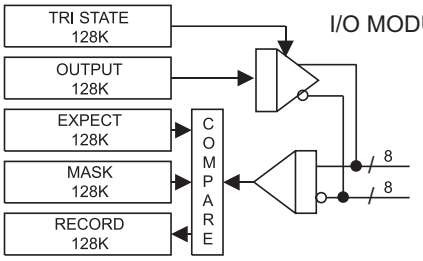
*SR104'S 16 CHANNELS ARE DEDICATED 8 OUTPUT AND 8 INPUT INTERNAL JUMPER FOR 8 BI-DIRECTIONAL

I/O MODULE SR106, SR107



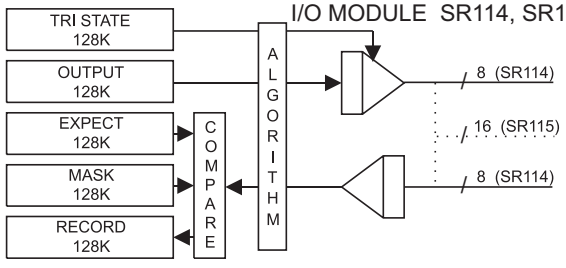
FEATURES	MODULE	
	SR106	SR107
# OF CHANNELS	16	16
OUTPUT LEVELS	8 PROG +/- 15V, 8 TTL	TTL
INPUT THRESHOLD	8 DUAL +/- 15V, 8 TTL	TTL
SPEED	STATIC	
MEMORY DEPTH	1	
# MEMORIES / CHAN	3	
CHAN GROUPING	PER CHANNEL	
BUS EMULATION CONTROL	PER CHANNEL	

I/O MODULE SR112



FEATURES	MODULE SR112
# OF CHANNELS	8
OUTPUT LEVELS	RS485 DIFFERENTIAL
INPUT THRESHOLD	RS485 DIFFERENTIAL
SPEED	25 MHZ
MEMORY DEPTH	128K
# MEMORIES / CHAN	5
CHAN GROUPING	PER CHAN
BUS EMULATION CONTROL	PER BYTE
REAL TIME COMPARE	YES

I/O MODULE SR114, SR115



FEATURES	MODULE	
	SR114	SR115
# OF CHANNELS	*16	16
OUTPUT LEVELS	PROG +/- 15V	TTL
INPUT THRESHOLD	DUAL +/- 15V	SINGLE, TTL
SPEED	50 MHZ	
MEMORY DEPTH	128K	
# MEMORIES / CHAN	5	
CHAN GROUPING	PER CHAN	
BUS EMULATION CONTROL	PER BYTE	
REAL TIME COMPARE	YES	

*SR114'S 16 CHANNELS ARE DEDICATED 8 OUTPUT AND 8 INPUT INTERNAL JUMPER FOR 8 BI-DIRECTIONAL

Figure 2 Module Features

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3 TECHNICAL DESCRIPTION

The SR192 system is comprised of five major logic sections:

1. The Motherboard.
2. The VXI/CPU Modules
3. DAC Reference Module
4. The I/O Module
5. The Timing Set Module

3.1 Motherboard

The motherboard PCB is a "C" size board which contains 4 motherboard front panel connectors and 17 headers for routing the SR192 IO signals to the front panel, 17 slots for the various plug-in modules, and 4 VXI system P1/P2 connectors.

The module connectors provide for 12 I/O modules, a DAC module, 2 timing set modules, a TSIO module and the CPU module. Figure 2 shows the motherboard from a side view.

The 12 I/O module slots DRA1-DRA6 and DRB1-DRB6 may be used to house any of the Talon I/O modules. Each slot is capable of routing up to 16 I/O signals to its associated connector on the front panel. Slot TSA and TSB house the two timing set modules. The signals from these modules are routed to the I/O modules and the front panel connector. The DAC slot is used to house the SR110 if it is required. The TSIO modules allow selection of various logic level conversion for some of the timing set A signals and one control signal. The CPU and VXI modules provide VXI backplane connections and SR192 system control.

The following list is the major functions of the SR192 motherboard:

- Route VXI backplane power/ground signals to the motherboard logic.
- Route signals to/from the front panel to the I/O and timing set modules.
- Provide level translation for selected timing I/O signals.
- Error counter and Error Address Memory RAM.

3.1.1 VXI Backplane Power/Ground

The SR192 connects with the VXI backplane through two sets of P1, P2 connectors. One set of connectors is located on the VXI module and provides all the VXI address/data and control signals to the CPU module. The other set of P1 and P2 connectors are located on the motherboard and are used to provide additional power and ground signals for the SR192 logic. All power pins from the VXI backplane are fused.

3.1.2 Front Panel Signal Routing

The motherboard is designed to route all the command and I/O signals to the front panel via PCB traces. This minimum use of cables helps to insure signal integrity. The headers for the front panel route the 192 IO signals and ground returns. In addition, a single header is used to route the other front panel signals such as SR111 probe, LED indicators, timing set signals, and various test points. The four motherboard front panel connectors route the timing signals as well as the driver/receiver power and reference signals. Figure 4 on the opposite page shows the signal routing from the front panel to the SR192 modules.

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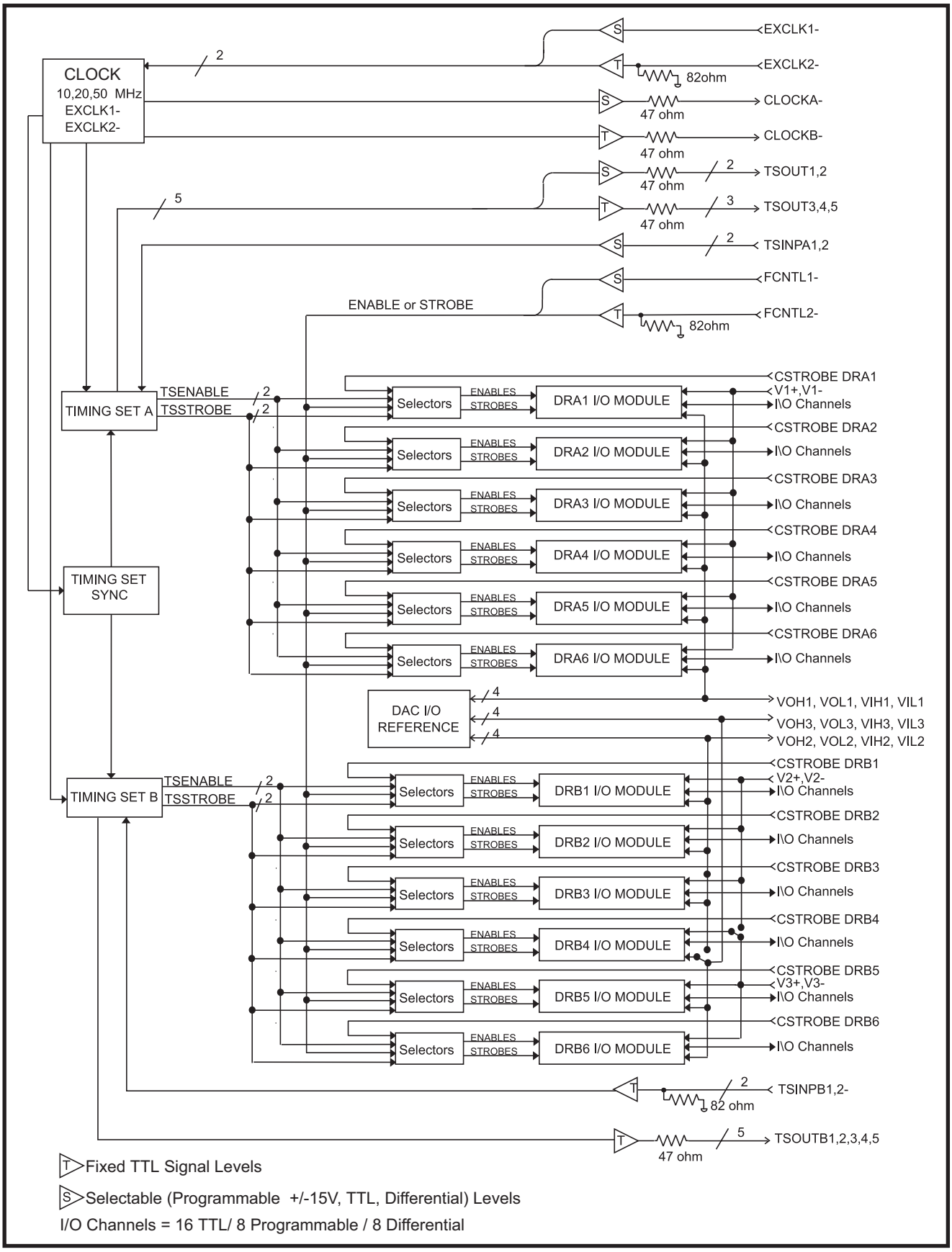


Figure 3 Motherboard Signal Routing

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The following table lists all the front panel connectors and there signal descriptions.

Connector Mnemonic	Number of Pins	I/O Description
J1	68	Contains CH1 through CH32, CSTROBE1 and CSTROBE2
J2	68	Contains CH33 through CH64, CSTROBE3 and CSTROBE4
J3	68	Contains CH65 through CH96, CSTROBE5 and CSTROBE6
J4	68	Contains CH97 through CH128, CSTROBE7 and CSTROBE8
J5	68	Contains CH129 through CH160, CSTROBE9 and CSTROBE10
J6	68	Contains CH161 through CH192, CSTROBE11 and CSTROBE12
J7	20	Used for synchronizing multiple SR192's together.
J8	60	Contains Timing Set I/O signals.
J9	28	Contains programmable reference signals.
J10	16	Positive and Negative rails for the programmable drivers.

Table 1 Front Panel Connector Description

3.1.3 I/O Level Translation

Certain I/O signals on the J8 connector can be either TTL, differential or programmable. The translators for these signals are located on the TSIO module located behind the SR192 front panel. The following table lists the I/O signal with selectable levels.

Signal Mnemonic	Signal Direction
TSINPUT1A	Input
TSINPUT2A	Input
FCNTL1	Input
EXTCLK1	Input
TSOUT1A	Output
TSOUT2A	Output
CLOCKA	Output

Table 2 Selectable I/O Levels

3.1.4 Error Counter and Address Memory

The motherboard monitors the real time compare error signals from every I/O module installed. If an error occurs then a counter is incremented and the address of the error is recorded in an error address RAM. This hardware eliminates the need to download the entire error memory to verify if an error had occurred saving time and test code.

The error counter will count up to 256K errors.

The error address RAM will store 128K error addresses

3.2 VXI/CPU Module

The CPU module resides in the last slot of the motherboard and communicates with the VXI backplane through the VXI module. It contains a Motorola 16MHz 68HC000 micro controller, FLASHRAM, system RAM, VXI interface logic and SR192 address map decoding logic. The CPU provides a SCPI format compatible parser to control data flow to/from the VXI controller. Many of the SR192 functions can also be accessed through the VXI A24/A32 space.

The FLASHRAM contains the SR192 operating system. Used in tandem with option BANK1 memory it allows the operating system to be field upgradeable without hardware modification. FLASHRAM programming support logic uses the 12 volts available from the VXI system backplane.

Option BANK1 memory also provides a means to execute different versions of the operating system without programming the FLASHRAM. BANK1 memory is loaded via the VXI A24/A32 space.

The CPU provides logic to automatically convert word transfers to and from the VXI A24/A32 space involving 8 bit SR192 I/O cards that support the Bus Size 8 (BS8-) signal.

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The following specifications apply to the CPU operating system:

SCPI Programming:

- Conforms to SCPI Version 1994.0 and IEEE-488.2 standard mandated commands.

VXI Interface:

- Message based, 1K byte input buffer, requires 8Meg of A24/A32 memory.
- A32 or A24 selectable A16D16 Slave.
- VXIbus IEEE-488.2 Instrument Protocol (I4).
- VXI Event Generation Protocol (EG).
- VXIbus Interrupter.
- SC (Static Configuration) Device.
- DC (Dynamic Configuration) Device.
- VXI Bus speed ~1uS per word.
- SCPI command parser throughput ~1ms per character.

The CPU communicates with the various plug-in modules via the address and data bus of the SR192 motherboard. The upper addresses form a module decode for the DAC, CPU, TSA, TSB, DRA1-DRA6 and DRB1-DRB6. Each slot can be addressed at up to 256K bytes. Along with the module decodes each slot has four function code lines F0 through F3. These function code lines enable each module to define 16 unique function codes address maps. These codes are used to pass module ID, operating status, etc. to the CPU or VXI.

The VXI module is a small PCB which mates with the CPU module and connects to the VXI system backplane . This module is the link to the SR192 for all VXI communication. In addition to providing the hardware link to the VXI bus it houses the system RAM for downloading operating system changes to the CPU FlashRAM, communication registers for the VXI protocol requirements, and optional RAM for future expansion.

3.3 DAC Module

The DAC Module is used to provide the output and input reference levels for the programmable I/O modules.

The SR192 is split into three reference groups as shown in figure 5.

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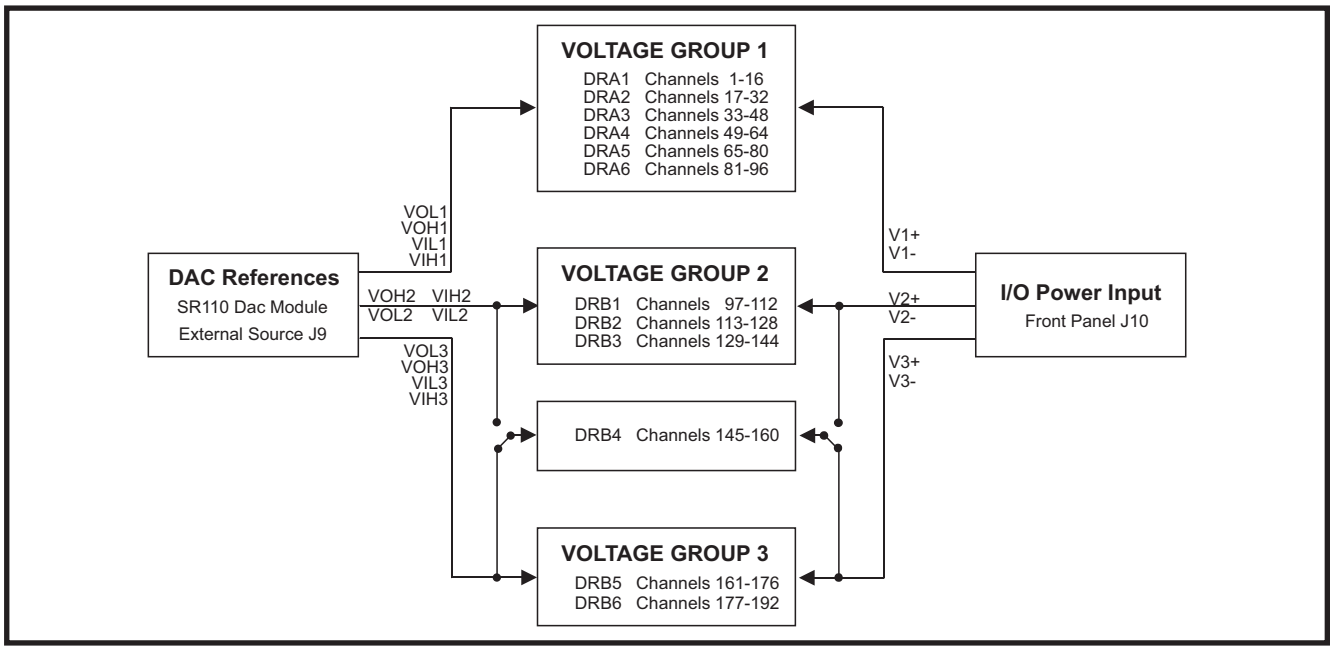


Figure 4 DAC Voltage Groups

Each voltage group has four references, VOL, VOH, VIL and VIH. The following table describes each reference and its range.

Reference Mnemonic	Description	Range
VOL	Output Low Level	-15 to +5 Volts
VOH	Output High Level	-5 to +15 Volts
VIL	Input Low Level	-15 to +5 Volts
VIH	Input High Level	-5 to +15 Volts

Table 3 DAC Reference Description

The resolution for all four references is 20mV.

3.4 I/O Module

Talon currently produces three type of I/O modules. Dynamic five memory, Dynamic three memory and static.

Dynamic I/O modules have 128K bits behind each channel for every memory. The 128K is user assignable and programmable into structures called TABLES. A table can be from 1 bit to 128K bits.

Static I/O module have one bit behind each channel.

Each IO module contains sixteen channels that are routed to the front panel for a total of 192 channels in an SR192 with 12 IO modules. The channel are user assignable and programmable into structures called GROUPS. A group can be from 1 channel to 192 channels.

Figure 6, on the following page, shows the relationship between tables and groups in the SR192.

The table structure allows the user to segment the 128K bits into smaller segments. Up to 256 tables can be created as long as there combined size is less than 128K.

The group structure allows the user to assign control signals to a group of channels even if the channels come from different IO modules inside the SR192. It also allows the user to program specific channel memory without affecting the remaining channels.

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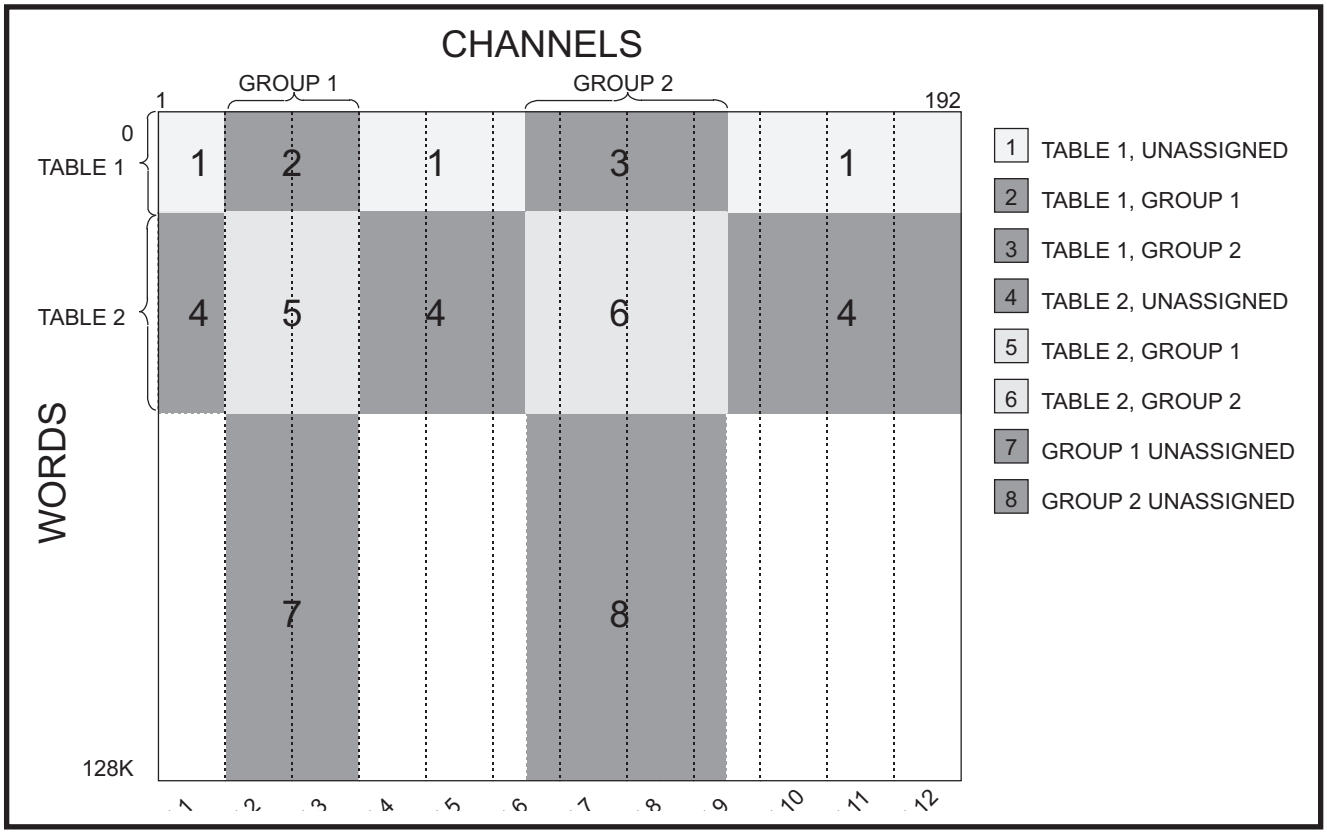


Figure 5 IO Module TABLES and GROUPS

3.4.1 Dynamic Output Architecture

The dynamic output structure of Talons I/O modules can be split into three types.

1. Standard Non-Registered.
2. Standard Registered.
3. Algorithmic

3.4.1.1 Standard Non-Registered Output

Figure 7 is the block diagram of the non-registered output structure.

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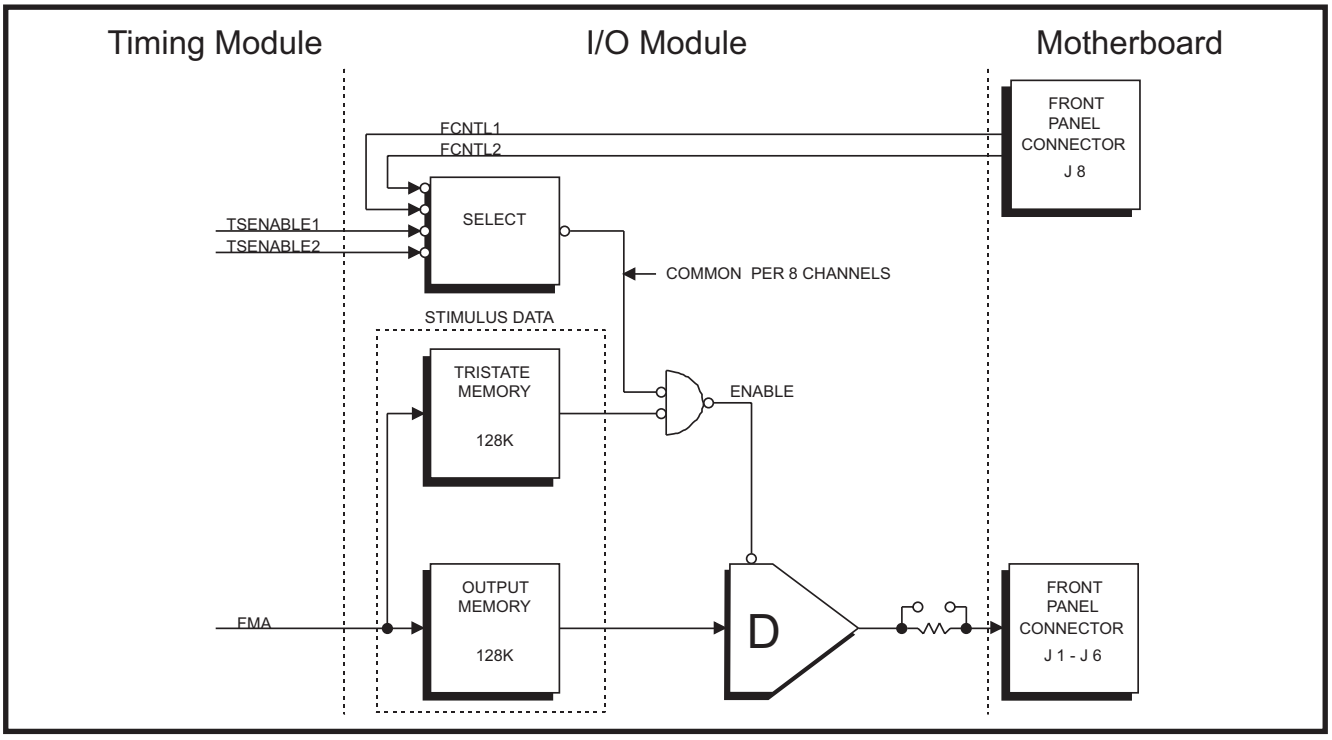


Figure 6 Block Diagram Non-Registered Output

Figure 7 shows four major blocks; the group enable selector, tristate memory, output memory and the driver.

The group enable selector allows the user to chose one of four signals to enable an entire group of channels. Each group of eight consecutive channels can have a different group enable signal describe below:

1. TSENABLE1 generated internally from the timing module.
2. TSENABLE2 generated internally from the timing module.
3. FCNTL1 generated externally from the J8 front panel connector.
4. FCNTL2 generated externally from the J8 front panel connector.

The tristate and output memory allows the user to generate stimulus and enable data on a per pin basis. Both memories are addressed internally by the FMA (Field Memory Address) bus generated by the timing module.

The driver is either fixed TTL, RS485 differential or +/-15V programmable.

The following figure and table illustrates the timing relationship for a single channel of non-registered output. The TS CLOCK and FMA signals are generated from the timing module and are described in detail in section 3.5 of this manual.

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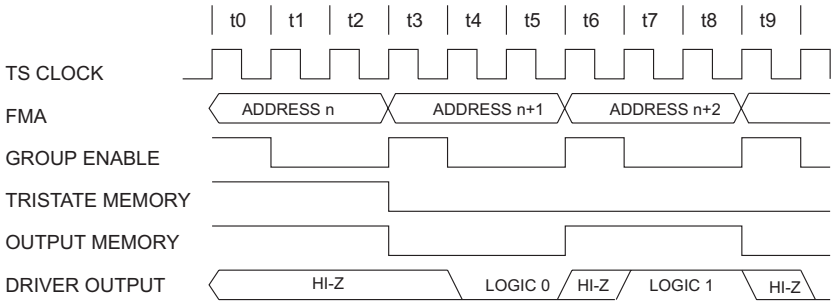


Figure 7 Non-Registered Output Timing Example

Time	Description
t0	New Field Memory Address (FMA) from timing module causes OUTPUT and TRISTATE MEMORY to go high.
t1	GROUP ENABLE goes low but DRIVER OUTPUT is HI-Z due to TRISTATE MEMORY set high.
t2	GROUP ENABLE goes low but DRIVER OUTPUT remains HI-Z due to TRISTATE MEMORY set high.
t3	New FMA address causes both TRISTATE and OUTPUT MEMORY to go low but DRIVER OUTPUT remains HI-Z due to GROUP ENABLE set high.
t4	GROUP ENABLE goes low in conjunction with the TRISTATE memory low causes the DRIVER OUTPUT to be enabled and set to logic 0 level.
t5	GROUP ENABLE and TRISTATE MEMORY remain low. DRIVER OUTPUT still enabled and set to logic 0 level
t6	New FMA address causes OUTPUT MEMORY to go high, DRIVER OUTPUT goes HI-Z due to GROUP ENABLE set high.
t7	GROUP ENABLE goes low causing DRIVER OUTPUT to go to logic 1 level.
t8	GROUP ENABLE and TRISTATE MEMORY remain low. DRIVER OUTPUT still enabled and set to logic 1 level
t9	New FMA address causes OUTPUT MEMORY to go low. DRIVE OUTPUT goes HI-Z due to GROUP ENABLE going high.

Table 4 Non-Registered Output Timing Description

3.4.1.2 Standard Registered Output

The figure 9 shows the block diagram of the registered output structure.

The registered output structure is identical to the non-registered except that the output and tristate memories are registered prior to the output driver. The register is loaded by the low level of an internal signal generated from the timing module (STIM_LOAD).

Figure 10 and the following table on the opposite page illustrates the timing relationship for a single channel of registered output.

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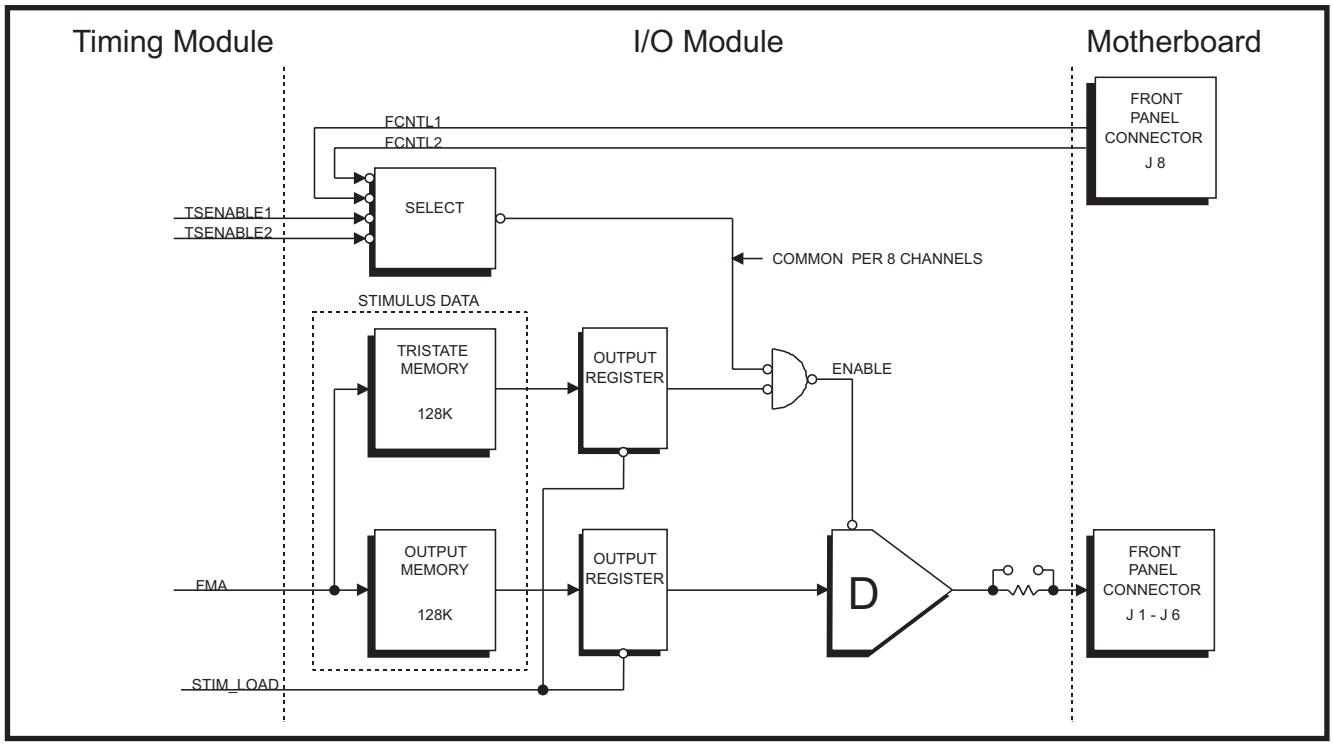


Figure 8 Block Diagram Registered Output

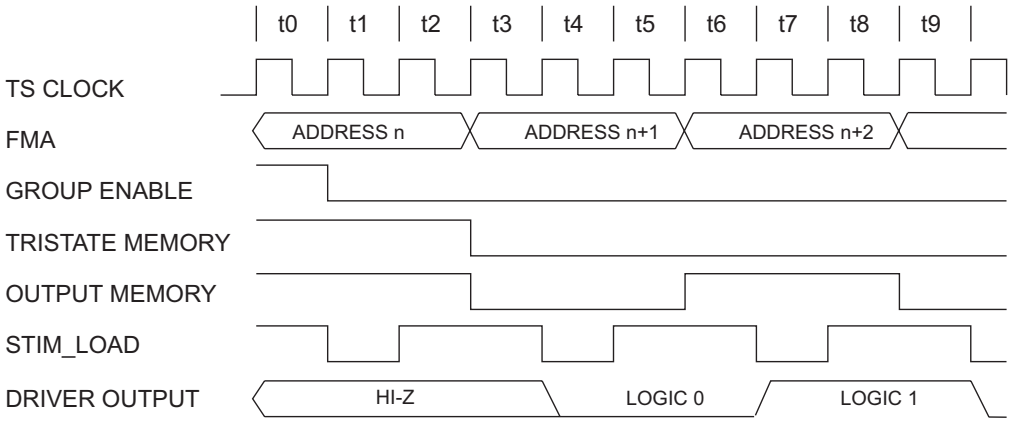


Figure 9 Registered Output Timing Example

Time	Description
t0	New Field Memory Address (FMA) from timing module causes OUTPUT and TRISTATE MEMORY to go high. GROUP ENABLE high puts DRIVER OUTPUT into HI-Z.
t1	GROUP ENABLE and STIM_LOAD goes low. DRIVER OUTPUT is HI-Z due to registered TRISTATE MEMORY set high.
t2	DRIVER OUTPUT remains HI-Z due to registered TRISTATE MEMORY set high.
t3	New FMA address causes both TRISTATE and OUTPUT MEMORY to go low but DRIVER OUTPUT remains HI-Z because STIM_LOAD has not loaded the new TRISTATE and OUTPUT MEMORY.
t4	STIM_LOAD goes low causing the DRIVER OUTPUT to be enabled and set to logic 0 level.
t5	GROUP ENABLE and registered TRISTATE MEMORY remain low. DRIVER OUTPUT still enabled and set to logic 0 level
t6	New FMA address causes OUTPUT MEMORY to go high, DRIVER OUTPUT remains low.
t7	STIM_LOAD goes low causing DRIVER OUTPUT to go to logic 1 level.

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Time	Description
t8	GROUP ENABLE and registered TRISTATE MEMORY remain low. DRIVER OUTPUT still enabled and set to logic 1 level.
t9	New FMA address causes OUTPUT MEMORY to go high. DRIVE OUTPUT remains high.

Table 5 Registered Output Timing Description

3.4.1.3 Algorithmic Output

Figure 11 is the block diagram for I/O modules that have algorithmic output.

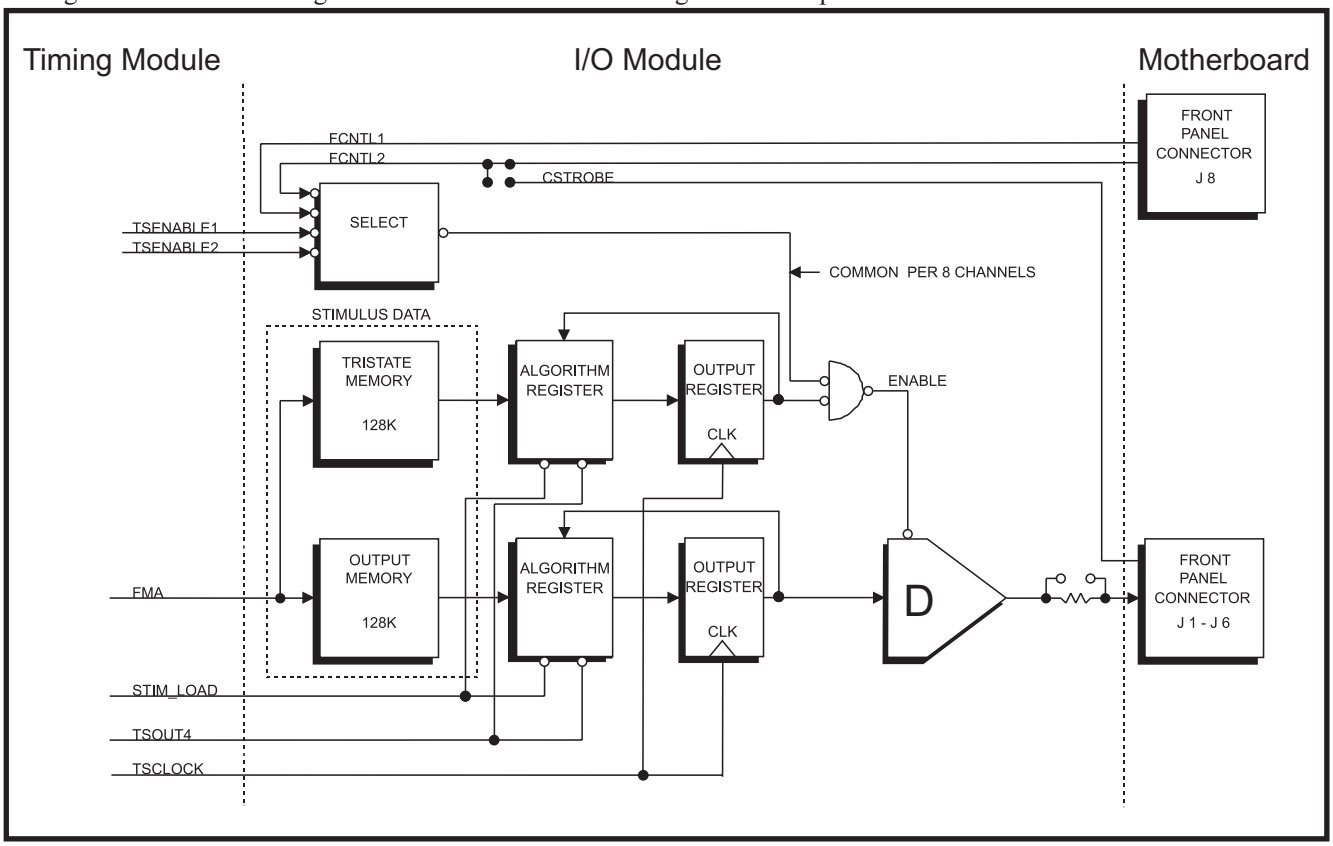


Figure 10 Algorithmic Output Block Diagram

At first glance the algorithmic and registered output architectures appear similar with the exception of an algorithm generator between the stimulus memory and the output register.

The data from the stimulus memory is loaded into the algorithm register on the low level of STIM_LOAD signal.

The selected algorithmic function is performed on the low level of the TSOUT4 timing module signal. When TSOUT4 is high the ALGORITHM REGISTER goes into a HOLD mode, i.e., the output is routed back into the input of the OUTPUT REGISTER.

OUTPUT REGISTER Data is always registered on the rising edge of the TSCLOCK signal.

The algorithm register contains the logic to select and perform one of ten output algorithms:

1. HOLD
2. SERIAL
3. MULTIPLEX

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4. INCREMENT BY ONE
5. INCREMENT BY TWO
6. INCREMENT BY FOUR
7. INCREMENT BY EIGHT
8. DATA FORMAT RETURN TO ONE
9. DATA FORMAT RETURN TO ZERO
10. DATA FORMAT RETURN TO COMPLIMENT

3.4.1.3.1 HOLD Output Algorithm

The HOLD algorithm routes the output to the input of the OUTPUT REGISTER when TSOUT4 is low.

3.4.1.3.2 SERIAL Output Algorithm

The SERIAL algorithm takes the contents of the OUTPUT REGISTER and shifts it one bit when TSOUT4 is low. Data is shifted from the most significant channel to the least significant channel. The least significant channel can also be routed to the most significant channel of the next adjacent 8 channels.

3.4.1.3.3 MULTIPLEX Output Algorithm

The MULTIPLEX algorithm takes the contents of the OUTPUT REGISTER's upper nibble and copies it to the lower nibble when TSOUT4 is low.

3.4.1.3.4 INCREMENT Output Algorithm

The INCREMENT algorithm adds the increment value to the current value of the OUTPUT REGISTER and feeds it back into the OUTPUT REGISTER when TSOUT4 is low. A carry out signal is generated and passed to adjacent modules.

3.4.1.3.5 Data Format Output Algorithm

The data format algorithm performs the desired return function to the contents of the OUTPUT REGISTER when TSOUT4 is low.

3.4.2 Dynamic Input Architecture

The input architecture, like the output output architecture, can be be viewed as three types:

1. Standard Input, Non-Registered Output
2. Standard Input, Registered Output
3. Algorithmic Input

3.4.2.1 Standard Input, Non Registered Output

Figure 12 shows the block diagram of the SR192 input architecture using non registered output.

The figure above shows six major blocks; the group strobe selector, expect memory, mask memory, record memory, comparator logic and the receiver.

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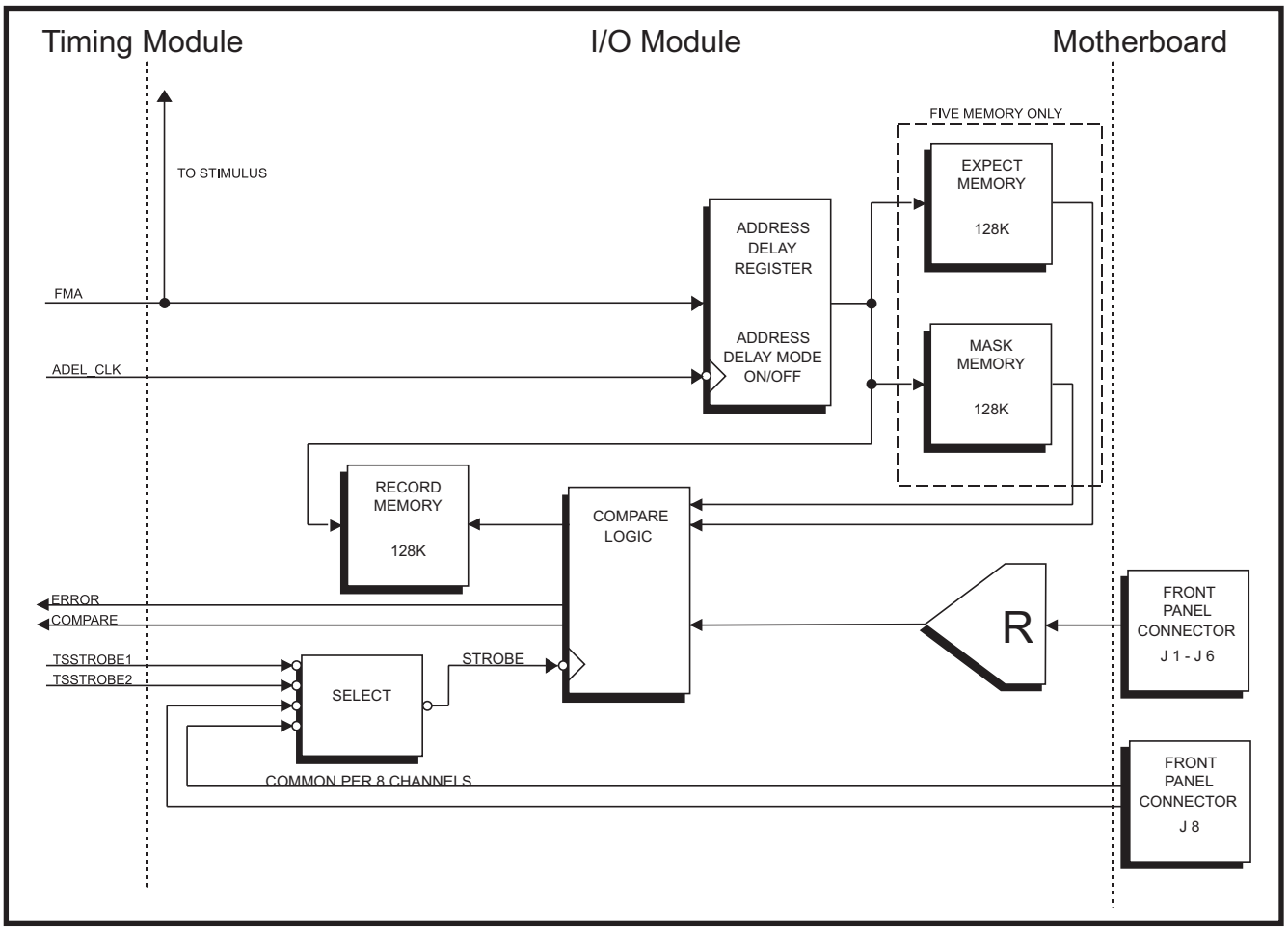


Figure 11 Standard Input, Output Non Registered

The group strobe selector allows the user to chose one of four signals to strobe an entire group of channels. Each group of eight consecutive channels can have a different group strobe signal describe below:

1. TSSTROBE1 generated internally from the timing module.
2. TSSTROBE2 generated internally from the timing module.
3. FCNTL1 generated externally from the J8 front panel connector.
4. FCNTL2 generated externally from the J8 front panel connector.

The expect and mask memory (available in the five memory modules) allows the user to generate expect results for the real time comparator. Both memories are addressed internally by the FMA (Field Memory Address) bus generated by the timing module. The FMA bus can additionally be registered by the address delay register if the expected response is delayed until after the next stimulus word is output. The address delay register is enabled/disabled via software and the controlling clock (ADEL_CLK) is generated from the timing module. The following table lists what can be compared using the expect and mask memories.

MASK BIT	EXPECT BIT	REAL TIME COMPARE CONDITION
0	0	Expect a zero. Data < VIL level
0	1	Expect a one. Data > VIH level
1	0	Mask bit off from real time compare.
1	1	Expect tristate. Data > VIL and Data < VIH

Table 6 Expect and Mask Memory

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The record memory stores the results of the compare logic. The compare logic also generates two signals (ERROR and COMPARE) back to the timing module that indicates if a compare or non compare was detected.

The results of the compare logic as well as the ERROR signal are latched on the falling edge of the STROBE signal. The COMPARE signal is the raw unlatched result of the compare logic.

The receiver is either fixed TTL, RS485 differential or +/-15V dual threshold programmable.

3.4.2.2 Standard Input Registered Output

Figure 13 shows the block diagram of the SR192 input structure when the output data is registered.

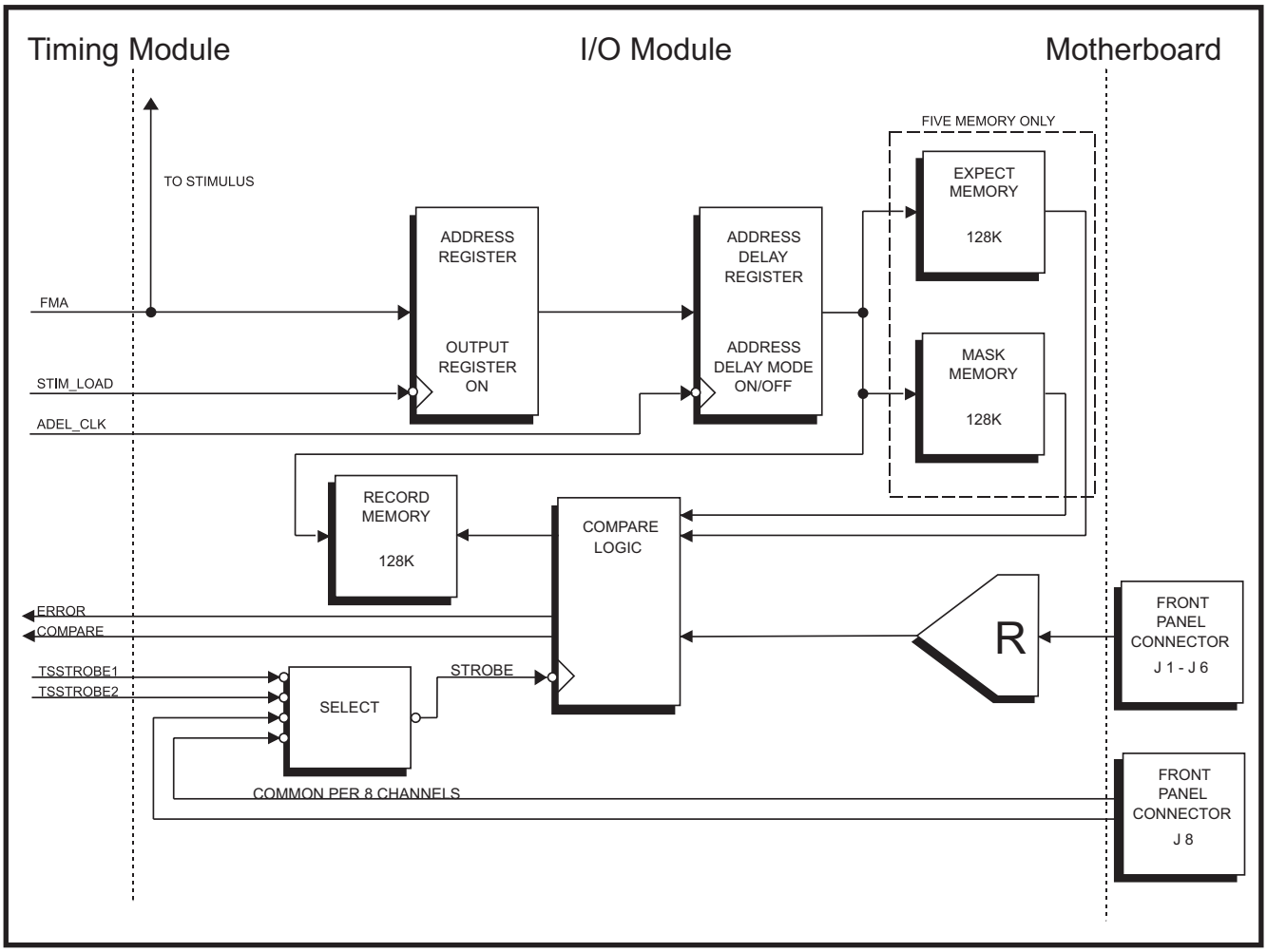


Figure 12 Standard Input, Output Registered

When the output data is registered the FMA bus is registered by the STIM_LOAD signal in order to synchronize the stimulus data with the mask and expect memories.

3.4.2.3 Algorithmic Input Architecture

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Figure 14 shows the block diagram of the algorithmic input architecture of the IO modules.

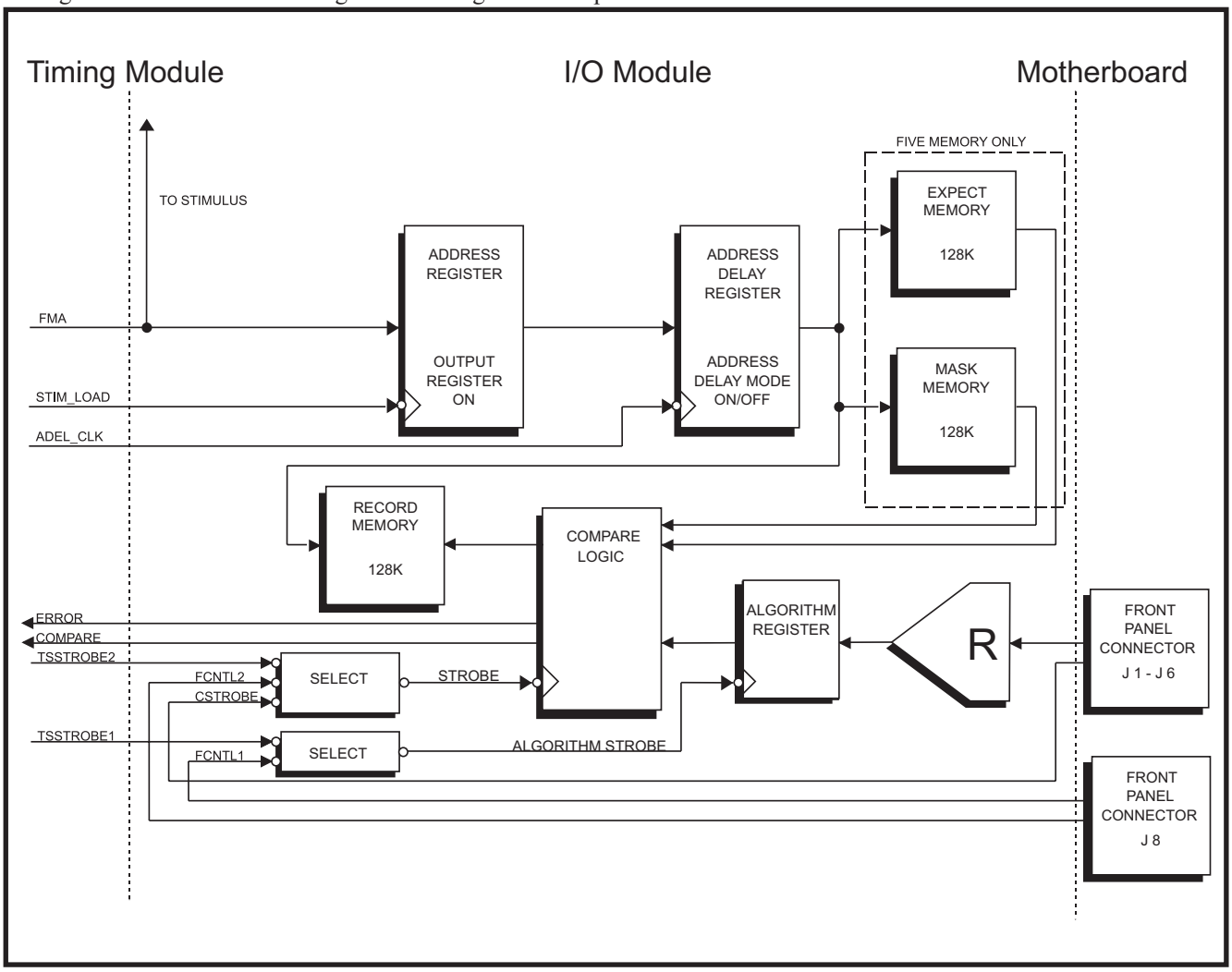


Figure 13 Algorithmic Input

There are two input algorithmic modes where the algorithm register is used (SERIAL and MULTIPLEX). All other modes set the algorithm register to transparent, i.e., data from the receiver is passed directly to the compare logic.

3.4.2.3.1 SERIAL Input Algorithm

The serial input algorithm take the data from the serial input bit and latches it into the input shift register on the falling edge of the ALGORITHM STROBE signal. The parallel data word is latched and compared on the falling edge of the STROBE signal.

The serial input bit can be either the most significant channel from the front panel or the serial output bit from the adjacent IO module.

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3.4.2.3.2 MULTIPLEX Input Algorithm

The ALGORITHM STROBE in the MULTIPLEX mode latches the lower nibble of the multiplexed data on the falling edge. The falling edge of the STROBE signal latches the upper nibble and triggers the compare logic.

3.4.3 Static Input/Output Architecture

The static IO modules provide a low cost solution to user who don't require high speed drivers or memory behind each pin.

Figure 15 shows the static non registered output block diagram.

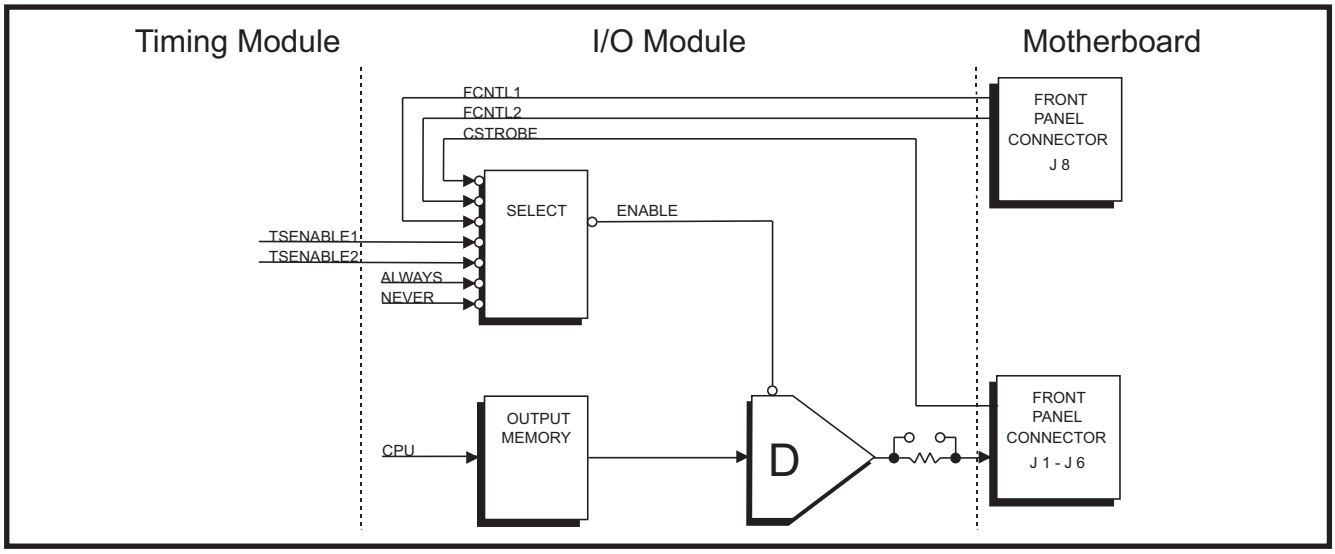


Figure 14 Static Non Registered Output

The enable selector allows the user to select the enable source for each pin. In addition the enable can be forced true always or never.

The output memory is a single sixteen bit register that can be programmed through software or directly via A32/A24 bus access.

Two types of static IO modules are available. The SR106 contains eight +/-15V programmable outputs and eight fixed TTL outputs. The SR107 contains sixteen fixed TTL outputs.

Figure 16 is the block diagram for the non registered static input.

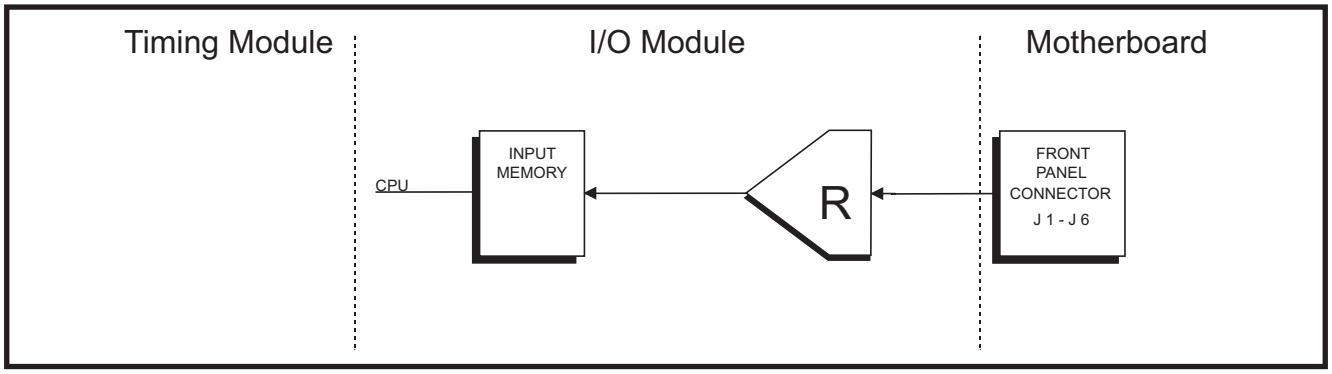


Figure 15 Static Non Registered Input

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The SR106 contains eight +/-15V single threshold programmable receivers and eight fixed TTL receivers. The SR107 contains sixteen fixed TTL receivers.

Figure 17 is the block diagram of the static registered output architecture.

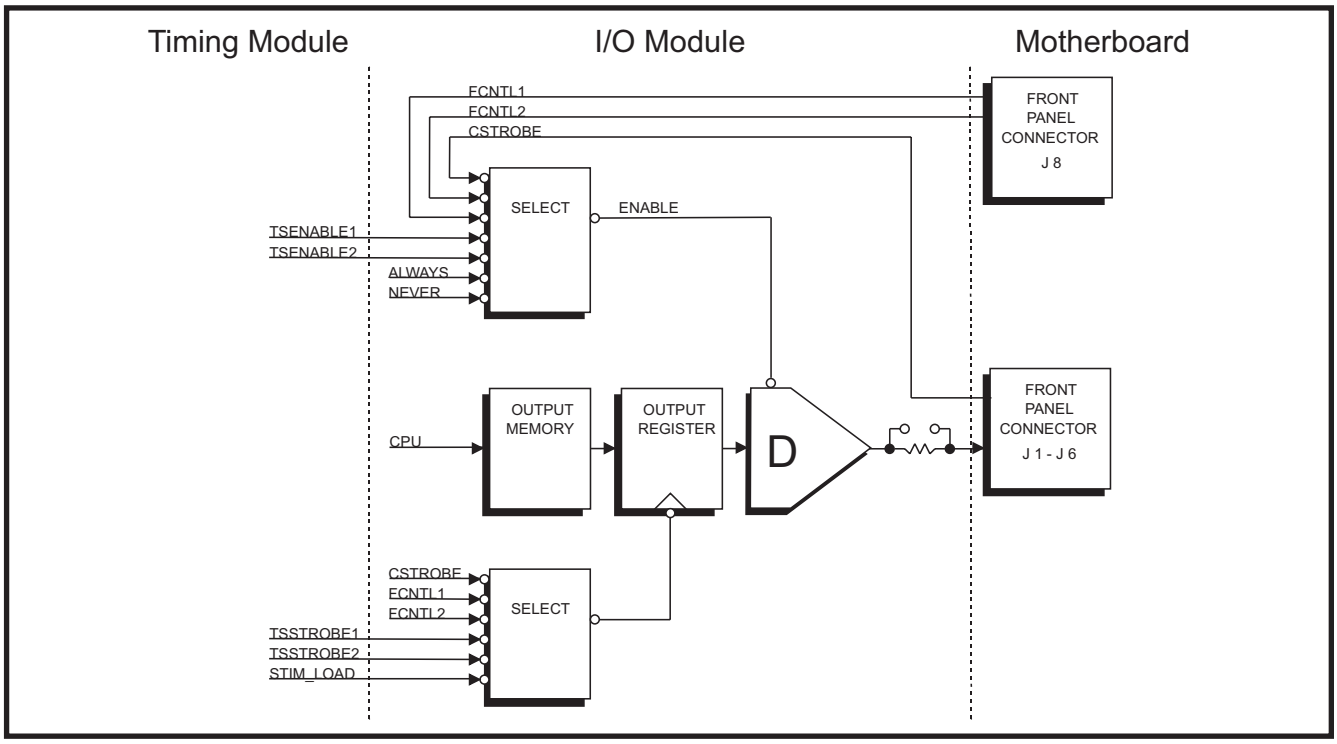


Figure 16 Static Registered Output

The registered output structure adds a selector and a register between the output memory and the driver.

Figure 18 is the registered static input block diagram.

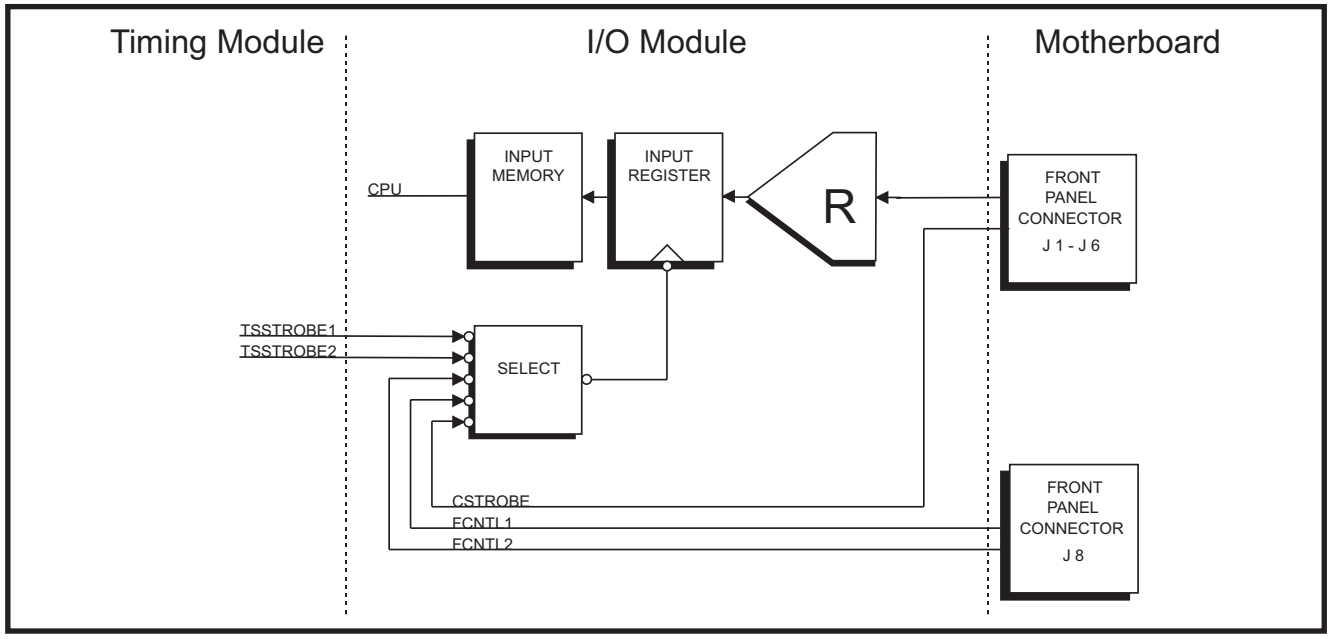


Figure 17 Static Registered Input

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3.5 Timing Set Module

The timing set module is the heart of the SR192 system. It controls what data is to be output and the timing of that data.

The timing of the stimulus/response data is specified in a structure called a TIMING SET. In addition the timing set provides the user with programmable outputs and control signals to simulate UUT timing and control.

The link between the timing set (defines stimulus/response timing) and the tables (defines the stimulus/response memory) is made in a structure called a SEQUENCE. A sequence is a timing set and a data table.

Two types of timing set modules are available, the SR100 and the SR101.

3.5.1 SR100 Timing Module

Figure 19 shows the block diagram of Talons SR100 timing module.

The TS CLOCK signal determines the minimum cell resolution of the timing set. The range of TS CLOCK is from DC to 50 MHz. The source of TS CLOCK is either internal or external.

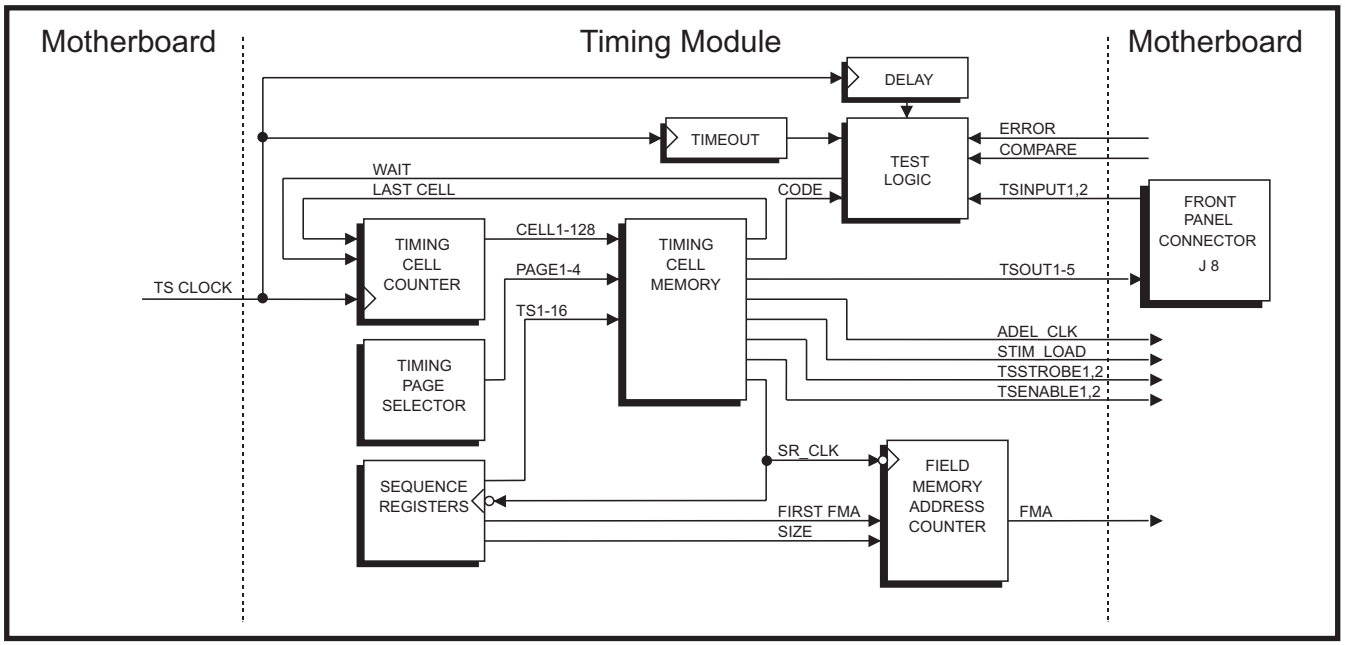


Figure 18 SR100 Block Diagram

The TIMING CELL COUNTER generates the cell address for the timing memory. Each timing set can have from 2 to 128 cells. The counter is cleared when the LAST CELL bit from the timing memory signals the end of the timing set. The WAIT signal acts as a count enable forcing the cell address not to increment while the TEST LOGIC is waiting for a handshake.

The TEST LOGIC allows the operator to test for a condition and wait at a specific cell address until the condition becomes true. A timeout value can be programmed to terminate the WAIT condition. The following conditions can be tested and waited for:

- High or low level of a front panel input.
- High or low transition of a front panel input.
- The latched error signal from the IO modules.

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- The unlatched compare signal from the IO modules.
- Programmable delay.

The PAGE SELECTOR allows the operator to select 1 of four pages of sixteen timing sets. Each page has a predefined timing set called IDLE.

The TIMING CELL MEMORY is used to program internal IO module control signals, general purpose user output signals and test codes.

The following figure is from the SR192 Timing Editor software.

The timing signals are defined as follows:

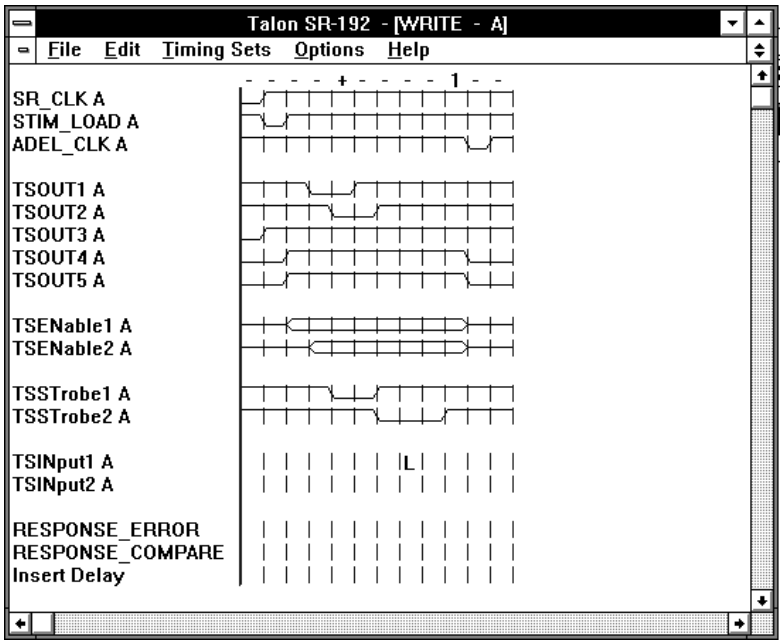


Figure 19 Timing Set Cell Editor

1) **SR_CLK**: The SR_CLK signal clocks the sequence logic. This starts the fetching of the next I/O word. All timing is referenced from the high to low edge of this signal.

2) **STIM_LOAD**: For applications where data signals cannot tolerate a “glitch” between successive I/O memory accesses, the STIM_LOAD signal clocks the Output Register on the I/O boards.

3) **ADEL_CLK:** For applications where the Input Sample Pulse is at the very end of the output cycle or into the next output cycle, the ADEL_CLK signal supplies a timing delay for the input logic.

4) **TSOUT1 through TSOUT5**: Five user defined timing signals

5) **TSENABLE1,2**: Group enable signals for output channels 1 to 96 or 97 to 192.

6) **TSSTROBE1,2**: Strobe signals for input channels 1 to 96 or 97 to 192.

7) **TSINPUT1,2**: Input signals to the timing set from the UUT. These signals can be tested for either a logic high or logic low condition. Test input 2 can also be tested for a high to low transition or a low to high transition. Multiple tests can occur within a timing set.

8) **RESPONSE_ERROR**: This Input signal is from the Channel Compare I/O logic. At the appropriate time during an I/O cycle, the comparator can be tested for an error. If an error occurs, the timing set will hang-up (if no timeout is programmed) and the VXI controller will be informed of the event.

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9) **RESPONSE_COMPARE**: Input signal from the Channel Compare I/O logic. At the appropriate time during an I/O cycle the Raw Compare can be tested for a compare. This function is used to wait for the UUT to be equal to a known logic state. The timeout function is disabled when testing the Raw Input Compare.

10) **Insert Delay**: A delay can be inserted into any of the timing cells. The delay causes the timing cell counter to wait until the delay counter is complete.

The SEQUENCE REGISTERS specify the timing set number, the first field memory address and the size (number of field memory addresses) for four individual sequences.

The FIELD MEMORY ADDRESS COUNTER generates the addresses for the IO modules.

3.5.1.1 SR100 Sequence Overview

Figure 21 depicts a timing sequence for the SR100 timing module. The sequence is created by grouping previously created timing sets and tables together into subsequences.

The overall sequence can be from 1 to 4 subsequences.

SUBSEQUENCE 1 = TIMING SET 4, TABLE 1.

SUBSEQUENCE 2 = TIMING SET 2, TABLE 2.

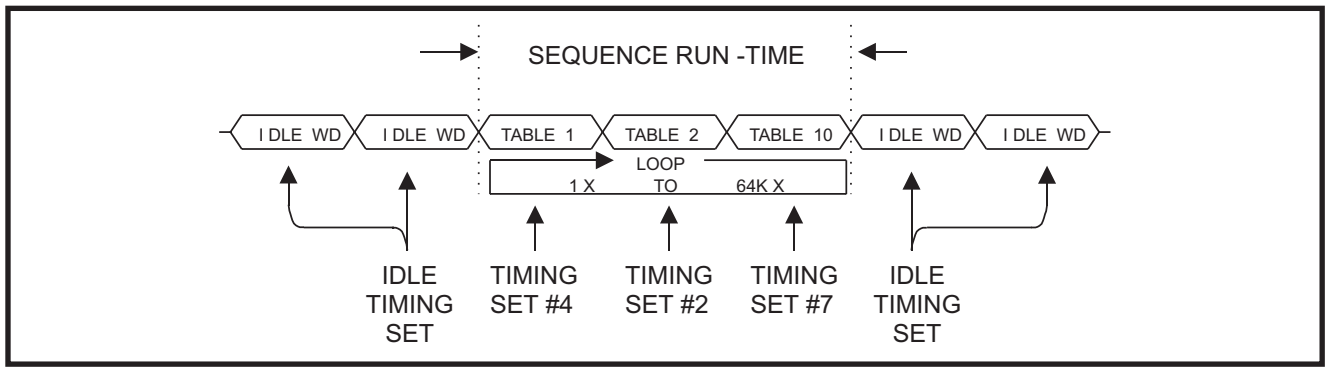


Figure 20 SR100 Sequence Example

SUBSEQUENCE 4 = TIMING SET 7, TABLE 10.

LOOP COUNT = from 1 to 64K

Tables 1,2,10 can all be a single word or combined up to 128K words.

Once the overall sequence is defined the user starts or executes the sequence. Starting a sequence causes the SR100 to enter the idle state if it is not already active. The idle state in the SR192 is executing the IDLE sequence. This includes the IDLE timing set as well as an idle data word.

Upon detection of the last timing set cell of the idle timing set, the SR192 steps to subsequence #1, selecting the respective timing set and table #. There is zero delay while changing timing sets and data tables between subsequences.

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The SR192 remains in subsequence #1 until the last word of the table, and the last bit of the timing set is detected.

At the time when the first subsequence is complete, the logic checks to see if this is the last subsequence. If it is not, the next subsequence is accessed and executed. When the last subsequence is detected, the loop counter is tested for completion. If it is not complete, the first subsequence is accessed and the entire one, two, three or four subsequences are repeated. When the loop counter is complete and the last subsequence is detected, the logic returns to the idle sequence. In all cases, there is zero delay when changing timing sets and data tables.

When complete, the user can interrogate the input memories, request CRC's to be generated on the input memories, execute a host of other commands, including the execution of another sequence of operations.

3.5.2 SR101 Timing Module

Figure 22 shows the block diagram of the SR101 timing module.

The SR101 is similar to the SR100 except instead of only having four sequence registers, the SR101 has 128K sequence memory controlled by sequence logic.

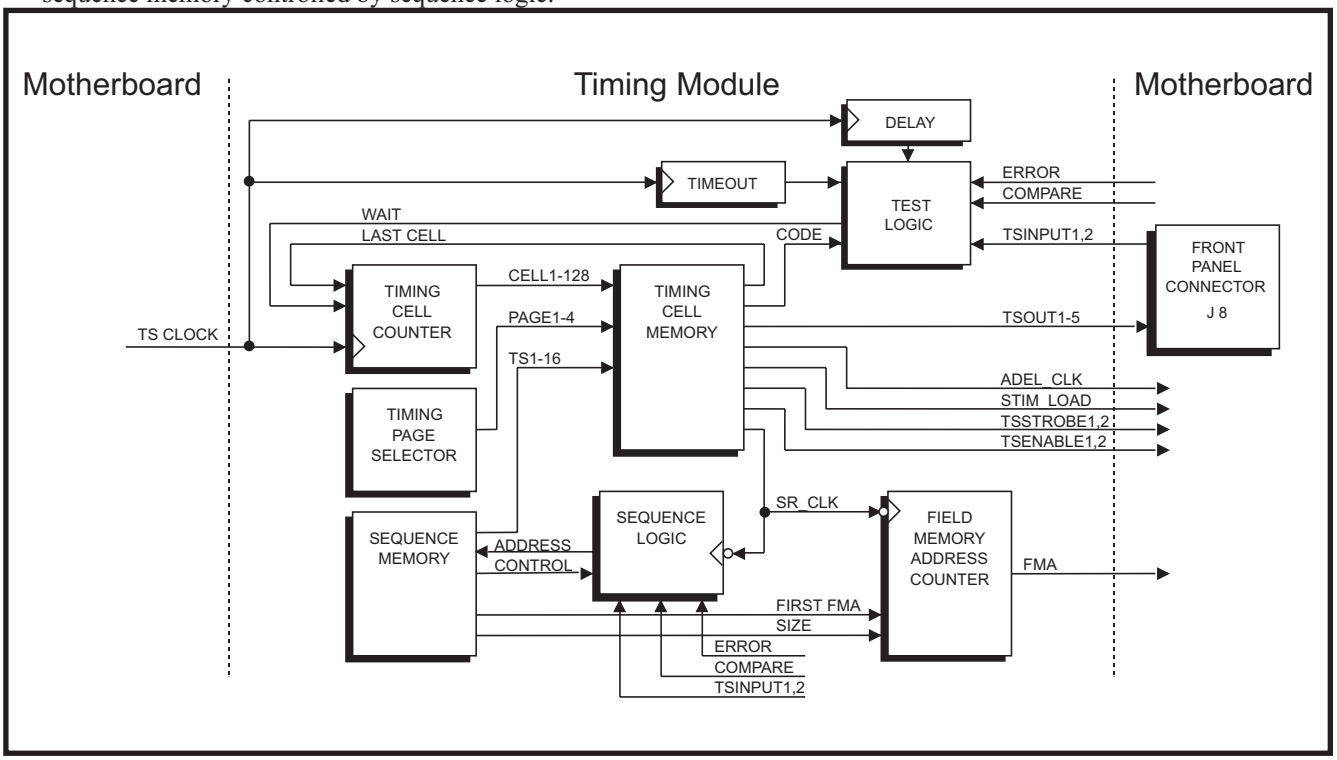


Figure 21 SR101 Block Diagram

The sequence logic generates a sequence address to the memory which specifies the sequence control, timing set, first FMA and size. The sequence logic can also be programmed to jump conditionally or unconditionally to another sequence.

The sequence control consists of the follow ing signals:

1) **JUMP CODE:** The JUMP CODE allows the operator to program a jump condition for the current sequence. The following conditions can be programmed:

TSINPUT1,2 Level	Jump if TSINPUT1,2 is high or low.
COMPARE	Jump if a compare is detected from the IO modules.
ERROR	Jump if a error is detected from the IO modules.

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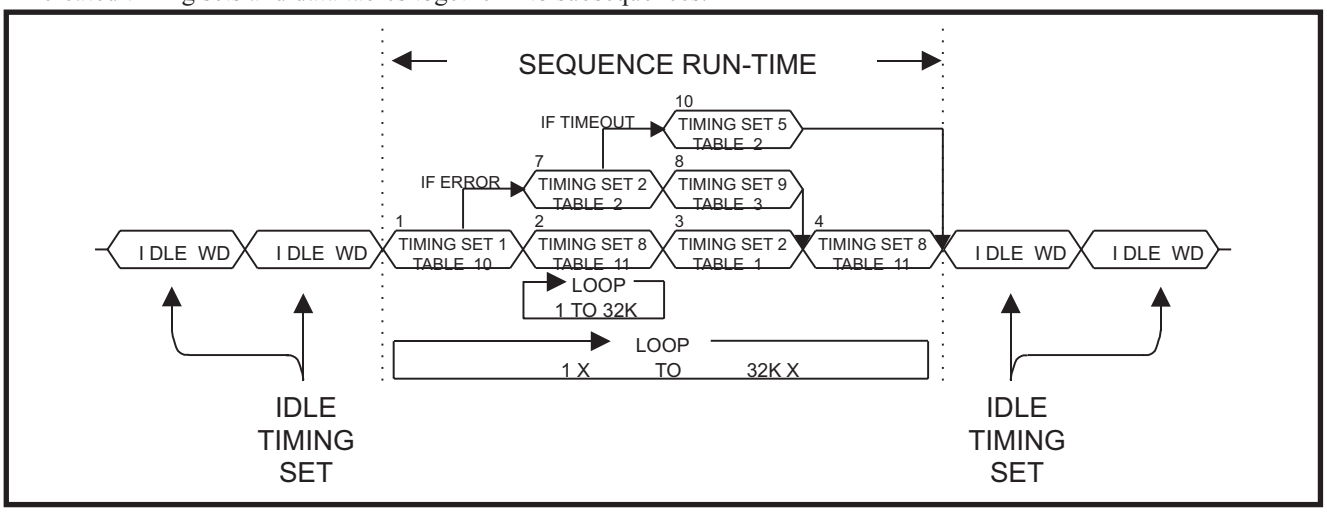
TIMEOUT	Jump if a timeout is detected from the timing module.
UNCONDITIONAL	Jump unconditionally.

2) **JUMP SEQUENCE ADDRESS**: The JUMP SEQUENCE ADDRESS is the sequence number to jump to if a jump occurs.

3) **SEQUENCE LOOP**: The SEQUENCE LOOP programs a loop counter for each sequence.

3.5.2.1 SR101 Sequence Overview

Figure 23 depicts a timing sequence for the SR101 timing module. The sequence is created by grouping previously created timing sets and data tables together into subsequences.



22Figure 22 SR101 Sequence Example

The overall sequence can be from 1 to 128K subsequences.

SUBSEQUENCE 1	TIMING SET 1, TABLE 10, JUMP TO SUBSEQUENCE 7 IF ERROR FROM IO MODULE.
SUBSEQUENCE 2	TIMING SET 8, TABLE 11, LOOP from 1 to 32K.
SUBSEQUENCE 3	TIMING SET 2, TABLE 1.
SUBSEQUENCE 4	TIMING SET 8, TABLE 11.
SUBSEQUENCE 7	TIMING SET 2, TABLE 2, JUMP TO SUBSEQUENCE 10 IF TIMEOUT FROM HANDSHAKE.
SUBSEQUENCE 8	TIMING SET 9, TABLE 3, JUMP TO SUBSEQUENCE 4.
SUBSEQUENCE 10	TIMING SET 5, TABLE 2, JUMP TO END.
SEQUENCE LOOP COUNT	from 1 to 32K

Tables 1, 2, 3, 10 and 11 can all be a single word or combined up to 128K words.

Once the overall sequence is defined the user starts or executes the specific subsequence (1 to 128K). Starting a sequence causes the SR101 to enter the idle state if it is not already active. The idle state in the SR192 is executing the IDLE sequence. This includes the IDLE timing set as well as an idle data word.

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Upon detection of the last timing set cell of the idle timing set, the SR192 steps to specified subsequence (#1 in our example), selecting the respective timing set and data table #. There is **zero delay** while changing timing sets and data tables between sequences.

The SR192 remains in the current subsequence until either the last cell of the timing set is detected and either the last word of the table or a jump condition is true. If the last word of the table is true then the logic tests the subsequence loop counter for completion. If the subsequence loop counter in not complete the the current subsequence is re-executed. If the loop counter is complete then the current subsequence is complete. If a jump condition is true then the current subsequence is switched to the specified jump subsequence.

At the time when the current subsequence is complete, the logic checks to see if this is the last subsequence. If it is not, the next subsequence is accessed (current plus one) and executed. When the last subsequence is detected, the loop counter is tested for completion. If it is not complete, the first subsequence is accessed and the entire sequence is repeated. When the loop counter is complete and the last sequence is detected, the logic returns to the idle sequence. In all cases, there is zero delay when changing timing sets and data tables.

When complete, the user can interrogate the input memories, request CRC's to be generated on the input memories, execute a host of other commands, including the execution of another sequence of operations.

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4 WHY THE BUS EMULATION MODE?

Assume an output waveform is to be generated as in figure 24.

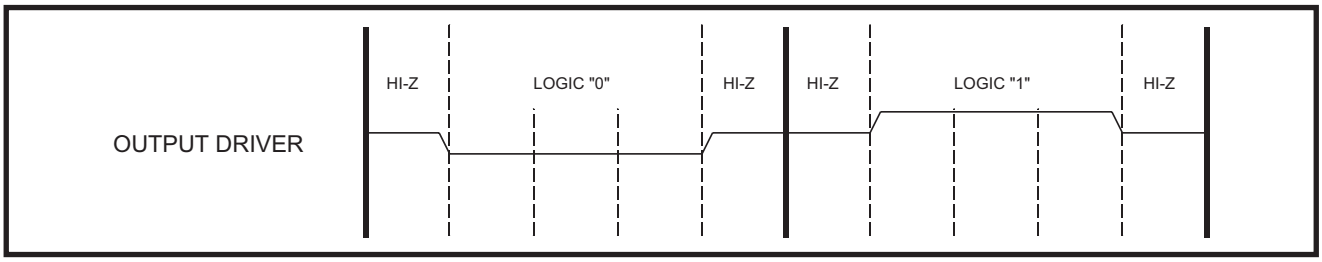


Figure 23 Bus Emulation Output Example

To generate this waveform using traditional stimulus/response mode the timing set enable output signal (TSENABLE) will be set low and the tristate memory will define when the output will be active. The output memory will define the output state, figure 25

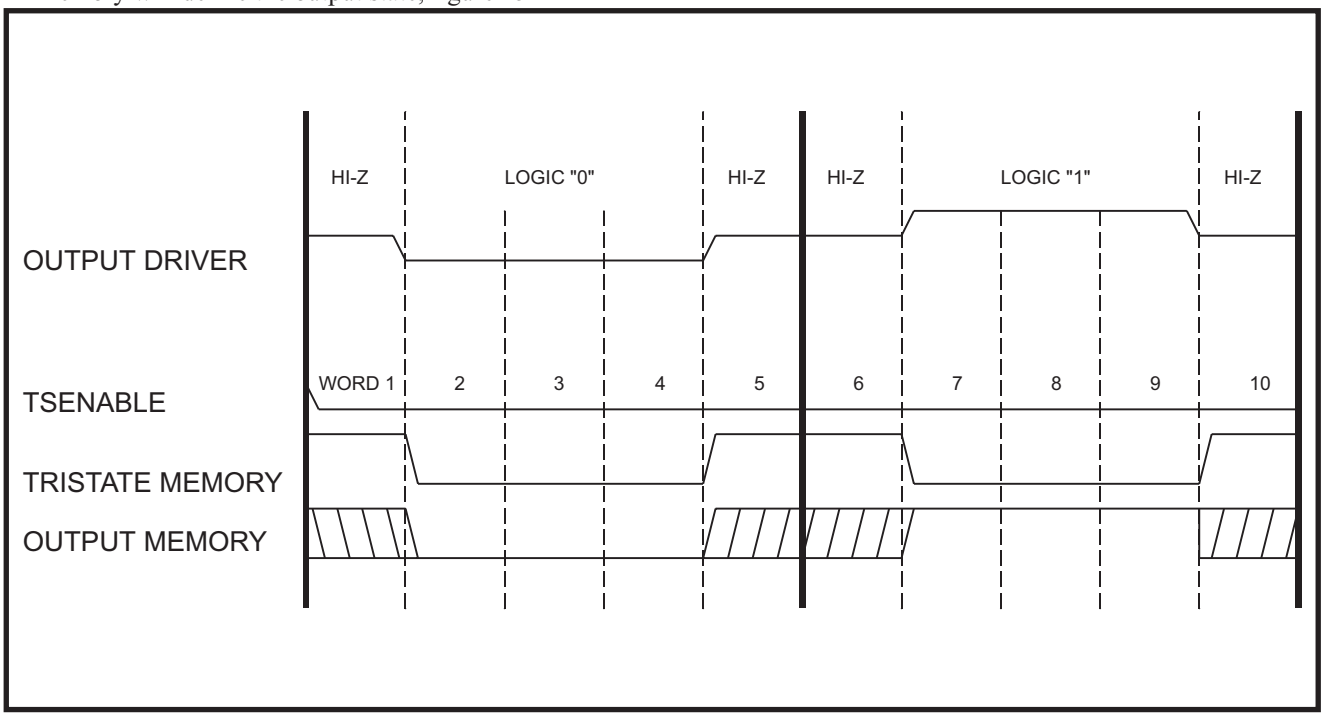


Figure 24 Stimulus/Response Mode Example Timing

To generate the same output using the bus emulation mode, figure 26, the tristate memory will be set low and the timing set output enable signal will enable the output. Again the output memory will define the state of the output. Note that bus emulation requires only two words of memory to generate these signals, where as the stimulus/response mode requires ten words of memory.

The obvious answer is that in bus emulation applications, a great deal of memory can be saved. This is true, however there is a far more important feature.

In most bus emulation applications, the receiving device transmits a signal back to the master device indicating that it is ready to either receive data or to transmit data. This event is known as “handshaking”. Typically, the handshake signals are nomenclatured with a “ready”, “data available” or similar mnemonic.

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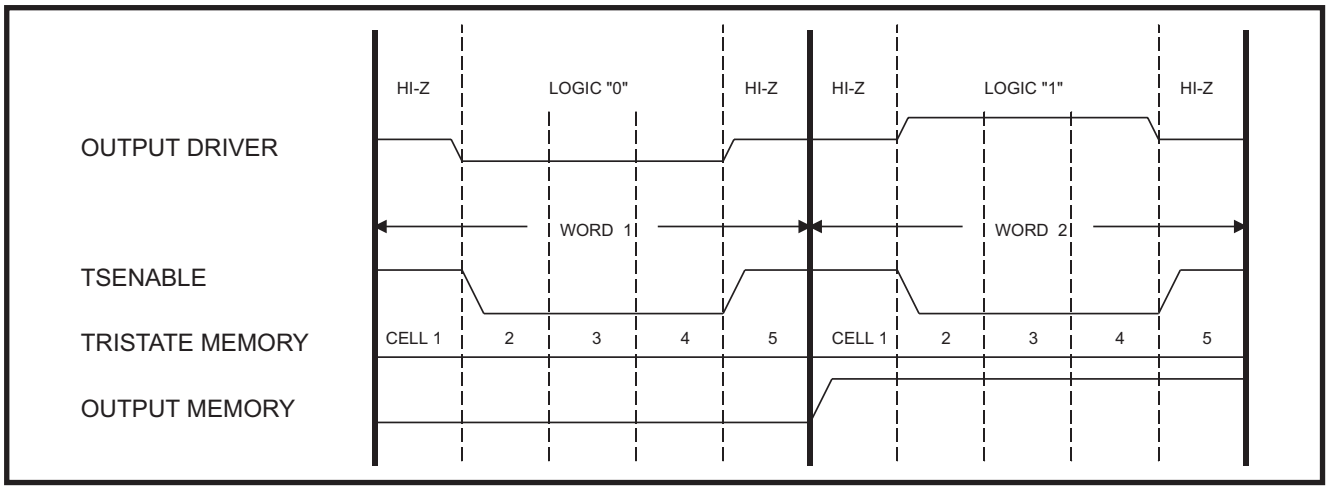


Figure 25 Bus Emulation Mode Example Timing

Thus, bus emulation requires that the timing set logic have the ability to pause at some time during the transmitting or receiving cycle and wait for the receiving device to become ready. Figure 27 depicts this event.

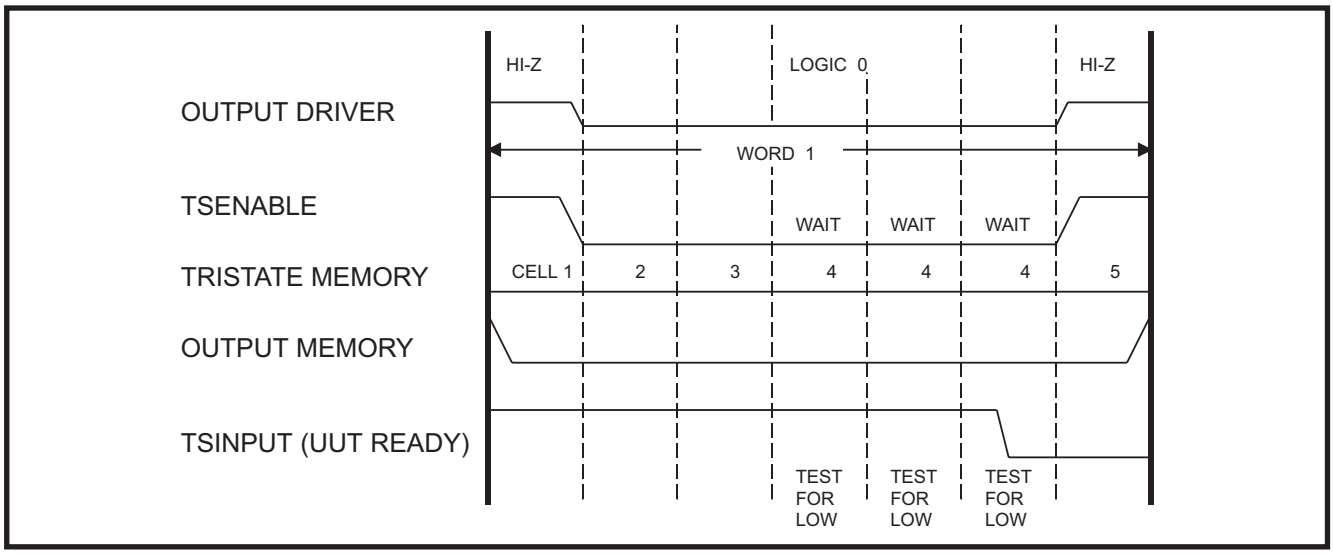


Figure 26 Bus Emulation Handshaking

During the “wait” time, the data and data enable signal must remain in the predefined state until the “handshake” sequence is detected.

The bus emulation architecture allows for the handshake event where as the stimulus/response architecture does not.

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5 DRIVER/RECEIVER SPECIFICATIONS

The table below depicts the specifications for the drivers and receivers respectfully.

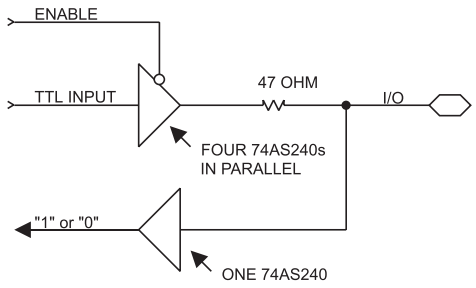
TTL DRIVER / RECEIVERS

Output Specifications

High Level Voltage	2.4V min
High Level Current	50 mA
Low Level Voltage	0.4V max
Low Level Current	50 mA
Output Impedance	50 ohm typ
Rise/Fall Time @ 20%, 80%	0.5V/nS typ
Short Circuit Protected	yes
Skew (Timing Set Signals)	<3 nS
Skew (Field I/O Signals)	<5 nS

Input Specifications

High Input Threshold	2.0V
Low Input Threshold	0.8V
Input Impedance	>50K ohm



1-CHANNEL

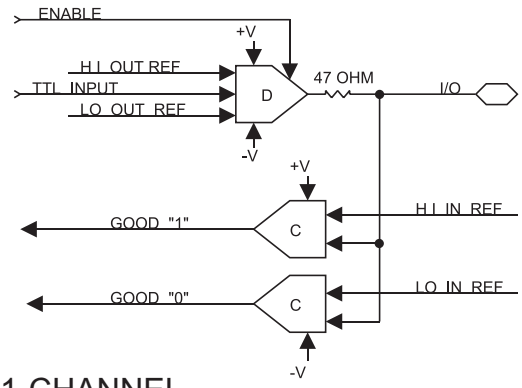
PROGRAMMABLE DRIVER / RECEIVERS

Output Specifications

High Level Voltage	-5V to +15V
High Level Current	50 mA
Low Level Voltage	+5V to -15V
Low Level Current	50 mA
Voltage Swing	20V max.
Output Impedance	50 ohm
Rise/Fall Time @ 20%, 80%	.5V/nsec typ
Short Circuit Protected	yes
Skew (Timing Set Signals)	<6 nS
Skew (Field I/O Signals)	<8 nS

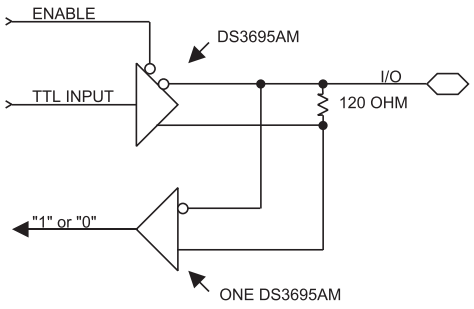
Input Specifications

High Input Threshold	-5V to +15V
Low Input Threshold	+5V to -15V
Input Impedance	>50K



1-CHANNEL

RS485 DIFFERENTIAL DRIVER / RECEIVERS



1-CHANNEL

Output Specifications

High Level Voltage	15V max
High Level Current	25 mA
Low Level Voltage	-10V max
Low Level Current	25 mA
Output Impedance	125 ohm parallel
Rise/Fall Time @ 20%, 80%	< 10 nS
Short Circuit Protected	yes
Skew (Timing Set Signals)	<6 nS
Skew (Field I/O Signals)	<8 nS

Input Specifications

High Input Threshold	15V max
Low Input Threshold	-10V min
Input Impedance	>12K ohm

Table 7 I/O Driver Specifications

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6 PROGRAMMING THE SR192

The SR192 is a message based device. The commands are "SCPI" like in structure. Although the commands follow the SCPI format, there presently is no standard SCPI command set for digital instruments.

The command set consists of eleven basic command types called subsystems, plus SCPI mandated commands, IEEE common commands and low level interface commands. The eleven subsystems are:

1) MODULE
2) ROUTE
3) CHANNEL
4) TIMING
5) TABLE
6) OUTPUT
7) INPUT
8) SEQUENCE
9) EXECUTE
10) CALCULATE
11) STATUS

Appendix B (attached to this document) provides a summary of the SR192 commands. Following are several programming examples. These are for example only. The user manual programming section should be referenced for an accurate command description.

6.1 SR192 Software Programming Tools

There are several software tools available to help program the SR192.

Timing / Table Editor	The Timing / Table Editor is a Microsoft Windows based application that allows the user to graphically create timing sets and tables. Once the timing sets and data tables are created the user can export the SCPI commands required to program the SR192 to a file. The exported file can then be sent to the SR192 via the Slot 0 controller.
LabWindows/CVI Driver	A LabWindows/CVI driver is available at no charge for users who are using National Instruments LabWindows/CVI program for test development.
LabView Driver	A LabView driver is available at no charge for users who are using National Instruments LabView program for test development.
VXI Plug & Play Driver	A WIN Framework Plug & Play driver is available for users at no charge who require Plug & Play compatibility.
Mentor QuickSim Utility	The Mentor QuickSim utility takes simulation files and converts them into Table Editor files that can then be exported and sent to the SR192.

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6.1.1 Stimulus Example

The following SCPI short form commands will generate a continuous 5MHz stimulus pattern on channels one through sixteen and a 10MHz pattern on TSOUT5.

*RST;*CLS	Perform a reset and a clear status IEEE command to initialize the SR192.
MOD:SEL TSA	Select timing module TSA for programming.
ROUT:PATH:DEF OUT,(@1:16)	Create a channel group called “OUT”.
TIM:SET:CLOC 10	Program timing module TSA's TS CLOCK to an internal 10MHz. Every cell will be 100nS.
TIM:DEF STIM,2	Define a two cell timing set called “STIM”. Two cell at 100ns per cell will give us a data rate of 200ns.
TIM:CELL STIM,1,#H7F2	Program SR_CLK, STIM_LOAD, TSENABLE1 and TSOUT5 low in the first cell.
TIM:CELL STIM,2,#HFF7	Program TSENABLE1 low in the second cell.
TABL:DEF DATA,16	Define a 16 transfer table called “DATA”.
TABL:SEL OUTPUT	Select the output memory.
TABL:MEM:WORD DATA,OUT,1,1	Program the first transfer of table “DATA” group “OUT” to a one.
TABL:MEM:FILL DATA,OUT,ROT,1,1	Perform the rotate fill function on table “DATA” file “OUT” starting at the first transfer and rotate once.
TABL:SEL TRIS	Select the tristate memory.
TABL:MEM:FILL DATA,OUT,COMP,1	Perform the compliment fill function on table “DATA” field “OUT” starting at the first transfer.
OUTP:ENAB OUT,TSEN1	Assign the timing module enable TSENABLE1 as the group enable signal for every channel in group “OUT”.
OUTP:CHAN:STAT ON	Turn on the channel output drivers.
OUTP:TIM:STAT ON	Turn on the timing output drivers.
OUTP:REF:SEL VGRP1	Select voltage group one.
OUTP:REF:HIGH 5.0	Program high reference to +5V.
OUTP:REF:LOW 0.0	Program low reference to 0V.
OUTP:REF:UPD	If the OUTP:REF:AUTO is set to OFF then the UPD command must be sent so that the DAC will update the programmed levels.
EXEC:MODE CONT	Set the SR192 timing module into continuous mode.
EXEC:TIM STIM,DATA	Execute timing set “STIM” with table “DATA”

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6.1.2 Response Example

The following SCPI commands will record response data from the stimulus example of the previous section. The device generating the response will set a data ready signal low to indicate that data is valid. The data ready signal will be sampled by the TSINPUT1 signal of the timing module to determine when to strobe the response data.

*RST;*CLS	Perform a reset and a clear status IEEE command to initialize the SR192.
MOD:SEL TSA	Select timing module TSA for programming.
ROUT:PATH:DEF IN,(@17:32)	Create a channel group called “IN”.
TIM:SET:CLOC 10	Program timing module TSA's TS CLOCK to an internal 10MHz. Every cell will be 100nS.
TIM:DEF RESP,4	Define a four cell timing set called “RESP”. Four cells at 100ns per cell will give us a maximum input data rate of 400ns.
TIM:CELL RESP,1,#HFFA	Program SR_CLK and STIM_LOAD low in the first cell.
TIM:TEST:LEV CELL RESP,TSIN1,LOW,2	Test and wait in cell two until TSINPUT1 goes low.
TIM:CELL RESP,3,#HFDF	Program TSSTROBE1 low in the third cell.
TABL:DEF DATA,16	Define a 16 transfer table called “DATA”.
TABL:SEL EXPECT	Select the expect memory.
TABL:MEM:WORD DATA,IN,1,1	Program the first transfer of table “DATA” group “IN” to a one.
TABL:MEM:FILL DATA,IN,ROT,1,1	Perform the rotate fill function on table “DATA” file “IN” starting at the first transfer and rotate once.
TABL:SEL MASK	Select the mask memory.
TABL:MEM:FILL DATA,IN,COMP,1	Perform the compliment fill function on table “DATA” field “IN” starting at the first transfer.
INP:STR IN,TSST1	Assign the timing module strobe TSSTROBE1 as the group strobe signal for every channel in group “IN”.
INP:REF:SEL VGRP1	Select voltage group one.
INP:REF:HIGH 2.4	Program high reference to +2.4V.
INP:REF:LOW 0.8	Program low reference to +0.8V.
INP:REF:UPD	If the INP:REF:AUTO is set to OFF then the UPD command must be sent so that the DAC will update the programmed levels.
EXEC:MODE SING	Set the SR192 timing module into single mode.
EXEC:TIM RESP,DATA	Execute timing set “RESP” with table “DATA”.

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6.1.3 Data Analysis Examples

The following SCPI commands show some of the data analysis features in the SR192. Data can not be analyzed until the execution sequence is complete. Several commands are available to determine if the sequence is complete.

Method 1:	
MOD:SEL TSA	Select timing module TSA.
MOD:STAT?	Read the TSA status. Bits 1 and 2 of the returned data indicates that the timing module is running or idle. Repeat this command until bit 1 is low and bit 2 is high.
Method 2:	
*OPC	Send the operation complete command. This command sets bit 0 of the event status register when the sequence is complete. Repeat the *ESR? command until bit 0 of the response is a 1.
Method 3:	
*OPC?	Send the operation complete query. This command puts a “1" into the output buffer when the sequence is complete. Continue to read from the SR192 until a ”1" is returned.
Method 4:	
*WAI	Send the wait command. This command freezes the SCPI parser until the sequence is complete.

Once the sequence has completed the following commands can be used to analyze the response data.

CALC:EMEM:COUN?	A built in counter counts the number of real time errors that occurred during the previous sequence. A non zero count indicates an error.
CALC:EMEM:ADDR? 1	If an error occurred then the error memory on the IO module recorded the channels that failed. The address at which the channel failed is also recorded. This command will return the absolute FMA of the first error.
CALC:CRC? RESP,IN,0,#HFFFF	Generate a 32 bit CRC polynomial on the response memory of table “RESP” group “IN” using zero as the seed and hex FFFF as a mask. Compare against known CRC.
TABL:SEL ERR	Select the error memory.
TABL:MEM:WORD? RESP,IN,1	Read the first word of table “RESP” group “IN”. A non zero response indicates an error on that channel. Repeat for every word.

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7 FEATURE SUMMARY

7.1 I/O Channel Parameters

- 192 TTL I/O Channels configured in groups of 8. These 192 channels consist of 96 channels linked to timing set A and 96 channels linked to timing set B.
- 96 +/- 15 volt programmable I/O channels configured in groups of 8. These 96 channels consist of 48 channels linked to timing set #1 and 48 channels linked to timing set #2.
- 96 RS485 differential I/O channels configured in groups of 8. These 96 channels consist of 48 channels linked to timing set #1 and 48 channels linked to timing set #2.
- The TTL, +/- 15 volt and differential I/O channels can be mixed in a single SR192 unit.

7.1.1 I/O Channel Memory Depth

- 128K per channel.

7.1.2 I/O Channel Speed

- 50MHz at +/- 5 volt programmable and TTL levels in multiplex mode.
- 25MHz at +/- 5 volt programmable and TTL levels.
- 12.5 MHz at +/- 15 volt programmable I/O levels

7.1.3 Five Memories Per Channel

- OUTPUT stimulus memory
- TRISTATE enable memory
- EXPECT response memory
- MASK response memory
- RECORD response memory

7.1.4 Error Address Memory

- 128K memory records the address of each stimulus/response transaction which resulted in an error.

7.1.5 Error Counter

- An 18 bit counter counts the number of errors which occurred within the total stimulus/response transactions.

7.1.6 Real Time Compare Modes

- Halt on Response Error.
- Wait for Response Compare.

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7.2 Timing Set A Parameters

- # of Timing Sets = 64
- 128 cells per signal per timing set SR100, 256 cells SR101. Minimum timing set = 2 cells.
- 50 MHz clock maximum. Clock selected from 50 MHz, 20 MHz, 10 MHz or an external clock.

7.2.1 13 Timing Set output signals (signals are TTL unless specified)

- 1 Output clock defined by the clock selected to drive the timing set. This clock incorporates a +/- 15 volt programmable driver.
- 1 Signal to increment sequence logic.
- 1 Signal to clock I/O channel output register.
- 1 Signal to clock input compare delay logic.
- 2 Signals for selection to enable output channels 1 - 96.
- 2 Signals for selection to strobe output or input compare logic, channels 1 - 96.
- 5 User defined output signals. 2 Signals incorporate +/- 15 volt programmable drivers. 3 signals are TTL drivers.

7.2.2 5 Timing Set Input Signals

- 1 External clock. This clock incorporates a +/- 15 volt programmable threshold receiver.
- 1 External input, test for high or low.
- 1 External input, test for high, low, positive transition or negative transition. This input incorporates a +/- 15 volt programmable threshold receiver.
- 1 Internal input, test for input channel compare equal true after input sample pulse.
- 1 Internal input, test for “raw” input channel compare before input sample pulse.

7.2.3 Programmable Delay

- Each timing set cell can be set to a programmable delay. Delay is from 1 to 128 clocks for the SR100 timing module and 1 to 32K for the SR101.

7.2.4 Timeout

- For each test cell which waits for an external event to occur, a timeout value may be set from 1 to 128 clocks for the SR100 timing module and from 1 to 32K for the SR101. The timeout will cause the timing set to advance to the next cell, as well as set a timeout register.

7.3 Timing Set B Parameters

- # of Timing Sets = 64
- 128 cells per signal per timing set in the SR100 and 256 cells per timing set in the SR101. Minimum timing set = 2 cells.
- 50 MHz clock maximum. Clock selected from 50 MHz, 20 MHz, 10 MHz or an external clock.

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7.3.1 13 Timing Set output signals (signals are TTL)

- 1 Output clock defined by the clock selected to drive the timing set.
- 1 Signal to increment sequence logic.
- 1 Signal to clock I/O channel output register.
- 1 Signal to clock input compare delay logic.
- 2 Signals for selection to enable output channels 97 - 192.
- 2 Signals for selection to strobe output or input compare logic, channels 97 - 192.
- 5 User defined output signals.

7.3.2 5 Timing Set Input Signals

- 1 External clock.
- 1 External input, test for high or low.
- 1 External input, test for high, low, positive transition or negative transition.
- 1 Internal input, test for input channel compare equal true after input sample pulse.
- 1 Internal input, test for "raw" input channel compare before input sample pulse.

7.3.3 Programmable Delay

Each timing set cell can be set to a programmable delay. Delay is from 1 to 128 clocks for the SR100 timing module and 1 to 32K for the SR101.

7.3.4 Timeout

- For each test cell which waits for an external event to occur, a timeout value may be set from 1 to 128 clocks for the SR100 timing module and from 1 to 32K for the SR101. The timeout will cause the timing set to advance to the next cell, as well as set a timeout register.

7.4 SR100 Sequence Features

- 4 Subsequences
- Sequence Loop 1-64K, continuous.

7.5 SR101 Sequence Features

- Sequence Loop 1-32K, continuous.
- Subsequence loop 32K.
- Conditional subsequence jump and subroutine branching.
- Unconditional subsequence jump and subroutine branching.

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7.6 External I/O Channel Control Signals

- Two external control signals used for input/output strobes and/or I/O enable channel function. These signals may be selected by channels 1 - 96 or channels 97 - 192.
- 1 External control signal incorporates a programmable +/- 15 volt input threshold receiver.
- 1 external control signal is TTL.

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