Operating Electronics
for Spectral Sensors
and Linear Image Arrays

PC/AT-ISA Interface Electronics
PD-ISA16V3

Technical Documentation

Board: **PD-ISA16V3-2 (06010.35 / 06010.36)**
PLD: **tim.602 / tim.507 / adrisav3**
Document: **Part ‚I', Version 3.21_E, 09.11.00 18:24**

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I. PC/AT-ISA Interface Electronics PD-ISA16V3

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I.1 General

The PC/AT Interface Electronics type PD-ISA16V3 is part of the PC/AT Operating Electronics for Spectral Sensors or MOS Linear Image Sensors.

Functionally, it allows the PC to control the Front End Electronics, to which the currently used Spectral Sensor is connected. The analog video signal originating from the sensor is digitized in the Front End Electronics and buffered in a FIFO - memory located on the Interface Board.

A clock control unit is integrated on the Interface Board, allowing autonomous control of various read-out cycles. To acquire a spectrum, the PC only has to select the appropriate read-out cycle, to set its parameters and to initiate it. With each read-out cycle completed, a scan counter located on the Interface Board is incremented. During acquisition of spectral data, the PC is free for additional tasks. At any time, it may either read the scan counter or get information on the status of spectral data acquisition by reading the filling grade of the FIFO memory.

I.2 Construction and Interfaces

The PC/AT Interface Electronics is designed as a plug-in board for the 16 bit AT (ISA) bus and is 100 mm x 160 mm in size.

There are two connectors on the backplate of the plug-in board: one 25-pin and one 9-pin Sub D connector. The 25-pin connector serves as an interconnection for the front-end electronics. The signals available on the 9-pin connector allow for additional functionality, such as computer-controlled flashlamp triggering or synchronization of the read-out procedure to the process (e. g. a chopper wheel).

As an alternative to the 25-pin cable interconnection to the Frontend Electronics, the Frontend board may be directly plugged onto the PC Interface Board. The electrical connection is provided by an array of socket connectors, arranged in parallel to ST2. Two holes are provided near the center of the PC Interface Board for mechanically fixing the arrangement.

I.3 Circuit Description

The PC-Interface Electronics circuitry can be roughly classified in five functional groups (circuit diagrams are contained in the appendix):

- 16 bit ISA bus interface (Diagram 1/6)
- Control and status ports, lighting control (Diagram 2/6)
- FIFO - buffer memory (Diagram 3/6)
- PDA (Photo-Diode-Array) readout clock control unit scan cycle control (Diagram 4/6)
- Timer / counter (Diagram 5/6)

Circuit diagram 6 shows the pinouts of the ISA bus connector, of the socket connector for the Frontend Electronics and of the service connector.

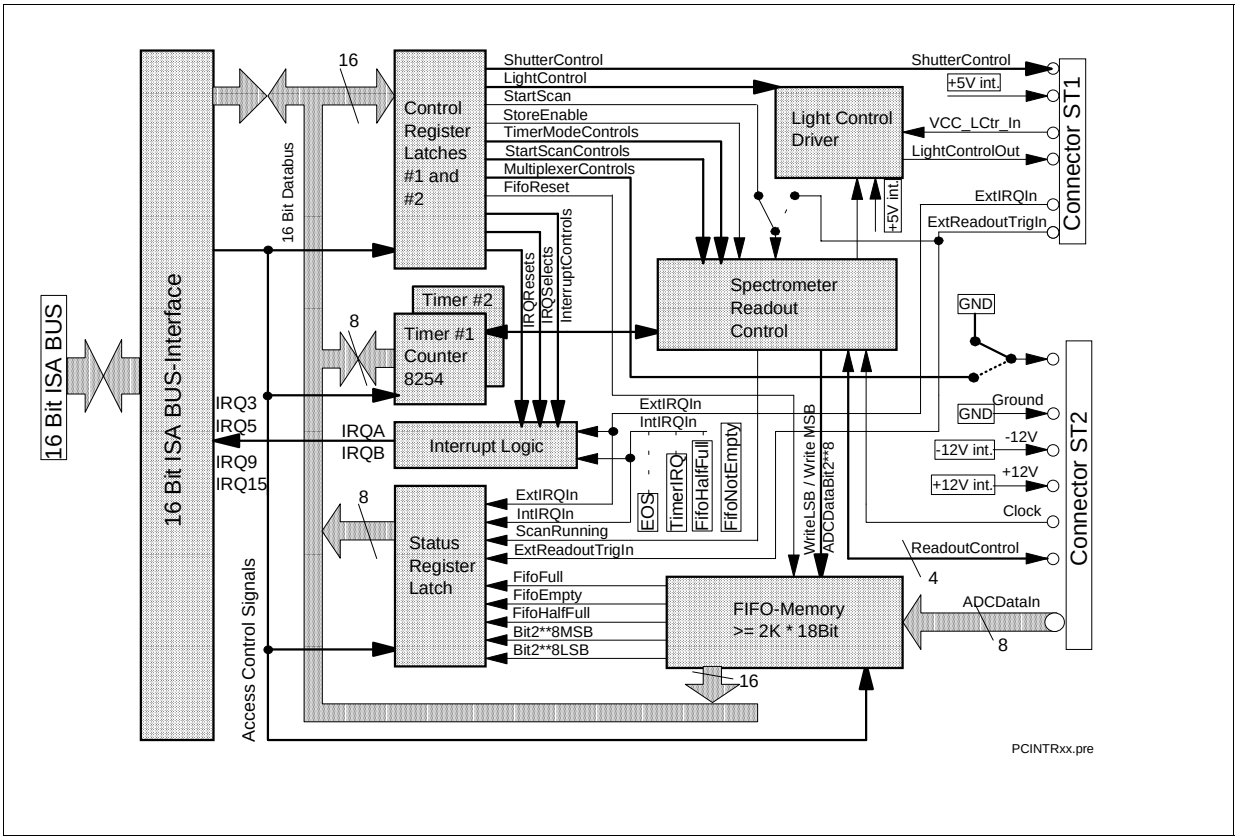


Fig. I 1: Block diagram of the PC Interface Electronics

I.3.1 16 bit ISA Bus Interface

The 16 bit ISA bus interface supports I/O read- and write access with 16 and 8 bit words with standard count or without wait cycles. The interrupt request signals produced by the plug-in board can be jumpered to use the IRQ3, IRQ5, IRQ9 or IRQ15 PC-signals.

The PC/AT Interface Board uses a block of 16 consecutive I/O addresses, starting from the base address. The base address can be set in steps of 16 within the PC I/O address range.

IC 1 compares the I/O base address set by the DIP switch array (address bits A4 .. A9) to the bus address bits SA4 .. SA9. Equality activates the address decoder GAL 'ADRISAV3', which performs access decoding, also considering the signals SA0 .. SA3, IOR#, IOW# and BHE#. After activating the data bus drivers (via the signals BEL and BEH), this GAL commands the selected component (chip-select for timers 1 and 2: signals TIMER1# and TIMER2# or read/write pulse for the status register (signal R-STS-C#), the control registers 1 and 2 (signals W-CTL-C1 and W-CTL-C2) or FIFO memory (signal R-FIFO-C), respectively).

The following table shows the possible data transfers between the PC and the components of the PC/AT Interface Board (overview):

I/O - address	data word length	transfer direction	component addressed
Base + 00_{HEX}	16 bit	write	control register #1
Base + 00_{HEX}	16 bit	read	status register
Base + 02_{HEX}	16 bit	write	control register #2
Base + 02_{HEX}	16 bit	read	FIFO - data word
Base + 04_{HEX}	8 bit	write/read	timer #1 timer 0
Base + 05_{HEX}	8 bit	write/read	timer #1 timer 1
Base + 06_{HEX}	8 bit	write/read	timer #1 timer 2
Base + 07_{HEX}	8 bit	write	timer #1 control port
Base + 08_{HEX}	16 bit	write/read	reserved
Base + $0A_{HEX}$	16 bit	write/read	reserved
Base + $0C_{HEX}$	8 bit	write/read	timer #2 timer 0
Base + $0D_{HEX}$	8 bit	write/read	timer #2 timer 1
Base + $0E_{HEX}$	8 bit	write/read	timer #2 timer 2
Base + $0F_{HEX}$	8 bit	write	timer #2 control port

If jumper J3 is set, the PC Interface Board activates the signal 0WS# (zero wait states) with each access. This shortens I/O access times, since the standard waits during a CPU cycle are omitted (16 bit access: 2 instead of 3 bus cycles, 8 bit access: 3 instead of 6 bus cycles).

I.3.2 Control Ports and Status Port

The Interface Electronics contains two control ports and one status port. The control ports enable the PC to control all actions within the Operating Electronics. All return signals may be read by the PC via the status port.

port	word length / used word length	ICs
control port #1	16 bit / D0 ... D15	LSB: IC 3 / MSB: IC14
control port #2	16 bit / D0 ... D7	LSB: IC 29
status port	16 bit / D0 ... D 15	LSB: IC 6 / MSB: IC 28

Signal assignment for control port #1:

data bit	signal designation	comment
D0	STOR_E1#	store enable 1, enables data storage
D1	FIFO_R#	FIFO reset, erases FIFO memory
D2	STSCAN1#	start scan 1, rising edge activates a scan cycle
D3	IRQ-R-C#	internal IRQ reset clock, clears internal IRQ
D4	EXTIR-C#	external IRQ reset clock, clears external IRQ
D5	BLZ-SW	software flash trigger, trigger signal for lighting control, directly influences external lighting control signal LIGHTOUT
D6	INTSEL0	interrupt select 0 and
D7	INTSEL1	interrupt select 1 select the interrupt source
D8	TIMSELM0	timer select 0 and
D9	TIMSELM1	timer select 1 select timer operating mode
D10	STS-SEL0	start scan select 0 and
D11	STS-SEL1	start scan select 1 determine the signal source for starting a scan cycle
D12	BLZ-HW-E	hardware flash trigger, enables the scan-synchronous activation of the external lighting control signal LIGHTOUT under hardware control
D13	BO_SEL2	board select 2, control signal routed exclusively to the status port for monitoring and test purposes (test base address setting or function of the bus interface), see also signals BO-SEL0 and BO-SEL1 in control port #2
D14	IRQ-SEL0	interrupt request select 0 and
D15	IRQ-SEL1	interrupt request select 1 for selection of the source signal for the internal interrupt request

Signal assignment for control port #2:

data bit	**signal designation**	**comment**
D0	FEESEL0#	Frontend Electronics select 0 and
D1	FEESEL1#	Frontend Electronics select 1, multiplexer control signals
D2	ZEIL_RES	array reset, reset signal for detector array or Multiplexer mode of operation
D3	SHUT-EA	shutter on/off, shutter control signal
D4	SHUT-R	shutter direction, shutter control signal
D5	STSC_R_C	test-start-scan reset clock, clears filp-flop
D6	BO-SEL0	board select 0 and
D7	BO-SEL1	board select 1, control signal routed exclusively to the status port for monitoring and test purposes (test base address setting or function of the bus interface), see also signal BO-SEL2
D8 .. D15	reserved	reserved

Remark: When switching on or resetting the PC, all control signals of both control ports are reset to logical 0.

Signal assignment for the status port:

data bit	signal designation	comment
D0	IRQIN1	internal interrupt request
D1	EXTIRQIN	external interrupt request
D2	FULL#	FIFO full, FIFO memory full
D3	EMPTY#	FIFO empty, FIFO memory empty
D4	SCANRUN	scan running, readout of the array active
D5	STSCAN8	start scan 8, external scan trigger signal
D6	BIT9-LSB	FIFO memory bit 2**8 of low Byte
D7	BIT9-MSB	FIFO memory bit 2**8 of high Byte
D8	BO-SEL0	board select 0 and
D9	BO-SEL1	board select 1 and
D10	BO-SEL2	board select 2 for test and monitoring of the bus interface
D11	HALF#	FIFO half, FIFO memory half full
D12	BUSY	Frontend ADC busy (for test operation without FEE)
D13	STS_SC_F	Frontend start scan, stored (for test operation without FEE)
D14	EX-IRQ-I	external interrupt request input, original signal from ST1 pin 1 unbuffered
D15	reserved	reserved

I.3.3 Lighting Control

The PC Interface Board provides two signals at connector ST1 (lighting control voltage input VCC_BLZ and control output LIGHTOUT), allowing to activate a lighting source (e. g. a flashlamp). The voltage swing of LIGHTOUT amounts to +5V or VCC_BLZ, depending on the setting of jumper 4. Lighting control is possible in one of three modes of operation:

mode of operation	settings required	comment
PC software controlled, digital output	jumper 5 in position 1	polarity determined by software
PC software controlled, pulse output	control signal BLZ-HW-E inactive (logic 0), jumper 5 in position 2 or position 3	jumper 5 sets polarity R1 and C10 set pulse width, the pulse is triggered by the rising edge of the control signal BLZ-SW
hardware controlled, pulse output	control signals BLZ-HW-E active (logic 1) and BLZ-SW inactive (logic 0), jumper 5 in position 2 or position 3	jumper 5 sets polarity, R1 and C10 set pulse width, before each data scan, a scan-synchronous trigger pulse is generated by the hardware (in PLD TIM_5x) before each data scan. The trigger pulse is concurrent with the start moment of the previous integration period.

The pulse width is fixed to 100 µs by external components connected to IC12A.

I.3.4 FIFO Buffer Memory

The buffer memory consists of two word length cascaded, asynchronous FIFO memory chips (type SN74ACT720x, x designates the storage capacity of the component [2:1K*9 / 3:2K*9 / 4:4K*9 / 5:8K*9] or type IDT720x, x designates the storage capacity of the component [3:2K*9 / 4:4K*9 / 5:8K*9 / 6:16K*9]).

The PC/AT Interface Electronics PD-ISA16V3 in standard version is equipped with 2 chips type SN74ACT7203 or IDT7203 (organization 2 KByte * 9, IC7 and IC8) in plug-in sockets. For larger memory capacity, the 2 kByte - IC's may be replaced by equivalent types, which are compatible in pin assignment and functionality, offering larger memory sizes (currently available for up to 16 kBytes).

The three status signals 'Full#', 'Half#' and 'Empty#' as well as bits 2**8 of the LSB and the MSB - FIFO have been routed to the status port. The status 'Full', 'Half' or 'Empty' is only derived from the flags of the LSB - FIFO. Memory chips of the type SN74ACT720x do not provide a 'Half' flag.

I.3.5 PDA Readout Clock Control Unit

The GAL IC's 'tim_5x' and 'tim_6x' constitute the photo diode array (PDA) readout clock control unit. Important input signals of this unit are:

- o STSCAN2# initiates a readout scan or readout cycle of the PDA.
  The mode of operation of the timer (Software, TimerSingle, Timer Continuous) is determined by the scan cycle clocking.
  The trigger mode of operation selects internal or external trigger.
  The readout clock control unit generates one or several START_F# - pulses for the Frontend, depending on the timer mode of operation.
- o EOS_F# is the return signal from the Frontend Electronics. It terminates the current scan (each START_F# - pulse is followed-up by an EOS_F# - pulse).
- o STORE-E1# in the timer mode of operation "software", Store Enable 1determines whether the values obtained by the next scan shall be stored in the FIFO memory. In both remaining timer modes of operation, the scan cycle clocking automatically controls FIFO operation.
  Store disabled: reset procedure for the PDA,
  charges are dumped, if present.
  Store enabled: read-out procedure
- o BUSY_F ADC on the FEE converting (from FEE, some 64 kHz)
- o CLK_F FEE clock (some 1 MHz)

In the course of one Scan, the PDA readout clock control unit generates the following control signals:

- o SCANRUN status signal Scan Running indicates, that a read-out process is performed currently (active from Start-Scan to End-of-Scan).
- o BYTE_F control signal Byte-Select for ADC on the FEE:
  High: ADC on the FEE writes the high-Byte (D8..D15) of the last conversion result to ADC_D0 through ADC_D7
  Low: ADC on the FEE writes the low-Byte (D0..D7) of the last conversion result to ADC_D0 through ADC_D7
- o WCLK-LB write clock for buffer memory, writes the LSB to the FIFO
- o WCLK-HB write clock for buffer memory, writes the MSB to the FIFO
- o 1PIXEL#1 status signal, indicates the time slot for sampling the signal from the first photodiode in a scan by a logic low level

I.3.6 Scan Cycle Clocking, Timer

The term scan cycle stands for a single reset procedure for the charges on the photodiode array (read-out procedure without data storage) and one or more read-out procedures with spectral data storage, sequenced with a delay of one integration period each time.

Scan cycle clocking can be set to one of three modes of operation by the PC via the two control signals TIMSELM0 and TIMSELM1 (Mode 0, 2 or 3):

Mode of Operation 'Software' (Timer Mode 0):

TIMSELM0 = Low
TIMSELM1 = Low

The PC takes full control of array read-out, scan cycle control by hardware is disactivated, the PC also performs integration timing.

In this mode of operation, the PC first initiates a read-out procedure by a pulse on signal STSCAN1# (Start Scan, triggered at the rising edge) without setting signal STOR-E1# (Store Enable) and waits for the Interface Board to finish the scan. This step resets the charges on the photodiode array. Afterwards, the PC has to wait for one integration period (or, more exactly: integration period - scan time) before starting a spectral data read-out procedure again by a pulse on signal STSCAN1#, this time the signal STOR-E1# is activated. The measurement data can be transferred to the PC either (a) during the read-out procedure for measurement data or (b) after finishing the scan. In case (a), the Interface Electronics indicates available measurement data by means of status flags generated by the FIFO memory. In case (b), the scan has to be finished (as in a reset procedure) before the measurement data can be transferred to the PC.

Reserved Mode of Operation (Timer Mode 1):

TIMSELM0 = High
TIMSELM1 = Low

Mode of Operation 'TimerSingle' (Timer Mode 2):

TIMSELM0 = Low
TIMSELM1 = High

The scanning cycle is controlled autonomously by the PC Interface Board, timed by the timers 1 and 2 of the timer / counter IC #1.

The only task for the PC is to program the timer circuit for the selected integration time in multiples of 1/10 ms and, afterwards, to initiate the scan cycle by means of a pulse on signal STSCAN1# (triggered at the rising edge). The scan cycle clocking will then first perform a reset procedure. Then, after the programmed integration time has passed, the read-out procedure for measurement data is executed.

The PC can detect the end of a scan cycle by polling the signal SCANRUN (scan running) or reading the scan counter (see below). Data may be read out from the FIFO buffer memory and processed already during the scan cycle.

Mode of Operation 'TimerContinuous' (Timer Mode 3):

TIMSELM0 = High
TIMSELM1 = High

The scan cycle is controlled autonomously by the PC Interface Board.

The behavior in the mode of operation 'TimerContinuous' resembles the mode of operation 'TimerSingle'. The difference is that a scan cycle is not finished after the read-out procedure for measurement data, here, integration period and data read-out procedure are repeated until stopped by the PC (by resetting the mode of operation to mode 0).

As in the mode of operation 'TimerSingle', the PC can determine the correct moment for stopping the cycle by polling the signal SCANRUN (scan running) or reading the scan counter (see below). Data may be read out from the FIFO buffer memory and processed already during the scan cycle.

Scan Counter

Timer 0 of the timer/counter IC #1, which is not used by integration timing, is prepared for use as a scan counter. To this end, GATE_0 is connected to V_{CC} and CLK_0 is connected to the signal EOS.

I.3.7 Interrupts

The interrupt logic of the PC Interface Board offers two separate interrupt paths:
'external interrupt request' and 'internal interrupt request'.

External Interrupt Request

Its signal source is the TTL input signal EX_IRQ_I of ST1, pin 1. A rising edge of EX_IRQ_I sets the flip-flop circuit dedicated to external interrupt request (IC4A) and activates the on-board signal EXTIRQIN. The control signal 'INTSEL1' allows to mask the external interrupt request or to forward it as IRQB. Depending on the connection made to jumper array 1, the request signal IRQB is then passed to IRQ3, IRQ5, IRQ9 or IRQ15 of the PC.

The flip-flop circuit for external interrupt request (IC4A) can be reset via the control word register by means of a pulse (active low) in signal EXTIR-C#.

The signal EXTIRQIN internal to the board is also routed to the status port to allow for polling

Internal Interrupt Request

Four different events are available as an interrupt source. The control signals IRQ-SEL-0 and IRQ-SEL-1 allow to select one of these events by software as an on-board interrupt request (signal IRQIN1).

mode	IRQ-SEL-1	IRQ-SEL-0	signal source	comment
0	Low	Low	TIM-IRQ via IC4B as EOS/TIM#	output timer-IC #2 / timer 2, application-specific function
1	Low	High	HALF	FIFO memory half full (only FIFO IDT720x)
2	High	Low	EMPTY#	FIFO memory not empty
3	High	High	EOS# via IC4B as EOS/TIM#	End of Scan, read-out of detector array completed

The events TIM-IRQ and EOS# (pulses active low) are buffered in the flip-flop circuit for internal interrupt request (IC4B) (falling edge activates EOS/TIM#). The request can be reset via the control word register by a pulse (active low) in signal IRQ-R-C#. 'FIFO not empty' and 'FIFO half full' are directly derived from the corresponding flag signals of the FIFO memory circuits. These requests can be reset by reading FIFO memory only.

The control signal 'INTSEL0' allows to mask the internal interrupt request or to forward it as IRQA. Depending on the connection made to jumper array 1, the request signal IRQB is then passed to IRQ3, IRQ5, IRQ9 or IRQ15 of the PC.

Interrupt Select via GAL 'ADRISAV3'

The table below shows the effect of the status of the interrupt select control lines on the request signals IRQA and IRQB:

INTSEL1	INTSEL0	IRQA	IRQB
Low	Low	inactive	inactive
Low	High	IRQIN1	inactive
High	Low	inactive	EXTIRQIN
High	High	IRQIN1	EXTIRQIN

I.3.8 Internal and External Scan Cycle Triggering / Chopper Operation

A scan cycle may be triggered under PC-control (internally) or via external control signals. The control signals STS-SEL0 and STS-SEL1 select one of three scan cycle trigger procedures, which are explained in the following.

For all (three) modes:

- In timer mode of operation 'Software' (timer mode 0), each trigger directly initiates a scan of the detector array (no matter if PC-controlled or external pulse- or edge triggered).

- In timer modes of operation 'TimerSingle' or 'TimerContinuous' each trigger starts a scan cycle.
  In timer mode of operation 'TimerSingle', a scan cycle consists of a dummy scan, the wait for the integration time and the data scan. In timer mode of operation 'TimerContinuous', a scan cycle consists of a dummy scan with continuously repeated waits for the integration time and data scans.

Computer Controlled Scan Cycle Triggering (Internal, Trigger Mode 0):

STS-SEL0 = Low
STS-SEL1 = Low

Each scan cycle must be initiated by the PC by the output of a start scan pulse via control signal STSCAN1# (standard procedure). In this mode of operation, the scan may be synchronized to external events indirectly by polling an external status signal via one of the digital inputs and by initiating the scan cycle from the program.

External Scan Cycle Triggering via Pulse (Trigger Mode 1):

STS-SEL0 = High
STS-SEL1 = Low

A scan cycle is triggered by hardware at each rising edge of the external signal EXT_SCANTRIG_IMP (STSCA7#, pulse input, active low). Its repetition period must be selected longer than the integration time currently set + scan time to be sure not to start a new scan cycle before the previous cycle is completed.

External Scan Cycle Triggering via Edge (Chopper, Trigger Mode 2):

STS-SEL0 = Low
STS-SEL1 = High

Each edge of the external signal EXT_SCANTRIG_FLANKE (STSCAN8#) triggers a scan cycle by hardware (IC10 and GAL TIM_6x are used for synchronization and pulse shaping of the signal CHOPP#). The time between two edges must be selected longer than the integration time set currently + scan time to be sure not to start a new scan cycle before the previous cycle is completed.

In this mode of operation it is possible, for example, to use the sync output signal of a chopper wheel directly as external scan trigger signal. At each level transition, a scan cycle is started and, in this way, dark current and measurement spectrum are acquired alternately in a continuous sequence. The

external scan trigger signal STSCAN8# is also routed to the status port on the PC Interface Board, allowing e. g. to monitor the chopper rate with the PC. Furthermore, the PC - Interface Electronics offers the possibility to determine whether a full scan cycle could be performed in chopper mode in the corresponding phase (illuminated or darkened). To this end, the scan trigger signal STSCAN8# (position 2-3) must be forwarded to bit 2**8 of the MSB - FIFO by means of the solder bridge BR5 instead of the identification signal for the first pixel (position 1-2). In this case, the additional information can be collected by the PC from the status port for each array pixel in parallel to reading out the spectral data from the FIFO memory.

Reserved (Trigger Mode 3):

STS-SEL0 = High
STS-SEL1 = High

I.3.9 Test Mode Simulated Frontend Electronics

Starting from version 3 of the PC Interface Board, the board's functions may be tested without a Frontend connected to it.

To simulate a scan procedure, the following steps have to be made:

- connect all positions (1...4) in jumper array J6
- program the timer IC #2 / timer 0
  for f_{OUT} = 1 MHz with a duty factor 1:1 (division ratio 4:1)
  for simulation of the clock signal CLK_F of the Frontend Electronics
- program the timer IC #2 / timer 1
  for f_{OUT} = 62,5 kHz with a duty factor 1:1 (division ratio 16:1)
  for simulation of the signal BUSY_F of the Frontend Electronics
- reset the flip-flop circuit IC18B (test start scan) (pulse in signal STSC_R_C)
- generate a start scan
- poll the BUSY signal and count n pixel cycles (e. g. n=256 for 256 pixel array)
- simulate an End Of Scan via the control signal SHUT_EA / EOS_SIM#

Then, for example, the checks that may be performed are:

- whether the correct number of n values was stored in the FIFO memory
- whether the End-of-Scan counter was incremented and
- whether the StartScan signal START_F# was present on connector ST2 (by reading the status of the flip-flop circuit 'Test Start Scan' via status signal STS_SC_F).

I.4 Arrangement of Components

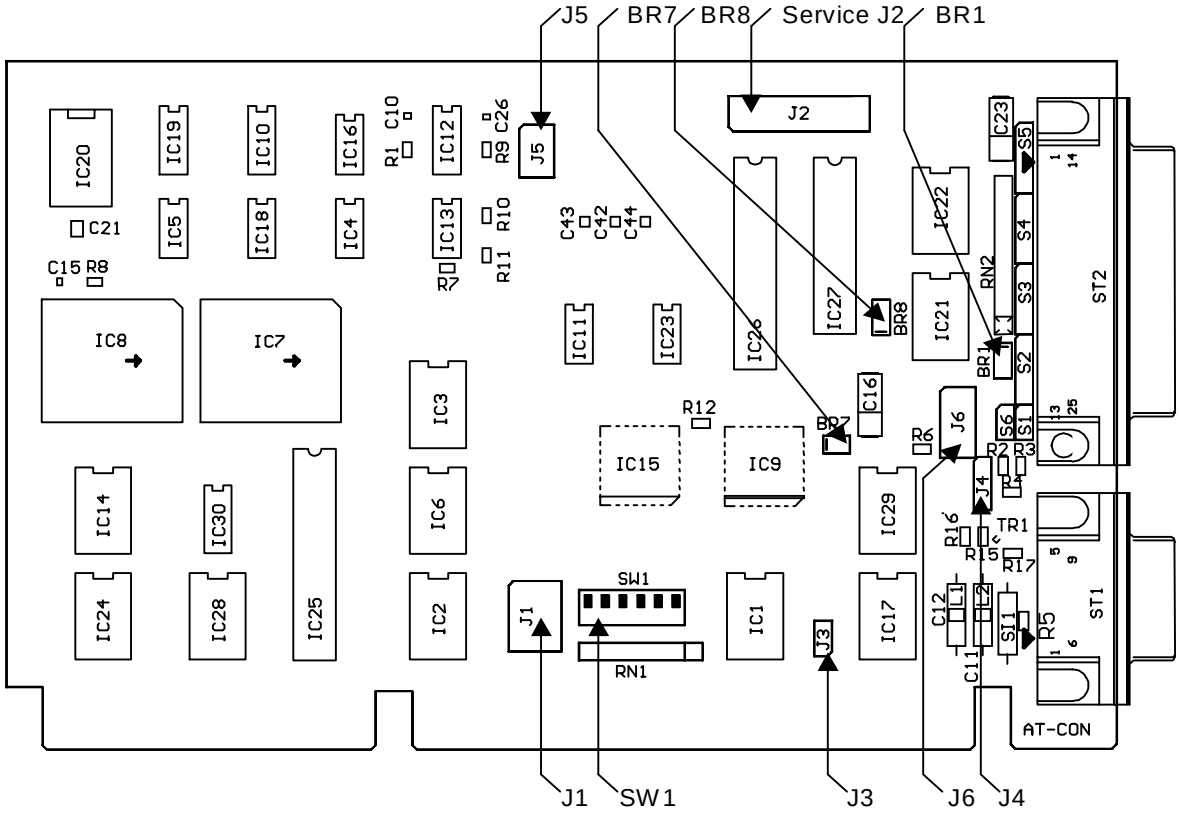


Fig. I 2: View of the PC/AT Interface Electronics, component side

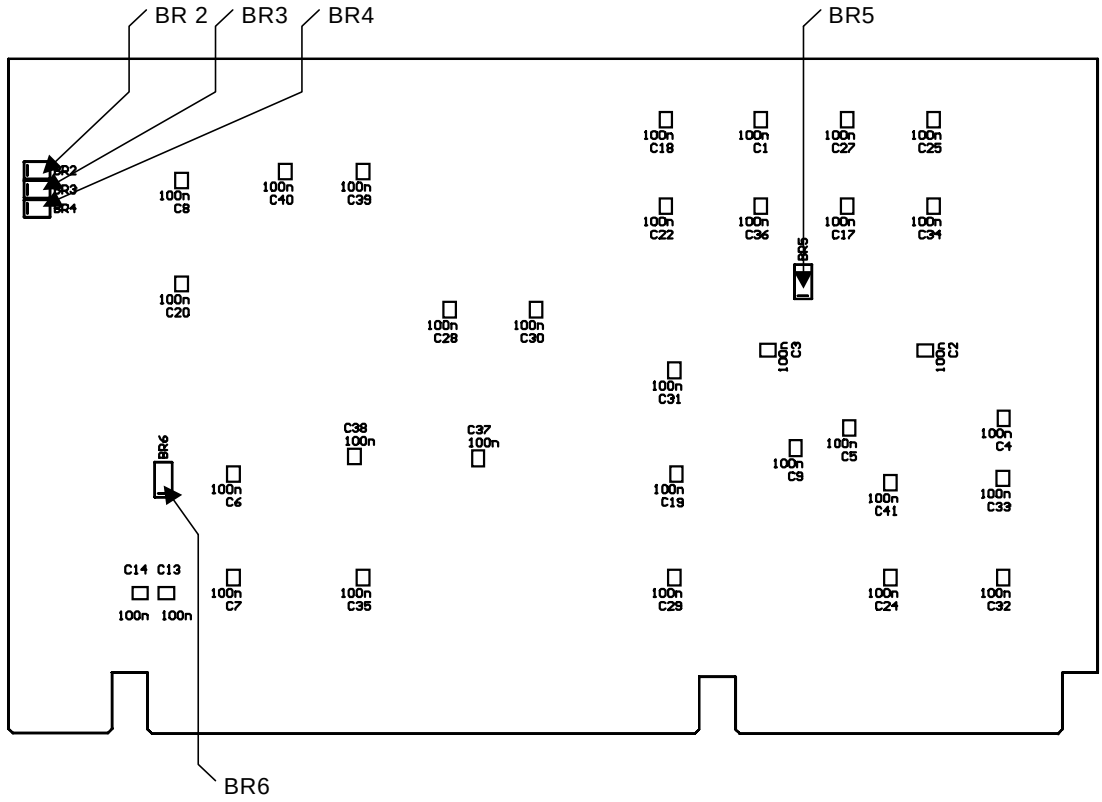


Fig. I 3: View PC/AT Interface Electronics, solder side

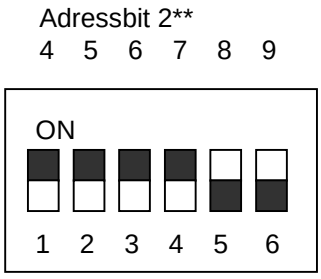
I.5 Board Settings

I.5.1 I/O Base Address (Dip Switch Block SW1)

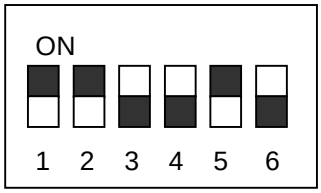
The I/O base address of the plug-in board is set by switches 1...6 of the DIP switch block SW1
(ON corresponds to Low).

Default setting: address 300 Hex

switch 1 : address bit 2**4
on to
switch 6 : address bit 2**9



Address 300H



Example:
Address 2C0H

Table of I/O base adresses supported by the demonstration software:

Adresse	S1	S2	S3	S4	S5	S6
200H	on	on	on	on	on	off
240H	on	on	off	on	on	off
280H	on	on	on	off	on	off
2C0H	on	on	off	off	on	off
300H	on	on	on	on	off	off
310H	off	on	on	on	off	off
320H	on	off	on	on	off	off
330H	off	off	on	on	off	off

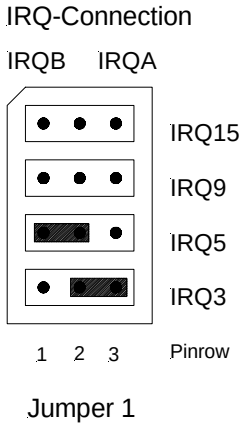
I.5.2 Connecting On-Board, internal IRQs to PC IRQs (Jumper 1)

Jumper 1 may be used to assign the two interrupt output signals of the Interface Board IRQA and IRQB to the interrupt request channels IRQ3, IRQ5, IRQ9 or IRQ15 of the PC.

IRQA is connected to all pins #3, IRQB is connected to all pins #1. The PC's IRQs are each routed to pin 2 of the corresponding row. Caution: It is not allowed to connect both interrupt output signals to the same interrupt request channel of the PC.

Assignment:

Connection IRQA with IRQ15	jumper 'IRQ15'	pin 2-3
Connection IRQA with IRQ9	jumper 'IRQ9'	pin 2-3
Connection IRQA with IRQ5	jumper 'IRQ5'	pin 2-3
Connection IRQA with IRQ3	jumper 'IRQ3'	pin 2-3
Connection IRQB with IRQ15	jumper 'IRQ15'	pin 1-2
Connection IRQB with IRQ9	jumper 'IRQ9'	pin 1-2
Connection IRQB with IRQ5	jumper 'IRQ5'	pin 1-2
Connection IRQB with IRQ3	jumper 'IRQ3'	pin 1-2



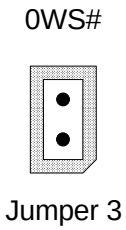
Jumper 1

Factory default setting: no connections
Example: the marked jumper positions connect IRQA to IRQ3 and IRQB to IRQ5.
Remark: the digits '1' and '3' on the circuit board designate the pin rows 1 and 3 (but not pins 1 and 3)!

I.5.3 Wait States (Jumper 3)

With jumper J3 closed, the PC Interface Board activates the signal 0WS# at each access.

The activation of the signal 0WS# (zero wait states) shortens memory or I/O access times by omitting waits normally inserted to the CPU cycles.
(16 bit access in 2 instead of 3, 8 bit access in 3 instead of 6 bus cycles).



Jumper 3

Assignment:

shortened CPU access cycles	J3 jumpered
standard CPU access cycles	J3 open

Factory default setting: J3 open (standard CPU access cycles)

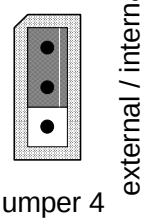
I.5.4 Flash Control (Jumper 4 and 5)

The PC Interface Board offers one output for controlling a lighting source (e. g. a flashlamp) synchronously with the read-out procedure of the array, PC or hardware controlled modes are available

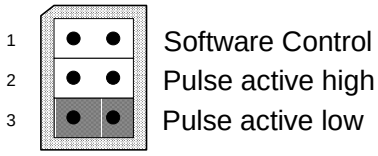
The jumpers 4 and 5 are used to set the voltage source (+5V internal or external source) and the signal's polarity (see also section 'Lighting Control').

Remark: The digit '1' on the circuit board designates position 1 (not pin 1)!

Factory default setting: internal voltage source (+5V), pulse active low



Jumper 4



Jumper 5

I.5.5 Test Mode Simulated Frontend Electronics (Jumper 6)

Closing all jumpers of the jumper array J6 puts the PC Interface Board into a test mode of operation, which allows operation of the board without a Frontend Electronics connected (simulation of the Frontend operation).

For normal operation, all jumper in jumper array 6 have to be removed.

Factory default setting: no connections

I.5.6 Solder Bridges (BR1 to BR8)

BR1:	position 1-2: ST2/pin22 = ZEIL_RES or TIM_IRQ (see BR8)	position 2-3: ST2/pin22 = Ground
BR2:	open: ST2/pin14 = FEE_SEL0	closed: ST2/pin14 = Ground
BR3:	open: ST2/pin15 = FEE_SEL1	closed: ST2/pin15 = Ground
BR4:	open: ST2/pin16 = 1st PIXEL	closed: ST2/pin16 = Ground
BR5:	position 1-2: bit D8 MSB-FIFO = 1PIXEL#1	position 2-3: bit D8 MSB-FIFO = STSCAN8#
BR6:	position 1-2: ST1/pin 7 = SHUT_R	position 2-3: ST1/pin7 = 1st PIXEL
BR7:	open: gate timer #2/2 = V_{CC}	closed: gate timer #2/2 = EOS_F#
BR8:	position 1-2: ST2/pin22 = ZEIL_RES	position 2-3: ST2/pin22 = TIM_IRQ

Remark: The factory default setting has been underlined.

I.6 Survey of Specifications

Functional Characteristics

- Trigger a reset procedure (photodiodes read-out without data storage)
- Trigger a read-out procedure with data storage in the buffer memory of the Interface Board
- Trigger a measurement procedure (reset, integration timing, read-out)
- Trigger the acquisition of a series of sequential spectra (reset and several read-out procedures, each time with integration period) with process sequencing within the Interface Board
- Two onboard timer IC's,
  timer #1: integration timing, scan counter
  timer #2: precision time measurements, timer/counter 2 is freely available
- FIFO buffer memory 2 K words (max. 32 K words)
- Data transfer from the FIFO also during the measurement, so that continuous spectra acquisition is possible
- Trigger output 1: TTL or external level, e.g. for triggering a flashlamp
- Trigger output 2: TTL level, outputs a pulse at read-out of the first pixel in each scan, also usable as a universal digital output
- Trigger output 3: universal TTL output, e.g. for shutter control
- Two trigger inputs (TTL) e. g. for synchronization of spectral data acquisition, or, alternatively, digital inputs
- Selectable function of the interrupt (external, read-out finished, FIFO not empty/half full, or timer 2; IRQ 3,5,9 or 15), or universal digital input

Interfaces

- Interface with Frontend Electronics: DSUB25 socket connector
- External interface: DSUB9 pin connector
- Power supply: +5 V, <500 mA from the PC
- PC interface: IBM compatible, AT (ISA) bus, 16 bits
- 16 I/O addresses (4*16 bits / 8*8 bits),
  base address selectable in steps of 16 in the range from 000H to 3F0H
- Circuit board dimensions: 100 * 160 [mm]

I.7 Connector Pin Assignment

I.7.1 Connector ST2 (to Frontend Electronics)

Connector type: 25 pin SUB-D connector, socket contacts

pin	signal designation	explanation
1	D0/D8	ADC data bit D0 or D8
2	D1/D9	ADC data bit D1 or D9
3	D2/D10	ADC data bit D2 or D10
4	D3/D11	ADC data bit D3 or D11
5	D4/D12	ADC data bit D4 or D12
6	D5/D13	ADC data bit D5 or D13
7	D6/D14	ADC data bit D6 or D14
8	D7/D15	ADC data bit D7 or D15
9	BUSY_F	ADC busy output
10	EOS_F#	sensor end of scan
11	START_F#	sensor start scan
12	BYTE_F	ADC byte select (D0..D7 or D8..D15)
13	GND	ground
14	FEE_SEL0 (GND) (*)	alternatively multiplexer control signal 0 (BR2 open) or ground (bridge BR2 installed)
15	FEE_SEL1 (GND) (*)	alternatively multiplexer control signal 1 (BR3 open) or ground (bridge BR3 installed)
16	1st PIXEL (GND) (*)	alternatively control signal 1st pixel in array (BR4 open) or ground (bridge BR4 installed)
17	GND	ground
18	GND	ground
19	GND	ground
20	GND	ground
21	GND	ground
22	Z_RES_F (GND)	alternatively sensor reset or multiplexer mode of operation (BR1 in position 1-2) or ground (bridge BR1 in position 2-3)
23	-12V_F	-12V power supply output
24	CLK_F	sensor read-out clock
25	+12V_F	+12V power supply output

Remark (*): In the standard shipping version of the PC Interface Board, the signal lines are connected to the corresponding control signals (not to ground).

I.7.2 Connector ST1 (Flash Control and Trigger)

Connector type: 9 pin SUB-D connector, pin contacts

pin	signal- and short designation	input / output	explanation
1	EXT_IRQ_IN (EX-IRQ-I)	TTL-input	**(1)** edge-triggered external interrupt request input: event-buffered (flip-flop), request may be routed to PC interrupt request or polled **(2)** alternatively for use as universal digital input
2	VCC_BLITZ_ EXT (VCC_BLZ)	flash trigger voltage input	input for the trigger voltage for flash control output
3	EXT_SCANTRIG_IMP (STSCA7#)	TTL input	trigger input for scan triggering by hardware upon **rising edge** (pulse input); Remark: period must be selected longer than the programmed integration time + read-out time to assure not to start a new scan cycle before the previous cycle is completed.
4	EXT_SCANTRIG_FLANKE (STSCAN8#)	TTL input	**(1)** Trigger input for scan triggering by hardware upon **arbitrary edge** (each edge triggers one scan, for typical application with chopper-synchronous scan) Remark: The time between two edges must be selected longer than the programmed integration time + read-out time to assure not to start a new scan cycle before the previous cycle is completed. **(2)** alternatively for use as universal digital input
5	LIGHTOUT	TTL or $U_{VCC\_BLITZ\_EXT}$ output	**(1)** pulse output (single shot) for flash control (level TTL or $U_{VCC\_BLITZ\_EXT}$), active high or active low, to be triggered either **(1a)** in mode of operation 'software flash' under PC-control or **(1b)** in mode of operation 'hardware - flash' by the EOS signal preceding the data scan (triggered by hardware at the start of the integration period before each data scan) **(2)** alternative for use as digital output, level TTL or $U_{VCC\_BLITZ\_EXT}$
6	5V_OUT	supply voltage output	+5V supply output for connection of peripheral components (e.g. shutter), I_{MAX} = 500mA, fuse SI1 on the Interface Board
7	alternative PIXEL_1 or SHUTTER_R (1PX/SH_R)	(TTL output with R_V = 100 Ohms)	**(1)** trigger output, pulse (active high) during read-out of the first pixel of the photodiode array (solder bridge BR6 in position 2-3) **(2)** alternatively for use as digital output, e.g. as direction signal for shutter (solder bridge BR6 in position 1-2 = Default setting)
8	SHUTTER_EA	(TTL output with R_V = 100 Ohms)	Digital output, for use e.g. as input-output switching signal for shutter control
9	GND		ground

I.7.3 Connector J2 (Service Connector)

Connector type: socket connector, pin contacts

pin number	signal designation	explanation
1	STSCAN6#	start pulse for read-out of the array
2	SCANRUN	read-out of the array running
3	CLK	clock signal
4	1PIXEL#1	identification signal 1st pixel of the array
5	EOS#	read-out of the array completed
6	STOR-E3#	enable data storage (internal importance only)
7	BYTE	toggle signal LSB/MSB for the ADC
8	W-CTL-C1	control word write signal
9	STSCAN1#	start scan 1, activates a scan cycle, (control port output signal)
10	R-STS-C#	status word read signal
11	STSCAN3#	start scan 3, activates a scan cycle, (integration timer output signal)
12	R-FIF-C#	read signal FIFO
13	BUSY	ADC converting
14	EMPTY#	FIFO empty
15	GND	ground
16	HALF#	FIFO half full

I.8 Standard Version, Jumper and Solder Bridges

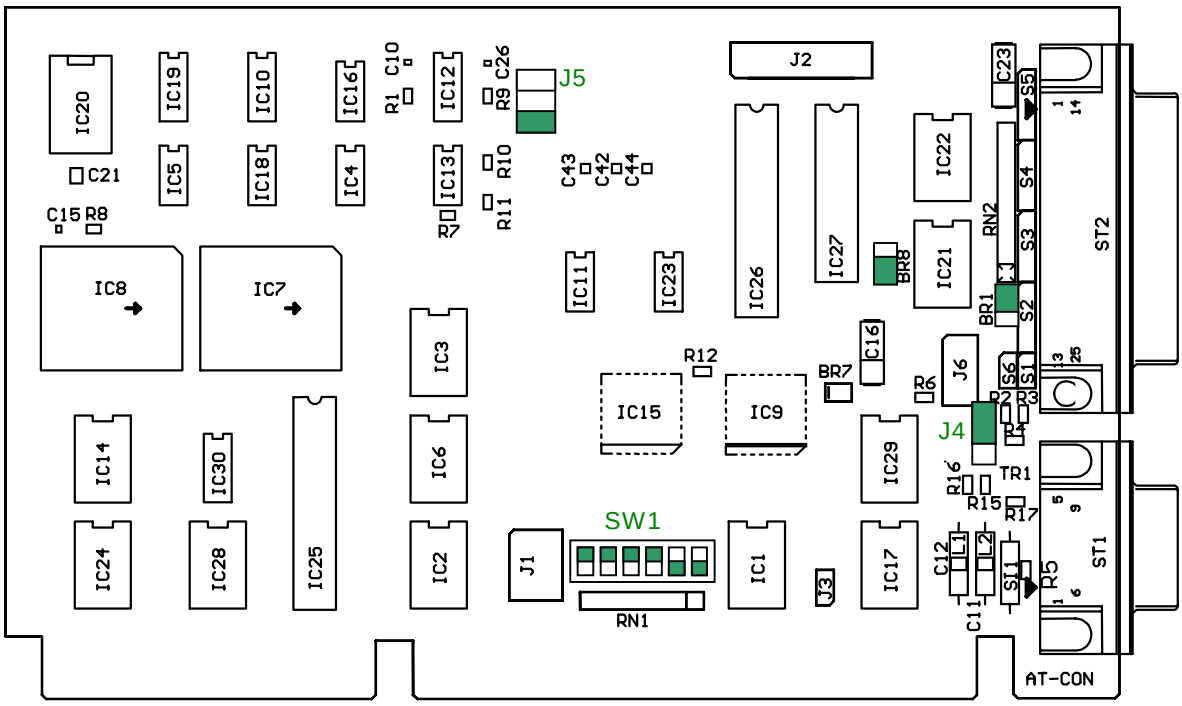


Fig. I 4: View of the PC/AT Interface Electronics, components side, default settings for jumpers and solder bridges

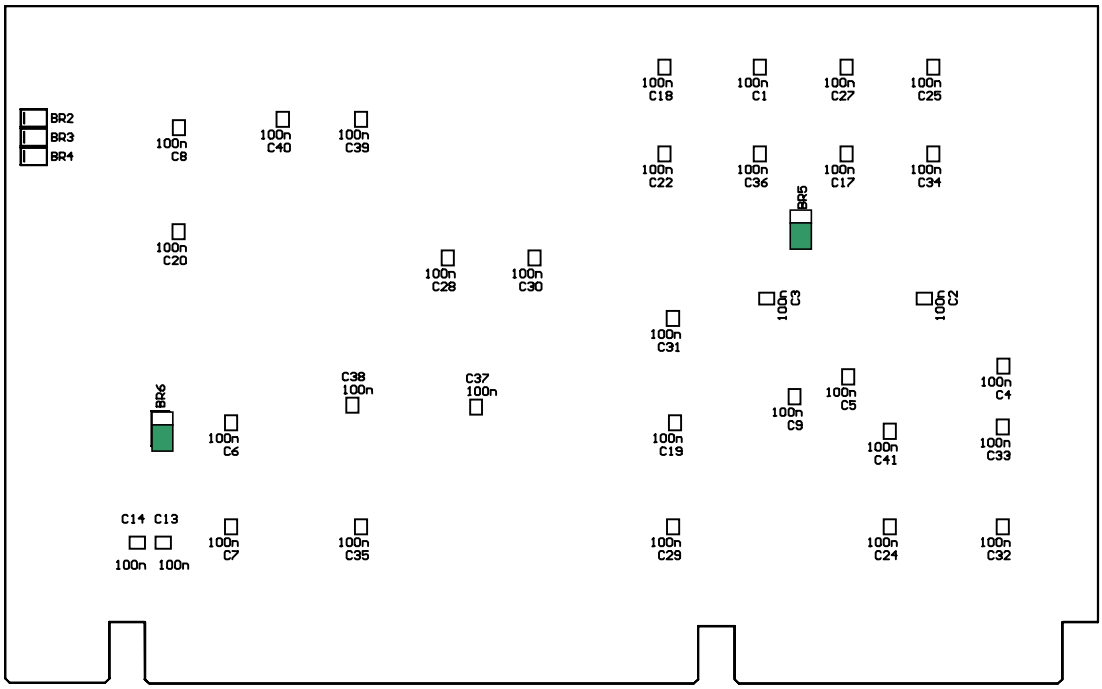
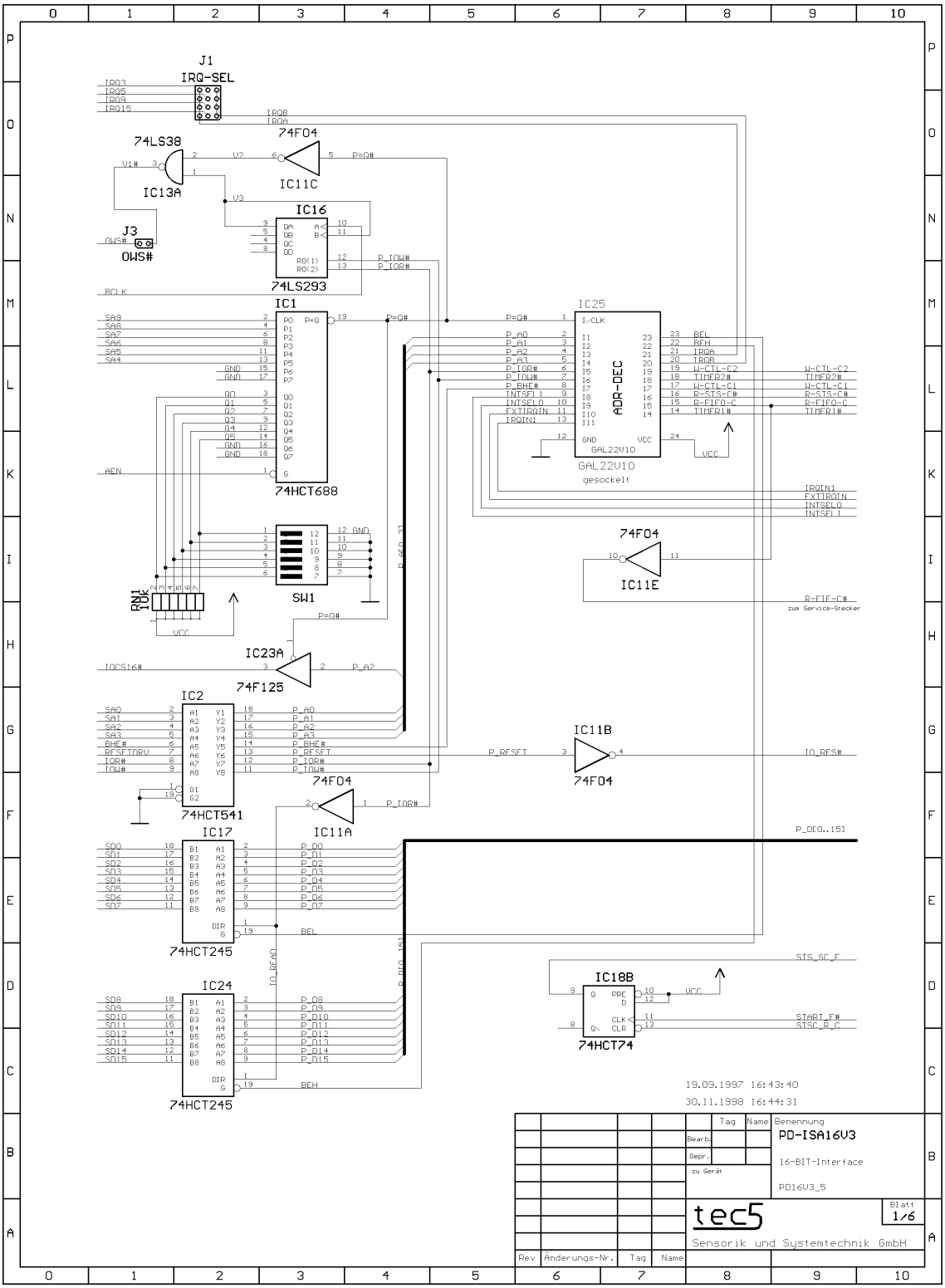


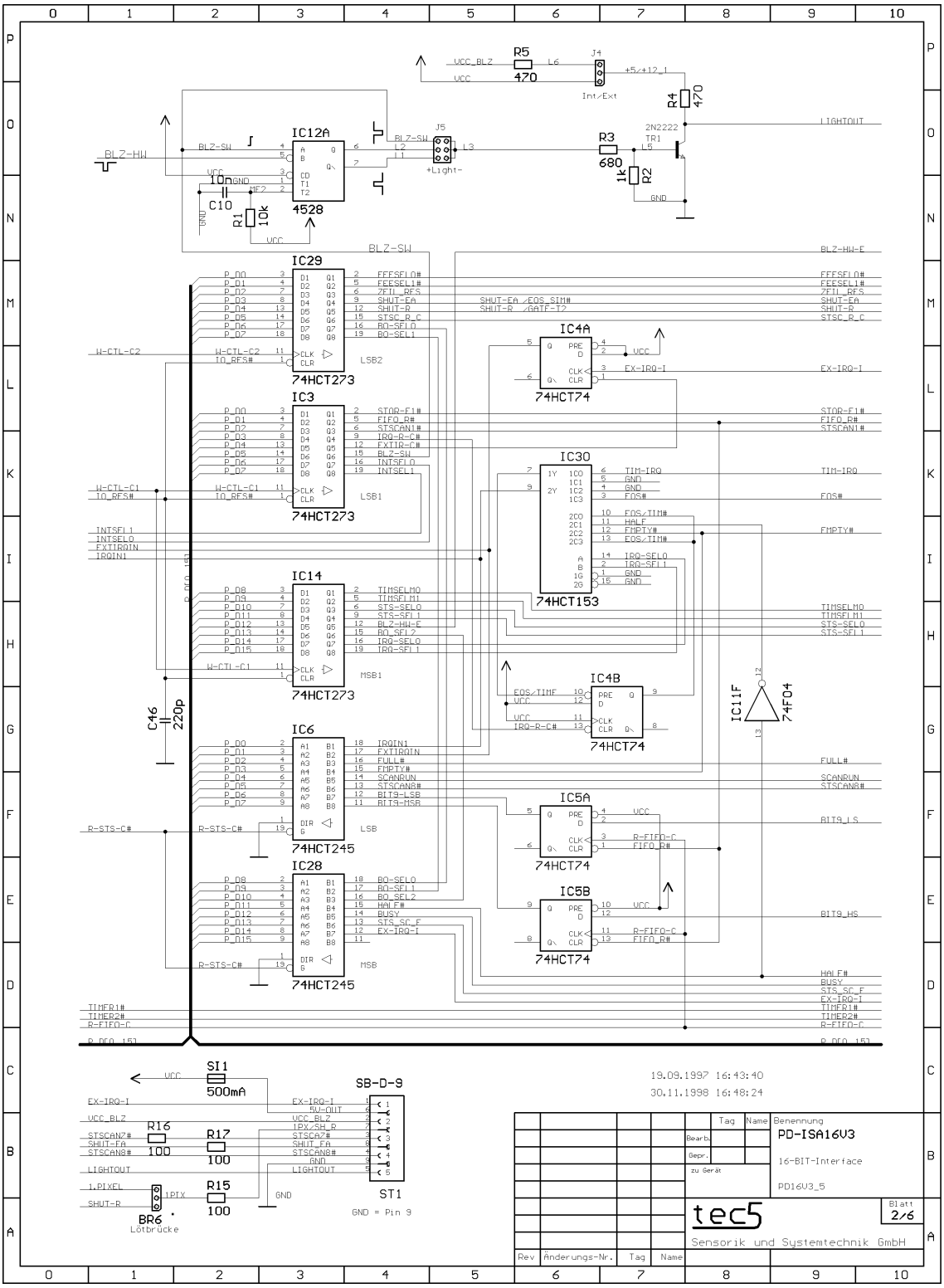
Fig. I 5: View of the PC/AT Interface Electronics, solder side, default settings for jumpers and solder bridges

A1 Circuit diagram PC/AT Interface Electronics PD-ISA16V3

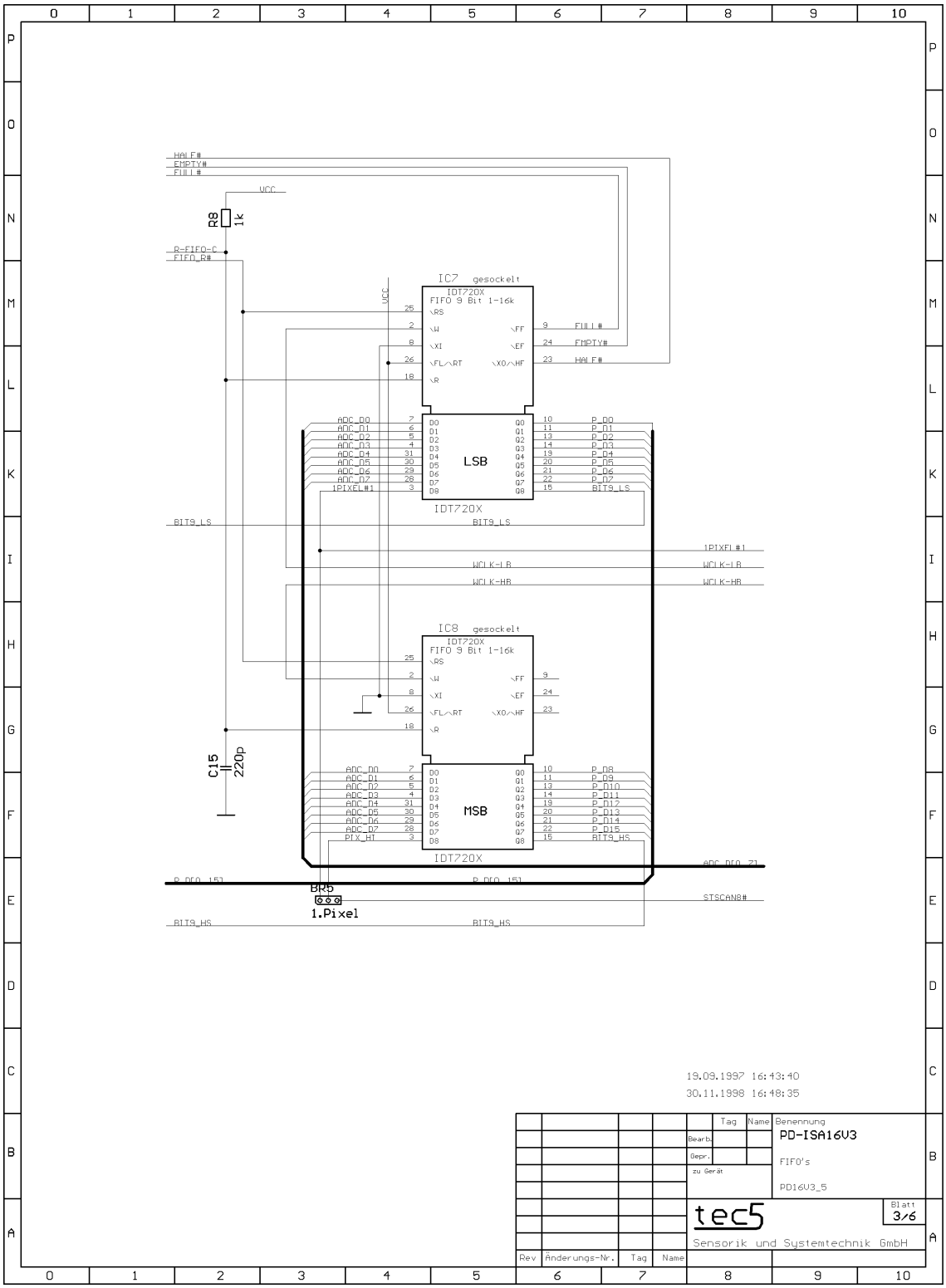
A1.1 Circuit diagram PC/AT Interface Electronics PD-ISA16V3 / Page 1 of 6



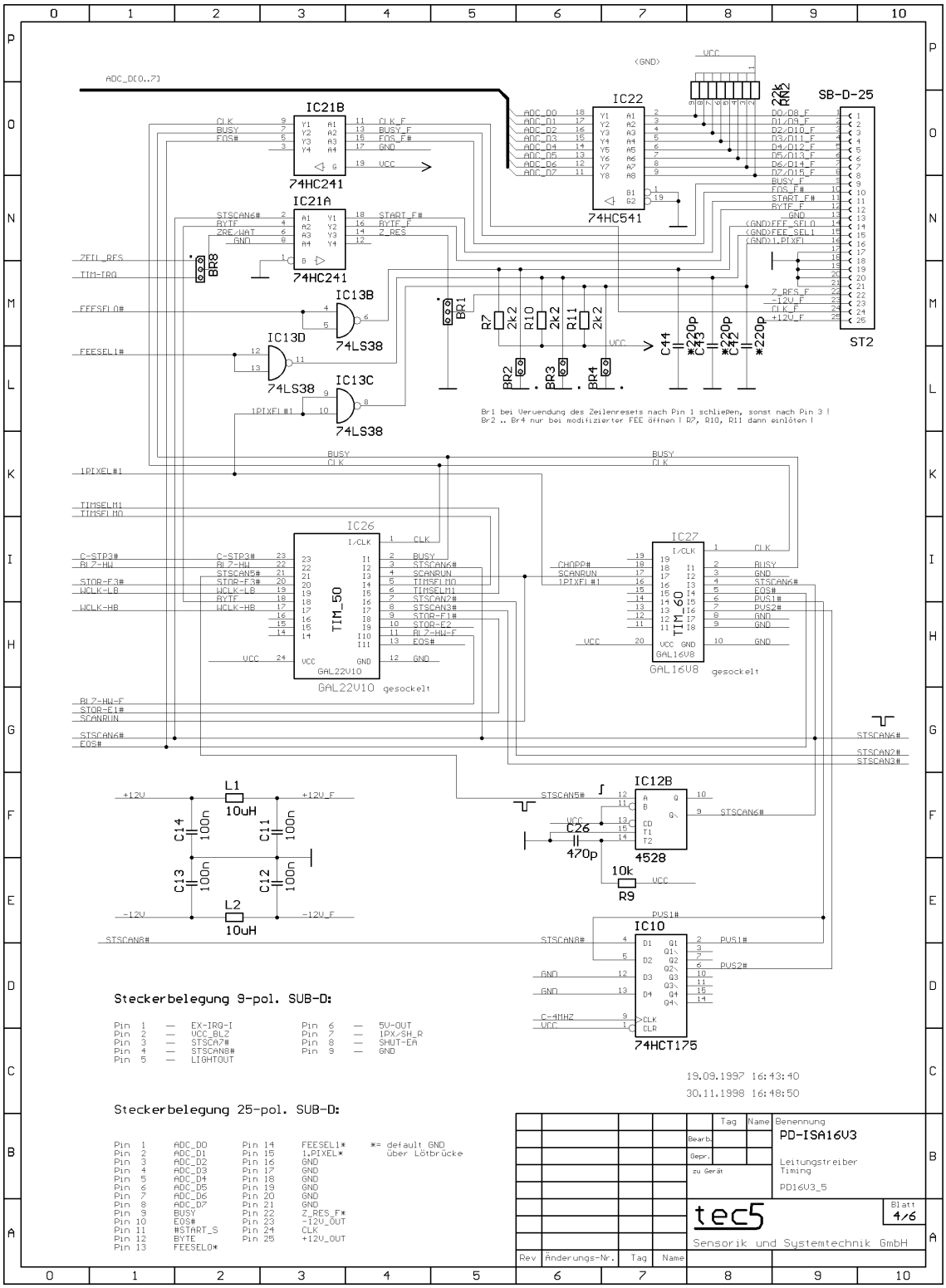
A1.2 Circuit diagram PC/AT Interface Electronics PD-ISA16V3 / Page 2 of 6



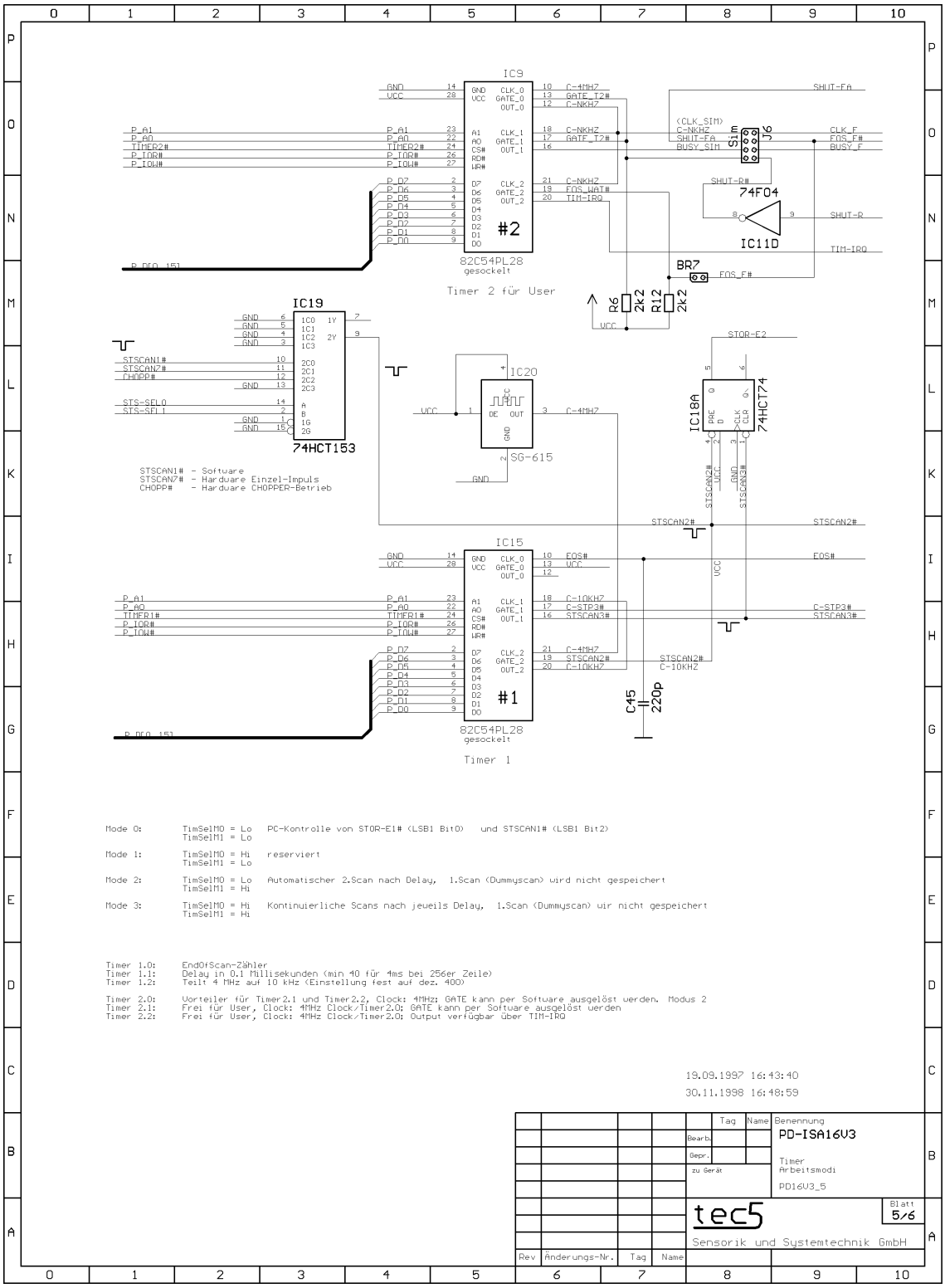
A1.3 Circuit diagram PC/AT Interface Electronics PD-ISA16V3 / Page 3 of 6



A1.4 Circuit diagram PC/AT Interface Electronics PD-ISA16V3 / Page 4 of 6



A1.5 Circuit diagram PC/AT Interface Electronics PD-ISA16V3 / Page 5 of 6



A1.5 Circuit diagram PC/AT Interface Electronics PD-ISA16V3 / Page 6 of 6