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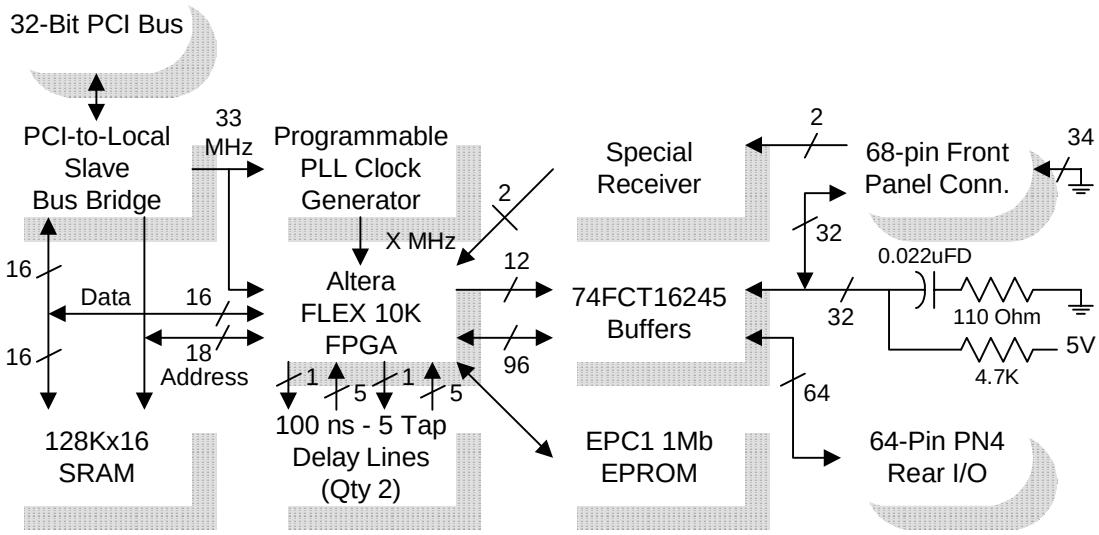
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96-Channel Reconfigurable Digital I/O



The Reconfigurable Digital I/O PMC provides a prototyping vehicle for implementing complex user-specific digital designs.

The product uses an Altera FLEX 10K Field Programmable Gate Array (FPGA) in a 240 pin Surface Mount package. The Altera FLEX 10K family in this package consists of a variety of parts from the 10K20 to the 10K70, with usable equivalent gate counts for the 10K70 from 46K to 118K gates for representative designs.

The EPF10K70RC240-4 is used for the default configuration, which provides the highest gate count at reasonable speeds. For volume production runs, other lower density and/or higher speed parts may be substituted.

The design features a total of 96 general-purpose Digital I/Os distributed at the front panel (32 I/Os) and at the rear I/O connector on the PMC (64 I/Os). Each group of eight I/O lines is buffered by a 74FCT16245, and the directionality of each group is individually controlled by a user-programmable signal from the Altera FPGA.

I/O out the PMC front panel is terminated with an R/C parallel network as shown. Termination for individual digital I/O lines may be disabled by de-populating the corresponding capacitor. The I/O out the rear of the PMC is not terminated; it is anticipated that users will terminated the rear I/O signals via a suitable transition module designed for the user's application.

A 128K x 16 SRAM is provided on the PMC, and is accessible from the Altera part as well as the PCI interface. A dual-port RAM effect is achieved by arbitrating accesses between the Altera FPGA and PCI bus using control logic implemented in the Altera part.

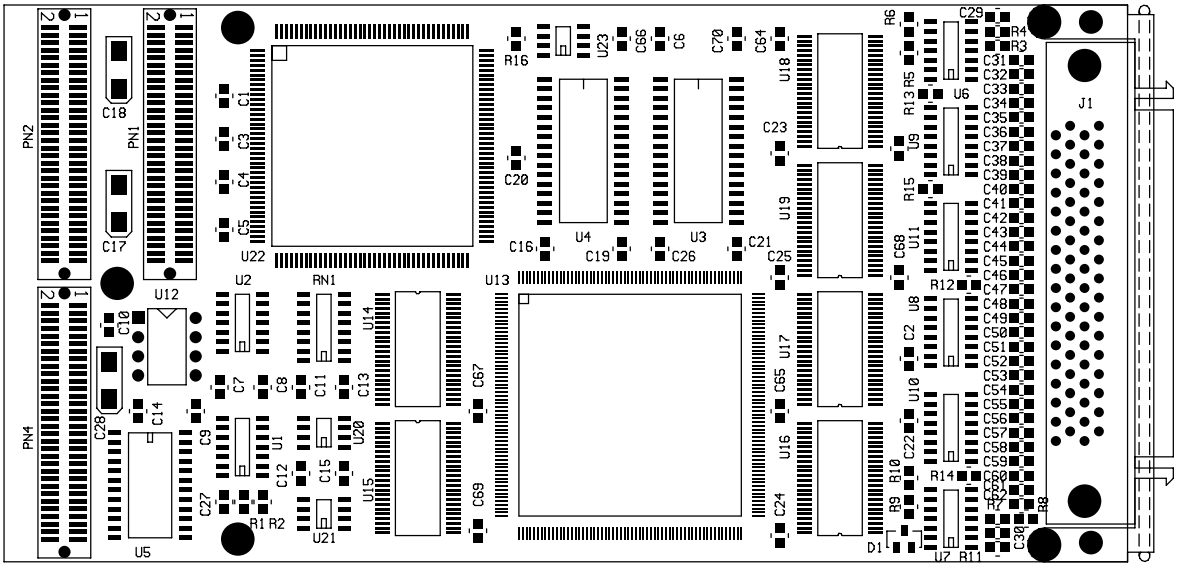
The 16-bit data bus from the PCI slave-only bridge chip, along with 18 address lines (A[17..0]), are connected to the Altera FPGA. 32-bit PCI bus is supported, and the PCI bridge will automatically decompose 32-bit PCI accesses into multiple 16-bit equivalents as needed.

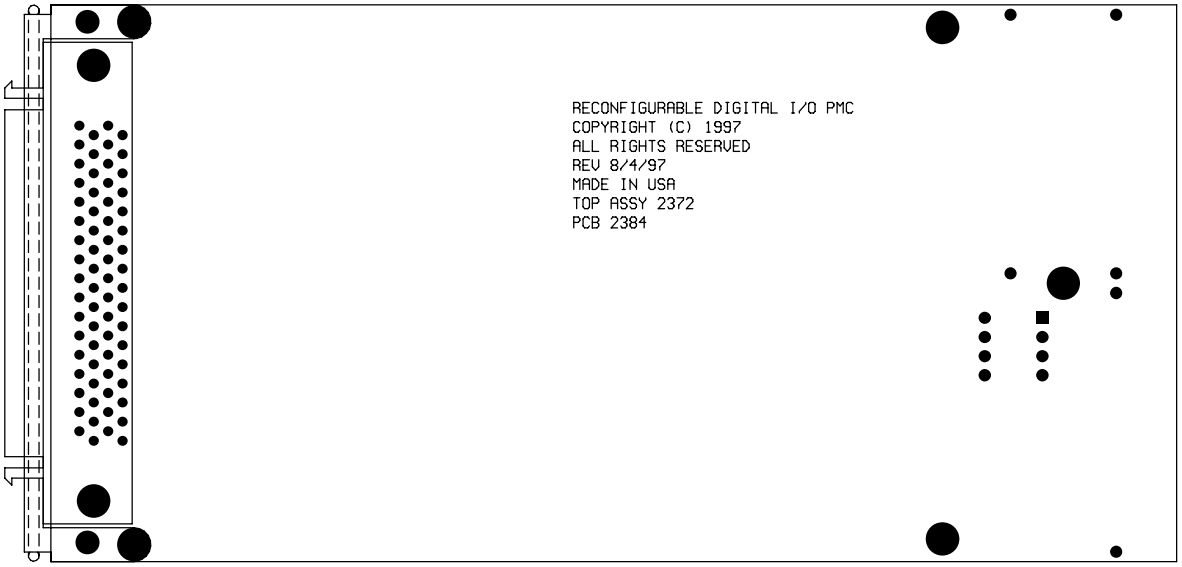
For application timing, the 33 Mhz from the PCI bus and a PLL-generated clock are inputs to the Altera FPGA. Any frequency with better than 0.1% accuracy can be generated by the PLL as programmed from the host processor. Also, two 100-ns delay lines with 5-taps spaced at 20 ns are available for user's time critical asynchronous needs. Finally, two special receivers are available for low-level serial clock and data recovery.

On power up, the Altera FPGA configuration cells are automatically loaded from a serial EPROM located on the PMC (U5, "EPC1"). The user may override this default configuration by dynamically reprogramming the FPGA from the host processor, or by burning an EPC1 with the user's application (EPC1 chips and programmer are not supplied).

An example implementation of a digital I/O board with dual-port access to the SRAM, implemented in Altera HDL ("AHDL"), and corresponding "C" source code running in the host is provided with the product. The Altera MAX-PLUS development software, or equivalent, is purchased directly from Altera.

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Product Summary

Technobox Part Number:	2372
Typical Power Dissipation:	TBD
Power Supplies Required:	+5V
PCI Signaling Environment:	5V

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