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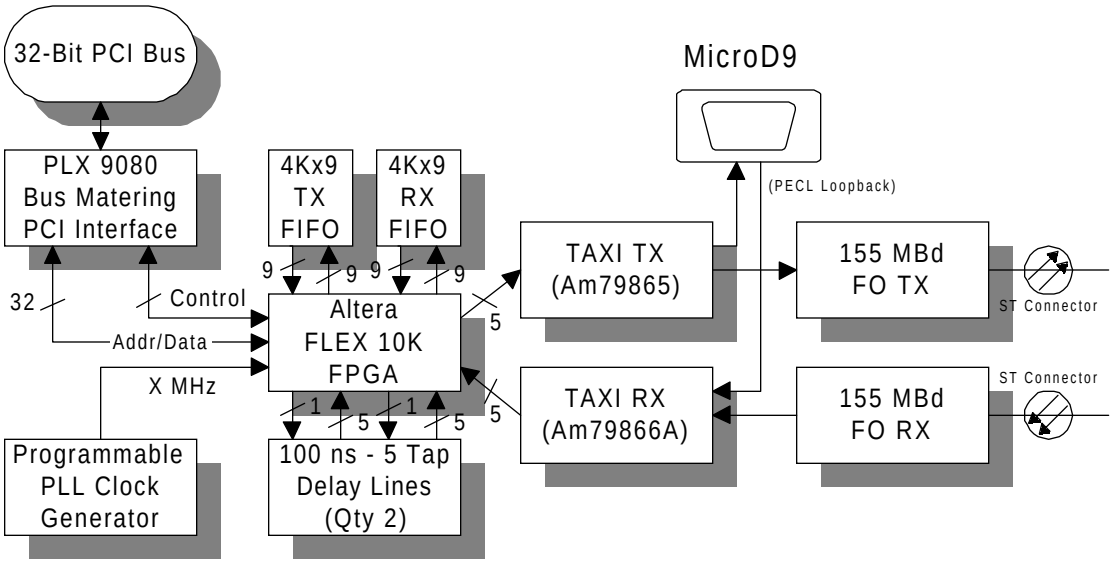
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2-Channel Reconfigurable 155 Mb/s Fiber Optic PMC



The Reconfigurable 155 Mb/s Fiber Optic (FO) PMC provides a means for implementing Fiber Optic interfaces for FDDI and other Fiber Optic standards having unusual requirements not supported by standard chipsets.

A single transmit channel and a single receive channel each operate at bitrates up to 155 Mb/s. The specific rate can be varied according to a Phase Locked Loop circuit or an on-board 25 Mhz crystal.

An Advanced Micro Devices FDDI PHY chipset converts the serial bitstream to/from the FO devices to 5-bit wide connections to the ALTERA FPGA. 4b/5b or 8b/10b encoding can be used as implemented in the ALTERA design.

The Fiber Optic interfaces are available out the PMC front panel, and use a standard “ST” style connector. 50 or 62.5 um, 1300 nm multi-mode optical fiber is supported by this product.

Also available at the front panel are the PECL equivalents of the serial data stream for the Transmit and Receive Fiber Optic devices, each providing a single differential pair at the MicroD9 connector. Use of either PECL or FO is selected according to the ALTERA design.

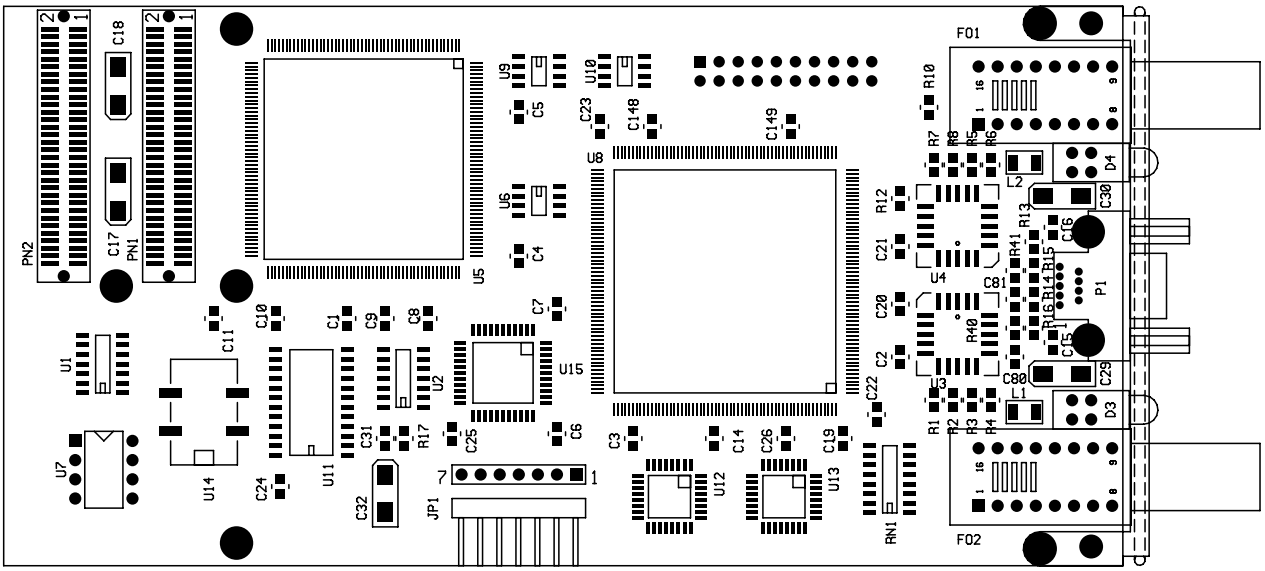
A central feature of this design is an ALTERA FLEX10K Field Programmable Gate Array (FPGA). Normally populated with a FLEX10K70 device, the board offers 3744 logic cells with 4096 registers, or roughly 70,000 gate density for typical designs. The ALTERA may be configured over the PCI bus, or by a OTP EPROM (“EPC1”) inserted on the PMC.

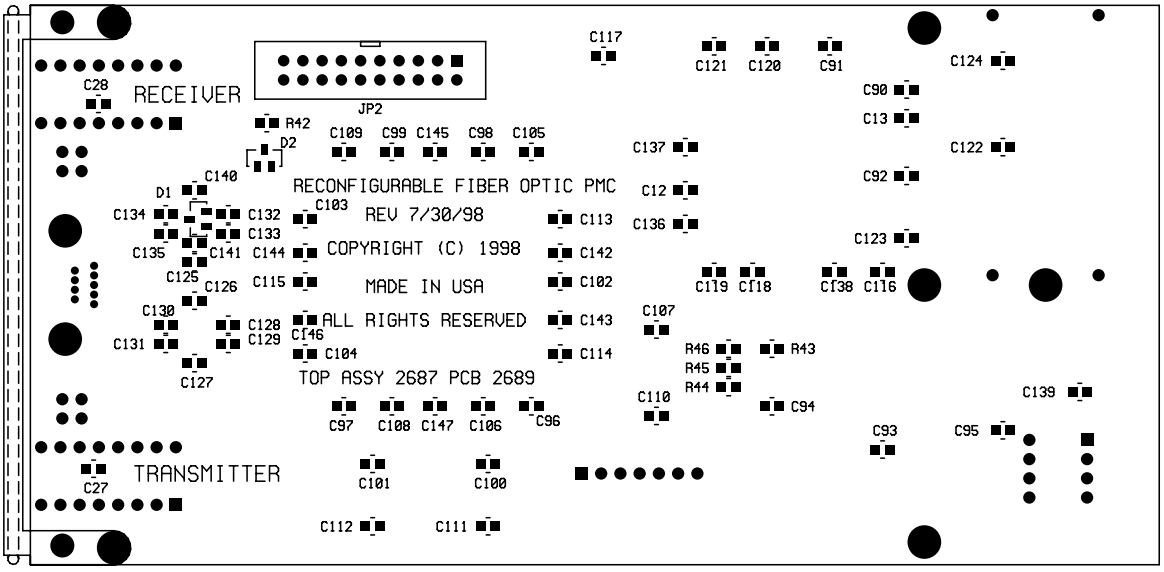
Available to the ALTERA part is a Phase Lock Loop (“PLL”) chip offering programmable frequencies up to 57.5 Mhz with typically 0.1% precision. Two 100-ns tapped delay lines provide fine-tuning of asynchronous combinatorial circuits. Two 4Kx9 synchronous FIFOs provide elastic buffering for data movement between the Fiber Optic interfaces and the PCI bus.

The PCI bus interface is implemented using a PLX Technology 9080 part. This chip provides two powerful DMA engines for moving data between host memory and the ALTERA FPGA. One DMA channel handles the TX FO interface, while the other handles the TX FO interface. Using the DMA in a “data chaining” mode allows un-interrupted transfer of data between the FO interfaces and multiple non-contiguous buffers in host memory. The 9080 may be configured to post a PCI interrupt after each DMA buffer is filled/emptied.

The product is supplied with an example ALTERA implementation which moves data between PLX9080 and the transmit/receive FO interfaces using a 4B/5B code. The ALTERA design incorporates interface to the 9080, assembly/disassembly registers for 32-bit to 8-bit conversion, TX and RX FIFO support, assembly/disassembly for 8-bit to 4-bit conversion, a lookup function for 4B/5B conversion, and use of the PLL for determining the TX/RX FO bit rate.

Also provided is example “C” source code to operate the FO interfaces in a loopback w/compare mode. This code demonstrates use of 9080 Data Chaining DMA, programming of the PLL, and downloading the ALTERA configuration image over the PCI bus.





Product Summary

Technobox Part Number:	2687
Typical Power Dissipation:	TBD
Power Supplies Required:	+5V
PCI Signaling Environment:	5V or 3.3V

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