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Digital I/O PMC

Enhanced 32-Channel RS485/422 Differential PMC

The Enhanced 32-channel Reconfigurable RS422/RS485 Digital I/O PMC provides a vehicle for implementing complex user-specific digital designs requiring a differential interface.

This product is a second-generation "enhanced" design derived from the P/N 2674/3353 products, and provides additional features including 64b/66MHz PCI bus support, up to 66 MHz local bus clock, double the local SRAM, and up to 20K Logic Elements compared to 3.7K LEs on the original 10K70 based design. All the features of the 2674/3353 boards have been incorporated into this new product, enabling customers easy migration for existing applications.

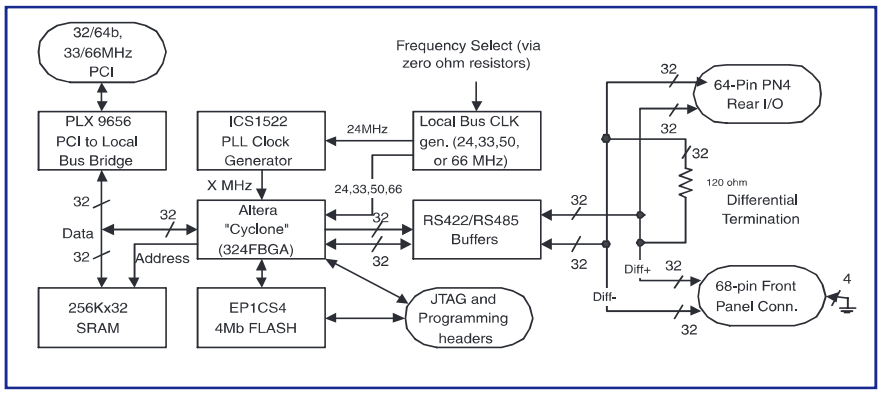
The product uses an Altera "Cyclone" FPGA in a 324 Fine-Line FPGA. This package spans the 4K, 12K, and 20K logic element parts. The standard, stocked product uses an EP1C12F324C8 density/speed part.

The design features a total of 32 general-purpose RS422/RS485 driven digital I/Os wired to both the front panel and rear PN4 connector (64 signals per connector taking into account 2 signals per differential pair). For each of the 32 channels, the bidirectionality is controlled by an output from the FPGA.

The 68-pin front panel connector is compatible with standard fast/wide differential SCSI cables. Furthermore, an optional Technobox transition panel (e.g., P/N 3044) may be used to break out the differential signals into more convenient individual connectors, such as DB9s.

Each of the 32 differential pairs is terminated with a 120 ohm parallel resistance or an R/C termination as shown in the block diagram. Individual resistors are used with each differential pair, allowing for easy removal or value change on a per-channel basis.

With the proper FPGA design the 256K x 32b SRAM provided on the PMC is accessible from the Altera part as well as the PCI interface. The 32-bit data bus is shared between the ALTERA and the PCI interface devices. The SRAM address is driven by ALTERA outputs. This technique allows a variety of memory

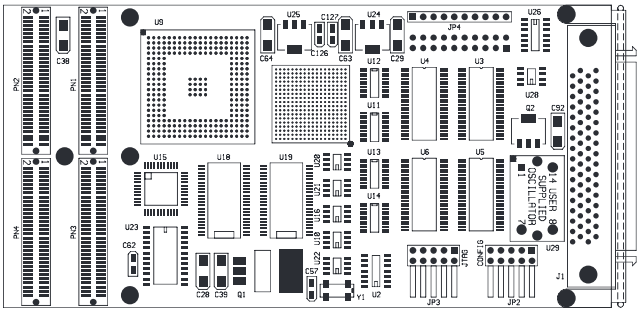


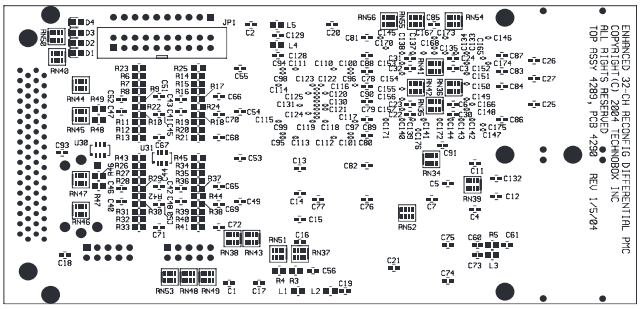


4289

- **Provides 32 Channels of General-purpose Digital I/O**
- **Second-generation Enhanced Design**
- **Supports 64 bit / 66 MHz PCI Bus**
- **FPGA-based**
- **Reprogrammable by Host or On-board Flash (EP1CS4)**
- **Variable SRAM Architectures Allowed**
- **Headers for JTAG Connection and FLASH Programming**
- **Sample FPGA Implementation and Host "C" Code**

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architectures for the SRAM: single-port SRAM, dual-port SRAM, one or more FIFOs, and even linked list structures for more complex .

For application timing, a local bus clock and a PLL generated clock are inputs to the ALTERA FPGA. The PLX local bus clock is selectable as 24, 33, 50, or 66 MHz using resistor-jumpers. Any frequency with better than 0.1% accuracy can be generated by the PLL as programmed from the host processor.

On power up, the Altera FPGA configuration cells are automatically loaded from a serial EPROM located on the PMC. The user may override this default configuration by dynamically reprogramming the FPGA from the host processor, or by in-circuit burning of the re-programmable FLASH EPCS4 chip with the user's application. Also, two 10-pin headers are provided for development with ByteBlaster cables. One is for the JTAG connection and the other is for programming the EP1CS4.

An example implementation of a digital I/O board with dual-port access to the SRAM and corresponding "C" source code running in the host is provided with the product. QUARTUS development software is available directly from Altera.

Specifications

Temperature (Operating): 0° to 55° C

Temperature (Storage): -40° to +85° C

Altitude: Not specified or characterized (Typical similar equipment is at 15,000 ft.)

Humidity (Operating/Storage): 5% to 90% non-condensing

Vibration: Not specified or Characterized

MTBF: Upon request

Typical Power Dissipation: TBD

Power Supplies Required: +5V

PCI Environment: 5V or 3.3V; 32/64 bits, 33/66 MHz

Ordering Information

Part Number: 4289 (w/EP1C12F324C8)

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