TEK Microsystems

FastPack Products

FP-Serial2-422
Two Channel EIA-422 Serial I/O Module
User's Manual

TEK/TM-13415A
17 February 1998

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Product Description

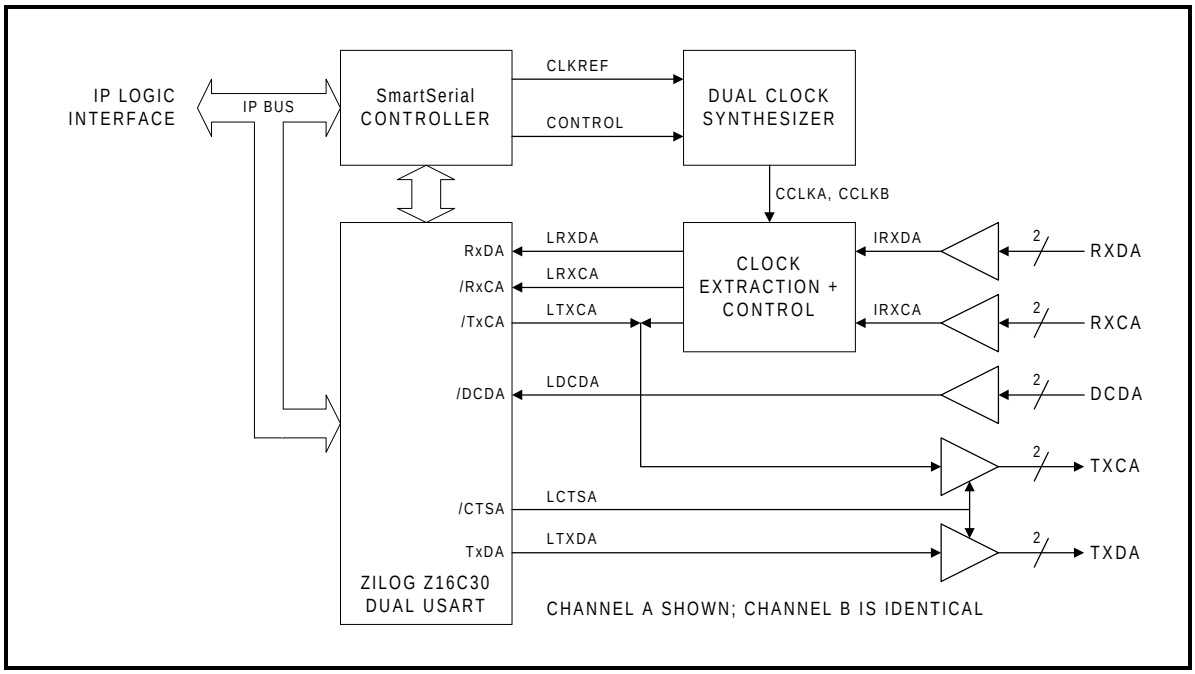
The FP-Serial2-422 is an ANSI/VITA 4-1995 IP module which provides two independent high speed full-duplex serial I/O channels between a carrier board and external peripherals.

The FP-Serial2-422 uses the Zilog Z16C30 Serial Communications Controller to provide the serial I/O functions and an EPLD-based SmartSerial controller to provide a high-performance interface between the Z16C30 and the carrier board using the ANSI/VITA 4-1995 IP interface.

The SmartSerial controller also provides a clock extraction function which extends the Z16C30's maximum data rate from 625 Kbps to 5 Mbps when operating without an external clock signal. With an external clock, the Z16C30 maximum data rate of 10 Mbps is fully supported.

The FP-Serial2-422 has a dual clock synthesizer which is used to generate baud rates for the two serial channels. Arbitrary baud rates may be generated with little or no error by configuring the clock synthesizer with an appropriate control word.

A block diagram of the FP-Serial2-422 is shown in the figure below.



Specifications

Clock Speed	8 or 32 MHz, auto-configuring
ID Space	Supported per ANSI/VITA 4-1995 specification, Format I
I/O Space	Byte and word accesses supported per ANSI/VITA 4-1995 specification
Memory Space	Not used
Interrupt Capability	Two interrupt levels, autovectored using Z16C30 status-affects-vector function
DMA Capability	Two DMA levels, independently enabled
Mechanical	Type I IP module per ANSI/VITA 4-1995 specification
Operating Temperature	0 to 70 degrees C. -40 to +85 degrees C available as special order.
Storage Temperature	-40 to +85 degrees C.

Support Information

Warranty Information

The FP-Serial2-422 is warranted against defects in material or workmanship for a period of three years from the original date of purchase. If a failure occurs within the warranty period, TEK will repair or replace the product at no cost to the user. For warranty repair, please contact TEK as described below and obtain an RMA number and return shipping instructions.

Contact Information

If technical support or repair assistance is required, please contact TEK through one of the following methods:

Internet	http://www.tekmicro.com
Email	support@tekmicro.com
Telephone	+1 781 270 0808
Facsimile	+1 781 270 0813
Mail	TEK Microsystems, Incorporated One North Avenue Burlington, MA 01803-3313

I/O Interface

Signal Names

The FP-Serial2-422 external interface consists of five EIA-422 signal pairs for each of two channels. The EIA-422 signals are TXD, TXC, RXD, RXC and DCD, and the channels are designated A and B. Each signal pair has a + and – signal to implement a differential EIA-422 interface.

Signal names are constructed as signal/channel/polarity (i.e. the TXD signals for channel A are named TXDA+ and TXDA–).

Signal Levels

All of the FP-Serial2-422's external I/O signals use EIA-422 signal levels.

Signal Terminations

Signals which are generated by the FP-Serial2-422 (TXD and TXC) are driven by an EIA-422 driver, National Semiconductor p/n DS34C87M or equivalent. The signal should be terminated at the other end of the cable.

Signals which are accepted by the FP-Serial2-422 (RXD, RXC, and DCD) are received by an EIA-422 receiver, National Semiconductor p/n DS34C86M or equivalent. Each set of signals is terminated using a 6-pin SIP resistor network with three isolated 180 ± 5% Ohm resistors (Dale p/n CSC06A03-181G or equivalent). Serial channel A is terminated using RN4 and serial channel B is terminated using RN3. Both resistor networks are socketed to allow field removal and replacement.

Signal Pinout

The FP-Serial2-422 external interface consists of the signals listed below:

Signal Name	Direction	I/O Pin	D15S pinout	D9S pinout
TXDA+	From FP	1	1	1
TXDA–	From FP	2	9	6
TXCA+	From FP	3	2	2
TXCA–	From FP	4	10	7
RXDA+	To FP	5	3	3
RXDA–	To FP	6	11	8
RXCA+	To FP	7	4	4
RXCA–	To FP	8	12	9
GND		9,10	5,13	5
DCDA+	To FP	11	6	–
DCDA–	To FP	12	14	–
GND		13-16	7,8,15	–
TXDB+	From FP	17	1	1
TXDB–	From FP	18	9	6
TXCB+	From FP	19	2	2
TXCB–	From FP	20	10	7
RXDB+	To FP	21	3	3
RXDB–	To FP	22	11	8
RXCB+	To FP	23	4	4
RXCB–	To FP	24	12	9
GND		25, 26	5,13	5
DCDB+	To FP	27	6	–
DCDB–	To FP	28	14	–
GND		29-32	7,8,15	–
N/C		33-40	–	–
Reserved		41-50	–	–

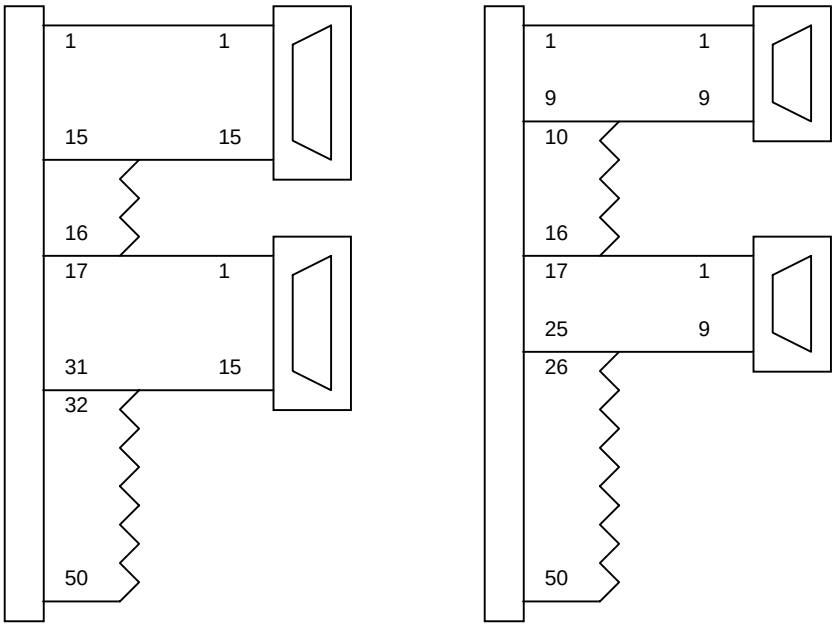
The I/O Pin column shows the pin numbers on the IP I/O connector. These pin numbers typically correspond directly to the IP carrier's external interface connector pin numbers. For example, a Motorola MVME162 VMEbus carrier maps each IP module's 50 I/O pins to a 2x25 header connector with the same pin numbering as the IP I/O connector.

Note that I/O pins 41-50 are reserved for factory test and should not be connected.

Cable Assembly

The I/O pinout is designed to support a ribbon cable assembly to a pair of 15-pin D-type connectors or a pair of 9-pin D-type connectors without requiring discrete wiring. Signals are arranged to allow the use of twisted-pair ribbon cable.

The cable assemblies may be constructed as shown below:



CABLE ASSEMBLY, 50-PIN TO DUAL 15-PIN D-TYPE

CABLE ASSEMBLY, 50-PIN TO DUAL 9-PIN D-TYPE

A 9-pin loopback connector may be constructed as follows:

- 1-3, 6-8, 2-4, 7-9

A 15-pin loopback connector may be constructed as follows:

- 1-3, 9-11, 2-4, 10-12

IP Logic Interface

Overview

The FP-Serial2-422 provides a high-performance control interface compatible with the ANSI/VITA 4-1995 IP specification.

The FP-Serial2-422 SmartSerial controller has a number of features to maximize performance and system throughput. Operation is supported at 8 and 32 MHz, with automatic detection of the IP clock rate and configuration of the onboard interface logic. Interrupt and DMA functions are fully supported, allowing maximum data throughput with minimum software overhead.

The FP-Serial2-422 implements a multiplexed bus interface to the Zilog Z16C30, allowing direct access to most on-chip registers. This eliminates the use of "pointer" registers for most operations, simplifying software functions and eliminating the need to mask interrupts when using indirect register access.

I/O read cycles from the FP-Serial2-422 use the minimum number of wait states possible to the Zilog Z16C30 register space.

I/O write cycles to the FP-Serial2-422 are transparently posted to maximize effective bus throughput. Write posting allows the FP-Serial2-422 to release the IP bus with zero wait states and complete the internal write cycle in parallel with the next carrier board operation.

Wait States

Wait states for each supported type of bus cycle are shown in the table below.

Cycle Type	Wait states @ 8 MHz	Wait states @ 32 MHz
ID read	0	1
I/O read from SmartSerial control register	0	1
I/O write to SmartSerial control register	0	0
I/O read from Z16C30 register	1	4
I/O write to Z16C30 register	0 (1 if back-to-back)	0 (3 if back-to-back)
Interrupt acknowledge read from Z16C30	3	10
DMA read from Z16C30 data register	1	3
DMA write to Z16C30 data register	1	3

Wait state performance for Z16C30 write cycles depends on the type of cycle and the next operation to the FP-Serial2-422. All write cycles are immediately acknowledged and posted if no write cycle is already in process. If a previously posted write cycle is in process, the FP-Serial2-422 will insert wait states to delay the current cycle until the previous write cycle has completed. The number of wait states shown above for I/O write cycles is the worst-case condition based on back-to-back write cycles to the FP-Serial2-422. No wait states are required if the next cycle does not access the FP-Serial2-422.

DMA writes are not posted to allow the DMAreq signal to be updated before acknowledging the cycle. This allows the FP-Serial2-422 to support back-to-back DMA write cycles, resulting in burst DMA throughput of 12.8 MB/s with a 32 MHz IP clock (32 MHz ÷ 5 clocks/cycle x 2 bytes/cycle).

ID Space

The FP-Serial2-422 ID space contains the following information at the addresses shown:

Address	ID Data	Description
0x00	0x49	Signature (ASCII "I")
0x01	0x50	Signature (ASCII "P")
0x02	0x41	Signature (ASCII "A")
0x03	0x48	Signature (ASCII "H")
0x04	0x33	Manufacturer ID (0x33 = TEK Microsystems)
0x05	0x22	Model Number (0x22 = FP-Serial2-422)
0x06	0x00	Revision (currently 0x00)
0x07	0x00	Reserved (set to 0x00)
0x08	0x00	Driver ID, low byte (currently 0x00)
0x09	0x00	Driver ID, high byte (currently 0x00)
0x0A	0x0C	Number of bytes used (currently 12)
0x0B	0xDB	CRC of above information

Future revisions of the FP-Serial2-422 will have different data in the revision field and may include a non-zero driver ID. The manufacturer ID and model number will remain as shown above.

I/O Space – Z16C30 Registers

The FP-Serial2-422 maps the Z16C30 into 62 out of 64 addressable 16-bit locations in the IP I/O space. The Z16C30 interface fully implements the multiplexed address/data bus, allowing direct access to most Z16C30 registers.

The SmartSerial controller automatically loads the Bus Control Register (BCR) when a hardware reset is performed. The BCR is loaded with 0x0005, specifying a multiplexed 16-bit address/data bus with register addresses on D[6:0] and a single-pulse INTACK cycle. The multiplexing of the onboard bus is transparent to the user.

The register map of the Z16C30 is shown on the following pages. The sample address shown is for a Motorola MVME162 with the FP-Serial2-422 installed in slot A.

Register Name	Acronym	IP A[6:1]	MVME162 Address
A: Channel Command/Address Register	CCAR	000000	FFF58000
A: Channel Mode Register	CMR	000001	FFF58002
A: Channel Command/Status Register	CCSR	000010	FFF58004
A: Channel Control Register	CCR	000011	FFF58006
A: Reserved		000100	FFF58008
A: Reserved		000101	FFF5800A
A: Test Mode Data Register	TMDR	000110	FFF5800C
A: Test Mode Control Register	TMCR	000111	FFF5800E
A: Clock Mode Control Register	CMCR	001000	FFF58010
A: Hardware Configuration Register	HCR	001001	FFF58012
A: Interrupt Vector Register	IVR	001010	FFF58014
A: I/O Control Register	IOCR	001011	FFF58016
A: Interrupt Control Register	ICR	001100	FFF58018
A: Daisy-Chain Control Register	DCCR	001101	FFF5801A
A: Miscellaneous Interrupt Status Register	MISR	001110	FFF5801C
A: Status Interrupt Control Register	SICR	001111	FFF5801E
A: Receive/Transmit Data Register	DR	010000	FFF58020
A: Receive Mode Register	RMR	010001	FFF58022
A: Receive Command Status Register	RCSR	010010	FFF58024
A: Receive Interrupt Control Register	RICR	010011	FFF58026
A: Receive Sync Register	RSR	010100	FFF58028
A: Receive Count Limit Register	RCLR	010101	FFF5802A
A: Receive Character Count Register	RCCR	010110	FFF5802C
A: Time Constant 0 Register	TC0R	010111	FFF5802E
A: Transmit Mode Register	TMR	011001	FFF58032
A: Transmit Command/Status Register	TCSR	011010	FFF58034
A: Transmit Interrupt Control Register	TICR	011011	FFF58036
A: Transmit Sync Register	TSR	011100	FFF58038
A: Transmit Count Limit Register	TCLR	011101	FFF5803A
A: Transmit Character Count Register	TCCR	011110	FFF5803C
A: Time Constant 1 Register	TC1R	011111	FFF5803E

Note that IP address 011000 (MVME162 address FFF58030) is not mapped to the Z16C30. This address is used for the SmartSerial CCR and DCR registers.

Register Name	Acronym	IP A[6:1]	MVME162 Address
B: Channel Command/Address Register	CCAR	100000	FFF58040
B: Channel Mode Register	CMR	100001	FFF58042
B: Channel Command/Status Register	CCSR	100010	FFF58044
B: Channel Control Register	CCR	100011	FFF58046
B: Reserved		100100	FFF58048
B: Reserved		100101	FFF5804A
B: Test Mode Data Register	TMDR	100110	FFF5804C
B: Test Mode Control Register	TMCR	100111	FFF5804E
B: Clock Mode Control Register	CMCR	101000	FFF58050
B: Hardware Configuration Register	HCR	101001	FFF58052
B: Interrupt Vector Register	IVR	101010	FFF58054
B: I/O Control Register	IOCR	101011	FFF58056
B: Interrupt Control Register	ICR	101100	FFF58058
B: Daisy-Chain Control Register	DCCR	101101	FFF5805A
B: Miscellaneous Interrupt Status Register	MISR	101110	FFF5805C
B: Status Interrupt Control Register	SICR	101111	FFF5805E
B: Receive/Transmit Data Register	DR	110000	FFF58060
B: Receive Mode Register	RMR	110001	FFF58062
B: Receive Command Status Register	RCSR	110010	FFF58064
B: Receive Interrupt Control Register	RICR	110011	FFF58066
B: Receive Sync Register	RSR	110100	FFF58068
B: Receive Count Limit Register	RCLR	110101	FFF5806A
B: Receive Character Count Register	RCCR	110110	FFF5806C
B: Time Constant 0 Register	TC0R	110111	FFF5806E
B: Transmit Mode Register	TMR	111001	FFF58072
B: Transmit Command/Status Register	TCSR	111010	FFF58074
B: Transmit Interrupt Control Register	TICR	111011	FFF58076
B: Transmit Sync Register	TSR	111100	FFF58078
B: Transmit Count Limit Register	TCLR	111101	FFF5807A
B: Transmit Character Count Register	TCCR	111110	FFF5807C
B: Time Constant 1 Register	TC1R	111111	FFF5807E

Note that IP address 111000 (MVME162 address FFF58070) is not mapped to the Z16C30. This address is used for the SmartSerial S*x*CR registers.

I/O Space – SmartSerial Registers

Overview

In addition to the Zilog Z16C30 registers, the FP-Serial2-422 contains four registers which provide control and status functions for the SmartSerial controller. These registers are:

Address	Name	Description
0x18 MSB	CCR	Card Control Register
0x18 LSB	DCR	DMA Control Register
0x38 MSB	SBCR	Serial Channel B Control Register
0x38 LSB	SACR	Serial Channel A Control Register

All registers are cleared upon hardware reset.

Card Control Register

The Card Control Register (CCR) provides the following functions:

Name	Access	Description
CCR[7:6]	R/O	EPLD revision level (currently 01)
CCR[5]	W/O	Reset; the FP-Serial2-422 is reset when this bit is written with a 1. Always reads as 0.
CCR[4]	R/W	1 = CMUXRFBn signal to ICD2051 is asserted (setting CCLKB to 8 MHz).
CCR[3]	R/W	1 = CMUXRFAn signal to ICD2051 is asserted (setting CCLKA to 8 MHz).
CCR[2]	R/W	CSCLKB signal to ICD2051
CCR[1]	R/W	CSCLKA signal to ICD2051
CCR[0]	R/W	CDATA signal to ICD2051

If CCR[5] is written to one, the FP-Serial2-422 should not be accessed for a minimum of 2 microseconds to allow onboard reset functions to complete.

The operation of the ICD2051 control signals is discussed in Appendix A.

DMA Control Register

The DMA Control Register (DCR) provides the following functions:

Name	Access	Description
DCR[7]	R/O	1 = 8 MHz IP clock, 0 = 32 MHz IP clock
DCR[6]	W/C	1 = DMA direction error has occurred. This bit is cleared when written with a 1.
DCR[5:4]	R/O	Unused; reads as 00.
DCR[3]	R/W	1 = Enable DMA request 1. This bit will be cleared if the carrier asserts DMAend during a DMA channel 1 acknowledge cycle.
DCR[2]	R/W	1 = Enable DMA request 0. This bit will be cleared if the carrier asserts DMAend during a DMA channel 0 acknowledge cycle.
DCR[1:0]	R/W	DMA mode as follows: 00 = RXA to DMAreq0, RXB to DMAreq1 01 = RXA to DMAreq0, TXA to DMAreq1 10 = TXB to DMAreq0, RXB to DMAreq1 11 = TXB to DMAreq0, TXA to DMAreq1

The DMA mode (DCR[1:0]) should not be changed when the DMA requests are enabled unless the associated Z16C30 REQ lines are disabled.

The DMA interface monitors the RXREQ/TXREQ outputs from the Z16C30 and generates an acknowledgement on the RXACK/TXACK inputs to the Z16C30. The Z16C30 must be configured to use these signals for DMA control prior to enabling the DMA requests.

RXREQ and TXREQ signals which are not being used are ignored by the SmartSerial controller. It is nevertheless recommended that unused REQ outputs be configured as outputs in the high (deasserted) state (Z16C30 IOCR[11:10] TxRMode set to either 01 or 11 and Z16C30 IOCR[9:8] RxRMode set to either 01 or 11).

RXACK and TXACK signals which are not being used may be configured as either general-purpose inputs to the Z16C30 or as ACK functions (Z16C30 HCR[7:6] TxAMode set to 00 or 01 and Z16C30 HDR[3:2] RxAMode set to 00 or 01). The SmartSerial controller always drives these signals.

Serial Control Registers

The Serial Control Register is divided into a Serial A Control Register (SACR) and Serial B Control Register (SBCR). The registers have similar functions with some additional capability in SBCR. Most of the following discussion refers generically to S*x*CR, which indicates SACR for channel A and SBCR for channel B.

The discussion of the S*x*CR register functions refers to a number of onboard signals which are listed below. For each signal, "*x*" may be either "A" or "B" for serial channel A or B. It may be useful to reference the block diagram on page 1 while reviewing the list of signals.

- CCLK*x*. This signal is the programmable clock output of the ICD2051. CCLK*x* is generated by the ICD2051 clock synthesizer and input to the SmartSerial EPLD.
- IRXD*x*. Input Receive Data. This signal is the TTL version of the EIA-422 RXD*x* input to the FP-Serial2-422. This signal is output by the DS34C86M EIA-422 receiver and input to the SmartSerial EPLD.
- IRXC*x*. Input Receive Clock. This signal is the TTL version of the EIA-422 RXC*x* input to the FP-Serial2-422. This signal is output by the DS34C86M EIA-422 receiver and input to the SmartSerial EPLD.
- LRXD*x*. Local Receive Data. This signal is the receive data from either IRXD*x* or the SmartSerial RXC FSM, depending on the S*x*CR configuration. This signal is output by the SmartSerial EPLD and input to the Z16C30 on the RxD*x* pin.
- LRXC*x*. Local Receive Clock. This signal is the receive clock which may be assigned to one of five sources depending on S*x*CR configuration. This signal is output by the SmartSerial EPLD and input to the Z16C30 on the /RxC*x* pin.
- LTXD*x*. Local Transmit Data. This signal is the transmit data from the Z16C30. This signal is output by the Z16C30 on the TxD*x* pin and input to the DS34C87M EIA-422 driver. The TXD*x* EIA-422 driver is enabled when LCTS*x* is high.
- LTXC*x*. Local Transmit Clock. This signal is the transmit clock and may be driven by the SmartSerial EPLD or by the Z16C30 on the /TxC*x* pin. The LTXC*x* signal is input to the DS34C87M EIA-422 driver, which is enabled when LCTS*x* is high.
- LCTS*x*. Local Clear To Send. This signal is a general-purpose output from the Z16C30 on the /CTS*x* pin. When LCTS*x* is low or tristated, the EIA-422 TXD*x* and TXC*x* drivers are disabled. When LCTS*x* is high, the EIA-422 TXD*x* and TXC*x* drivers are enabled.
- LDCD*x*. Local Data Carrier Detect. This signal is a general purpose input to the Z16C30 on the /DCD*x* pin. LDCD*x* is output by the DS34C86M EIA-422 receiver and is the TTL version of the EIA-422 DCD*x* signal.

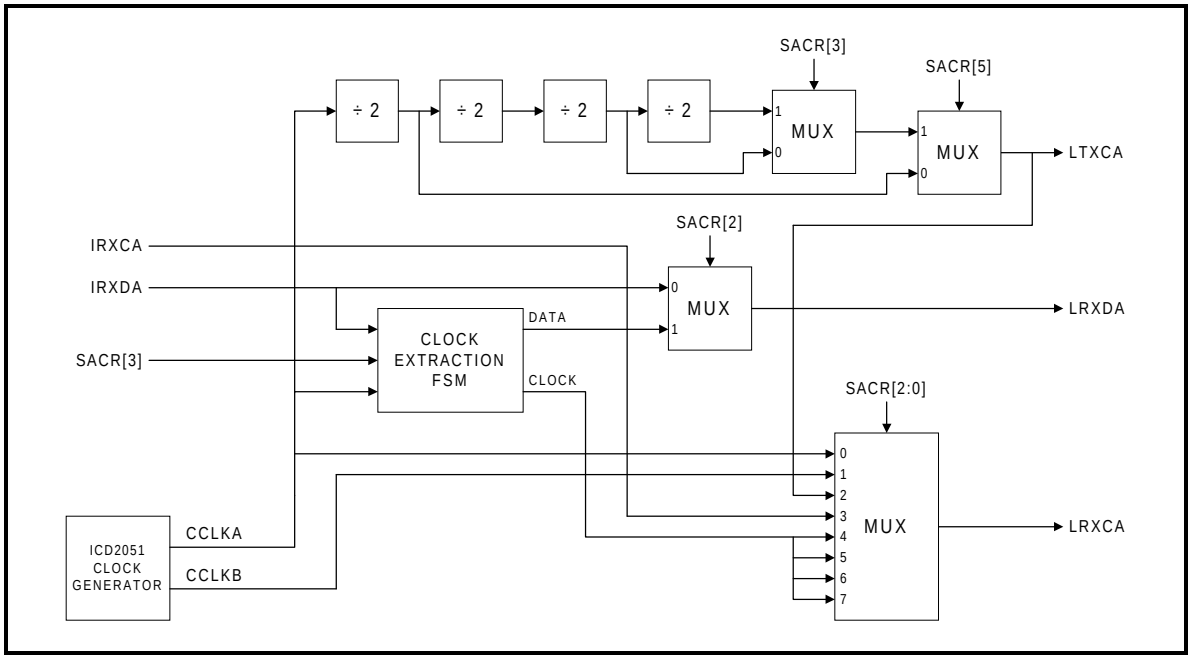
The FP-Serial2-422 design imposes the following constraints on the Z16C30 configuration:

- The RxD*x* pin should be configured as the Receive Data input to the Z16C30; the SmartSerial controller always drives this pin.
- The /RxC*x* pin should be configured as an input to the Z16C30; the SmartSerial controller always drives this pin.
- The /CTS*x* pin should be configured as an output from the Z16C30. The /CTS*x* pin should be low to disable the TXD/TXC EIA-422 drivers and high to enable the TXD/TXC EIA-422 drivers.
- The /DCD*x* pin should be configured as an input to the Z16C30.
- The TxD*x* pin should be configured as an output from the Z16C30.
- The /TxC*x* pin should be configured to be either an output from the SmartSerial EPLD (S*x*CR[6] is 1) and an input to the Z16C30, or tristated from the SmartSerial EPLD (S*x*CR[6] is 0) and an output from the Z16C30. The LTXC*x* signal should always be driven by one of the two possible sources to avoid oscillations and spurious EIA-422 TXC outputs.

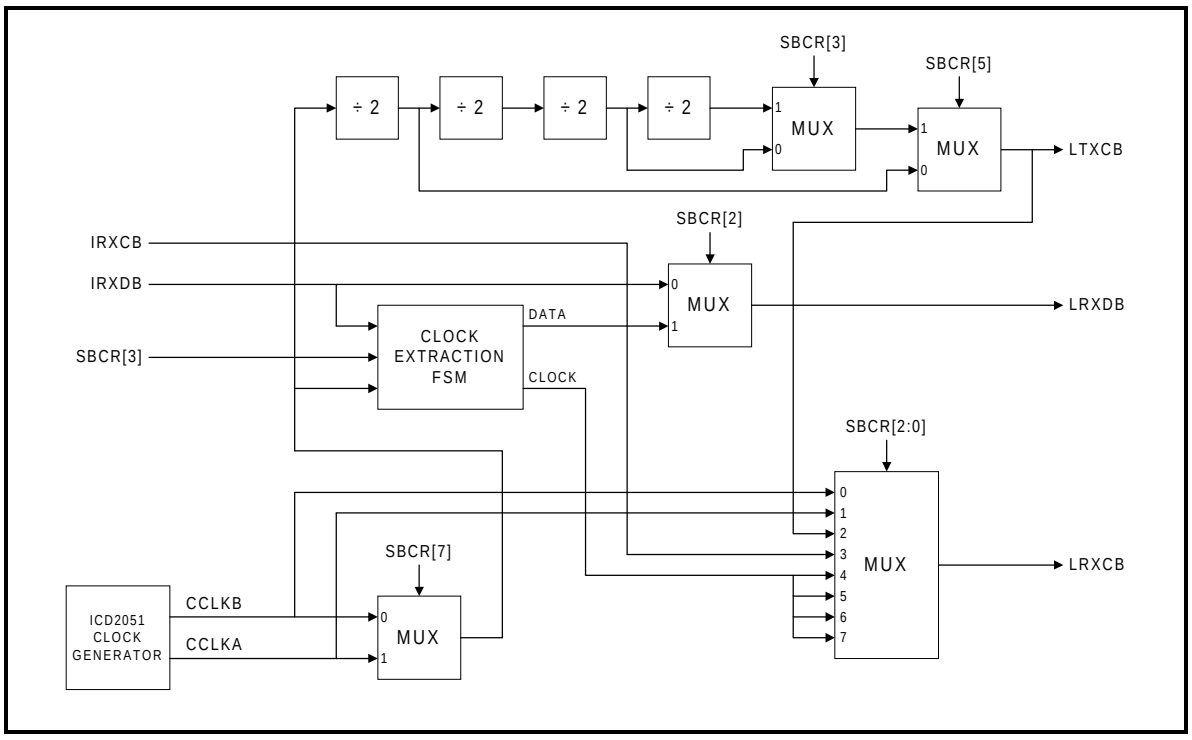
The Serial Control Register (S*x*CR) provides the following functions:

Name	Access	Description
S*x*CR[7]	R/O	SACR: Unused; reads as 0. SBCR: 0 = use CCLKB for FSM and TXC clock source; 1 = use CCLKA for FSM and TXC clock source.
S*x*CR[6]	R/W	0 = TXC*x* output tristated from EPLD; 1 = TXC*x* output enabled from EPLD.
S*x*CR[5]	R/W	0 = TXC*x* output is CCLK*x*/2; 1 = TXC*x* output is CCLK*x*/8 or 16 (depends on S*x*CR[3]).
S*x*CR[4]	R/W	FSM enable (0 = hold in reset; 1 = enabled)
S*x*CR[3]	R/W	FSM clock divider (0 = CCLK*x*/8; 1 = CCLK*x*/16). Also used to control TXC*x* if S*x*CR[5] is 1.
S*x*CR[2:0]	R/W	LRXC*x* source. 000=CCLK*x*, 001=other CCLK, 010=TXC*x*, 011=IRXC*x* (input clock), 100=FSM 7 bits, 101=FSM 8 bits, 110=FSM 9 bits, 111=FSM 10 bits.

A block diagram of the Channel A signal flow (controlled by SACR) is shown below.



A block diagram of the Channel B signal flow (controlled by SBCR) is shown below. The only difference between channel A and B is the addition of a CCLKA vs. CCLKB multiplexer prior to the Clock Extraction FSM.



Interrupt Space

The FP-Serial2-422 maps the Z16C30 channel A interrupt to IP interrupt request 0 and the channel B interrupt to IP interrupt request 1. When an interrupt is acknowledged by the IP carrier, the appropriate interrupt vector is read from the Z16C30. The user is required to configure the Z16C30 to respond to interrupts with a vector (i.e. ICR[13] must be zero). The user may enable or disable the vector-includes-status option.

The Z16C30 interrupt daisy chain is not used; prioritization may be performed by the IP carrier between interrupt requests 0 and 1 if necessary.

DMA I/O Space

The FP-Serial2-422 accepts four possible DMA request inputs from the Z16C30 (RXREQA, TXREQA, RXREQB, and TXREQB) and maps two of the four requests to IP DMA requests 0 and 1. The mapping from Z16C30 request to IP DMA request is determined by DCR[1:0]. The supported options include both RX channels, both TX channels, RX and TX for channel A, and RX and TX for channel B.

When a DMA I/O cycle is performed, an appropriate ACK signal is generated (i.e. if RXREQA generates IP DMA request 0 and a DMA I/O cycle is performed in response to request 0, RXACKA will be asserted for the DMA I/O cycle). If the DMA I/O cycle has the wrong direction, the DCR[6] bit is set to indicate a DMA direction error. This would typically indicate a software error in programming either the FP-Serial2-422 or the IP carrier's DMA controller.

DMA I/O cycles are always 16 bits wide. The user is required to ensure that the DMA request level is a minimum of 1 and that the WordStatus bit (RICR[3]) is set.

If the IP carrier asserts DMAend during a DMA I/O cycle, the DMA request level being acknowledged is disabled (DCR[3] or DCR[2] is cleared, depending on the request being acknowledged). Typically, the IP carrier DMA controller will also generate an interrupt to have the host processor configure the next DMA transfer. The FP-Serial2-422 never drives the DMAend signal.

Optional Accessories

The FP-Serial2-422 is supported by the following optional accessories:

Part Number	Description
13460-3	Cable Assembly, FP-Serial2-422 50-pin 25x2 I/O to dual D9S, 3 feet
13461-3	Cable Assembly, FP-Serial2-422 50-pin 25x2 I/O to dual D15S, 3 feet
13462-1	Plug, Loopback, D9P
13463-1	Plug, Loopback, D15P
13464-3	Cable Assembly, FP-Serial2-422 D9P null modem, 3 feet
13465-3	Cable Assembly, FP-Serial2-422 D15P null modem, 3 feet
13681-1	FP-Serial2-422 Starter Kit Includes Zilog Z16C30 documentation and data sheets for other FP-Serial2-422 components Includes the following cabling: one D15S breakout cable, two D15P loopback plugs, and one D15P null modem cable Includes FastPack driver kit with FP-Serial2-422 drivers. ANSI C source code for all software is included. Includes MVME162/162FX Test Software EPROM
13682-1	MVME162/162FX Test Software (EPROM)

Software drivers and sample application software may be requested from TEK's technical support department.

Appendix A:
Cypress ICD2053 Clock Synthesizer

The FP-Serial2-422 uses a Cypress ICD2051 dual clock synthesizer to generate two independent bit rate clocks designated CCLKA and CCLKB. These clocks are used by the SmartSerial controller to generate RXC and TXC clocks for the Z16C30.

The ICD2051 generates the bit rate clocks using an 8 MHz reference clock. The reference clock is generated from the IP clock by the SmartSerial controller. The 8 MHz clock uses either the IP clock itself (at 8 MHz) or divides the IP clock by 4 (at 32 MHz), depending on the IP clock rate.

The ICD2051 is configured by downloading a 22-bit control word for each clock output. The ICD2051 control signals are listed below; most of the control signals are directly generated by Card Control Register bits.

ICD2051 Signal	CCR	Function
MUXRFBn	CCR[4]	If CCR[4] is high, the MUXRFBn signal is asserted. When asserted, CCLKB is set to the reference clock (8 MHz). When deasserted, CCLKB is set to the synthesized clock. Transitions are guaranteed to be glitch-free.
MUXRFAn	CCR[3]	Same as MUXRFBn, but for CCLKA.
CSCLKB	CCR[2]	When a low-to-high edge occurs on this signal, the CDATA state is clocked into the CCLKB control word.
CSCLKA	CCR[1]	Same as CSCLKB, but for CCLKA.
CDATA	CCR[0]	Provides serial data for CSCLK*x* rising edge.

The procedure for clocking a 22-bit control word into the ICD2051 is shown below. The procedure assumes that CCLKA is being configured.

1. Assert the MUXRFAn signal by writing a 1 to CCR[3].
2. Write the CDATA bit to the desired value by writing CCR[0]. The first bit is the LSB of the 22-bit control word.
3. Set the CSCLKA high by writing a 1 to CCR[1].
4. Read the CCR.
5. Set the CSCLKA bit low by writing a 0 to CCR[1].

6. Read the CCR.
7. Repeat steps 2 through 6 for each of the 22 bits of the control word.
8. Wait the ICD2051 settling time (10 milliseconds).
9. Deassert the MUXRFAn signal by writing a 0 to CCR[3].

The following C language routine will perform this operation:

```
#define CCR_MUXRFB   (1 << 4)
#define CCR_MUXRFA   (1 << 3)
#define CCR_CSCLKB   (1 << 2)
#define CCR_CSCLKA   (1 << 1)
#define CCR_CDATA    (1 << 0)

void icd2051_cfg (volatile WORD8 *ccr, WORD32 cvalue)
{
      int i;

      *ccr |= CCR_MUXRFA;              /* Assert MUXRFAn */
      for (i = 0; i < 22; i++) {
            *ccr &= ~CCR_CDATA;        /* Clear CDATA */
            if (cvalue & 1)
                  *ccr |= CCR_CDATA;   /* Set CDATA */
            *ccr |= CCR_CSCLKA;        /* Set CSCLKA */
            *ccr;                      /* Use 2 IP clks */
            *ccr &= ~CCR_CSCLKA;       /* Clear CSCLKA */
            *ccr;                      /* Use 2 IP clks */
            cvalue >>= 1;              /* Setup next bit */
            }
      /* Insert code to wait 10 ms */
      /* Or, read CCR 106667 times (32 MHz / 3 x 10 ms) */
      for (i = 0; i < 106667; i++) *ccr;

      *ccr &= ~CCR_MUXRFA;       /* Deassert MUXRFAn */
}
```

The "Read CCR" steps are required to ensure minimum CSCLKA low and high times. Because the ICD2051 reference clock is derived from the IP clock, the minimum times are guaranteed by reading the CCR once for each CSCLKA state.

PC-based software to generate 22-bit control words for arbitrary output frequencies may be downloaded from Cypress's Web site (http://www.cypress.com).

Note that CCLKA and CCLKB should not be configured to generate the same frequency or to run the internal ICD2051 PLL at the same frequency due to harmonic constraints. If serial channels A and B are required to use the same frequency, the serial channels should both be configured to operate from CCLKA and CCLKB should be set to a different frequency.

Appendix B:
Non-Standard IP Clock Frequencies

The ANSI/VITA 4-1995 specification allows the IP clock signal to operate at either 8 or 32 MHz. Some carrier cards have the ability to operate at other clock frequencies. For example, the Motorola MVME162-4xx series has a 25 MHz 68040 processor and the IP interface controller can operate at either 8 or 25 MHz. Operation at 25 MHz does not conform to the IP specification, but may be desirable if the user assesses the risks involved.

This Appendix discusses the performance of the FP-Serial2-422 when using a non-standard IP clock frequency. These performance characteristics may be changed with future revisions of the card.

There are several implementation areas where the FP-Serial2-422 is affected by the IP clock frequency:

- The SmartSerial controller has a clock speed detection circuit which is used during reset to configure the controller in either "low" or "high" frequency mode. The mode may be checked by reading the DCR[7] bit, which is set to one if the SmartSerial controller is in 8 MHz (low frequency) mode.
- The number of wait states for bus cycles is determined by the SmartSerial controller based on the mode. When in low frequency mode, the SmartSerial controller generates wait states for an 8 MHz bus interface. When in high frequency mode, the SmartSerial controller adds additional wait states to support a 32 MHz bus interface. Because extra wait states do not cause improper operation (other than running slower than desired), the wait state generator in low frequency mode is valid for any frequency up to 8 MHz and the wait state generator in high frequency mode is valid for any frequency up to 32 MHz.
- The ICD2051 reference clock is driven by the IP clock (in low frequency mode) or by the IP clock divided by four (in high frequency mode).

At non-standard frequencies, the user should ensure that the FP-Serial2-422 is operating in high frequency mode. If the FP-Serial2-422 is in low frequency mode, it may not generate sufficient wait states for bus cycles at the actual operating frequency. This condition could result in erratic operation.

The clock detection circuit is guaranteed to operate as follows:

Frequency	FP-Serial2-422 Mode
Between 8 and 15.1 MHz	Low frequency mode. Wait states set for 8 MHz operation. ICD2051 reference clock driven by IP clock.
Between 15.1 and 25.7 MHz	May be set to low or high frequency mode on reset. Operation will be consistent with mode specified by DCR[7] until another reset occurs.
Between 25.7 and 32 MHz	High frequency mode. Wait states set to 32 MHz operation. ICD2051 reference clock driven by IP clock divided by four.

Because the FP-Serial2-422 is not guaranteed to select high frequency mode at 25 MHz, operation with an IP clock frequency of 25 MHz is not recommended.