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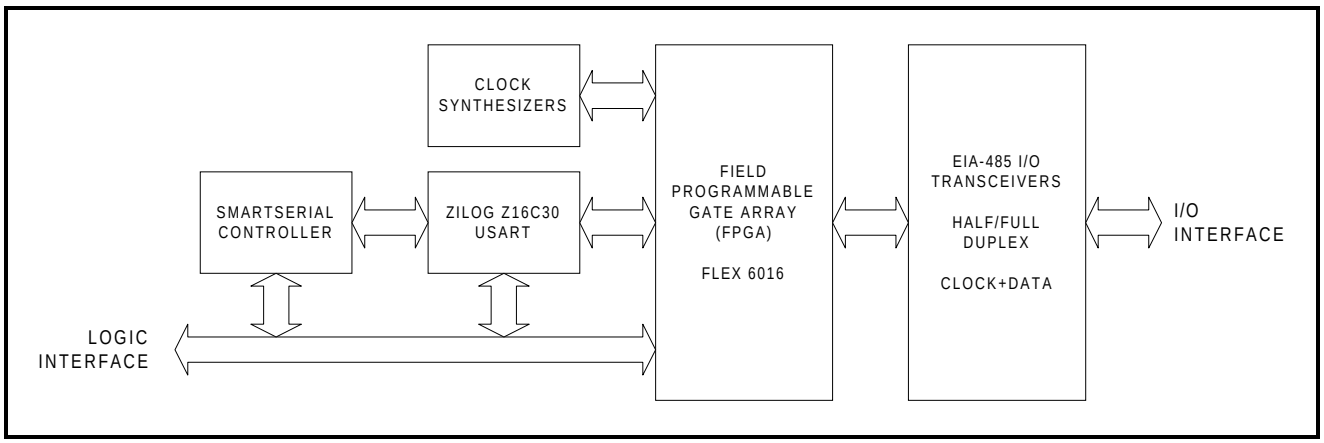
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Find the *Tek Microsystems FP-Serial2flex-485* at our website: *Click HERE*

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FP-Serial2*flex*-485



FP-Serial2*flex*-485 Block Diagram

Description

When you need the highest possible serial I/O performance along with unmatched flexibility, TEK's FP-Serial2*flex*-485 is ready to be put to work.

The FP-Serial2*flex* starts with a Zilog Z16C30, one of the most versatile USART chips available today. The Z16C30 includes 32-byte Transmit and Receive FIFOs for each channel, flexible interrupts and built-in DMA support, along with hardware support for character and message based protocols ranging from simple asynchronous communications to synchronous protocols such as SDLC, HDLC and Bisync.

In addition to the capabilities of the Z16C30, the FP-Serial2*flex* adds features like dual PLL-based clock synthesizers for exact baud rate generation and TEK's SmartSerial controller for the highest possible IP bus performance at both 8 and 32 MHz.

Finally, the FP-Serial2*flex* adds a customizable FPGA between the Z16C30 and the external EIA-485 interface, providing unmatched power and flexibility. Standard FPGA programs are available to extend the Z16C30's capabilities, or you can use TEK's engineering toolkit to develop custom logic programs for your specific requirements.

Like all FastPack products, each FP-Serial2*flex*-485 comes with a 30-day satisfaction guarantee, unlimited technical support, and a 3 year limited warranty.

Key Features/Benefits

Feature	Benefit
Fully compliant with ANSI/VITA-4 specification	Interoperable with all IP carriers at both 8 and 32 MHz
Built around Zilog Z16C30	Easily supports most common protocols, including async, SDLC/HDLC, Bisync and others
PLL-based clock synthesizer for each channel	Supports exact generation of arbitrary baud rates, even at high data rates
Customizable FPGA logic	Supports custom logic for data encoding/decoding, synchronization or framing
Off-the-shelf FPGA program for Z16C30 DPLL emulation	Supports all Z16C30 data encoding modes at baud rates up to 5 Mbps without an external clock
Free demonstration logic programs and software available from TEK	Rapid "drop-in" integration into your application

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FP-Serial2*flex*-485

Specifications

Bus Interface	ANSI/VITA 4-1995 and IndustryPack compatible
Clock Speed	8 or 32 MHz, auto sensing
Size	Single-size, Type I (1.8" x 3.9" x 0.314" max)
Address Spaces	ID (8-bit data), I/O (16-bit data)
Number of Channels	Two
Serial Data Rate	10 Mbps with external clock 5 Mbps without external clock
Interrupt Sources	Autovectored, one source per channel
DMA Sources	Channel A RX/TX Channel B RX/TX Channel A and B RX Channel A and B TX
Logic Capacity	Altera EPF6016, 16K gates
Operating Frequency	40-50 MHz, depending on logic program
Power Requirements	+5 Volts, 420 mA
Operating Temperature	0 to +70 degrees C -40 to +85 degrees C available by special order
Storage Temperature	–40 to +85 degrees C

I/O Pinout:

I/O Pin	Signal Name	Direction
1	TXD1+	To/From FP
2	TXD1–	To/From FP
3	TXC1+	To/From FP
4	TXC1–	To/From FP
5	RXD1+	To FP
6	RXD1–	To FP
7	RXC1+	To FP
8	RXC1–	To FP
9-10	GND	
11	DCD1+	To FP
12	DCD1–	To FP
13-16	GND	
17	TXD2+	To/From FP
18	TXD2–	To/From FP
19	TXC2+	To/From FP
20	TXC2–	To/From FP
21	RXD2+	To FP
22	RXD2–	To FP
23	RXC2+	To FP
24	RXC2–	To FP
25-26	GND	
27	DCD2+	To FP
28	DCD2–	To FP
29-32	GND	
33-50	N/C	

Ordering Information

FP-Serial2*flex*-485 **Two channel EIA-485 Serial I/O Interface with customizable FPGA logic**

Includes development kit, sample logic programs, and demonstration software at no additional cost. Development of new custom logic programs requires Altera's MAX+Plus II software.

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