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Instruction Manual

Tektronix

GTS1063 & GTS1250
GBIC Test Systems

071-0568-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Wear Eye Protection. Wear eye protection if exposure to high-intensity rays or laser radiation exists.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

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Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



CAUTION
Refer to Manual



Double
Insulated



Protective Ground
(Earth) Terminal



Laser Source

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Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

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Product Support	For questions about using Tektronix measurement products, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Tektronix offers extended warranty and calibration programs as options on many products. Contact your local Tektronix distributor or sales office. For a listing of worldwide service centers, visit our web site.
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. 14200 SW Karl Braun Drive Beaverton, OR 97077 USA
Website	Tektronix.com

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Preface

This is the Instruction Manual for the GTS1063 and GTS1250 GBIC Test Systems. This manual provides user information and information to troubleshoot and repair the instrument to the module level.

Related Manuals

Additional documentation for your GBICs is contained in manuals supplied by the GBIC manufacturer.

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Getting Started

The GTS1063 and GTS1250 GBIC Test System are tools for GBIC (Gigabit Interface Converter) designers and users (GTS1250 for gigabit ethernet and the GTS1063 for fibre channel) that provide a quick, consistent, and reliable platform for supporting GBIC transceivers in a number of required applications.

The GBIC Test System provides a trap door into which you can plug a standard GBIC. The front panels with a GBIC installed are shown in Figure 1. A GBIC is an industry standard module that converts input digital electrical signals (ECL) to optical amplitude modulation outputs and accepts optical amplitude modulation signals as input and converts them to digital electrical signals (ECL).

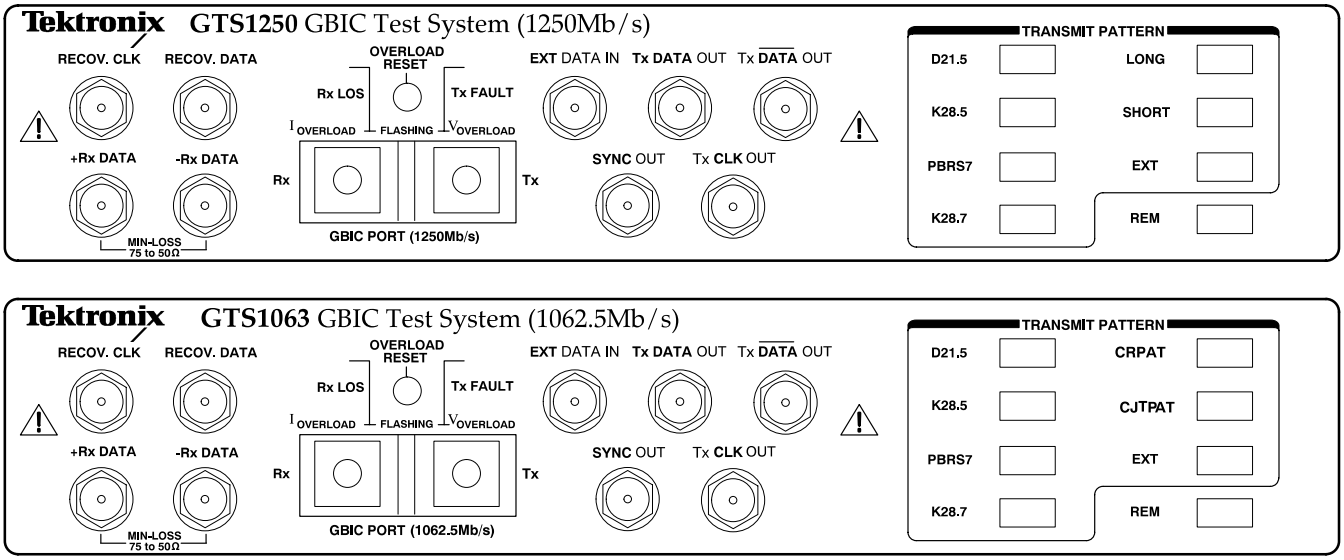


Figure 1: GTS1063 and GTS1250 Front Panels

The GBIC Test System provides industry standard 1.25 Gb/s (GTS1250) or 1.0625 Gb/s (GTS1063) digital signals to drive your GBIC transmitter (plugged into the receptacle) for test purposes; you can also drive your GBIC transmitter using external patterns. The GBIC Test System provides electrical data outputs and optionally performs serial clock recovery of the received GBIC signal (for additional information on these and other outputs and inputs see *Operating Basics* starting on page 9)

The GBIC Test System provides the following key features:

- Transmit differential data out

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- Transmit clock out
- Transmit sync pulse out at the data frame rate
- Receive differential data out
- Recovered clock out (Option 01 only)
- Recovered data out (Option 01 only)
- Buffered receive data out (standard instrument only)
- Provides industry standard digital transmit test patterns: D21.5, PRBS7, K28.7, K28.5, LONG (GTS1250), SHORT (GTS1250), CRPAT (GTS1063), and CJTPAT (GTS1063)
- Accepts external data to drive a GBIC
- Accepts external or internal full rate serial clock
- Receives data from a GBIC
- Accepts industry standard gigabit serial data GBICs: this makes the GTS1250 and GTS1063 useful in multimode, single-mode, short wavelength, long wavelength, and even metallic twisted pair (copper) applications
- Bit Error Rate Testing of gigabit serial data links: acts as an electrical-to-optical (E-O) transducer and an optical-to-electrical (O-E) transducer for Bit Error Rate Test (BERT) instruments
- Provides a cost effective, stand-alone stimulus for testing, demonstrating, and developing O-E related time-domain waveform instruments (that is, oscilloscopes with internal or external optical front-ends)
- Supplies a stand-alone optical and electrical gigabit serial data Tx source: deterministic jitter measurements, random jitter measurements, eye-pattern testing, and so forth
- Diagnostic tool for GBIC functionality tests: Tx failure and Rcv Loss-of-Signal (LOS)
- The differential receive signals from the GBIC host side connector often require mask testing for compliance; the built-in 75–50 Ω min-loss conversion network allows you to easily attach a 50 Ω oscilloscope or attach a 50 Ω input test device for such testing.

For a complete list of specifications, see page 29.

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Options

Tektronix will ship the options shown in Table 1.

Table 1: Options

Option	Description
01	Serial clock recovery (1.250 Gb/s only on GTS1250 and 1.0625 Gb/s only on GTS1063)
A1	European power cord
A2	UK power cord
A3	Australian power cord
A5	Swiss power cord
AC	Chinese power cord
A99	No power cord
C3	Three years of calibration
D1	Calibration data
D3	Three years of calibration data
R3	Three years of extended warranty

Standard Accessories

The GBIC Test System comes standard with the following accessories:

Table 2: Standard Accessories

Accessory	Part number
Instruction manual	071-0568-00
Certificate of Calibration	——
US power cord	161-0066-00

For a list of replaceable part numbers, see page 77.

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Optional Accessories

Table 3 list optional accessories recommended for the GBIC Test System.

Table 3: Optional Accessories

Accessory	Part number
IBM 850 nm multimode 1.25 Gb/s GBIC[1]	119-6112-00
IBM 1310 nm single-mode 1.25 Gb/s GBIC[1]	119-6113-00
Side-By-Side Instrument Rack Adapter	TVGF13

1 **GBIC functions as well at the lower 1.0625 GB/s rate.**

For a list of part numbers, see page 77.

Installation

To learn how to install, access the front panel, power on, and power off the GBIC Test System, do the following procedures:

Preparation

To properly install and power on the GBIC Test System, do the following steps:

1. Be sure you have the appropriate operating environment. Specifications for temperature, relative humidity, altitude, vibrations, and emissions are included in the Table 14 starting on page 37.



CAUTION. *To prevent damage to your GBIC, provide proper ventilation. Do not block the cabinet ventilation holes, or disable the fan. Do not remove the cabinet feet, they provide proper clearance for ventilation.*

2. Leave space for cooling. Do this by verifying that the ventilation holes on the sides, top, and bottom of the cabinet are free of any airflow obstructions. Leave at least 5.1 cm (2 inches) free on each side.



WARNING. *To avoid electrical shock, be sure that the power cord is disconnected before checking or replacing the fuse.*

3. The internal AC input to the power supply is protected with a 250V, 3.15 A(Fast) fuse. This fuse is only accessible by service personnel (see *Fuse Removal and Replacement* on page 73).

4. Check that you have the proper electrical connections. The GBIC Test System requires 100 to 240 VAC_{RMS} ±10% 47 Hz to 63 Hz, and 60 W.

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5. Connect the proper power cord from the rear-panel power connector (see Figure 6 on page 16) to the power system.

Installing a GBIC

The GBIC Test System is designed to aid in the testing of 1250 Mb/s (GTS1250) or 1.0625 Gb/s (GTS1063) Gigabit Interface Converter (GBIC) modules (see Figure 2). The GBIC Test System accepts industry standard GBIC modules in a front-panel receptacle. A brief description of a GBIC module follows:



WARNING. *To prevent personal injury, only use industry standard GBICs that comply with FDA and IEC825-1 safety standards. The optional accessory GBICs available with the GBIC Test System meet Class 1 laser safety standards 21 CFR part 1000, & EN60825.*

You can use one of several versions of transceivers in completing a link. Short wavelength (780 nm, 850 nm) multimode optical transceivers are cost effective and capable of spanning 550 m on quality fibers. Single-mode long wavelength (1310 nm, 1550 nm) optical transceivers are similar to those used by SONET/SDH telecom public networks, and are capable of spanning 10 kilometers. Metallic twisted pair cables with absolutely no optics are sufficient for many short (75 m) links and require even lower implementation cost. All of these transceivers can be easily interchanged due to the GBIC standard.

A GBIC has a standard electrical interface on one end which passes differential serial ECL or PECL electrical signals at the full Gigabit Ethernet (1.25 Gb/s) or Fibre Channel (1.0625 Gb/s) rate. This interface and the mechanical design to allow plug-and-play provide the network designer a quick way to custom select the type of transceiver that economics or physical limitations require for any particular data link.

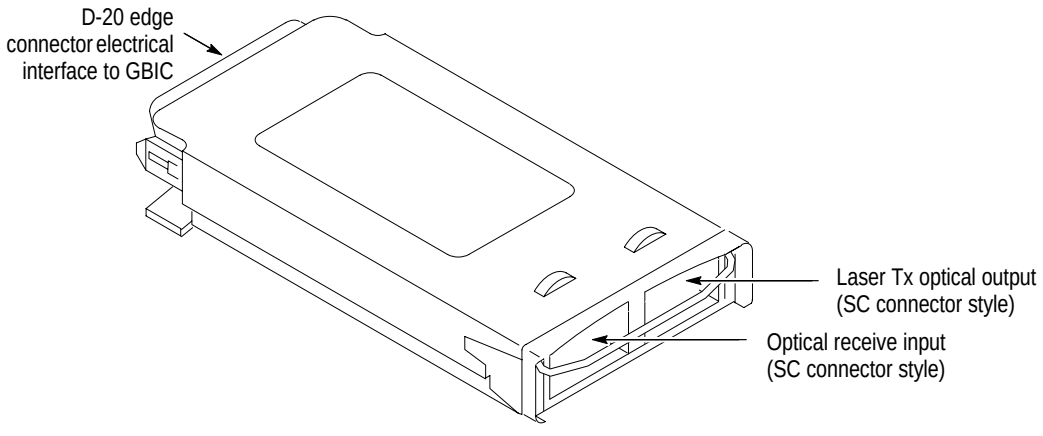


Figure 2: A GBIC example

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To install a GBIC, use Figure 3 as a guide while performing the following steps:

1. If your GBIC contains a removal bail, move the bail up to unlock the GBIC.
2. With the top of the GBIC facing up and the GBIC D-20 connector to the rear, insert the GBIC into the front-panel GBIC receptacle. The GBIC, when properly installed, will have its transmit output connector on the right side of the GBIC receptacle (looking at the front of the instrument).
3. Press the GBIC into the front panel until it locks into place.

NOTE. *Some GBICs contain a removal bail that aids installation and removal of the GBIC. Other GBICs only contain a removal lever.*

4. If your GBIC contains a removal bail, move the bail up prior to installation, then down after installation to lock the GBIC in place.

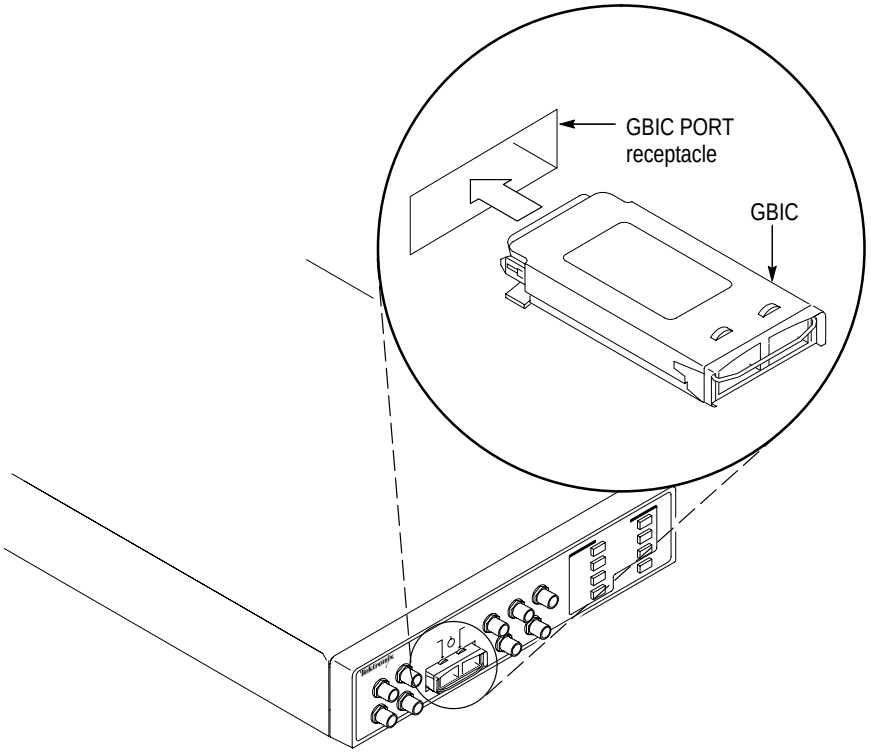


Figure 3: GBIC Test System with zoomed GBIC receptacle

Power on

To power on the GBIC Test System, push the rear-panel power switch to toggle it on (see Figure 6).

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Power up defaults

To be compatible with ATE test systems, the GBIC Test System defaults to REM mode enabled at power on. Therefore, in an automatic program environment, the GBIC Test System does not require any button pushes when the test system powers up. The pattern selected in this initial power up mode is that which is determined by the TTL assertion state at the rear remote connector at time of power up.

If not in an automatic program environment, press the button for the pattern you want to transmit.

To exit REM mode from the front panel, push any other button.

Power off

To power off the GBIC Test System, toggle the power switch.

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Operating Basics

Figure 4 on page 10 shows the front panels of the GBIC Test Systems. The GBIC Test System has a receptacle for your GBIC. Connectors for received data and recovered clock, transmitted data, clock, and sync out, and external data inputs are included on the front panel. Jitter and EXT clock inputs are on the rear panel.

Handling

Handle the GBIC Test System carefully at all times.



WARNING. *To prevent eye injury, do not look directly into any optical output port. Laser light can be harmful to your eyes.*

Connecting Signals

The GBIC Test System uses SMA connectors. Never attach a cable if the cable has a worn or damaged connector because the GBIC Test System connector may become damaged as well.

Use extra care when attaching or removing a cable from the connectors. Turn only the nut, not the cable. When attaching a cable, align the connectors carefully before turning the nut. Use light finger pressure to make this initial connection. Then tighten the nut lightly with a wrench.

For best repeatability and to prolong the life of both connectors, use a torque wrench and tighten the connection to the range of 79 to 112 N-cm (7 to 10 lb-in).

If the connectors will receive heavy use, such as in a production environment, you should install adapters (for example, connector savers) on the GBIC Test System to make connections to the device under test.

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Front Panel

The GBIC Test System user interface is almost entirely dedicated to the selection of the outgoing transmit pattern. A rear-panel TTL interface allows remote control of instrument.

All control buttons, input and output SMAs (except the jitter and external clock inputs), the GBIC receptacle, and the status indicators are on the front panel. The front panels are shown in Figure 4.

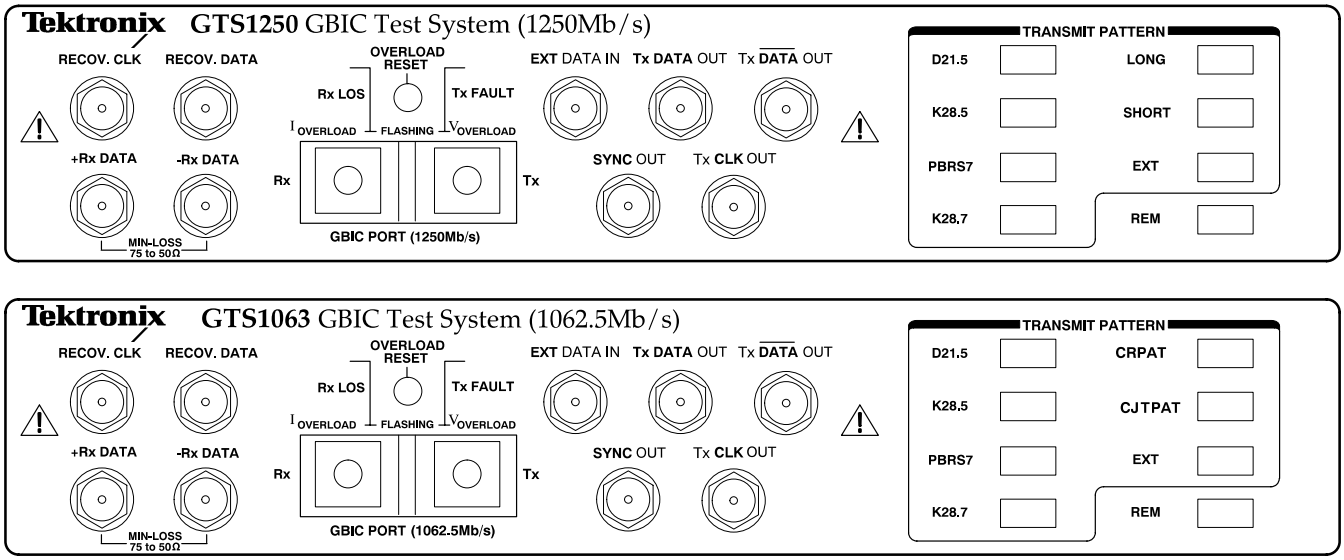


Figure 4: The GTS1063 and GTS1250 front panels

Selecting the Transmit Pattern

A GBIC has a transmit and receive side. The front-panel connectors and buttons are grouped to the side of the GBIC they are associated with. When properly installed, the GBIC transmit output connector is on the right side of the GBIC receptacle (looking at the front of the instrument). All the connectors on the right side of the GBIC receptacle are associated with transmitter signals. All connectors on the left side of the GBIC receptacle are associated with receive signals.

All front-panel buttons (except for the REM and RESET button) select the transmit output pattern. Only one pattern is active at a time. The abbreviated description of the currently selected and active transmit pattern is illuminated. When the external clock is enabled, by activating a control signal on the REMOTE INTERFACE, the front panel EXT indicator blinks.

To select a transmit pattern, press the button next to the desired transmit pattern.

The REM button selects remote control of the GBIC Test System. When this button is pushed, the rear-panel TTL interface (see *Remote Interface* on page 17)

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selects the transmit pattern. When the front-panel lock signal is activated on the REMOTE INTERFACE, the REM indicator blinks.

Transmit Patterns

All patterns except PRBS7 are defined in the IEEE 802.3 Annex 36A, 1998 standard (GTS1250) or the T11.2/Project 1230/Rev 7 Fibre Channel — Methodologies for Jitter Specification standard (GTS1063). These patterns are described by the IEEE standard as jitter test patterns. This section describes each transmit pattern.

D21.5. This is a high frequency test pattern. This pattern is a continuous 1010101010 output at 1.25 Gb/s that is equivalent to a 625 MHz square wave (GTS1250) or 1.0625 Gb/s that is equivalent to a 531.25 MHz square wave (GTS1063). This pattern is often referred to as the high-frequency Random Jitter test pattern. The IEEE 802.3 D21.5 code-group character is a 1010101010. Use this test pattern to measure the random jitter of the transmit signal.

PRBS7. This is a pseudo random test pattern. This pattern is a repeating binary string with a total bit length of 127 (equivalent to 2^7–1). This provides every possible 7-bit series of bit combinations except the all 1s state (the longest string of consecutive bits in such a pattern is therefore seven). Many bit-error-rate testers lock on PRBS patterns such as PRBS7 to measure error ratios. Note that the gigabit ethernet and fibre channel standards use an 8B/10B encoding scheme such that the longest string of consecutive 1s or 0s possible is only five; for this reason the PRBS7 pattern may exhibit more data-dependent jitter on the outgoing transmit signal than a GBIC in an actual 1.25 or 1.0625 Gb/s network.

K28.7. This is a low-frequency test pattern. The pattern is a continuously repeating 1111100000 output at 1.25 Gb/s that is equivalent to a 125 MHz square wave (GTS1250) or 1.0625 Gb/s that is equivalent to a 106.25 MHz square wave (GTS1063). This pattern is often referred to as the low-frequency Random Jitter test pattern. In addition to measuring random jitter (RJ), the pattern is used to test GBIC rise and fall times. The IEEE 802.3 special code-group character K28.7 negative disparity is 0011111000. This pattern, repeated back-to-back, produces a pattern of five 1s followed by five 0s. Since the ending disparity of this character is negative, the K28.7 code-group repeated always transmits the negative disparity version of K28.7.

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K28.5. This is a mixed frequency test pattern. This pattern is intended to contain a combination of both high frequency and low frequency patterns, and therefore combine random jitter effects with deterministic jitter. (Deterministic jitter is horizontal timing jitter of the data edges due to different patterns; asymmetry in transmitters will exhibit noticeable deterministic jitter.) Use this signal to make deterministic jitter measurements by averaging this signal to remove the random jitter. For this pattern, the IEEE 802.3 (GTS1250) or Fibre Channel (GTS1063) special code-group character K28.5 is used. The K28.5 negative disparity 10-bit character (0011111010) is followed by the K28.5 positive disparity 10-bit character (1100000101). The two 10-bit patterns are logical inversions of each other. The K28.5 character ends with the opposite disparity that it begins with. Thus the character repeated alternates between the two disparity versions of itself.

LONG (GTS1250)**.** This is a complex continuous pattern for system jitter measurements. The frequency spectrum content of this pattern is broad with minimal peaking. The pattern is a valid packet of GBE data with full encapsulation rules obeyed. The length of the pattern prior to 8B/10B encoding is 1536 bytes. (After 8B/10B encoding, the 1536 8-bit bytes would produce 1536 10-bit sequences, and therefore a total bit length of 15,360 bits.) The IEEE 802.3 standard defines the pattern prior to 8B/10B encoding, but the GTS1250 actually transmits the 10B serial version adhering to both encapsulation and running disparity rules.

The 8B/10B encoding and subsequent encapsulation of the packet is listed down to the bit level in Appendix A on page 83.

CRPAT (GTS1063)**.** This Compliant Random Pattern is a complex continuous pattern for system jitter measurements. The frequency spectrum content of this pattern is broad with minimal peaking. The pattern is a valid Fibre Channel data frame with full encapsulation rules obeyed.

The 8B/10B encoding and subsequent encapsulation of the packet is listed down to the bit level in Appendix B on page 87.

SHORT (GTS1250)**.** This is a complex continuous pattern for system jitter measurements. This pattern is similar to the LONG pattern, but with a shorter loop length of the RPAT sequence. There are 372 8-bit bytes in the encapsulated packet. (This produces a total bit length after 8B/10B encoding of 3720.)

The 8B/10B encoding and subsequent encapsulation of the packet is listed down to the bit level in Appendix A on page 83.

CJTPAT (GTS1063)**.** This Compliant Jitter Tolerance Pattern is a complex continuous pattern for system jitter measurements. The frequency spectrum

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content of this pattern is intended to contain worst case large instantaneous phase jumps. The pattern is intended to be a valid Fibre Channel data frame with full encapsulation rules obeyed.

The 8B/10B encoding and subsequent encapsulation of the packet is listed down to the bit level in Appendix B on page 87.

EXT. This button selects the signal applied to the EXT DATA IN connector. The external signal is digitally received (ECL AC coupled levels) and used to drive the GBIC differential transmitter. In this mode, you can apply an arbitrary pattern at any rate (see *Data rates, minimum and maximum* on page 31 for the range of rates) up to the bandwidth limit of the GBIC (that is, you can drive the GBIC at other data rates using an external pattern generator).

Receive Signals

This section describes each receive-side signal.

Recov. DATA OUT (recovered data). This output provides a 50 Ω, AC-coupled, ~ECL/2 level signal from the GBIC Rx differential data signal. With the Clock Recovery option, this signal is a digitally buffered and retimed signal synchronous with the serial recovered data. Without serial clock recovery, this signal is a digitally buffered signal of the GBIC Rx differential signal without any retiming. The polarity of this signal matches the differential polarity of the GBIC receiver.

Recov. CLK. This output is a 1.25 GHz (GTS1250) or 1.0625 GHz (GTS1063) clock signal synchronous with the incoming data signal. This clock is only available with Option 01. The Rx receive data from the GBIC is buffered and routed to the serial clock recovery circuit. The clock recovery circuit is tuned for receiving 1.25 Gb/s (GTS1250) or 1.0625 Gb/s (GTS1063) NRZ data signals within a narrow window around this data rate (see *Lock range* on page 34 for the minimum and maximum supported offset). If no signal is present (or no GBIC installed), that is when the Rx LOS status signal is active, this output is disabled to reduce noise. YOu can defeat this output by grounding the TX_LOS signal on the rear-panel Remote Interface.

NOTE. *To allow the recovered clock and recovered data to work properly, terminate the +Rx DATA and –Rx DATA outputs at all times, even when not in use. If the external +Rx DATA and –Rx DATA outputs are not properly terminated coaxially (or with SMA 50 Ω cap terminations) to 50 Ω DC, then severe impedance mismatch reflections distort the digital data pickoff.*

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+Rx_DATA and –Rx_DATA. These outputs are analog 50 Ω connections to the actual –Rx_DATA and +Rx_DATA signals from the GBIC. The received signal in standard GBIC modules is a 75 Ω differential signal. To allow these signals to easily connect to 50 Ω oscilloscopes, each of the 75 Ω signals is converted to 50 Ω by a 75-to-50 Ω MIN-LOSS passive electrical circuit.

These connectors may also be used as inputs. For information on using these connectors as inputs see *Appendix C: Recovering a Clock from an External Electrical Signal* on page 91.

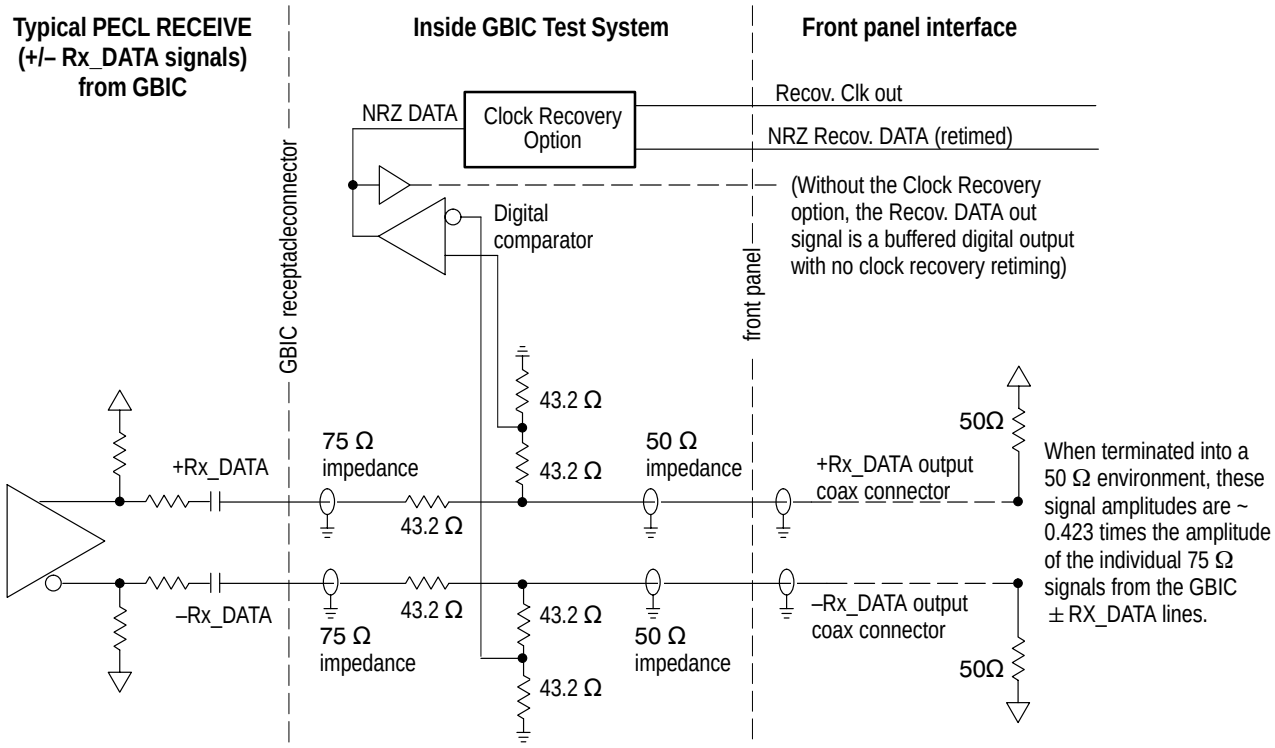


Figure 5: Rx_DATA Min–Loss Signal, Recovered Clock, and DATA paths

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Transmit Signals

This section describes each transmit-side signal.

Tx DATA and Tx $\overline{\text{DATA}}$ OUT. These 50 Ω, AC coupled, ~ECL/2 level signals match what is being sent to the GBIC transmitter. Digital polarity is maintained with the digital differential polarity of the signal being sent to the GBIC.

Tx CLK OUT. This 50 Ω, AC coupled, ~ECL/2 level, 1.25 GHz (GTS1250) or 1.0625 GHz (GTS1063) clock signal is synchronous with the outgoing transmitted signal. When EXT mode is selected, this output is disabled.

SYNC OUT. This 50 Ω, AC-coupled, ~ECL/2 level signal is synchronous to and at the framerate of the outgoing pattern. When EXT mode is selected, this output is disabled. Use this Sync pulse to trigger an oscilloscope at a rate slower than the data rate of the pattern, thereby allowing you to capture the individual 1s and 0s of the entire pattern (as opposed to seeing an eye-pattern when equivalent-time sampling using a trigger signal with a rep rate higher than the pattern data rate). The repetition rate of this Sync pulse depends on the specific pattern selected (see *Tx SYNC Out pulse* on page 30).

EXT DATA IN. This is an input through which you can supply an NRZ, AC-coupled, 50 Ω data signal to digitally modulate the GBIC transmitter (EXT mode must be selected). When in EXT mode, a signal input to this connector is digitally received, buffered, and routed to the electrical differential data outputs as well as the differential inputs of the GBIC. The logical polarity of the signal is maintained. When not in EXT mode, the input signal is ignored.

NOTE. *To minimize noise from this input, do not connect a signal to this connector when using an internal Tx Pattern.*

Tx Fault and Rx LOS Indicators

The GBIC Test System monitors the flags coming from the GBIC Port receptacle (Rx_LOS and Tx_FAULT). In general, if the TX_FAULT signal is high, then the Tx FAULT LED is illuminated. Similarly, if the RX_LOS signal is high, then the Rcv LOS LED is illuminated. These signals and their definition are discussed in more detail in *GBIC Flags* on page 19. During an overload of the GBIC port receptacle supplies, these indicators blink (see *GBIC Overload Indicators* on page 16 for more information).

NOTE. *When no GBIC is installed, both the Rcv LOS and Tx FAULT indicators are illuminated.*

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GBIC Overload Indicators

The GBIC Test System also uses the Tx Fault and Rcv LOS indicators to indicate GBIC voltage and current overloads (I Overload and V Overload). During an overload of the GBIC port receptacle supplies (example: if a Vdd shorted GBIC is plugged in), the RX LOS and TX FAULT indicators blink. These signals and their definitions are discussed in more detail in *GBIC Overload Flags and Supply Monitor Signals* on page 20.

OVERLOAD RESET

When the GBIC Test System detects an overload of the GBIC supply, it blinks the overload indicator and shuts down the GBIC VDD +5 V supply. To reset this latched overload condition, remove the overload (such as uninstalling a shorted GBIC) and press the GBIC Overload RESET button (see Figure 4 on page 10).

Rear Panel

The rear panel is shown in Figure 6. The rear panel contains the power connector, the power switch, the Ext Clk Input connector, the Tx JITTER INPUT connector, and the REMOTE INTERFACE connector.

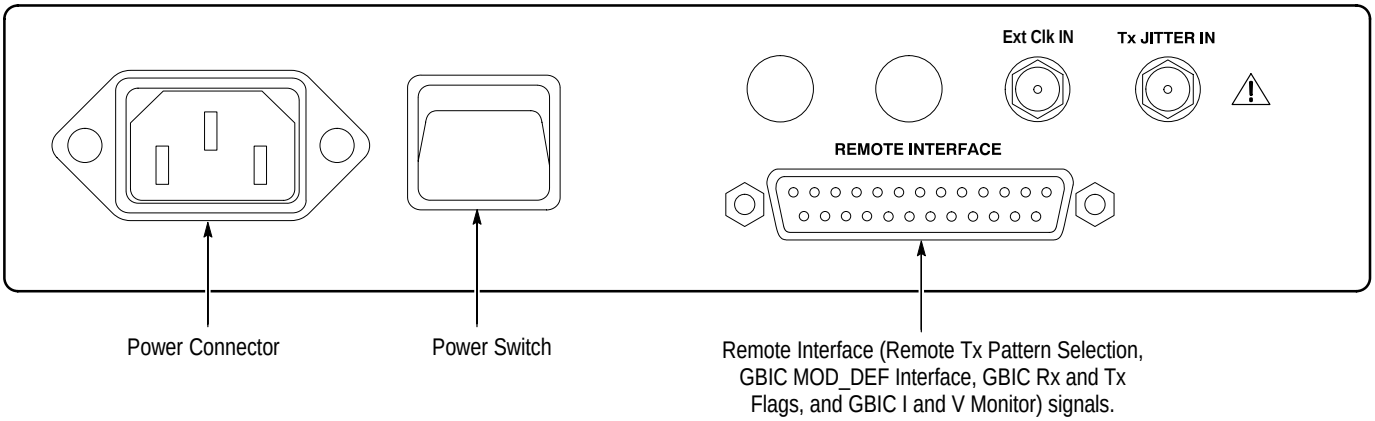


Figure 6: Rear Panel of GTS1250

Tx JITTER INPUT

This is an input through which you can supply a DC coupled signal to modulate the digital decision threshold of the ECL logic gates just prior to the GBIC differential inputs. Modulation of the decision threshold modulates the horizontal timing of the data edges of the transmitted pattern. The higher the amplitude of the JITTER IN signal, the greater the horizontal timing jitter in the Tx output data edges. The transfer function (V_{p-p} corresponding to jitter time p-p) level limits, and frequency coupling limits are defined in the *External Tx Jitter Input Specifications* on page 32.

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External Clock Input

This is an input through which you can supply a 1.25 GHz (GTS1250) or 1.0625 GHz (GTS1063) clock to externally clock the transmit patterns. To enable the input, pull the remote interface EXT_CLK_ENA pin low.

The quality of the clock determines the amount of jitter; the outgoing data will have the same timing jitter content as the EXT CLK IN signal.

Remote Interface

The Remote Interface is implemented with a 25-pin, male D connector on the rear panel. This interface serves five separate interface requirements:

- TTL input 3-bit remote control of Tx Pattern selection (when in REM mode).
- TTL output flags, for GBIC Tx Fault and Rx LOS, and TTL GBIC laser disable control (TX DISABLE).
- Serial Clock and bidirectional Data (similar to I2C) for GBIC serial-ID communication (also known as the GBIC MOD_DEF pins).
- GBIC VDD +5 V supply current or voltage overload flags, overload RESET, GBIC +5 V VDD current and voltage monitor signals, GBIC +5 V VDD supply offset, and GBIC power enable.
- Miscellaneous control inputs: front-panel lockout and external-clock enable.

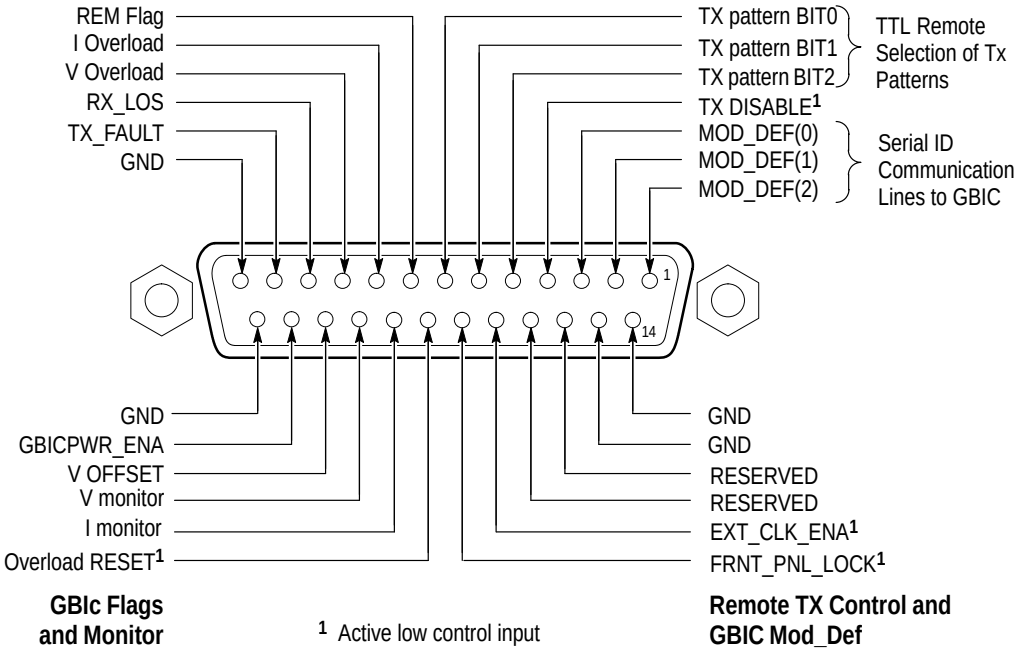


Figure 7: Rear Remote Interface connector pinout

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Remote Tx Pattern Selection

Pressing the REM button enables rear panel TTL control of the Tx Pattern selection and illuminates the front-panel REM indicator (if remote operation was already enabled, pushing the button has no effect). The 3-bit logic combination applied to the 3-bit interface (see Table 4) determines which pattern and front-panel indicator are active when REM mode is active. A logic 1 in the table represents a TTL high, and a 0 represents a TTL low. Any TTL signal that is not driven is pulled high (logic 1) by internal pull-up resistors.

Table 4: Remote pattern selection codes

BIT2	BIT1	BIT0	Tx Pattern selected
0	0	0	OFF (output data pattern is disabled)
0	0	1	D21.5
0	1	0	K28.5
0	1	1	PRBS7
1	0	0	K28.7
1	0	1	LONG (GTS1250) or CPAT (GTS1063)
1	1	0	SHORT (GTS1250) or CJTPAT (GTS1063)
1	1	1	EXT (default when no signal is applied to the TTL bits)

External Clock Enable

External clock enable (active low) selects either the internal clock or the clock supplied at the rear-panel external clock input. With no input to the enable pin (EXT_CLK_ENA), the internal 10 kΩ pull-up resistor selects the internal clock. Holding the enable pin at a TTL low selects the external 1.256 GHz for the GTS1250 or 1.0625 GHz for the GTS1063 signal input at the rear-panel external clock input (EXT_CLK). When the external clock is enabled, the front panel EXT indicator blinks.

***NOTE**. If you enable the external clock input, but do not supply an external clock signal, the GBIC Test System will oscillate and have poor jitter.*

FRNT_PNL_LOCK

Front panel lock (active low) controls whether front-panel controls are ignored. If this pin is a TTL LOW, the Tx Pattern REM indicator blinks, the Tx Pattern is selected by the remote selection code, and front-panel button presses are ignored. When this pin goes HIGH, the REM indicator is illuminated (stops blinking), but the front-panel buttons can control the transmit pattern. This pin is internally pulled HIGH with a 10 kΩ resistor; the default, no connection, state allows the front panel to control the transmit pattern.

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GBIC Flags

An industry standard GBIC outputs two digital flags and has one Tx enable/disable input. These flags are available on a rear-panel connector (see Figure 7). The following bullets describe the flags:

Tx_FAULT. If this signal is supported by the GBIC, a TTL high level is output and the front-panel Tx Fault LED is illuminated when a laser fault is detected by the GBIC. If a GBIC does not support this signal, the GBIC 5.1 standard requires that the GBIC hold this signal low (TTL level low). A fault is generally excessively high output power from the laser. This could pose an eye safety hazard. Therefore, the laser driver is disabled by the GBIC when this occurs (refer to IEC825-1 for specific safety hazard levels).

This output is commonly a TTL open collector output driver: the GBIC Test System uses a 10 kΩ pull-up resistor to +5 V on this signal path. A GBIC may have a method for resetting the TX_FAULT condition. For example, assuming the TX_FAULT condition no longer exists, the IBM GBIC requires driving the TX_DISABLE input to the GBIC to unlatch a TX_FAULT condition. Refer to the specifications for your GBIC for more details on the TX_FAULT and the reset method for this signal.

Rx_LOS. If this signal is supported by the GBIC, a TTL high level is output and the front panel Rcv LOS LED is illuminated when the incoming power level is below a certain threshold (usually this threshold is near the sensitivity limit of the GBIC). If a GBIC does not support this signal, the GBIC 5.1 standard requires the GBIC hold this signal low (TTL level low).

This output is usually a TTL open collector output driver. The GBIC Test System uses a 10 kΩ pull-up resistor to +5 V on this signal path. Refer to the specifications of your GBIC for more details on this signal.

Tx_DISABLE. In general (the GBIC response to this signal is dependent on the GBIC), a TTL low on this rear-panel pin turns off the GBIC laser Tx output. This signal is ORed with the front-panel OVERLOAD RESET. When you press the front-panel OVERLOAD RESET button, you also turn off the GBIC laser Tx output even if no overload condition exists.

This GBIC signal is generally compatible with TTL open collector drivers and normally has a 4.7 kΩ pull-up to the positive supply. The GBIC Test System enables the GBIC laser Tx output in the absence of a signal on the rear panel TX_DISABLE.

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GBIC Overload Flags and Supply Monitor Signals

A +5 V voltage or current overload in the GBIC receptacle is indicated on the front panel. The status of these overload states is also available as TTL signals on the rear panel. In addition, the absolute analog levels of both the GBIC voltage and current loading can be monitored through buffered analog voltages on a rear connector:

I Overload. If a +5 V current overload exists in the GBIC receptacle (see *GBIC Receptacle Supply Specifications* starting on page 36), this rear-panel flag is high (see figures 6 and 7) and the GBIC Test System shuts down the GBIC VDD supply and makes the front-panel I Overload indicator blink. The GBIC Test System turns the GBIC VDD +5V supply back on after the overload is removed (such as uninstalling a shorted GBIC) and the GBIC Overload RESET button is pressed or the REMOTE INTERFACE Overload RESET signal is pulsed low.

V Overload. If a +5 V voltage overload exists (this is possible because of the remote port V Offset input) in the GBIC receptacle, this rear-panel flag is high and the GBIC Test System shuts down the GBIC VDD supply and makes the front-panel V Overload indicator blink. The GBIC Test System turns the GBIC VDD +5V supply back on after the overload is removed and the GBIC Overload RESET button is pressed.

GBIC suppliers often guarantee Class I laser safety levels for the laser transmitter output when an overvoltage from the GBIC host is prevented. The GBIC Test System internal voltage regulator for the GBIC VDD supply and shutting down the VDD supply on voltage or current overload protect the GBIC from voltage overload.

Overload RESET (Active Low). After a GBIC I or V Overload, you can turn the +5 V VDD supply back on (assuming the overload condition is removed) by either a power cycle, a front panel GBIC Overload RESET button press, or by temporarily toggling this rear-panel signal low.

I Monitor. An analog voltage representing the +5 V VDD current load of a GBIC is available at the rear-panel I Monitor pin. This voltage is a linear function of the current load in the GBIC Port Receptacle +5 V Vdd supply. See *Rear-Panel Interface Connector Level Specifications* on page 36 for the conversion gain between the voltage output versus current flow. An operational amplifier buffers this current-monitor signal through a 1 kΩ resistor (measure this signal using a high impedance multimeter).

V Monitor. An analog voltage representing the +5 V VDD being applied to the GBIC is available at the rear-panel V Monitor signal pin. This is a direct connection to the +5 V VDD supply at the GBIC receptacle port through a 1 KΩ resistor (measure this voltage using a high impedance multimeter).

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V OFFSET. This is an analog voltage that is added to the +5 V supply to the GBIC receptacle. Input is limited to about ±1.2 V maximum, and about 20 kΩ input impedance. This allows you to test if a GBIC can operate error free to the specified ± supply margins.

For example, the +5 V GBIC supply is nominally +5.0 V for a particular GBIC. Inputting +150 mV results in a 5.0 + 0.150 V = 5.15 V GBIC supply. Inputting –100 mV yields 5.0 V –0.100 V = 4.9 V.

GBICPWR_ENA. Using this signal you can turn off the DC V_{dd} supply to the GBIC port. This pin is pulled high inside the GBIC Test System. When you drive this pin TTL LOW, the GBIC V_{dd} supply is off.

GBIC Serial-ID Communication

GBIC modules contain three module definition pins: MOD_DEF(0), MOD_DEF(1), and MOD_DEF(2). GBICs can implement these bits as static information or as serial communication. The GBIC Test System connects the MOD_DEF pins from an installed GBIC in the following manner (see Figure 8):

- MOD_DEF(0) is attached to a 4.7 kΩ pull-up resistor to +5 V and is available at the rear-panel connector
- MOD_DEF(1) is connected to the GBIC serial communication clock line (SCA)
- MOD_DEF(2) is connected to the GBIC serial communication data (SDA) line

You can use an I2C Bus Master to read internal GBIC Status information if serial communication is supported by the installed GBIC. For details regarding the serial communication protocol and signal levels, refer to the GBIC 5.1 standard and the GBIC specifications.

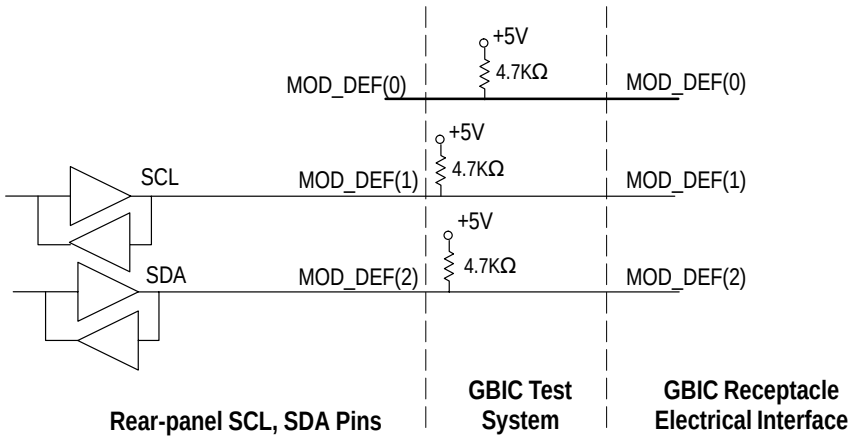


Figure 8: Serial ID connections to rear panel and GBIC

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GBIC Receptacle

The instrument front panel contains a rectangular opening for accepting GBIC modules. The dimensions for the receptacle and related mechanical rail-guide assembly are defined in the Gigabit Interface Converter (GBIC) standard 5.1. The guide and rail assembly (along with trap dust door) used by the GBIC Test System is a design that meets the GBIC 5.1 standards (see AMP application notes 114-6061 and 114-6069).

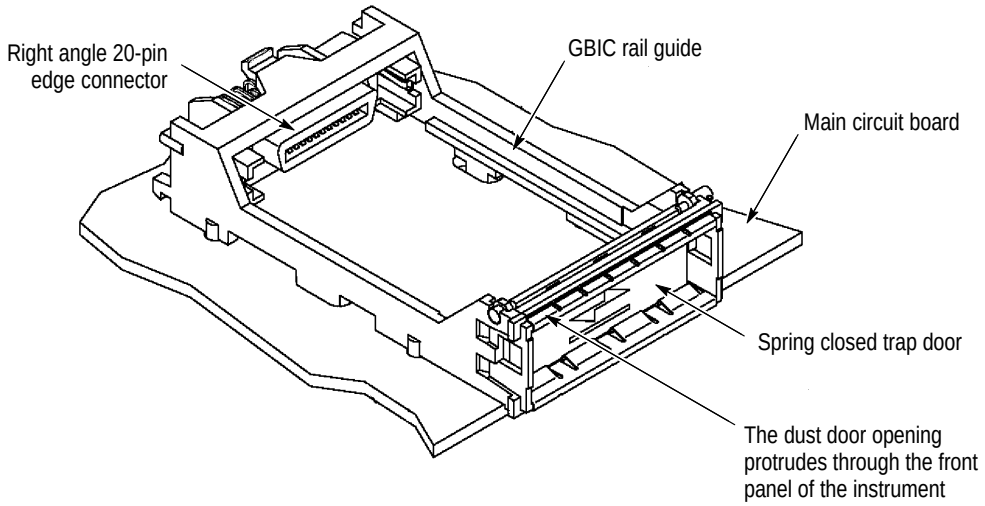


Figure 9: Isometric view of AMP GBIC receptacle rail guide assembly.

The internal D-connector inside the GBIC Port receptacle is a standard 20-pin female connector. The pinout of this connector interfaces to a GBIC module having the pin assignment shown in Figure 10 and Table 5.

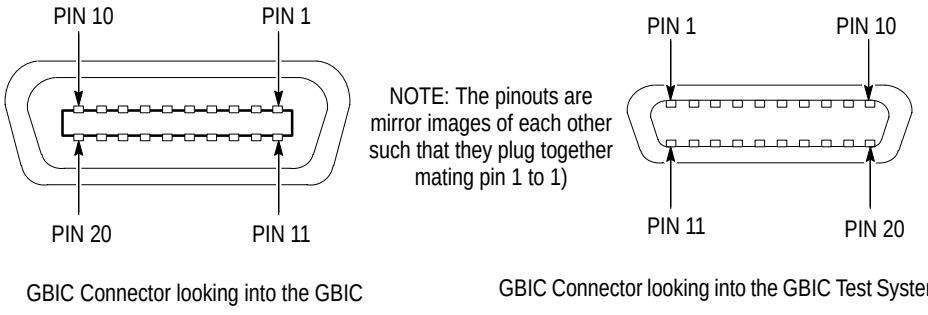


Figure 10: GBIC pinout supported by the GBIC Test System Receptacle

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Table 5: GBIC Pin Assignment

Pin	Description	Pin	Description
1	RX_LOS	11	RGND
2	RGND	12	–RX_DATA
3	RGND	13	+RX_DATA
4	MOD_DEF(0)	14	RGND
5	MOD_DEF(1)	15	VDDR[1]
6	MOD_DEF(2)	16	VDDT[1]
7	TX_DISABLE	17	TGND
8	TGND	18	+TX_DAT
9	TGND	19	–TX_DAT
10	TX_FAULT	20	TGND

1 **GBIC power is supplied to both pins from the same supply using separate paths and decoupling.**

Using the Rear Panel TTL REMOTE Interface

This section describes using the rear-panel REMOTE INTERFACE to select the transmitted signal.

Controlling Operation Remotely

When you push the REM button, you can select the Tx Pattern through the rear-panel TTL interface. When in this mode, the selected Tx Pattern on the front panel is illuminated and the REM indicator remains illuminated. Pushing any of the Tx Pattern selection buttons, while in the remote (REM illuminated) mode, turns on the associated Tx Pattern and turns off remote mode. Pushing the REM button when the REM indicator is already illuminated has no effect.

In REM mode when no TTL signal is applied at the rear-panel connector, the default Tx Pattern is EXT.

Selecting the Transmitted Signal

To remotely select a transmit signal, perform the following steps:

1. If not already selected, press the front-panel REM button.
2. Using Table 4 on page 18 and Figure 7 on page 17 as a guide, connect the required TTL voltage levels for the desired patterns to the rear-panel Remote Interface.

To exit REM mode, select a transmit pattern using the front-panel Tx Patterns select buttons.

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Connecting to a BERT, and Testing the Bit Error Rate

A critical element in a digital transmission system is how error free its transmissions are. This measurement is made by a bit-error-rate tester (BERT), which replaces one or more of the system components during a test transmission.

To measure the system error rate, the test equipment performs one or more of the following pairs of functions:

- Data-pattern generation and error monitoring
- Clock generation and recovery
- Jitter generation and measurement

The functions used depend on how the GBIC Test System and the BERT are connected.

A digital transmission system includes a data source, such as a computer ethernet-transceiver network-interface card.

A clock source produces a clock signal that times each bit in the digital signal.

A driver prepares the signal for the transmission system.

A typical system in which the GBIC Test System is used to assist in BERT testing might include laser transmitters, fiber, optical receivers, and possibly repeaters. A malfunction in any component can cause the recovered data to differ from the original data. The primary job of a BERT is to determine the system error rate.

The GBIC Test System can be the data source, the clock source, the driver, the source of the recovered clock and data when using the clock recovery option, or even the system under test if testing an installed GBIC.

To test the bit error rate, set up the GBIC Test System and the BERT as shown in either Figure 11 or Figure 12. Use the setup in Figure 11 if the transmit and receive ends of the fiber are far apart; use the setup in Figure 12 if they are close together. These setups allow the GBIC Test System to act as the data and clock source for testing a GBIC or other parts of the transmission system. BER receivers compare the incoming serial data to an expected data pattern. You must program the BER receiver to have an expected pattern that matches the pattern being generated by the GBIC Test System; the PRBS7 is a common fixed pattern that you can program into most BER receivers with a single button push.

If the transmit and receive ends of the fiber are close together and if the link distance is short enough to not allow significant phase drift (propagation delay changes due to environmental changes, modal propagation differenced, and so forth), the Tx CLK might be used in place of the recovered clock.

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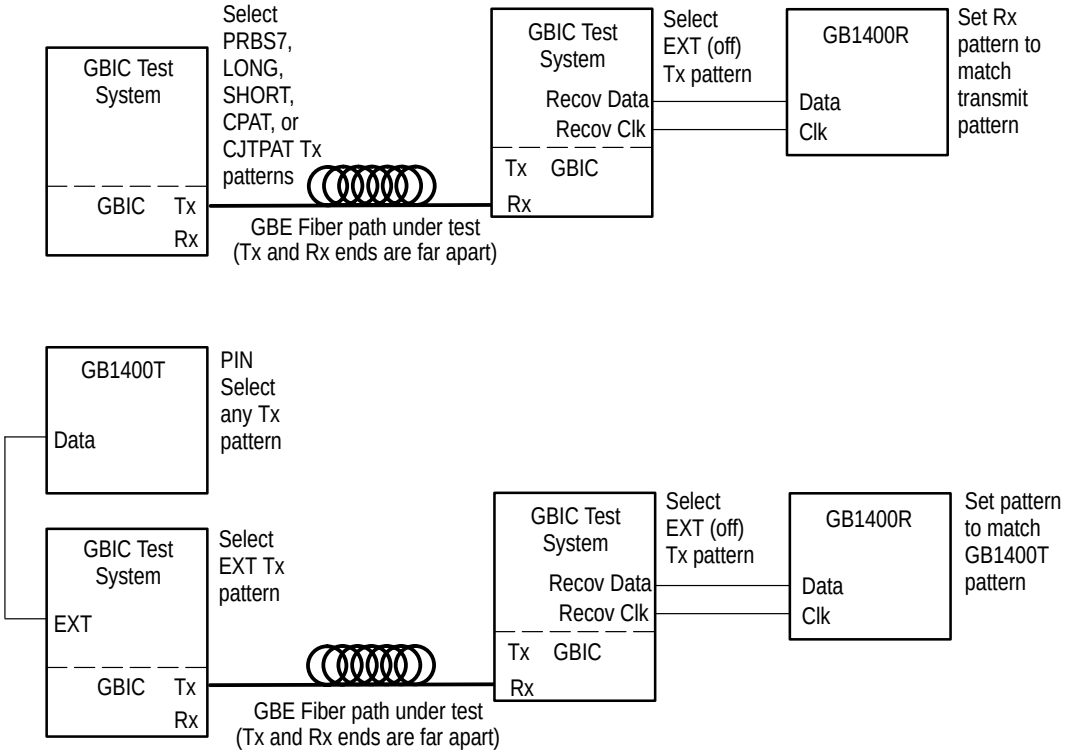


Figure 11: BER Test of GBE Fiber Path (Tx and Rx ends are far apart)

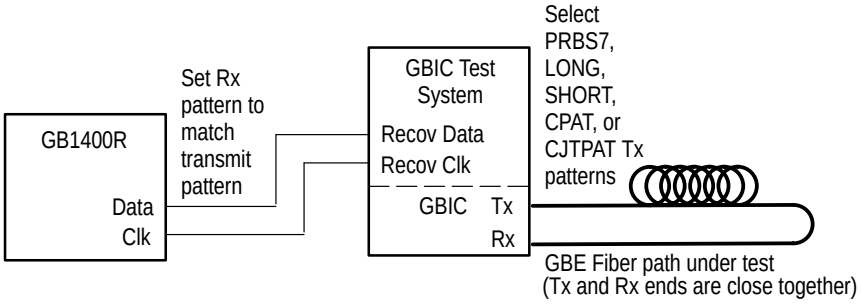


Figure 12: BER Test of GBE Fiber Path (Tx and Rx are close together: loopback)

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Adding Jitter to the Transmitted Signal

Under normal conditions, the clock source should be essentially jitter free to test a GBIC. However, you may want to stress the system. To do so, the GBIC Test System has a jitter input to modulate the phase of the clock.

On the receive end, the BERT monitors the effect of the controlled jitter in two ways. First it looks for an increased error rate. Second, it measures the jitter remaining in the recovered data.

As shown in figures 13 and 14, the setup for adding jitter to the transmitted signal is the same as for bit error rate testing except for the insertion of a sinewave or DC voltage at the JITTER IN input.

To add jitter to the transmitted signal perform the following steps:

1. Set up the equipment as shown in Figure 13 or 14.
2. If using the setup in Figure 13, set the sinewave generator to the desired jitter frequency.
3. Set the sinewave generator or DC voltage to the amplitude required to generate the desired horizontal jitter (see *External Tx Jitter Input Specifications* on page 32.
4. If you have a clock generator source capable of adding frequency or phase modulation to the clock, then alternatively you can also produce jitter on the front panel and GBIC signals by applying such a clock to the rear-panel Ext Clk IN input.

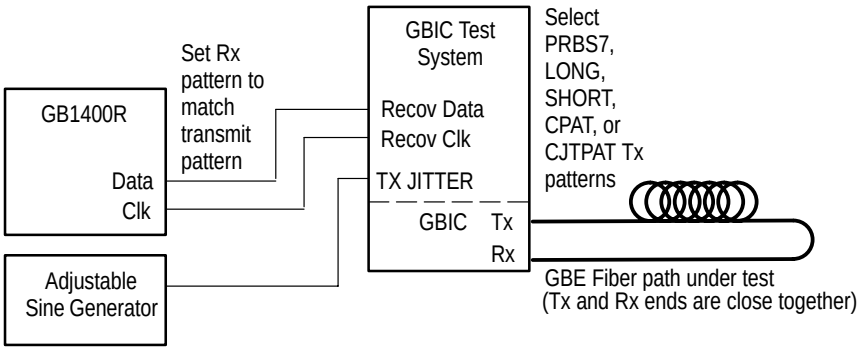


Figure 13: Stress Testing via increasing Transmitted Jitter through the rear Tx JITTER INPUT

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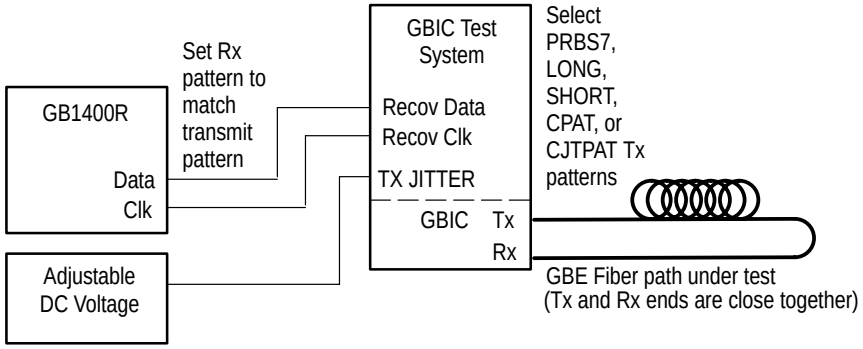


Figure 14: Stress Testing via increasing Deterministic Jitter through the rear Tx JITTER INPUT

Fiber Path Repeater or Monitor

You can use the GBIC Test System with Option 01 as a repeater or monitor in a gigabit ethernet (GBE) fiber path. Short wavelength (780 nm, 850 nm) multi-mode optical transceivers are capable of spanning 550 m on quality fibers. Single-mode long wavelength (1310 nm, 1550 nm) optical transceivers are capable of spanning 10 kilometers. Metallic twisted pair cables are sufficient for many short (75 m) links. You can extend these ranges using a repeater.

To use the GBIC Test System as a repeater or monitor in the fiber path perform the following steps:

1. Set up the GBIC Test System as shown in Figure 15.
2. Select the EXT TRANSMIT PATTERN.
3. Connect a coaxial cable between the RECOV. DATA and EXT DATA IN connectors.
4. Insert the GBIC Test System into the fiber path at the GBIC Tx and Rx connectors.
5. The GBIC Test System should now repeat the data farther down the fiber path.
6. To monitor the data on the fiber, use a coaxial cable to connect the +Rx DATA connector of the GBIC Test System to the input of an oscilloscope, protocol analyzer, or other monitoring equipment.

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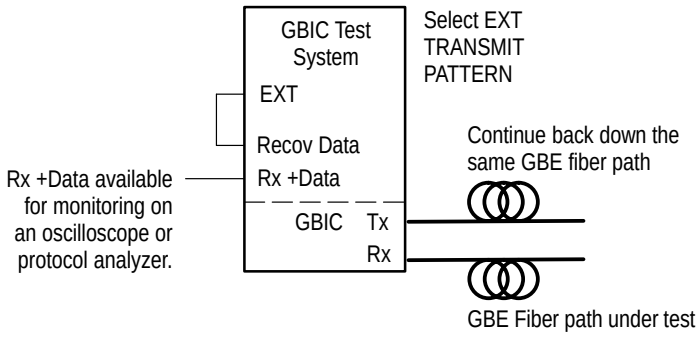


Figure 15: Using the GBIC Test System as a fiber path repeater or monitor

Installation in a Rack

You may install your GBIC Test System in the optional TVGF13 Rack Adapter. In addition to the instructions that come with the adapter, do the steps shown in Figure 16 before installing your GBIC Test System in the rack adapter.

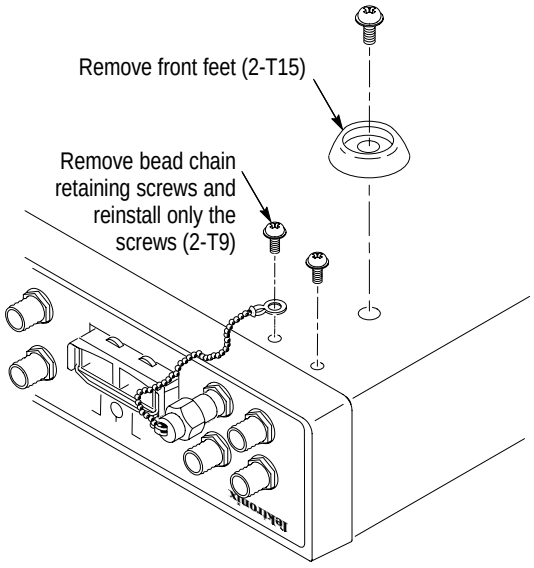


Figure 16: GBIC Test System modifications before installation in rack adapter

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Specifications

This section contains the specifications of the GTS1250 and GTS1063 GBIC Test Systems. All specifications are guaranteed unless noted as "typical." Typical specifications are provided for your convenience but are not guaranteed. Specifications marked with the ✓ symbol have corresponding checks in the *Performance Verification* section on page 43.

Table 6: Tx Data and Tx Clock Out Specifications

Specification	Description
Tx Data rate (Clk frequency)	Tx output data rate (internally generated patterns): GTS1250: 1.250000 Gb/s ± 75 ppm GTS1063: 1.06250000 Gb/s ± 75 ppm Test Method: The Tx pattern is set to K28.7 (5 1s, 5 0s) such that the output is a 125 MHz (GTS1250) or 106.25 MHz (GTS1063) square wave; the Tx DATA electrical output is sent to a counter capable of measuring past 125 MHz.
Tx Rise and fall times	CLK and DATA output rise time: < 300 ps CLK and DATA output fall time: < 300 ps Rise and fall times are the transition duration from 10% to 90% (rise) or 90% to 10% (fall). A 50 Ω output termination is required to meet specification.
✓Tx Output level swings	Output swing levels are specified for 50 Ω RF cable lengths of < 0.5 m in length and < 0.25 dB loss in the first 2 GHz frequency range. Tx DATA output peak-to-peak minimum: > 300 mV_{p-p} maximum: < 600 mV_{p-p} Tx CLK output peak-to-peak minimum: > 300 mV_{p-p} maximum: < 600 mV_{p-p} Both the Tx DATA and CLK outputs are AC coupled and require external 50 Ω termination for proper output swings. The 50 Ω cable (Tektronix part number 015-0560-00) used is relatively short (2 ns). Tx SYNC output peak-to-peak minimum: > 300 mV_{p-p} maximum: < 600 mV_{p-p} The SYNC Out pulse is AC coupled and requires external 50 Ω termination for proper output swings. The level of the Sync Out pulse relative to AC-GND level depends on the duty cycle of the SYNC Out pulse; this is pattern dependent. The 50 Ω cable (Tektronix part number 015-0560-00) used is relatively short (2 ns).
✓Tx Data, $\overline{\text{Data}}$ duty cycle (balance)	Tx DATA signals have a balanced output of 50% ± 1% for internally generated data patterns only. For a pattern with a perfect balance between numbers of logical 1s and 0s, the Tx Data output shall individually have a balanced 50% duty cycle output.

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Table 6: Tx Data and Tx Clock Out Specifications (cont.)

Specification	Description
Tx SYNC Out pulse width and repetition rate (typical)	GTS1250 Repetition rate: — Pulse width D21.5, K28.7: 62.5 MHz (10 in 20 UI) — 8 ns ± 1 ns K28.5: 31.25 MHz (20 in 40 UI) — 16 ns ± 1 ns PRBS7: 984.251 kHz (10 in 1270 UI) — 8 ns ± 1 ns LONG: 81.3802 kHz (160 in 15360 UI) — 128 ns ± 1 ns SHORT: 336.02 kHz (160 in 3720 UI) — 128 ns ± 1 ns GTS1063 Repetition rate: — Pulse width D21.5, K28.7: 51.125 MHz (10 in 20 UI) — 9.4 ns ± 1 ns K28.5: 26.5625 MHz (20 in 40 UI) — 18.8 ns ± 1 ns PRBS7: 836.614 kHz (10 in 1270 UI) — 9.4 ns ± 1 ns CRPAT: 466.008 kHz (2640 in 2280 UI) — 263.353 ns ± 1 ns CJTPAT: 402.462 kHz (280 in 2640 UI) — 263.353 ns ± 1 ns Test Method: Split Tx SYNC Out pulse through an electrical splitter: use half to trigger an 1180X oscilloscope and measure the other half on the SD-22.
External clock sensitivity	> 300 mV_{pp} and < 1.4 V_{pp}, AC coupled
✓Data-to-Clock random jitter	Tx DATA, $\overline{DATA}$: < 4 ps RMS; < 35 ps_{p-p}. < 2 ps RMS; < 25 ps_{p-p} typical
Data-to-SYNC Out random jitter (typical)	Tx DATA, $\overline{DATA}$: < 4 ps RMS; < 42 ps_{p-p} for D21.5, K28.7 patterns only. Test Method: To measure, set the DATA pattern to 1010101010 repeating (125 MHz [GTS1250] or 531.25 MHz [GTS1063] square wave: D21.5 pattern). Trigger a Tektronix SD-22 sampler (12.5 GHz is used) and an 1180X oscilloscope by the Sync Out. Measure the rising edge of the sampled DATA that occurs in the first 30 ns after the trigger event. Make histogram measurements at the 50% crossing level, capturing 100 waveforms and then stop further acquisitions.
✓Data-to-SYNC Out (K28.5 pattern) deterministic jitter	Tx DATA, $\overline{DATA}$: < 40 ps_{p-p} DJ; (0.05 UI for GTS1250; 0.0425 UI for GTS1063). < 20 ps_{p-p} DJ; (0.025 UI for GTS1250; 0.021 UI for GTS1063), typical

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Table 7: External Data Input Specifications

Specification	Description
Input voltage swing, minimum and maximum (typical)	Minimum: 300 mV_{p-p} (50%, ± 1% average duty cycle) Maximum: 1.5 V_{p-p} (50%, ± 1% average duty cycle) This single-ended NRZ Data input is capacitively AC coupled to an internal line receiver. The slew rate (10% to 90%, 90% to 10%) of the input data should not fall below 2 ns.
Data rates, minimum and maximum	Minimum: 100 Mb/s Maximum: 1.4 Gb/s These data rates are the limits of the External Data Input to receive externally supplied NRZ Data (within level specifications with the longest consecutive pattern of 1s and 0s not more than seven) and to then pass this serial data as a differential 75 Ω signal into the GBIC receptacle +TX_DATA and –Tx_DATA signal paths without significant RC time constants being imposed on the data sequence.
Maximum nondestructive DC voltage	10 V This is the maximum nondestructive DC potential that can be applied to this capacitively-coupled input.
Maximum nondestructive AC input voltage swing	5 V_{p-p} This is the maximum nondestructive AC voltage swing that can be applied to this capacitively coupled input; the input 50 Ω termination can be damaged above this level.
Jitter Transfer	This DATA Input is digitally compared and then sent directly to the GBIC receptacle ± Tx_DATA pins as a differential signal input; no significant timing jitter is added nor subtracted from that which is inherent in the external DATA Input signal.

Table 8: External Clock Input Specifications

Specification	Description
Input voltage swing, minimum and maximum (typical)	Minimum: 300 mV_{p-p} (50%, ± 1% average duty cycle) Maximum: 1.5 V_{p-p} (50%, ± 1% average duty cycle) Typical: 5.0 V This single-ended clock input is capacitively AC coupled to an internal line receiver. The slew rate (10% to 90%, 90% to 10%) of the input data should not fall below 300 ps.
Maximum non-destructive AC input voltage swing (typical)	5.0 V peak-peak The maximum non-destructive AC voltage swing that can be applied to this capacitively coupled input; the input 50-ohm termination is damaged above this level.

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Table 8: External Clock Input Specifications (cont.)

Specification	Description
Input clock rate	GTS1250: 1.250000 GHz ± 1% GTS1063: 1.062500 GHz ± 1% These rates are the limits of the External Clock Input to receive externally supplied NRZ Data (within level specifications with the longest consecutive pattern of 1s and 0s not more than seven) and to then pass this serial data as a differential 75 Ω signal into the GBIC receptacle +TX_DATA and –Tx_DATA signal paths without significant RC time constants being imposed on the data sequence.
Jitter Transfer and tolerance	Horizontal jitter transfer: 1:1 Jitter tolerance: not specified The EXT CLK IN clock is divided by 10 and drives a parallel 10-bit-to-serial serializer-deserializer (SERDES) IC to produce the serial data stream; this serial data stream is retimed against the full serial clock, and as such the outgoing data will have the same timing jitter content as the EXT CLK IN signal.

Table 9: External Tx Jitter Input Specifications

Specification	Description
Input-to-DATA jitter transfer function	A 1 V input yields approximately +110 ps increase in logic HIGH pulse widths: (500 mV_{pp} maximum input). Values exceeding ± 500 mV and less than 2.0 V typically yield 130 ps per Volt. The Tx Jitter Input signal is DC coupled, divided by 5, and applied added to the V_{bb} logic threshold of one side of a differential digital ECL gate in series with the serial 1.25 Gb/s Tx DATA path. This coupling allows the external DC signal to directly modulate the digital DATA threshold, in effect causing both positive and negative fluctuations in the duty cycle (pulse width) of the serial DATA stream. The rising edge of the internally generated DATA signal is not strictly specified, and therefore the transfer function of the externally supplied Tx Jitter to horizontal timing jitter is subject to variations. In general, however, small signals input as jitter (< 500 mV_{pp}) will be more linear than large signals.
Input bandwidth, typical	–3 dB bandwidth: DC to 4.75 MHz (± 0.5 MHz) The frequency at which the peak-to-peak pulse width edge variation is –3 dB (0.707) of that experienced at frequencies approaching DC.
Maximum nondestructive voltage input (AC or DC)	5 Volts This is the maximum nondestructive DC potential that can be applied to this input; the input 50 Ω termination can be damaged above this level.

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Table 10: Rx Electrical Specifications

Specification	Description
± Rx_DATA Termination	Both +Rx_DATA and –Rx_DATA Min-Loss outputs must be DC terminated to 50 Ω. The Recovered Clock and Recovered DATA originate from a buffered pickoff of the ± Rx_DATA signals in the resistive branch of the internal 75-to-50 Ω min-loss conversion circuitry. If the external +Rx DATA and –Rx DATA outputs are not properly terminated coaxially (or with SMA 50 Ω cap terminations) to 50 Ω DC, then severe impedance mismatch reflections distort the digital data pickoff. It is necessary to terminate the +Rx DATA and –Rx DATA outputs at all times, even when not in use, to allow the recovered clock and recovered data to work properly.
⩗Rx Recovered CLK and DATA output level swings	Output level swings are specified for 50 Ω RF cable lengths of < 0.5 m and < 0.25 dB loss in the first 2 GHz frequency range. Rx DATA output peak-to-peak minimum: > 300 mVp-p maximum: < 600 mVp-p Test Method: Optical DATA input pattern is set to 1111100000 repeating (125 MHz [GTS1250] or 531.25 MHz [GTS1063] square wave: K28.7 repeated) for measuring maximum swing and to 1010101010 (D21.5 repeated) for minimum swing. A Tektronix SD-22 sampler (12.5 GHz is used). RF 50 Ω cable used (Tektronix part number 015-0560-00) is relatively short (2 ns). Use optical loopback from GBIC Tx to GBIC Rx for stimulus. Rx Recovered CLK output peak-to-peak minimum: > 300 mVp-p maximum: < 600 mVp-p Test Method: Optical DATA input pattern is set to 1010101010 (D21.5 repeated). A Tektronix SD-22 sampler (12.5 GHz is used). RF 50 Ω cable used (Tektronix part number 015-0560-00) is relatively short (2 ns). Both Rx DATA and Recovered CLK outputs are AC coupled and require external 50 Ω termination for proper output swings. The 50 Ω cable used (Tektronix part number 015-0560-00) is relatively short (2 ns).
Rx rise and fall times	Rx DATA output rise: < 300 ps Rx DATA output fall: < 300 ps Recovered CLK output rise: < 300 ps Recovered CLK output fall: < 300 ps Rise times and fall times are defined as the transition duration from 10% to 90% (rise) or 90% to 10% (fall).

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Table 10: Rx Electrical Specifications (cont.)

Specification	Description
Rx ± Rx_DATA min-loss path bandwidth	< 3 dB loss separately in each path up to 2.0 GHz The differential 75 Ω output from the GBIC connector passes through two separate 75-to-50 Ω min-loss passive impedance conversion networks. The frequency response of this network is limited by the parasitics in the actual passive components and the circuit board transmission lines. Test Method: A differential TDR (Tektronix SD-24) is used to drive the two 50 Ω outputs differentially. The GBIC Port receptacle ± Rx_DATA 75 Ω differential pins are left open. The TDR signal will pass through the min-loss pad, up to GBIC Port open, reflect off of this large impedance mismatch, and return to the TDR head again through the min-loss pad. The resulting step (differential) of the TDR result is converted to frequency domain by an FFT. Since the TDR signal traverses the path twice, the resulting FFT vertical dB versus frequency scale is halved to determine the one-pass bandwidth (–3 dB) of this path.
± Rx_DATA min-loss input path sensitivity (typical)	Single-ended input Minimum: 100 mV_{p-p} Maximum: 2 V_{p-p}
Rx ± Rx_DATA min-loss path conversion gain (typical)	50 Ω amplitude is 42.3% ± 2% of 75 Ω amplitude The differential amplitude between the GBIC receptacle pins +Rx_DATA and –Rx_DATA are converted to the two 50 Ω outputs with 0.423 gain. For example: a 1 V_{p-p} differential 75 Ω signal from a GBIC will be represented on the front panel ± Rx_DATA with a 423 mV_{p-p} differential signal as measured between the +Rx_DATA output and –Rx_DATA output. This conversion gain assumes an external DC 50 Ω termination is attached to these outputs. This conversion gain is defined relative to the individual voltage swings that would be observed if one of the RX_DATA signals was probed (single-ended) at the GBIC-to-host interface and both ± Rx_DATA signals were terminated within the GBIC host (150 Ω differential, 75 Ω individually).
Lock range, Rx recovered clock data rate	Maximum data rate: GTS1250:: 1.25 Gb/s +1% (1.2625 Gb/s) GTS1063: 1.0625 Gb/s +1% (1.07312 Gb/s) Minimum data rate: GTS1250: 1.25 Gb/s –1% (1.2375 Gb/s) GTS1063: 1.0625 Gb/s –1% (1.05187 Gb/s)

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Table 10: Rx Electrical Specifications (cont.)

Specification	Description
Rx recovered clock phase lock loop bandwidth (Jitter Transfer Bandwidth)	GTS1250: 750 kHz ± 100 kHz GTS1063: 637 kHz ± 100 kHz The recovered clock will track variations in the instantaneous data rate up to the phase lock loop bandwidth (at the PLL BW the peak-to-peak transfer of timing jitter in the incoming DATA signal applied to the GBIC optical receiver will be reduced by 0.707). The specified bandwidth (jitter transfer bandwidth from incoming DATA signal to outgoing recovered clock) of the phase-locked-loop (PLL) in the GTS1000 Clock Recovery circuitry requires that the DATA stream applied to the receiver has a certain transition density. Pseudo-random data patterns (such as PRBS7) tend to have an average statistical time interval between transition edges of two unit intervals: this is equivalent to saying the average length of consecutive logic zeroes or logic ones that occur in the data pattern is roughly two bit periods in length. The D21.5 data pattern (1010101010) is an example of a pattern that has a much higher transition density than a PRBS or typical network: the Recovered Clock circuitry will generally show a higher PLL bandwidth for higher transition densities and a lower PLL bandwidth for lower transition density patterns.
Rx recovered clock jitter tolerance	f_{MOD} < 30 kHz: 1.5 UI (1200 ps, GTS1250; 1411.76 ps, GTS1063) 3 MHz > f_{MOD} > 30 kHz: 0.15 UI (120 ps) f_{MOD} is the frequency of horizontal timing jitter in the incoming optical data signal. This specification assumes the installed GBIC module can tolerate beyond these limits.
✓Rx recovered clock to data random jitter	Maximum: < 8 ps RMS Typical: < 4 ps RMS
Rx recovered clock maximum tolerable consecutive logic 0 or 1	Maximum: 15 consecutive 0s or 1s in incoming data stream This is the longest consecutive string of logic 0s or logic 1s the clock recovery circuit can tolerate in the incoming optical data signal and still guarantee glitch-free BER performance of greater than 10^{-15}. This specification assumes the installed GBIC module used to receive the signal can tolerate beyond these limits.

Table 11: Internal DC Power Supply Specifications

Specification	Description
External AC levels to power supply module	100 V to 240 V ± 10%, 47 to 63 Hz, < 60 W; CAT II

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Table 12: GBIC Receptacle Supply Specifications

Specification	Description
✓GBIC Vdd (+5 V) Min/Max voltage	Minimum: 4.8 V Maximum: 5.25 V Typical: 5.0 V
GBIC Vdd (+5 V) Maximum current available	400 mA steady state The overload shutdown feature (see *I Overload* on page 20) protects this supply against short circuits.
GBIC Vdd (+5 V) output ripple	Output ripple: < 50 mV_{p-p} relative to receptacle GND

Table 13: Rear-Panel Interface Connector Level Specifications

Specification	Description
TTL remote control logic control voltage levels	Input HIGH voltage (V_{IH}): 2.0 V minimum Input LOW voltage (V_{IL}): 0.8 V maximum Voltages are relative to GND on the 9-pin remote connector
Rear-panel I Monitor Signal	+1 mV per 1 mA, ±3%, of +5 V GBIC Receptacle supply current load (relative to rear-panel connector ground). The drive circuit, which converts the current to this voltage signal, is passively buffered to the rear-panel signal pin through a series 1 kΩ resistor. This signal is a positive only voltage relative to the current load average: this signal has about 100 kHz bandwidth.
Rear-panel V Monitor Signal	Direct 1 to 1 passive GBIC voltage monitor, ±3% This signal is passively buffered from the GBIC Receptacle Port +5 V Vdd supply to the rear-panel signal pin through a series 1 kΩ resistor. Bandwidth of this signal is not specified due to the presence of decoupling at the source of the signal.
Rear-panel V Offset	Input impedance: 20 kΩ ±10% to GND Input range: –500 mV to +500 mV Gain: 1 to 1 addition of this signal to the GBIC Port Vdd supply. Accuracy: ±10% (use V monitor to know true voltage) Voltage levels are referenced relative to GND on the rear panel. Signals exceeding the ± range are clamped at approximately a diode drop.

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Table 14: Environmental Characteristics

Specification	Description
Temperature, non-operating	Class 6 (–55° C to +75° C) The environmental exposure is the procedure stated in Tektronix Design Standard 062-2847-00 for Class 6 equipment.
Temperature, operating	10° C to +40° C (50 to 104° F) This operating condition is guaranteed for the instrument itself independent of the GBIC installed. This procedure conforms to the temperature portion of the test in MIL-T-28800E for Type III, Class 6 equipment, using the limits above.-
Humidity, non-operating	0% to 75% relative humidity from +30° C to +60° C.
Humidity, operating	0% to 75% relative humidity from +10° C to +40° C.
Random vibration, non-operating	2.46 g RMS, from 5 to 500 Hz, 10 minutes each axis. Tektronix Standard 062-2858-00 rev. B modified, Random Vibration, Tektronix Class 3 with power spectral density break-points as follows: Constant 0.020 g^2/Hz from 5 Hz to 100 Hz, then falls at –3 dB/octave from 100 to 200 Hz, then constant 0.010 g^2/Hz from 200 to 350 Hz, then falls at –3 dB/octave from 350 to 500 Hz to 0.007 g^2/Hz @ 500 Hz. Tested both with and without an IBM GBIC-1250 GBIC module installed.
Random vibration, operating	0.31 g RMS, from 5 to 500 Hz, 10 minutes each axis. Tektronix Standard 062-2858-00 rev. B, Random Vibration, Tektronix Class 3 Tested both with and without an IBM GBIC-1250 GBIC module installed.
Packaged product vibration and shock	The packaged product qualifies under the Distribution Cycle 1 Assurance Level II for packaged products 0 to 20 lbs. Test 2 for Warehouse and Vehicle Stacking (compression) is omitted. Tektronix standard 062-2858-00, Rev. B. Tested both with and without an IBM GBIC-1250 GBIC module installed.
Altitude, operating and nonoperating	Operating: 3000 m (9847 ft) Nonoperating: 12190 m (40,000 ft) MIL-T-2880E modified for more exposure time and more severe test levels than required for any Type III equipment regardless of Class.
Weight, shipping	5.22 kg (11.5 lbs.), including standard accessories

[2] **The humidity limits are derived from a psychrometric chart using a maximum wet bulb temperature of 29° C. The highest RH (20%) at the maximum temperature (+60° C) diverges from the psychrometric chart (which would indicate 6%). The 20% number is a practical limit. Test chambers cannot be set below this number.**

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Table 15: Electromagnetic Compatibility (EMC)

Specification	Description
Emissions	Emissions shall be within the limits specified by the following requirements. Enclosure: EN 55011 Class A limits for radiated emissions AC Mains: EN 55011 Class A limits for conducted emissions Emissions: EN 61000-3-2 AC power line harmonic emissions EN 61000-3-2 AC power line fluctuation AS/NZS 2064, Australian emission standard for Industrial, Scientific, and Medical Equipment Use only high quality shielded interface cables having a reliable, continuous outer shield (braid and foil) that has low impedance connections to shielded connector housings at both ends.
Immunity, enclosure, radio frequency electromagnetic field	Better than 10^{-9} BER performance when the unit is subjected to a 3 V/m electromagnetic field over the frequency range of 27 MHz to 1000 MHz. IEC 61000-4-3; with a GBIC installed, use a GB1400T to drive a PRBS7 pattern into a GBIC Test System outside the chamber (call this unit number 1; not under test). A fiber connection from the Tx optical out (GBIC) of unit number 1 is sent into the Tx optical in (GBIC) of the unit in the chamber under test. The recovered data of the unit under test is looped back to its own EXT Tx input, set to EXT mode, and the TX optical output is routed via fiber back out of the chamber into the Optical Rx port of unit number 1. The recovered clock and data of Unit number 1 are routed to a GB1400R, and the overall loop BER is measured (BER performance of any one component in such a loop is equal to or better than the whole loop BER).
Immunity, enclosure, electrostatic discharge (ESD)	Up to 8 kV air discharge and 4 kV contact discharge with no change to control settings, no impairment of normal operation, and no damage that prevents recovery of normal operation by the user. IEC 61000-4-2; tested both with and without an IBM GBIC-1250 GBIC module installed; failure of GBIC itself is not warranted since Tektronix has no direct control over the GBIC specification.
Immunity, fast transients, electrical	No loss of stored data, change to control settings, degradation of performance, or temporary loss of function will occur when the system is subjected to the transients as described below:

Port	Peak Voltage (kV)	Tr/Th (ns)	Rep. Freq. (kHz)
Signal and Control	0.5	5/50	5
AC Power	1.0	5/50	5

IEC 61000-4-4

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Table 15: Electromagnetic Compatibility (EMC) (cont.)

Specification	Description
Immunity, AC power line source voltage dips and interruptions	Voltage Dips: 30% reduction/10 ms, as per EN 61000-4-11 60% reduction/100 ms, as per EN 61000-4-11 Voltage Interruptions: > 95% reduction/5 seconds as per EN 61000-4-11 100% reduction/1 cycle as per EN 61326
Immunity, AC power line transients	No loss of stored data, change to control settings, degradation of performance, or temporary loss of function will occur when the system is subjected to the transients as described below: **Mode** — **Peak Voltage[1]** Common — 2 kV Differential — 1 kV IEC 61000-4-5
Immunity, conducted disturbances induced by RF fields	No instrument failures when the instrument power leads are injected with a 150 kHz to 80 MHz, 3 V_{RMS} signal 80% amplitude modulated at 1 kHz. IEC 61000-4-6

1 **2/50 us Tr/Th voltage into open circuit, 8/20 us Tr/Th current into short circuit.**

Table 16: Safety Characteristics

Specification	Description
Power consumption	50 W maximum when powered from AC line
Source frequency	47 to 63 Hz
Safety certifications	UL3111-1, CAN/CSA-C22.2 No. 1010.1

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Table 17: Certifications and compliances

Category	Standards or description	
EC Declaration of Conformity – EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Union:	
	EN 55011	Class A Radiated and Conducted Emissions
	EN 55011	Class B Radiated and Conducted Emissions
	EN 50081-1 Emissions:	
	EN 55022	Class B Radiated and Conducted Emissions
	EN 60555-2	AC Power Line Harmonic Emissions
	EN 50082-1 Immunity:	
	IEC 801-2	Electrostatic Discharge Immunity
	IEC 801-3	RF Electromagnetic Field Immunity
	IEC 801-4	Electrical Fast Transient/Burst Immunity
	IEC 801-5	Power Line Surge Immunity
Australia/New Zealand Declaration of Conformity – EMC	Complies with EMC provision of Radiocommunications Act per the following standard(s):	
	AS/NZS 2064.1/2	Industrial, Scientific, and Medical Equipment: 1992
	AS/NZS 3548	Information Technology Equipment: 1995
EMC Compliance	Meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility when it is used with the product(s) stated in the specifications table. Refer to the EMC specification published for the stated products. May not meet the intent of the directive if used with other products.	
FCC Compliance	Emissions comply with FCC Code of Federal Regulations 47, Part 15, Subpart B, Class A Limits.	
EC Declaration of Conformity – Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Union:	
	Low Voltage Directive 73/23/EEC, amended by 93/69/EEC	
	EN 61010-1:1995/A2	Safety requirements for electrical equipment for measurement, control, and laboratory use.
U.S. Nationally Recognized Testing Laboratory Listing	UL3111-1	Standard for electrical measuring and test equipment.
Canadian Certification	CAN/CSA C22.2 No. 1010.1	Safety requirements for electrical equipment for measurement, control, and laboratory use.
Installation (Overvoltage) Category	Terminals on this product may have different installation (overvoltage) category designations. The installation categories are:	
	CAT III	Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location.
	CAT II	Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected.
	CAT I	Secondary (signal level) or battery operated circuits of electronic equipment.
Additional Compliance	IEC61010-1 /A2	Safety requirements for electrical equipment for measurement, control, and laboratory use.

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Table 17: Certifications and compliances (cont.)

Category	Standards or description
Safety Certification Compliance	
Temperature, operating	10 to +40° C (50 to 104° F)
Altitude (maximum operating)	3000 meters
Equipment Type	Test and measuring
Safety Class	Class 1 (as defined in IEC 61010-1, Annex H) – grounded product
Overvoltage Category	Overvoltage Category II (as defined in IEC 61010-1, Annex J)
Pollution Degree	Pollution Degree 2 (as defined in IEC 61010-1). Rated for indoor use only. Pollution degree is measure of the contaminates that could occur in the environment around and within a product. Typically the internal environment inside a product is considered to be the same as the external. Products should be used only in the environment for which they are rated. Pollution Degree 1 — No pollution or only dry, nonconductive pollution occurs. Products in this category are generally encapsulated, hermetically sealed, or located in clean rooms. Pollution Degree 2 — Normally only dry, nonconductive pollution occurs. Occasionally a temporary conductivity that is caused by condensation must be expected. This location is a typical office/home environment. Temporary condensation occurs only when the product is out of service. Pollution Degree 3 — Conductive pollution, or dry, nonconductive pollution that becomes conductive due to condensation. These are sheltered locations where neither temperature nor humidity is controlled. The area is protected from direct sunshine, rain, or direct wind.
Humidity, operating	80% maximum for temperatures up to 31° C, decreasing linearly to 50% at 40° C (104° F)
Power input	Accepts 100, 115, 220, 230, or 240 VAC ±10%. Automatically switches internally with no user intervention required. CAT II. Instrument accepts ranges from 100 to 240 VAC input (power supply autoranges) through a universal three-conductor instrument plug: this is routed through a line filter internally before being sent to the power supply.

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Performance Verification

Use the following procedures to verify the warranted specifications of the GBIC Test System. Before beginning these procedures, see page 45; photocopy the test record and use it to record the performance test results. The recommended calibration interval is one year.

These procedures test the following specifications:

- Tx DATA, CLK, and SYNC voltage swing
- Rx recovered DATA and CLK voltage swing
- Tx DATA duty cycle
- Random and deterministic jitter
- GBIC PORT V_{dd} Voltage Tolerance

Prerequisites

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- The cabinet must be installed on the GBIC Test System.
- The GBIC Test System outputs must be terminated in a load of 50 $\pm$ 2 Ω.
- The GBIC Test System must have been last calibrated/adjusted at an ambient temperature between +20° C and +30° C, must have been operating for a warm-up period of at least 20 minutes, and must be operating in an environment with temperature, altitude, humidity, and vibration within the operating limits described in *Environmental Specifications* on page 37.

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Equipment Required

Table 18 lists the equipment required to perform the performance verification procedure. The types and quantities of connectors may vary depending on the specific equipment you use.

Table 18: Test equipment

Description	Minimum requirements	Example product
Sampling oscilloscope with sampling head	Bandwidth: 6 GHz Jitter: < 2.1 ps at 25 ns delay	11801C or CSA803C with SD-22 sampling head, V-K adapter and rigid cable.
Semi-rigid cable (2)	for use with SD-22 sampling head	015-0560-00
Cable, coax (3)	50 Ω, SMA male each end	174-1341-00
Power splitter	50 Ω	Tektronix 015-1014-00
GBIC	1.25 GB/s	Tektronix 119-6112-00
Digital voltmeter	4 1/2 digit, ± 1% at 5 Vdc	Tektronix DMM150, TX1 or TX3
Optical cable	SC-SC multimode	Fiber Instrument Sales SC-SC:S3-YYS-1-FIS or SC-SC:Ss-77M-1-FIS

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GTS1250 GBIC Test System Test Record

Photocopy this form and use it to record the performance test results.

Test Record

Instrument Serial Number: _____ Certificate Number: _____

Temperature: _____ Relative Humidity %: _____

Date of Calibration: _____ Technician: _____

Performance Test	Minimum	Incoming	Outgoing	Maximum
<Test name>				
Tx DATA Voltage Swing, D21.5	300 mV_{pp}	_____	_____	600 mV_{pp}
Tx $\overline{DATA}$ Voltage Swing, D21.5	300 mV_{pp}	_____	_____	600 mV_{pp}
Tx DATA Voltage Swing, K28.7	300 mV_{pp}	_____	_____	600 mV_{pp}
Tx $\overline{DATA}$ Voltage Swing, K28.7	300 mV_{pp}	_____	_____	600 mV_{pp}
Tx CLK Voltage Swing	300 mV_{pp}	_____	_____	600 mV_{pp}
Tx SYNC Voltage Swing	300 mV_{pp}	_____	_____	600 mV_{pp}
Rx Recovered DATA Voltage Swing (Option 01 only, D21.5)	300 mV_{pp}	_____	_____	600 mV_{pp}
Rx Recovered CLK Voltage Swing (Option 01 only, D21.5)	300 mV_{pp}	_____	_____	600 mV_{pp}
Rx Recovered DATA Voltage Swing (Option 01 only, K28.7)	300 mV_{pp}	_____	_____	600 mV_{pp}
Tx DATA Duty Cycle	49%	_____	_____	51%
Tx $\overline{DATA}$ Duty Cycle	49%	_____	_____	51%
Data-to-Clock Random Jitter	———	_____	_____	4 ps RMS; 35 ps pp
Data-to-SYNC Deterministic Jitter	———	_____	_____	40 ps DJ_{pp}
Rx Recovered Clock-to-Data Random Jitter (Option 01 only)	———	_____	_____	8 ps RMS
GBIC PORT V_{dd} Voltage Tolerance	4.85 V	_____	_____	5.15 V

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Setup For PV

1. The GTS1250 and the test equipment should be warmed up for 20 minutes at an ambient temperature between 20 and 30° C.
2. Calibrate the loop gain and offset of both sampling head channels. See your oscilloscope and sampling head user manuals for more information.
3. When inputs or outputs of the GBIC Test System are not in use, replace the 50 Ω terminations.

Tx DATA, CLOCK, and SYNC Output levels

Equipment required	One sampling oscilloscope with SD22 sampling head Two Semi-rigid cables for SD22 sampling head One coaxial cable One optical cable GBIC, 1.25 GB/s Power splitter
Prerequisites	See page 43

NOTE. *Make sure that the optical connector ends of both the fiber and the input to the GTS1250 are well cleaned before performing this step.*

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.

NOTE. *The longer wavelengths of 1310 nm and especially 1550 nm are sensitive to loss in fiber due to bending of the fiber. The fiber bend radius of the GTS1250 fiber input should lay with >1.5 inch bend radius along the fiber's entire length. This precaution must be maintained throughout the entire performance verification procedure.*

2. Connect the optical fiber between the Tx and Rx connectors of the GBIC.
3. Connect an SMA cable between the Sync output of the GBIC Test System and the oscilloscope Ext trigger input as shown in Figure 17.

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4. Connect SMA cables between the Tx DATA and Tx $\overline{\text{DATA}}$ outputs of the GBIC Test System and the SD-22 inputs of the oscilloscope as shown in Figure 17.

5. Set the GBIC Test System Transmit pattern to D21.5.

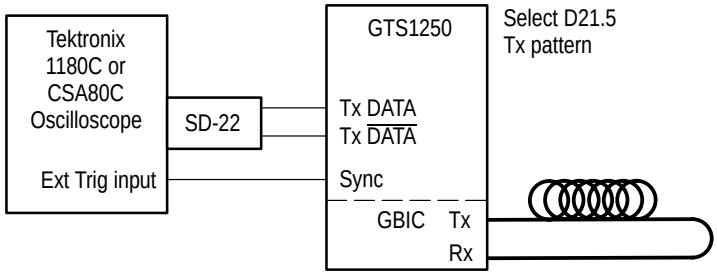


Figure 17: Tx Data levels (swing)

6. Perform the initial setup of the oscilloscope using the following steps:

   a. Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.

   b. From the Trigger major menu, set the trigger source to external.

   c. Set the trigger level to 0.0 V; set the trigger polarity to positive edge.

   d. Display both SD-22 channels.

   e. Set the Vertical Size of both channels to 100 mV/div.

   f. Set the Horizontal Size to 500 ps/div.

   g. Select the WAVEFORM menu, and select the Horizontal Desc. menu.

   h. Set the oscilloscope record length to 512 points.

   i. Set the oscilloscope to 32 averages on both channels.

   j. Select the DISPLAY MODES menu.

   k. Select the Persist/Histograms pop-up menu, select the Normal menu, and then select Exit.

***NOTE**. For increased accuracy, you may perform a LOOP Gain adjustment of the SD22 head on the oscilloscope. If you need instructions, refer to the oscilloscope and SD22 user manuals.*

7. Perform the test with the following sequence on the oscilloscope:

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a. Select the MEASURE menu and then the Measurements pop-up menu.

b. Select the Pk-Pk measurement, and then select Exit.

c. Select Pk-Pk on the menu screen.

d. Verify that, after 32 acquisitions have completed, the Mean value of the amplitude measurement for both the Tx DATA and Tx $\overline{\text{DATA}}$ channels is >300 mV and <600 mV. Record the value on the test record.

e. Set the Transmit Pattern to K28.7.

f. Set the Horizontal Size to 2 ns/div.

g. Verify that, after 32 acquisitions have completed, the Mean value of the amplitude measurement for both Tx DATA and Tx $\overline{\text{DATA}}$ channels is >300 mV and <600 mV. Record the values on the test record.

8. Remove the SMA cables from the Tx DATA and Tx $\overline{\text{DATA}}$ outputs of the GBIC Test System. When inputs or outputs are not in use, replace the 50 Ω terminations. Connect an SMA cable between the Tx CLK output of the GBIC Test System and the SD-22 input of the oscilloscope as shown in Figure 18.

a. Set the Horizontal Size to 500 ps/div.

9. Verify that, after 32 acquisitions have completed, the Mean value of the amplitude measurement is >300 mV and <600 mV. Record the value on the test record.

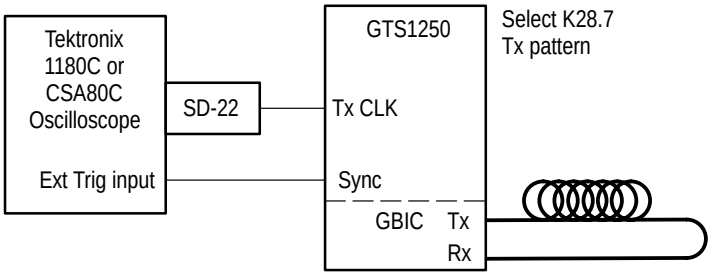


Figure 18: Tx CLK levels

10. Remove the SMA cable from the Tx CLK outputs of the GBIC Test System. Remove the SMA cable from the Ext Trig input of the oscilloscope. Connect an SMA cable between the SYNC output of the GBIC Test System and a power splitter. Connect an SMA cable from the power splitter to the SD-22 input of the oscilloscope as shown in Figure 19. Connect an SMA cable from the power splitter to the Ext Trig input of the oscilloscope.

11. Set the Horizontal Size to 5 ns/div.

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12. Verify that, after 32 acquisitions have completed, the Mean value of the amplitude measurement is > 150 mV and < 300 mV (one half of the specification due to the attenuation of the power splitter). Record the value on the test record.

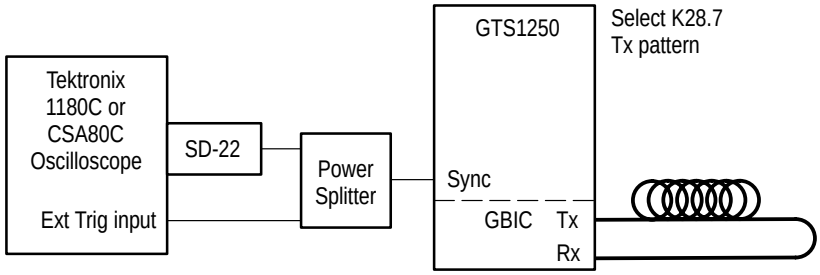


Figure 19: SYNC levels

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Recovered Data and Clock Output Levels (Option 01 Only)

Equipment required	One sampling oscilloscope with SD22 sampling head Two Semi-rigid cables for SD22 sampling head One optical cable One coaxial cable GBIC, 1.25 GB/s
Prerequisites	See page 43

***NOTE**. Make sure that the optical connector ends of both the fiber and the input to the GTS1250 are well cleaned before performing this step.*

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.

***NOTE**. The longer wavelengths of 1310 nm and especially 1550 nm are sensitive to loss in fiber due to bending of the fiber. The fiber bend radius of the GBIC Test System fiber input should lay with >1.5 inch bend radius along the entire length of the fiber. This precaution must be maintained throughout the entire performance verification procedure.*

2. Install the GBIC and connect the appropriate optical fiber between the Tx and Rx connectors of the GBIC.
3. Connect an SMA cable between the Sync output of the GBIC Test System and the oscilloscope Ext trigger input as shown in Figure 20.
4. Connect an SMA cable between the RECOV DATA output of the GBIC Test System and the upper SD-22 input of the oscilloscope, and connect another cable between the RECOV CLK output of the GBIC Test System and the lower SD-22 input of the oscilloscope as shown in Figure 20.
5. Set the GBIC Test System Transmit pattern to D21.5.

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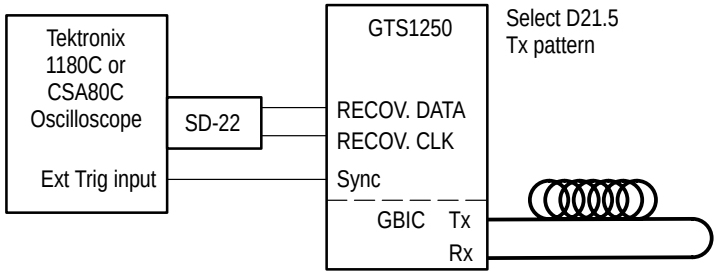


Figure 20: Recovered clock and data levels

6. Perform the initial setup of the oscilloscope using the following steps:

a. Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.

b. From the Trigger major menu, set the trigger source to external.

c. Set the trigger level to 0.0 V; set the trigger polarity to positive edge.

d. Set the Vertical Size to 100 mV/div.

e. Set the Horizontal Size to 500 ps/div.

f. Set the oscilloscope record length to 512 points.

g. Set the oscilloscope to 32 averages on both channels.

***NOTE**. For increased accuracy, you may perform a LOOP Gain adjustment of the SD22 head on the oscilloscope. If you need instructions, refer to the oscilloscope and SD22 user manuals.*

7. Perform the test with the following sequence on the oscilloscope:

a. Select the MEASURE menu and then the Measurements pop-up menu.

b. Set the Pk-Pk measurement to measure both the Recov. CLK and RECOV DATA waveforms, and then select Exit.

c. Select Pk-Pk on the menu screen.

d. Verify that, after 32 acquisitions have completed, the Mean value of the amplitude measurements on both channels are >300 mV and <600 mV. Record the values for both channels on the test record.

8. Set the GBIC Test System Transmit pattern to K28.7.

9. Set the Horizontal Size to 2 ns/div.

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10. Verify that, after 32 acquisitions have completed, the Mean value of the RECOV DATA amplitude measurement is > 300 mV and < 600 mV. Record the value on the test record.

Tx Data Duty Cycle

Equipment required	One sampling oscilloscope with SD22 sampling head Two Semi-rigid cables for SD22 sampling head One optical cable GBIC, 1.25 GB/s One coaxial cables
Prerequisites	See page 43

NOTE. *Make sure that the optical connector ends of both the fiber and the input to the GTS1250 are well cleaned before performing this step.*

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.

NOTE. *The longer wavelengths of 1310 nm and especially 1550 nm are sensitive to loss in fiber due to bending of the fiber. The fiber bend radius of the GTS1250 fiber input should lay with >1.5 inch bend radius along the fiber's entire length. This precaution must be maintained throughout the entire performance verification procedure.*

2. Install a GBIC in the GBIC Test System, and connect the optical fiber between the Tx and Rx connectors of the GBIC.
3. Connect SMA cables between the GBIC Test System and the oscilloscope as shown in Figure 21.
4. Set the GBIC Test System Transmit pattern to PRBS7.

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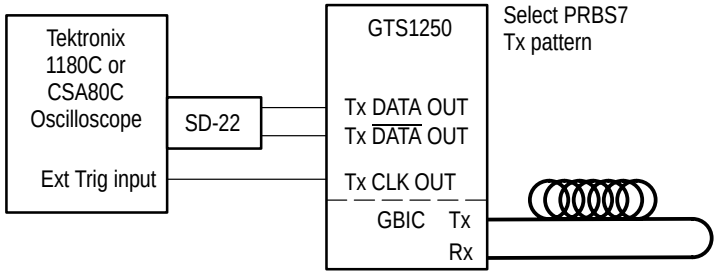


Figure 21: Tx Data duty cycle

5. Perform the initial setup of the oscilloscope using the following steps:

   a. Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.

   b. From the Trigger major menu, set the trigger source to external.

   c. Set the trigger level to 0.0 V; set the trigger polarity to positive edge.

   d. Display an Tx DATA OUT signal.

   e. Set the Vertical Size to 100 mV/div.

   f. Set the Vertical Offset to 0 V.

   g. Set the Horizontal Size to 200 ps/div.

   h. Set the main Horizontal Position to < 100 ns

   i. Set the oscilloscope record length to 512 points.

   j. Select the DISPLAY MODES menu.

   k. Select the Persist/Histograms pop-up menu, select the Color Grading, and then select Exit.

   l. Acquire the Tx DATA signal.

***NOTE**. For increased accuracy, you may perform a LOOP Gain adjustment of the SD22 head on the oscilloscope. If you need instructions, refer to the oscilloscope and SD22 user manuals.*

6. Perform the test with the following sequence on the oscilloscope:

   a. Select the MEASURE menu and then change the measurement method to Statistics Mode.

   b. Select the MEASURE menu and then the Measurements pop-up menu.

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c. Select the DUTY CYCLE measurement, and then select Exit.

d. Touch the Duty Cycle measurement box to expand the box. Set the LEVEL MODE to ABSOLUTE, and set MESIAL to 0 V.

e. Verify that, after the measurement settles, the duty cycle measurement for Tx DATA OUT is ≥ 49% and ≤ 51%. Record the value on the test record.

f. Remove the Tx DATA OUT signal from the display and instead display the Tx $\overline{\text{DATA}}$ OUT signal.

g. Repeat steps 5a through 6d

h. Verify that, after the measurement settles, the duty cycle measurement for Tx $\overline{\text{DATA}}$ OUT is ≥ 49% and ≤ 51%. Record the value on the test record.

Tx Clock to Data Random Jitter

Equipment required	One sampling oscilloscope with SD22 sampling head Semi-rigid cable for SD22 sampling head Coaxial cable
Prerequisites	See page 43

NOTE. *Make sure that the optical connector ends of both the fiber and the input to the GTS1250 are well cleaned before performing this step.*

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.

NOTE. *The longer wavelengths of 1310 nm and especially 1550 nm are sensitive to loss in fiber due to bending of the fiber. The fiber bend radius of the GTS1250 fiber input should lay with >1.5 inch bend radius along the fiber's entire length. This precaution must be maintained throughout the entire performance verification procedure.*

2. Connect an SMA cable between the Tx DATA output of the GBIC Test System and the oscilloscope Ext trigger input as shown in Figure 22.

3. Connect an SMA cable between the Tx CLK output of the GBIC Test System and the SD-22 input of the oscilloscope as shown in Figure 22.

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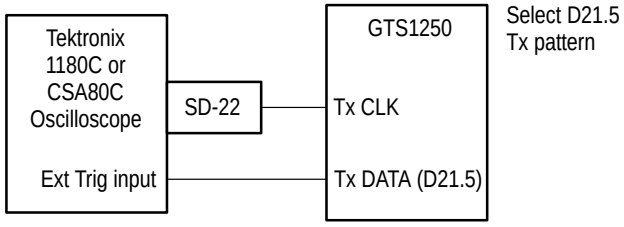


Figure 22: Tx Clock to Data Random Jitter Test Setup

4. Set the GBIC Test System Transmit pattern to D21.5.
5. If a GBIC is installed in the GBIC Test System, disconnect or turn off any signal going into the receive side of the GBIC; disconnect any signals attached to the +Rx DATA and –Rx DATA connectors.
6. Perform the initial setup of the oscilloscope using the following steps:
   a. Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.
   b. From the Trigger major menu, set the trigger source to external.
   c. Set the trigger level to 0.0 V; set the trigger polarity to positive edge.
   d. Display the Tx CLK OUT signal.
   e. Set the Vertical Size to 50 mV/div.
   f. Set the Horizontal Size to 100 ps/div.
   g. Set the oscilloscope record length to 512 points.
7. Perform the test with the following sequence on the oscilloscope:
   a. Find a rising clock edge that is displayed between 20 to 30 ns horizontal timing position (if you need to adjust the position, select the horizontal and adjust the lower Horizontal knob to adjust the horizontal timing position); adjust the waveform so that the 50% rising edge crossing point of the clock signal is at the center of the graticule grid (see Figure 23) of the oscilloscope display (to adjust the position, select the horizontal or vertical and adjust using the lower knob).

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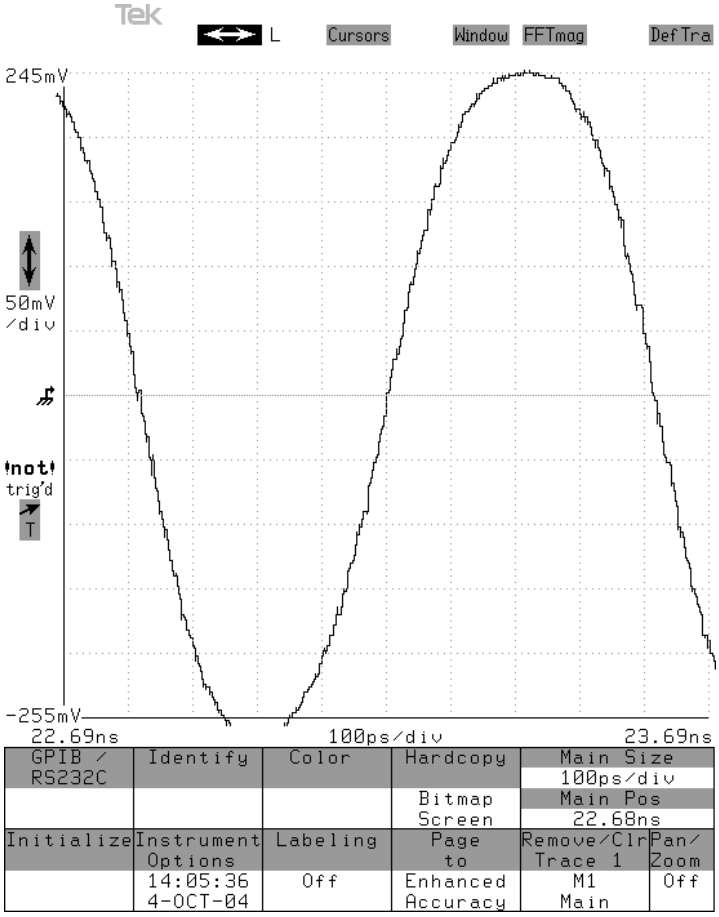


Figure 23: Centered rising edge

b. Select the WAVEFORM menu and then the Horizontal Desc pop-up menu.

c. Set the Horizontal positioning mode to expand about the CENTER.

d. Set the Vertical Size to 5 mV/div; set the Horizontal Size to 5 ps/div; if the waveform was not properly centered, adjust the horizontal position slightly to maintain the edge crossing near the center the the display.

e. Define a horizontal histogram across the middle of the display with a height of 1 mV (see Figure 24). Set the display mode to STOP on N waveforms where N is set to 1000; touching the STOP ON N button in the DISPLAY MENU will begin an infinite persistence acquisition of the waveform which will stop acquiring after 1000 waveforms have been accumulated.

f. Along the bottom of the display, note the RMS (that is, standard deviation) value of the resulting histogram result. This is the horizontal

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RMS jitter of the Clock to Data; Verify that the jitter value is < 4 ps RMS and < 35 ps peak-to-peak.

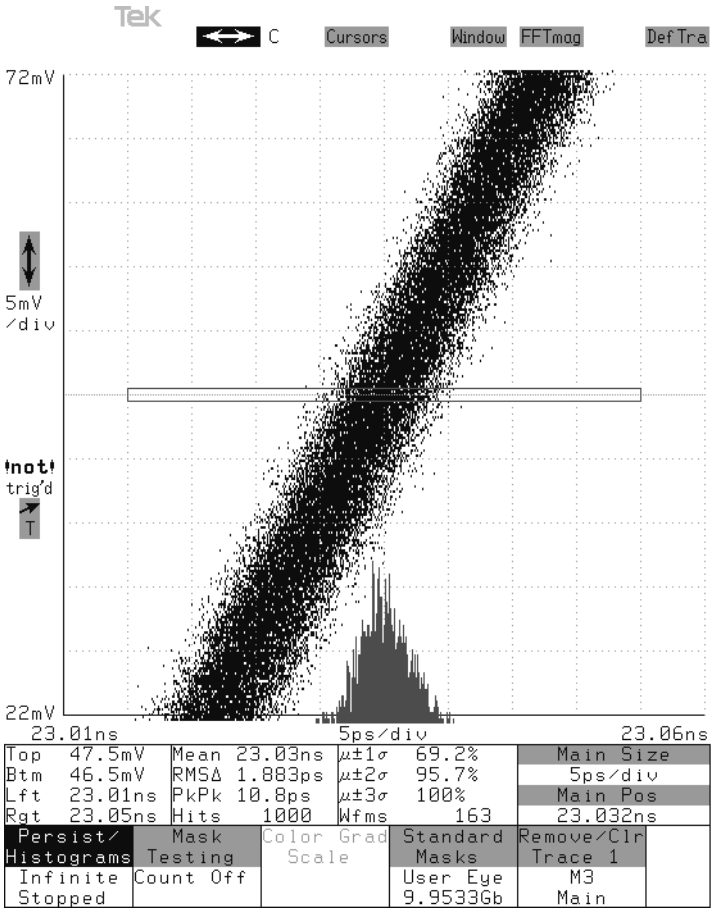


Figure 24: Random jitter histogram

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Fast Deterministic Jitter

This procedure is a quick check of deterministic jitter. Use this procedure to verify a PASS condition for a GBIC Test System deterministic jitter. If this procedure yields a deterministic jitter result which exceeds the specification, you must then perform the longer ten edge procedure starting on page 61 in order to accurately determine whether a PASS or FAIL condition exists.

Equipment required	One sampling oscilloscope with an SD22 sampling head One Semi-rigid cable for sampling head One coaxial cables
Prerequisites	See page 43

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.
2. Connect an SMA cable between the Tx DATA output of the GBIC Test System and the SD-22 input of the oscilloscope as shown in Figure 25.
3. Connect an SMA cable between the the Tx CLK output of the GBIC Test System and the oscilloscope Ext trigger input.

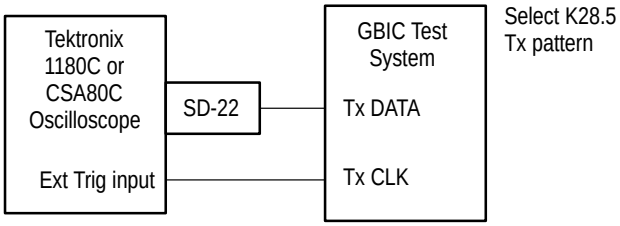


Figure 25: Tx Data Deterministic Jitter Test Setup

4. Set the GBIC Test System Transmit pattern to K28.5.
5. Perform the initial setup of the oscilloscope using the following steps:
   - **a.** Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.
   - **b.** From the Trigger major menu, set the trigger source to external.
   - **c.** Set the trigger level to 0.0 V; set the trigger polarity to positive edge.
   - **d.** Display the SD-22 channel.
   - **e.** Set the Vertical Size to 100 mV/div.

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f. Set the Vertical Offset to 0.0 V/div.

g. Set the Horizontal Size to 500 ps/div.

h. Set the Main Position to any value less than 50 ns.

i. Set the oscilloscope record length to 512 (maximum) points.

j. Set the oscilloscope horizontal positioning mode to expand about the CENTER.

k. Select the WAVEFORM menu and then the Sampling Head Fnc's pop-up menu. Set Smoothing to Off.

l. Select the UTILITY menu and then the Instrument Options pop-up menu. Set Vectored Trace to Off.

m. Use the oscilloscopes controls, place the resulting Tx Data eye pattern on the display such that the crossing of the eye is at the very center of the display.

n. Adjust the oscilloscope controls to expand the displayed waveform such that the vertical scale is 20 mV per division and the horizontal scale is 10 ps per division. While expanding the waveform, readjust the horizontal and vertical controls to maintain the crossing of the eye at the center of the display.

o. Set the oscilloscopes DISPLAY MODE to generate a horizontal histogram. Select and then adjust the VERTICAL LIMITS to create a rectangular histogram box 2 mV in vertical height and placed such that it intersects across the crossing of the eye (see Figure 26).

6. Perform the test with the following sequence on the oscilloscope:

a. Expand the Persistence/Histogram menu. Set the STOP on N waveforms mode to 100 waveforms. Select the STOP on N waveforms mode (this will cause the oscilloscope to start a new persistence acquisition in which the oscilloscope stops acquiring after 100 waveforms are acquired).

***NOTE**. If this fast method yields a result which might indicate marginal deterministic jitter performance, use the ten edge method for determining the true deterministic jitter of the K28.5 pattern.*

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b. The eye pattern crossing contains the total jitter of the GBIC Test System Tx DATA output. This jitter is comprised mainly of deterministic and random jitter. The random jitter adds to the total peak-to-peak jitter, and as such the total jitter measured is always greater than the deterministic jitter alone. Deterministic jitter can be estimated by measuring the horizontal distance between the left-most local-maxima and right-most local-maxima peak distributions of the histogram. If the displayed peak-to-peak jitter is less than the deterministic jitter specification (40 ps), then the GBIC Test System deterministic jitter is within specification. For example, if the GBIC Test System outputs a deterministic jitter of 20 ps peak-to-peak and a random jitter of 12 ps peak-to-peak, then the peak-to-peak result of an eye crossing histogram on such a signal yields approximately 20 ps +12 ps = 32 ps peak-to-peak distribution.

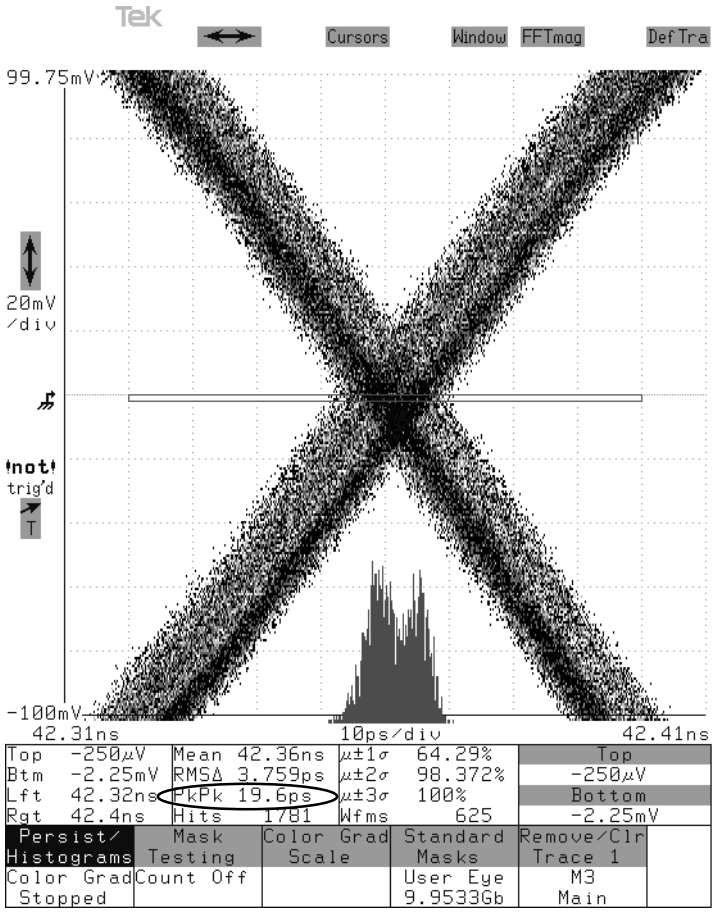


Figure 26: Histogram deterministic jitter measurement

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Tx DATA to SYNC OUT Deterministic Jitter

If you performed the previous procedure, skip this procedure. This ten edge deterministic jitter test is a lengthy test to perform manually, yet it provides an accurate result for K28.5 deterministic jitter. If you desire a quicker check of deterministic jitter, use the *Fast Deterministic Jitter* procedure on page 58.

Equipment required	One sampling oscilloscope with an SD-22 sampling head One Semi-rigid cable for sampling head Two coaxial cables
Prerequisites	See page 43

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.
2. Connect an SMA cable between the the SYNC OUT of the GBIC Test System and the oscilloscope Ext trigger input.
3. Connect an SMA cable between the Tx DATA output of the GBIC Test System and the SD-22 input of the oscilloscope as shown in Figure 27.

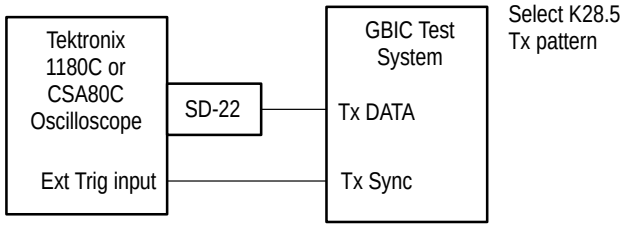


Figure 27: Tx Data Deterministic Jitter Test Setup

4. Set the GBIC Test System Transmit pattern to K28.5.
5. Perform the initial setup of the oscilloscope using the following steps:
   a. Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.
   b. From the Trigger major menu, set the trigger source to external.
   c. Set the trigger level to 0.0 V; set the trigger polarity to positive edge.
   d. Display the SD-22 channel.
   e. Set the Vertical Size to 100 mV/div.

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f. Set the Vertical Offset to 0.0 V/div.

g. Set the Horizontal Size to 2 ns/div.

h. Set the oscilloscope record length to 5120 (maximum) points.

6. Perform the test with the following sequence on the oscilloscope:

a. Acquire the signal so that the first instance of the rising edge followed by 4UI of high level (that is a 5-bit consecutive high sequence in the data pattern) occurs midway in the first graticule on the left side of the display (see Figure 28). This edge is the first positive going transition in a K28.5-disparity 10-bit code group.

The figure shows the repeating Deterministic Jitter Test Pattern (K28.5) and the oscilloscope crossing measurement being used to determine the position of the first crossing point (edge #0: this point is used as the reference crossing for the next 5 falling edges and 4 more rising edges)

NOTE. *The K28.5 Tx Pattern is a repeating 10-bit K28.5 —disparity code group followed by a 10-bit K28.5 +disparity code group which results in a 20-bit repeating pattern. Each instance of the 20-bit pattern in the waveform contains 5 positive going rising edges and 5 negative going falling edges. The following procedure measures the relative occurrence of the 50% crossover point of each of these edges relative to the rising edge in the middle of the first graticule (known as edge #0 with a crossing time of T0). The term UI in the procedure refers to* Unit Interval *and is the width of a single data bit (that is a 1250 Mb/s NRZ data stream from a GTS1250 will have an ideal UI of 800 ps, while a 1062.5 Mb/s NRZ data stream from a GTS1063 will have an ideal UI of 941.176 ps).*

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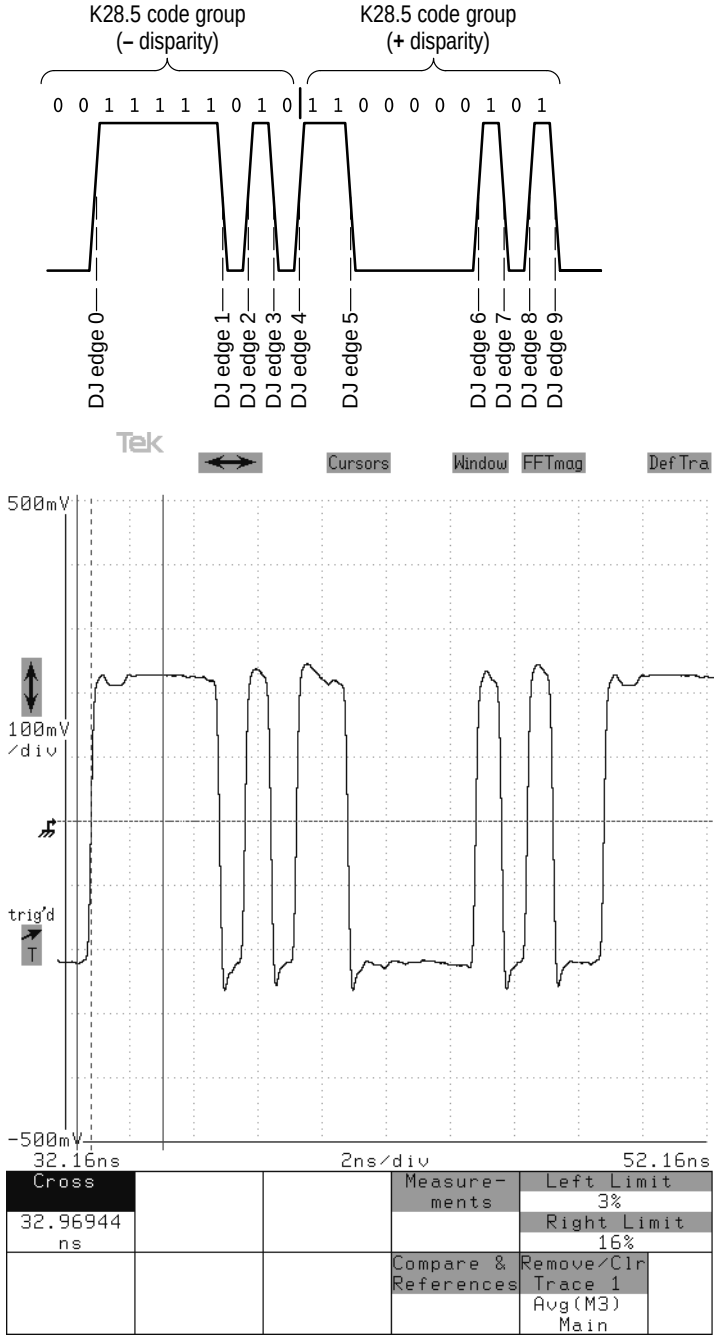


Figure 28: K28.5-disparity 10-bit code group with rising edge in first graticule

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b. Average the signal 32 times.

c. Select the CROSS measurement for the DATA waveform.

- Touch the CROSS result in the bottom of the display to expand the control box for the CROSS parameters (see Figure): set the crossing LEVEL MODE to ABSOLUTE and the REF LEVEL to 0.0 Volts. The LEFT and RIGHT limits, after being touched, are controlled by the two knobs at the lower right of the display.
- Set the crossing slope (in the expanded CROSS parameter window) to +.

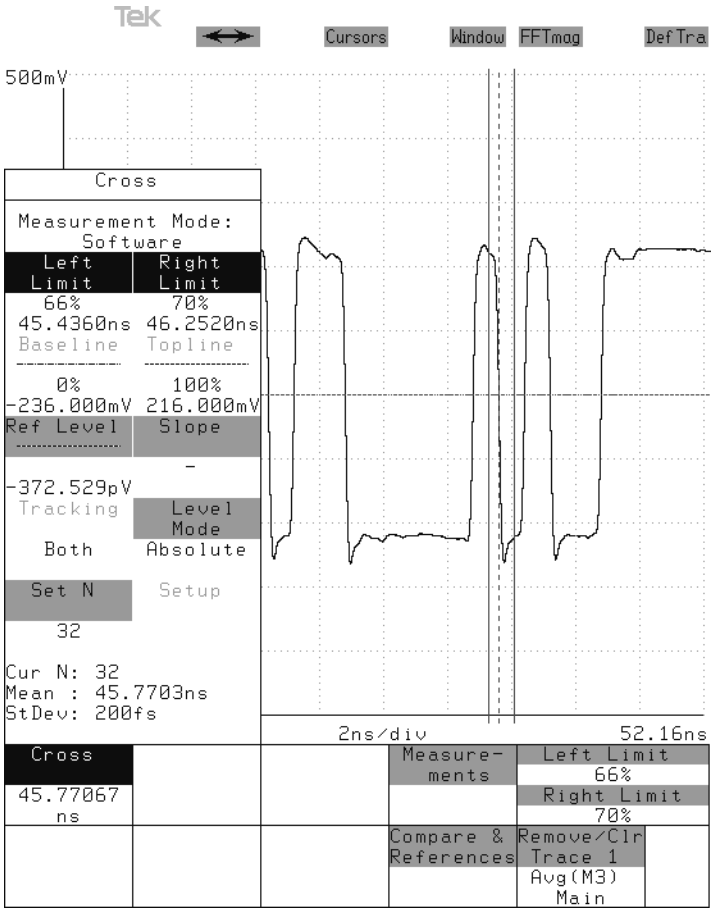


Figure 29: Expanded Cross measurement setup and test patten falling edge

- Adjust the LEFT and RIGHT limits such that the first rising edge (edge #0) is the only edge between these limits.

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- Allow the averaging of the CROSS result to settle (that is the StDev: after several seconds, the standard deviation in the expanded CROSS parameter window will settle below a picosecond) and record the mean result of the crossing: this is the first edge (edge #0) and is used as the timing reference for all subsequent nine transition edges.

NOTE. *Since the final result of this portion of the procedure is a peak-to-peak measurement, the result will be the same no matter which of the 10 transition edges in the 20-bit K28.5 pattern are used as the reference timing edge.*

- For each of the nine edges (rising or falling) following edge #0, adjust the LEFT and RIGHT limits to isolate each edge for a similar CROSS result: specify the correct slope (+ for rising, or — for falling) manually for each CROSS measurement or else the measurement result will be an ERROR.

7. Record the results of the CROSS measurements for all ten consecutive edges in Table 19. The ideal crossing location for each edge is in the table to the right of the measured values: the ideal crossing locations following reference edge #0 are integer multiples of the UI bit period added onto the reference edge. For example: if the first edge #0 of a GTS1250 occurs at 32.969 ns, then the next edge, which occurs 5 UI later in this example, has an ideal location of 32.969 ns + (5 x 800 ps) = 36.969 ns. The unit interval (UI) is the inverse of the data rate: the GTS1063 has a data rate of 1.0625 Gb/s and therefore its UI = 941.176 ps, the GTS1250 has a data rate of 1.2500 Gb/s and therefore its UI = 800.000 ps. Table 20 shows example measurement data for determining the deterministic jitter of the Tx Data output.

a. The error between each measured edge and its ideal location is determined by subtracting the exact location from the measured location. note: since edge #0 is used as the reference, its ideal location and its measured location are the same and hence have zero error.

b. Add the magnitude of the largest positive and largest negative error to yield the peak-to-peak deterministic jitter in the K28.5 test pattern (example: +5 ps error and –3 ps error yield 8 ps_{p-p}). The calculated peak-to-peak error should be < 40 ps.

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Table 19: Deterministic Jitter Calculation

Edge number	Bit periods after edge (T0)	Measured 50% crossing	Ideal (zero DJ) position of edge crossing (calculated)	Error (Deterministic jitter) in edge position relative to ideal perfect position (measured–ideal)
0	0		(T0)+(0xUI)=	0 (the reference edge)
1	5		(T0)+(5xUI)=	
2	6		(T0)+(6xUI)=	
3	7		(T0)+(7xUI)=	
4	8		(T0)+(8xUI)=	
5	10		(T0)+(10xUI)=	
6	15		(T0)+(15xUI)=	
7	16		(T0)+(16xUI)=	
8	17		(T0)+(17xUI)=	
9	18		(T0)+(18xUI)=	
				DJ = peak-peak error =

Table 20: Example Deterministic Jitter Calculation

Edge number	Bit periods after edge (T0)	Measured 50% crossing (example data)	Ideal perfect (zero DJ) position of edge crossing	Error (Deterministic jitter) in edge position relative to ideal perfect position (measured–ideal)
0	0	32.973 ns (T0)	(T0)+(0xUI)= 32.973 ns	0 (the reference edge)
1	5	36.974 ns	(T0)+(5xUI)= 36.973 ns	+1 ps
2	6	37.776 ns	(T0)+(6xUI)= 37.773 ns	+3 ps
3	7	38.577 ns	(T0)+(7xUI)= 38.573 ns	+4 ps
4	8	39.378 ns	(T0)+(8xUI)= 39.373 ns	+5 ps
5	10	40.973 ns	(T0)+(10xUI)= 40.973 ns	0.0 ps
6	15	44.972 ns	(T0)+(15xUI)= 44.973 ns	–1 ps
7	16	45.770 ns	(T0)+(16xUI)= 45.773 ns	–3 ps
8	17	46.576 ns	(T0)+(17xUI)= 46.573 ns	+3 ps
9	18	47.375 ns	(T0)+(18xUI)= 47.373 ns	+2 ps
				DJ = peak-peak error = (+5 ps – (–3 ps)) = 8 ps

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Recovered Clock to Data Random Jitter

Equipment required	One sampling oscilloscope with SD22 sampling head Semi-rigid cable for SD22 sampling head One coaxial cables One optical cable GBIC, 1.25 GB/s
Prerequisites	See page 43

***NOTE**. Make sure that the optical connector ends of both the fiber and the input to the GTS1250 are well cleaned before performing this step.*

1. Connect your wrist strap to the antistatic connector on the front of your oscilloscope.
2. Install a GBIC in the GBIC Test System, and connect the optical fiber between the Tx and Rx connectors of the GBIC.

***NOTE**. The longer wavelengths of 1310 nm and especially 1550 nm are sensitive to loss in fiber due to bending of the fiber. The fiber bend radius of the GTS1250 fiber input should lay with >1.5 inch bend radius along the fiber's entire length. This precaution must be maintained throughout the entire performance verification procedure.*

3. Connect an SMA cable between the RECOV. DATA output of the GBIC Test System and the oscilloscope Ext trigger input as shown in Figure 30.
4. Connect an SMA cable between the RECOV CLK output of the GBIC Test System and the SD-22 input of the oscilloscope as shown in Figure 30.

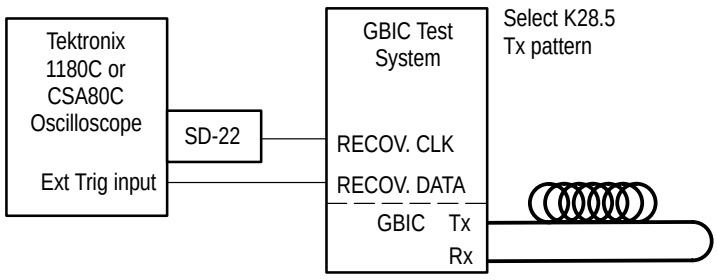


Figure 30: Recovered Clock to Recovered Data Random Jitter Test

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5. Set the GBIC Test System Transmit pattern to K28.5.
6. Perform the initial setup of the oscilloscope using the following steps:
   a. Initialize the oscilloscope to default settings using the Initialize selector which appears in the Utility major menu.
   b. From the Trigger major menu, set the trigger source to external.
   c. Set the trigger level to 0.0 V; set the trigger polarity to positive edge.
   d. Display the SD-22 channel.
   e. Set the Vertical Size to 50 mV/div.
   f. Set the Horizontal Size to 100 ps/div.
   g. Set the oscilloscope record length to 512 points.
7. Perform the test with the following sequence on the oscilloscope:
   a. Find a rising clock edge that is displayed between 20 to 30 ns horizontal timing position; adjust the waveform so that the 50% rising edge crossing point of the clock signal is at the center of the graticule grid of the oscilloscope display.
   b. Set the Horizontal positioning mode to expand about the CENTER.
   c. Set the Vertical Size to 5 mV/div; set the Horizontal Size to 5 ps/div; if the waveform was not properly centered, adjust the horizontal position slightly to maintain the edge crossing near the center the the display.
   d. Define a horizontal histogram across the middle of the display with a height of 1 mV (see Figure 31). Set the display mode to STOP on N waveforms where N is set to 1000; touching the STOP ON N button in the Display menu will begin an infinite persistence acquisition of the waveform which will stop acquiring after 1000 waveforms have been accumulated.
   e. Along the bottom of the display, note the RMS (that is, standard deviation) value of the resulting histogram result. This is the horizontal RMS jitter of the Clock to Data; Verify that the jitter value is < 4 ps RMS and < 35 ps peak-to-peak.

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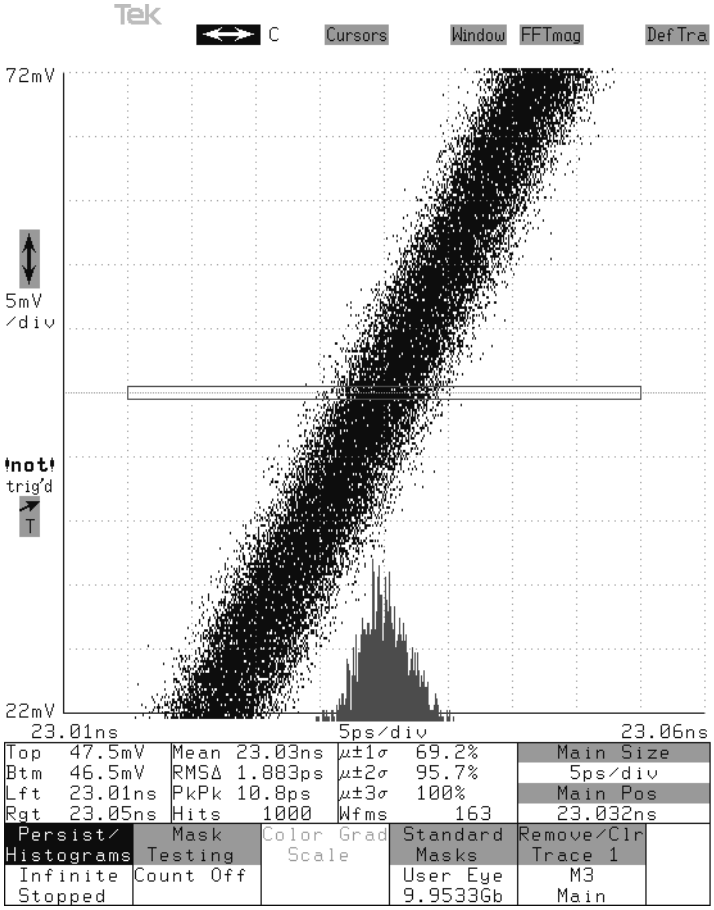


Figure 31: Random jitter histogram

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GBIC Port Vdd default Voltage

Equipment required	Digital multimeter GBIC
Prerequisites	See page 43

NOTE. *Make sure that the optical connector ends of both the fiber and the input to the GTS1250 are well cleaned before performing this step.*

1. Connect your wrist strap to the antistatic connector on your instrument.
2. Install a GBIC into the GBIC port of the GBIC Test System.
3. Power on the GBIC Test System and position it such that the rear-panel Remote Interface is facing you.

NOTE. *During this test no signal should be attached to the rear-panel V_OFF-SET signal.*

4. Connect the DMM common (or GND) lead to pin 25 of the Remote Interface connector (see Figure 32).
5. Connect the V lead of the DMM to pin 22 of the Remote Interface connector (the V_MONITOR signal for the GBIC _5 V supply).
6. Verify that the voltage measurement is >4.85 V and <5.15 V. Record the value on the test record.

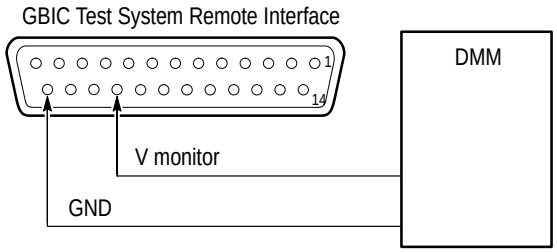


Figure 32: GBIC port Vdd default voltage Test Setup

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WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all safety summaries before performing any service.

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Fuse Removal and Replacement

This section explains how to remove and replace the power supply fuse. All field replaceable parts are listed in *Replaceable Parts*, which begins on page 77.

WARNING. *Disconnect the power cord from the instrument before attempting any disassembly procedures.*

Required Tools

The following tools are required to replace the fuse.

Table 21: Required tools for fuse removal and replacement

Name	Description
Screwdriver handle	Accepts Torx®-driver bits
Torque driver	Accepts Torx bits; can be set up to 4 ft-lb
T-7 Torx tip	Torx-driver bit for T-7 size screw heads

Fuse Replacement

To replace the power supply fuse:

1. Remove the power cord.
2. Remove the 8 screws from the top cover. See Figure 33.
3. Carefully lift the top cover off the bottom cover assembly.

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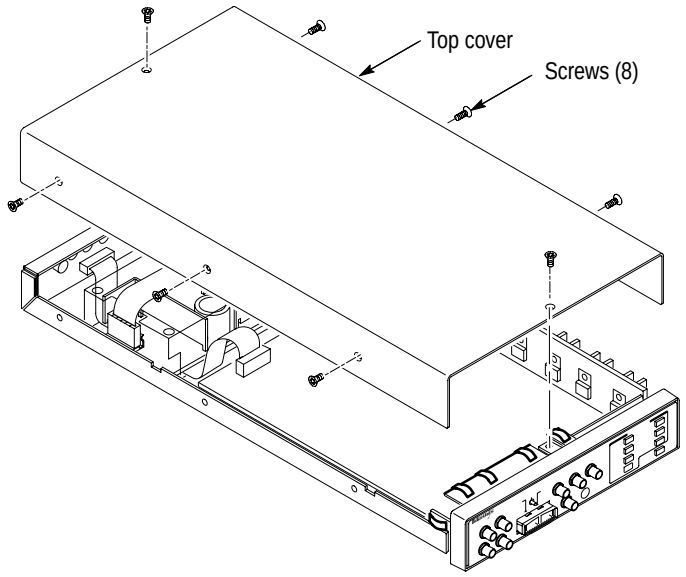


Figure 33: Removing the top cover

Refer to Figure 34 for the following steps:

4. Disconnect the power supply cable from the power supply.
5. Disconnect the TTL remote cable from the main logic board.
6. Carefully lift the clear plastic shield located over the power supply.
7. Replace the fuse cartridge on the Power Supply board with the fuse listed in the *Replaceable Parts* section beginning on page 77.
8. Reposition the power supply shield back over the Power Supply board.
9. Connect the power supply cable to the power supply.
10. Connect the TTL remote cable to the main logic board.
11. Place the top cover on the bottom cover assembly. Check that the plastic power supply shield is tucked inside the bottom cover assembly.
12. Insert the (8) machine screws through the top cover into the bottom cover assembly. Tighten the screws using a torque driver set to 4 ft-lb.
13. If other cables were removed, reinstall them using Table 22 on page 76 as a guide.

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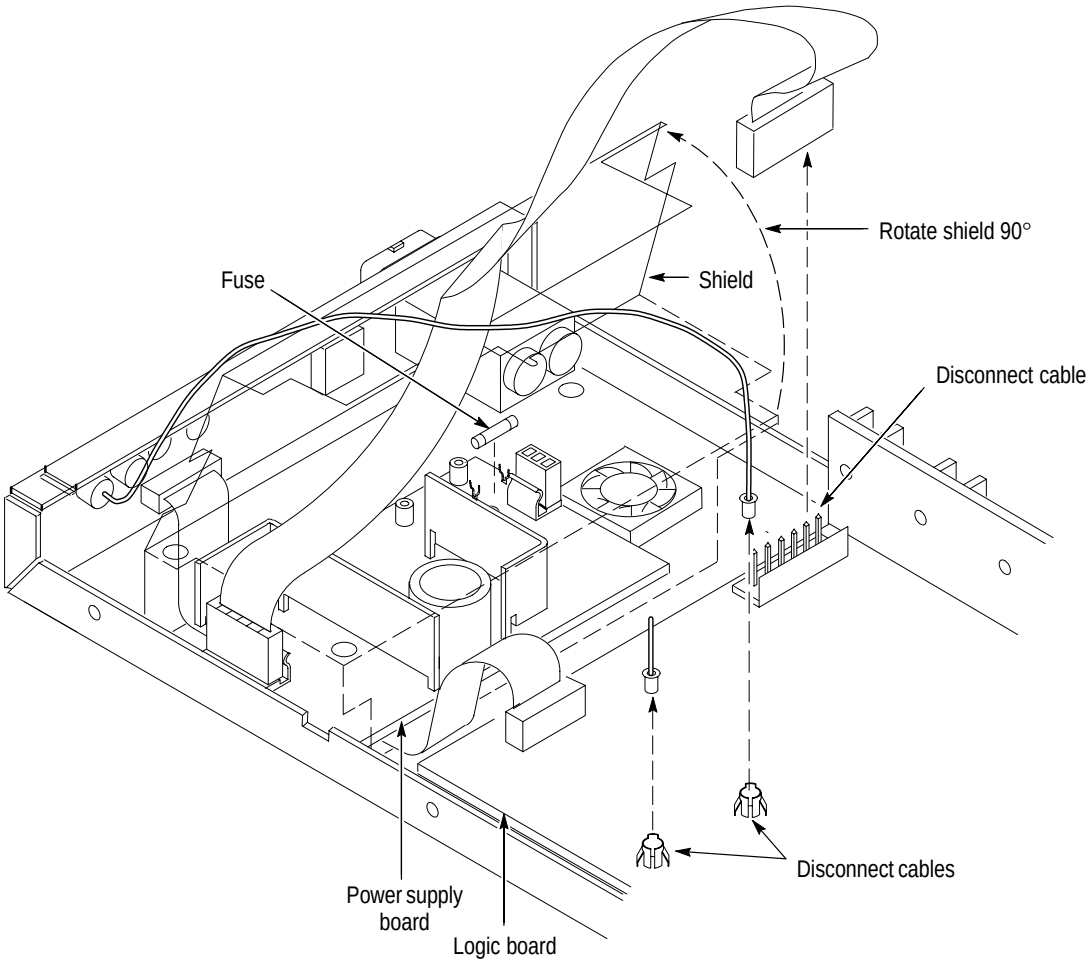


Figure 34: Replacing the fuse

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Table 22: Cable Connections

Panel connector	Board connector J number
RECOV. CLK (Option 01)	J12
RECOV. DATA (Standard)	J17
RECOV. DATA (Option 01)	J13
+Rx DATA	J14
–Rx DATA	J15
EXT DATA IN	J11
Tx DATA OUT	J16
Tx $\overline{\text{DATA}}$ OUT	J24 (The 4 may be covered by a component)
SYNC OUT	J9
Tx CLK OUT	J22
Tx JITTER IN	J6
EXT CLK IN	J23

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Replaceable Parts

For information about replaceable parts, contact your Tektronix sales representative.

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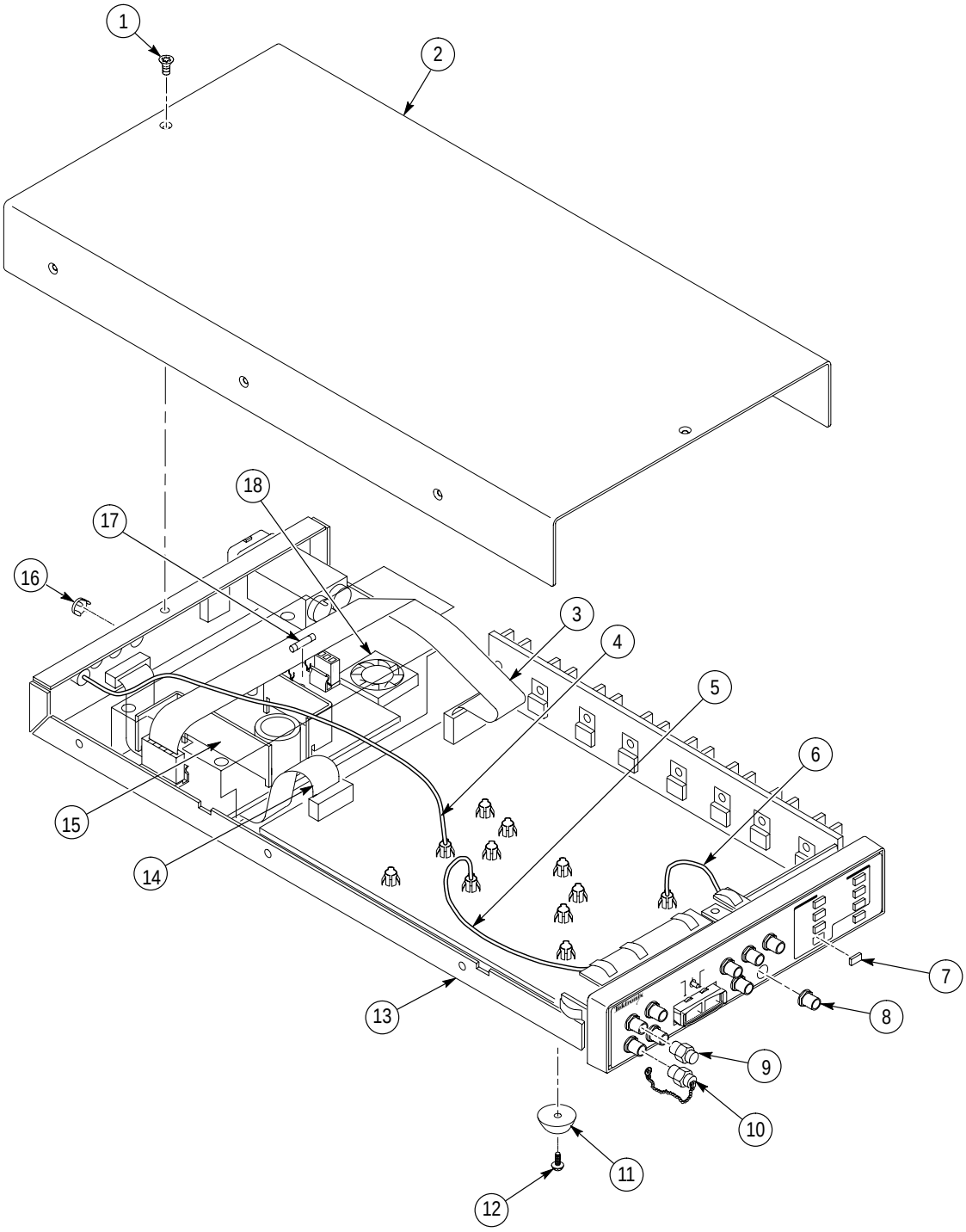


Figure 35: Replaceable parts

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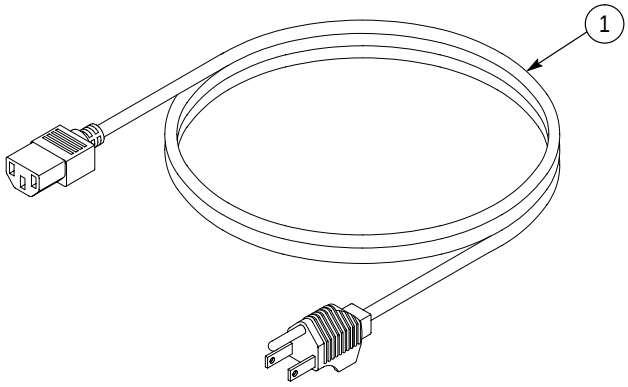


Figure 36: Standard accessories

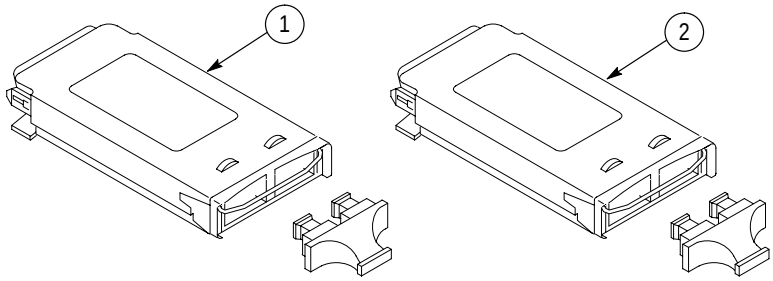


Figure 37: Optional accessories

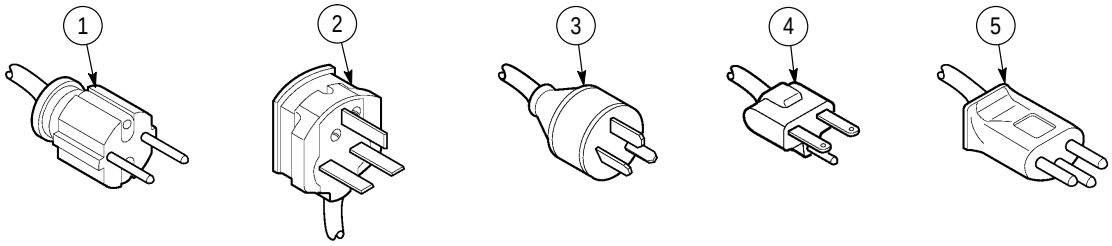


Figure 38: Optional power cords

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Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
35							
–1	211–0303–00			14	SCREW,MACHINE:4–40 X 0.25,FLH 100 DEG,STL CD PL,TORX DR,T7	93907	ORDER BY DESC
–2	200–4465–01			1	COVER,TOP:0.62 AL,CLR CHROMATE,ORS20,	TK1943	200–4465–01
–3	174–4407–00			1	CA ASSY,SP:DISCRETE,PSC,6,18 AWG,13.0 L,0.156 CTR,1 X 6,0.156 CTR,RCPT,W/FRICTION LOCK	060D9	174–4407–00
–4	174–2388–00			3	CA ASSY:COAX,RFP,50Ω,1.08NS +/–50PS,6.0,MALE PELTOLAS	060D9	174–2388–00
–5	175–5534–00			4	CA ASSY,RF:50Ω COAX,6.25 L,9–2,PELTOLA X PELTOLA	060D9	175–5534–00
–6	174–2386–00			4	CABLE ASSY:COAX,RFP,50 OHM,475PS +/–50PS,6–2,MALE PELTOLA BOTH ENDS,MACHINED	060D9	174–2386–00
–7	366–0616–00			8	PUSH BUTTON:0.585 X 0.3 X 0.150	7X318	ORDER BY DESC
–8	103–0269–00			11	ADAPTER,CONN:SMA TO PELTOLA,FEMALE TO FEMALE,STR,PNL,D/FLAT,0.385 MTG HOLE,GOLD/NICKEL	24931	39JR198–1
–9	015–1022–00			1	TERMN,COAXIAL:50 OHM,0.5W,SMA	26805	2001–4401–00
–10	011–0176–00			2	TERM,RF:SMA,PLUG,STR,SST,W/BEAD CHAIN.	16179	2001–6115–02
–11	348–0001–00			4	FOOT,CABINET:BLACK RUBBER	TK2208	ORDER BY DESC
–12	211–0730–00			1	SCR,MACHINE,W/WSHR:6–32 X 0.375,PNH,STL, CDPL,T–15	0KB01	ORDER BY DESC
–13	200–4563–00			1	COVER,BOTTOM:AL,TEK BLUE PAINT,ORS20	TK1943	200–4563–00
–14	174–4332–00			1	CA ASSY,REMOTE JUMPER,RIBBON,28AWG, 112CTR,25POS,DSUB,FEMALE,STR2X13	80009	174–4332–00
–15	119–4112–00			1	PWR SPLY:SWITCHING,AUTO IN 85–264VAC, 47–440HZ,OUT 5VDC 5A,+15V 2A, –15V 0.5A	TK1955	NFS40–7610
–16	134–0260–00			3	BTN,PLUG:0.375 HOLE,STL,NP,6 PRONG	91833	7602
–17	159–0296–00			1	FUSE,CARTRIDGE:3.15A,250V	61857	MT4–2A
–18	119–6237–00			1	FAN,TUBEAXIAL:5VDC,0.08A,0.40W,4.6CFM,5500RPM,28DBA,40MM X 40MM X 10MM W/3.25" LEADS & AMP 104	0ADN8	AFB0405MA
	210–0802–00			12	WASHER,FLAT:0.15 IDX0.312 ODX0.032,STL CD PL	86928	ORDER BY DESC
	211–0371–00			4	SCR,MACHINE:4–40 X 0.500,PNH,STL,CDPL,T–9 TORX DR	0KB01	ORDER BY DESC
36					**Standard accessories**		
–1	161–0066–00			1	CA ASSY,PWR;3,18 AWG,250V/10A,98 INCH,STR,IEC320,RCPT X NEMA 5–15P,US,SAFTEY CONTROLLED	0B445	ECM–161–0066–00
–2	071–0568–00			1	MANUAL,TECH:INSTRUCTION,GTS1250	TK2548	071–0568–00
37					**Optional accessories**		
–1	119–6112–00			1	MODULE,OPTO:GBIC INTERFACE,1063/1250MBD GIGABIT INTERFACE CONVERTER,850NM,1250.0 MBAUD,1000B	9F560	IBM42S12SNYAA20

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Replaceable parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
–2	119–6113–00			1	MODULE,OPTO:GBIC INTERFACE,1063/1250MBD GIGABIT INTERFACE CONVERTER,1310NM,1250.0 MBAUD,1000	9F560	IBM42S12LNYAA20
NOT SHOWN	015–0553–00			1	ADPTR,SMA,ELEC:SLIDE ON MALE TO FEMALE	98291	50–674–6324–990
38					**Optional Power Cords**		
–1	161–0066–09			1	CA ASSY,PWR:3,0.75MM SQ,250V/10A,99 INCH,STR,IEC320,RCPT,EUROPEAN	2W733	ORDER BY DESC
–2	161–0066–10			1	CA ASSY,PWR:3,1.0 MM SQ,250V/10A,2.5 METER,STR,IEC320,RCPT X 13A,FUSED UK PLUG(13A FUSE),UNI	TK2541	ORDER BY DESC
–3	161–0066–11			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,STR,IEC320,RCPT,AUSTRALIA	80126	ORDER BY DESC
–3	161–0304–00			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,STR,IEC320,RCPT,CHINA	0B445	E13.900.098.A01
–4	161–0066–12			1	CA ASSY,PWR:3,18 AWG,250V/10A,98 INCH,STR,IEC320,RCPT X NEMA 6–15P,US	S3109	ORDER BY DESCRIPTION
–5	161–0154–00			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,STR,IEC320,RCPT,SWISS	5F520	86515030

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Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
05JW7	PURDY ELECTRONICS CORP	INTEROPTIC DIVISION 720 PALOMAR AVE	SUNNYVALE, CA 94086
060D9	UNITREK CORPORATION	3000 COLUMBIA HOUSE BLVD, SUITE 1 20	VANCOUVER, WA 98661
0ADN8	DELTA PRODUCTS CORP–DPZ	4405 CUSHING PARKWAY	FREMONT, CA 94538
0B445	ELECTRI–CORD MFG CO INC	312 EAST MAIN STREET	WESTFIELD, PA 16950
0C5R7	ALCOA FUJIKURA LTD	150 RIDGEVIEW CIRCLE	DUNCAN, SC 29334
0CKD9	FIBER INSTRUMENT SALES INC	161 CLEAR ROAD	ORISKANY, NY 13424
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND, OR 97214–4657
16179	M/A COM INC	1011 PAWTUCKER BLVD. PO BOX 3295	LOWELL, MA 01853–3295
24931	FCI/BERG ELECTRONICS INC	RF/COAXIAL DIV 2100 EARLYWOOD DR PO BOX 547	FRANKLIN, IN 46131
26805	M/A COM OMNI SPECTRA INC	MICROWAVE CONNECTOR DIV 140 4TH AVE	WALTHAM, MA 02254
2W733	BELDEN WIRE & CABLE COMPANY	2200 US HWY 27 SOUTH PO BOX 1980	RICHMOND, IN 47374
5F520	PANEL COMPONENTS CORP	PO BOX 115	OSKALOOSA, IA 52577–0115
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
62712	SEIKO INSTRUMENTS USA INC	ELECTRONIC COMPONENTS DIV 2990 W LOMITA BLVD	TORRANCE, CA 90505
7X318	KASO PLASTICS INC	5720–C NE 121ST AVE, STE 110	VANCOUVER, WA 98682
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
80126	PACIFIC ELECTRICORD CO	747 WEST REDONDO BEACH PO BOX 10	GARDENA, CA 90247–4203
86928	SEASTROM MFG CO INC	456 SEASTROM STREET	TWIN FALLS, ID 83301
91833	KEYSTONE ELECTRONICS CORP	31–07 20TH ROAD	ASTORIA, NY 11105–2017
93907	CAMCAR DIV OF TEXTRON INC	ATTN: ALICIA SANFORD 516 18TH AVE	ROCKFORD, IL 611045181
98291	ITT CANNON RF PRODUCTS	585 EAST MAIN STREET	NEW BRITAIN, CT 06051
9F560	IBM CORPORATION	420 E SOUTH TEMPLE ST	SALT LAKE CITY, UT 84145
S3109	FELLER U.S. CORPORATION	72 VERONICA AVE UNIT #4	SOMERSET, NJ 08873
TK1943	NEILSEN MANUFACTURING INC	3501 PORTLAND RD NE	SALEM, OR 97303
TK1955	ARTESYN TECHNOLOGIES	47173 BENICIA ST	FREMONT, CA 94538
TK2208	NORTHWEST RUBBER EXTRUDERS INC	11155 SW DENNEY RD	BEAVERTON, OR 97008
TK2541	AMERICOR ELECTRONICS LTD	UNIT–H 2682 W COYLE AVE	ELK GROVE VILLAGE, IL 60007
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

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Appendix A: GTS1250 Long and Short Patterns

This appendix displays the SHORT and LONG patterns.

The IEEE 802.3 patterns

The IEEE 802.3 standard (1998 edition) describes the LONG and SHORT continuous random test patterns in section Annex 36A. The standard lists the patterns in HEX format prior to 8B-10B encoding and also prior to insertion of the packet encapsulation delimiter. The GTS1250 generates these LONG and SHORT patterns as they would appear on the physical layer after 8B-10B encoding and with proper packet encapsulation.

Table Formats

Tables 23 and 24 describe the sequential bit sequence of the LONG and SHORT patterns. The tables are arranged such that the time domain occurrence of the bits is from left to right, and top to bottom. The tables are divided into groups of three rows which contain the information shown in Figure 39.

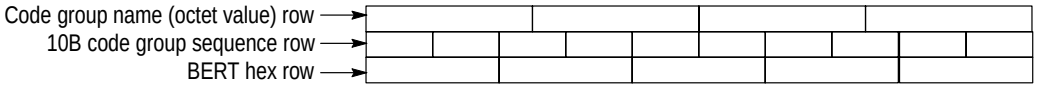


Figure 39: Long Pattern and Short Pattern table format

Code Group Name (Octet Value)

This row lists the code groups transmitted in time domain order (from left to right, top to bottom). The Octet value (8-bit HEX prior to 8B10B encoding) of the code group is listed in parenthesis.

10B Code Group Sequence

This row lists the individual bit sequence in the pattern in time domain order (from left to right, top to bottom). The 10-bit code groups are broken into 4-bit sequences for the convenience of programming Bit Error Rate Test (BERT) receivers; the 4-bit fields allow you to better fit the 10B data sequence into such byte-oriented equipment.

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BERT Hex The majority of BERT instruments use 8-bit bytes for programming long data patterns. Be aware that BERT equipment generally transmits (and expects at the paired BERT receiver) the least significant bit (LSB) first and the most significant bit (MSB) last. BERT equipment is programmed, though, in the Octet Hex manner in which the most significant hex value is listed first and the least significant hex value last (that is, a hex value of F0 would be transmitted in a bit sequence of 00001111). For the your convenience, the 4-bit sequences of the middle row are grouped into 8-bit bytes in the third bottom row and the BERT hex value to match the LSB-first, MSB-last sequence is listed.

Table 23: LONG Continuous Random Test Pattern Data Sequence

Preamble and Start of Frame (SFD)									
K27.7 (FB)		D21.2 (55)		D21.2 (55)		D21.2 (55)			
1101	1010	0010	1010	0101	1010	1001	0110	1010	0101
5B		54		5A		69		A5	
D21.2 (55)		D21.2 (55)		D21.2 (55)		D21.6 (D5)			
1010	1001	0110	1010	0101	1010	1001	0110	1010	0110
95		56		5A		E69		65	
Modified RPAT Sequence (Repeated 126 times)									
D30.5 (BE)		D23.6 (D7)		D3.1 (23)		D7.2 (47)			
0111	1010	1000	0101	0110	1100	0110	0111	1000	0101
5E		A1		36		E6		A1	
D11.3 (6B)		D15.4 (8F)		D19.5 (B3)		D20.0 (14)			
1101	0011	0001	0111	0010	1100	1010	1000	1011	1011
CB		E8		34		15		DD	
D30.2 (5E)		D27.7 (FB)		D21.1 (35)		D25.2 (59)			
1000	0101	0111	0110	0001	1010	1010	0110	0110	0101
A1		6E		58		65		A6	
Cyclic Redundancy Check (CRC)									
D20.4 (94)		D18.6 (D2)		D20.2 (54)		D12.5 (AC)			
0010	1111	0101	0011	0110	0010	1101	0100	1101	1010
F4		CA		46		2B		5B	
Inter–Packet Gap (IPG)									
K29.7 (FD)		K23.7 (F7)		K28.5 (BC)		D5.6 (C5)			
0100	0101	1100	0101	0111	1100	0001	0110	1001	0110
A2		A3		3E		68		69	

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Table 23: LONG Continuous Random Test Pattern Data Sequence (Cont.)

K28.5 (BC)		D16.2 (50)		K28.5 (BC)		D16.2 (50)			
0011	1110	1010	0100	0101	0011	1110	1010	0100	0101
7C		25		CA		57		A2	
K28.5 (BC)		D16.2 (50)		K28.5 (BC)		D16.2 (50)			
0011	1110	1010	0100	0101	0011	1110	1010	0100	0101
7C		25		CA		57		A2	

Table 24: SHORT Continuous Random Test Pattern Data Sequence

Preamble and Start of Frame (SFD)									
K27.7 (FB)		D21.2 (55)		D21.2 (55)		D21.2 (55)			
1101	1010	0010	1010	0101	1010	1001	0110	1010	0101
5B		54		5A		69		A5	
D21.2 (55)		D21.2 (55)		D21.2 (55)		D21.6 (D5)			
1010	1001	0110	1010	0101	1010	1001	0110	1010	0110
95		56		5A		69		65	
Modified RPAT Sequence (Repeated 29 times)									
D30.5 (BE)		D23.6 (D7)		D3.1 (23)		D7.2 (47)			
0111	1010	1000	0101	0110	1100	0110	0111	1000	0101
5E		A1		36		E6		A1	
D11.3 (6B)		D15.4 (8F)		D19.5 (B3)		D20.0 (14)			
1101	0011	0001	0111	0010	1100	1010	1000	1011	1011
CB		E8		34		15		DD	
D30.2 (5E)		D27.7 (FB)		D21.1 (35)		D25.2 (59)			
1000	0101	0111	0110	0001	1010	1010	0110	0110	0101
A1		6E		58		65		A6	
Cyclic Redundancy Check (CRC)									
D15.1 (2F)		D0.7 (E0)		D10.5 (AA)		D15.7 (EF)			
0101	1110	0101	1000	1110	0101	0110	1010	1000	1110
7A		1A		A7		56		71	
Inter–Packet Gap (IPG)									
K29.7 (FD)		K23.7 (F7)		K28.5 (BC)		D5.6 (C5)			
0100	0101	1100	0101	0111	1100	0001	0110	1001	0110
A2		A3		3E		68		69	

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Table 24: SHORT Continuous Random Test Pattern Data Sequence (Cont.)

K28.5 (BC)		D16.2 (50)			K28.5 (BC)			D16.2 (50)	
0011	1110	1010	0100	0101	0011	1110	1010	0100	0101
7C		25		CA		57		A2	
K28.5 (BC)		D16.2 (50)			K28.5 (BC)			D16.2 (50)	
0011	1110	1010	0100	0101	0011	1110	1010	0100	0101
7C		25		CA		57		A2	

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Appendix B: GTS1063 CRPAT and CJTPAT Patterns

This appendix displays the CRPAT and CJTPAT patterns.

Fibre Channel MJS Jitter Test Patterns

The Fibre Channel working group submitted a Working Draft for Methodologies for Jitter Specification (MJS) in 1998. This draft was a technical report to the Accredited Standards Committee of National Committee for Information Technology Standardization (NCITS) and has a revision number known as T11.2/Project 1230/Rev 7, December 16, 1998.

The MJS document defined several jitter test patterns. The **RPAT** (Random Pattern) was developed to provide a broad and flat spectral content of frequency; a modified version of this was also defined in which the format of the pattern was properly encapsulated within a “compliant” frame structure, and is named **CRPAT** (Compliant Random Pattern). The **CJTPAT** (Compliant Jitter Tolerance Pattern) was developed to provide a data stream which would induce large instantaneous phase jumps; a modified version of this was also defined in which the format of the pattern was properly encapsulated within a ”compliant” frame structure, and is named **CJTPAT** (Compliant Jitter Test Pattern).

Table Formats

Tables 25 and 26 describe the sequential bit sequence of the CRPAT and CJTPAT patterns. The tables are arranged such that the time domain occurrence of the bits is from left to right, and top to bottom. The tables are divided into groups of three rows which contain the information shown in Figure 40.

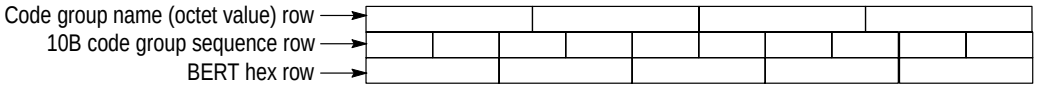


Figure 40: Long Pattern and Short Pattern table format

Code Group Name (Octet Value)

This row lists the code groups transmitted in time domain order (from left to right, top to bottom). The Octet value (8-bit HEX prior to 8B10B encoding) of the code group is listed in parenthesis.

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10B Code Group Sequence

This row lists the individual bit sequence in the pattern in time domain order (from left to right, top to bottom). The 10-bit code groups are broken into 4-bit sequences for the convenience of programming Bit Error Rate Test (BERT) receivers; the 4-bit fields allow you to better fit the 10B data sequence into such byte-oriented equipment.

BERT Hex

The majority of BERT instruments use 8-bit bytes for programming long data patterns. Be aware that BERT equipment generally transmits (and expects at the paired BERT receiver) the least significant bit (LSB) first and the most significant bit (MSB) last. BERT equipment is programmed, though, in the Octet Hex manner in which the most significant hex value is listed first and the least significant hex value last (that is, a hex value of F0 would be transmitted in a bit sequence of 00001111). For the your convenience, the 4-bit sequences of the middle row are grouped into 8-bit bytes in the third bottom row and the BERT hex value to match the LSB-first, MSB-last sequence is listed.

Table 25: CRPAT Compliant Random Pattern Data Sequence

Idle Primitive (Repeated 6 times)									
K28.5 (BC)		D21.4 (95)			D21.5 (B5)			D21.5 (B5)	
0011	1110	1010	1010	0010	1010	1010	1010	1010	1010
7C		55		54		55		55	
Start PF Frame (Class 3 normal: SOFn3)									
K28.5 (BC)		D21.5 (B5)			D22.1 (36)			D22.1 (36)	
0011	1110	1010	1010	1010	0110	1010	0101	1010	1001
7C		55		65		A5		95	
RPAT Sequence (Repeated 16 times)									
D30.5 (BE)		D23.6 (D7)			D3.1 (23)			D7.2 (47)	
1000	0110	1011	1010	0110	1100	0110	0100	0111	0101
61		5D		36		26		AE	
D11.3 (6B)		D15.4 (8F)			D19.5 (B3)			D20.0 (14)	
1101	0000	1110	1000	1101	1100	1010	1000	1011	0100
0B		17		3B		15		2D	
D30.2 (5E)		D27.7 (FB)			D21.1 (35)			D25.2 (59)	
0111	1001	0100	1001	1110	1010	1010	0110	0110	0101
9E		92		57		65		A6	
Cyclic Redundancy Check (CRC)									
D14.7 (EE)		D3.1 (23)			D21.2 (55)			D22.0 (16)	
0111	0010	0011	0001	1001	1010	1001	0101	1010	1011
4E		8C		59		A9		D5	

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Table 25: CRPAT Compliant Random Pattern Data Sequence (Cont.)

End of Frame (Pattern dependent EOFn)									
K28.5 (BC)		D21.5 (B5)		D21.6 (D5)			D21.6 (D5)		
1100	0001	0110	1010	1010	1010	1001	1010	1010	0110
83		56		55		59		65	

Table 26: CJTPAT Compliant Jitter Tolerance Pattern Data Sequence

Idle Primitive (Repeated 6 times)									
K28.5 (BC)		D21.4 (95)		D21.5 (B5)			D21.5 (B5)		
0011	1110	1010	1010	0010	1010	1010	1010	1010	1010
7C		55		54		55		55	
Start of Frame (Class 3 normal: SOFn3)									
K28.5 (BC)		D21.5 (B5)		D22.1 (36)			D22.1 (36)		
0011	1110	1010	1010	1010	0110	1010	0101	1010	1001
7C		55		65		A5		95	
Low Density Transition Pattern (Repeated 41 times)									
D30.3 (7E)		D30.3 (7E)		D30.3 (7E)			D30.3 (7E)		
1000	0111	0001	1110	0011	1000	0111	0001	1110	0011
E1		78		1C		8E		C7	
Transferring from Low to High Transition Densities									
D30.3 (7E)		D30.3 (7E)		D30.3 (7E)			D20.3 (74)		
1000	0111	0001	1110	0011	1000	0111	0000	1011	1100
E1		78		1C		0E		3D	
D30.3 (7E)		D11.5 (AB)		D21.5 (B5)			D21.5 (B5)		
0111	1000	1111	0100	1010	1010	1010	1010	1010	1010
1E		2F		55		55		55	
HIGH Density Transition Pattern (Repeated 12 times)									
D21.5 (B5)		D21.5 (B5)		D21.5 (B5)			D21.5 (B5)		
1010	1010	1010	1010	1010	1010	1010	1010	1010	1010
55		55		55		55		55	
Transferring from High to Low Transition Densities									
D21.5 (B5)		D30.2 (5E)		D10.2 (4A)			D30.3 (7E)		
1010	1010	1010	0001	0101	0101	0101	0101	1110	0011
55		85		AA		AA		C7	

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Table 26: CJTPAT Compliant Jitter Tolerance Pattern Data Sequence (Cont.)

D30.3 (7E)		D30.3 (7E)			D30.3 (7E)			D30.7 (FE)	
1000	0111	0001	1110	0011	1000	0111	0001	1110	0001
E1		78		1C		8E		87	
Cyclic Redundancy Check (CRC)									
D21.7 (F5)		D14.1 (2E)			D22.7 (F6)			D29.6 (DD)	
1010	1011	1001	1100	1001	0110	1000	0110	1110	0110
D5		39		69		61		67	
End Of Frame (Pattern dependent EOFn)									
K28.5 (BC)		D21.5 (B5)			D21.6 (D5)			D21.6 (D5)	
1100	0001	0110	1010	1010	1010	1001	1010	1010	0110
83		56		55		59		65	

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Appendix C: Recovering a Clock from an External Electrical Signal

Consider the information in this appendix when recovering a clock from an external signal.

± Rx DATA connectors used as electrical inputs

There are applications in which you may need to recover a serial clock from an electrical data stream. An example of such an application might be: GBIC modules are often powered on a separate circuit board with 50-ohm input and output connectors; this is a common application, especially among GBIC manufacturers that wish to calibrate and/or test a GBIC module under well controlled environmental conditions, such as temperature. In applications where the GBIC module cannot be installed into the GBIC Receptacle (such as for testing 1x9 GBIC modules), the +Rx Data and –Rx Data MIN–LOSS outputs can act in reverse as electrical inputs.

Overriding RX_LOS to Enable the Clock Recovery Circuit

If there is no GBIC present, the GBIC Test System detects the RX_LOS line being pulled HIGH and shuts down the recovered clock circuitry (to optimize noise and power when no signal is present). To use the clock recovery circuitry without a GBIC in the receptacle, hold the RX_LOS signal LOW by driving the RX_LOS signal (pin 11) of the REMOTE INTERFACE connector low (or simply short this pin to GND)

Proper AC Input Coupling: Single-ended or Complimentary

The internal Min-Loss 75-to50 ohm conversion network is a passive network of resistors with a differential comparator measuring the difference between the +Rx_Data path and the –Rx_Data path (see the diagram in Figure 5 on page 14). This network is DC coupled to the front panel +RX DATA and –RX DATA connectors; due to the DC coupling, any external single-ended input signal applied to just one of the +/–RX Data connectors must be AC coupled through an external DC-block, and the unused RX DATA connector must be DC terminated with a 50-ohm termination (use the termination attached to front panel). Two separate complimentary signals may also be input into both the RX Data connectors using similar AC coupling on both inputs (in which case the signal input to +Rx DATA must have its compliment signal input to the –Rx Data connector with matching phase).

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Proper Internal Termination: Using a Powered Down GBIC as a Termination

The –RX Data and +Rx Data connectors on the GBIC Test System are 50 ohms impedance as seen into the instrument when the +Rx Data and –Rx Data pins on the GBIC connector are terminated in 75 ohms (to AC GND). Without a GBIC installed into receptacle the termination mismatch from a 50 ohm signal being input into either the +Rx Data or –Rx Data can cause reflections, and these in turn can create errors. One method of terminating the GBIC receptacle +/–Rx Data pins is to install a standard GBIC into the receptacle and then use the rear panel D25 pin 24 (GBICPWR_ENA) to shut down the power to the GBIC, thereby avoiding the GBIC signals from interfering with the external electrical signal you are inputting to the +Rx Data or –Rx Data connectors. By holding the GBICPWR_ENA signal low (or shorting this pin to GND) the GBIC will be silent due to lack of power, yet the GBIC will sill provide proper 75 ohm termination for the –Rx_DATA and +RX_DATA signal lines.

Input Sensitivity

Using the +/–RX DATA connectors as inputs has been type tested by Tektronix to have a Bit Error Performance better than 10^{-10} for single-ended or complimentary inputs (see page 34).

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Glossary

Accuracy
The closeness of the indicated value to the true value.

Address
A number specifying the location of a terminal, a peripheral device, a node, or any other unit or component in a network. A set of numbers that uniquely identifies a location in computer memory, a packet of data traveling through a network.

Attenuation
A decrease in magnitude of current, voltage, or power of a signal.

Attenuator
A transducer that reduces the amplitude of a signal.

Bandwidth
The difference between the high and low frequencies of a transmission band. The range of frequencies handled by a device or system. Bandwidth is a measure of network capacity. Analogue bandwidth is measured in cycles per second. Digital bandwidth is measured in bits of information per second.

BER
An acronym for Bit Error Ratio (or Rate). The principal measure of quality of a digital transmission system. BER is defined as:

BER = Number of Errors/Total Number of Bits

BER is usually expressed as a negative exponent. For example, a BER of 10^{-7} means that on average 1 bit out of 10^{7} bits is in error.

BER Floor
A limiting of the bit-error-ratio in a digital system as a function of received power due to the presence of signal degradation mechanisms or noise.

Bit Error
An incorrect bit. Also known as a coding violation.

Bit Rate
The number of bits transmitted in a specified (usually 1 second) time.

Channel
A communications path or the signal sent over a channel.

Channel capacity
The maximum usable data rate for a given channel.

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Clock
A signal that provides a timing reference.

Clock recovery
Recovering the clock from the incoming data.

dB
Decibel: a method of expressing power or voltage ratios. The decibel scale is logarithmic. It is often used to express the efficiency of power distribution systems when the ratio consists of the energy put into the system divided by the energy delivered (or in some cases, lost) by the system. One milliwatt is usually the reference for 0 decibels. The formula for decibels is:

$$dB_{level} = 10\log\left(\frac{level}{reference}\right)$$

In the electrical domain:

$$dB_{power} = 10log\left(\frac{P_{out}}{P_{ref}}\right) = 10log\left(\frac{\frac{V^2_{out}}{R}}{\frac{V^2_{ref}}{R}}\right) = 20log\left(\frac{V_{out}}{V_{ref}}\right)$$

$$\frac{V^2_{ref}}{50ohm} = 1mW$$

In optical:

$$dBm_{power} = 10log\left(\frac{P_O}{P_{ref}}\right)$$

$$P_{ref} = 1mW = 0dBm$$

dBm
The symbol for power level in decibels relative to 1 mW.

Demodulation
A process whereby a modulated signal is returned to its original form.

Deterministic jitter
The difference between the maximum and minimum deviations from the expected timing positions of data after removing the random jitter.

Differential (relating to data (electrical)signal)
A signal transmission method that requires the voltage levels in a pair of cables/signals to convey information.

Digital Signal
A signal made up of a series of on and off pulses.

Digital Transmission System
A transmission system where information is transmitted in a series of on and off pulses.

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Dispersion (example in fiber)
In an optical system, the broadening and distortion of a pulse due to multipath waveform propagation.

ES
An acronym for Errored Second. A second with at least one error.

Echo
An interference signal reflected back to the source from the terminating end.

ECL
Emitter-coupled logic is a high speed logic that uses emitter-coupled transistors.

Error Detection
Checking for errors in data transmission. A calculation is made on the data being sent and the results are sent along with it. The receiving station then performs the same calculation and compares its results with those sent. Each data signal conforms to specific rules of construction so that departures from this construction in the received signals can be detected. Any data detected as being in error is either deleted from the data delivered to the destination, with or without an indication that such deletion has taken place, or delivered to the destination together with an indication that it is in error.

Error Rate
The ratio of the number of data units in error to the total number of data units.

Fiber optics
A method of transmitting information in which light is modulated and transmitted over high–purity, filaments of glass. The bandwidth of fiber optic cable is much greater than that of copper wire.

Fiber Optics Transmission System (FOTS)
A transmission system transmitting light through thin glass fibers.

GBIC
Gigabit interface converter modules are transceivers that complete a link. GBICs are available in short and long wavelength optical and in metallic twisted pair cable designs.

Link
A transmission path between two stations, channels, or parts of a system.

LOF
An acronym for Loss of Frame.

Long wavelength
The spectrum from 1200 to 1600 nanometers.

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LOS
An acronym for Loss of Signal.

Modulation
A process of varying the frequency, phase, or amplitude of a signal so it is suitable for transmission over the medium between the transmitter and the receiver.

Multi-Channel Cable
An optical cable having more than one fiber.

Multimode
A fiber that can carry light at two or more wavelengths at the same time

Multiplexer
Equipment that combines two or more signals into one.

Multiplexing
Combine several communications signals into one.

Noise
Any unwanted energy that interferes with a signal or measurement.

Packet
A group of bits transmitted as a unit that includes source and destination address, data, control, an identification number, and error control information.

Packet Switching
A technique in which data is sent in fixed-length packets. Each packet is sent separately and may be interspersed with packets from other locations.

PRBS
Pseudo-random binary-pulse sequence. A repeating bit pattern that appears to be random. The bit pattern is used for telecommunications system testing.

Protocol
Formal conventions that govern the format and control of signals in a communication process.

Pulse modulation
The modulation of a series of pulses to represent the information.

Random jitter
Jitter whose value at a future instant cannot be predicted.

Residual Error Rate
The error rate remaining after attempts at correction are made.

Rx
An abbreviation for receiver.

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Short wavelength
The spectrum from 800 to 1000 nanometers.

Single mode
A fiber, designed to carry light of a single wavelength, that confines the light to a single path.

Telecommunications
The transmission or reception of signals by wire, radio, optical, or other system.

Terminal
A point where information enters or leaves a communications network. An input or output device designed to send or receive data.

Tip
One of a pair of conductors associated with telecommunications.

Transmission system
Facilities to transfer information from one location to another using copper conductors, fiber, or microwave radio.

Twisted Pair
This term describes the traditional copper cable used for short distance communications.

Tx
An abbreviation for transmitter

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