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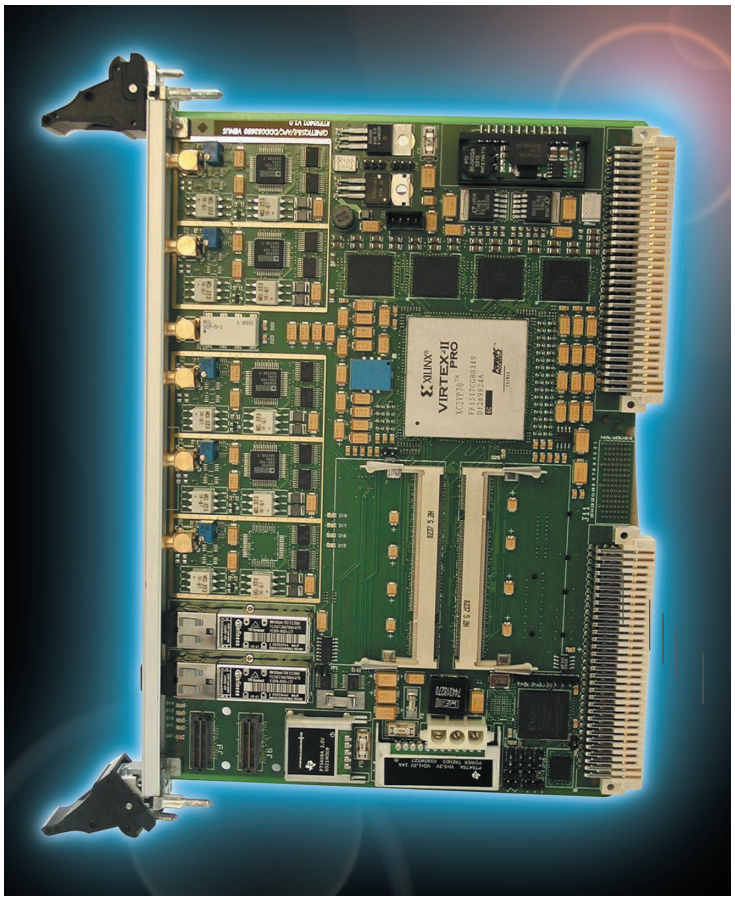
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Quixilica VENUS VXS-1



- 5x 14 bit 105 MSPS AD6645 Digitizers
- Xilinx XC2VP70 FPGA
- VME/VXS form factor, VITA 41.0 Compliant, 8 x 3.125 Gbps serial I/O links
- 2x Front Panel SFP slots for 2.5 Gbps fiber or copper transceivers
- 2x DDR SDRAM SODIMM Slots, up to 1 GB each
- 4x QDR SRAMs, 4 Mwords x 18 bits, 2 word burst
- Quixstart flexible FPGA configuration system
- Developer's Kit available containing FPGA interface cores, software and reference design

The Quixilica VENUS VXS-1 is part of the QinetiQ Quixilica VXS family of FPGA based processing hardware. The Quixilica VXS family provides a complete range of flexible analog and digital IO products in the VITA 41.0 VXS form factor. The product range couples high performance analog and digital IO front ends with a scalable FPGA based processing architecture. Memory and inter-processor communications resources have been optimized to address the requirements of very high performance real time digital signal processing applications. This family of products is supported by a range of development kits, FPGA cores and software, providing users with power and flexibility while retaining consistency and ease of use across the range.

Key applications for the VENUS VXS-1 include radar, electronic warfare, software radio and telecommunications.

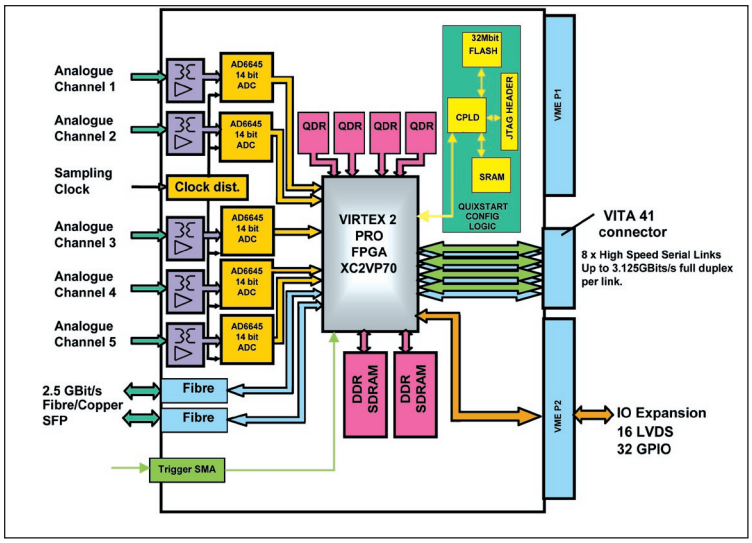
Hardware Description

The VENUS VXS-1 is a 6U form factor card that can be employed as a payload card as defined in the VITA 41.0 VXS specification. The card can also be deployed in a standard VME 64 chassis if the P0 connector is not populated. The VME 64 interface is used only for powering the card - the VME bus interface itself is not implemented. Control and high speed data IO for the card will be implemented using the high speed serial links available on the front panel and/or the backplane P0 connector. The card can also be used standalone (i.e. without a backplane) if desired.

The VENUS VXS-1 is supplied with a standard FPGA bitstream and Windows based software application for a multi-channel, snapshot data capture system.

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VENUS VXS-1 Block Diagram



A standard Gigabit Ethernet link to the front panel is used to interface the card to the host PC.

A hardware reference manual provides users with sufficient detail to develop their own FPGA based applications for the card entirely from scratch. However, for rapid development, an additional Developer's Kit can be purchased which contains FPGA interface cores, software and source code for the snapshot data capture system as a reference design.

FPGA

A Xilinx Virtex-II Pro XC2VP70 FPGA is at the heart of the VENUS VXS-1 product. The FPGA provides interfacing between the ADCs, memories and IO resources on the card as well as providing the user with a platform for implementing high performance real time processing.

The P70 FPGA provides two embedded PPC 405 processors and 16 Rocket IO high speed serial multi Gbps transceivers. The Rocket IO links are the principal mechanism used for high speed data IO and control on the VENUS VXS-1 card.

Analog to Digital Converters

5 channels of 105 MSPS, 14 bit resolution analog to digital conversion are provided on the VENUS VXS-1. The input channels are based around the Analog Devices AD6645 with options for either transformer AC coupled or buffered DC coupled analog inputs. A single external sampling clock is distributed to all 5 channels via a low skew, low jitter passive clock distribution network to ensure optimal performance in a range of multi-channel applications. A connection is also available for an external trigger input to the FPGA, allowing the user complete flexibility to implement a range of trigger options in firmware.

Memory

The VENUS VXS-1 provides 2 independent SODIMM sites for Double Data Rate (DDR) SDRAM modules, interfaced to the FPGA. DDR memory allows data to be read or written on both the rising and falling edges of the clock and the SODIMM modules support 64 bit wide data transfers. Standard SODIMM modules up to 1 Gbyte are currently available. Users can either purchase their own modules or specify the memory they require as additional cost items to be fitted to the VENUS VXS-1 card prior to delivery.

VENUS VXS-1 also provides 4 independent Quad Data Rate (QDR) SRAM memories. QDR memory provides independent read and write buses as well as allowing data transfers on both clock edges. Currently, 4 x 18 MB devices are fitted to the board. Two word burst memory arranged as 4 Megawords deep by 18 bits wide is used. Clock speeds of at least 100 MHz are possible on the standard version of VENUS VXS-1. Other footprint compatible QDR memories can be fitted as a special build option if required - contact the factory to discuss special requirements.

Front Panel High Speed Serial IO

Two SFP sites are provided on the front panel of the VENUS VXS-1. These can be populated with commercially available fibre optic or copper SFP modules. Short wave fiber optic modules that support data transfer rates up to 2.5Gbit/s are supplied as standard with the VENUS VXS-1. These modules provide physical layer support for standard protocols such as Gigabit Ethernet, Infiniband and Serial FPDP.

Alternative SFP modules for long wave fiber or copper (e.g. Gigabit Ethernet) can be supplied and fitted if required - please contact the factory to discuss special requirements.

N.B. Suitable FPGA cores are required to support the higher layers for specific protocols.

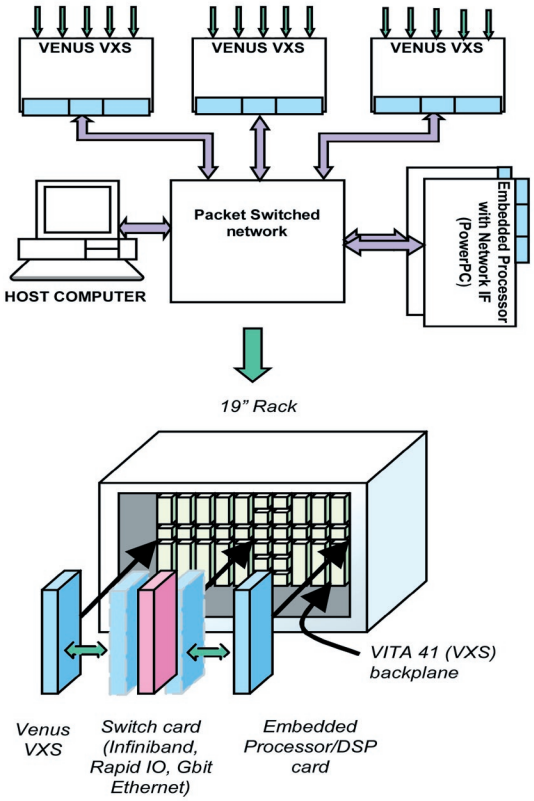
The QinetiQ Quixtream over UDP FPGA cores and software are supplied as part of the Developer's Kit (see below). This provides the user with a toolset to allow transfer of high speed data and control information from the FPGA into standard host computers running Windows or Linux via Gigabit Ethernet interfaces. Contact the factory to discuss support for other communications protocols if required.

VXS Backplane High Speed Serial IO

The VENUS VXS-1 can be used as a VITA 41.0 payload card. Up to 8 high speed serial links of up to 3.125 Gbps full duplex data rates are supported via the VITA 41.0 standard MultiGig RT2 P0 connector. Different custom or standard communication protocols can be run over these physical links by providing appropriate firmware in the FPGA.

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Population of the VITA 41.0 P0 connector is a build option that must be specified if the user wishes to deploy the high speed serial links on a backplane. Other hardware and firmware products in the Quixilica range and from third party vendors are also available to aid rapid implementation of complete VXS systems. Tekmicro will be pleased to advise on the use of VXS based bitstream products from a range of vendors to address specific application requirements.



P2 Connector GPIO

Up to 32 single ended, 2.5 Volt logic lines and 16 LVDS differential pairs from the FPGA are available on the P2 expansion connector. Sufficient information is supplied in the VENUS VXS-1 hardware manual for users to develop fully custom transition cards for their application if they need to. QinetiQ also has available a number of existing transition cards that are suitable for a wide range of simple GPIO applications. Customization for individual applications may also be possible. Contact the factory for details.

Quixstart FPGA Configuration

A number of options are available for configuring the FPGA on the VENUS VXS-1. For development purposes, a JTAG connection is available that allows users to configure the FPGA via standard Xilinx development tools such as Impact and Chipscope. When a stable design is available, an on-board flash memory can be programmed with the final bitstream and the FPGA will configure on power up. QinetiQ's Quixstart configuration mechanism also supports flexible configuration or reconfiguration of the FPGA through a Gigabit Ethernet link. In this mode the VENUS VXS-1 can be set up to fetch its configuration from a remote server after a power up or reset event. This is useful for applications where different bitstreams may be used to run the board in different modes. It is also suitable for applications where remote bitstream reconfiguration is required or where it is undesirable to have bitstreams held in on-board flash due to security considerations.

The setup files and software required for the full Quixstart system are supplied as part of the Developer's Kit for the VENUS VXS-1.

Software Support

Basic Software

The VENUS VXS-1 is supplied with a bitstream and executable Windows GUI application for a multi-channel snapshot data capture system. This provides users with a mechanism to experiment with and verify correct operation of the card. To use the application, users will require a host PC equipped with a Windows 2000/XP operating system and a fibre optic Gigabit Ethernet interface.

A UCF file for the FPGA and a detailed hardware reference manual is provided to allow users to implement their own FPGA designs from scratch if desired.

Recommended Development Tools

The following development tools are required/recommended for use with the VENUS VXS-1 if users are developing their own FPGA designs for the card:

- Xilinx ISE or Foundation (V6.x)
- Xilinx Chipscope software (Recommended for on-chip hardware debugging)
- Xilinx Parallel IV JTAG download cable
- Simulation / Synthesis tools as preferred by the user. (If not using Xilinx Foundation)
- Xilinx EDK (Required if developing for embedded PPC 405 cores in FPGA)
- Microsoft Visual C++ (If using Application Developer's Kit)

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VENUS VXS-1 Application Developer's Kit

To aid rapid development of user FPGA designs for the VENUS VXS-1, it is recommended that the additional Application Developer's Kit for the VENUS VXS-1 is purchased. This kit provides the following items:

- Quixilica Quixtream UDP/Gigbit Ethernet FPGA Cores host software (Windows and LINUX)
- DDR SDRAM FIFO Interface FPGA Cores
- QDR SRAM FIFO Interface FPGA Cores
- Setup files and instructions for Quixstart FPGA configuration system
- Reference design - Source code for snapshot data capture system firmware and software
- User manuals for all of the kit components and reference design

Signal Processing Cores

A complete range of high performance signal processing cores is available as part of the QinetiQ Quixilica range, including floating point arithmetic, programmable FIR filters, Digital Receivers, FFTs and QR Decomposition. Customization or development of IP for specific applications is also possible. Contact factory for availability of IP and targeted Application Developer's Kits for radar and EW applications using the VENUS VXS-1.

Quixtream Cores and Software for High Speed Interconnect

QinetiQ is continuing to develop support for other standard communications protocols as part of the Quixtream high speed communications product family. Contact us for availability of cores and software to support Infiniband, Serial FPDP, PCI Express, USB 2 and more.

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Ordering Information

VENUS VXS-1 6U VME Digitizer Card
Part Number: Qx-VENUS-VXS-A-P

A = Signal coupling into ADC analog inputs
: A => AC coupled
: D => DC coupled

P = P0 MultiGig RT2 Connector Build Option
: Y => Fit P0 Connector (For use in VXS Chassis)
: N => Don't Fit P0 Connector (For use in VME 64 Chassis)

Xilinx XC2VP70-6C Devices fitted as standard

Supplied populated with 2 x 2.5 Gbps short wave fiber optic SFP transceivers as standard

Contact factory for following optional items:

- Alternative FPGA speed grades and/or industrial silicon variants
- Supply of DDR SODIMM modules pre-fitted
- Availability of alternative QDR memory chips
- Supply of copper or long wave fiber SFP transceivers

VENUS VXS-1 Application Developers Kit

Part Number: Qx-VEN-DK01-DL

Contact factory for availability of additional DSP cores and Quixtream interconnect cores.

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