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Logic Analyzers

TLA Family



The TLA family of logic analyzers consists of the TLA600 Series and the TLA700 Series. The TLA600 offers a selection of standalone logic analyzer instruments at prices that make 500 ps timing resolution available to designers of today's mainstream embedded systems. The TLA700 Series offers the highest performance for today's demanding applications and consists of portable and benchtop modular mainframes with expansion mainframe capability. Instrument modules include logic analyzer, pattern generator and digitizing oscilloscope. A full line of complementary support products for popular processors and buses is available for the entire TLA family.

Breakthrough Solutions for Real-time Digital Systems Analysis

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA answers the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture and analyze real-time system operation in order to debug, verify, optimize and validate digital systems.

Hardware developers, Hardware/Software integrators and embedded software developers will appreciate the range of capabilities of the TLA. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state and high-speed timing analysis; using deep state acquisition to find the cause of complex problems; generating the digital stimulus for functional verification, debugging and stress testing; and offering non-intrusive real-time software execution tracing that correlates to the source code and to the hardware events.

This kind of performance is matched by value. Productivity and connectivity features such as the open Microsoft Windows platform make all TLA logic analyzers easy to use and easily networked into the design environment. Modularity and flexibility features help you protect your current investment.

Features & Benefits

MagniVu™ Technology Provides 500 ps Timing Resolution on All Channels All the Time Through the Same Probe

Up to 200 MHz State Acquisition with 400 MHz Data Rate for Advanced Processors and Buses

Simultaneous State and High Speed Timing Analysis Through the Same Probes Pinpoints Elusive Faults

500 MHz Deep Timing Analysis with Up to 128 Mb Per Channel

Broad Processor and Bus Support

Universal Source Code Support for Correlating High-level Language Source with Real-time Trace

Performance Analysis Support for Optimizing Target System

Remote Control Using Microsoft COM/DCOM Technology Supports Advanced Data Analysis

Microsoft Windows 2000 Professional PC Platform Provides Familiar User Interface With Network Connectivity

All Probes, Software and Accessories Fully Interchangeable Between all TLAs

Applications

Hardware Debug and Verification

Processor/Bus Debug and Verification

Embedded Software Integration, Debug and Verification

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▶ Characteristics

TLA Logic Analyzers

General

Number of Channels (all channels are acquired including clocks) –
TLA601/611/621, TLA7N1: 34 channels (2 are clock channels).
TLA602/612/622, TLA7N2, TLA7P2: 68 channels (4 are clock channels).
TLA603/613/623, TLA7N3: 102 channels (4 are clock and 2 are qualifier channels).
TLA604/614/624, TLA 7N4, TLA 7P4: 136 channels (4 are clock and 4 are qualifier channels).
Channel Grouping – No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).

TLA700 Module "Merging" – Three 102 channel or 136 channel modules can be "merged" to make up to a 408 channel module. Merged modules exhibit the same depth as the lesser of the three individual modules. Word/range/setup-and-hold/glitch/transition recognizers span all three modules. Only one set of clock connections is required.

Time Stamp – 50-Bits at 500 ps resolution (6.5 day range).

Clocking/Acquisition Modes – State, timing, 2x timing, simultaneous.

Number of Mainframe Slots Required per TLA700 Module – 2.

Input Characteristics (with P6417, P6418 or P6434 Probes)

Capacitive Loading – 1.4 pF typical data; 2 pF typical clock (P6418).
2 pF typical data and clock (P6417 & P6434).

Threshold Selection Range – From +5.0 V to –2.0 V in 50 mV increments.

Threshold Selection Channel Granularity – Separate selection for clock (1) and data (16) for each 17 channel probe connector.

Threshold Accuracy (including probe) – ±100 mV.

Input Voltage Range – Operating: 6.5 V_{p-p} centered around the programmed threshold.
Non-destructive: ±15 V.

Input Signal Swing (probe overdrive) – ±250 mV or ±25% of signal swing, whichever is greater (P6417 & P6418).
±300 mV or ±25% of signal swing (P6434).

Input Signal Minimum Slew Rate – 200 mV/ns typical.

State Acquisition Characteristics (with P6417, P6418 or P6434 Probes)

State Clock Rate – 100 MHz standard, 200 MHz optional.

State Data Rate (half/full channels) –
400 MHz/200 MHz, typical. Requires 200 MHz state option.

State Memory Depth with Timestamps – 64 Kb, 256 Kb, 1 Mb, 4 Mb, 16 Mb or 64 Mb Bits per channel (4 Mb, 16 Mb and 64 Mb available only on TLA700).

Setup Time Selection Range – From 8.5 ns before, to 7.0 ns after clock edge.

Setup-and-hold Window – 2.0 ns typical.

Minimum Clock Pulse Width – 2 ns.

Active Clock Edge Separation – 5 ns.

Demux Channel Selection – Channels can be demultiplexed to other channels through user interface with 8 channel granularity.

Timing Acquisition Characteristics (with P6417, P6418 or P6434 Probes)

MagniVu™ Timing – 500 ps.

MagniVu Timing Memory Depth – 2 Kb (2048) per channel.

Deep Timing Resolution (half/full channels) – 2 ns, 4 ns to 50 ms.

Deep Timing Resolution with Glitch Storage Enabled – 10 ns to 50 ms.

Deep Timing Memory Depth (half/full channels with timestamps and with or without transitional storage) – 128/64 Kb, 512/256 Kb, 2/1 Mb, 8/4 Mb, 32/16 Mb, 128/64 Mb per channel (8/4 Mb, 32/16 Mb and 128/64 Mb available only on TLA700).

Deep Timing Memory Depth with Glitch Storage Enabled – Half of default main memory depth.

Channel-to-channel Skew – ≤1 ns typical.

Minimum Recognizable Pulse Width (single channel) – 2 ns.

Minimum Recognizable Glitch Width (single channel) – 2 ns.

Minimum Recognizable Multi-channel Trigger Event – Sample period + 2 ns.

Trigger Characteristics

Independent Trigger States – 16.

Maximum Independent If/then Clauses per State – 16.

Maximum Number of Events per If/then Clause – 8.

Maximum Number of Actions per If/then Clause – 8.

Maximum Number of Trigger Events – 18
(2 counter/timers plus any 16 other resources).

Number of Word Recognizers – 16.

Number of Range Recognizers – 4.

Number of Counter/Timers – 2.

Trigger Event Types – Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation.

Trigger Action Types – Trigger module, trigger all, store, don't store, start store, stop store, increment counter, reset counter, start timer, stop timer, reset timer, goto state, set/clear signal, do nothing.

Trigger Sequence Rate – DC to 250 MHz (4 ns).

Counter/Timer Range – 51-Bits each (>100 days @ 4 ns).

Counter Rate – DC to 250 MHz (4 ns).

Timer Clock Rate – 250 MHz (4 ns).

Counter/Timer Latency – None (can be tested or reset immediately after starting).

Range Recognizers – Double bounded (can be as wide as any group, must be grouped according to specified order of significance).

Setup-and-hold Violation Recognizer Setup Time Range – From 8 ns before to 7 ns after clock edge in 0.5 ns increments.

Setup-and-hold Violation Recognizer Hold Time Range – From 7 ns before to 8 ns after clock edge in 0.5 ns increments.

Trigger Position – Any data sample.

MagniVu Trigger Position – MagniVu data is centered around the module trigger.

Storage Control (data qualification) – Global (conditional), by state (start/stop), by trigger action, or transitional.

Storage Window Granularity – Single sample or block-of-31 samples before and after.

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P6417 Probe Cable Length – 1.8 m (6 ft.).

P6418 Probe Cable Length – 1.9 m (6.25 ft.).

P6434 Probe Cable Length – 1.5 m (5 ft.).
All three probes have the same electrical length.

TLA700 Pattern Generator Modules

General

Data Width –
64 Channel full channel mode.
32 Channel half channel mode.

Module "Merging" – Five modules can be "merged" to make up to a 320 channel module. Merged modules exhibit the same depth as the lesser of the 5 individual modules.

Number of mainframe slots required – 2.

Data Rate –
Internal Clock:
0.5 Hz to 134 MHz full channel mode.
1.0 Hz to 268 MHz half channel mode.
External Clock:
DC to 134 MHz full channel mode.
DC to 268 MHz half channel mode.

External Clock Input –
Polarity: positive or negative.
Threshold: –2.56 V to +2.54 V, nominal; programmable in 20 mV increments.
Sensitivity: ≤500 mV_{p-p}.
Impedance: 1 kΩ terminated to ground.

Data Depth –
256 K full channel/512 K half channel.
1 M full channel/2 M half channel (optional).

Pattern Sequencing Characteristics

Blocks – Separate sections of pattern program that are output in a user definable order by the Sequencer. Block pattern depth can be from 40 sequences (full channel mode) or 80 sequences (half channel mode) up to the entire depth of the TLA7PG2. A maximum of 4,000 Blocks may be defined.

Sequencer – A 4000 line memory that allows the user to pick the output order of individual Blocks. Each line in the sequencer allows the definition of a Block to be output, a Repeat Count for that Block, A Wait For event condition for the Block, the Signal state for that Block (asserted or unasserted), and a Jump If event condition, with a sequence line to jump to if the condition is satisfied.

Sub-sequences – Up to 50 contiguous lines of the Sequencer memory may be defined as a Sub-sequence. A Sub-sequence can then be treated like a block. (Example: 15 Sequences of Blocks are defined as Sub-sequence A1. Now any line in the Sequencer can output A1. Five calls to Sub-sequence A1 will be flattened out to 75 sequences at run time.)

Jump If – Jumps to the specified sequence if a user defined event is true. The user defined event is a boolean combination of the eight external event input lines and the one-of-four intermodule signals. The user defined Event is selectable between level and edge (event going from false to true). One Jump If may be defined for every Block. The Jump If command works at all clock rates, including the maximum half channel mode rate of 268 MHz.

Wait For – Pattern output is paused until the user defined Event is true. One Wait For may be defined for every Block.

Assert Signal – One of the four inter-module signals is selected to be controlled from the pattern generator program. Signals may be asserted and unasserted allowing true interaction with the logic analyzer modules and with other pattern generator modules. Signal action (assert or unassert) may be defined for every Block.

Repeat Count – The sequence is repeated from 1 to 65,536 times. Infinite may also be selected. One Repeat Count may be defined for every Block. Note that a Repeat value of 10,000 takes one sequence line in memory, not 10,000.

Step – While in Step mode, the TLA7PG2, the user can manually satisfy (i.e., click an icon) Wait For and Jump conditional events. This allows the user to debug the logic flow of the program's sequencing.

Initialization Block – The unconditional Jump command allows the user to implement an equivalent function.

Common to P6470 TTL/CMOS & P6471 ECL Probes

Number of Data Outputs – 16 in Full Channel Mode. 8 in Half Channel Mode.

Number of Clock Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)

Number of Strobe Outputs – 1. (Only one of Clock Output and Strobe Output can be enabled.)

Number of External Event Input – 2.

Clock Output Polarity – Positive.

Strobe Type – RZ only.

Strobe Delay – Zero or Trailing Edge.

P6470 TTL/CMOS Probe

Output Type –
HD74LVC541A for Data Output.
HD74LVC244A for Clock/Strobe Output.

Rise/Fall Time (20% to 80%) –

	Timing values measured using 75 Ω termination (internal to probe), 1 MΩ + <1 pF load and V_{OH} set to 5.0 V.	**Timing values measured using 75 Ω termination (internal to probe), 510 Ω + 51 pF load and V_{OH} set to 5.0 V.**
Clock/Strobe Output:		
Rise:	640 ps typical.	6.5 ns typical.
Fall:	1.1 ns typical.	6.3 ns typical.
Data Output:		
Rise:	680 ps typical.	5.2 ns typical.
Fall:	2.9 ns typical.	4.5 ns typical.

Output Voltage (nominal, load: 1 MΩ) –
V_{OH}: 2.0 V to 5.5 V, tri-stateable, programmable in 25 mV increments.
V_{OL}: 0 V.

Data Output Skew –
<510 ps typical between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<480 ps typical between all data output pins of single probe.

Data Output to Strobe Output Delay – 1.7 ns typical when strobe delay set to zero.

Data Output to Clock Output Delay – 2.4 ns typical.

External Clock Input to Clock Output Delay –
Full Channel mode: 61.5 ns typical.
Half Channel mode: 61.5 ns typical.

Number of External Inhibit Input – 1.

External Inhibit Input to Output Enable Delay – 34 ns typical for Data Output.

External Inhibit Input to Output Disable Delay – 86 ns typical for Data Output.

Probe D Data Output to Output Enable Delay –
(for Internal Inhibit) 7 ns typical for Data Output.

Probe D Data Output to Output Disable Delay –
(for Internal Inhibit) 8 ns typical for Data Output.

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External Event Input to Clock Output Setup (for inhibit) (event-filter: off) –
Full Channel mode: 1.5 clocks + 150 ns typical.
Half Channel mode: 2 clocks + 150 ns typical.

External Event Input and Inhibit Input –
Input Type: 74LVC14A.
Minimum Pulse Width: 100 ns.

P6471 ECL Probe

Output Type –
100E151 for data output.
100EL16 for strobe output.
100EL04 for clock output.
All outputs are unterminated.

Rise/Fall Time (20% to 80%) –

	Timing values measured using 51 Ωs to –2.0 V.
Clock Output:	
Rise:	320 ps typical.
Fall:	330 ps typical.
Data Output:	
Rise:	1200 ps typical.
Fall:	710 ps typical.
Strobe Output:	
Rise:	290 ps typical.
Fall:	270 ps typical.

Data Output Skew –
<170 ps typical between all data output pins of all modules in the mainframe after inter-module skew is adjusted manually.
<140 ps typical between all data output pins of single probe.

Data Output to Strobe Output Delay – 2.94 ns typical when strobe delay set to zero.

Data Output to Clock Output Delay – 780 ps typical.

External Clock Input to Clock Output Delay – 51 ns typical.

External Event Input –
Input Level: ECL.
Input Type: 10H116.
Minimum Pulse Width: 50 ns.

P6470 Probe Cable Length – 1.6 m (5 ft.)

P6471 Probe Cable Length – 1.6 m (5 ft.)

TLA700 Digitizing Oscilloscope Modules

General

Number of Channels per Module –
TLA7D2, TLA7E2: 4 channels.
TLA7D1, TLA7E1: 2 channels.

Sample Rate –
TLA7E1, TLA7E2: 5 GS/s on all channels.
TLA7D1, TLA7D2: 2.5 GS/s on all channels.

Bandwidth (at probe tips) –
TLA7E1, TLA7E2:
100 mV to 10 V range: 1 GHz.
50 mV to 99.8 mV range: 900 MHz.
20 mV to 49.8 mV range: 600 MHz.
All others:
500 MHz.
TLA7D1, TLA7D2: 500 MHz on all channels in all ranges.

Memory Depth – 15,000 samples per channel in all modes.

Number of Mainframe Slots Required – 2.

Vertical System

Input Sensitivity Range – 10 mV to 100 V full scale.

Vertical Resolution – 8-Bits (256 levels).

DC Gain Accuracy – ±1.5% of full scale range.

Analog Bandwidth Selections – 20 MHz, 250 MHz, and Full.

Input Coupling – AC, DC, or GND.

Input Impedance Selections – 1 MΩ in parallel with 10 pF, or 50 Ω.

AC Coupled Lower Frequency Limit – ≤10 Hz when AC 1 MΩ coupled, ≤200 kHz when AC 50 Ω coupled.

Maximum Input Voltage at Probe Connector – 300 V_{RMS}, but no greater than ±420 V peak (1 MΩ or ground input coupling).

Probe Input Characteristics

Probe Input Interface – TEKPROBE™ probe interface.

Input Loading – Less than 1 pF in parallel with 1 MΩ with either P6243 or P6245.

Usable Input Voltage Range at Probe Tip – P6243 Probe: ±8 V. P6245 Probe: ±18 V.

Acquisition System

Sample Rate Range – 200 ps to 200 ms in 1, 2.5, 5 sequence.

Timebase Accuracy – ±100 ppm over any interval ≥1 ms.

Record Length Range – 512 to 15,000 samples per channel in all modes.

Acquisition Modes – Single-shot, repetitive.

Trigger System

Trigger Modes – Normal, auto.

Trigger Position – Anywhere in the acquired record (pre-fill can be set anywhere from 0% to 100%).

Trigger Types – Edge, pulse width, timeout, glitch, runt, slew rate, logic pattern, setup-and-hold violation.

Trigger Actions – Trigger, trigger all, set signal, arm, immediate, wait for system trigger.

Edge Trigger – Conventional level driven trigger, positive or negative slope, on any channel or external trigger input. Coupling Selections: DC, AC, noise reject, HF reject, LF reject.

Pulse Width Trigger – Trigger on width of positive or negative pulse, either within or not within selectable time limits; settable from 2 ns to 1 s.

Timeout Trigger – Triggers when a pulse fails to complete when specified; settable from 2 ns to 1 s.

Glitch Trigger – Trigger on (or reject) glitches of positive, negative, or either polarity; settable from 2 ns to 1 s. Minimum glitch width: 2.0 ns, with 200 ps resolution (2 ns to 10 ns settings).

Runt Pulse Trigger – Trigger on a pulse that crosses one threshold but fails to cross a second threshold before crossing the first again; settable from 2 ns to 1 s.

Slew Rate Trigger – Trigger on pulse edge rates that are either faster or slower than a set rate, edges can be rising, falling, or either; settable from 2 ns to 1 s.

Logic Pattern Trigger – Triggers when a logical combination (AND, OR) of all the input channels (Hi, Lo, Don't Care) stays true or false for a specified period of time; settable from 2 ns to 1 s.

Setup-and-hold Trigger – Trigger on violations of both setup time and hold time between clock and data which are on separate input channels; setup time settable from –100 ns to +100 ns in 200 ps increments; hold time settable from –1 ns to +102 ns; minimum settable window of setup time + hold time is 2 ns.

P6243 Probe Cable Length – 1.3 m (51 in.).

P6245 Probe Cable Length – 1.3 m (51 in.).

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TLA700 Mainframes

General (TLA714, TLA720, TLA7XM)

Instrument Slots –
TLA714: Holds 4 single-wide or 2 double-wide modules.
TLA720: Holds 10 single-wide or 5 double-wide modules.
TLA7XM: Holds 12 single-wide or 6 double-wide modules.

Ten TLA7XMs

	TLA714 – 24 Dual/48 Single*2,3 TLA720 – 60 Dual/120 Single*2,3		
Mainframe	**LA*1**	**PG*1**	**DSO*1**
Max channels per module	136 ch	64 ch	4 ch
TLA714	3,264	1,536	96
TLA720	8,160	3,840	240

*1 All logic analyzer (LA), pattern generator (PG) and digitizing oscilloscope (DSO) modules are dual-wide or occupy two single-wide slots.

*2 TLA7XM Expansion Module occupies one single-wide slot in both the TLA714/TLA720 mainframe and the TLA7XM expansion mainframe.

*3 Using a TLA7XM expansion mainframe with an existing TLA714/TLA720 mainframe requires Version 4.0 or higher TLA application software. TLA720 benchtop mainframes, S/N: B019999 and lower, require TLA7UP Option 09 TLA720 Benchtop Mainframe Upgrade. Please refer to the TLA Upgrade Guide for further details.

For configurations beyond ten TLA7XM expansion mainframes, please contact your local Tektronix account manager.

TLA700 PC Characteristics (TLA714 and TLA720)

Operating System – Microsoft Windows 2000 Professional.

Processor – Pentium.

DRAM –
TLA714: 64 MB SDRAM (128 MB with Opt. 1S).
TLA720: 128 MB SDRAM.

Display Memory – 2 MB.

Sound – Built-in PC speaker transducer; multimedia sound can be added via PC Card interface.

Replaceable Hard Disk Drive –
TLA714: 10 GB (30 GB with Opt. 1s).
TLA720: 30 GB.
A second internal fixed hard disk is available for both mainframes with TLA7UP Opt. 10.

CD ROM – 24x, Internal.

Floppy Disk Drive – Built-in 3.5 in. 1.44 MB drive.

Year 2000 Compliant – Yes.

TLA700 Integral Controls (TLA714 only)

Front-Panel Display –
Size: 10.4 in. diagonal.
Type: Active-matrix color TFT LCD with backlight.
Resolution: 800 x 600.
Colors: 16.8 M (true color).

Simultaneous Display Capability – Both the front-panel and external displays can be used simultaneously at 800 x 600 resolution.

Front-panel Knobs – Special function knobs for instrument control.

Front-panel Qwerty Keypad – Mini-QWERTY keypad and Hex keypad.

Front-panel Pointing Device – Glidepoint finger pad.

TLA700 External Peripheral Interfaces (TLA714 and TLA720)

External Display Port Type – Female DB15 SVGA connector.

External Display Resolution – Up to 1600 x 1200 non-interlaced @ 256 colors.

External Display Compatibility – DDC2B (Dynamic Display Configuration 2).

External Keyboard Port Type – PS2 mini-DIN.

External Mouse Port Type – PS2 mini-DIN.

Parallel Interface Port Type – IEEE 1284-C connector (comes standard with adapter to female DB25 connector).

Parallel Interface Modes – Centronics mode, EPP (Extended Parallel Port), ECP (Microsoft high-speed mode).

Serial Interface Port Type – Male DB9.

PC Card (CardBus) Slot Types – Two slots, two PC Card Type I/II or one PC Card Type III.

USB Port – Two (2).

TLA600 PC Characteristics

Operating System – Microsoft Windows 2000 Professional.

Processor – Celeron®.

DRAM – 64 MB SDRAM (128 MB with Opt. 1J).

Sound – Built-in PC speaker transducer; 16-Bit I/O and Mic In port.

Hard Disk Drive – 10 GB (30 GB with Opt. 1J).

CD ROM – 40x, Internal.

Floppy Disk Drive – Built-in 3.5 in. 1.44 MB drive.

Year 2000 Compliant – Yes.

TLA600 Integral Controls (TLA61X/62X only)

Front-Panel Display –
Size: 10.4 in. diagonal.
Type: Active-matrix color TFT LCD with backlight.
Resolution: 800 x 600.
Colors: 16.8 M (true color).

Simultaneous Display Capability – Both the front-panel and external displays can be used simultaneously, each with independent resolutions.

Front-panel Knobs – Special function knobs for instrument control.

Front-panel Qwerty Keypad – Mini-QWERTY keypad.

TLA600 External Peripheral Interfaces

External Display Port Type – Female DB15 SVGA connector.

External Display Resolution – Up to 1280 x 1024 non-interlaced @ 16 M colors.

LAN Port Type – 10/100-BaseT, RJ-45.

External Keyboard Port Type – PS2 mini-DIN.

External Mouse Port Type – PS2 mini-DIN.

Parallel Interface Port Type – Female DB25.

Parallel Interface Modes – Centronics mode, EPP (Extended Parallel Port), ECP (Microsoft high-speed mode).

Serial Interface Port Type – Male DB9.

Audio Out Port Type – Stereo minijack.

Mic In Port Type – Minijack.

PC Card (CardBus) Slot Types – Two slots, two PC Card Type I/II or one PC Card Type III.

USB Port – One (1).

Symbolic Support (All TLA Logic Analyzers)

Number of Symbols/Ranges – Unlimited (limited only by amount of virtual memory available on TLA).

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Object File Formats Supported –

- IEEE695
- OMF 51, OMF 86, OMF 166, OMF 286, OMF 386
- COFF
- Elf/Dwarf 1 and 2
- Elf/Stabs
- TSF (if your software development tools do not generate output in one of the above formats, TSF or the Tektronix symbol file, a generic ASCII file format is supported. The generic ASCII file format is documented in the TLA User Manual). If a format is not listed, please contact your local Tektronix representative.

External Instrumentation Interfaces (all TLA logic analyzers)

System Trigger Output – Asserted whenever a system trigger occurs (TTL-compatible output, back-terminated into 50 Ω).

System Trigger Input – Forces a system trigger (triggers all modules) when asserted (TTL-compatible, edge-sensitive, falling-edge latched).

External Signal Output – Can be used to drive external circuitry from a module's trigger mechanism (TTL-compatible output, back-terminated into 50 Ω).

External Signal Input – Can be used to provide an external signal to arm or trigger any or all modules (TTL-compatible, level-sensitive).

P6041 External Signal Cable Length – (SMB to BNC adapter cable, two each TLA720 only) 1.1 m (42 in.).

Power

TLA60X/61X/62X –
Voltage range/frequency: 90-250 VAC @ 45-66 Hz.
100-132 VAC @ 360-440 Hz.
Input current: 6 A maximum at 90 VAC (70 A surge).
Power consumption: 400 W maximum.

TLA714 –
Voltage range/frequency: 90-250 VAC @ 45-66 Hz.
100-132 VAC @ 360-440 Hz.
Input current: 6 A maximum at 90 VAC (70 A surge).
Power consumption: 600 W maximum.

TLA720 and TLA7XM –
Voltage range/frequency: 90-250 VAC @ 45-66 Hz, 100-132 VAC @ 360-440 Hz.
Input current: 16.5 A maximum at 90 VAC (70 A surge).
Power consumption: 1450 W maximum.

Physical Characteristics

TLA714 Portable

Dimensions	**mm**	**in.**
Height	235	9.25
Width	432	17
Depth	455	17.5
Weight	**kg**	**lb.**
Net (w/o modules)	11.4	25
Shipping (typical)	25.5	56

TLA720 Benchtop & TLA7XM Expansion

Dimensions	**mm**	**in.**
Height	346	13.65
Width	425	16.7
Depth	673	26.5
Weight	**kg**	**lb.**
Net (w/o modules)	22.7	50
Shipping (typical)	51.8	114

TLA60X

Dimensions	**mm**	**in.**
Height	281.94	11.10
Width	457.20	18.00
Depth	414.02	16.30
Weight	**kg**	**lb.**
Net (w/o probes)	16.8	37
Shipping (typical)	38.6	85

TLA61X/62X

Dimensions	**mm**	**in.**
Height	281.94	11.10
Width	457.20	18.00
Depth	414.02	16.30
Weight	**kg**	**lb.**
Net (w/o probes)	17.3	38
Shipping (typical)	39.1	86

Environmental

Temperature –
Operating: +5°C to +50°C.
Nonoperating: –20°C to +60°C.

Humidity –
20% to 80%.
Operating: ≤30°C; 80% relative humidity (29°C maximum wet bulb temperature).
Nonoperating: 8% to 80% (29°C maximum wet bulb temperature).

Altitude –
Operating: –1,000 ft to 10,000 ft. (–305 meters to 3,050 meters).

Safety – UL3111-1, CSA1010.1, EN61010-1, IEC61010-1.

Ordering Information

TLA60X

Logic Analyzer with External Display.

Includes: Mouse, Keyboard, Front-panel Cover, Accessory Pouch, Probe retainer bracket, Probe manual, Power Cord (North American 120 VAC, 60 Hz), Software, User Manual, Certificate of Calibration, and One-year Warranty (return to Tektronix), and your choice of probes. Display is not included – order Opt. 1M or Opt. 2M or use any SVGA monitor.

TLA601 – 34 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state. Requires external display.

TLA602 – 68 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state. Requires external display.

TLA603 – 102 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state. Requires external display.

TLA604 – 136 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state. Requires external display.

TLA61X

Logic Analyzer with Internal Display.

Includes: Mouse, Keyboard, Front-panel cover, Accessory Pouch, Probe Retainer Bracket, Probe Manual, Power Cord (North American 120 VAC, 60 Hz), Software, User Manual, Certificate of Calibration, and One-year Warranty (return to Tektronix), and your choice of probes.

TLA611 – 34 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state.

TLA612 – 68 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state.

TLA613 – 102 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state.

TLA614 – 136 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 256 K depth and/or 200 MHz state.

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▶ Quantity of Probes per Option

Option		TLA7N1	TLA7N2	TLA7N3	TLA7N4	TLA7P2	TLA7P4	TLA7Q2	TLA7Q4
1P	Add P6418 Probes	2	4	6	8	4	8	4	8
2P	Add P6434 Probes	1	2	3	4	2	4	2	4
3P	Add P6417 Probes	2	4	6	8	4	8	4	8

Option		TLA601/611/621	TLA602/612/622	TLA603/613/623	TLA604/614/624
1P	Add P6418 Probes	2	4	6	8
2P	Add P6434 Probes	1	2	3	4
3P	Add P6417 Probes	2	4	6	8

Please refer to the "Logic Analyzer Probe Selection Guidelines" for further details on the probe which is best for your application.

TLA62X

Logic Analyzer with Internal Display.

Includes: Mouse, Keyboard, Front-panel cover, Accessory Pouch, Probe Retainer Bracket, Probe Manual, Power Cord (North American 120 VAC, 60 Hz), Software, User Manual, Certificate of Calibration, and One-year Warranty (return to Tektronix), and your choice of probes.

TLA621 – 34 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 1 M depth (must select one probe option below). Option for up to 200 MHz state.

TLA622 – 68 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 1 M depth (must select one probe option below). Option for up to 200 MHz state.

TLA623 – 102 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 1 M depth (must select one probe option below). Option for up to 200 MHz state.

TLA624 – 136 channel Logic Analyzer, 2 GHz timing, 100 MHz state, 1 M depth (must select one probe option below). Option for up to 200 MHz state.

Logic Analyzer Probe Options

Opt. 1P – Add P6418 17 channel general-purpose probes (each includes two 8 channel leadsets, one 1 channel leadset, 20 SMT KlipChip™ grabber tips).

Opt. 2P – Add P6434 34 channel high-density probe(s).

Opt. 3P – Add P6417 17 channel general-purpose probes (each includes two 8 channel leadsets, one 1 channel leadset, 20 SMT KlipChip grabber tips). Quantity of probes per option.

TLA60X/61X Logic Analyzer Options

(Base configuration is 64 K depth @ 100 MHz state)

1S – Increase to 256 K depth @ 100 MHz state.

4S – Increase to 64 K depth @ 200 MHz state.

5S – Increase to 256 K depth @ 200 MHz state.

TLA62X Logic Analyzer Option

(Base configuration is 1 M depth @ 100 MHz state)

6S – Increase to 1 M depth @ 200 MHz state.

TLA60X/61X/62X Options

Opt. 1J – 128 MB DRAM/30 GB hard disk.

Opt. 1K – Add LACART logic analyzer cart.

Opt. 1M – Add 17 in. monitor (119-5700-00).

Opt. 2M – Add 21 in. monitor (119-5798-00).

TLA714

Portable Color Mainframe.

Includes: Mouse, Keyboard, Front-panel Cover, Accessory Pouch, Two Dual-wide Panel Fillers for Empty Slots, Printer Adapter, Power Cord (North American 120 VAC, 60 Hz), Software, User Manual, Certificate of Calibration, and One-year Warranty (return to Tektronix).

TLA720

Benchtop Color Mainframe.

Includes: Mouse, Keyboard, Five Dual-wide Panel Fillers for Empty Slots, Printer Adapter, Two P6041 SMB to BNC Adapter Cables; Power Cord (North American 120 VAC, 60 Hz), Software, User Manual, Certificate of Calibration, and One-year Warranty (return to Tektronix). Display is not included – order Opt. 1M or Opt. 2M or use any SVGA monitor.

TLA7XM

Expansion Mainframe.

Includes: Two expansion modules, Three expansion cables, Six dual-wide panel fillers for empty slots, One single-wide panel filler for empty slot, manual, Power Cord (North American 120 VAC, 60 Hz), Statement of Compliance, and One-year Warranty (return to Tektronix).

If installing a TLA7XM expansion mainframe into a TLA704/TLA711 or TLA714/TLA720 mainframe, please consult the TLA Family Upgrade Guide for upgrade information.

TLA714/720 Options

Opt. 1S – 128 MB DRAM/30 GB replaceable hard disk (TLA714 only).

Opt. 1A – Add LAN PC Card (119-6072-00).

Opt. 1K – Add LACART logic analyzer cart.

Opt. 1M – Add 17 in. monitor (119-5700-00).

Opt. 2M – Add 21 in. monitor (119-5798-00).

Logic Analyzer Modules

Includes: Probe retainer bracket, Probe Manual, User Manual, Certificate of Calibration, One-year Warranty (return to Tektronix), and your choice of probes.

TLA7N1 – 34 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 4 M depth and/or 200 MHz state.

TLA7N2 – 68 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 4 M depth and/or 200 MHz state.

TLA7N3 – 102 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 4 M depth and/or 200 MHz state.

TLA7N4 – 136 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 K depth (must select one probe option below). Options for up to 4 M depth and/or 200 MHz state.

TLA7P2 – 68 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 16 M depth (must select one probe option below). Option for up to 200 MHz state.

TLA7P4 – 136 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 16 M depth (must select one probe option below). Option for up to 200 MHz state.

TLA7Q2 – 68 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 M depth (must select one probe option below). Option for up to 200 MHz state.

TLA7Q4 – 136 channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 M depth (must select one probe option below). Option for up to 200 MHz state.

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Logic Analyzer "N, P & Q" Module Probe Options

Opt. 1P – Add P6418 17 channel general-purpose probes (each includes two 8 channel leadsets, one 1 channel leadset, 20 SMT KlipChip™ grabber tips).

Opt. 2P – Add P6434 34 channel high-density probe(s).

Opt. 3P – Add P6417 17 channel general-purpose probes (each includes two 8 channel leadsets, one 1 channel leadset, 20 SMT KlipChip™ grabber tips).

Logic Analyzer "N" Module Options

(Base configuration is 64 K depth @ 100 MHz state)

1S – Increase to 256 K depth @ 100 MHz state.

2S – Increase to 1 M depth @ 100 MHz state.

3S – Increase to 4 M depth @ 100 MHz state.

4S – Increase to 64 K depth @ 200 MHz state.

5S – Increase to 256 K depth @ 200 MHz state.

6S – Increase to 1 M depth @ 200 MHz state.

7S – Increase to 4 M depth @ 200 MHz state.

Logic Analyzer "P" Module Options

(Base configuration is 16 M depth @ 100 MHz state)

1S – Increase to 16 M depth @ 200 MHz state.

Logic Analyzer "Q" Module Options

(Base configuration is 64 M depth @ 100 MHz state)

1S – Increase to 64 M depth @ 200 MHz state.

Pattern Generator Module

TLA7PG2 – 64 channel Pattern Generator Module, 134 MHz data rate, 256 K depth (please select probe option below).

Includes: Four probe cables, User Manual, Certificate of Calibration and one year warranty (return to Tektronix).

Opt. 1M – Increase to 1 M depth.

Opt. 1P – Add four P6470 TTL/CMOS probes (each includes two 8 channel leadsets and one 5 channel leadset).

Opt. 2P – Add four P6471 ECL probes (each includes two 8 channel leadsets and one 5 channel leadset).

Opt. 1C – Add 168 SMT KlipChip grabber tips.

Digitizing Oscilloscope Modules

Includes: Probes, User Manual, Certificate of Calibration, and One-year Warranty (return to Tektronix).

TLA7D1 – 2 channel DSO module, 500 MHz bandwidth, 2.5 GS/s sample rate, 15 K depth (includes two P6243 1.0 GHz active FET probes, probe calibration adapter, and manual).

TLA7D2 – 4 channel DSO module, 500 MHz bandwidth, 2.5 GS/s sample rate, 15 K depth (includes four P6243 1.0 GHz active FET probes, probe calibration adapter, and manual).

TLA7E1 – 2 channel DSO module, 1 GHz bandwidth, 5 GS/s sample rate, 15 K depth (includes two P6245 1.5 GHz active FET probes, probe calibration adapter, and manual).

TLA7E2 – 4 channel DSO module, 1 GHz bandwidth, 5 GS/s sample rate, 15 K depth (includes four P6245 1.5 GHz active FET probes, probe calibration adapter, and manual).

TLA Family International Power Plugs

Opt. A1 – Universal Euro 220 VAC; 50 Hz.

Opt. A2 – UK 240 VAC; 50 Hz.

Opt. A3 – Australian 240 VAC; 50 Hz.

Opt. A4 – North American 240 VAC; 60 Hz.

Opt. A5 – Switzerland 220 VAC; 50 Hz.

Opt. A99 – No Power Cord.

TLA Family Service Options

Opt. IN – Product installation service (on-site configuration and user familiarization; excluding network integration).

Opt. R3 – Extends depot repair warranty service period to three years.

Opt. S1 – Uplifts standard one-year warranty service of mainframe and installed modules to on-site service.

Opt. S3 – Uplifts Opt. C3 and/or R3 of mainframe and installed modules to on-site service (must be ordered with Opt. C3 and/or R3).

Opt. C3 – Three years of Calibration Service (includes initial calibration and two annual calibrations).

Add calibration test data report.

Opt. D1 – Add calibration test data report.

Opt. D3 – Provides test data for each calibration (must be ordered with Opt. C3).

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