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User Manual

Tektronix

VX4244
16-Channel Digitizer Module

070-9067-06

This document supports firmware version X.XX and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

CE

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Avoid Electric Overload

To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Ground the Product

This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

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Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:



DANGER
High Voltage



Protective Ground
(Earth) Terminal



ATTENTION
Refer to Manual



Double
Insulated

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Certifications and Compliances

Overvoltage Category

Overvoltage categories are defined as follows:

CAT III: Distribution level mains, fixed installation

CAT II: Local level mains, appliances, portable equipment

CAT I: Signal level, special equipment or parts of equipment, telecommunication, electronics

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Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

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Preface

This is the user manual for the VX4244 16-Channel Digitizer Module.

Please read and follow all instructions for installation and configuration. Use the Installation Checklist to insure proper installation, and as a record of initial settings.

This manual assumes you are familiar with VXIbus instruments and operation, and with the purpose and function of this instrument. The *Operating Basics* section gives a summary of VXIbus operation, and presents an overview of this instrument's operation.

The *Syntax and Commands* section has a summary of all the commands, and detailed descriptions of each command.

Conventions

The names of all switches, controls, and indicators appear in this manual exactly as they appear on the instrument.

Specific conventions for programming are given in the section *Syntax and Commands* and in *Appendix E: Examples*.

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Getting Started

This section begins with a brief description of the VX4244, and then explains how to configure and install the module in a VXIbus mainframe. Then you can choose to perform the quick functional check, also included in this section, to gain confidence that the instrument operates properly.

Product Description

The VX4244 16-Channel Digitizer Module is a printed circuit board assembly for use in a mainframe conforming to the VXIbus Specification. The VX4244 supplies sixteen channels of 16-bit differential input, analog-to-digital conversion data, sampling at up to 200 kHz. The sixteen analog inputs are organized as four groups of four channels each. Each group can operate independently, or in concert with any or all of the other groups. For example, one group could be actively acquiring data, while the second group is waiting for a trigger, the third group transferring data, and the fourth group is being post-processed. Programmable features of each channel group include the sampling frequency, arming, triggering, acquisition control (pre-/center-/post-triggering), and the number of active channels in the group. In addition, each channel's input range is independently programmable.

Refer to Figure 1–1 for a functional block diagram of the VX4244.

Triggering

The VX4244 provides extensive triggering control. The trigger inputs for each channel group include the eight VXI TTL triggers, an external trigger input, an internal (software) trigger, the VXI command trigger, and a four-quadrant threshold/ slope trigger. Any or all of these twelve conditions can be logically ANDed or ORed to generate the group trigger (except for the VXI command and software triggers, which are mutually exclusive). In addition, each of the four group triggers is fed to a master trigger logic circuit, which allows the four group triggers to be logically ANDed or ORed to generate a master trigger output. The master trigger out can also be programmed to strobe any of the eight VXI TTL triggers.

Time-tag

A 32-bit time-tag counter is provided for each channel group. The input to the time-tag can be either the VXI 10 MHz ECL clock (100 ns resolution), or the master sampling clock. The time-tag clocks are free-running until the channel group is triggered (at which time the counters are inhibited from counting). The SYNC signal described below can be used to reset the time-tag counters.

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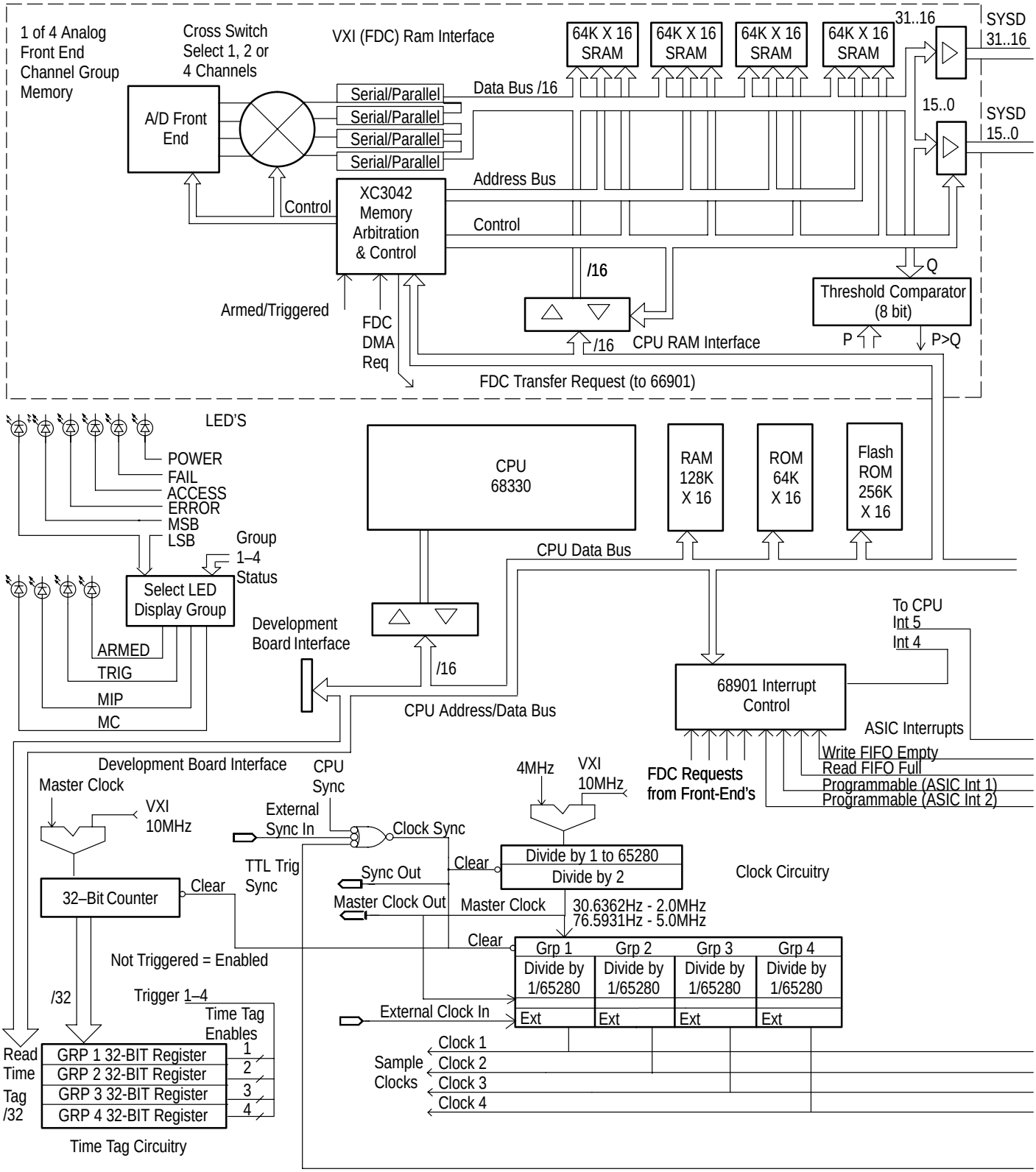
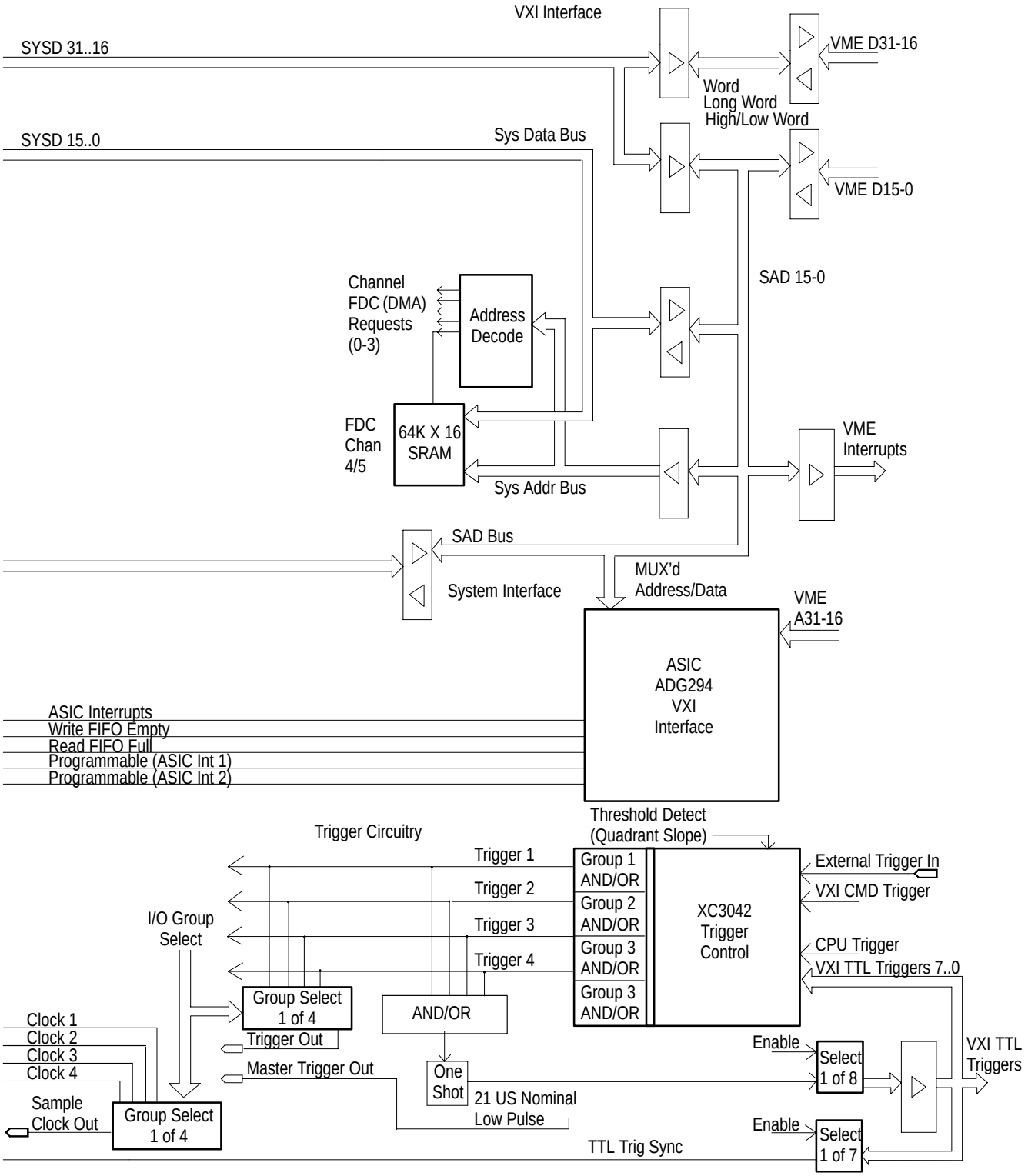


Figure 1–1: VX4244 Block Diagram

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Synchronization

A SYNC function is provided for synchronizing multiple digitizers. This function can be programmed to use any of seven (1 through 7) VXI TTL trigger inputs (if enabled), a software command, or an external sync input. The SYNC input is the logical OR of these conditions. The SYNC signal is global to all channel groups, and resets all frequency generation counters on the module. In addition, the SYNC signal is used to reset the time-tag counters. A front panel SYNC OUT signal is provided which is the logical OR of the three conditions described above.

Sampling

The module uses a two-stage clock scheme. The first stage is the master (reference) clock. Its source can be programmed to be either internal (4 MHz) or the VXI 10 MHz ECL clock. This clock is divided by two, then fed to a 16-bit divider to generate the master clock. The master clock is then fed to each of the four channel groups, which employ an additional 16-bit divider to generate the actual sampling clock for the group. In addition, each group can be programmed to use the EXTERNAL CLOCK input signal from the front panel.

Data Collection

Pre-/center-/post-triggering is programmable for each channel group. In addition, Fast Data Channel (FDC) requests can be generated at programmable sample counts. This programmability allows data to be transferred from a group at the same time data is being acquired.

Configuration

The number of channels active within each group is programmable. Any one of the four channels may be enabled, or any two of the four channels, or all four channels can be enabled. A total of 256 Kwords of memory is available to each channel group. If only one channel is enabled, it gets the entire 256 Kwords. For two channels, each channel gets 128 Kwords, and for four channels, each channel gets 64 Kwords.

Inputs

Each channel's differential input range is independently programmable to ±0.2, 0.5, 1.0, 2.0, 5.0, 10.0, or 20.0 V. Single-ended signals can be acquired by grounding the negative side of the input.

An isolation relay is supplied for each input, to protect both the module and the unit-under-test from spurious voltages on power-on. These relays switch between an on-board reference for self test (default), and the analog inputs.

DSP

To facilitate interfacing to digital signal processors, all serial bit streams and required control signals from all sixteen A/D channels are brought out through the front-edge connector.

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Fuses

The VX4244 Module has +5, –5, +12, –12, +24, –24, and –2 V fuse(s). The fuses protect the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

If the +5 V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If any fuse opens, the fault must be removed before the fuse is replaced. Refer to a qualified service person for assistance.

BITE (Built-in Test Equipment)

Built-in Test Equipment is provided by extensive self tests that are automatically invoked on power-up, and may also be invoked on command. Circuitry tested includes the CPU and all memory, the Analog-to-Digital (A/D) converters, thresholds, latches and counters, the analog front-end, and the signal cross switching. Arming, triggering, measurement complete, time-tag, and EEPROM are also tested. The front panel LEDs provide visual BITE for module operation.

Accessories

Table 1–1 lists the standard accessories included with the VX4244.

Table 1–1: Standard Accessories

Accessory	Part Number
VX4244 User Manual	070-9067-XX
VX4244 Reference Manual	070-9377-XX

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Controls and Indicators

The following controls and indicators are provided to select and display the functions of the VX4244 Module's operating environment. See Figures 1–2 and 1–3 for their physical locations.

Switches

The Logical Address switches must be correctly set to insure proper operation. See *Configuration* for details of how to set the switches.

LEDs

The following LEDs are visible at the top of the VX4244 Module's front panel to indicate the status of the module's operation. See *Operating Basics* for a description of each LED's meaning.

POWER	FAIL
ARMED	ACCESS
TRIG	ERROR
MIP	GRP2
MC	GRP1

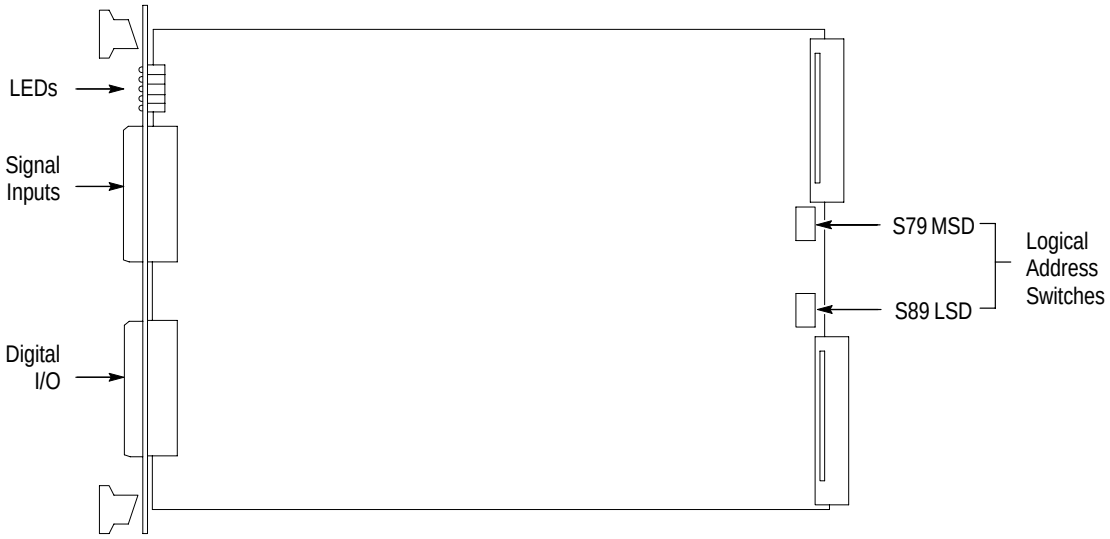


Figure 1–2: VX4244 Connector, Indicator, and Switch Locations

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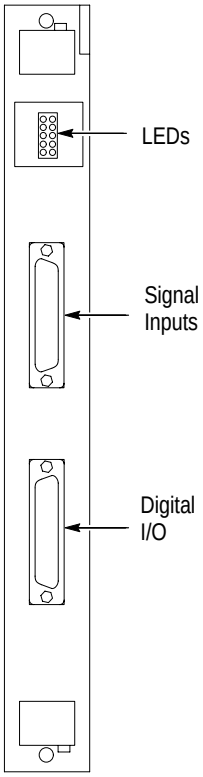


Figure 1–3: VX4244 Front Panel

Configuration

The following switches must be correctly set to insure proper operation. Refer to Figure 1–2 for their physical locations.

Logical Address Switches

Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4244 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

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The actual physical address of the VX4244 Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4244 will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Address (d)
Ah	0	A	(64 * 10) + 49152 = 49792d
15h	1	5	(64 * 21) + 49152 = 50496d

where:

L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the VX4244 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address. Consult the operating manual of the IEEE-488 Interface Module being used.

Front Panel Connectors

The front panel has two 50-pin D-type connectors. Refer to *Appendix B* for connector pinouts.

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Installation

This section describes how to install the VX4244.

Tools Required

A slotted screwdriver set is required for proper installation.

Requirements and Cautions

The VX4244 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's Logical Address switch defines the module's programming address. Refer to *Configuration* for information on selecting and setting the module's logical address. To avoid confusion, it is recommended that the slot number and the logical address be the same.

***NOTE**. Note that there are two printed ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector marked "VX4244" is at the top.*

In order to maintain proper mainframe cooling, unused mainframe slots must be covered with the blank front panels supplied with the mainframe.

Based on the number of instrument modules ordered with a Tektronix mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot and C size double-slot blank front panels can be ordered from your Tektronix supplier.

***NOTE**. Verify that the mainframe is able to provide adequate cooling and power with this module installed. Refer to the mainframe Operating Manual for instructions.*

If the VX4244 is used in a Tektronix Mainframe, all VX4244 cooling requirements will be met.

***NOTE**. If the VX4244 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VXI Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.*

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Installation Procedure

Follow these steps to install the VX4244.

CAUTION. *The VX4244 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.*

1. Record the revision level, serial number (located on the label on the top shield of the VX4244), and switch settings on the Installation Checklist.
2. The module can now be inserted into one of the instrument slots of the mainframe.
3. Cable Installation. If the mainframe has a cable tray, route the cable from the front panel of the module down through the cable tray at the bottom of the mainframe and out the rear of the mainframe.

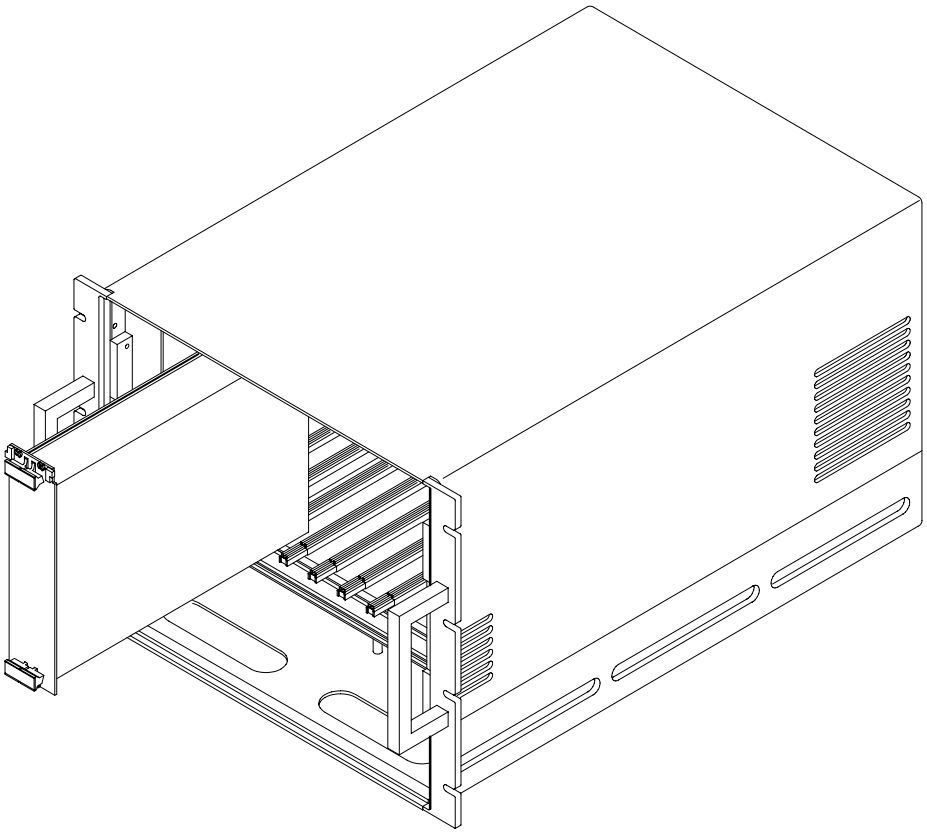


Figure 1–4: Module Installation

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Installation Checklist

Installation parameters will vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the module.

Revision Level: _____

Serial No.: _____

Mainframe Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____
(FFh enables dynamic configuration.)

Interrupt Level Select Switch: Dynamically programmed by the Resource Manager.

Cables Installed: (if any)

Performed by: _____ Date: _____

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Functional Check

The VX4244 Module will execute a self test at power-on, or on direction of a VXIbus hard or soft reset condition, or on command. The power-on self test consists of an interface self test and an instrument self test. The commanded self test performs only the instrument self test. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4244's commander, sets the Reset bit in the VX4244's Control register.

At power-on, as well as during self test, all analog inputs remain isolated from the module's front panel connector.

During power-on, or a hard or soft reset, the following actions take place:

1. The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing a self test, and the Failed LED is on. In the case of a soft reset, SYSFAIL* is set. However, all Tektronix/CDS commanders will simultaneously set SYSFAIL INHIBIT. This is done to prevent the resource manager from prematurely reporting the failure of a card.

2. A subset of the instrument self test, as described in the *TST command, is then executed. This tests the CPU and all memory, the Analog to Digital (A/D) converters, thresholds, latches and counters, and the analog front-end. Arming, triggering, measurement complete, time-tag, and EEPROM are also tested. If the self test fails, the module makes an internal record of what failure(s) occurred. The ERROR? command can be used to view the results.

3. On completion of the interface self test, SYSFAIL* is de-asserted. If the test fails, the SYSFAIL* line remains active. If the interface self test passed, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). If it failed, the module enters the VXIbus FAILED state.

After self test, the module is returned to its default state, as described in the *RST command description.

Self test can also be run at any time during normal operation by using the *TST command. This test is more comprehensive than the power-on test, as it is not subject to the 5 second completion requirement. At the end of a self test initiated by this command, the module is restored to its power-on state.

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During a commanded self test:

1. SYSFAIL* is not asserted.
2. The module executes a comprehensive test of the instrument.
3. When the self test is completed, the module sets itself to the power-on default state, with the exception of queuing any errors detected by the self test. The ERROR? command can be used to view the results.

SYSFAIL * Operation

SYSFAIL* becomes active during power-on, hard or soft reset, self test, or if the module loses any of its power voltages. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4244 Module to deactivate SYSFAIL* in all cases except when +5 V power is lost.

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Operating Basics

The VX4244 16-Channel Digitizer Module is a VXIbus Message Based instrument, and communicates using the VXIbus Word Serial Protocol. The module is programmed by ASCII characters issued from the system controller to the VX4244 via the module's VXIbus commander and the VXIbus mainframe backplane. Refer to the manual for the VXIbus device that will be the VX4244 Module's commander for details on the operation of that device.

The sixteen analog inputs of the VX4244 are organized as four groups of four channels each. Each group can operate independently, or in concert with any or all of the other groups. For example, one group could be actively acquiring data, while the second group is waiting for a trigger, the third group transferring data, and the fourth group is being post-processed. Programmable features of each channel group include the sampling frequency, arming, triggering, acquisition control (pre-/center-/post-triggering), and the number of active channels in the group. In addition, each channel's input range is independently programmable.

Power-on

The VX4244 will complete its self test and be ready for programming five seconds after power-on. The VXIbus Resource Manager may add an additional one or two second delay. The Power LED will be on, and all other LEDs off. The MSG LED will blink during the power-on sequence as the VXIbus Resource Manager addresses all modules in the mainframe. The default condition of the module after power-on is is listed in the *RST command description. Self test failures are described in *Appendix C*.

The format and syntax for the command strings is described in *Syntax and Commands*. An alphabetical listing of the complete description of each command is in the *Command Descriptions*.

Front-Panel Indicators

The VX4244 current operating status may be determined from the LEDs on the front panel.

Power LED This green LED is normally lighted and is extinguished if the ±5, –2, ±12, or ±24 V supplies fail or module fuses blow.

Failed LED This normally off red LED is lighted whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete an

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interface self test, loss of a power rail, or failure of the module's central processor.

If the module loses any of its power voltages, the Failed LED will go on and SYSFAIL* will be asserted. A module power failure is indicated when the module's Power LED is extinguished.

Access LED This yellow LED is normally off. When lighted, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a 5 µs cycle will light the LED for approximately 0.2 seconds. The LED will remain lighted if the module is being constantly accessed.

Armed LED When lighted, this green LED indicates the channel group is "armed" and is awaiting or processing the trigger. This LED goes out when data sampling is complete.

TRIG (Triggered) LED When lighted, this green LED indicates the channel group has triggered.

MIP (Measurement In Progress) LED When lighted, this green LED indicates that sampling for the channel group is taking place. The LED is turned off whenever the memory is full, the memory is accessed via the CPU, or the module is halted or reset.

MC (Measurement Complete) LED This green LED indicates the conversion process for the channel group is complete.

Error LED This yellow LED indicates an error has been detected by the module. It is cleared when all errors have been read from the module, or the module is reset.

GRP2, GRP1 LEDs These LEDs reflect the current channel group being displayed (see the DISPlay command). They are encoded as shown below.

GRP2	GRP1	Group
Off	Off	1
Off	On	2
On	Off	3
On	On	4

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Instrument I/O – VXIbus Basics



CAUTION. *If the user's mainframe has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR* (as defined by the VXIbus Specification) may cause operating problems on these boards.*

The VX4244 Module is a C size single slot VXIbus Message-Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4244 Module is neither a VXIbus commander or VMEbus master, and therefore it does not have a VXIbus Signal register. The VX4244 is a VXIbus message based servant.

The module supports the Normal Transfer Mode of the VXIbus, using the Write Ready, Read Ready, Data In Ready (DIR), and Data Out Ready (DOR) bits of the module's Response register.

A Normal Transfer Mode read of the VX4244 Module proceeds as follows:

1. The commander reads the VX4244's Response register and checks if the Write Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.
2. The commander writes the Byte Request command (0DEFFh) to the VX4244's Data Low register.
3. The commander reads the VX4244's Response register and checks if the Read Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.
4. The commander reads the VX4244's Data Low register.

A Normal Transfer Mode Write to the VX4244 Module proceeds as follows:

1. The commander reads the VX4244's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready and DIR bits until they are true.
2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX, depending on the End bit) to the VX4244's Data Low register.

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The VX4244 Module also supports the Fast Handshake Mode during readback. In this mode, the module is capable of transferring data at optimal backplane speed without the need of the commander's testing any of the handshake bits. The VX4244 Module asserts BERR* to switch from Fast Handshake Mode to Normal Transfer Mode, per VXI Specification. The VX4244's Read Ready, Write Ready, DIR and DOR bits react properly, in case the commander does not support the Fast Handshake Mode.

A Fast Handshake Transfer Mode Read of the VX4244 Module proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the VX4244's Data Low register.
2. The commander reads the VX4244's Data Low register.

The VX4244 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the VX4244's address space may cause incorrect operation of the module.

As with all VXIbus devices, the VX4244 Module has registers located within a 64 byte block in the A16 address space.

The base address of the VX4244 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches.

VX4244 Configuration Registers

Table 2–1 is a list of the VX4244 Configuration registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The address is relative to the module's base address.

Table 2–1: Register Definitions

Register	Address	Type	Value (Bits 15–0)
ID Register	0000H	RO	1011 1111 1111 1100 (BFFCh)
Device Type	0002H	RO	See Device Type definition below
Status	0004H	R	Defined by state of interface
Control	0004H	W	Defined by state of interface
Offset	0006H	WO	Not used
Protocol	0008H	RO	1111 0111 1111 1111 (F7FFh)
Response	000AH	RO	Defined by state of the interface

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Table 2–1: Register Definitions (Cont.)

Register	Address	Type	Value (Bits 15–0)
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below
Data Low	000EH	R	See Data Low definition below

Register Bit Definitions. The Read Protocol command response is F62Bh.

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Command Syntax

Command protocol and syntax for the VX4244 Module are as follows:

- A command string consists of a string of ASCII-encoded characters (up to 255 maximum) terminated by a <program message terminator>. The <program message terminator> is optional white space, followed by any one of the following command terminations:

  A line feed <LF> character (0a hex, 10 decimal)

  The END bit set

  The END bit with a line feed

  The command string is buffered until the terminator is encountered, at which time the entire string is processed.

- Commands can be sent either individually, or strung together by delimiting the individual commands with a semi-colon (;). For example, the string

  ```
  VOLT:RANGE 10 (@2);TRIG:SOURCE EXT (@1)
  ```

  sets channel 2 to a voltage range of ±10 volts, and group 1's trigger source to the external trigger input.

NOTE. *Up to twenty command strings can be queued for processing by the module. If this limit is exceeded, the additional command strings will be lost, until space is freed up on the input queue. The Wait to Continue (*WAI) and Operation Complete Query (*OPC?) commands will block processing and cause the queue to fill up.*

- All characters in a command may be sent in either upper or lower case form.
- Multiple data parameters passed by a command, or returned in a response are separated by a comma (,).

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- White space characters can be used to make a command string more readable, and are ASCII-encoded bytes in the range 00–09, 0B–20 hex (0–9,11–32 decimal). This range includes the ASCII control characters and the space, but excludes the line feed <LF>. White space characters are ignored when legally encountered in a command string. White space is allowed anywhere in a command string, EXCEPT for the following:

  Within a program mnemonic (for example, `VO LT`)

  Around a colon (:) mnemonic separator (for example, `VOLT: RANGE` or `VOLT :RANGE`)

  Between a mnemonic and a (?) (for example, `VOLT:RANGE ?`)

  Following an asterisk (*) (for example, `* STB?`)

  Within a number (for example, `12 34`)

  Within a channel/group list (for example, `( @1) or (@1, 2)`)

  The following is a legal command string illustrating the use of white space:

  ```
  VOLT:RANGE 1.OOE+1 (@1,2,5:9); ERR?; fetch:data? 10 , 11
  ```

  Without white spaces, this string is:

  ```
  VOLT:RANGE1.OOE+1(@1,2,5,9);ERR?;fetch:data?10,11
  ```

- A question mark (?) following a command indicates a response is to be returned. All responses from the module are terminated with the line feed <LF> (0a hex) character.

NOTE. *If a read operation is performed without first issuing a command requiring a response (?), a BUS TIMEOUT will occur.*

- In the command descriptions, the following special characters are used. Except for the colon (:), these characters are not part of the command, and should not be sent. If an optional field is omitted, the command's default will be applied.

  [ ] Brackets indicate an optional field

  | A bar indicates a logical OR choice

  : A colon is used to separate command fields

  < > Field indicator

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Field Definitions

<channel list>. The channel list field is used to apply commands to multiple channels. Channels can be listed individually, separated by a comma; sequentially, separated by a colon; or a combination of the two. For example, (@1,3,5,9:11,16) specifies channels 1, 3, 5, 9, 10, 11, and 16. Valid channel numbers are 1 through 16. If a query response is expected from the command, the response is returned in the same order as the channel list. For example specifying (@1,16,2) returns the value of channel 1, followed by the value of channel 16, followed by the value of channel 2. In addition (ALL) can be specified as a channel list, equivalent to (@1:16).

<group list>. The group list field is used for those commands which apply to a channel group. There are four channel groups of four channels each:

Group	Channels
1	1 – 4
2	5 – 8
3	9 – 12
4	13 – 16

The same syntax as the <channel list> applies to the <group list>. For example, (@1,2,3:4) specifies groups 1, 2, 3, and 4. In addition (ALL) can be specified as a group list, equivalent to (@1:4).

<channel id> or <group id>. Some commands can only be specified on a single channel or group. The syntax is the same as above, but only one channel or group can be specified, for example, (@1).

Specifiers

<boolean>. ASCII 0 or 1

<hex16 value>. 16 bit hex value, ASCII 0000 through FFFF, right justified.

<x..y>. Any single value between x and y, inclusive of x and y.

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Syntax Example

Capital letters indicate the minimum required characters which need to be sent. Lower case letters are optional. As an example, the syntax of one of the voltage commands is given as:

```
[SENSe:]VOLTage[:DC]:RANGe[:UPPer] <voltage> [<channel list>]
```

Each of the following is a valid form of this command:

```
SENSE:VOLTAGE:DC:RANGE:UPPER 1.0E+00 (@1)

volt:dc:rang:upp 1.0 (@1)

volt:rang:upp 1 (@1)

volt:rang 1 (defaults to channel 1)
```

Numeric Value Formats

When specifying numeric values, fixed or floating-point formats are allowed. All numbers are rounded to the nearest value appropriate for the particular command as specified in the command description. If a sign is not specified, the number is assumed to be positive.

A number whose value is 5 can be represented by any of the following:

```
5

5.0000

+.5e1

+05

50E-1

5.0

0.500E+001

0.0000000000000005e16
```


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Functional Command Groups

This section lists the VX4244 commands by functional command group.

System Commands

Although these non-data commands are initiated by the VX4244's commander rather than the system controller, they have an effect on the VX4244 Module. The following VXIbus Instrument Protocol Commands will affect the VX4244:

Command	Effect
Clear	The module clears its VXIbus interface and any pending commands. Current module operations are unaffected.
Trigger	If programmed, this command can be used to trigger the VX4244 sampling process.
Begin Normal Operation	The module will begin operation if it has not already done so.
Read Protocol	The module will return its protocol to its commander.

Module Commands

A summary of the VX4244 Module's commands is listed below. This is followed by detailed descriptions of each of the commands. A sample program using these commands is shown in *Appendix E: Examples*.

Command Summary

Command	Description
ABORt	stops data sampling on the group(s) specified.
ARM	controls the use of the external ARM input, and zeroing memory when a group(s) is INITiated.
CALibrate	calibrates the channel specified for the voltage range specified.
DISPlay	controls the LED display on the front panel: ARMED, TRIG, MIP, and MC, showing the state of the specified channel group.
ERRor	reads the error messages from the module or returns the number of error messages queued.
FDC	sets up Fast Data Channel functions.
FETCh	retrieves some basic signal parameters.
FORMat	enables/disables overrun flagging.
FREQuency	sets various sampling clock parameters, and controls clock synchronization.
INITiate	arms the specified channel groups.
OUTPut	controls various output functions of the module.

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Command	Description
ROSCillator	sets the reference (master) clock frequency.
ROUTe	defines the active channels within a channel group.
SWEep	sets up the group sampling frequencies and record lengths
TRIGger	sets group triggering parameters.
VERSion	returns the SCPI command version level.
VOLTage	sets the input voltage ranges of the channels.

IEEE 488.2 Commands

Command	Description
*CAL?	Calibration query; returns the calibration status.
*CLS	Clear Status command; clears the Event Status Register (ESR) and any pending Service Requests (SRQs).
*ESE <mask>	Event Status Enable (ESE) command; defines the mask for event status reporting.
*ESE?	Event Status Enable (ESE) query; returns the value of the Event Status Enable register.
*ESR?	Event Status Register (ESR) query; returns the value of the Event Status Register.
*IDN?	Identification query; returns a 4-field response.
*OPC	Operation Complete command; controls setting the OPC bit in the Event Status register (ESR).
*OPC?	Operation Complete query; puts a 1 in the output queue when all pending operations have been completed.
*RST	Reset; resets the module to its power-on state.
*SRE	Service Request Enable (SRE) register; defines the mask for generating VXI Request True interrupts.
*SRE?	Service Request Enable (SRE) query; returns the value of the Service Request Enable register.
*STB?	Status Byte (SB) query; returns the value of the status byte register.
*TST	Execute the self test.
*TST?	Self Test query; returns the self test status.
*WAI	Wait to Continue; suspends command processing until all pending operations have been completed.

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Command Descriptions

This section lists the VX4244-specific commands and queries in alphabetic order. The IEEE 488.2 Common Commands are listed in the next section.

ABORt

Command Syntax `ABORt [<group list>]`

Query Syntax N/A

Query Response(s) N/A

***RST Value** N/A

Limits N/A

Related Commands INITiate

Description The ABORt command disarms and stops data sampling (if active) on the specified group(s). All input relays of the specified group(s) are opened.

If [<group list>] is not specified, it defaults to 1.

Examples

Command	Response
ABORT (@1)	N/A; abort sampling on channel group 1.
abor (@1:4)	N/A; abort sampling on all channel groups.

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ARM

Command Syntax

```
ARM
   [:SEQuence[<n>]]
      [:LAYer[<n>]]
         :SLOPe  POSitive | NEGative
         :SOURce EXTernal | IMMediate [<group list>]
         :ZERO <boolean> [<group list>]
```

Query Syntax

```
ARM
   [:SEQuence[<n>]]
      [:LAYer[<n>]]
         :SLOPe?
         :SOURce? [<group list>]
         :ZERO?   [<group list>]
```

Query Response(s)

:SLOPe	POS | NEG	
:SOURce	EXT | IMM	
:ZERO	0 | 1	(1 = enabled)

***RST Value**

:SLOPe	POSitive	
:SOURce	IMMediate	(all groups)
:ZERO	0	(all groups)

Limits

<boolean>	0 | 1
<n>	1 to 32767

Related Commands INITiate

Description The ARM commands define various conditions for arming the group triggers in response to an INITiate command.

ARM:SLOPe defines the active *edge* of the external arm input. It is executed on receipt of an INITiate command.

ARM:SOURce EXTernal enables the external arm input. If EXTernal is specified, the INITiate command arms the external arm input, which must

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transition through the specified slope to arm the triggers. ARM:SOURce IMMediate internally arms the triggers on INITiate.

ARM:ZERO controls whether group memory is zeroed prior to arming the triggers when an INITiate command is received. A '1' indicates memory is to be cleared. A '0' does not clear the memory.

If [<group list>] is not specified, it defaults to 1. If <boolean> is not specified, it defaults to 0.

The optional SEQuence and LAYer fields are included for SCPI compatibility only, and have no effect on the module.

***NOTE**. The ARMED LED reflects the state of the internal armed signal only. When the module is armed, the LED will light regardless of the state of the external armed input (if enabled).*

***NOTE**. The external arm input is global to all channel groups. If a channel group has been previously initiated with negative slope, and external arm is enabled (and has not armed), then initiating a new channel group with a positive arm slope will cause the first group's external arm to become active.*

Examples

Command	Response
ARM:SEQUENCE1: LAYER1:SLOPE NEGATIVE	N/A; set external arm slope to negative edge true.
arm:slop?	NEG<LF>
arm:sour ext (@2)	N/A; set group 2 to enable external arm.
arm:source?(all)	IMM,EXT,IMM,IMM<LF>
ARM:zero 1 (@2,4)	N/A; enable zeroing of memory for groups 2 and 4.
arm:zero?(@1:4)	0,1,0,1<LF>

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CALibrate

Command Syntax

```
CALibrate
   :VALUe <calibration value> [<channel id>]
   :ZERO  <voltage range> [<channel id>]
```

Query Syntax

```
CALibrate
   :VALUe?
   :ZERO?
```

Query Response(s)

:VALUe?	+xx.xxxxxx, +yy.yyyyy (x's = offset value; y's = gain value)
:ZERO?	+xx.xxxxxx (offset value)

***RST value**

N/A

Limits

<calibration value>	0.0796 – 19.90
<voltage range>	0.2 – 20.0 (rounded up to nearest input range)

Related Commands

*CAL?

Description

This command calibrates the range specified for the channel specified. The CAL:VALUE command calibrates the gain and offset for the value specified (see the table below). The CAL:ZERO command calibrates only the offset for the range and channel specified. If <voltage range> is zero, the CAL:ZERO command will calibrate the offset for all ranges on the channel specified.

The Error LED will blink while the calibration command is being executed. This command resets the module prior to execution. After completion, the module is restored to its *RST state with the exception that calibration errors (if any) will be queued.

The CAL:VALUe? query returns the calibrated offset and gain values. The CAL:ZERO? query returns the calibrated offset value.

The *CAL? query, the Operation Complete bit of *ESR?, or the *SRE interrupt can be used to determine when the calibration has completed. If the calibration fails, the ERRor? command can be used to view the results.

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The following commands are allowed during the CALibrate routine (all others are ignored):

*CAL?	*ESE?	*ESR?	*IDN?
*SRE?	*STB?	*TST?	*WAI
*OPC	*OPC?		

If [<channel id>] is not specified, it defaults to 1.

For firmware revisions 1.3 and later, a differential calibration is performed to increase the DC accuracy of the input ranges. That is, each range is calibrated based on its +95% and –95% values. See Appendix G for the calibration procedure. Use the following calibration values to calibrate the implied input range:

Input Voltage Span	Recommended Calibrator Voltage	Range Calibrated
±0.0796 – ±0.199	±0.190 VDC	0.2
±0.199 – ±0.499	±0.475 VDC	0.5
±0.499 – ±0.999	±0.950 VDC	1.0
±0.999 – ±1.990	±1.900 VDC	2.0
±1.990 – ±4.990	±4.750 VDC	5.0
±4.990 – ±9.990	±9.500 VDC	10.0
±9.990 – ±19.90	±19.00 VDC	20.0

Examples

Command	Response
CALibrate:VALUe 0.19 (@5)	N/A; calibrate the gain and offset of the 0.2 volt range for channel 5 to an input value of 0.19 volts.
CAL:ZERO 5(@16)	N/A; zero the offset for channel 16, range 5.
CAL:ZERO 0 (@1)	N/A; zero the offset for all channel 1 ranges.
CALibrate:VALUe?	+0.000006,–0.190006<LF>
CAL:ZERO?	+0.000006<LF>

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DISPlay:GROUp

Command Syntax `DISPlay:GROUp [<1..4>]`

Query Syntax `DISPlay:GROUp?`

Query Response(s) 1 to 4 (currently displayed group)

***RST Value** 1

Limits 1 through 4

Related Commands N/A

Description The DISPlay:GROUp command controls the display on the front panel for the ARMED, TRIG (triggered), MIP (measurement in progress), and MC (measurement complete) LEDs. The state of these signals for the group specified is displayed. A lighted LED indicates the signal is active.

The group LEDs also provide a visual indication of which channel group is being displayed. These LEDs are encoded as:

GRP2	GRP1	Group
Unlit	Unlit	1
Unlit	Lit	2
Lit	Unlit	3
Lit	Lit	4

If [<1..4>] is not specified, it defaults to 1.

Examples

Command	Response
DISPLAY:GROUP 3	N/A; display group 3's status.
DISP:GROUP?	3<LF>
disp:grou 1	N/A; display group 1's status.

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ERRor?

Command Syntax N/A

Query Syntax

```
[SYSTem:]
   ERRor?
   ERRor:COUNt?
```

Query Response(s) Error message or number of errors queued.

***RST Value** N/A

Limits N/A

Related Commands N/A

Description The error command reads the error messages from the module. Up to 20 errors can be queued. Errors are output on a first-in first-out basis. If the error queue is filled, the last error in the queue is overwritten with the message –350,“Queue overflow”. If no errors are queued, or when the queue has been emptied, the module will respond with 0,“No error”. Where applicable, a <description> field is provided to clarify the error. The maximum error message length is 255 characters.

The ERR:COUNT? command returns the number of error messages queued.

If enabled, the module will set the appropriate Error bit in the Event Status register (*ESR? command) when an error is detected. See the *ESR? command for more detail.

Error values from –100 to –199 are Command errors. Error values from –200 to –299 are Execution errors. Error values from –300 to –399 are Device Dependent errors. Error values from –400 to –499 are Query errors. Error messages are:

```
0,"No error"
-100,"Command error;<description>"
-102,"Syntax error;<description>"
-103,"Invalid separator;<description>"
-109,"Missing parameter;<description>"
-110,"Command header error;<description>
-112,"Program mnemonic too long;<description>"
-113,"Undefined header;<description>"
```


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```
-131,"Invalid suffix;<description>"
-171,"Invalid expression;<description>"
-220,"Parameter error;<description>"
-221,"Settings conflict;<description>"
-222,"Data out of range;<description>"
-223,"Too much data;<description>"
-300,"Device-specific error;LCA failure,<description>"
-300,"Device-specific error;EEPROM error,<description>"
-300,"Device-specific error;Calibration error,<description>"
-311,"Memory error;<description>"
-315,"Configuration memory lost;<description>"
-330,"Self-test failed;<description>"
-350,"Queue overflow"
-400,"Query error;Missing '?'<description>"
-410,"Query INTERRUPTED"
```

Examples

Command	Response
SYSTEM:ERROR?	0,“No error”<LF>
err?	–113,“Undefined header;VOLX:RANGE 5”<LF>
ERR:Count?	1<LF>

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FETCh

Command Syntax N/A

Query Syntax

```
FETCh
   :MAXimum?        [<count>][,<starting address>] [<channel id>]
   :MINimum?        [<count>][,<starting address>] [<channel id>]
   :AVErage?        [<count>][,<starting address>] [<channel id>]
   :TRMS?           [<count>][,<starting address>] [<channel id>]
   :DATa?           <count>  [,<starting address>] [<channel id>]
   :BINary?         <count>  [,<starting address>] [<channel id>]
   :PTRansition?    [<count>][,<starting address>] [<channel id>]
   :NTRansition?    [<count>][,<starting address>] [<channel id>]
   :TIMEtag?        [<group list>]
```

Query Response(s) See the examples below.

***RST Value**

<count>	the amount of memory available/channel
<starting address>	0 (trigger address)

Limits

<count>	1 to the amount of memory available/channel
<starting address>	± the amount of memory available/channel

Related Commands ROUTe

TRIGger:OFFSet?

Description The FETCh commands retrieve some basic signal parameters.

<count> defines the number of samples to perform the FETCh on. For example, FETCh:MAX 100 returns the maximum value found in the first 100 samples after the trigger. If <count> is not specified, it defaults to the amount of memory available for that channel. <count> MUST be specified for FETCh:BINary and FETCh:DATa, or an out of range error will be generated.

<starting address> defines the starting address of the data relative to the trigger address (address 0). For example, FETCh:MIN 100,–50 returns the minimum value found in 100 samples beginning 50 locations before the trigger, the trigger point (address 0), and ending 49 locations after the trigger. If <starting address> is not specified, it defaults to 0. If a single channel is active in a group, there is a four sample ambiguity as to the actual trigger address. For example, if a

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threshold trigger was specified, the actual trigger point can be anywhere from address 0 to address 3. For two channels/group, the ambiguity is 2 (address 0 to 1). For four channels/group, there is no ambiguity. See the TRIGger:OFFSet? query for determining the actual trigger location.

If <channel id> is not specified, it defaults to 1. Except for time-tag data, note that only one channel can be specified per FETCh command. Also, the channel specified must have been ROUTed, or an error will be generated when a FETCh command is received.

Because the FETCh commands take a relatively long time to process, the Error LED will blink while the FETCh command is being executed. If a FETCh is requested on an armed channel, the channel's group will be disarmed before executing the FETCh. For this case, address 0 is set to the current write address of the memory (presumably the oldest data in memory).

MAXimum returns the maximum value found for the channel specified.

MINimum returns the minimum value found.

AVErage returns the average value calculated.

DATa returns ASCII encoded data. A maximum of 1000 data values can be returned per FETCh command.

BINary returns two's complement binary data via word serial. A maximum of 5000 binary data values can be returned per FETCh command. For two's complement data, hex 8000 represents negative full scale (–32768 decimal), hex 0000 represents 0, and hex 7fff represents positive full scale (32768 decimal). One bit below zero is ffff hex, and one bit above zero is 0001 hex. The actual value of the sample is (binary value * (voltage range / 32768)). For word serial transfers, the most significant byte is transferred first, followed by the least significant byte.

PTRansition returns the maximum positive transition found between any two successive data points.

NTRansition returns the maximum negative transition found between any two successive data points.

TRMS returns the true RMS value of the data. The TRMS is the square root of the sum of the squares of each data point, divided by the number of samples.

For the MAX, MIN, PTR, and NTR responses, the second value returned is the address of the data relative to the trigger address (0).

TIMEtag reads the time tag values of the specified group(s). The resolution of the time is based on the source programmed by the FREQ:TIMEtag command. The time-tag counters are zeroed when a synchronization pulse is received, then immediately begin counting. The counters continuously count until their respective group is triggered, at which time their count is frozen. This provides

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the relative time between group triggers and absolute time relative to the sync signal.

For a time-tag clock source of 10 MHz (100 ns resolution), the counters can count to 100e–9 * (2^32 – 1) = 429.497 seconds before rolling over. If the master clock were selected at 200 kHz (5 µs resolution), the counters would count to 21474.8 seconds (5.965 hours). If [<group list>] is not specified, it defaults to 1.

Examples

Command	Response
FETCH:MAXIMUM?(@1)	Fetch the maximum value of channel 1. The first value is the maximum value found. The second value is the address of the maximum value. +11.123456,0123456<LF>
fetch:data? 3,123455	Fetch the data around the maximum value found in the example above. +11.123000,+11.123456,+11.123400<LF>
fetc:min? 100	Fetch the minimum value of 100 samples beginning at address 0 of channel 1. –1.123456,0000000<LF>
fetch:ave? (@16)	Fetch the average value of channel 16. +3.333333<LF>
fetch:data? 3,250	Fetch 3 data values beginning 250 locations after the trigger. +11.123456, +1.234567, –1.234567<LF>
fetch:bin? 100,321	Fetch 100 binary samples beginning 321 locations after the trigger. —— returns two's complement binary data ——
fetch:ptr?	Fetch the maximum positive transition found. +1.234567,0123456<LF>
fetch:ntr?	Fetch the maximum negative transition found. –1.234567,0123456<LF>
fetch:timetag?(@2)	Fetch the time-tag value of channel 2. +1.123456789012E+02<LF>
fetch:trms?	Fetch the true RMS value. +0.003009<LF>

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FORMat

Command Syntax

```
FORMat
   :OVERrun <boolean>
```

Query Syntax

```
FORMat
   :OVERrun?
```

Query Response(s)

:OVERrun 0 | 1 (1 = enabled)

***RST Value**

:OVERrun 0 (off)

Limits

<boolean> 0 to 1

Related Commands

VXI:FDC
INITiate

Description

The FORMat:OVERrun command controls flagging of data loss during continuous Fast Data Channel (FDC) data acquisition.

The OVERrun option is a means to flag data loss when collecting data in a continuous (free-run) acquisition scenario. As memory is being filled, periodic Fast Data Channel (FDC) requests can be generated to off-load the data from the module. If the system controller does not off-load the data sufficiently fast, overrun can occur since data is continuously being acquired.

The overrun option uses the least significant bit (LSB) of the 16-bit data to flag when overrun has occurred. An LSB of 0 indicates no overrun. If overrun occurs, the LSB is set high for the four samples prior to where data loss occurred, and additional data acquisition is inhibited. As memory is freed by off-loading data from the module, additional data samples can be acquired.

For example, suppose that the module was set up with overrun enabled in the 2048 sample FDC AUTO mode, and initiated continuously:

```
FORMAT:OVERRUN 1; VXI:FDC MODE AUTO 2048; INIT:CONT
```

If no FDC transfers occurred, the module would collect 128 buffers of 2048 samples each, and then inhibit additional collection until a buffer was freed. The last four samples of the 128th buffer would have the LSB bit set to 1.

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The overrun function is global to all channel groups on the module. Because it affects the data values being acquired, it can not be modified if any group is actively sampling data. An error will be generated on receipt of an INITiate command if this is attempted. A ‘1’ enables the overrun mode. A ‘0’ disables it.

Examples

Command	Response
FORMAT:OVERRUN?	0<LF>
form:over 1	No response; enable overrun mode.

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FREQuency:TINTerval
FREQuency:RANGe

Command Syntax

```
[SENSe:]
   FREQuency
      :TINTerval [<time interval>] [<group list>]
      :RANGe [<frequency>] [<group list>]
```

Query Syntax

```
[SENSe:]
   FREQuency
      :TINTerval? [<group list>]
      :RANGe? [<group list>]
```

Query Response(s)

:TINTerval	+x.xxxxxxxE+xx (time interval)
:RANGe	+x.xxxxxxxE+xx (frequency value)

***RST Value**

:TINTerval	5 µs (all groups)
:RANGe	200 kHz (all groups)

Limits

:TINTerval	(1 to 65280) / (ROSCillator frequency) 5 µs minimum
:RANGe	(ROSCillator frequency) / (1 to 65280) 200 kHz Maximum

Related Commands

FREQ:SYNChronize
FREQ:SOURce
ROSCillator

Description

The FREQ:TINTerval and FREQ:RANGe commands define the sampling period/frequency of a channel group(s).

The FREQ:TINT and FREQ:RANGe commands set the sampling time interval/ sampling frequency of the group(s) specified. The VX4244 Module uses a two-stage clock scheme. The first stage is the reference (master) clock. This clock (ROSCillator) is fed to each of the four channel groups, which use dividers to generate the actual sampling clock of that group. These dividers can generate a sampling frequency of 1 to 1/65280th of the reference clock.

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The maximum group frequency is the lesser of the programmed value, the ROSCillator frequency / 2, or 200 kHz. If the specified frequency is greater than the (ROSCillator frequency / 2), an out of range error message will be generated. Programmed values are rounded to the nearest divisible integer value.

The query responses to the FREQ:TINT and FREQ:RANGe commands return the actual (rounded) time interval/frequency values programmed. The FREQ:TINT and FREQ:RANGe commands are reciprocals of each other (time = 1 / frequency).

If FREQ:SOURce:INTernal is specified, the dividers described above are used. EXTernal feeds the external clock directly to the analog/digital converters. That is, no division is performed on the external clock.

If [<group list>] is not specified, it defaults to 1. If <frequency> is not specified, it defaults to the lesser of the (ROSCillator frequency) / 2, or 200 kHz.

NOTE. *Be careful when using these commands. They are executed immediately after processing. Unlike programming the ROSCillator, these commands are allowed while a channel group is actively sampling. This is to allow dynamic modification of the sampling interval(s). The normal mode of operation is to program these parameters prior to arming the channel groups.*

NOTE. *Modifying the ROSCillator source or frequency automatically modifies the group frequencies to the lesser of the (ROSCillator frequency) / 2, or 200 kHz. Therefore the ROSCillator should be programmed (if required) prior to the group frequencies.*

Examples

Command	Response
SENSE:FREQUENCY :RANGE 200E3 (@1:4)	N/A; set the sampling frequency of all channel groups to 200 kHz (5 μs sampling period).
freq:tint 10e–6 (@2)	N/A; set group 2 to a 10 μsecond sampling period (100 kHz sampling frequency).
freq:tint? (@2)	+1.0000000E–05<LF>
freq:rang? (@1,2)	+2.0000000E+05,+1.0000000E+05<LF>

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FREQuency:SOURce
FREQuency:SLOPe
FREQuency:TIMEtag

Command Syntax

```
[SENSe:]
   FREQuency
      :SOURce INTernal | EXTernal [<group list>]
      :SLOPe  POSitive | NEGative
      :TIMEtag CLK10 | ROSCillator
```

Query Syntax

```
[SENSe:]:
   FREQuency
      :SOURce? [<group list>]
      :SLOPe?
      :TIMEtag?
```

Query Response(s)

:SOURce	INT | EXT
:SLOPe	POS | NEG
:TIMEtag	CLK10 | ROSC

***RST Value**

:SOURce	Internal
:SLOPe	Positive
:TIMEtag	Clk10

Limits N/A

Related commands

ROSCillator
FREQ:RANGe
FETCh:TIMEtag
FREQ:SYNChronize

Description The FREQ:SOURce command sets the source of the clock for the FREQ:TINT/ FREQ:RANGe commands. INTernal uses the internal clocks to generate the sampling frequencies for the group(s) specified. EXTernal uses the external clock input as the sampling clock.

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The FREQ:SLOPe command sets the active *edge* of the external clock input to either positive true or negative true. Data is sampled on the falling edge of the clock.

The FREQ:TIMEtag command sets the source of the time-tag clock to either the VXI 10 MHz ECL clock or the ROSCillator clock.

If [<group list>] is not specified, it defaults to 1.

NOTE. *Be careful when using these commands. They are executed immediately upon processing. Unlike programming the ROSCillator, these commands are allowed while a channel group is actively sampling. This is to allow dynamic modification of the parameters. The normal mode of operation is to program these parameters prior to arming the channel groups.*

Examples

Command	Response
freq:source ext	N/A; set group 1 to external clock input.
freq:sour? (all)	EXT,INT,INT,INT<LF>
freq:sour? (@2,1)	INT,EXT<LF>
freq:slope negative	N/A; set external clock slope to negative edge.
freq:slop?	NEG<LF>
freq:time?	CLK10<LF>
freq:timetag rosc	N/A; set the time-tag clock source to the reference oscillator.
freq:time?	ROSC<LF>

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FREQuency:SYNChronize

Command Syntax

```
[SENSe:]
   FREQuency
      :SYNChronize
         :LEVEl POSitive | NEGative
         :IMMediate
         :TTLTrg <1..7> | 8
```

Query Syntax

```
[SENSe:]
   FREQuency
      :SYNChronize
      :LEVEl?
      :TTLTrg?
```

Query Response(s)

:LEVEl	POS | NEG
:TTLTrg	1 to 7 | 8 (off)

***RST Value**

:LEVEl	Negative
:TTLTrg	8 (off)

Limits

:TTLTrg	1 through 8

Related Commands

ROSCillator
FREQuency: RANGE
FETCh:TIMEtag

Description

This command synchronizes the clocks for the channel groups, and/or synchronizes the clocks of multiple modules. Three means are provided for synchronization: via command (FREQ:SYNC:IMM); via the external sync input; or via one of the VXI TTL triggers (FREQ:SYNC:TTLTrg <1..7>). Synchronization will occur when any of these three signals is active (logical OR). The synchronization pulse also resets all time-tag counters to zero.

The active LEVEL of the external sync input can be programmed to be either a TTL level 1 (POSitive) or 0 (NEGative). For the VXI TTL triggers, note that TTL trigger 0 can NOT be used. Specifying SYNC:TTLTrg 8 inhibits the TTL trigger syncs.

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***NOTE**. Be careful when using synchronization. The intention is to program the group frequencies first, initiate a synchronization, and then arm the groups/modules. If any group is actively sampling, a sync signal will cause its clock to be reset, possibly causing an ambiguous sample to be taken. The SYNC commands are executed immediately upon processing.*

***NOTE**. Because the external sync input is a level, it can be used as a master clock gating signal to the module. That is, when the signal is active, all sampling clocks on the module are inhibited.*

Examples

Command	Response
SENSE:FREQ :SYNCHRONIZE:LEVEL POSITIVE	N/A; set the external sync input to high true.
FREQ:SYNC:LEVE?	POS<LF>
FREQ:SYNC:IMM	N/A; pulse the sync line.
FREQ:SYNC:TTLTrg?	8<LF>
freq:sync:ttlt 7	N/A; enable TTLTRG 7 as sync input.
freq:sync:ttltrg?	7<LF>

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INITiate

Command Syntax

```
INITiate
   [:IMMediate] [<group list>]
    :DELAy [<delay time>] [<group list>]
    :CONTinuous [<group list>]
```

Query Syntax N/A

Query Response(s) N/A

***RST value** N/A

Limits <delay time> 0 to 1e9 seconds in 16 ms increments

Related Commands

ABORt
ARM
FDC
FORMat
FREQuency
OUTPut
ROSCillator
ROUTe
SWEep
TRIGger
VOLTage

Description The INITiate command arms the specified channel groups. If [<group list>] is not specified, it defaults to 1. All INITiate commands perform the sequence described below, with the following differences.

The INIT:IMMediate command performs the sequence described below with no changes. The amount of data acquired after the trigger is specified by the SWEep command.

The INIT:DELAy command is the same as the INIT:IMM command, but will not arm the triggers until the specified delay period has expired. If, for example, the module was programmed to collect 100 samples (SWEep:POINts 100) after the trigger, and the trigger was active when INITiated, then only 100 samples would be collected. If one channel in the group was active, then the rest of the data would be old data from a previous acquisition (262044 samples). Assuming a sampling period of 5 µs (262044 * 5e–6 = 1.31022 seconds), then issuing the

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command “INIT:DELAy 1.31022” would acquire 1.31022 seconds worth of data prior to arming the trigger.

The delay can be programmed in increments of 16 ms, with a resolution of 16 ms. For example, specifying a delay of 32 ms will collect between 32 to 48 ms of data prior to arming the trigger. All delays are rounded up to their nearest 16 ms interval. If <delay value> is not specified, or is specified as 0, no delay will be executed.

The INIT:CONTinuous command puts the specified channel group(s) into free-running mode. Data acquisition continues indefinitely, until stopped by a *RST, ABORt, or FETCh command on the group(s) specified. When stopped, the trigger address (address 0) is set to the location where data acquisition stopped. Using the CONTinuous mode in conjunction with the Fast Data Channel (FDC) commands allows simultaneous acquisition and data off-loading to allow long-term data acquisition.

The INITiate sequence is:

1. The module verifies the overrun bit is not being modified if any group is actively armed (FORMat:OVERrun).
2. The module verifies there are channels ROUTed for the group(s) being initiated.
3. The module verifies the programmed SWEep:POINts size(s) and FDC <size(s)> (if applicable) are less than or equal to the amount of memory available per channel.
4. If a threshold trigger has been programmed, the module verifies the threshold channel specified has been ROUTed, and the level is within the programmed VOLTage range of the channel.

Assuming no errors are found, the following sequence is then performed:

1. The input voltage ranges (VOLT:RANGe) for the ROUTed channels within the group(s) are set. The input relays are closed for the ROUTed channels and opened for the inactive channels in the group(s). After setting/clearing all relays, an approximately 16 mS delay is enabled to allow the relays to settle.
2. If ARM:ZERO has been enabled for the group(s) being INITiated, the memory is zeroed.
3. The internal registers are loaded (SWEep:POINts, TRIGger options, ARM options).
4. The applicable channels are ROUTed.
5. The external trigger input slope, external arm slope, and overrun bit setups are programmed (TRIGger:SLOPe, ARM:SOURce, FORMat:OVERrun).

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6. The Measurement Complete Status bits in the *ESR register are cleared for the group(s) being initiated.
7. Data acquisition is enabled. If applicable, the external arm input is enabled.
8. If a INITiate:DELAy has been programmed, the delay time is executed.
9. The triggers are armed.
10. A software trigger is executed.

Examples

Command	Response
INITIATE:IMMEDIATE (all)	N/A, initiate all channel groups.
INIT(@1:4)	N/A, initiate all channel groups.
INIT:DELAY 16e–3 (@2,4)	N/A, initiate groups 2 and 4 with a 16 ms data acquisition to trigger arm delay.
INIT:CONT (@4)	N/A, initiate group 4 in the continuous acquisition mode.

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OUTPut

Command Syntax

```
OUTPut
    :GROUp [<1..4>]
    :TRIGger
        :SLOPe POSitive | NEGative
        :TTLTrg <0..7> | 8 (off)
        :LOGIc AND | OR
        :MASK <hex16 value>
        :LOAD
```

Query Syntax

```
OUTPut
    :GROUp?
    :TRIGger
        :SLOPe?
        :TTLTrg?
        :LOGIc?
        :MASK?
```

Query Responses

:GROUp	1 through 4 (group number)
:SLOPe	POS | NEG
:TTLTrg	0 through 7 | 8 (off)
:LOGIc	AND | OR
:MASK	<hex16 value>

***RST Value**

:GROUp	1
:SLOPe	POSitive
:TTLTrg	OFF
:LOGIc	OR
:MASK	0

Limits

:GROUp	1 to 4

Related Commands TRIGger

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Description

The OUTPut command controls various output functions of the module.

The OUTPut:GROUp command controls which group's TRIGGER and sample CLOCK outputs are routed to the front panel interface. It is executed immediately upon processing of the command. The trigger and clock outputs are positive EDGE true.

The OUTPut:TRIGger commands control the master trigger output of the module. The master trigger can be programmed to be the logical AND or OR of any of the four group triggers by using the OUTPut:TRIGger:LOGIc and OUTPut:TRIGger:MASK commands. The MASK value is an ASCII hex encoded value (0 to F), with the bit positions as defined below (only the four LSBs are significant; any additional bits are ignored):

Bit	Trigger Group
0	1
1	2
2	3
3	4

For example, "OUTP:TRIG:MASK 000A" (0000 0000 0000 1010 hex) defines trigger groups two and four. The master trigger can also be programmed to strobe any one of the eight VXI TTL trigger lines. If enabled (OUTP:TRIG:TTLT x), the VXI trigger line will be strobed with an approximately 21 µs low pulse when the master trigger becomes active. Specifying a TTLTrg value of 8 disables strobing of the VXI TTL triggers. Like the group triggers (TRIGger command), as each trigger condition occurs, it is latched by the module. When all conditions have been satisfied, the master trigger is activated.

However, unlike the group triggers, the master trigger conditions are cleared and re-enabled after a master trigger is output. This allows multiple strobes to be generated on the TTL trigger line. For example, if the logical OR of all four channel groups were programmed, as each channel group triggers, it would cause a strobe on the TTL trigger line.

The SLOPe option defines the active edge of the front panel interface master trigger output. It is executed immediately on receipt of the command. Like the VXI master output trigger, the front panel master trigger out is an approximately 21 µs pulse. For a positive slope, the output is nominally low, and pulses high. For a negative slope, the output is nominally high and pulses low.

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NOTE. *Normally the output trigger slope should be programmed prior to loading the master trigger. This is to prevent inadvertent triggering caused by changing the nominal output level of the signal.*

NOTE. *The OUTPut:TRIGger:LOAD command loads the defined logic, mask, and TTLTRG conditions. It MUST be issued when defining or re-defining any of these three conditions to enable them.*

Examples

Command	Response
OUTPUT:GROUP 2	N/A; set multiplexed output to group 2.
outp:grou?	2<LF>
output:trigger:slope negative	N/A; set master trigger output to negative edge true.
outp:trig:slo?	NEG<LF>
outp:trig:ttlt?	8<LF>
outp:trig:ttlt 5	N/A; enable VXI TTL trigger 5 to be strobed.
outp:trig:ttlt?	5<LF>
output:trig:mask 8	N/A; strobe master trigger when group 4's trigger goes active.
outp:trig:mask?	0008<LF>
output:trig:load	N/A; load the master trigger conditions.

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ROSCillator

Command Syntax

```
[SENSe:]
   ROSCillator
      :SOURce INTernal | CLK10
      :FREQuency <frequency>
```

Query Syntax

```
[SENSe:]
   ROSCillator
      :SOURce?
      :FREQuency?
```

Query Response(s)

:SOURce INT | CLK10

:FREQuency +x.xxxxxxxE+xx (frequency value)

***RST Value**

:SOURce Internal

:FREQuency 2.0 MHz

Limits

Source	Frequency	Maximum Frequency Out	Minimum Frequency Out
Internal	4.0E6	2.0E6	30.6372 Hz
Clk10	10.0E6	5.0E6	76.5931 Hz

Related Commands

FREQ:SYNChronize
FREQ:TINTinterval
FETCh:TIMEtag

Description

The VX4244 Module uses a two-stage clock scheme. The first stage is the reference (master) clock. The master clock output is the source clock frequency divided by 2 to 130560 (in increments of 2). This clock is fed to each of the four channel groups, which employ an additional divider to generate the actual sampling clock for that group (FREQ:TINTerval / FREQ:RANGe commands). For each channel group, the master clock can be divided from 1 to 65280.

The source of the master clock can be programmed to be either the internal (on-board) clock source (ROSC:SOURce INTernal), or the VXI 10 MHz ECL clock input (ROSC:SOURce CLK10). Depending on the clock's source, the frequency of the master clock can be programmed to be between 30.6372 Hz to 5 MHz. Programmed frequencies are rounded up to the nearest divisible integer

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value. Changing the source automatically resets the frequency to the maximum value.

The query response to the ROSC:FREQ? command returns the actual frequency value programmed. The master clock is loaded immediately upon processing the command, except as noted below, or on the activation of a SYNC signal.

If <frequency> is not specified, an error is generated.

NOTE. *Issuing a ROSCillator command automatically resets the group frequencies. If the reference oscillator is greater than 400 kHz, the group frequencies are set to 200 kHz. Otherwise, the group frequencies are set to (ROSCillator frequency) / 2.*

NOTE. *If ANY channel group is active, the reference clock cannot be re-programmed because ambiguous results can occur. An error will be generated if this is attempted.*

NOTE. *The reference oscillator generally does not need to be programmed for most applications. The exception is when group sampling frequencies below (reference oscillator frequency / 130560) are required.*

Examples

Command	Response
SENSE:ROSCILLATOR :FREQUENCY 500E3	N/A; set the reference clock to 500 kHz.
rosc:freq 200	N/A; set the reference clock to 200 Hz.
rosc:source?	INT<LF>
rosc:sour clk10	N/A; set the reference clock source to VXI CLK10.
rosc:sour?	CLK10<LF>
rosc:freq?	+2.0000000E+06<LF>

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ROUTe

Command Syntax

```
ROUTe
   :OPEN  [<channel list>]
   :CLOSe [<channel list>]
```

Query Syntax

```
ROUTe
   :OPEN?  [<channel list>]
   :CLOSe? [<channel list>]
   :STATe?
```

Query Response(s)

:OPEN	listing of channel states (1 = open, 0 = closed)
:CLOSe	listing of channel states (1 = closed, 0 = open)
:STATe	listing of all the closed channel numbers

***RST Value**

Channel 1 routed only.

Limits

N/A

Related Commands

VXI:FDC
SWEep:POINts
FETCh

Description

The ROUTe command defines the active channels within a channel group. Each channel group can have one, two, or four channels active within its group. For one channel, any of the four input channels can be selected as the active channel. For two channels, any two of the input channels can be selected as the active channels.

Sweep memory and FDC size (if applicable) are automatically reallocated to the maximum available PER channel, whenever the ROUTe command is issued (SWEep:POINts, VXI:FDC:... <size>). If a single channel is enabled, 262144 samples of memory are available to the channel. For two channels, 131072 samples of memory are available for each channel. For four channels, 65536 samples of memory are available per channel. The FDC address(es) are also set to 0 (the trigger address).

The ROUTe:CLOSe command enables the specified channels. The ROUTe:OPEN command disables the specified channel. Once a channel is enabled, it remains enabled unless specifically closed, or upon reset of the module.

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The ROUTe command keeps track of two states of the module. The first state is the currently active state, and is indicated by the ROUTe:STATe response. The second state is the next state to be configured when the module is INITiated. The active channels for the next state are indicated by the OPEN and CLOSe responses.

If [<channel list>] is not specified, it defaults to channel 1.

NOTE. *Because the ROUTe command automatically reallocates memory, it should be issued prior to the SWEep:POINts and/or FDC...<size> commands. The record length and FDC size are set to the available memory/channel.*

Examples

Command	Response
ROUTE:CLOSE(@1:4,16)	N/A; close channels 1 through 4, and 16.
route:state?	01,02,03,04,16<LF>
rout:close?(@1:16)	1,1,1,1,0,0,0,0,0,0,0,0,0,0,1<LF>
rout:open? (all)	0,0,0,0,1,1,1,1,1,1,1,1,1,1,0<LF>
rout:close?(@16:13)	1,0,0,0<LF>

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SWEep:POINts

Command Syntax

```
[SENSe:]
   SWEep
      :POINts <record length> [<group list>]
```

Query Syntax

```
[SENSe:]
   SWEep
      :POINts? [<group list>]
```

Query Response(s) xxxxxxx (number of points)

***RST Value** <record length> 262144

Limits <record length> 12 to the maximum amount of memory available per channel

Active Channels Group	Memory Available
4	65536
2	131072
1	262144

Related Commands
ROUTe
INITiate

Description The SWEep:POINts command defines the number of samples to collect *after* the trigger event occurs. Varying this count allows the data collected to be pre-, post- or center-triggered. For example, with four channels active, specifying a record length of 32768 causes 32768 samples to be collected before the trigger, and 32768 samples collected after the trigger, thus 'centering' the trigger event in memory. Similarly, a length of 100 causes (65536 – 100) samples to be collected prior to the trigger, and 100 samples collected after the trigger.

***NOTE**. If the trigger is active immediately upon arming the card, no pre-trigger data would be collected. To ensure pre-trigger data, the DELAY option of the initiate command can be used to control the number of samples acquired prior to arming the trigger.*

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The amount of memory available to an individual channel is based on the number of channels active within that channel's group. This is controlled by the ROUTe command. Issuing the ROUTe command automatically reallocates the maximum amount of memory available to each channel, and sets the record length to this value. Therefore, the ROUTe command should be issued prior to defining the record length.

If all four channels in a group are active, the record length can be set to a resolution of 1. If two channels are active, the record length can be set to a resolution of 2 (rounded up if odd). For example, setting a length of either 13 or 14 causes 14 samples to be collected on each channel. For a single channel, the resolution is 4 (rounded up). Similarly, setting a record length of 13, 14, 15, or 16 causes 16 samples to be collected.

If a record length is not specified, it defaults to the amount of memory available/channel. If <group list> is not specified, it defaults to group 1.

Examples

Command	Response
SENSE:SWEEP:POINTS 1234 (@2)	N/A; define 1234 samples to be collected after the trigger for group 2.
swe:poin 1000 (@1:4)	N/A; set all groups to collect 1000 samples after the trigger.
sweep:points?	0001000<LF>
sweep:points? (all)	0001000,0001000,0001000,0001000<LF>

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TRIGger

Command Syntax

```
TRIGger
   :LOGIc AND | OR [<group list>]
   :SOURce EXTernal | IMMediate | VXICmd | TTLTrg <0..7> |
     THREshold [<group list>] | GRP<1..4>
   :MASK <hex16 mask value> [<group list>]
   :SLOPe POSitive | NEGative
   :THREshold:PSLope  <level> [<channel list>]
      :NSLope  <level> [<channel list>]
      :GTLevel <level> [<channel list>]
      :LTLevel <level> [<channel list>]
      :GTAny <level> [<group list>]
      :LTAny <level> [<group list>]
```

Query Syntax

```
TRIGger:LOGIc? [<group list>]
   :SLOPe?
   :SOURce? [<group list>]
   :MASK? [<group list>]
   :THREshold?
   :OFFSet? [<group list>]
```

Query Response(s)

:LOGIc	AND | OR
:SLOPe	POS | NEG
:MASK	<hex16 value>
:THREshold	PSL@<channel> +x.xxxE+xx NSL@<channel> +x.xxxE+xx GTL@<channel> +x.xxxE+xx LTL@<channel> +x.xxxE+xx
:SOURce	a listing of all trigger conditions separated by a '&' or '|' (AND/OR) symbol.
:OFFSet?	[<integer>]

***RST Value**

:LOGIc	OR
:SOURce	IMMediate
:SLOPe	NEGative
:MASK	0200 (hex)

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:THREshold PSLope +0.00

:OFFSet 0.

Limits

:THREshold ± the voltage range of the specified channel

Related Commands

ROUTe
INITiate
VOLTage
OUTPut:TRIGger

Description

The TRIGger commands set triggering parameters. There are 12 different trigger sources for each channel group. They are the eight VXI TTL triggers, an external trigger input, internal (software) command trigger, the VXI command trigger, and a threshold trigger. The software command trigger and VXI command trigger are mutually exclusive. That is, specifying one automatically inhibits the other. If both are specified, the VXI command trigger will be used.

The TRIGger:LOGIC command defines whether the specified triggers are to be logically ANDed or ORed to trigger the specified group.

Use the TRIGger:SOURce command to specify a single trigger condition. Use the TRIGger:MASK command to specify multiple trigger conditions. The MASK value is an ASCII hex encoded value, with the bit positions as defined below:

Bit	Trigger
0 (LSB) – 7	VXI TTL triggers 0 through 7
8	External trigger
9	Software trigger
10	Threshold trigger
11	VXI command trigger
12–15	Unused (returned as 0's)

As an example, if MASK = 0321 (hex) = 0000 0011 0010 0001, the active triggers would be the VXI TTL trigger 0, VXI TTL trigger 5, external trigger, and the software trigger.

The INITiate command arms the triggers. After initiation, each trigger condition is latched as it occurs. When all specified conditions have occurred, the group is triggered. The exception is the threshold triggers, which are not latched. That is, for a logical AND, all other defined trigger conditions must occur before the threshold condition will be recognized.

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The TRIGger:SLOPe command defines the active edge of the external trigger input.

***NOTE**. The external trigger input is global to all channel groups. If a channel group has been previously initiated with a negative slope external trigger (and has not yet triggered), then initiating a new channel group with a positive trigger slope will cause the first group's external trigger to become active.*

If a threshold trigger is specified with either the SOURce or MASK option, the type of threshold triggering must be defined with the TRIGger:THREshold options. For four-quadrant triggering, use the positive slope (PSLope) and negative slope (NSLope) options. For first quadrant triggering, a positive slope with a positive threshold causes the trigger to be active when the signal transitions positively through the level defined. Second quadrant triggering uses a negative slope with a positive threshold. This causes the trigger to be active when the signal transitions negatively through the threshold level. Similarly for the third and fourth quadrant triggers (using negative threshold levels).

Note that the signal must transition through the programmed level with the specified slope. That is, if a positive slope of 1V were programmed, and the input signal was 2V, the module would not trigger until the level dropped below one volt and then transitioned back above one volt.

If the greater than level (GTLevel) and less than level (LTLevel) options are programmed, the module will trigger when the input exceeds the specified level (GTLevel), or is less than the specified level (LTLevel).

Any one channel of a group can be used as the threshold channel. If multiple channels are defined within a group, the last defined channel in the <channel list> will be used. Note also that the channel must be enabled with the ROUTe command, and the threshold level must be within the range of the input voltage. If either of these are not true, an error will be generated when the INITiate command is executed. The TRIGger:THREshold response always returns the values for all four channel groups, regardless of whether they are enabled or active.

The actual threshold value programmed is returned in the query response of the TRIG:THR? command. The resolution is determined based on the currently programmed voltage range of the channels, and is the input range divided by 128. (For example, 20V/128 = 156.25 mV for the ±20 V input range.) If the threshold value is greater than the input voltage range, a range of ± 20 volts is assumed. The following formula is used to calculate the actual threshold value:

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$$actual\ value\ =\ round\ down\left[\frac{PV\ \div\ \left(\frac{VR}{32768}\right)}{256}\right]\times\frac{VR}{128}$$

where PV = programmed threshold value; VR = input voltage range.

For example, specifying a threshold of 6.5 volts on a ±20 volt input range, will program the threshold level as

ROUND DOWN {[(6.5 / (20/32768)] / 256} * (20 / 128.0)
= {ROUND DOWN [41.6] } * 0.15625
= 41 * 0.15625 = 6.40625 Volts

For a –6.5 volt threshold:

ROUND DOWN {[(–6.5 / (20/32768)] / 256} * (20 / 128.0)
= ROUND DOWN [–41.6] * 0.15625
= –42 * 0.15625 = –6.5625

If <group list> or <channel list> is not specified, it defaults to 1.

About the TRIGger: SOURce:GRPx Commands. The Trigger:SOURce GRPx commands allow any channel to trigger any or all of the other channel groups.

For example, if a positive slope, threshold trigger is programmed for channel two of group one, according to the following command:

```
"TRIG:SOURCE THRESHOLD (@1);TRIG:THRESHOLD:PSLOPE 0 (@2)"
```

and all other groups are programmed to trigger on group one, according to this command:

```
"TRIG:SOURCE GRP1 (@2:4)
```

Then all groups will trigger simultaneously after INITiation when channel two transitions positively through zero.

When the source channel is programmed for a threshold (or slope) trigger, the clocks controlling each group should be the same frequency, and all groups INITiated simultaneously for proper operation for the following query:

```
"TRIGger:OFFSet?"
```

For the above example, the INITiate command would be INIT (@1:4)

About the TRIGger:THREshold: Commands. The TRIGger:THREshold:GTAny and the TRIGger:THREshold:LTAny commands define the group's trigger condition to occur if *any* of the active channels in the group go outside the threshold level.

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For example, if all four channels in group one were active, the commands TRIG:SOUR THRESHOLD (@1) and TRIG:THRESHOLD:GTANY 0.75 (@1) would cause group one to trigger if any of the four channels goes greater than 0.75 V.

Similarly, the command TRIG:THRESHOLD:LTA 0.75 would cause the group to trigger if any of the four channels drops less than 0.75 V.

About the TRIGger:OFFset? Query. The TRIGger:OFFSet? query returns the actual trigger location relative to address 0. The memory architecture of the VX4244 is such that data is written into memory after every 4 A/D conversions. If four channels are active within a group, the four inputs are converted simultaneously. Therefore, after each convert pulse, the four samples are written into memory.

For a single active channel in a group, each convert pulse take two samples, one per channel. The second convert pulse takes another two samples. The four samples are then written into memory.

For two active channels in a group, each convert pulse takes one sample. After the fourth conversion, the data is written into memory.

Because of this architecture, the trigger event can only be detected as having occurred sometime prior to the writing of the data into memory. For four active channels in a group, each convert pulse generates a write cycle. Therefore, the trigger event, relative to the A/D conversions is known within one convert clock cycle (with an External Trigger Uncertainty ≤ 1 Sample clock).

For 2 active channels, two samples are taken per channel before the data is written into memory, so the trigger event could have occurred prior to either of the two conversions. This causes a trigger ambiguity of 0 or 1, meaning the actual trigger even could have occurred prior to the first conversion (address 0) or prior to the second conversion (address 1). For a single active channel, the trigger event could have occurred prior to any one of the four conversions, so the ambiguity could be anywhere from address 0 to address 3.

For all trigger conditions (except threshold triggering), additional detection and compensation is done to account for A/D pipelining, internal circuit delays, and to ensure that trigger data is not overwritten. This typically causes an additional trigger offset of two locations. For four active channels, the typical TRIG:OFFS? response is 2. For two active channels, the typical response is 2 or 3. For single active channel, the typical response range is from 2 to 5.

Threshold detection is done digitally as the data is written into memory. Because this inherently takes care of pipelining and circuit delays, the TRIG:OFFS? response is 0 for four active channels, 0 or 1 for two active channels, and 0 through 3 for a single active channel.

For common trigger sources and synchronized clocks, the four channel groups typically report the identical trigger offset.

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Examples

Command	Response
TRIGGER:LOGIC AND (@1,3)	N/A; define groups 1 and 3 as logical ANDs.
trig:logic? (all)	AND,OR,AND,OR<LF>
trig:slope?	NEG<LF>
trig:sour ext(@1)	N/A; define group 1 as external trigger.
trig:sour?(@1:4)	EXT,IMM,IMM,IMM<LF>
trig:mask?(all)	0100,0200,0200,0200<LF>
trig:mask 0101	N/A; define group 1 as VXI ttl trigger 0 and external trigger.
trig:sour?	TTL0&EXT<LF>
trig:thre?	PSL@01 +0.000,PSL@05 +0.000,PSL@09 +0.000, PSL@13 +0.000<LF>
trigger:threshold:nslope –2.2 (@2)	N/A; set channel 2 to third quadrant trigger at a level of –2.2 volts.
trig:thresh?	NSL@2 –2.200E+00,PSL@05 +0.000E+00,PSL@09 +0.000E+00, PSL@13 +0.000E+00<LF>
trigger:offset?	1<LF>
trig:offs?(@1:4)	0,1,0,3<LF>
TRIG:THRE:LTA 0.75 (@1)	N/A;trigger when any active channel in group 1 goes less than 0.75 volts.

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VERSion?

Command Syntax N/A

Query Syntax `[SYSTem:]VERSion?`

***RST Value** N/A

Limits N/A

Query Response(s) SCPI version level.

Related Commands N/A

Description The version command returns the SCPI version level.

Examples

Command	Response
system:version?	1994.0<LF>
SYST:VERS?	1994.0<LF>
vers?	1994.0<LF>

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VOLTage

Command Syntax

```
[SENSe:]
   VOLTage
      [:DC]
         :RANGe
            [:UPPer] <voltage> [<channel list>]
             :LOWer <voltage>  [<channel list>]
             :PTPeak <voltage> [<channel list>]
```

Query Syntax

```
[SENSe]
   :VOLTage
      [:DC]
         :RANGe
            [:UPPer]? [<channel list>]
             :LOWer?  [<channel list>]
             :PTPeak? [<channel list>]
```

Query Response(s) +xx.xx

***RST Value** All channels ±20 Volts

Limits

<voltage>	± 0.2, 0.5, 1.0, 2.0, 5.0, 10.0, 20.0 (+ = upper, – = lower)
<voltage>	+ 0.4, 1.0, 2.0, 4.0, 10.0, 20.0, 40.0 (peak to peak)

Related Commands TRIGger:THREshold

Description The VOLTage command sets the input voltage ranges of the channels.

All three of the voltage commands are inter-related, and are included for compatibility's sake only. That is, setting an upper range of +2 volts is the same as setting a lower range of –2 volts, or setting a peak-to-peak range of 4 volts. If a voltage value is specified other than one listed in 'Limits' above, the value is rounded to the next higher range. For example, specifying 6 volts sets the range up to 10 volts. An absolute value of <voltage> less than 0.2 or greater than 20 will cause an error to be generated for the UPPER and LOWER commands. For the PTP command, the range is 0.4 to 40.0.

If [<channel list>] is not specified, it defaults to 1.

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Examples

Command	Response
SENSE:VOLTAGE:DC: RANGE:UPPER 5 (@1:16)	N/A; set all 16 channels to ±5 volts.
volt:range?(@1)	+5.00<LF>
volt:range:lower?	–5.00<LF>
volt:range:ptp?	+10.00<LF>
volt:range:lower	–10 (@1,2) N/A; set channels 1 and 2 to ±10 volts.
volt:rang:lower? (@1:2)	–10.00,–10.00<LF>

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VXI:FDC

Command Syntax

```
VXI
   [:SERVant]
      :FDC
         :MODE
            IMMediate [<size>][,<address>] [<hwFDC list>]
            AUTOmatic [<size>][,<address>] [<hwFDC list>]
            OFF [<group list>]
         :TRANsfer FDC | WORDserial
```

Query Syntax

```
VXI
   [:SERVant]
      :FDC
         :MODE? [<group list>]
         :TRANsfer?
         :QUEUe?[group list]
```

Query Response(s)

:MODe	IMM,xxxxxxx,yyyyyyy | AUT,xxxxxxx,yyyyyyy | OFF,xxxxxxx,yyyyyyy	(x's = size, y's = address)
:TRANsfer	FDC | WORD	

***RST value** All FDC channels OFF (disabled)

Limits

<size>	262144
<address>	± <size>

Related Commands

INITiate
ROUTe
SWEep:POINts
FORMat:OVERrun

Description The Fast Data Channel commands (FDC) are used for high-speed data transfer over the VXI bus. There are four hardware supported FDC channels for each of the four channel groups. FDC channel 0 corresponds to group 1, FDC channel 1 to group 2, FDC channel 2 to group 3, and FDC channel 3 to group 4. FDC channel 4 is a software supported FDC channel which can be used to transfer responses from the card via FDC (as opposed to Word Serial). FDC channel 5 is

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a software supported FDC channel which can be used to send commands to the module, and is interchangeable with word serial inputs.

The <size> field specifies the size of the FDC transfer request, in samples. Since each sample is two bytes wide (16 bits), the size in bytes of the FDC transfer requested is the <size> field * 2. The sample count per channel is the <size> field divided by the number of active channels in the group. For example, for two active channels in a group, specifying an FDC transfer <size> of 2048 samples (4096 bytes) generates a transfer of 1024 samples per channel.

The <address> field specifies the A/D memory starting address to transfer the data from (address 0 = trigger address). The <address> field has a resolution of 4 if a single channel in a group is active, a resolution of 2 for two active channels/group, and a resolution of 1 for four active channels/group. Addresses are rounded down to the nearest resolved value. For example, for two channels active in group 3, specifying VXI:FDC:MODE IMM 100,7 (@3) will generate a request of <size> 100 (50 samples/channel), with the data beginning at address 6 (rounded down to the nearest by-2 value).

The VXI:FDC:MODE IMMediate command generates an FDC transfer request of the <size> specified, beginning at the A/D memory <address> specified, for the group(s) specified. If VXI:FDC:MODE AUTO is active, then the VXI:FDC:MODE IMMediate command is inhibited, and will generate an error if received. For the IMMediate mode only, the query response to the VXI:FDC:MODE command will return an IMMediate while the transfer is pending or not complete. Otherwise, it returns an OFF response.

The VXI:FDC:MODE AUTOmatic command is the same as the IMMediate command, except it generates an FDC request when Measurement Complete goes active (after INITiate). For example, the following table shows a command sequence to collect one full buffer's worth of data, and generate an FDC transfer request of <size> 262144 (524288 bytes), beginning 100 locations before the trigger, and ending 262044 locations after the trigger:

Command Sequence	Comments
`ROUTe:CLOSe (@1)`	Enable channel 1 only.
`SWEEp:POINts 262044`	Set number of samples to collect after triggering.
`VXI:FDC:MODE AUTO 262144,-100 (@1)`	Set up the FDC transfer.
`INITiate (@1)`	Trigger the card.

When simultaneously collecting and transferring data continuously (INIT:CONT), the VXI:FDC:MODE AUTO setup generates a request each time the specified amount of data has been acquired after the group(s) has been triggered. The data must be off-loaded from the card to free memory for

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additional acquisitions. If it isn't, data acquisition is inhibited until an FDC buffer is freed. If the FORMat:OVERrun is enabled, the LSB will be set to 1 for the four samples prior to the point where overrun began to occur, otherwise the LSB is set to 0. The <address> in the continuous mode is automatically set to the trigger address for the first FDC transfer request, and is automatically incremented to the next block location for subsequent requests.

The <size> values for the VXI:FDC:MODE AUTO command will round to the closest, higher value of FDC size listed below:

2048	4096	8192	16384
32768	65536	131072	262144

The VXI:FDC:MODE OFF command turns off the FDC transfer modes (IMMediate and AUTOmatic) for the group(s) specified.

The VXI:FDC:MODE? query returns the current FDC transfer state as either OFF, IMMediate or AUTOmatic with the size and address values, for the group(s) specified.

The VXI:FDC:TRANsfer command allows responses to be received either via FDC (VXI:FDC:TRAN FDC), or via VXI word serial (VXI:FDC:TRAN WORDserial). Data is re-directed immediately to the output source. For example,

```
VXI:FDC:TRAN FDC;ERROR?
```

causes the error response to be sent to FDC channel 4.

The VXI:FDC:QUEUe? query returns the current number of FDC buffers queued up for the group(s) specified.

If <size> is not specified, it defaults to 16384. If <address> is not specified, it defaults to 0 (trigger address). If <hwFDC list> is not specified, it defaults to 1.

NOTE. *The ROUTe command automatically reallocates the <size> of an FDC buffer to the maximum available, and loads the <address> to 0. It therefore should be issued PRIOR to defining the VXI:FDC:MODE groups.*

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Examples

Command	Response
VXI:FDC:MODE IMMEDIATE 1000,0 (@1)	N/A, generates an FDC channel 0 request to transfer 1000 samples (2000 bytes), beginning at address 0.
vxi:fdc:mode auto 16384 (@1:4)	N/A, enable all channel groups to request an FDC transfer of 16384 samples when the measurement is complete.
VXI:FDC:MODE OFF (@1)	N/A, disable FDC for group 1 (FDC channel 0).
vxi:fdc:mode?(@2)	AUT,0016384,0000000<LF>
VXI:FDC:TRANsfer FDC	N/A, enable all responses from the card to be transferred via FDC channel 4.
vxi:fdc:tran?	FDC<LF>
VXI:FDC:QUEUe? (@1:4)	016,000,000,000<LF>

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IEEE 488.2 Common Commands

This section lists the IEEE 488.2 common commands and queries recognized by the VX4244.

*CAL?

Calibration Query. For the calibration query, the state of the calibration routine is returned, as defined in the responses below.

Query Response(s)

–1<LF>	Calibration failed
0<LF>	Calibration successful
1<LF>	Calibration in progress

*CLS

Clear Status. This commands clears the following:

Event Status Register (ESR)
Clears any pending Service Requests (SRQs)
Clears the error queue
Clears the Status Byte register (STB)
Clears the Serial Poll Response bits to the Request True interrupt (SRE)

*ESE <mask>

Event Status Enable (ESE) command. This command defines the mask for setting the Event Status Summary bit (bit 5) in the Status Byte register (*STB?). The mask is logically AND'ed with the Event Status register (*ESR?) to determine whether or not to set the Event Status Summary bit. The mask can be any numeric value from 0 to 255, corresponding to the encoded bits of the ESR register. A '1' in a bit position enables reporting of the function. A '0' disables it. The *ESE register is cleared at power-on, or by writing an *ESE 0 command only. If <mask> is not specified, it defaults to 0. Bits 1 and 6 are unused, and are always interpreted as zero.

For example, the command *ESE 37 (hex 25, binary 00010101) enables setting the Event Status Summary bit whenever an operation is complete, a query error is detected, or an execution error is detected.

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*ESE?

Event Status Enable (ESE) query. This command returns the value of the Event Status Enable register as a numeric value from 0 to 255. For example, a value of 32 (hex 40, binary 0010000) indicates that command error reporting is enabled. Bits 1 and 6 are always returned as zeroes.

*ESR?

Event Status Register (ESR) query. This command returns the value of the Event Status Register. The *ESR command is destructively read (that is, read and cleared). The Event Status Summary bit in the Status Byte (*STB?) is also cleared by a read of the ESR. The ESR is set to 128 on power-on (bit 7) set. It is cleared by an *ESR? or *CLS command only. When converted to a binary number, the bits of the ESR correspond to:

bit	0 (LSB)	Operation Complete
	1	Request Control
	2	Query error
	3	Device Dependent error
	4	Execution error
	5	Command error
	6	User Request
	7 (MSB)	Power On

The Error bits are set whenever the module detects an error. The error values from –100 to –199 are Command errors. Error values from –200 to –299 are Execution errors. Error values from –300 to –399 are Device Dependent errors. Error values from –400 to –499 are Query errors.

The Request Control and User Request bits are unused, and are always reported as zeroes.

The Operation Complete bit is set in response to an *OPC command. A 1 indicates that the module has completed all pending commands and queries.

*IDN?

Identification query; This returns a 4-field response. Field 1 is the manufacturer, field 2 the model, field 3 the serial number, and field 4 contains both the SCPI and the firmware version levels. The response syntax is:

```
TEKTRONIX,VX4244,XX0000001,SCPI:94.0 FV1.0<LF>
```


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*OPC

Operation Complete. This command causes the module to set the Operation Complete bit in the Event Status register (ESR) when all pending commands and queries are complete.

*OPC?

Operation Complete query. This command causes the module to place a “1” in the output queue when all pending commands and queries are complete. All commands following *OPC are suspended until the pending operations are complete. The *OPC? command does not affect the OPC bit in the Event Status register.

*RST

Reset. This command resets the module to its power-on state. The default condition of the VX4244 Module after the completion of power-on self test or on receipt of an *RST command is as follows:

External Arm Slope	positive
Arm Source	immediate
Arm Zeroing	off
Overrun Enable	off
Display Group	1
Group Sampling Frequencies	200 kHz
Group Clock Source	internal
External Clock Slope	positive
Timetag Clock Source	10 MHz VXI CLK10
Output Group (Trigger/Clock)	1
Output Trigger Slope	positive
VXI Master Trigger Out	off
Reference Oscillator Source	internal
Reference Oscillator Frequency	2 MHz
Active (routed) Channels	1 only
Sweep Record Length	262144
External Synchronization Level	negative
VXI TTLTRG Synchronization	off
Group Triggering Logic	OR
Group Trigger Source	internal
External Trigger In Slope	negative
Voltage Range	±20 V, all channels
Fast Data Channels	disabled
Error Queue	cleared (*RST only)
Input Relays	all open

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*SRE <mask>

Service Request Enable (SRE) register. This command defines the mask for generating VXI Request True interrupts. The mask can be any number from 0 to 255, corresponding to the encoded bits defined below. Bits 4, 6, and 7 are unused, and are ignored if received. A ‘1’ in a bit position enables the corresponding service request. A ‘0’ disables it. The *SRE register is cleared at power-on, or by writing an *SRE 0 command only. If <mask> is not specified, it defaults to 0. When converted to a binary number, the bits of the *SRE correspond to:

bit	0 (LSB)	Measurement Complete (group 1) / FDC0
	1	Measurement Complete (group 2) / FDC1
	2	Measurement Complete (group 3) / FDC2
	3	Measurement Complete (group 4) / FDC3
	4	———————
	5	Event Status Summary
	6	———————
	7 (MSB)	———————

To generate the Event Status Summary interrupt, the event must be enabled with the *ESE command.

*SRE?

Service Request Enable (SRE) query. This command returns the value of the Service Request Enable register as a numeric value from 0 to 255. Bits 4, 6, and 7 are unused, and are reported as zeroes.

*STB?

Status Byte (SB) query. This command returns the value of the Status Byte register as a numeric value from 0 to 255. The Status byte is also the value returned by a VXI READ STB command (with bit 6 set to 0). The Status byte is encoded as follows:

bit	0 (LSB)	Measurement Complete (group 1) / FDC0 state
	1	Measurement Complete (group 2) / FDC1 state
	2	Measurement Complete (group 3) / FDC2 state
	3	Measurement Complete (group 4) / FDC3 state
	4	———————
	5	Event Status Summary bit
	6	Service Request Pending Summary bit
	7 (MSB)	———————

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For bits 0 through 3, a ‘1’ indicates that a measurement acquisition has been completed, or that a Fast Data Channel (FDC) request is active.

Bit 4 is unused, and is always returned as a 0.

For bit 5, a ‘1’ indicates an event status condition is active. This bit reflects the logical AND of the Event Status Enable register and the current Event Status register. If any bits are set after the ANDing, then the Event Status Summary bit is set.

For bit 6, a ‘1’ indicates a VXI Request True interrupt has been generated. Like bit 5, it reflects the logical AND of the Service Request Enable register, and the currently active service request conditions. If any bits are set after the ANDing, then the Service Request Pending Summary bit is set. This bit is destructively read. That is, it is cleared when the *STB? command is executed.

*TST

Execute the self test. The Error LED will blink while the self test is being executed. The self test takes approximately 30 seconds to complete. After executing the *TST command, the module is returned to its *RST state with the exception that self test errors (if any) will be queued.

The Operation Complete bit of *ESR?, or the *TST? query, or the *SRE interrupt can be used to determine when the test has been completed. The *TST? query gives a summary of the results. The *ERRor? command gives the failure results (if any). See *Appendix C* for a listing of self test failures.

The following commands are allowed during *TST execution (all others are ignored):

*CAL?	*ESE?	*ESR?	*IDN?
*STB?	*SRE?	*TST?	*WAI
*OPC	*OPC?		

*TST?

Self Test query. For the self test query, the state of the self test routine is returned, as defined in the responses below.

Query Response(s)

–1<LF>	self test failed
0<LF>	self test successful
1<LF>	self test in progress

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*WAI

Wait to Continue. This command causes the module to wait until all pending commands and queries are complete. All commands following *WAI are suspended until the pending operations are complete.

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Appendix A: Specifications

This appendix contains the VX4244 specifications. All specifications are warranted unless they are designated *typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Table A–1: Specifications

Characteristic	Description			
Number of Inputs[1]	16			
Input Voltage Ranges[1]	± 0.2, ± 0.5, ± 1.0, ± 2.0, ± 5.0, ± 10.0, ± 20.0 Volts			
Reference Oscillator (Master Clock)[2]				
Source[2]	Internal (4 MHz) VXI 10 MHz ECL clock			
Frequency[2]	Source frequency / (2 to 130560) (in division increments of 2)			
Range	**Source**	**Frequency**	**Max Freq out**	**Min Freq out**
	Internal	4.0E6	2.0E6	30.6372 Hz
	Clk10	10.0E6	5.0E6	76.5931 Hz
Stability (Internal Clock)	0.01% (100 ppm)			
Sample Clock[3]				
Source[3]	Master Clock External Clock			
Frequency[3]	Master Clock / (1 to 65280) External – DC to 200 kHz maximum			
Signal Input	Type	Differential		
	Bandwidth	DC to 300 kHz (–3 dB typical)		
	Roll-off	–6 dB/octave (at 300 kHz typical) –12 dB/octave (at 500 kHz typical)		
	Coupling	DC, ground		
	Impedance	99.8 kΩ ±0.5%, each input side		
	Common Mode	±24 V maximum		
	Common Mode Rejection Ratio (CMRR)	>68 dB at 100 Hz		
	Protection	±80 V max (DC + peak AC)		
Resolution (for 16 bits)	**Range**	**Resolution**		
	±0.2	6.1037 µV/bit		
	±0.5	15.259 µV/bit		
	±1.0	30.519 µV/bit		
	±2.0	61.037 µV/bit		

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Table A–1: Specifications (Cont.)

Characteristic	Description			
	±5.0	152.59 µV/bit		
	±10.0	305.19 µV/bit		
	±20.0	610.37 µV/bit		
DC Accuracy Error (using average function)	<0.2% full scale			
Effective Bits (AC accuracy)	Dynamic accuracy based on least squares fit to idealized 16-bit sine wave, and the formula Effective Bits = 16 –[log2(RMS error actual / RMS error ideal)] (parenthetical values are typical)			
	Range	**1 kHz**	**10 kHz**	**20 kHz**
	0.2	>9.0 (10.5)	>9.0 (10.5)	>9.0 (10.5)
	0.5	>10.2 (11.6)	>10.2 (11.6)	>10.2 (11.4)
	1.0	>11.1 (12.4)	>11.1(12.3)	>10.9 (11.9)
	2.0	>11.9 (12.6)	>11.6 (12.4)	>11.2 (12.0)
	5.0	>12.3 (13.0)	>12.0 (12.8)	>11.2 (12.1)
	10.0	>12.6 (13.2)	>12.1 (12.9)	>11.2 (12.2)
	20.0	>12.6 (13.2)	>12.1 (12.9)	>11.2 (12.2)
Sample Memory (per channel group)				
Depth	256 Kwords (262144) (16-bit) for a single channel / group 128 Kwords (131072) for two active channels / group 64 Kwords (65536) for four active channels / group			
Control[3]	Pre-/post-triggering from 1 to the total amount of available memory per channel, or FREE running. Memory can be optionally programmed to be zeroed prior to arming the trigger.			
Group Triggering[3]	Any AND or OR combination of the following (the automatic and VXI command triggers are mutually exclusive): ± External Trigger In (active edge programmable) Threshold trigger (8-bits accuracy) Automatic (on command) VXI TTL trigger (1 of 8 programmable) VXI Command trigger			
Master Trigger[2]	Any AND or OR of the four group triggers. Programmable to drive any one of the eight VXI TTL triggers.			
External Trigger Uncertainty	≤1 Sample clock			
Trigger Rearm Time	ARM:ZERO 1 (ON) approximately 2 s per group ARM:ZERO 0 (OFF) approximately 100 ms per group			
Voltage Threshold[3]				
Range	± 100% Full Scale			
Resolution	8 Bits			

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Table A–1: Specifications (Cont.)

Characteristic	Description
Synchronization	The Logical OR of any the following: Internal (on command) External any one of VXI TTL triggers 1 – 7.
Time Tag	
Source[2]	VXI 10 MHz clock Master Clock
Range	32 bits (2^32 = 4,294,967,296 counts)
Resolution	1 / (frequency of the source) seconds
Error Queue	20 messages deep
Input Queue	20 command strings deep
Overrun[2]	Programmably enabled to drive LSB high if overrun occurs. LSB = 0 if no overrun.
Digital Input/Output	All I/O TTL/CMOS compatible, one HCT load (inputs), HCT244 driver (outputs)
External CLOCK Input[2]	Programmable to either positive or negative EDGE true. Clock frequency: DC to 200 kHz Clock high or low minimum time = 40 ns.
External TRIGGER Input[2]	Programmable to either positive or negative EDGE true. 20 ns minimum pulse width.
External SYNC Input[2]	Programmable to either positive or negative LEVEL true. 20 ns minimum pulse width.
External ARM Input	Programmable to either positive or negative EDGE true. 20 ns minimum pulse width.
MASTER TRIGGER OUT[2]	Programmable to either positive or negative LEVEL true.
MASTER CLOCK OUT	Positive EDGE true. 50% ± 5% duty cycle.
SYNC OUT	Active LEVEL low true.
Group TRIGGERED OUT[2]	Programmable to either positive or negative LEVEL true.
Group CLOCK out	Programmable to either positive or negative LEVEL true. 50% ± 5% duty cycle.
	NOTE. *The source of the group clock and triggered output signals can be programmed to be any one of the four channel groups.*
DSP Interface Signals	(See Figure A–1 at the end of this section for timing information). Serial Outputs: See Figure A–1. 8 MHz Clock Outputs: 50% ± 5% duty cycle. A/D Sync Outputs: See Figure A–1.
VXI Data Transfer	
Word Serial	ASCII Two's complement binary

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Table A–1: Specifications (Cont.)

Characteristic	Description				
Fast Data Channel (FDC)	FDC transfers are done using a type of Direct Memory Access for maximum transfer speeds. Data transfers can be either 16 or 32 bit two's complement binary. Depending on the number of active channels in a group, the data is transferred as follows (A2 refers to the VME address line A2).				
FDC Byte/Word/Long Word Alignment	16-bit Transfers (1 active channel)				
	Transfer	**VME A2**	**D15 – D8**	**D7 – D0**	
	1	0	CH1 WORD 1 LO	CH1 WORD 1 HI	
	2	1	CH1 WORD 2 LO	CH1 WORD 2 HI	
	3	0	CH1 WORD 3 LO	CH1 WORD 3 HI	
	4	1	CH1 WORD 4 LO	CH1 WORD 4 HI	
	16-bit Transfers (2 active channels)				
	Transfer	**VME A2**	**D15 – D8**	**D7 – D0**	
	1	0	CH1 WORD 1 LO	CH1 WORD 1 HI	
	2	1	CH2 WORD 1 LO	CH2 WORD 1 HI	
	3	0	CH1 WORD 2 LO	CH1 WORD 2 HI	
	4	1	CH2 WORD 2 LO	CH2 WORD 2 HI	
	16-bit Transfers (4 active channels)				
	Transfer	**VME A2**	**D15 – D8**	**D7 – D0**	
	1	0	CH1 WORD 1 LO	CH1 WORD 1 HI	
	2	1	CH2 WORD 1 LO	CH2 WORD 1 HI	
	3	0	CH3 WORD 1 LO	CH3 WORD 1 HI	
	4	1	CH4 WORD 3 LO	CH4 WORD 3 HI	
	32-bit Transfers (1 active channel)				
	Transfer	**D31 – D24**	**D23 – D16**	**D15 – D8**	**D7 – D0**
	1	CH1 WORD 1 LO	CH1 WORD 1 HI	CH1 WORD 2 LO	CH1 WORD 2 HI
	2	CH1 WORD 3 LO	CH1 WORD 3 HI	CH1 WORD 4 LO	CH1 WORD 4 HI
	32-bit Transfers (2 active channel)				
	Transfer	**D31 – D24**	**D23 – D16**	**D15 – D8**	**D7 – D0**
	1	CH1 WORD 1 LO	CH1 WORD 1 HI	CH2 WORD 1 LO	CH2 WORD 1 HI
	2	CH1 WORD 2 LO	CH1 WORD 2 HI	CH2 WORD 2 LO	CH2 WORD 2 HI
	32-bit Transfers (4 active channel)				
	Transfer	**D31 – D24**	**D23 – D16**	**D15 – D8**	**D7 – D0**
	1	CH1 WORD 1 LO	CH1 WORD 1 HI	CH2 WORD 1 LO	CH2 WORD 1 HI
	2	CH3 WORD 1 LO	CH3 WORD 1 HI	CH4 WORD 1 LO	CH4 WORD 1 HI

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Table A–1: Specifications (Cont.)

Characteristic	Description	
CPU	Motorola 68330 16-bit processor. 128 Kwords RAM. 256 Kwords FLASH memory. 64 Kwords EEPROM.	
VXI Transfer Rate, FDC	Data Strobe (DS*) low to Data Transfer Acknowledge (DTACK*) high 900 ns	
IEEE 488.2 Commands	*CAL?	Calibration query
	*CLS	Clear Status command
	*ESE	Standard Event Status Enable command
	*ESE?	Standard Event Status Enable query
	*ESR?	Standard Event Status Register query
	*IDN?	Identification query
	*OPC	Operation Complete command
	*OPC?	Operation Complete query
	*RST	Reset command
	*SRE	Service Request Enable command
	*SRE?	Service Request Enable query
	*STB?	Read Status Byte query
	*TST	Self test command
	*TST?	Self test query
	*WAI	Wait to Continue
VXIbus Compatibility	Fully compatible with the VXIbus Specification V1.4 for message-based instruments.	
VXI Device Type	VXI message based instrument.	
VXI Protocol	Word serial or Fast Data Channel Version 2.07.	
Dynamic Configuration	Yes (set Logical Address switch to FFh).	
VXI Card Size	C size, one slot wide.	
Module-Specific Commands	All module-specific commands and data are sent via the VXIbus Byte Available command or via Fast Data Channels 4 and 5. All module-specific commands are made up of ASCII characters. Module specific data may be either ASCII or binary.	
VMEbus Interface	Data transfer bus (DTB) slave – A16, D16 Fast Data Channel A32 D16/D32 (FDC).	
Interrupt Level	Dynamically configured by the Resource Manager.	
Interrupt Acknowledge	D16; lower 8 bits returned are the logical address of the module.	

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Table A–1: Specifications (Cont.)

Characteristic	Description	
VXIbus Commands Supported	All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command error: ABORT NORMAL OPERATION ASSIGN INTERRUPT LINE ASYNCHRONOUS MODE CONTROL BEGIN NORMAL OPERATION BYTE AVAILABLE (with or without END bit set) BYTE REQUEST CLEAR CLEAR LOCK CONTROL EVENT END NORMAL OPERATION ERROR QUERY READ INTERRUPT LINE READ INTERRUPTER READ PROTOCOL READ STATUS SET LOCK TRIGGER	
VXIbus ProtocolEvents Supported	VXIbus events are returned via VME interrupts. The following event is supported and returned to the module's commander: REQUEST TRUE (In IEEE-488 systems, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)	
VXIbus Registers	ID Device Type Status Control Protocol Response Data Low See *Register Definitions* for definition of register contents.	
Device Type Register Contents	770B	
Power Requirements	All required DC power is provided by the power supply in the VXIbus mainframe.	
Voltage	+5 V Supply	4.75 VDC to 5.25 VDC
	–5.2 V Supply	–5.0 VDC to –5.4 VDC
	–2 V Supply	–1.9 VDC to –2.1 VDC
	+12 V Supply	+11.5 VDC to +12.5 VDC
	–12 V Supply	–11.5 VDC to +12.5 VDC
	+24 V Supply	+23.5 VDC to +24.5 VDC
	–24 V Supply	–23.5 VDC to –24.5 VDC

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Table A–1: Specifications (Cont.)

Characteristic	Description	
Current (Peak Module, I_{PM})	+5 V Supply	3.1 A (fused at 5 A)
	–5.2 V Supply	30 mA (fused at 1 A)
	–2.0 V Supply	30 mA (fused at 1 A)
	+12 V Supply	320 mA (fused at 2 A)
	–12 V Supply	210 mA (fused at 2 A)
	+24 V Supply	440 mA (fused at 2 A)
	–24 V Supply	440 mA (fused at 2 A)
Fuses	Replacement fuses: Littelfuse P/N 273005 (5 A), 273002 (2 A), and 273001 (1 A).	
Cooling	Provided by the fan in the VXIbus mainframe. Less than 10° C temperature rise with 3.46 liters/sec of air at a pressure drop of 0.080 mm of H_2O.	
Temperature	–10° C to +65° C, operating (assumes ambient temperature of 55° C and airflow to assure less than 10° C temperature rise). –40° C to +85° C, storage.	
Humidity	Less than 95% R.H. non-condensing, –10° C to +30° C. Less than 75% R.H. non-condensing, +31° C to +40° C. Less than 45% R.H. non-condensing, +41° C to +55° C.	
EC Declaration of Conformity	Meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the official Journal of the European Communities: EN 55011 Class A[4]: Radiated and Conducted Emissions EN 50081–1 Emissions: EN 60555–2 Power Harmonics EN 50082–1 Immunity: IEC 801–2 Electrostatic Discharge IEC 801–3 RF Radiated IEC 801–4 Fast Transients IEC 801–5 Surge	
Module Envelope Dimensions	197 mm high, 221 mm deep, 13 mm wide. (7.75 in × 8.69 in × 0.5 in).	
Dimensions, Shipping	When ordered with a Tektronix Inc. mainframe, this module will be installed and secured in one of the instrument module slots (slots 1–12). When ordered alone, the module's shipping dimensions are: 254 mm × 254 mm × 127 mm. (10 in × 10 in × 5 in).	
Weight	1.62 kg (3.62 lbs)	
Weight, Shipping	When ordered alone, the module's shipping weight is: 2.07 kg (4.62 lbs)	
Mounting Position	Any orientation.	

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Table A–1: Specifications (Cont.)

Characteristic	Description
Mounting Location	Installs in an instrument module slot (slots 1–12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connectors	2 DD50 connectors. Refer to *Appendix B* for connector pinouts.
Software Version	See *IDN? command

1 **indicates programmability on a channel basis**

2 **indicates programmability on a module basis**

3 **indicates programmability on a group basis**

4 **To ensure compliance with the above requirement (EN55011), only high-quality shielded cables should be attached to the front-panel connectors. High-quality cables have a reliable, continuous outer shield (braid & foil) that has low impedance connections to shielded connector housings. In addition, two ferrite cores, such as Steward part number 28A2024–000 (28A2024-0A0 with clip-on case) or equivalent, should be installed on any cable attached to the Digital I/O port at the end nearest the VX4244.**

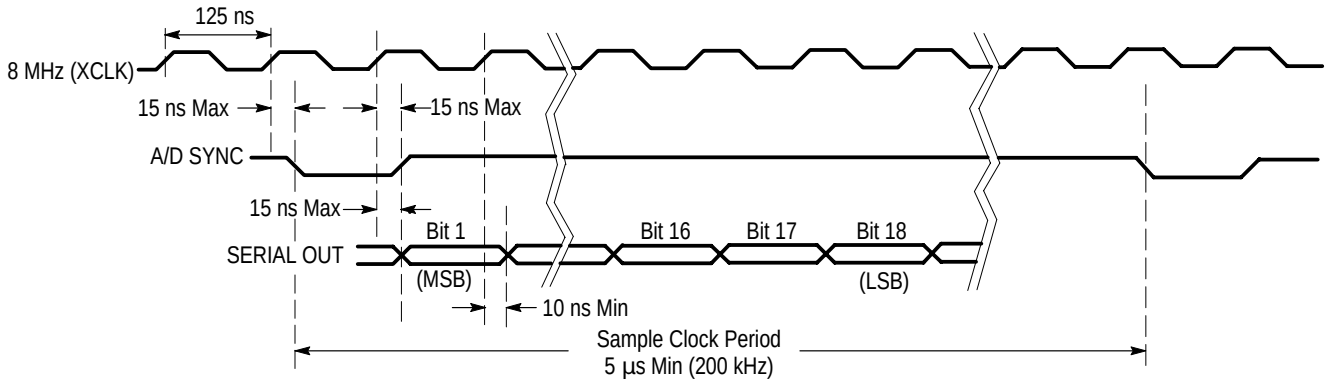


Figure A–1: VX4244 Serial Output Timing Diagram

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Appendix B: Input/Output Connections

Table B–1: Input Connections in Signal Input Connector

S1 Pin	Input Signals
1	Channel 01+
2	Ground
3	Channel 03+
4	Ground
5	Channel 05+
6	Ground
7	Channel 07+
8	Ground
9	Channel 09+
10	Ground
11	Channel 11+
12	Ground
13	Channel 13+
14	Ground
15	Channel 15+
16	Ground
17	No connection
18	Channel 01–
19	Channel 02–
20	Channel 03–
21	Channel 04–
22	Channel 05–
23	Channel 06–
24	Channel 07–
25	Channel 08–
26	Channel 09–
27	Channel 10–
28	Channel 11–
29	Channel 12–
30	Channel 13–
31	Channel 14–

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Table B–1: Input Connections in Signal Input Connector (Cont.)

S1 Pin	Input Signals
32	Channel 15–
33	Channel 16–
34	Ground
35	Channel 02+
36	Ground
37	Channel 04+
38	Ground
39	Channel 06+
40	Ground
41	Channel 08+
42	Ground
43	Channel 10+
44	Ground
45	Channel 12+
46	Ground
47	Channel 14+
48	Ground
49	Channel 16+
50	No connection

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Table B–2: Input/Output Connections on Digital I/O Connector

P1 Pin	Digital I/O
1	Serial Out Channel 1
2	Serial Out Channel 2
3	Serial Out Channel 3
4	Serial Out Channel 4
5	Serial Out Channel 5
6	Serial Out Channel 6
7	Serial Out Channel 7
8	Serial Out Channel 8
9	Serial Out Channel 9
10	Serial Out Channel 10
11	Serial Out Channel 11
12	Serial Out Channel 12
13	Serial Out Channel 13
14	Serial Out Channel 14
15	Serial Out Channel 15
16	Serial Out Channel 16
17	No connection
18	A/D Sync group 1
19	8 MHz clock
20	Ground
21	Ground
22	A/D Sync group 2
23	8 MHz clock
24	Ground
25	Ground
26	A/D Sync group 3
27	8 MHz clock
28	Ground
29	Ground
30	A/D Sync group 4
31	8 MHz clock
32	Ground
33	Ground
34	External Clock Input
35	External SYNC Input

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Table B–2: Input/Output Connections on Digital I/O Connector (Cont.)

P1 Pin	Digital I/O
36	External Trigger Input
37	Master Trigger Output
38	Ground
39	Ground
40	SYNC Output
41	Master Clock Output
42	Group Trigger Output
43	Group Clock Output
44	Ground
45	Ground
46	External Arm Input
47	No connection
48	No connection
49	No connection
50	Factory Test Serial Output (Do not connect)

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Appendix C: Self Test Failures

For the <description> fields below, x's represents a field filled in by the program. Where possible, the channel or group is identified. Also, if possible, the "U" number of the chip is identified. For some responses, the "should be" ("s/b") value is given, followed by ("–>") the actual value read. An "h" appended to a response indicates a hex value. The quotes (") are used for readability, and are not part of the response.

LCA failures are further identified by the following <description fields>:

Self Test Failure	Description
`LCA failure,No Load of Memory controllers (DONE bit inactive)`	Indicates the memory LCAs could not be loaded correctly. These are U23, U63, U1031, and U1431. The done bit is status<9> on the schematic.
`LCA failure,No Load of Trigger controller (DONE bit inactive)`	Indicates the trigger LCA (U95) could not be loaded correctly. The done bit is status<10> on the schematic.
`LCA failure,Write Counter Load Failure (group x Uxxxx) s/b 12345h -> xxxxxh?`	Indicates the write address counters could not be loaded correctly. The value should be (s/b) 12345h(ex). The last value is the actual hex value read.
`LCA failure,Read Counter Load Failure (group x Uxxxx) s/b 98765h -> xxxxxh?`	Indicates the read address counters could not be loaded correctly. The value should be (s/b) 98765h(ex). The last value is the actual hex value read.
`LCA failure,Write Counter Increment failure (group x Uxxxx) s/b xxxxxh -> xxxxxh?`	Indicates the write address counters are not incrementing correctly.
`LCA failure,Read Counter Increment failure (group x Uxxxx) s/b xxxxxh -> xxxxxh?`	Indicates the read address counters are not incrementing correctly.
`LCA failure,Read Counter Decrement failure (group x Uxxxx) s/b xxxxxh -> xxxxxh?`	Indicates the read address counters are not decrementing correctly.
Self test/Memory failures are further identified by the following <description> fields:	
`CPU RAM failure U551/U552`	Indicates the main CPU memory failed its read/write test.
`RAM error 'walking 1' (group x Uxxxx) s/b xxxxh -> xxxxh?`	Indicates the group memory identified could not be written/read correctly. A "1" is walked through each of the 16 bits of the first bank of the group's A/D 16-bit-wide memory.
`RAM error 'walking 0' (group x Uxxxx) s/b xxxxh -> xxxxh?`	Indicates the group memory identified could not be written/read correctly. A "0" is walked through each of the 16 bits of the first bank of the group's 16-bit wide memory.
`RAM error (group x U xxxx) @xxxxh s/b xxxxh -> xxxxh?`	Indicates the group memory identified could not be written/read correctly. RAM memory is loaded and verified with an incrementing value. @xxxx is the address of the RAM where the failure occurred.

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Self Test Failure	Description
`Address error on clock every read (group x Uxxxx) @xxxxh s/b xxxxh -> xxxxh?`	Indicates the address clocking control is not operating correctly. In this test, every read of the memory should cause an increment of the read address counters.
`Address error on clock every A2 even read (group x Uxxxx) s/b xxxxh/xxxxh -> xxxxh/xxxxh?`	Indicates the address clocking control is not operating correctly. In this test, the address should increment only when A2 is active. The two values represent the values of the first and third memory banks, and should be even and two counts apart.
`Address error on clock every A2 odd read (group x Uxxxx) s/b xxxxh/xxxxh -> xxxxh/xxxxh?`	Indicates the address clocking control is not operating correctly. In this test, the address should increment only when A2 is active. The two values represent the values of the second and fourth memory banks, and should be odd and two counts apart.
`Address error on clock every A1 & A2 read (group x Uxxxx) s/b xxxxh -> xxxxh?`	Indicates the address clocking control is not operating correctly. In this test, the address should increment after every A1 AND A2 read.
`Armed signal in invalid active (low) state (group x Uxxxx)`	Indicates the armed signal is active, but should not be. The U number identified is the source of the armed signal.
`Armed signal not active (high) (group x Uxxxx)`	Indicates the armed signal did not go active. The U number identified is the source of the armed signal. The module strobes a low pulse on the 'armstb' signal to arm the module.
`Triggered signal in invalid active state (group x U95)`	Indicates a trigger is active when it shouldn't be.
`Triggered signal in invalid active armed state (group x U95)`	Indicates the trigger is active while armed, but shouldn't be.
`Triggered signal not active (group x U95)`	Indicates the trigger failed to occur. The module strobes a low pulse on the 'softrg' signal to trigger the module for this test.
`Time Tag not counting (group x) xxxxxxxxh?`	Indicates the time tag counters are not operating correctly. The value returned should be greater than 1 and less than 1000 hex.
`Time Tag did not clear (group x) xxxxxxxxh?`	See above.
`Time Tag not counting (group x) xxxxxxxxh <- xxxxxxxxh?`	Indicates the time tag counters are not operating correctly. The second field should be greater than the first field.
`Time Tag counting did not stop on trigger (group x) xxxxxxxxh <- xxxxxxxxh?`	The time-tag counters should have stopped when their respective group trigger occurs. The second value should equal the first value.
`Invalid board id (U88) (reloading default calibration factors VXxxxx?`	Indicates the board id stored in EEPROM has been corrupted (or this is the first time the module has ever been turned on). The default calibration factors are automatically reloaded into EEPROM. If this message persists on power-cycles, the EEPROM needs to be replaced.
	NOTE. *The unit must be re-calibrated if this message appears.*
`Could not properly perform EEPROM write/read operation (U88)`	Indicates operation of the EEPROM is suspect.
`Threshold trigger in invalid active state (channel xx)`	Indicates the threshold triggering of the channel indicated is active, but should not be. This can be caused by either a bad analog front end, or a bad digital comparator chip.

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Self Test Failure	Description
Threshold trigger failed to occur (channel xx)	Indicates the threshold triggering of the channel indicated is not operating correctly. See above.
Single channel cross switch/threshold trigger in invalid active state (channel xx)	Indicates the trigger is in an inactive state. For this test, the cross switches are set for a single channel only.
Single channel cross switch/threshold trigger failed to occur (channel xx)	See above.
Dual channel low cross switch/ threshold trigger in invalid active state (channels xx/xx)	For this test, the cross switches are set for two input channels, with the lower of the two channels used to detect the threshold.
Dual channel low cross switch/ threshold trigger failed to occur (channels xx/xx)	See above.
Dual channel high cross switch/ threshold trigger in invalid active state (channels xx/xx)	For this test, the cross switches are set for two input channels, with the higher of the two channels used to detect the threshold.
Dual channel high cross switch/ threshold trigger failed to occur (channels xx/xx)	See above.
Armed signal still active on memory full (group x)	Indicates the 'memfull' signal failed to occur, or failed to clear the 'armed' signal.
Invalid sample count (group x) start xxxxxh end xxxxxh diff xxxxx (s/b xxx)	This test verifies that the number of samples programmed to be taken is the actual number taken. Start is the starting address, end is the ending address, and diff is the difference (in decimal). s/b is what the difference should be.
Terminal Count/Memory full not functioning (group x) count s/b 20 -> xxx	Indicates the module did not stop sampling data when it should have.

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Appendix D: Module Diagnostic Commands

The following commands are intended for diagnosing problems on the module, and should not be used for any other purpose. For the self-test subset commands, the ERRor? command can be used to read the results of the test. The Error LED blinks while processing these commands. Since the diagnostic commands modify internal registers, use the *RST command to return the module to a known state.

DIAGnostic	Command Description
:ADCOnversion	Performs the A/D conversion/threshold triggering portion of self-test.
:ARMEd	Performs the armed test portion of self-test.
:CPURam	Performs the CPU RAM portion of self-test.
:EEPRom	Performs the EEPROM portion of self-test.
:FERAm	Performs the A/D memory test and memory addressing portion of self-test.
:LCACounters	Performs the LCA counter test portion of self-test.
:TIMEtag	Performs the time-tag test portion of self-test.
:TRIGgers	Performs the trigger test portion of self-test.
:TRMCount	Performs the terminal count test portion of self-test.
:XSONe	Performs the single channel cross-switch test portion of self-test.
:XSTLow	Performs the two-channel low cross switch portion of self-test.
:XSTHigh	Performs the two-channel high cross switch portion of self-test.
:CALData? [<channel id>]	Returns the calibration factors stored in EEPROM for the channel specified. The values returned are the offset and gain DAC values for each of the seven input ranges. Example: DIAG:CALD? (@1)
:GAIN <hex12 value> [<channel list>]	Loads the hex value into the gain DAC for the channel(s) specified. 800 Hex is nominal 0 (no gain). FFF Hex is the maximum positive gain trim. 000 hex is the maximum negative gain trim. Example: DIAG:GAIN 7F0 (@1:16)
:GRPClk <hex16 value> [<group list>]	Loads the hex value into the group clock counters specified. The hex value is the two's complement divisor for the master clock. For example, the two's complement of 4 is FFFC (invert and add one). Therefore, loading an FFFC hex into the counters, causes the group clock frequency to be $\frac{1}{4}^{th}$ the master clock frequency. Example: DIAG:GRPC 89AB (@1,3)
:MSTClk <hex16 value>	Loads the hex value into the master clock counters (U762/U771). The divisor for the master clock source is calculated similarly to the DIAG:GRPClk command discussed above. Example: DIAG:MSTC 89AB

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DIAGnostic	Command Description
:OFFSet <hex16 value> [<channel list>]	Loads the hex value into the offset DAC for the channel(s) specified. The offset DAC is actually two 8-bit DAC's, with the output of the first DAC (most significant byte) fed to the input of the second DAC (least significant byte). For these DAC's, 80 Hex is zero, FF hex is positive full-scale, 00 Hex is negative full-scale. Example: DIAG:OFFS 8000 (@1:4)
:RADDress <hex 16 value> [<group list>]	Loads the A/D memory read address with the value specified for the groups specified. The multiplexed read/write address counters to the memory defaults to the write address, so the read address is valid only during a read of the memory. Example: DIAG:RADD 1234 (@1:4)
:RADDress? [<group list>]	Returns a <hex16 value> indicating the current read address of the memory for the group(s) specified.
:RAMP [<group list>]	Loads A/D RAM with a ramp waveform for the group(s) specified. Example: DIAG:RAMP (@1:4)
:RANGe <voltage> [<channel list>]	Sets the input attenuation analog switches and loads the gain and offset DAC's to the range specified for the channels specified. Example: DIAG:RANG 5 (@6,7,12:16)
:RELAy OPEN | CLOSe [<channel list>]	Opens or closes the input relays specified in channel list. Example: RELA:CLOS (@1:16)
:STRElay OPEN | CLOSe	Opens or closes the self-test relay. Example: STRE:CLOS
:WADDress <hex 16 value> [<group list>]	Loads the A/D memory write address with the value specified for the groups specified. The multiplexed read/write address counters to the memory defaults to the write address. Example: DIAG:WADD 1234 (@1:4)
:WADDress? [<group list>]	Returns a <hex16 value> indicating the current write address for the group(s) specified.
OUTPut:UART "<message>"	Outputs the message string to the front-panel serial interface. This interface is a TTL output, which can be hooked to an RS-232 driver chip to drive a monitor. The RS-232 parameters are 8 bits, one start, one stop, no parity. It is used for factory testing in conjunction with the following jumper settings: **J4 J5** OFF OFF Normal operation mode. OFF ON Debug mode. ON OFF Continuous self-test mode. ON ON Continuous self-test suppress.

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When connected to a VX3767 Development Module, and FLASH memory is programmed in the development mode, the debug mode outputs internal status messages through the development module to both the monitor and ethernet ports on the VX3767 module.

The continuous self-test and continuous self-test suppress modes put the module into continuous self-test when a TEMPCYCLE command is written to the module. The module will stay in this mode until J4 is removed from the card. The non-suppress mode outputs to the UART interface status and error information as it executes self-test. The suppress option outputs only the error messages, or a '.' heartbeat each time it executes self-test.

DIAGnostic:DEFAULT:CALIBRATION Command

***NOTE**. The DIAGnostic:DEFAULT:CALIBRATION command loads all default calibration values into the module. If executed, the module MUST be re-adjusted to meet its specifications. Executing this command generates an error message indicating the module is no longer in calibration.*

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Appendix E: Examples

This example script demonstrates how the some of the various programmable features of the VX4244 are used. It is assumed the module has completed its power-on self test.

- Query the identity of the card.

  WRITE `*IDN?<LF>`
  READ `TEKTRONIX,VX4244,0,SCPI:94.0 FV:1.0<CR><LF>`

- Query the card for any self-test errors.

  WRITE `ERROR?<LF>`
  READ `0,"NO ERROR"<LF>`

- Set group 1 and 3 to sample at 100 kHz. Note that the <CR> is considered a white space, and is ignored if received. Note also that both upper and lower case letters are allowed, and the use of either the shortened or full versions of the parameters. All responses from the card are terminated with a <LF>. Commands can be terminated with either a <LF>, an END bit, or both. Because the group frequencies are greater than their minimum values, the reference oscillator (ROSC) does not need to be modified. Otherwise, it should be programmed prior to programming the group frequencies.

  WRITE `Freq:Range 100e3 (@1,3)<CR><LF>`

- Query the current frequency ranges for all channel groups. Note that channels 2 and 4 are at their default frequencies of 200 kHz. Also, note that (all) and (@1:4) are interchangeable.

  WRITE `frequency:range? (all)<LF>`
  READ `+1.0000000E+05,+2.0000000E+05,+1.0000000E+05,`
  `+2.0000000E+05<LF>`

- Synchronize all the group clocks.

  WRITE `FREQ:SYNC:IMM<LF>`

- Define the active channels to be channel 2 only on group 1, channels 7 and 8 on group 2, all channels on group 3, and channel 16 only on group 4. Note that the ROUTe command reallocates any SWEep:POINts counts programmed, and should therefore precede those commands.

  WRITE `ROUTE:CLOSE (@2,7,8,9:12,16)<LF>`

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- Query the currently active channels.

```
WRITE       route:state?
READ        02,07,08,09,10,11,12,16<LF>
```

- Query all closed channels. Note that (all) and (@1:16) are interchangeable.

```
WRITE       route:close?(@1:16)
READ        0,1,0,0,0,0,1,1,1,1,1,1,0,0,0,1<LF>
```

- Define group 1 to collect 1000 samples after its trigger, group 2 to collect 131000 samples after its trigger, group 3 to collect 65536 samples after its trigger, and group 4 to collect 10 samples after its trigger. Note that commands can be strung together when delimited with a semi-colon (;).

```
WRITE       SWEEP:POINTS 1000 (@1);swee:poin 131000 (@2)<LF>
WRITE       sweep:points 65536(@3);sweep:points 10(@4)  <LF>
```

- Set the voltage ranges for the channels. Note that setting a voltage range for an inactive channel is allowed.

```
WRITE       sense:voltage:range:dc:upper 1 (@1:4,16)<LF>
WRITE       volt:range 2(@7,8,9)<LF>
WRITE       volt:range 5 (@10,11)<LF>
WRITE       volt:range 10(@16)<LF>
```

- Query the voltage settings of channels 16, 7, 10, and 2 in that order.

```
WRITE       volt:range? (@16,7,10,2)<LF>
READ        +10.0, +2.00, +5.00, +1.00<LF>
```

- Define the master trigger output to be the AND of group 1 and 2's trigger, and to strobe the VXI TTLTRG 5 when true. Note that the OUTPut:TRIGger:LOAD command must follow any change in the master trigger setups to latch and enable the defined conditions.

```
WRITE       OUTPut:TRIGger:LOGIc AND<LF>
WRITE       output:trig:mask 3 <LF>
WRITE       outp:trig:ttltrg 5<LF>
WRITE       output:trigger:load<LF>
```

- Define the group trigger conditions. For group 1, trigger on receipt of the INITiate command. For group 2, trigger on VXI TTLTRG 3. For group 3, trigger when channel 10 transitions positively through 2.5 volts, and for group 4, trigger when the VXI TTLTRG 3 and the external trigger have occurred.

```
WRITE       TRIGger:SOURce IMMediate (@1)<LF>
WRITE       trig:source ttltrg 3(@2)<LF>
WRITE       trig:sour threshold (@3)<LF>
```


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```
WRITE       trig:threshold:pslope 2.5(@10)<LF>
WRITE       trig:logic AND (@4)<LF>
WRITE       trig:mask 18(@4)<LF>
```

- Arm all channel groups.

```
WRITE       INITiate (all)<LF>
```

- Verify no errors.

```
WRITE       err?<LF>
READ        0,"NO ERROR"<LF>
```

- Loop until Measurement Complete on group 1. Note that an alternative method is to use the VXI Request True interrupt to notify the resource manager that the measurement is complete (*SRE command).

  while (measurement not complete)

  ```
  WRITE     *STB?<LF>
  READ      <status_byte_value>
  ```
  if (status_byte_value AND 1) then measurement_complete

  end

- Find the maximum value of channel 2.

```
WRITE       FETCh:MAXimum? (@2)<LF>
READ        +0.123456,0054321<LF>
```

- Get the data values one before the maximum value, the maximum value, and one after the maximum value.

```
WRITE       fetch:data? 3,54320<LF>
READ        +0.123000, +0.123456, -0.543210<LF>
```

- Stop the sampling on all channel groups and open all input relays.

```
WRITE       ABORt (all)<LF>
```

- Bring the board back to its power-on state.

```
WRITE       *RST<LF>
```


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Appendix F: Performance Verification

This procedure verifies the performance of the VX4244 16-Channel Digitizer Module. The verification may be performed in your current VXIbus system if it meets the requirements described in Table F–2.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

Please familiarize yourself with the following conventions which apply throughout this procedure:

- Each test sequence begins with a table, similar to the one below, providing information and requirements specific to that section. The item number after each piece of equipment refers to an entry in Table F–1, *Required Test Equipment*. Following the table, you will be given instructions for interconnecting the VX4244-under-test and for checking performance parameters. You can then record the test results in the Test Record (Table F–4).

Equipment Requirements	Digital Volt Meter (item 3) Function Generator (item 2)
Prerequisites	All prerequisites listed on page F–2

- This procedure assumes that you will be using the National Instruments PC GPIB controller and software (NI-488.2M), configured as described in Table F–3. In each test sequence you will be instructed to issue Interface Bus Interactive Control (ibic) commands to set up the VX4244-under-test system. All commands may be entered in upper or lower case. Please refer to the NI-488.2M User Manual for additional information. If you are using a different controller, simply substitute the equivalent commands.

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Prerequisites

The verification sequences in this procedure are valid when the following requirements are met:

- The VX4244 module covers are in place and the module is installed in an approved VXIbus mainframe according to the procedure in the chapter *Getting Started*
- The VX4244 has passed the power-on self test
- The VX4244 has been operating for a warm-up period of 10 minutes in an ambient temperature environment as specified in *Appendix A: Specifications*

Equipment Required

This procedure uses traceable signal sources and measurement instruments to check performance. Table F–1 lists the equipment requirements. You may use equipment other than the recommended example if it meets the minimum requirements listed.

Table F–1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. DC Calibration Generator	Amplitude to ±20 V; accuracy to 0.1%	Data Precision 8200	Checking DC accuracy
2. Pattern Generator	±10 V, 10 MHz Sine Wave	Tektronix/CDS VX4750	Checking CMRR & Bandwidth
3. Digital Volt Meter (DVM)	5-1/2 digit, 100 VDC range, 300 kHz AC Bandwidth, accuracy > 0.002 %.	HP3456A	Checking voltage accuracy
4. 50 Ω BNC Coxial Cable (two required)	50 Ω, BNC male connectors	Tektronix part number 012-0057-01	Interconnecting electrical signals
5. BNC T adapter	50 Ω impedance; BNC female to BNC female to BNC male	Tektronix part number 103-0028-00	Interconnecting electrical signals
6. BNC Female to Dual Banana	50 Ω impedance; BNC female, Dual Banana plug	Tektronix part number 103-0090-00	Interconnecting electrical signals
7. BNC Female to Clip Lead	50 Ω impedance; BNC female, Dual Clip Leads	Tektronix part number 013-0076-00	Interconnecting electrical signals
8. DD50S interconnect assembly	DD-50S (female) connector,Tektronix part number 131-1344-00, 26 AWG ribbon wire.	Assemble as shown in Figure F–1	Interconnecting electrical signals
9. 1 in Alligator Clip			Shorting input signals

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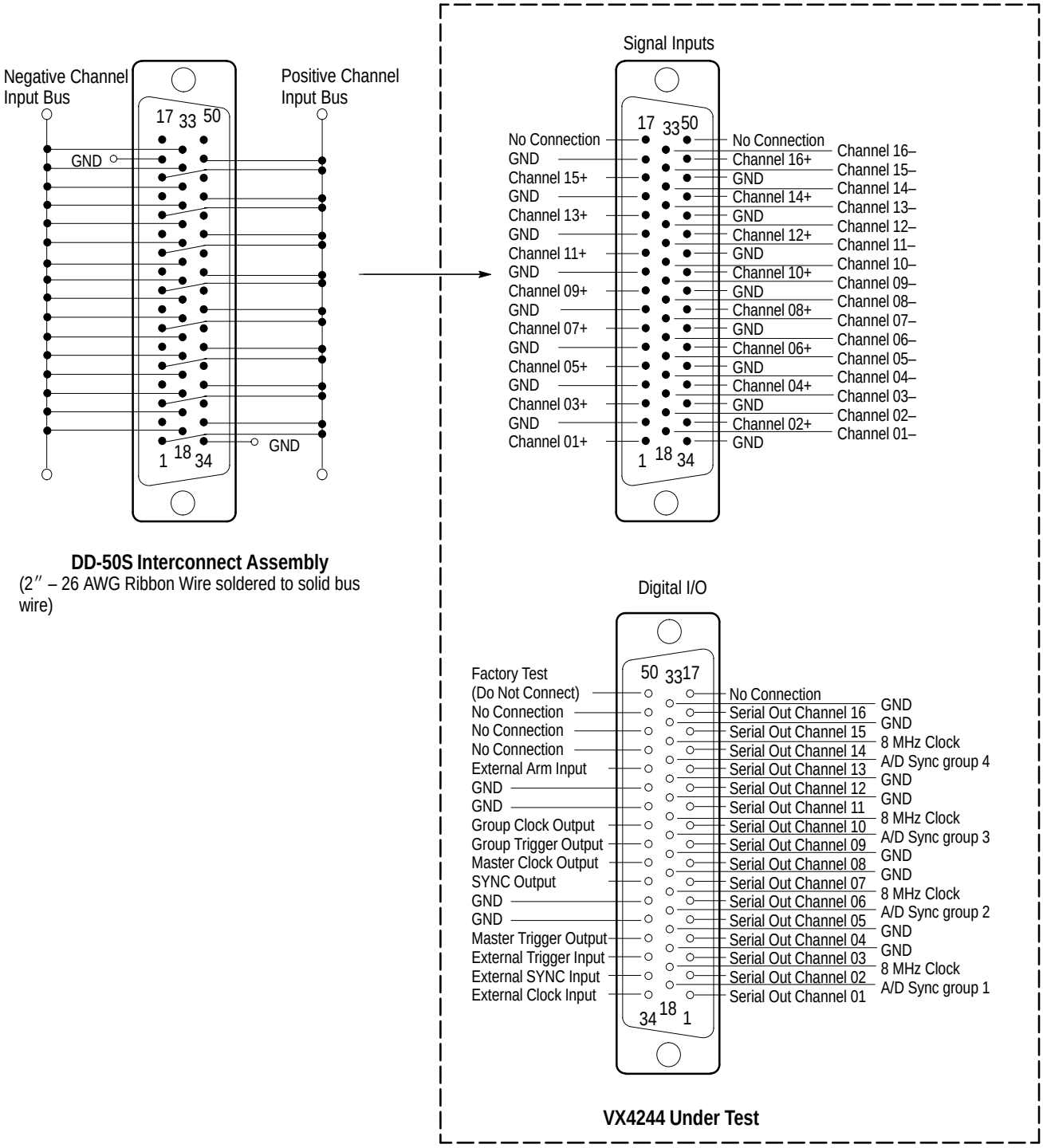


Figure F–1: DD-50S Interconnect Assembly

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VX4244 Under-Test Configuration

In order to perform this procedure, the VX4244-under-test must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table F–2.

Table F–2: Elements of a Minimum VX4244-Under-Test System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	Two available slots in addition to the Slot 0 controller, for the VX4244 and a Pattern Generator	Tektronix VX1400A, VX1410	Power, cooling, and backplane for VXIbus modules
2. Slot 0 Controller	Resource Mgr., Slot 0 Functions, IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Resource Mgr., Slot 0 Functions, GPIB Interface
3. IBM PC or compatible	286 Processor; GPIB card and Software,Talker/Listener/Controller	IBM 486 PC, National Insruments GPIB PC2A card & NI-488.2M software	System Controller
4. GPIB Cable	≈ 2 m length, GPIB connectors	Tektronix p/n 0120–0991-00	Connecting PC GPIB to Slot 0
5. VX4244-Under-Test	Not applicable	Not applicable	Verify its performance

Test System Configuration

Table F–3 describes the VXIbus system configuration assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in the test sequences. (No secondary addressing is assumed.)

Table F–3: VXIbus Test System Configuration (Assumed)

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	13 (0D hex)	13
VX4244-under-test	VX4244	Slot 1	01	1
VX4750	VX4750	Slot 2	02	2

Test Record

Photocopy the Test Record, and use it to record the performance verification results for your module.

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Table F–4: VX4244 Test Record

VX4244 Serial Number:	Temperature and Relative Humidity:
Date of Last Calibration:	Verification Performed by:
Certificate Number:	Date of Verification:

VXIbus Interface		**Logical Address, IEEE Address, Slot No., MFG., Model, etc.**	
Table Command and Self Test Response	1st. Response		
	2nd Response		
	3rd Response		
	4th Response		
		Passed	**Failed**
	Self Test (*TST)		

Signal Input Verification			**Max.**	0.0200V	0.0200V	4.5200V	–4.4800V	18.0200V	–17.980 V
			Min.	–0.0200V	–0.0200V	4.4800 V	–4.5200V	17.9800V	–18.020 V
	CMRR	**Bandwidth**	**DC Input**	0.0000V	–0.0000V	4.5000V	–4.5000V	18.0000V	–18.000V
Channel 1									
Channel 2									
Channel 3									
Channel 4									
Channel 5									
Channel 6									
Channel 7									
Channel 8									
Channel 9									
Channel 10									
Channel 11									
Channel 12									
Channel 13									
Channel 14									
Channel 15									
Channel 16									

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Self Test (*TST)

The VX4244 includes a built-in self test (BITE) which is executes each time the power is turned on and (more extensively) when the Self Test command (*TST) is issued. Internal reference circuitry and test routines verify the CPU, RAM, A/D converters, thresholds, latches, counters, the analog input amplifiers, and the cross switching. Arming, triggering, measurement complete, time-tag, and EEPROM are also tested.

In addition to BITE, front panel lights display the status of POWER and module FAILED error conditions. Following system initialization, the presence of the POWER light indicates that the self test has passed and that the supplies are correct. If a power supply fails (+5 V, ±24 V, ±12 V, –5.2 V, or –2 V), or a corresponding fuse opens, the POWER light will be off, and the red FAILED light will be on (indicating that SYSFAIL* has been asserted). If the +5 V supply fails, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module.

NOTE. *If you experience an error indication from the Slot 0 Resource Manager, the VX4244-under-test, or other VXIbus module, investigate and correct the problem before proceeding. Common items to check are logical address conflicts (see Table F–5), breaks in the VXIbus daisy chain signals, improper seating of a module, loose GPIB cable, improperly set Slot 0 single step switch, or loose or blown fuses.*

Performance Verification Tests

The verification sequences in this procedure contain instructions for the example test equipment listed in Table F–1. You may use instrumentation other than the recommended examples if it meets the minimum requirements listed. The order of execution of the test sequences has been chosen to minimize system setup and programming requirements. It is recommended that you follow the order presented, as some tests rely on previously verified parameters.

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VXIbus Interface

This sequence verifies that the VX4244 configures correctly and communicates properly with your GPIB system controller.

Equipment Requirements	No additional test equipment is required for this sequence.
Prerequisites	All prerequisites listed on page F–2

***NOTE**. If you are using National Instruments NI-488.2 software you can select the buffer 1 display mode to allow more comfortable viewing of the ASCII response. Just type* `buffer 1.`

1. To verify the system configuration, send the TABLE command to the VX4521 Slot 0 Resource Manager and confirm the responses shown in Table F–5. Your configuration may not be identical, but the responses should be similar. If you are using a controller other than the VX4521, use the equivalent procedure to observe the system configuration.

Table F–5: VXIbus System Configuration

Command to Type	Response to Verify
`ibic`	
`ibfind VX4521`	
`ibwrt "table"`	
`ibrd 200`	03 (number of modules)
`!`	`LA 0, IEEE 13, Slot 0, MFG FFDh, MODEL VX4521, PASS, , RM..`
`!`	`LA 1, IEEE 01, Slot 1, MFG FFCh, MODEL VX4244, PASS, 488.2, MESG, 0, V1.3, NORMAL`
`!`	`LA 2, IEEE 02, Slot 2, MFG FFCh, MODEL VX4750, PASS, TRIGGER;LOCK:READ STB, MESG, 0, V1.3, NORMAL`

2. Perform an extended self test and verify that there are no pending errors:

   ```
   ibfind VX4244

   ibwrt "*tst"
   ```
   (Observe front panel activity for about 30 seconds)

   If the ERROR light remains on after the test, determine the cause with the "ERRor?" query command (also, see *Appendix C: Self Test Failures*, and *Appendix D: Module Diagnostic Commands*).

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Bandwidth

This sequence verifies the Bandwidth of the input gain switch amplifier, the input attenuators (divide by 2, 5, and 10), and the A/D converter for the individual channels. All input components are utilized and therefore verified by checking the 5 and 20 V ranges.

Equipment Requirements	Pattern Generator (item 2) BNC to Dual Banana Plug (item 6) BNC coaxial cable, two required (item 4) BNC T (item 5) BNC to Clip Lead adaptor (item 7) DD-50S interconnect adaptor (item 8)
Prerequisites	All prerequisites listed on page F–2

1. Attach the DD-50S interconnect adaptor to the VX4244 Signal Inputs connector. Connect the VX4750 FUNC OUT signal to the VX4244 positive and negative channel inputs and to the DVM using two coaxial cables, a BNC-T adaptor, a BNC-to-dual Banana adaptor, and a BNC-to-Clip-Lead adaptor.

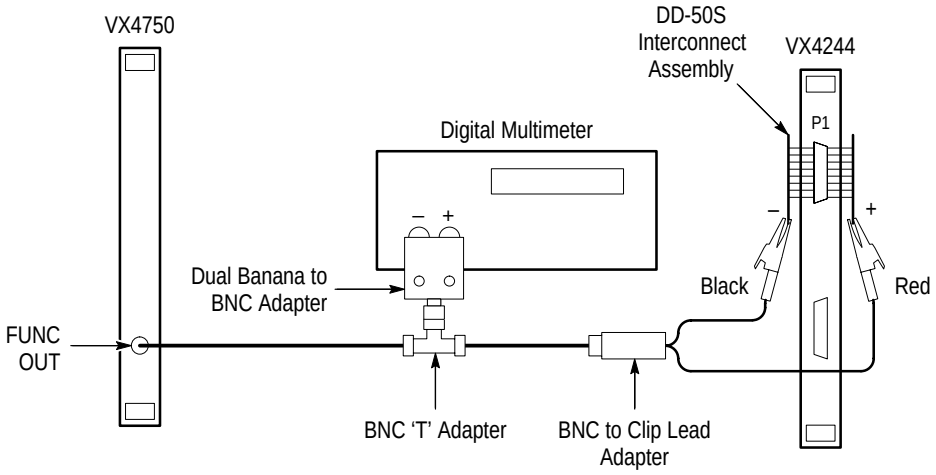


Figure F–2: Setup for Bandwidth Test

2. Reset the VX4750 to its power-on state, for a 1 MΩ output impedance, and for a 4.5 V_{pk} (3.182 V_{rms}) 151 kHz sine waveform.

```
ibfind VX4750

ibwrt "*rst;imp 1e6;ampL 4.5 Vp;freq 151e3"
```


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3. Set the VX4244 to its power-on default state and for the 5.0 V range. Then initiate an acquisition and fetch the true RMS value of 4096 samples. Verify that the bandwidth roll off (computed as $20Log_{10}(V_{DVM}/V_{4244})$) is less than 2.7dB. For example if the input signal from the VX4750 (V_{DVM}) is 3.3078, and the measured value returned from the VX4244 is +3.074752, then the bandwidth roll-off is $20Log_{10}(3.3078/3.074752)$ = 0.634 dB.

```
set VX4244

ibwrt "*rst;volt:range 5 (all)"

ibwrt "route:open(all);route:close(@1)"

ibwrt "init(@1)"
```
(initiate acquisition on group 1 inputs)

```
ibwrt "fetch:trms? 4096 (@1)"
```
(fetch channel of interest value)

```
ibrd 100
```
(record as V_{4244} and perform calculation)

If you intend to verify additional channels, repeat the last four commands substituting the channel number of interest in the route command and the four channel group to which it belongs in the init command.

4. Repeat the test using the 20 V range of the VX4244 with an 11 V_{pk}, 151 kHz sine wave input signal. Again verify less than 2.7dB bandwidth roll-off. (For example if V_{RMS} (as read from the DVM) is 8.0139 and the true RMS value returned from the VX4244 is +7.471113, then the bandwidth roll-off would be calculated as $20Log_{10}$ (8.0139/7.471113) = 0.609dB.

```
set vx4750

ibwrt "ampL 11vp"

set VX4244

ibwrt "volt:range 20 (all)"

ibwrt "route:open(all);route:close(@1)"

ibwrt "init(@1)"
```
(initiate acquisition on group 1 inputs)

```
ibwrt "fetch:trms? 4096 (@1)"
```
(fetch channel of interest value)

```
ibrd 100
```
(perform calculation and verify < 2.7dB roll-off)

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If you intend to verify additional channels, repeat the last four commands substituting the channel number of interest in the route command and the four channel group to which it belongs in the init command.

Common Mode Rejection

This sequence verifies the a Common Mode Rejection Ratio (CMRR) of better than 2500:1 (>68 dB, at 100 Hz).

Equipment Requirements	VX4750 (item 2) 50 Ω BNC cable (item 4) BNC to Clip Lead adapter (item 7) DD-50S interconnect adapter (item 8) 1 in alligator clip (item 9)
Prerequisites	All prerequisites listed on page F–2

1. Attach the DD-50S interconnect adaptor to the VX4244 Signal Inputs connector. Connect the VX4750 FUNC OUT signal to the VX4244 positive and negative channel inputs using a coaxial cable and a BNC-to-Clip-Lead adapter. Attach the red clip lead to the positive-channel signal bus and the black clip lead to the negative-channel signal bus of the DD-50S interconnect adaptor.

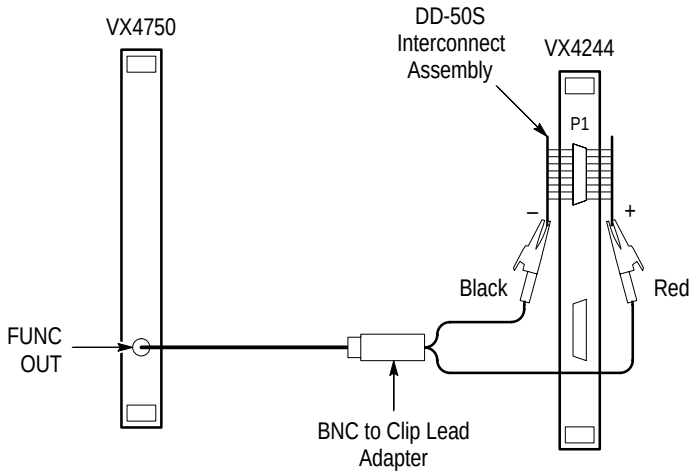


Figure F–3: Setup for CMRR Test

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2. Set the VX4750 to its power-on default, for a 1 MΩ output impedance, and a 100 Hz, 20 V_{p-p} sine wave.

   ```
   set VX4750

   ibwrt "*rst;imp 1e6;ampL 20vpp;freq 100"
   ```

3. Reset the VX4244 to its power-on default state and to open all relays except the channel being tested. Initiate an acquisition for the group containing the channel being tested, and fetch a true RMS value from the first 4096 data samples. Read the result and record the value returned as the differential voltage value (V_{diff}) for the calculation in Step 6.

   ```
   set VX4244

   ibwrt "*rst;route:open(all);route:close(@1)"

   ibwrt "init(@1)"
   ```
   (acquire GROUP containing channel of interest)
   ```
   ibwrt "fetch:trms? 4096 (@1)"

   ibrd 100
   ```
   (Record this reading as V_{diff}; e.g. V_{diff}=7.333311.)

4. Reconnect the VX4750 for a single ended voltage measurement as follows:

   a. Move the black clip lead from the DD-50S negative channel bus to a DD-50S ground pin (pin 16 or 34).

   b. Short the positive and negative DD-50S assembly buses together using an alligator clip (the red clip lead should now be connected to both the positive and negative channel buses).

5. Acquire the single-ended voltage (V_{single}) with the following commands:

   ```
   ibwrt "*rst;route:open(all);route:close(@1)"

   ibwrt "init(@1)"

   ibwrt "volt:range .2(@1)"

   ibwrt "fetch:trms? 4096 (@1)"

   ibrd 100
   ```
   (Record this reading as Vsingle-ended; e.g. Vs=0.000612.)

6. Calculate the CMRR as $20Log_{10}$ (V_{diff}/V_{single}) and verify that the result is greater than 68 dB. For the example voltage readings above, 20 Log_{10}(7.333311/0.000612) results in a CMRR of 81.57 dB.

7. If you want to verify CMRR for all channels, repeat steps 3 through 6 for channels 2 through 16 by substituting the channel number being verified

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following the @ in all command strings except those containing “init(@x)”. In the command strings containing “init(@x)” substitute the corresponding group number in place of the “x” (for example, group 1 contains channels 1 through 4, group 2 contains channels 5 through 8, and so forth).

DC Voltage Accuracy

This sequence verifies the DC accuracy of the input gain-switch amplifier, the input attenuators (divide by 2, 5, and 10) and the A/D converter for each channel. All input components are utilized, and therefore verified, by checking the 5 and 20 V ranges.

Equipment Requirements	DC Calibration Generator (item 1) BNC to Dual Banana Plug (item 6) BNC cable (item 4) BNC to Clip Lead adaptor (item 7) DD50S interconnect adaptor (item 8)
Prerequisites	All prerequisites listed on page F–2

1. Connect the DC Calibrator to the VX4244 positive and negative channel inputs using a BNC-to-dual Banana adaptor, a BNC coaxial cable, a BNC-to-Clip-Lead adaptor and the DD-50S interconnect assembly. Set the Calibrator to +4.5 VDC.

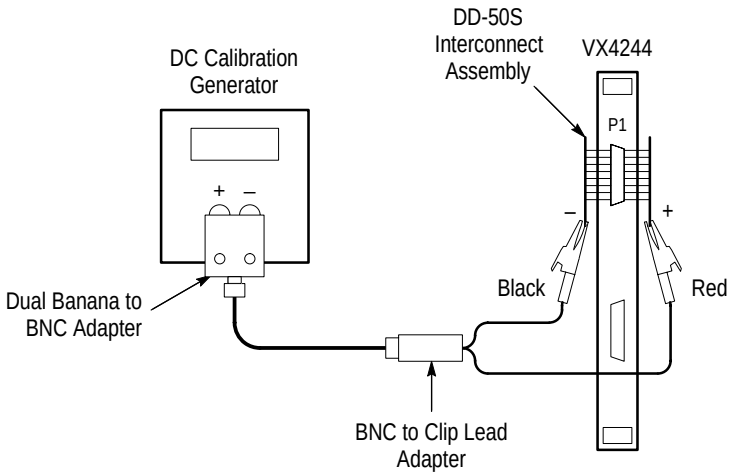


Figure F–4: Setup for DC Voltage Accuracy Test

2. Set the DC Calibrator output to +4.50000 VDC.

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3. Set the VX4244 to its power-on state and select the 5.0 V range.

   ```
   set VX4244

   ibwrt "*rst;volt:range 5 (all)"
   ```

4. Select the input channel to be tested by closing the corresponding relay. Then initiate an acquisition and fetch an average value. Verify the result to be within 0.2% of the full scale range.

   ```
   ibwrt "rout:open(all);rout:clos(@1)"
   ```
   (select channel to test)

   ```
   ibwrt "init(@1)"
   ```
   (initiate acquisition on group containing channel)

   ```
   ibwrt "fetch:ave? 1000 (@1)"
   ```
   (average first 1000 samples)

   ```
   ibrd 100
   ```
   (Observe Calibrator value to be within 0.2% of full scale)

5. Set the DC Calibrator to 0.00000 VDC.

6. Initiate an acquisition, fetch the average value, and verify the result to be within 0.2% of the full scale range.

   ```
   ibwrt "init(@1)"
   ```
   (acquire group containing channel under test)

   ```
   ibwrt "fetch:ave? 1000 (@1)"

   ibrd 100
   ```

7. Set the DC Calibrator to –4.50000 VDC (or –18.0000 VDC; see step 11).

   ```
   ibwrt "init(@1)"

   ibwrt "fetch:ave? 1000 (@1)"

   ibrd 100
   ```

8. If you want to verify additional channels, repeat steps 3 through 7 for remaining input channels (2 through 16). Substitute the channel number being tested in all commands except the “init” commands. In the INIT commands, substitute the Group number (1 through 4) containing the channel being tested.

9. To verify the 20 V range, reset the DC Calibrator to +18.0000 VDC.

10. Set the VX4244 to the 20 V range.

    ```
    ibwrt "volt:range 20 (all)"
    ```


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11. Repeat steps 4 through 8 substituting –18.000 VDC for –4.50000 VDC in step 7.

This completes the VX4244 verification procedure.

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WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

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Appendix G: User Service

This appendix contains service-related information for the VX4244 that covers the following topics:

- Preventive maintenance
- Troubleshooting
- User-replaceable parts
- Adjustment

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent VX4244 malfunction and enhance reliability. Inspect and clean the VX4244 as often as conditions require by following these steps:

1. Turn off power and remove the VX4244 from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with a lint-free cloth dampened with water or a 75% isopropyl alcohol solution. Do not use abrasive cleaners.

Troubleshooting

If you suspect a malfunction, first double check connections to and from the VX4244. If the trouble persists, perform the *Functional Check* beginning on page 1–12. You can also execute the diagnostic commands found in *Appendix D*; however, be sure to observe the precaution in *Appendix D* regarding use of the DIAGnostic:DEFAULT:CALIBRATION command.

If the self test or diagnostic commands indicate a failure, contact your Tektronix field office or representative for assistance.

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User-Replaceable Parts

Table G–1 lists the user-replaceable parts of the VX4244. Refer to Figure G–1 for the part locations.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

Table G–1: User-replaceable Parts

Part	Part Number
User Manual	070-9067-XX
ID marker, bottom	334-8838-XX
ID marker, top	334-8839-XX
Collar screw	950-0952-XX
Screw	211-0867-XX
Spare fuse 5A	159-0207-XX
Spare fuse 2A	159-0128-XX
Spare fuse 1A	159-0116-XX



CAUTION. *Static discharge can damage any semiconductor component in this module. Replace fuses only in a static-free environment.*

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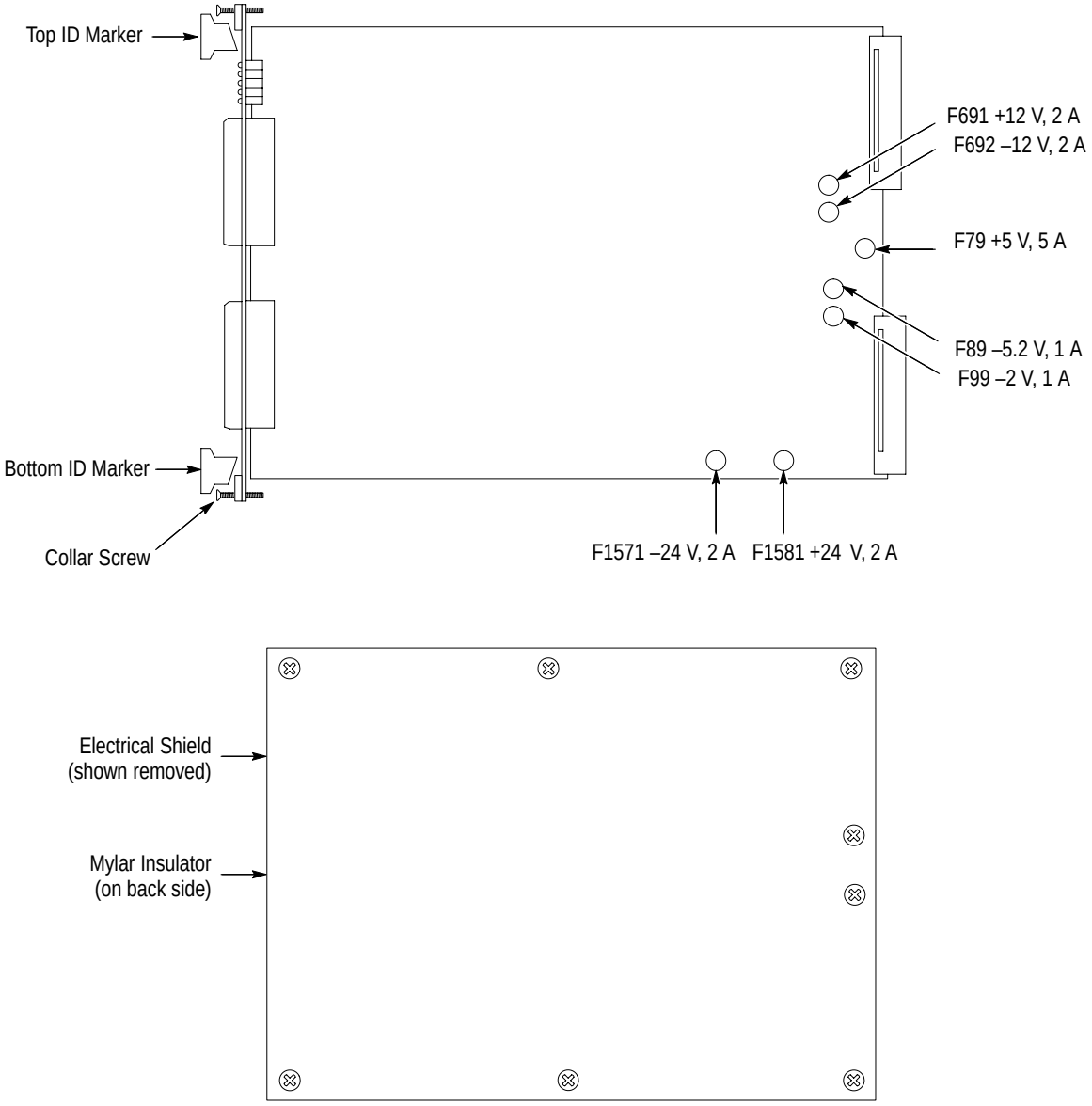


Figure G–1: User-replaceable Part Locations

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Adjustment

Use this procedure to adjust the DC Accuracy of the VX4244.

Equipment Required	Precision DC voltage calibrator, Advantest R6144/6142 or equivalent
Prerequisites	Twenty minute warm up
Time Required	Approximately one-half hour (automated)

Beginning with CH1, perform the following steps for each of the sixteen channels:

1. Connect the precision DC voltage source (calibrator) so that its output voltage is applied between the positive and negative inputs of the VX4244 channel being adjusted.
2. Set the precision DC voltage source output to the value in Table G–2.
3. Send a CALibrate command to the VX4244 as specified in Table G–2. Substitute the channel id for the channel being adjusted, for example, substitute (@2) to adjust CH2.

Table G–2: VX4244 Adjustments for Each Channel (CH1 shown)

DC Voltage Source Setting	Calibrate Command
+0.190	CAL:Value 0.19 (@1)
–0.190	CAL:Value –0.19 (@1)
+0.475	CAL:Value 0.475 (@1)
–0.475	CAL:Value –0.475 (@1)
+0.950	CAL:Value 0.95 (@1)
–0.950	CAL:Value –0.950 (@1)
+1.900	CAL:Value 1.90 (@1)
–1.900	CAL:Value –1.900 (@1)
+4.750	CAL:Value 4.75 (@1)
–4.750	CAL:Value –4.750 (@1)
+9.500	CAL:Value 9.50 (@1)
–9.500	CAL:Value –9.500 (@1)
+19.90	CAL:Value 19.9 (@1)
–19.90	CAL:Value –19.90 (@1)

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Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted. Not all terms appear in every manual.

Accessed Indicator
An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.

ACFAIL*
A VMEbus backplane line that is asserted under these conditions: 1) by the mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.

A-Size Card
A VXIbus instrument module that is 100.0 × 160 mm × 20.32 mm (3.9 × 6.3 in × 0.8 in), the same size as a VMEbus single-height short module.

Asynchronous Communication
Communications that occur outside the normal “command-response” cycle. Such communications have higher priority than synchronous communication.

Backplane
The printed circuit board that is mounted in a VXIbus mainframe to provide the interface between VXIbus modules and between those modules and the external system.

B-Size Card
A VXIbus instrument module that is 233.4 × 160 mm × 20.32 mm (9.2 × 6.3 in × 0.8 in), the same size as a VMEbus double-height short module.

Bus Arbitration
In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.

Bus Timer
A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.

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Client
In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10
A 10 MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1–12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

CLK100
A 100 MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1–12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

Commander
In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command
A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers
In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers
A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card
A VXIbus instrument module that is 340.0 × 233.4 mm × 30.48 mm (13.4 × 9.2 in × 1.2 in).

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Custom Device
A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

Data Transfer Bus
One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

DC SUPPLIES Indicator
A red LED indicator that illuminates when a DC power fault is detected on the backplane.

Device Specific Protocol
A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card
A VXIbus instrument module that is 340.0 × 366.7 mm × 30.48 mm (13.4 × 14.4 in × 1.2 in).

DTB
See Data Transfer Bus.

DTB Arbiter
A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT
Device Under Test.

ECLTRG
Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 Ω; the asserted state is logical High.

Embedded Address
An address in a communications protocol in which the destination of the message is included in the message.

ESTST
Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Self Test
Any self test or diagnostic power-on routine that executes after the initial kernel self test program.

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External System Controller
The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator
A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

IACK Daisy Chain Driver
The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

ID-ROM
An NVRAM storage area that provides for non-volatile storage of diagnostic data.

Instrument Module
A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

Interface Device
A VXIbus device that provides one or more interfaces to external equipment.

Interrupt Handler
A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter
A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ
The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus
A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller
The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus mainframe or several mainframes. See Resource Manager.

Local Processor
The processor on an instrument module.

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Logical Address
The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

Mainframe
Card Cage. For example, the Tektronix VX1400 Mainframe, an operable housing that includes 13 C-size VXIbus instrument module slots.

Memory Device
A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message
A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

Message Based Device
A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines
Module/system identity lines.

Physical Address
The address assigned to a backplane slot during an access.

Power Monitor
A device that monitors backplane power and reports fault conditions.

P1
The top-most backplane connector for a given module slot in a vertical mainframe such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal mainframe.

P2
The bottom backplane connector for a given module slot in a vertical C-size mainframe such as the VX1400; or the middle backplane connector for a given module slot in a vertical D-size mainframe such as the VX1500.

P3
The bottom backplane connector for a given module slot in a vertical D-size mainframe such as the Tektronix VX1500.

Query
A form of command that allows for inquiry to obtain status or data.

READY Indicator
A green LED indicator that lights when the power-on diagnostic routines have been completed successfully. An internal failure or failure of +5 V power will extinguish this indicator.

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Register Based Device
A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.

Requester
A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.

Resource Manager
A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.

Self Calibration
A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.

Self Test
A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-on.

Servant
A VXIbus message-based device that is controlled by a commander.

Server
A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.

Shared Memory Protocol
A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

Slot 0 Controller
See Slot 0 Module. Also see Resource Manager.

Slot 0 Module
A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.

SMP
See Shared Memory Protocol.

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STARX
Two (2) bi-directional, 50 Ω, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 ns, and the lines are well matched for timing skew.

STARY
Two (2) bi-directional, 50 Ω, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 ns, and the lines are well matched for timing skew.

STST
STart/STop protocol; used to synchronize modules.

SYNC100
A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2 ns of skew.

Synchronous Communications
A communications system that follows the “command-response” cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL*
A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

System Clock Driver
A functional module that provides a 16 MHz timing signal on the Utility Bus.

System Hierarchy
The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

Test Monitor
An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

Test Program
A program, executed on the system controller, that controls the execution of tests within the test system.

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Test System
A collection of hardware and software modules that operate in concert to test a target DUT.

TTLTRG
Open collector TTL lines used for inter-module timing and communication.

VXIbus Subsystem
One mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.

Word Serial Protocol
A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).

Word Serial Communications
Inter-device communications using the Word Serial Protocol.

WSP
See Word Serial Protocol.

10-MHz Clock
A 10 MHz, ±100 ppm timing reference. Also see CLK10.

100-MHz Clock
A 100 MHz, ±100 ppm clock synchronized with CLK10. Also see CLK100.

488-To-VXIbus Interface
A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

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