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User Manual

Tektronix

VX4790A
Arbitrary Waveform Generator Module

070-9152-02

This document applies for firmware version 1.00 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

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EC Declaration of Conformity

We

Tektronix Holland N.V.
Marktweg 73A
8444 AB Heerenveen
The Netherlands

declare under sole responsibility that the

VX4790A and all options

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

CONDITIONS: To ensure compliance with EMC requirements this module must be installed in a mainframe which has backplane shields installed which comply with Rule B.7.45 of the VXIbus Specification.

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#[n][m] programs the arbitrary-waveform voltage in binary. (A - 15)
GETBIN? [n] Returns the values programmed in ARB memory in binary format. (3 - 15)
[z]R programs the number of times to repeat the waveform, or programs continuous transmission. (3 - 41)
SCOPY [s] [d] [n] Copies one portion of waveform memory to another. (3 - 42)
SFILL [a] [s] Fills a block of waveform memory with the value in the first location of the block. (3 - 55)
STARTBIN [a] [c] Sets up the parameters for a binary load of waveform memory and puts the module into binary mode. (3 - 58)

TRIGGER COMMANDS

[z]T resets the memory to the first location and starts actual transmission of the programmed waveform, or retriggers the module when it is halted at a breakpoint. (3 - 61)
Q used to halt output of a waveform. (3 - 40)

WAVEFORM EDIT COMMANDS

[z]M selects a memory location in the programmed waveform or set of waveforms for editing or start of transmission. (3 - 36)
[z]N moves the memory pointer to allow memory loads, but does not move the counter pointer that directs the ARB memory. (3 - 37)

MISCELLANEOUS COMMANDS

K resets the module to its power-up state. (3 - 34)
SETDEF Sets the power up default values for the current memory page without resetting the settings for other memory pages. (3 - 44)
? reports the module's status and clears errors. (3 - 70)
GETREV? Returns the revision number of the board. (3 - 30)
STEST runs the on-board self test to check the integrity of the ARB. (3 - 60)
SMEMTEST Starts the test of the entire installed waveform memory. (3 - 56)
GETERR? Reports any errors which may have occurred. (3 - 20)
GETINT? Returns the status of any interrupts, regardless of whether or not they have been enabled. (3 - 25)
GETMEM? Returns the amount of installed memory. (3 - 27)
GETPAGE? Returns the current memory page. (3 - 28)

VX4790A ARBITRARY WAVEFORM GENERATOR QUICK REFERENCE GUIDE

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 1 - 4)
Follow Installation guidelines. (p. 2 - 1)

The default condition of the VX4790A Module after the completion of power-up self test is as follows:

Sampling Frequency - 25 MHz.
Voltage Waveform - 0 V dc waveform.
Isolation Relay - Output Disconnected.
Repeat Count - Continuous.
External Trigger - Disabled.
Interrupts - Disabled.
Low Pass Filter - Disabled.
Memory Edit Address - 0.
Attenuator - Disabled.
External Attenuator - Disabled.
Voltage Range - ±10 Volts.
Error Status - Result of self test.
Output State - Not triggered.
Paging - Set to 0, reset.

LEDs

When lit, the LEDs indicate the following:

Power	power supplies functioning
Failed	module failure
ERR	an error has been found in self test or programming
MSG	module is processing a VMEbus cycle
FHS	the module is in the fast handshake mode
RUN	ARB memory is actively transmitting
BKPT	ARB memory breakpoint is active
XCLK	an external clock input is enabled
XTRG	an active external trigger input
LOCK	when lit constantly indicates that the phase lock loop is in a lock condition. If flashing, indicates that the phase lock loop is not locked and selected ARB sample periods or frequencies will not be correct if run.

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SYSTEM COMMANDS

These non-data commands are initiated by the VX4790A's commander. The following VXIbus Instrument Protocol commands will affect the VX4790A:

BEGIN NORMAL OPERATION	TRIGGER
BYTE AVAILABLE	SET LOCK
CLEAR	READ STATUS
BYTE REQUEST	READ PROTOCOL
CLEAR LOCK	IDENTIFY COMMANDER

COMMAND SYNTAX

Command protocol and syntax for the VX4790A Module is as follows: (3 - 3)

1) Each command is an ASCII character. Modifiers are ASCII numbers preceding the letter command.
   <CR> = carriage return. <LF> = line feed.
   <TM> = terminator: indicates a line feed or a semicolon. Only required on multicharacter commands.
2) Any character may be sent in either upper or lower case form.
3) Any of the following white space characters:
   00 hex 0B - 19 hex
   01 - 08 hex 20 hex 09 hex
   have no effect on any of the commands and any number of white space characters may be used together.
4) All numbers may be specified in integer or floating point notation, with or without exponent. Any number may be omitted on all single character commands.
5) For the M and N commands, if the number is enclosed by parenthesis (), this module will interpret it in hexadecimal format.

MODULE COMMANDS

This summary lists the commands in the order they typically would be programmed. Detailed descriptions are in alphabetical order.

SETUP COMMANDS

[z]C programs the external clock input enable. (3 - 9)
[z]X selects the external-trigger source (VXIbus TTLTRG lines or front panel). (3 - 66)
[z]U selects the EOW (End Of Wave) bit or the programmed synchronization pulse for connection to the front panel Sync output. (3 - 62)
[z]I enables or disables generation of VXIbus interrupts by the ARB. (3 - 33)
GETMASK? Returns the programmed interrupt mode. (3 - 26)
GOTOBUF Enables input buffering. (3 - 31)
GOTONBUF Disables input buffering. (3 - 32)
SETPAGE [p] Sets the memory page. (3 - 46)
[z]O controls the isolation relays on the ARB output. (3 - 38)

PRE-PROGRAMMED WAVEFORM COMMANDS - program the specified wave at the programmed amplitude and frequency.

SETSINE [z] [f] Programs a sine wave. (3 - 50, 3 - 51)
or SETSINO [z] [m] [f]
SETSQUARE [z] [m] [f] Programs a square wave. (3 - 52)
SETTRIANG [z] [m] [f] Programs a triangle wave. (3 - 53)
SETSAWTOO [z] [m] [f] Programs a sawtooth wave. (3 - 49)

FREQUENCY COMMANDS

[z]F, [z]P or [z]D F (Frequency) (3 - 13), P (Period) (3 - 39), or D (Divide) (3 - 12) commands program the basic sample rate of the module.

SETDIV [d] Sets the sample clock divider without changing the frequency of the phase locked loop oscillator. (3 - 45)
SETPLL [f] Sets the frequency of the phase locked loop oscillator without changing the sample clock divider. (3 - 48)
GETFREQ? Returns the actual frequency of the frequency source. (3 - 24)
GETDIV? Returns the setting of the sample clock divider. (3 - 19)
GETPLL? Returns the frequency of the sample clock's phase locked loop oscillator. (3 - 29)
[z]L enables or disables the low pass filters on the analog output. (3 - 35)

VOLTAGE/ATTENUATOR COMMANDS

SETVOLTR[z] Sets the output voltage range. (3 - 54)
[z]% sets the output attenuation to be set on all programmed voltage outputs. (3 - 72)
GETATT? Returns the currently programmed attenuation value. (3 - 14)
[z]A Enables or disables the external attenuator input. (3 - 8)

ARBITRARY WAVEFORM COMMANDS

[pv]V (variations: B, W, or Z) sequentially programs the arbitrary-waveform voltages. The variations allow including a breakpoint and/or end-of-wave. (3 - 63)
Y programs the programmed sync bit in the V, B, W, or Z commands. (3 - 69)
GETDATA? [n] Returns ARB memory. (3 - 18)
GETCODE? [n] Returns ARB memory, including sync, breakpoint, and end-of-wave codes. (3 - 17)

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Table of Contents

Section 1
General Information and Specifications

Introduction . . . . . 1 – 1
Controls And Indicators . . . . . 1 – 4
Switches . . . . . 1 – 4
Fuses . . . . . 1 – 5
LEDs . . . . . 1 – 5
SMB Connector Inputs and Outputs . . . . . 1 – 6
BITE (Built-In Test Equipment) . . . . . 1 – 6
Specifications . . . . . 1 – 8

Section 2
Preparation For Use

Installation Requirements And Cautions . . . . . 2 – 1
Installation Procedure . . . . . 2 – 2
Installation Checklist . . . . . 2 – 4

Section 3
Operation

Overview . . . . . 3 – 1
Power-up . . . . . 3 – 2
System Commands . . . . . 3 – 2
Module Commands . . . . . 3 – 3
Summary . . . . . 3 – 4
Command Descriptions . . . . . 3 – 8
SYSFAIL, Self Test, and Initialization . . . . . 3 – 73
Synchronizing Multiple Instrumentation Modules . . . . . 3 – 74

Section 4
Programming Examples

Definition of BASIC Commands . . . . . 4 – 1
Programming Example In BASIC . . . . . 4 – 2

Appendices

Appendix A – VXIbus Operation . . . . . A – 1
Appendix B – Input/Output Connections . . . . . A – 5
Appendix C – VXI Glossary . . . . . A – 7
Appendix D – Advanced Program Capabilities . . . . . A – 15
Appendix E – Frequency Source Accuracy . . . . . A – 19
Appendix F (Option 1M) – MATE Programming . . . . . A – 21
Appendix G – User Service . . . . . A – 41
Appendix H – Options . . . . . A – 43
Appendix I – VX4790A Performance Verification . . . . . A – 45
Appendix J – VX4790A Adjustment Procedure . . . . . A – 67

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Avoid Electric Overload

To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

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WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:



DANGER
High Voltage



Protective Ground
(Earth) Terminal



ATTENTION
Refer to Manual



Double
Insulated

Certifications and Compliances

Overvoltage Category

Overvoltage categories are defined as follows:

CAT III: Distribution level mains, fixed installation

CAT II: Local level mains, appliances, portable equipment

CAT I: Signal level, special equipment or parts of equipment, telecommunication, electronics

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VX4790A
Arbitrary Waveform Generator

Section 1
General Information and Specifications

Introduction

The VX4790A Arbitrary Waveform Generator Module (ARB) is a printed circuit board assembly designed for use in a mainframe conforming to the VXIbus Specification. It generates user-defined waveforms of up to 262,144 voltage samples (more with additional memory options) at sample rates of up to 25 MHz using either the internal or an external clock source.

One of the main features of the VX4790A is its ability to vary the output frequency and amplitude of a stored waveform without having to re-send that waveform from the system controller. In addition, the ARB has sine, square, sawtooth, and triangular waveforms stored in internal memory, giving it many of the features of a function generator. The user only has to specify frequency and amplitude when invoking any of these waveforms.

The ARB Module produces an analog output capable of driving a 50 Ohm load in three voltage ranges:

- ±10.22 Volts programmable in 5 milliVolt steps,
- ±5.11 Volts with a 2.5 milliVolt resolution, and
- ±0.1 Volts with a 50 microVolt resolution.

A programmable attenuator is provided which can reduce the programmed output voltage. The output value may be expressed as a percentage of full scale when programmed internally or varied based on an externally supplied reference. When the external reference input is selected, output level is set to 50% of full scale based on 0 volts at the reference input. Applying +1.5 volts to the external reference input will then set the output level to 100%, while -1.5 volts will set the output level to 0%. A varying signal of up to 1.5 V ptp may be applied for up to 99% AM modulation.

A series of low pass filters may be switched into the output under program control. Filters available include: 5 MHz low pass, 500 KHz low pass, and 50 KHz low pass.

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The effect of these filters on the output waveform is smoother transitions between voltage steps, and reduced harmonics.

The programmed waveform(s) can be repeated continuously or from one to 255 times. Programmable breakpoints can be entered in any non-consecutive voltage samples, excluding the first voltage sample of the waveform. A breakpoint causes the waveform to pause until it is retriggered by software, or by a TTL trigger from an external source. This feature is particularly useful in applications where it is desirable to coordinate portions of the output waveform with other portions of the test.

Waveform programming can be done in ASCII, binary, or CIIL (with Option 1M installed) syntax. The module can be triggered by software or by an external hardware source. The ARB has a 16 KByte input buffer enabling it to receive data at VXI backplane speed. This is particularly valuable for applications involving large blocks of data and fast system controllers.

Multiple ARB Modules can be slaved to a single module, or to a common external clock (sample rate) source to allow output waveforms to be phase synchronized. This feature expands the range of applications for the ARB. For example, the phase relationship between waveforms that have been synchronized in this manner can be varied under program control by specifying a new starting memory location for each individual output waveform.

Memory locations are easily programmed using a string of numeric ASCII characters which directly specify the output voltage for each sample. The editing capability allows individual points in the waveform to be changed without requiring a complete memory reload. In addition, memory loading is further optimized during a block waveform load by an auto-increment feature. With this, you need only program the starting waveform address at the beginning of the block waveform load.

Auxiliary inputs provide for an external clock (sample rate) input (up to 25 MHz), and for an external trigger. When external clock (sample rate) is selected, either the front panel input or any one of the 8 VXI TTL trigger lines may be used as a source. Auxiliary outputs provide a clock (sample rate) output at a frequency equivalent to the programmed sample rate, and a synchronization pulse that is generated at the end of each waveform cycle. The ARB may also be triggered by any of the TTL trigger lines as well as externally or under software control.

Note that certain terms used in this manual have very specific meanings in the context of a VXIbus System. These terms are defined in the VXIbus Glossary (Appendix C).

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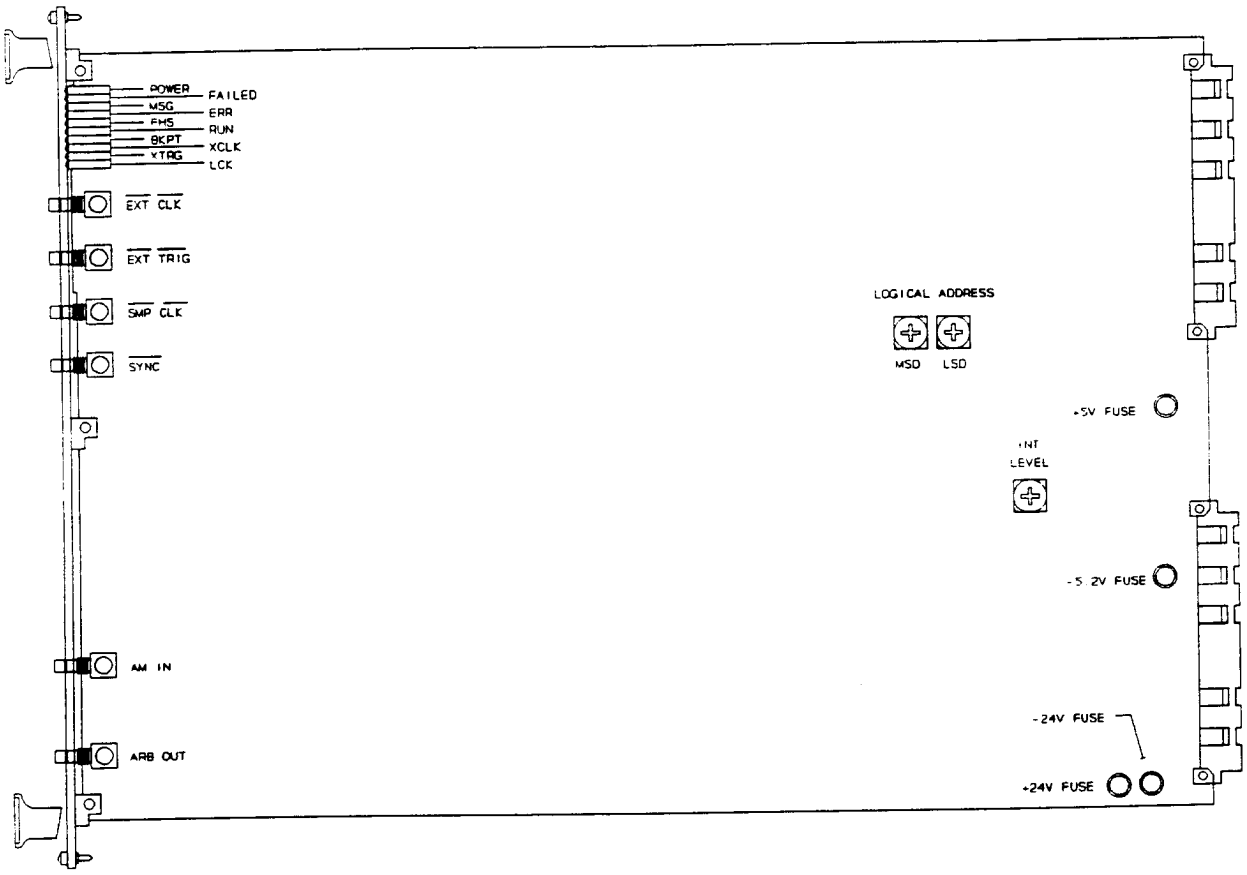


Figure 1: VX4790A Controls and Indicators

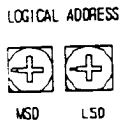
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Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4790A Module's operating environment. See Figures 1 and 2 for their physical locations.

Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4790A is set to a value between 1 and FEh (254d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

The actual physical address of the VX4790A Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4790A will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

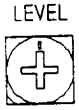
where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the VX4790A Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address. Consult the operating manual of the Slot 0/Resource Manager being used for recommendations on setting the module's logical address.

If the VX4790A is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC).

VMEbus Interrupt Level Select Switch



Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander. The VMEbus interrupt level on which the VX4790A Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

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Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4790A's interrupt handler, typically the module's commander. Setting the switch to 0 or 8 will disable the module's interrupts. Switch setting 9 should not be used.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

Fuses

Each of the VX4790A power buses has an on-board fuse. The module has fuses for +5V, -5.2V, +24V, and -24V. The fuses protect the module in case of an accidental shorting of the power busses or any other situation where excessive current might be drawn.

If the +5V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If the +5V fuse opens, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section of this manual.

LEDs

The following LEDs are visible at the top of the VX4790A Module's front panel to indicate the status of the module's operation:

Power LED
This green LED is normally lit and is extinguished if the +5V, ±24V (including the derived internal ±17.5V supplies), or -5.2V power supplies fail, or if the +5V, ±24V, or -5.2V fuses blow.

Failed LED
This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete a self test, loss of a power rail, or failure of the module's central processor.

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NOTE:

If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL asserted. A module power failure is indicated when the module's Power LED is extinguished.*

MSG LED
This green LED is normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

ERR LED
When lit, this LED indicates that the module has detected an error condition.

FHS LED
When lit, the Fast Handshake LED indicates the module is in the fast handshake mode of operation. This occurs during Buffered mode, binary download, and readback.

RUN LED
When lit, the Run LED indicates the ARB memory is actively transmitting.

BKPT LED
This green LED is lit when the ARB memory breakpoint is active.

XCLK LED
A lit LED indicates that an external clock input is enabled.

XTRG LED
An active external trigger input is indicated by the XTRG LED being lit.

LCK LED
When this LED is lit constantly, it indicates that the phase lock loop is in a lock condition. If the LED is flashing, this indicates that the phase lock loop is not locked and selected ARB sample periods or frequencies will not be correct if run.

SMB Connector Inputs and Outputs

Six SMB connectors provide the External Trigger Input, External Clock (sample rate) Input, External Reference Input, Sync Output, Sample Clock Output and Arbitrary Waveform Output signals. See Appendix B for a detailed description of these signals.

BITE (Built-In Test Equipment

The VX4790A Module has a self test mode that tests memory, outputs test waveforms, and verifies the correct voltage level and frequency by means of an on-

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board eight bit analog to digital converter and an on-board frequency detection device. The output is disconnected from the connector output during the self test.

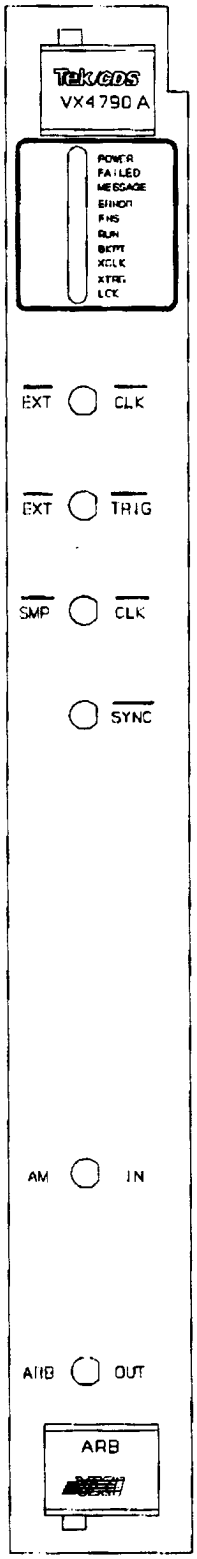


Figure 2: VX4790A Front Panel

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Specifications

Number of Channels:	Single channel.
Amplitude Resolution:	12 bits (4,096 vertical samples). A 12-bit attenuator improves effective waveform resolution to significantly more than 12 bits.
Waveform Memory:	262,144 16-bit memory locations (horizontal samples). Option 01: 524,288 16-bit memory locations. Option 02: 1,048,576 16-bit memory locations.
Memory-Update Capability:	Random-access update of any point in waveform memory. Automatic increment of address for sequential memory points.
Waveform-Repeat Capability:	Waveform programmable for a repeat count of 1 through 255 times, or continuous.
Output Amplitude:	±10.22 V dc maximum into a 50-Ohm load, programmable in 5 mV steps. ±5.11 V dc into a 50-Ohm load, programmable in 2.5 mV steps. ±0.1 V dc into a 50-Ohm load, programmable in 50 uV steps.
Output Source Impedance:	50 Ohm ±5.11 dc range and ±0.1 V dc range. 5 Ohm, ±10.22 V dc range.
Sample Output Accuracy:	
dc Accuracy:	(includes gain, offset, and non-linearity errors) ±0.4% of full scale in 5 V range into 50 ohms. ±1% of full scale in 10 V range into 50 ohms. ±1.7% of full scale in 0.1 V range into 50 ohms.
Non-linearity:	0.15% of full scale in 5 V range into 50 ohms. 0.20% of full scale in 10 V range into 50 ohms. 0.40% of full scale in 0.1 V range into 50 ohms.
Differential Non-linearity:	± ½ bit (within any range, assuming 12 bit resolution).
dc Temp. Drift:	±0.03%/°C of full scale.
Warmup Time:	10 minutes to dc accuracy.
Settling Time: (full scale, 5 V range)	175 ns (to dc accuracy). 115 ns (to 1.5% accuracy).

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Output Current:	200 mA, maximum. Short circuit protected.
Attenuator (Internal):	
Resolution:	12 bits, programmable.
Non-linearity:	±0.6% of full scale.
Differential Non-linearity:	± ½ bit (equivalent to ±1.25 mV for a 10 V programmed output; ±0.625 mV for a 5 V output).
Attenuator (External):	
Modulation Bandwidth:	9 KHz (3 dB), 18 KHz (6 dB).
Range:	0 to 100% (-1.5 V to +1.5 V dc input).
DC Accuracy:	±2.5%.
Output Filter:	User programmable: 5 MHz, 500 KHz, and 50 KHz low pass filters (-3dB).
Programmable Sample Rates:	25 MHz to 0.8 Hz, programmable as a six significant digit frequency or period.
Frequency Accuracy:	Programmed with a value of three significant digits: 0.005% (0°C to 50°C). Programmed with a value of four or more significant digits: 0.025% worst case (0°C to 50°C). (See Appendix E.)
Frequency Range:	0.75 Hz to 25 MHz.
External Clock Input:	User-supplied, 0 Hz to 25 MHz, TTL-compatible signal. Minimum clock duration: Clock high - 18 ns. Clock low - 18 ns.
Waveform Triggering:	Triggering under program control, or with external trigger.
External Trigger Input:	Enabled or disabled under program control.
External Trigger Input:	User-supplied, active-low, TTL-compatible pulse, negative edge triggered. Minimum pulse width: 160 ns. The waveform starts within 200 nsec. of the trigger.
Breakpoint Capability:	Any points in a waveform, except the first sample point in the waveform or any two sequential sample points, can be programmed to pause transmission until the module is retriggered (by hardware or software trigger).

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Interrupt Capability:	Programmable interrupt at end of transmission, on breakpoint(s) or any combination.
Power-up Default Programming:	Sampling Frequency - 25 MHz. Voltage Waveform - 0 V dc waveform. Isolation Relay - Output Disconnected. Repeat Count - Continuous. External Trigger - Disabled. Interrupts - Disabled. Low Pass Filter - Disabled. Memory Edit Address - 0. Attenuator - Disabled. External Attenuator - Disabled. Voltage Range - ± 10 Volts. Error Status - Result of self test. Output State - Not triggered. Paging - Set to 0, reset.
Auxiliary I/O Capability:	End-of-waveform output or user programmed sync output. External attenuation input. External clock input. External trigger input.
Auxiliary Outputs:	Advanced Schottky-TTL drive, 40 standard TTL loads.
Auxiliary Inputs:	Advanced Schottky-TTL load, 0.3 standard TTL load.
VXIbus Compatibility:	Fully compatible with the VXIbus Specification for message-based instruments.
VXI Device Type:	VXI message based instrument, Revision 1.4.
VXI Protocol:	Word serial.
VXI Module Size:	C size, one slot wide.
Module-Specific Commands:	All module-specific commands and data are sent via the VXIbus Byte Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.
VMEbus Interface:	Data transfer bus (DTB) slave - A16, D16 only.
Interrupt Level:	Switch selectable, levels 1 (highest priority) through 7 (lowest).
Interrupt Acknowledge:	D16, lower 8 bits returned are the logical address of the module.

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VXIbus Data Rate:

Buffered mode write: 200 Kbytes/sec maximum.
Nonbuffered mode write: 20 Kbytes/sec maximum.
Binary mode write, VXIbus fast handshake: 500 Kbytes/sec. in non-buffered mode.

VXIbus TTLTRG Support:

Any of the eight VXIbus TTLTRG lines may be program selected as the VX4790A sample clock source (limited to 12.5 MHz operation), or as the External Trigger source.

Any of the eight VXIbus TTLTRG lines may be driven under program control by the front panel External Clock Input or the front panel External Trigger Input.

VXIbus Commands Supported:

All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an unrecognized command error:

- BEGIN NORMAL OPERATION
- BYTE AVAILABLE (with or without END bit set)
- BYTE REQUEST
- CLEAR
- CLEAR LOCK
- IDENTIFY COMMANDER
- READ PROTOCOL
- READ STATUS
- SET LOCK
- TRIGGER

VXIbus Protocol Events Supported:

VXIbus events are returned via VME interrupts. The following events are supported and returned to the VX4790A Module's commander:

- UNRECOGNIZED VXIbus COMMAND
- REQUEST TRUE (In IEEE-488 systems, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)

VXIbus Registers:

ID
Device Type
Status
Control
Protocol
Response
Data Low
See Appendix A for definition of register contents.

Device Type Register Contents:

1111 0100 1110 1001 (F4E9h).

Power Requirements:

All required dc power is provided by the power supply in the VXIbus mainframe.

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Voltage:	+5 Volt Supply:	4.75 V dc to 5.25 V dc.
	+24 Volt Supply:	+23.5 V dc to +24.5 V dc.
	-24 Volt Supply:	-23.5 V dc to -24.5 V dc.
	-5.2 Volt Supply:	-4.75 V dc to -5.25 V dc.
Current (Peak Module, I_{PM}):	5 Volt supply:	4.1 A
	+24 Volt supply:	300 mA
	-24 Volt supply:	300 mA
	-5.2 Volt supply:	140 mA
Current (Dynamic Module, I_{DM}):	5 Volt supply:	563 mA @ 7 MHz
	+24 Volt supply:	538 mA @ 3 MHz
	-24 Volt supply:	202 mA @ 4 MHz
	-5.2 Volt supply:	450 mA @ 50 MHz

Fuses: Replacement fuses: Littlefuse P/N 273005 and Littlefuse P/N 273001 and Littlefuse P/N 273002

Cooling: Provided by the fan in the VXIbus mainframe. Less than 5°C temperature rise or less than 7°C rise with 1 channel at 150 mA output current with 2.85 l/s of air at a pressure drop of 0.067 mm of H_2O.

Temperature: 0°C to +50°C, operating.
-40°C to +85°C, storage.

Humidity: Less than 95% R.H. non-condensing, 0°C to +30°C.
Less than 75% R.H. non-condensing, +31°C to +40°C.
Less than 45% R.H. non-condensing, +41°C to +50°C.

Radiated Emissions: Complies with VXIbus Specification.

Conducted Emissions: Complies with VXIbus Specification.

Module Envelope Dimensions: VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in)

Dimensions, Shipping: When ordered with a Tektronix/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1 - 12).

When ordered alone, the module's shipping dimensions are:

406 mm x 305 mm x 102 mm.
(16 in x 12 in x 4 in).

Weight: 1.5 kg. (3.25 lb).

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Weight, Shipping:	When ordered with a Tektronix/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1-12). When ordered alone, the module's shipping weight is: 1.9 kg. (4.25 lb).
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connectors:	SMB connectors. Refer to Appendix B for connector pinouts.
Equipment Supplied:	1 - VX4790A Module. 1 - VX1729 Data Cable.
Options:	Option 1M - provides MATE capability. Option 01: 524,288 16-bit memory locations. Option 02: 1,048,576 16-bit memory locations.
Software Revision:	V3.9

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Section 2
Preparation For Use

Installation Requirements And Cautions

The VX4790A Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's Logical Address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the VX4790A Module's logical address. To avoid confusion, it is recommended that the slot number and the logical address be the same.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

CAUTION

Note that there are two ejector handles on the module. To avoid installing the module incorrectly, make sure the ejector labeled "VX4790A" is at the top.

In order to maintain proper mainframe cooling, unused mainframe slots must be covered with blank front panels supplied by the mainframe manufacturer.

Based on the number of IAC Modules ordered with a Tektronix/CDS mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot blank front panels can be ordered from your Tektronix supplier.

CAUTION

Verify that the mainframe is able to provide adequate cooling and power for the VX4790A Module. Refer to the mainframe Operating Manual for instructions on determining cooling and power compatibility.

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CAUTION

If the VX4790A Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VX4790A Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.

Installation Procedure

CAUTION

The VX4790A Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the module's revision level, serial number (located on the label on the top shield of the VX4790A), and switch settings on the Installation Checklist. Only qualified personnel should install the VX4790A Module.

2) Verify that the Logical Address and Interrupt Level switches are switched to the correct values.

3) The module can now be inserted into any slot of the chassis other than slot 0.

4) Installation of Cables -
Use a VX1729 Cable to interface between the module I/O connector and the Unit Under Test (UUT).

Calibration procedures are given in the Service Manual.

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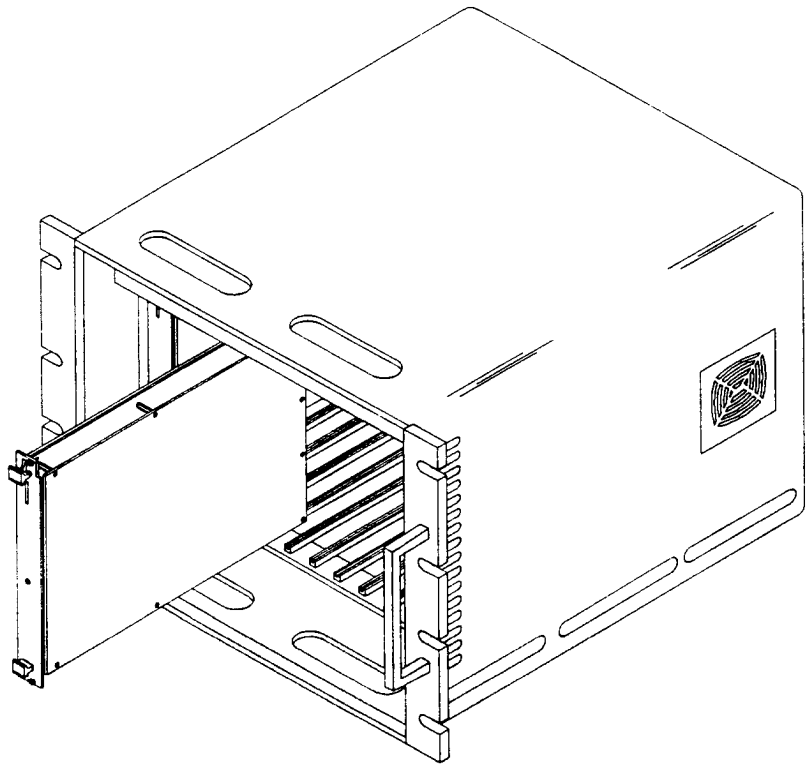


Figure 3: Module Installation

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Installation Checklist

Installation parameters may vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the VX4790A Module.

Revision Level: _____

Serial No.: _____

Mainframe Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Cable Installed:

VX1729 Cable: _____

Performed by: _____ Date: _____

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Section 3
Operation

Overview

The VX4790A generates user defined waveforms of up to 262,144 voltage samples (more are available with additional memory options) at sample rates of up to 25 MHz using either the internal clock or an external sample rate clock source. The ARB has sine, square, sawtooth, and triangular waveforms stored in internal memory, and can vary the output frequency and amplitude of a stored waveform without having to re-send that waveform from the system controller.

A series of low pass filters may be switched into the output under program control. Filters available include: 5 MHz low pass, 500 KHz low pass, and 50 KHz low pass. The effect of these filters on the output waveform is smoother transition between voltage steps, and reduced harmonics.

The ARB Module produces an analog output capable of driving a 50 Ohm load in three voltage ranges:

±10.22 Volts programmable in 5 milliVolt steps,
±5.11 Volts with a 2.5 milliVolt resolution, and
±0.1 Volts with a 50 microVolt resolution.

A programmable attenuator is provided which can reduce the programmed output voltage. The output value may be expressed as a percentage of full scale when programmed internally or varied based on an externally supplied reference. When the external reference input is selected, output level is set to 50% of full scale based on 0 volts at the reference input. Applying +1.5 volts to the external reference input will then set the output level to 100%, while -1.5 volts will set the output level to 0%. A varying signal of up to 1.5 V ptp may be applied for up to 99% AM modulation.

The VX4790A accepts programming in ASCII, binary, or CIIL (with Option 1M installed). The waveform can be programmed to repeat continuously or from one to 255 times. Programmable breakpoints may be entered at any non-consecutive sample points, except for the first voltage sample of the waveform. Retriggering can be done by software or by a TTL trigger from an external source. The steady state voltage to be output during a breakpoint (including at the end of a waveform) is also programmable.

The VX4790A Module is a VXIbus Message Based Device and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the VX4790A Module's commander for details on the operation of that device.

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Power-up

The VX4790A Module will complete its self test and be ready for programming five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay to this time. The Power LED will be on, and all other LEDs off. The MSG LED will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the mainframe.

System Commands

Although these non-data commands are initiated by the VX4790A's commander rather than the system controller, they have an effect on the VX4790A Module. The following VXIbus Instrument Protocol Commands will be accepted by the VX4790A:

Command	Effect
Clear	The module clears its VXIbus interface and any pending commands. Current module operations are unaffected.
Trigger	The ARB is triggered as if it were given a 1T command. (Refer to the T command in the Command Descriptions subsection.)
Begin Normal Operation	The module will begin operation per VXI Specification.
Read Protocol	The module will return its protocol to its commander.
Read Status	The module will return its status to its commander.
Byte Available	Transfers module commands to this module.
Byte Request	Requests data be returned from the module.
Identify Commander	No action taken.
Set Lock	No action taken.
Clear Lock	No action taken.

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Module Commands

A summary of the VX4790A Module's commands is listed below. The summary also shows any required order needed for commands. This is followed by detailed descriptions of each of the commands. A sample BASIC program using these commands is shown at the end of this section.

NOTE:

If Option 1M (MATE TMA) has been ordered with this module, see Appendix M for information on ATLAS/CIIL programming syntax. The commands listed in this section are not effective with the MATE option installed.

Command protocol and syntax for the VX4790A Module are as follows:

1) Each command consists of an ASCII character. Modifiers affecting the command are in the form of ASCII numbers preceding the letter command.

   <CR> indicates a carriage return.

   <LF> indicates a line feed.

   <TM> terminator: indicates a line feed or a semi-colon. Terminators are only required on multicharacter commands.

2) Any character may be sent in either upper or lower case form.

3) Any of the following white space characters have no effect on any of the commands, and any number of white space characters may be used together.

   00 hex
   01 hex through 08 hex
   09 hex (TAB character)
   0B hex through 19 hex (including carriage return)
   20 hex (SPACE character)

4) All numbers may be specified in integer or floating point notation, with or without exponent. Any number may be omitted on all single character commands, which assumes the default value of the number 0.

5) For the commands requiring addresses, the number can also be given enclosed by parenthesis (), and this module will interpret it in hexadecimal format. for example, the commands 65536N and (10000)N have the same meaning and are interpreted in exactly the same manner.

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Summary

Detailed descriptions of each command (in alphabetical order) are given following the summary. This summary lists the commands in the order they typically would be programmed.

SETUP COMMANDS

The setup commands program supplementary capabilities of the VX4790A and in many cases can be omitted. When required, they are typically defined prior to waveform generation definition.

C	Clock - programs the external clock input enable.
X	eXternal trigger - selects the external-trigger source (VXIbus TTLTRG lines or front panel).
U	User sync enable - selects the EOW (End Of Wave) bit or the programmed synchronization pulse for connection to the front panel Sync output.
I	Interrupt - programs the interrupt mode.
GETMASK?	Returns the programmed interrupt mode.
GOTOBUF	Enables input buffering.
GOTONBUF	Disables input buffering.
SETPAGE	Sets the memory page.
O	Output - controls the isolation relays on the ARB output. The O command can be issued just prior to triggering the waveform if it is necessary to keep the 0 V default waveform disconnected from the UUT during waveform definition.

PRE-PROGRAMMED WAVEFORM COMMANDS

The pre-programmed waveform commands provide easy generation of standard sine, square, triangle, and sawtooth waveforms. If arbitrary waveforms are desired, the Frequency, Voltage, and Arbitrary Waveform command sets described below must be used.

SETSINE	Programs a sine wave at a specified amplitude and frequency, about 0 Volts.
SETSINO	Programs a sine wave at a specified maximum amplitude, minimum amplitude and frequency.

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SETSQUARE	Programs a square wave at a specified amplitude and frequency.
SETTRIANG	Programs a triangle wave at a specified amplitude and frequency.
SETSAWTOO	Programs a sawtooth wave at a specified amplitude and frequency.

FREQUENCY COMMANDS

The frequency commands provide various methods of programming the sample clock frequency and the analog output filter setting.

F, P or D	F (Frequency), P (Period), or D (Divide) commands program the basic sample rate of the module.
SETDIV	Sets the sample clock divider without changing the frequency of the phase locked loop oscillator.
SETPLL	Sets the frequency of the phase locked loop oscillator without changing the sample clock divider.
GETFREQ?	Returns the actual frequency of the frequency source.
GETDIV?	Returns the setting of the sample clock divider.
GETPLL?	Returns the frequency of the sample clock's phase locked loop oscillator.
L	Low-pass filter command controls the filter on the analog output.

VOLTAGE/ATTENUATOR COMMANDS

The Voltage/Attenuator commands select the output range, program the on-module attenuator, or connect the front panel EXT REF input for external attenuation control.

SETVOLTR	Sets the output voltage range.
%	Percent attenuation command sets the output attenuation to be set on all programmed voltage outputs.
GETATT?	Returns the currently programmed attenuation value.
A	Enables or disables the external attenuator input.

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ARBITRARY WAVEFORM COMMANDS

The Arbitrary Waveform commands define unique waveforms, program the length of the defined waveform, and specify break-points and a front panel pulse output at specified points in the waveform.

V, B, W, or Z	Voltage - sequentially programs the arbitrary waveform voltages. The B, W, and Z commands are variations of the V command that program a breakpoint, end-of-waveform, or a breakpoint and end-of-waveform, respectively, in addition to the voltage sample.
Y	User sYnc - programs the programmed sync bit in the V, B, W, or Z commands.
GETDATA?	Returns ARB memory.
GETCODE?	Returns ARB memory, including sync, breakpoint, and end-of-wave codes.
#[n][m]	The # (Binary) command is described in Appendix D, Advanced Programming Capabilities. The Binary command programs the arbitrary-waveform voltage in binary and is used in place of the V command for high speed downloading of voltage values.
GETBIN?	Returns the values programmed in ARB memory in binary format.
R	Repeat - programs the number of times to repeat the waveform, or programs continuous transmission.
SCOPY	Copies one portion of waveform memory to another.
SFILL	Fills a block of waveform memory with the value in the first location of the block.
STARTBIN	Sets up the parameters for a binary load of waveform memory and puts the module into binary mode.

TRIGGER COMMANDS

The Trigger commands trigger and halt the waveform output.

T	Trigger - resets the memory to the first location and starts actual transmission of the programmed waveform, or retriggers the module when it is halted at a break-point.
Q	Quit - may be used to halt output of a waveform.

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WAVEFORM EDIT COMMANDS

The Waveform Edit commands permit changes to the waveform without requiring the complete waveform memory to be reloaded.

M Memory edit - allows random access to any location in the memory partition for updating any point(s) in the waveform with a subsequent V command. The M command can also be used to cause waveform output to begin at a memory location other than zero when a 1T Trigger command is issued.

N poiNter - moves the memory pointer to allow memory loads as in the M command, but does not move the counter pointer that directs the ARB memory. This allows the ARB memory to be programmed when the ARB is at a memory breakpoint, without changing the current memory pointer.

MISCELLANEOUS COMMANDS

The remaining commands provide a reset of the module or report the status of the module.

K Kill command resets the module to its power-up state.

SETDEF Sets the power up default values for the current memory page without resetting the settings for other memory pages.

? Status - reports the module's status and clears errors the module has detected.

GETERR? Reports any errors which may have occurred.

GETINT? Returns the status of any interrupts, regardless of whether or not they have been enabled.

GETMEM? Returns the amount of installed memory.

GETPAGE? Returns the current memory page.

GETREV? Returns the revision firmware number of the board.

SMEMTEST Starts the test of the entire installed waveform memory.

STEST Self test - runs the onboard self test to check the integrity of the ARB.

A detailed description of each command, in alphabetical order, is given on the following pages. Responses from the module are shown underlined.

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Command Descriptions

Command: A (Attenuator select)

Syntax: [z]A

Purpose: Selects the external attenuator reference input (AM IN).

Description: The A command enables or disables the external attenuator reference input as follows:

[z]	Description
0	external attenuator reference off
1	external attenuator reference on

When the external attenuator reference input is selected by sending the 1A command, the output amplitude of the waveform stored in memory is then affected by the voltage supplied to the AM IN input. If zero volts are applied to the AM IN input, the output will be 50% of the programmed waveform amplitude. If +1.5 volts is applied, the output signal would be 100% of the programmed voltage. A -1.5 Volt signal would attenuate the signal to 0% of the programmed voltage.

If the external attenuator reference is off, the waveform output will be attenuated as programmed by the % command.

The external attenuator reference input (AM IN) has a 3 dB bandwidth of 900 Hz and may be used to amplitude modulate the ARB output.

Example: 1A Enables the external attenuator reference (AM IN).

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Command: C (Internal Clock)

Syntax: [z]C

Purpose: The Clock command programs the clock source for the VX4790A Module and provides connections to allow a single clock source for multiple VX4790A Modules.

Description: The clock source may be selected from an internal clock, an external front panel sample rate clock, or any of the VXIbus TTLTRG inputs. The C command is also used to specify connection of a clock to any of the eight TTLTRG lines for use by another VXIbus module. If a C command is to be programmed, it should be the first command received by the module.

The source selected by the C command will remain unchanged when a Q (Quit) command is received by the module. The clock source is returned to internal by a K (Kill) command, or by a RESET command (see Appendix A).

The following table shows clock connections for various programmed values of [z]. The VX4790A Clock Source is the clock source for the VX4790A being programmed. Clock sources are the on-board 25 MHz internal clock, front panel EXT CLK IN connection, and the VXIbus TTLTRG lines. Additional connections permit a common clock source to be used in multiple modules in various configurations.

Selections 0 and 1 permit operation to 25 MHz. All other selections limit clock frequency to the VXIbus TTLTRG limit of 12.5 MHz.

A discussion of the various clock connections follows the table.

[z]	VX4790A Clock Source	Additional Front Panel or TTLTRG Connections
0	Internal 25 MHz Clock	None
1	Front panel Ext Clk	None (see the Note at the end of this list).
10	TTLTRG0*	Front panel External Clock In to TTLTRG0*.
11	TTLTRG1*	Front panel External Clock In to TTLTRG1*.
12	TTLTRG2*	Front panel External Clock In to TTLTRG2*.
13	TTLTRG3*	Front panel External Clock In to TTLTRG3*.
14	TTLTRG4*	Front panel External Clock In to TTLTRG4*.

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15	TTLTRG5*	Front panel External Clock In to TTLTRG5*.
16	TTLTRG6*	Front panel External Clock In to TTLTRG6*.
17	TTLTRG7*	Front panel External Clock In to TTLTRG7*.
20	TTLTRG0*	None
21	TTLTRG1*	None
22	TTLTRG2*	None
23	TTLTRG3*	None
24	TTLTRG4*	None
25	TTLTRG5*	None
26	TTLTRG6*	None
27	TTLTRG7*	None

NOTE: User cabling of front panel Sample Clock Out to front panel External Clock In is required for [z] = 30 through 37.

30	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG0*.
31	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG1*.
32	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG2*.
33	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG3*.
34	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG4*.
35	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG5*.
36	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG6*.
37	Internal 25 MHz Clock	Front panel External Clock Input to TTLTRG7*.

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NOTE: The External Clock input provides the sample clock input, and when selected (1C command), replaces the internally-generated sample clock. The ARB waveform will be output at the rate of the External Clock input, and is not affected by the Divide, Period, or Frequency (D, F, P) commands.

Clock selections 10 through 17 use the clock from the backplane TTLTRG line as this module's clock source. In addition, these selections connect this module's front panel External Clock Input to the same TTLTRG* line, permitting multiple modules to use this module's front panel clock source as their clock source via a TTLTRG line. Other modules wishing to use this clock source would program a clock selection of 20 to 27.

Clock selections 20 to 27 use the clock from the VXIbus backplane TTLTRG lines as this module's clock source.

Clock selections 30 through 37 allow use of the internal clock of this VX4790A Module to drive other modules. The module uses its own internal sample clock and by external connection of the module's front panel Sample Clock Output to its front panel External Clock Input, other modules may use this module's sample clock. The External Clock front panel input is connected internally on the module to the specified VXIbus TTLTRG line to provide this capability. This should be used for sample clocks of 12.5 MHz and less (see the F, P, or D commands for programming the sample clock rate).

Chaining the Sample Clock output of a 'master' VX4790A to the External Clock input of additional VX4790A Modules provides the capability of synchronizing waveforms from multiple ARBs. The sample clock rate from the 'master' is controlled by the Divide, Period, or Frequency (D, F, P) commands, and will affect the output frequency of all ARBs chained in this manner.

Example: 13C Connects the front panel external clock input to TTLTRG3* and uses the TTLTRG3* line for the external clock input for the ARB sample clock.

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Command: D (Divide)

Syntax: [z]D

Purpose: The D (Divide) command specifies the number of main clock divisions, or periods, in the output sample rate. The output sample rate is the time between successive output-voltage updates from the ARB Module's memory (40 ns per division for internal clock).

The D command is provided for programming compatibility with the 53A-243 CDSbus Arbitrary Waveform Generator Card. See the F or P command for direct programming of the frequency or period of the sample clock. See the SETDIV and SETPLL commands to individually set the internal clock and the divider.

Description: [z] is a 0- to 8-digit decimal number from 0 to 16,777,218 that specifies the number of divisions of the main clock rate. A 1D, 0D, or a D command all specify a 40 ns (25 MHz) clock rate. The command 123D sets a clock rate of 123 * 40 ns (equal to 4.92 microsecond) sample clock period (203.25203252 KHz sample clock).

On power-up, the value of the D command is set to 1 (a 40 ns or 25 MHz rate if internal clock is selected). The value of the D command is not altered by a Q (Quit) command sent to the module, but is reset to the power-up value by a K (Kill) command or a RESET command to the module (see Appendix A).

The F, P, and D commands are three different methods for programming the output sample rate clock. Only one of the three commands, or the SETSINE (or one of the other pre-programmed waveform commands) is required for programming the output rate of the module.

Example: 3D Programs a 120 ns clock for the ARB sample clock. The 120 ns clock period is equivalent to an 8.333... MHz sample clock rate.

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Command: F (Frequency)

Syntax: [z]F

Purpose: The F command is used to set the frequency of the VX4790A sample clock and also the Sample Clock Output connector on the front panel.

Description: [z] is the frequency in Hertz. It may be programmed as any valid floating point number with or without exponent, from 0.75 Hz to 25 MHz.

On power-up, the value of the F command is set to 25 MHz. The value of the F command is not altered by a Q (Quit) command, but is reset to the power-up value by a K (Kill) command, or by a VXI RESET command (see Appendix A for RESET command). Refer to Appendix E for details on the setting accuracy of the F command.

The F, P, and D commands are three different methods for programming the output sample rate clock. Only one of the three commands, or the SETSINE (or one of the other pre-programmed waveform commands) is required for programming the output rate of the module.

Example: 6.125e6F Programs the sample clock to a 6.125 MHz clock rate.

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Command: GETATT?

Syntax: GETATT?<TM>

Purpose: The GETATT? command returns the currently programmed attenuation value.

Description: This command is used to return the currently programmed attenuation value, programmed by the %, SETSINE, SETSAWTOO, SETSQUARE, or SETTRIANG commands.

Example:
96.9%
GETATT?<TM>

96.90%<CR><LF> (response)

The 96.9% programs the attenuator at 96.9% of full scale. The GETATT? command queries the VX4790A Module for the currently programmed attenuation value. The returned response of 96.9% verifies the attenuation value just programmed.

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Command: GETBIN?

Syntax: GETBIN? [n]<TM>

Purpose: This command returns the values programmed in ARB memory, starting from location [n], in binary format.

Description: [n] specifies the memory location. If [n] is omitted, 0 will be assumed.

The GETBIN? command returns the values programmed into the ARB memory in binary format. Each 16-bit binary value is returned as four hexadecimal characters. Eight values per line are returned, separated by a space character and terminated with a <CR><LF>. Any number of lines may be read, each line returning the next eight memory locations. When the end of the available memory locations is reached, the word "END" will be returned. All subsequent unrequested reads will return data points until a GETDATA?, GETCODE?, or ? command is executed.

NOTE: This command will terminate any waveform output. This command is only active on the currently selected page. Refer to SETPAGE and GETPAGE? commands.

The 12-bit voltage value is returned as the twelve lower bits, bits 11 through 0. The breakpoint, sync and end-of-wave codes are returned in the top four bits of the data. The sync bit is bit 14, breakpoint, bit 13, and end-of-wave bit, bit 12. Bit 15 is unused and is set to 0.

Bit ordering within the four-character hexadecimal value is as follows. The first character returned contains bits 15 to 12, the most significant bit being bit 15. The second character contains bit 11 to bit 8, the third character bit 7 to bit 4, and the final character contains bit 3 to bit 0.

The 12 bits representing the voltage values are encoded in binary. Representative values for bits 11 to 0 are:

Bit 11 ... Bit 0	Hex	Actual Voltage 5 V Range	Actual Voltage 10 V Range
0 0 0 0 0 0 0 0 0 0 0 0	000	-5.12 V	-10.24 V
0 1 1 1 1 1 1 1 1 1 1 1	7FF	-0.0025 V	-0.005 V
1 0 0 0 0 0 0 0 0 0 0 0	800	0 V	0 V
1 1 1 1 1 1 1 1 1 1 1 1	FFF	+5.1175 V	+10.235 V

The following conversion formulas may be used to convert the 3-character hexadecimal value for the 5 V and 10 V range:

If the three least significant characters are h_2, h_1, and h_0, then the voltage for the 5 V range is:

$$\text{Voltage} = [(256 * h_2) + (16 * h_1) + (h_0 - 2048)] * 5.12 / 2048$$

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For the 10 V range:

$$\text{Voltage} = [(256 * h_2) + (16 * h_1) + (h_0 - 2048)] * 10.24 / 2048$$

For these formulas, use values of 10, 11, 12, 13, 14 and 15 for the hexadecimal characters A, B, C, D, E, and F in h_2, h_1, and h_0.

Use the GETCODE? command to return the values in volts with breakpoint, sync, and end-of-wave codes, and use GETDATA? to return the data in volts, without codes.

Example: If the following were programmed:

```
SETVOLTR 10<CR><LF>
0N 0V .1B .2V .3YB .4V .5YV .6V .7Z .8V .9YZ 1V 1.1W 0V 0V 0V 0V;
GETBIN?;
```

the response would be:

```
0800 2814 0828 683C 0850 4864 0878 388C <CR><LF>
08A0 78B4 08C8 18DC 0800 0800 0800 0800 <CR><LF>
```

The SETVOLTR command sets the voltage range to 10 volts. 0N sets the address pointer for the ARB memory to 0. The next 16 character groups program 16 locations of ARB waveform, some with just voltage values, others with breakpoints and sync outputs, and the twelfth location with an end-of-wave.

The GETBIN? command queries the VX4790A for a response in binary format reporting the memory contents. The response is returned as two lines, each line reporting the contents of eight locations of ARB memory data. The fourth value returned, 683C, is evaluated as an example to verify that it agrees with what was programmed:

The first character, 6, indicates the state of the sync bit, the breakpoint bit, and the end-of-wave bit. A value of 6 indicates that bits 14 and 13 are set, and bit 12 is clear. Bit 14 and bit 13 indicate that the sync and breakpoint bits are set, which agrees with the YB characters programmed by the fourth location programming of .3YB.

The 83C characters will be substituted in the formula for voltage for the 10 Volt range:

$$\text{Voltage} = [(256 * 8) + (16 * 3) + (12 - 2048)] * 10.24 / 2048$$
$$= 60 * 10.24 / 2048 = 0.300$$

which agrees with the 0.3 volts programmed.

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Command: GETCODE?

Syntax: GETCODE? [n]<TM>

Purpose: This command returns the values programmed in ARB memory starting from location [n].

Description: [n] specifies the memory location. If [n] is omitted, 0 will be assumed.

The GETCODE? command returns the values programmed in ARB memory, starting from location [n], with breakpoint, sync, and end-of-wave codes. The values returned are in volts, four values per line. Any number of lines may be read, each line returning the next four memory locations. When the end of the available memory locations is reached, the word "END" will be returned. All subsequent unrequested reads will return pending errors until a GETBIN?, GETDATA?, or ? command is executed.

NOTE: This command will terminate any waveform output. This command is only active on the currently selected page. Refer to SETPAGE and GETPAGE? commands.

Breakpoint, sync and end-of-wave codes are returned with each value. The codes are B for breakpoint, W for end of wave, Z for breakpoint and end of wave. A Y code follows the above code to represent the sync bit.

Use the GETDATA? command to return the values without the codes, and GETBIN? to return the data in binary format.

Example: If the following were programmed:

```
SETVOLTR 10;
ON 0V .1B .2V .3YB .4V .5YV .6V .7Z .8V .9YZ 1V 1.1W;
```

then GETCODE?; would return:

```
0.000,   0.100B,  0.200,   0.300BY,<CR><LF>
0.400,   0.500Y,  0.600,   0.700Z, <CR><LF>
0.800,   0.900ZY, 1.000,   1.100W, <CR><LF>
```

The above values are returned in a 43 character field. The four values may be acquired from the string with a MID$ string function starting in columns 1, 12, 23, and 34 and a string length of seven. The breakpoint, sync, and end-of-wave codes (if present) start in columns 8, 19, 30, and 41.

If the 0.1 Volt range is selected (Option 01), the field is 47 characters in length, and the voltage values are eight characters each, starting in columns 1, 13, 25, and 36.

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Command: GETDATA?

Syntax: GETDATA? [n]<TM>

Purpose: This command returns the values programmed in ARB memory, starting from location [n], in volts.

Description: [n] specifies the memory location. If [n] is omitted, 0 will be assumed.

The values returned are in volts, four values per line. Any number of lines may be read, each line returning the next four memory locations. When the end of the available memory locations is reached, the word "END" will be returned. All subsequent unrequested reads will return pending errors until a GETBIN?, GETCODE?, or ? command is executed.

NOTE: This command will terminate any waveform output. This command is only active on the currently selected page. Refer to SETPAGE and GETPAGE? commands.

Use the GETCODE? command to return the values with the breakpoint, sync and end-of-wave codes, and GETBIN? to return the data in binary format.

Example: If the following were programmed:

```
SETVOLTR 10;
0N 0V .1B .2V .3YB .4V .5YV .6V .7Z .8V .9YZ 1V 1.1W;
```

then GETDATA?; would return:

```
0.000,   0.100,   0.200,   0.300,  <CR><LF>
0.400,   0.500,   0.600,   0.700,  <CR><LF>
0.800,   0.900,   1.000,   1.100,  <CR><LF>
```

The above values are returned in a 43-character field. The four values may be acquired from the string with a MID$ string function starting in columns 1, 12, 23, and 34 and a string length of seven.

If the 0.1 Volt range is selected (Option 01), the field is 47 characters in length, and the voltage values are 8 characters each, starting in columns 1, 13, 25, and 36.

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Command: GETDIV?

Syntax: GETDIV?<TM>

Purpose: The GETDIV? query returns the setting of the sample clock divider.

Description: The GETDIV? query is used to determine the setting of the divider that makes up the sample clock frequency. The sample clock frequency is the phase locked loop frequency divided by the divider. See the GETPLL? query to determine the phase locked loop frequency. See the GETFREQ? query to determine the sample clock frequency.

Example:
SETDIV 5<TM>
GETDIV?<TM>
Response data: 5<CR><LF>

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Command: GETERR? (Error Reporting)

Syntax: GETERR?<TM>

Purpose: The GETERR? command instructs the ARB module to return its error status the next time input is requested from the module.

Description: Errors reported by this command include those detected during self test.

All errors listed in this section cause a Request True interrupt to be generated (if interrupts are enabled via the I command), and the ERR LED to be lit.

All errors occurring since the last GETERR? command or reset condition will be returned, beginning with the first error found. After issuing the GETERR? command to the VX4790A Module, the system controller should continue to request input from the module until the "No additional errors to report" message is returned from the module. This insures that the error buffer is empty. The ERR LED will go out when the last error is read.

Response Syntax:

The format of data returned by the ERR? command is:

[error],[english message]<CR><LF>

where:

[error] is a 2-digit error code.

[english message] is an English message describing the error.

Examples: The two-digit error codes, their message, and meaning are as follows:

00,NO ADDITIONAL ERRORS TO REPORT

There are no more errors to report.

10,RAM ERROR

This indicates that the Random Access Memory (RAM) required for the operation of this instrument does not function properly. This RAM should not be confused with the ARB RAM. The VXI interface on the VX4790A has been designed to operate and communicate with the system controller even with no operational RAM onboard. Instrument operation will be unpredictable in this case, until the RAM or its control circuitry is fixed or replaced.

11,SELF TEST FAILURE: ARB RAM: ADDR <HEX4>, WROTE <HEX2>, READ <HEX2>

This indicates that the ARB RAM does not function properly. The bad address (returned as 4 hex digits), the value written to it (returned as 2 hex

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digits), and the value read from this location (returned as 2 hex digits) are included in the message.

12,SELF TEST FAILURE: FREQUENCY
The frequency test described under the STEST command has failed, although there were transitions of the test waveform.

13,SELF TEST FAILURE: NO CLOCK
The test waveform is remaining at a steady voltage level.

14,SELF TEST FAILURE: DELAYED TRIGGER
The frequency test described under the STEST command passed, but only after waiting over 200 µsecs for the ARB to trigger. This indicates a problem with the trigger circuit.

15,SELF TEST FAILURE: AMPLITUDE: PROGRAMMED <VOLTS>V, READ <VOLTS>V
The ARB voltage self test returned an incorrect voltage level. If the READ value is approximately 0 volts, this could indicate a problem in the triggering circuitry.

16,SELF TEST FAILURE: SELF TEST A/D INOPERATIONAL
The A/D used during the amplitude portion of the self test is not operational.

20,VOLTAGE OUT OF RANGE
The voltage value sent is too large for the current voltage range.

21,PERCENT VALUE TOO LARGE
The value sent with the % command was over 100%.

22,DIVIDE COUNT TOO LARGE
The programmed divide count (D command) was more than 16,777,218.

24,FREQUENCY UNDERRANGE
The programmed frequency resulted in an attempt to program the sample clock to below 0.75Hz.

25,FREQUENCY OVERRANGE
The programmed frequency resulted in an attempt to program the sample clock to more than 25MHz.

26,PERIOD UNDERRANGE
The programmed period resulted in a sample clock with a period below 40ns.

27,PERIOD OVERRANGE
The programmed period resulted in a sample clock with a period greater than 1.3333 seconds.

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30,INVALID <COMMAND> OPTION <VALUE>
A number <VALUE> sent with the <COMMAND> command is invalid for this command.

31,INVALID VOLTAGE RANGE
The specified voltage range (SETVOLTR command) must be 10, 5, or 0.1.

32,INVALID VALUE FOR REPEAT COUNT: <VALUE>
Invalid repeat count was received. Valid repeat count values are 0 through 255.

40,UNRECOGNIZED COMMAND
The received command was unrecognized.

41,RECEIVED UNEXPECTED <CHAR> WHILE <REASON>
<CHAR> = <single quote><character><single quote> for printable characters (20 hex through 7f hex), for example 'G'.
or
<CHAR> = <SP><ASCII hex digit><ASCII hex digit> for non-printable characters (00 hex through 19 hex and 80 hex through FF hex), for example, 0A.

<REASON> = one of the following:
- EXPECTING A LINE FEED, SEMICOLON OR COMMA.
- EXPECTING A NUMERIC.
- PARSING MANTISSA.
- PARSING EXPONENT.

42,TOO MANY DIGITS IN EXPONENT
More than 3 digits were received in an exponent.

43,HEX VALUE NOT ALLOWED
A hex value (a number with parenthesis around it) was sent to a command that does not support it (D, F, and P commands).

44,MEMORY VALUE OUT OF RANGE
The memory value given is higher than the available memory. This error is generated by functions that require an address input.

45,OVERFLOW OF AVAILABLE MEMORY
An attempt was made to write beyond available memory. This error is generated when the SFILL, SCOPY, or V commands attempt to write waveform points past the end of available memory.

46,PAGE VALUE OUT OF RANGE
An attempt was made to access a memory page higher than can be supported by the installed memory or 16, whichever is higher.

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47,ARB RAM TEST FAILURE: BLOCK n, ADDR <HEX4> H, WROTE <HEX2> H, READ <HEX2> H

This message is generated by the SMEMTEST command when the waveform memory does not function properly. See the SMEMTEST command for the meaning of the failure message.

48,LENGTH OUT OF RANGE

The count length supplied to the STARTBIN command would cause data to be loaded beyond the end of available memory.

49,FUNCTION NOT SUPPORTED WITH CIIL OPTION

An attempt was made to use a function with the CIIL option that is only available in the commercial option.

50,FUNCTION NOT SUPPORTED IN COMMERCIAL VERSION

An attempt was made to use a function with the commercial version that is only available with the CIIL option.

99,TOO MANY ERRORS

More error messages have occurred since the last GETERR? command, than can fit in the VX4790A's output buffer.

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Command: GETFREQ?

Syntax: GETFREQ?<TM>

Purpose: The GETFREQ? command returns the actual frequency of the sample clock.

Description: The GETFREQ? command is used to return the actual frequency that the sample clock was programmed to. This is typically used after a F, P, or D command, to find what the actual programmed frequency was, as compared to the requested frequency. For most cases, the difference will be less than the crystal accuracy. Refer to Appendix E, on Frequency Source Accuracy.

Example:

```
7.777F
GETFREQ?
```

would return:

```
7.7770004 HZ<CR><LF>
```


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Command: GETINT?

Syntax: GETINT?<TM>

Purpose: This command is used to return the status of any interrupts.

Description: This command returns the same information as the VXI Read Status command (serial poll on IEEE-488 systems) except the bits are not cleared as they are when performing the VXIbus Read Status command.

The value is returned as a 1-byte ASCII hexadecimal character followed by a <CR><LF>. The value, as for the I command, is the sum of the following values:

Partial Value	Interrupt Type
1	Breakpoint has occurred
2	End of Transmission has occurred
4	Memory access error has occurred
8	Command syntax or self test error has occurred.

The interrupt state of any of the above conditions will be returned whether or not the interrupt type has been enabled. (Enabling the interrupt also permits a VXIbus interrupt to the ARB module's commands to be generated.)

A more detailed description of the interrupt types is given in the I command description.

Example: GETINT?<TM>

A response value of 5<CR><LF>
indicates that both a breakpoint and a memory access error have occurred.

A response value of A<CR><LF>
indicates that a command syntax of self test error has occurred, and an End of Transmission has occurred.

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Command: GETMASK?

Syntax: GETMASK?<TM>

Purpose: This command returns the interrupt mask as programmed by the I command.

Description: The value is returned as a 1-byte ASCII hexadecimal character followed by a <CR><LF>. The value, as for the I command, is the sum of the following values:

Partial Value	Interrupt Type
1	Breakpoint has occurred
2	End of Transmission has occurred
4	Memory access error has occurred
8	Command syntax or self test error has occurred.

A more detailed description of the interrupt types is given in the I command description.

Examples: 7I
GETMASK?<TM>
Response data: 7<CR><LF> would be returned.

12I
GETMASK?<TM>
Response data: C<CR><LF> would be returned, indicating that the memory access error interrupt and command syntax or self test error interrupts were enabled by the 12I command string.

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Command: GETMEM?

Syntax: GETMEM?<TM>

Purpose: The GETMEM? query returns the amount of installed memory.

Description: The GETMEM? query is used to determine the amount of installed memory. The module determines installed memory at power-up or reset. If there is a discrepancy between the amount of memory physically installed and the value returned by this query, then there is probably a hardware error and the module needs to be serviced.

The value returned by this command is the maximum available memory when the memory page is set to zero. Subtracting one from this value will give the highest valid address for commands requiring address input.

Example: GETMEM?<TM>
Response data: 262144<CR><LF> would be returned from a module with 256k of installed waveform memory. The actual value returned will depend on how much memory is actually installed.

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Command: GETPAGE?

Syntax: GETPAGE?<TM>

Purpose: The GETPAGE? query returns the current memory page.

Description: The GETPAGE? query is used to determine which memory page is currently being used. See the SETPAGE command for a description of memory pages.

Example:
SETPAGE 3<TM>
GETPAGE?<TM>
Response data: 3<CR><LF>

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Command: GETPLL?

Syntax: GETPLL?<TM>

Purpose: The GETPLL? query returns the frequency of the sample clock's phase locked loop oscillator.

Description: The GETPLL? query is used to determine the frequency of the phase locked loop that along with the divider makes up the sample clock frequency. The sample clock frequency is the phase locked loop frequency divided by the divider. See the GETDIV? query to determine the divider setting and the GETFREQ? query to determine the sample clock frequency.

Example:
SETPLL 16500000<TM>
GETPLL?<TM>
Response data: 16500000<CR><LF>

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Command: GETREV?

Syntax: GETREV?<TM>

Purpose: Returns the revision number of the module firmware.

Description: This command returns the revision level of the onboard firmware as an alphanumeric string.

Example: GETREV?<TM>

Response Syntax: An example of a typical response is:

REVISION 1.0<CR><LF>

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Command: GOTOBUF

Syntax: GOTOBUF<TM>

Purpose: Enables the 16 Kbyte input buffer. The command allows the system controller to send data and commands to the VX4790A over the VXIbus at optimum speed, independent of the parsing and execution speed of this module.

Description: In the buffered mode, all data sent to the module is buffered before being parsed, allowing much faster transfer rates. This module operates using the VXIbus Fast Handshake mode while in buffered mode. See the Synchronizing Multiple Instrumentation Modules section for details on synchronizing multiple modules used in the buffered mode.

NOTE: The following discussion applies only to users planning on sending extremely large amounts of data in a very short period of time (roughly more than 3000 V, B, W, or Z commands within a second).

If more than 8000 bytes of data are sent to the module in under 400 milliseconds (which roughly corresponds to 100 µs/character, or 3000 V, B, W, or Z commands per second), the data will be received faster than the module's parser is able to process the characters, and eventually the module's 16384 byte buffer will fill up. This will cause a temporary VXIbus hold off condition, which is transparent except for the effect it has on data transfer speed. If the system controller is slower than the module's parser rate, as many are, this hold off condition would never be encountered.

When the hold off situation occurs, the VX4790A will not allow the VXIbus system controller to send any additional data until the parser has emptied half of its input buffer.

As an example, the first time the 16384 byte buffer is filled, the system controller will be held off until the first 8192 bytes are parsed. From this point on, every time the module releases the hold off condition, the controller may send another 8192 bytes, at which time it has to wait on the parser again. Care must be taken not to set the timeout variable available in most controllers to too small a value in these applications.

Each character sent takes up one byte in the module input buffer unless the END bit is set (EOI for IEEE-488), in which case it takes up three bytes. All VXIbus commands (i.e. Trigger, Set Lock) take up three bytes. Refer to the VX4790A commander's manual for information on generation of VXIbus commands.

Example: GOTOBUF<TM>

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Command: GOTONBUF

Syntax: GOTONBUF<TM>

Purpose: Disables the input buffer. The command puts the module into the nonbuffered mode of operation.

Description: In the nonbuffered mode, a byte of command/data is not accepted from the VXIbus until the previous character has been processed. By using this mode, the VX4790A maintains synchronization with its commander.

The major advantage of this method is that another module which may use the output of the VX4790A can immediately be programmed after the VX4790A and be assured that the output of the VX4790A is valid. Consult the Synchronizing Multiple Instrumentation Modules section for more details.

NOTE: The following paragraph only applies to the programmer who will be switching back and forth between buffered and nonbuffered mode.

It is important to note that since this command may be received while the module is in the Buffered mode, it will not take effect until the processor has parsed it (receiving characters and processing them occur independently in buffered mode). To guarantee that the module is actually in Nonbuffered mode before executing another command, a query command (any command ending in a question mark) may be sent to the VX4790A after the GOTONBUF command and the result read. This will re-synchronize the module and the controller, since the response to the query is not returned until both the GOTONBUF and ERR? commands (for example) have been processed.

Example: GOTONBUF<TM>

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Command: I (Interrupt)

Syntax: [z]I

Purpose: The I (Interrupt) command enables or disables generation of VXIbus interrupts by the ARB Module.

Description: [z] is a 1- to 2-digit decimal number that defines which interrupts are enabled. The number consists of the summed value of the following values. A value of 3, for example, enables the breakpoint and end of transmission interrupts; all other interrupts will be disabled.

[z]	Interrupt Condition
0	Interrupts disabled.
1	Breakpoint interrupts enabled. An interrupt is generated whenever a breakpoint occurs, as programmed by the B or Z commands.
2	End-of-transmission interrupts enabled. A single interrupt is generated at the completion of the total programmed waveform after the specified number of repeats has occurred.
4	Memory error interrupts enabled. An interrupt is generated whenever an attempt is made to read or write the ARB memory or reload the address counter while ARB is running. If a write was attempted during this time, the memory location will not have been updated.
8	Command interrupt enabled. An interrupt is generated if there is an error in the command sent or during self test. The specific reason for the interrupt can be determined with the GETERR? command.

The occurrence of any of the above interrupt conditions is latched by the ARB Module, whether or not enabled by the I command. The resulting state can be read with a GETINT? command or a VXIbus Read Status command (which occurs on a serial poll on IEEE-488 systems). The VXIbus Read Status command is required to clear the interrupt latch; GETINT? does not clear the interrupt latch. Enabling an interrupt condition by the I command permits generation of a VXIbus interrupt in addition to the reporting.

The Interrupt Mode will remain at the last programmed state unless power is cycled, a RESET input is sent to the module (see Appendix A), or a K (Kill) command is programmed, in which case all interrupts are disabled.

Example: 15I If all interrupt types are to be enabled, a value of 15 (the sum of 1, 2, 4, and 8) is sent to the module.

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Command: K (Kill)

Syntax: K

Purpose: The K (Kill) command returns the module to its power-up state.

Description: On receipt of the K command, the module is returned to its power-up state with all parameters at the default settings:

Sampling Frequency	25 MHz
Voltage Waveform	0 V dc waveform
Repeat Count	Continuous
External Trigger	Disabled
Interrupt	Disabled
Low Pass Filter	Disabled
Attenuator (external)	Disabled
Attenuator (percent)	100% of programmed voltage will be output
Isolation Relay	Output is disconnected
Memory Edit Address	0
External Trigger Source	Front panel
Front Panel Sync Output	End-of-wave selected
Input Buffer	Disabled
Error Status	Cleared
Output State	Not triggered
Clock Source	Internal
Period	40 ns
Query Mode	Returns errors (GETERR? command)
* Paging	Page set to 0 and page settings reset

The contents of memory are programmed with a value of 0 V dc in the first two locations with an end-of-waveform indication in the second. The remainder of memory is unchanged.

* See the SETDEF command to reset the module to the above parameters without resetting the pages.

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Command: L (Low Pass Filter)

Syntax: [z]L

Purpose: The L (Low Pass Filter) command enables or disables the low pass filters on the output of the Arbitrary Waveform Generator.

Description: z is a single digit which specifies:

z	Effect
0	5 MHz Low pass filter switched off.
1	5 MHz Low pass filter switched on.
2	500 KHz Low pass filter switched off.
3	500 KHz Low pass filter switched on.
4	50 KHz Low pass filter switched off.
5	50 KHz Low pass filter switched on.
6	All filters switched off.

Any one or combination of the filters can be selected. The filters smooth voltage steps, but also limit the output slew rate.

On power-up, the low pass filters are switched off. The value of the L command is not altered by a Q (Quit) command, but is reset to the power-up value by a K (Kill) command, or by a RESET command (see Appendix A for RESET command).

Example: 2L switches off the 500 KHz low pass filter.

3L;4L switches the 500 KHz filter on, and the 50 KHz filter off.

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Command: M (Memory Edit)

Syntax: [z]M

Purpose: The M (Memory edit) command selects a memory location in the programmed waveform or set of waveforms for editing or start of transmission.

Description: [z] is a number from 0 to (available memory) that specifies the initial memory location for editing or transmission. The available memory will equal the installed memory if SETPAGE is set to 0, or 65535 if paging is set to a number other than 0.

The M command may be followed by a V, B, W, or Z command to load the specified memory location. If subsequent V, B, W, or Z commands are issued, data will be loaded into sequential memory locations following the location specified by the M command.

The M command may also be issued just prior to a 1T command to cause the ARB Module's output to begin at a memory location other than 0. If a repeat count or continuous output is programmed, the waveform will continue to location 0 after the end of the waveform is reached.

If a repeat count of 1 is programmed, the M command may be used in conjunction with programming the end of waveform bit and the 1T command for the random access and single transmission from a collection of waveforms or waveform segments stored in the ARB memory.

Examples:

1. 4021M1.12V2.30 V directs the value in memory location 4021 to be changed to 1.12 V, and the value in memory location 4022 to be changed to 2.30 V.

2. 500M1T causes the ARB Module to begin outputting from memory location 500.

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Command: N (poiNter)

Syntax: [z]N

Purpose: The N (poiNter) command selects a memory location in the waveform sample for editing or reprogramming.

Description: [z] is a number from 0 to (available memory) that specifies the initial memory location for editing. The available memory will equal the installed memory if SETPAGE is set to 0, or 65535 if paging is set to a number other than 0.

The N command may be followed by a V, B, W, or Z commands to load the specified memory location. If subsequent V, B, W, or Z commands are issued, data will be loaded into sequential memory locations following the location specified by the N command.

Unlike the M command, the N command does not affect the starting memory location for transmission. The ARB Module's transmitter starting location is not updated, as it is with the M command.

Example: 4021N1.12V2.30 V directs the value in memory location 4021 to be changed to 1.12 V, and the value in memory location 4022 to be changed to 2.30 V.

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Command: O (isOlation relay)

Syntax: [z]O

Purpose: The O command connects and disconnects the isolation relay of the ARB output.

Description: The isolation relay connection is specified as follows:

[z]	Description
0	disconnects the ARB output from the front connector.
1	connects the ARB output to the front connector.

NOTE: The VX4790A Module does not have the ARB Output connected to the front panel connector on power-up or after a RESET. A 1O command must be sent to transmit a waveform from the front panel ARB output connector.

Example: 1O closes the isolation relay, so that the ARB output is connected to the front panel connector.

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Command: P (Period)

Syntax: [z]P

Purpose: The P command is used to set the period of the output sample rate clock.

Description: [z] is the period value in seconds. It may be programmed as any valid floating point number with or without exponent, from 1.33 to 40E-9.

On power-up, the value of the P command is set to a 40 ns period. The value of the P command is not altered by a Q (Quit) command, but is reset to the power-up value by a K (Kill) command, or by a RESET command (see Appendix A for RESET command). See Appendix E, Frequency Source Accuracy, for a discussion of sample clock accuracy.

The F, P, and D commands are three different methods for programming the output sample rate clock. Only one of the three commands, or the SETSINE (or one of the other pre-programmed waveform commands) is required for programming the output rate of the module.

Example: A 2.05647E-3P command will set the period of the sample clock to 2.05648 milliseconds (a frequency of 486.26779 Hz).

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Command: Q (Quit)

Syntax: Q

Purpose: The Q (Quit) command terminates the ARB Module's output.

Description: When the Q command is issued, waveform output will stop, and the ARB Module's output voltage will go to zero volts.

Any voltages, modes, or sample rates previously programmed will remain unchanged after a Q command is issued.

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Command: R (Repeat)

Syntax: [z]R

Purpose: The R (Repeat) command specifies the number of times the ARB is to transmit its stored waveform.

Description: [z] is a number from 0 to 255 that specifies the number of repetitions. A value of 0 specifies a continuous repeat. The Repeat value will remain at the last programmed value unless power is cycled or a RESET command is sent to the module (see Appendix A). On power-up or upon receipt of a RESET command, the repeat count is set to the default value of continuous.

Examples: 99R causes the stored waveform to repeat 99 times.

0R causes the stored waveform to repeat continuously until the sequence is halted by a Q or K command, or by a RESET command. The same programming result is achieved by sending an R or 0R.

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Command: SCOPY

Syntax: SCOPY [s] [d] [n]<TM>

Purpose: The SCOPY command copies one portion of waveform memory to another.

Description: This command is used to copy one portion of waveform memory to another. The memory portions can be overlapping.

[s] Source start address.

[d] Destination start address.

[n] Number of sample points to copy.

The source start address and destination address must be within the available memory. The available memory will depend on the amount of installed memory and the memory page. See the SETPAGE command for a description of memory paging. Use the GETMEM? query to obtain the amount of installed memory. Hexadecimal numbers may be used by placing them inside parentheses.

The number of sample points should not cause the SCOPY command to go beyond the available memory. That is, the start or destination addresses plus the number of sample points should not exceed the available memory. If an attempt to copy beyond the available memory is made, the copy will be stopped at the end of the available memory and a Memory Over Range error will be generated.

The copy time is approximately 70 microseconds per sample point. Since memory portions can overlap, it is possible to generate multiple cycles of a waveform or even fill a section of memory with a voltage level using this command. Filling a section of memory with a common voltage can be more efficiently accomplished using the SFILL command, however, since it only takes 10 microseconds per sample point. Since the memory will be copied exactly including end of wave, break points, and user synch, it may be desirable to use the SCOPY command before setting these points, or to delete these points before using SCOPY.

Examples:

```
K;SETSINE 5 1E3; 16383N;0V<TM>
SCOPY 0 16384 49152<TM>
65536N; 0V; SFILL 65536 65536<TM>
131071N;0W;1O;T<TM>
```

or

```
K;SETSINE 5 1E3; 16383N;0V<TM>
SCOPY 0 (4000) (C000)<TM>
65536N; 0V; SFILL 65536 65536<TM>
131071N;0W;1O;T<TM>
```


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The above commands will generate a burst of four 1 KHz sinewave cycles by first generating a sinewave using the SETSINE function, deleting the end of wave, duplicating the sinewave three additional times into the first 64k of memory using the SCOPY command, filling the next 64k with 0v, putting an end of wave at the end, turning on the output relay, and then triggering the waveform.

NOTE: At 1 KHz the internally generated sinewave takes up the first 16k of memory; at higher frequencies the waveform may be generated into a smaller section of memory. The numbers given in the above example will have to be adjusted accordingly.

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Command: SETDEF

Syntax: SETDEF<TM>

Purpose: The SETDEF command sets the power-up default values for the current memory page without resetting the settings for other memory pages.

Description: The SETDEF command is used to set power-up defaults for the current memory page without resetting the settings for other memory pages. See the K command for a list of the default settings. See the SETPAGE command for a description of memory pages.

Example: SETPAGE 3;SETDEF<TM>

The above commands would set the memory page to 3 and set power-up defaults for that page only.

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Command: SETDIV

Syntax: SETDIV [d]<TM>

Purpose: The SETDIV command sets the sample clock divider without changing the frequency of the phase locked loop oscillator.

Description: [d] a number from 1 to 16777216 which sets the divider.

Normally the F command is the easiest way to set the frequency of the sample clock. The F command will automatically calculate the best combination of phase locked loop frequency and divider to achieve the desired sample clock frequency. When a change in phase locked loop frequency occurs, however, it can take up to a second for the phase locked loop oscillator to settle to the new frequency. Under some circumstances it may be possible to achieve an acceptable and faster frequency change by using a common phase locked loop frequency and changing only the divider. See the SETPLL command for independently setting the phase locked loop.

Example: SETDIV 52<TM>

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Command: SETPAGE

Syntax: SETPAGE [p]<TM>

Purpose: The SETPAGE command sets the memory page value.

Description: [p] The page number. A page is a 64K block of memory within the installed waveform memory. Valid values are 0 - 4 for 256K modules. Page values 1 - 4 divide the memory into 64k pages. Setting [p] to 0 makes the entire installed waveform memory available.

Option 1 adds 256K of installed waveform memory (4 pages) for a maximum of 8 pages, and Option 2 adds 768 K, for a maximum of 16 pages (see Figure 4).

The waveform memory can be divided into 64k sections (pages) with each section containing a separate waveform. Each page is a virtual ARB environment. Addresses start at 0 for all functions with a maximum address of 65535. Any of the pre-programmed waveforms provided (SETSINE, SETSQUARE, etc.) can be generated. The waveform, frequency, repeat count, attenuation, trigger and clock sources, filters, and isolation relay states are stored for and restored to each page when switching between pages. When a page is first entered after a reset or a K command, the above settings are inherited from the previous page. Use the SETDEF command to set the page to default values if that is not desired. Do not use the K command, since it will also reset paging.

Since page 0 makes the entire installed waveform memory available, any waveforms loaded into page 0 will overwrite memory used by other pages. If, for example, a 128k waveform is loaded into page 0, it will occupy memory that pages 1 and 2 would use. However, it is still possible to use pages 3 and 4 for additional smaller waveforms. All pages used after page 0 will be 64K, and can not be combined (see Figure 5). If Options 1 or 2 are installed, using page 0 makes all installed memory available. If the waveform loaded into page 0 does not use it all the remaining full pages are available as 64K pages. For example, if 435k was loaded into page 0 in Figure 5, pages 8 through 16 would still be available.

It is also possible to copy waveforms from one page to another while on page 0 by using the SCOPY command. If you use this technique, be sure to initialize the destination page by first switching to it, then back to page 0.

When switching between pages, the module is stopped and requires a trigger to restart. This allows you to delay before re-triggering if necessary to allow for delay in locking to the new frequency. See the SETDIV and SETPLL commands.

Examples: Example 1: K;SETPAGE 1<TM>

The module is first reset, then set to page 1, which occupies the first 64k of waveform memory.

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Example 2: SETPAGE 3; SETDEF<TM>

The module is set to page 3 with default settings.

Example 3:
K;SETPAGE 1; SETSINE 1 1E3; 1O<TM>
SETPAGE 2; SETSINE 5 1E3<TM>
SETPAGE 3; SETTRIANG 5 -5 1E3<TM>
SETPAGE 4; SETSAWTOO -5 5 1E3<TM>
SETPAGE 1; T<TM>

The module is first reset with the K command, then each of four pages is programmed with a 1v peak sinewave, a 5v peak sinewave, 5v peak triangle wave, and a 5v peak sawtooth wave. Finally, the module is reset to page 1 and triggered. The module would be left outputting the 1v peak sinewave. The waveform could be quickly changed to the triangle wave by sending "SETPAGE 3; T<TM>". Note that it was not necessary to resend the 1O command to turn on the output relay, since this would be inherited from the previous page as long as a SETDEF was not sent. However, it would not have been valid to wait until the last command, since this would have only turned on the output relay for page 1.

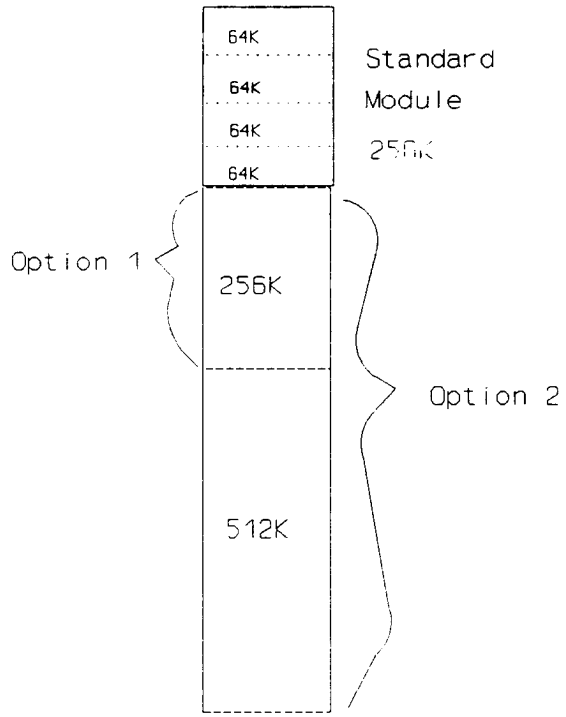


Figure 4: Memory Configuration

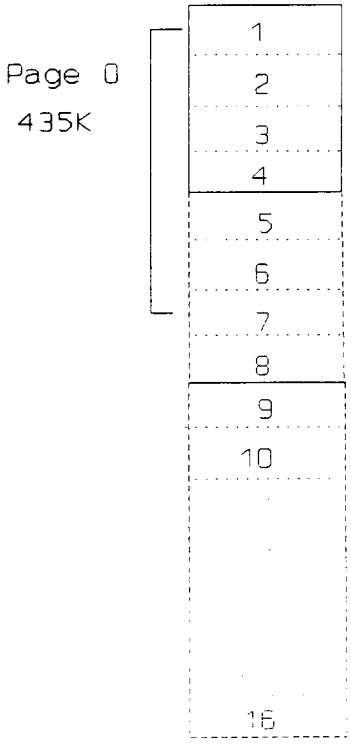


Figure 5: Using Page 0

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Command: SETPLL

Syntax: SETPLL [f]<TM>

Purpose: The SETPLL command sets the frequency of the phase locked loop oscillator without changing the sample clock divider.

Description: [f] A frequency between 12500000 and 25000000. It may be programmed as a floating point number with an exponent.

Normally the F command is the easiest way to set the frequency of the sample clock. The F command will automatically calculate the best combination of phase locked loop frequency and divider to achieve the desired sample clock frequency. When a change in phase locked loop frequency occurs, however, it can take up to a second for the phase locked loop oscillator to settle to the new frequency. Under some circumstances it may be possible to achieve an acceptable and faster frequency change by using a common phase locked loop frequency and changing only the divider. See the SETDIV command for independently setting the divider.

The frequency of the phase locked loop can be set to frequencies between 12.5 MHz and 25 MHz. An attempt to set the frequency outside these limits will generate a Frequency Under Range or Frequency Over Range error.

The resolution of the phase locked loop is 5000 Hz. Any frequency between the limits can be programmed, however, the oscillator will be set to the nearest 5000 Hz increment. The GETPLL? query can be used to determine the actual frequency.

Example 1: SETPLL 16500000<TM>

Example 2: SETPLL 16.5E6<TM>

Both of the above two examples will set the phase locked loop oscillator to 16.5 MHz.

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Command: SETSAWTOO

Syntax: SETSAWTOO [z] [m] [f]<TM>
or SST [z] [m] [f]<TM>

Purpose: Loads ARB memory with a sawtooth wave at the programmed voltage levels and frequency.

Description: This command loads the ARB memory with a sawtooth wave, with the following parameters:

[z] specifies the low or high peak amplitude in volts

[m] specifies the high or low peak amplitude in volts

[f] specifies the frequency

The ramp portion of the wave will have a positive slope if [z] is less than [m], and a negative slope if [z] is greater than [m].

The frequency (F, P, D commands), voltage range (SETVOLTR command), and attenuation (%, A commands) will all be reprogrammed by this command. The voltage range will be set to the lowest voltage range possible, and the attenuation will be reprogrammed and set for internal. The frequency and attenuation which was actually programmed may be obtained with the GETFREQ? and GETATT? commands respectively. Note that the GETFREQ? command returns the sample frequency, not the frequency of the programmed wave.

The SETSAWTOO command is provided to give the ARB Module function generator capability. However, since an ARB basically outputs a sequence of discrete voltage levels, the quality of the sawtooth signal will diminish as the sawtooth frequency approaches the maximum sample frequency of 25 MHz. Maximum frequency available will depend on the quality of the signal required in the application.

A trigger (T or External Trigger) command must be given to start the waveform.

Example: SETSAWTOO -4 3.5 12.5E3<CR><LF>

A sawtooth wave is programmed to ramp from -4 to 3.5 volts at a frequency of 12.5KHz.

SST -4 3.5 12.5E3<CR><LF>

This example would create the same result as the previous example.

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Command: **SETHAVR**

Syntax: **SETHAVR [z] [f]<TM> or SHV [z] [f]<TM>**

Purpose: **This command loads ARB memory with a haversine function at the programmed voltage and frequency.**

Description: **This command loads ARB memory with a haversine function. The haversine function is equivalent to 1/2 (1 − cos Θ)., which is also equivalent to $\sin^2$ (1/2 Θ). The command has the following parameters:**

[z] specifies the peak voltage level in volts. The haversine function will have maximum value of [z] and minimum value of 0 volts.

[f] specifies the frequency in Hertz. Note that the function repeates every 180 degrees, which may make it appear that the function is operating at twice the given frequency.

The frequency (F, D, P commands), voltage range (SETVOLTR command), and attenuation (%, A commands) will all be reprogrammed by this command. The voltage range will be set to the lowest voltage range possible, and the attenuation will be reprogrammed and set for internal. The frequency and attenuation which was actually programmed may be obtained with the GETFREQ? and GETATT? commands respectively. Note that the GETFREQ? command returns the sample frequency, not the frequency of the programmed wave.

The SETHAVR command is provided to give the ARB Module function generator capability. However, since an ARB basically outputs a sequence of discrete voltage levels, the quality of the haversine function signal will diminish as the haversine function frequency approaches the maximum sample frequency of 25 MHz. Maximum frequency available will depend on the quality of the signal required in the application. For haversine function waveforms, the availability of the filtering provided by the L (Low Pass Filter) command maximizes the useful frequency range of the SETHAVR command.

A trigger (T or External Trigger) command must be given to start the waveform.

Example: **SETHAVR 3.12 350<CR><LF>**

The ARB is programmed with a haversine function with maximum value of 3.12 volts, a minimum value of 0 volts, and a frequency of 350 Hz.

SHV 3.12 350<CR><LF>

This example would create the same result as the previous example.

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Command: SETSINO

Syntax: SETSINO [z] [m] [f]<TM>
or SSO [z] [m] [f]<TM>

Purpose: This command loads ARB memory with a sine wave at the programmed voltage minimum, voltage maximum and frequency.

Description: This command loads ARB memory with a sine wave with the following parameters:

[z] specifies the low or high peak voltage amplitude in volts.

[m] specifies the high or low peak amplitude in volts.

[f] specifies the frequency in Hertz.

The frequency (F, D, P commands), voltage range (SETVOLTR command), and attenuation (%, A commands) will all be reprogrammed by this command. The voltage range will be set to the lowest voltage range possible, and the attenuation will be reprogrammed and set for internal. The programmed frequency and attenuation may be obtained with the GETFREQ? and GETATT? commands respectively. Note that the GETFREQ? command returns the sample frequency, not the frequency of the programmed wave.

The SETSINO command is provided to give the ARB Module function generator capability. However, since an ARB basically outputs a sequence of discrete voltage levels, the quality of the sine wave signal will diminish as the sine wave frequency approaches the maximum sample frequency of 25 MHz. Maximum frequency available will depend on the quality of the signal required in the application. For sine wave waveforms the availability of the filtering provided by the L (Low Pass Filter) command maximizes the useful frequency range of the SETSINE command.

A trigger (T or External Trigger) command must be given to start the waveform.

Example: SETSINO -3.12 5.12 350

The ARB is programmed with a sine wave with maximum and minimum values of 5.12 and -3.12 volts, and a frequency of 350 Hz.

SSO -3.12 5.12 350

This example would create the same result as the previous example.

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Command: SETSQUARE

Syntax: SETSQUARE [z] [m] [f]<TM>
or SSQ [z] [m] [f]<TM>

Purpose: Outputs a square wave at the programmed [z] high amplitude peak, [m] low amplitude peak and [f] frequency.

Description: This command loads the ARB memory with a square wave with the following parameters:

[z] specifies the high amplitude of the square wave

[m] specifies the low amplitude of the square wave

[f] specifies the frequency

The frequency (F, D, P commands), voltage range (SETVOLTR command), and attenuation (%, A commands) will all be reprogrammed by this command. The voltage range will be set to the lowest voltage range possible, and the attenuation will be reprogrammed and set for internal. The frequency and attenuation which was actually programmed may be obtained with the GETFREQ? and GETATT? commands respectively. Note that the GETFREQ? command returns the sample frequency, not the frequency of the programmed wave.

For a square wave, the sample frequency will be double the square wave frequency. The maximum square wave frequency available will be 12.5 MHz. At higher frequency, the quality of the square wave will be limited by the settling time specifications listed in the Specifications section of this manual.

A trigger (T or External Trigger) command must be given to start the waveform.

Example: SETSQUARE -1 -3 2000<CR><LF>

This programs a square wave with a high amplitude of -1 Volt and a low amplitude of -3 volts and a frequency of 2 KHz.

SSQ -1 -3 2000<CR><LF>

This example would create the same result as the previous example.

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Command: SETTRIANG

Syntax: SETTRIANG [z] [m] [f]<TM>
or STR [z] [m] [f]<TM>

Purpose: Loads ARB memory with a triangle wave at the programmed voltage levels and frequency.

Description: This command loads the ARB memory with a triangle wave, with the following parameters:

[z] specifies the low or high peak amplitude in volts

[m] specifies the high or low peak amplitude in volts

[f] specifies the frequency

The frequency (P,D,F commands), voltage range (SETVOLTR command), and attenuation (%,A commands) will all be reprogrammed by this command. The voltage range will be set to the lowest voltage range possible, and the attenuation will be reprogrammed and set for internal. The frequency and attenuation which was actually programmed may be obtained with the GETFREQ? and GETATT? commands respectively. Note that the GETFREQ? command returns the sample frequency, not the frequency of the programmed wave.

The SETTRIANG command is provided to give the ARB Module function generator capability. However, since an ARB basically outputs a sequence of discrete voltage levels, the quality of the triangle wave signal will diminish as the triangle wave frequency approaches the maximum sample frequency of 25 MHz. Maximum frequency available will depend on the quality of the signal required in the application.

A trigger (T or External Trigger) command must be given to start the waveform.

Example: SETTRIANG -4 3.5 12.5E3<CR><LF>

A triangle wave is programmed to ramp between -4 and 3.5 volts at a frequency of 12.5KHz.

STR -4 3.5 12.5E3<CR><LF>

This example would create the same result as the previous example.

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Command: SETVOLTR

Syntax: SETVOLTR[z]<TM>

Purpose: Sets the output voltage range.

Description: Output voltage range is selected by the number [z] as follows:

[z]	Voltage Range
10	+10.235 to -10.24 volts into a 50 ohm load with a voltage resolution of 5 millivolts.
5	+5.1175 to -5.12 volts into a 50 ohm load with a voltage resolution of 2.5 millivolts.
.1	+0.10235 to -0.1024 volts into a 50 ohm load with a voltage resolution of 500 microvolts.

For any of the voltage ranges, voltage levels are programmed by the V, B, W, and Z commands, or by the SETSINE, SETSAWTOO, SETSQUARE, or SETTRIANG pre-programmed waveform commands.

Voltages programmed outside of the selected range by the V, B, W, or Z commands will generate an error. Voltages programmed by the pre-programmed waveform commands will re-program (as necessary) the voltage range selected by the SETVOLTR command. The voltages programmed may be attenuated using the A command or the % command.

Example: SETVOLTR .1 selects the optional 0.1 Volt voltage range for subsequent V, B, W, or Z commands.

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Command: SFILL

Syntax: SFILL [a] [s]<TM>

Purpose: The SFILL command fills a block of waveform memory with the value in the first location of the block.

Description: [a] The start address of the block of waveform memory to fill. This address must contain the voltage level with which to fill the block.

[s] The size of the block in sample points.

The start address must not exceed the available memory. The available memory is determined by the amount of installed memory and the memory page. See the GETMEM? query to obtain the amount of installed memory and the SETPAGE command for description of memory paging. Hexadecimal numbers may be used by placing them inside parentheses.

The size of the block should not cause the SFILL command to go beyond the available memory. That is, the size of the block plus the start address should not exceed the available memory. If an attempt to fill beyond the available memory is made, the fill will be stopped at the end of the available memory and a memory over range error will be generated.

Since the block will be filled with the value in the first location of the block, use the N (or M) and V commands to load the first location with desired voltage before initiating the SFILL command. Whatever is in the first location will be duplicated, so that location should not contain a break point, user synch, or end of wave unless duplicating these is intended.

The SFILL command will take approximately 10 microseconds per sample.

Example: 0N3V;SFILL 0 65536<TM> or

ON3V;SFILL (0) (10000)<TM>

The above examples will fill the first 65536 waveform samples with 3 volts by first putting 3 volts into the first location then filling the block of memory with that voltage.

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Command: SMEMTEST

Syntax: SMEMTEST<TM>

Purpose: The SMEMTEST command starts a test of the entire installed waveform memory.

Description: The SMEMTEST command can be used in conjunction with the GETMEM? query to test the full waveform memory.

Sending the SMEMTEST command to the module will start the module's internal waveform memory test. The test will take approximately 20 seconds for each 256k of memory installed. Any waveforms loaded into memory will be lost. During the test the XTRG LED will blink once each time 64k of is memory tested. Since the module only tests what it 'knows' is installed, the GETMEM? query should also be done to make sure that module was initialized to the amount of memory physically installed.

If errors are detected during the test, the test will stop, an error message will be placed in the error queue, and the ERROR LED will light. If no errors are detected then the no error message will be read out of the error queue. Running this command will clear the error queue of any previous error messages.

If an error is detected, the error message will contain information which can help determine the location of the fault. A service manual and a schematic will be needed at this point in order for this information to be of any use. First the failure message will return a block number. The waveform memory is tested in 16k blocks and this block number indicates which 16k block was being tested when the error was detected. Blocks 1 - 16 are in the first 256k section, blocks 17 - 32 are in the second 256k section and so forth. Second the failure message returns an address. Each waveform address is divided into two processor addresses. Even addresses read and write data from data lines 8 - 16 and odd addresses read and write data from data lines 0 - 7. Third the error message will return the data written and the data read from the address. Since this is a hex number, the most significant digit represents the upper four of the address's data lines and the least significant digit represents the lower four.

Example 1:
SMEMTEST<TM>
GETERR?<TM>
Response data: 00,NO ADDITIONAL ERRORS TO REPORT

In the above example 20 seconds should be allowed for each 256k of installed waveform memory after sending the SMEMTEST command before sending the GETERR? query or attempting to read a response from the module. This delay might be unnecessary if the controller is set up for appropriately long timeouts. However, the system will then hang while waiting for the module to respond.

Example 2:
SMEMTEST<TM>
GETERR?<TM>

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Response data: 47,ARB RAM TEST FAILURE: BLOCK 17, ADDR 2065 H WROTE 55 H, READ 51 H<CR><LF>

The above example assumes that an error was found. Block 17 would indicate the second 256k section of RAM, the odd address would indicate data lines 0 - 7, and the error in the lower nibble would further narrow it down to lower four of these.

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Command: STARTBIN

Syntax: STARTBIN [a] [c]<TM>

Purpose: The STARTBIN command sets up the parameters for a binary load of waveform memory and puts the module into binary mode.

Description: The STARTBIN command is used to set up the module to accept a binary load or waveform memory.

[a] The start address of the memory to be filled.

[c] The count of waveform samples to be sent. Since each waveform sample is made up of two bytes, the byte count will be twice this number (bytes = count x 2).

The start address must be within the range of available memory and the count cannot attempt to load beyond available memory. Both the address and count are checked before the module is put into binary mode. If either are out of bounds an error will be generated and the module will not be placed into binary mode. An interrupt can be generated in this circumstance if desired. See the command interrupt under the I command. If numbers are placed inside parentheses, they will be considered hexadecimal.

Once the module is in binary mode, all data sent to the module will be considered binary waveform data until the module receives the number of bytes needed to make up the count of waveform samples. The module can be taken out of the binary mode by sending an end bit or doing an unsolicited read from the module, a VXI reset, or by recycling power.

Each waveform sample is made from 16 bits, with the lower 12 bits used for the waveform amplitude and the upper bits used for end-of-wave, breakpoint, and user synch. When sending binary data to the module, each 16-bit sample is divided into two bytes with the most significant byte sent first. The 16 bits are used as follows:

Bits 0 - 11	Waveform voltage with 000h most negative, FFFh most positive and 800h zero. 800h will always be zero with the positive and negative swings depending on the voltage range, multiplier setting, and load.
Bit 12	Set to a 1 if end of wave, otherwise a 0.
Bit 13	Set to a 1 for a breakpoint, otherwise a 0.
Bit 15	Set to a 1 for a user synch point, otherwise a 0.
Bit 16	Not used. Usually set to 0.

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The lower 12 bits are the binary value that will converted by the DAC to a voltage output. 800h will always be zero regardless of the range, multiplier setting, or load. FFFh will always be the most positive and 000h will always be the most negative. The following table shows the output voltage change with each increment or decrement of the binary value assuming the multiplier is set to 100% and a 50 ohm load is used:

.1 Volt Range	5 Volt Range	10 Volt Range
.00005 V	.0025 V	.005 V

An example of binary data in hex format: 08 00 0F FF 08 00 10 00

The above example programs a four point waveform with points at zero, maximum positive, zero, and maximum negative with end of wave. The STARTBIN command to setup for this would be: STARTBIN 0 4<TM>

Note that the binary example above uses hex only to represent the binary data. The binary data is what is to be sent, not the hex representation. Also note that computers based on Intel and other processors may store integer data with the least significant bytes first. If your computer is one of these and you are storing waveform values as integers, the two bytes of the each integer will have to be swapped before transmission.

As soon as the terminator for the STARTBIN command is received, the module is in binary mode and anything sent will be loaded into waveform memory as binary data. This means that no white spaces or additional terminators can be sent after the terminator. One recommendation is to place the STARTBIN command as a header in the binary data with a semicolon as a terminator. It is recommended that the controller be placed in binary mode prior to sending the STARTBIN command since some controllers may send additional characters or an end of transmission after a terminator or the last character of a group.

The module can support binary transfers as fast as 500K bytes/second as long as it is not in buffered mode. Not all controllers can support this rate, however. Still, binary transfers can be much faster than trying to program large waveforms by sending voltage points in ASCII. For best performance during binary transfers, make sure the module is not in buffered mode.

Getting binary transfers to work properly can be more difficult than sending waveforms in ASCII using the V command. Familiarity with your system controllers (IEEE 488, VXI, etc.) and some trial and error may be necessary.

Example: STARTBIN 0 16384;b.....b

In the above example the b.....b represents the binary data. Since 16384 waveform samples are to be sent the binary data must 32768 bytes long. Notice that there are no spaces separating the semicolon used for the terminator and the start of binary data.

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Command: STEST

Syntax: STEST

Purpose: The Self Test command completes an on-board integrity test of the ARB module.

Description: The self test performs the following operations:

1) The output is disconnected from the output connector by an isolation relay.

2) A RAM test is performed on the first 16,384 memory locations of ARB RAM. Use the SMEMTEST command to test the remainder.

3) A frequency test is performed by loading a test waveform into the ARB memory, running it, and sampling the test waveform at a 468 KHz rate for 160000 samples, verifying the correct voltage level for each sample, using an on-board A/D converter.

4) An amplitude test is performed by running the ARB at a variety of voltage levels, and verifying the voltage levels with voltage measurement circuitry provided on the module.

5) After the self test, the isolation relay is returned to its pre-test setting. All other assets of the board that were used during self test (such as the frequency source) will be returned to their pre-test states, with the exception of the ARB memory, which has been modified. The memory is programmed with a 0 in the first location, and a 0 with end-of-wave at the second location. All other locations are undefined.

After self test, the module should be read to see if any errors have occurred. All errors are described under the GETERR? command. If the self test passed, the "NO ADDITIONAL ERRORS" response will be returned.

CAUTION:

DATA STORED IN THE ARB MEMORY DURING A SELF TEST COMMAND WILL BE ALL OR PARTIALLY LOST DURING EXECUTION OF THE COMMAND AND WILL NEED TO BE RELOADED! ! !

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Command: T (Trigger)

Syntax: [z]T

Purpose: The T (Trigger) command resets the ARB memory pointer to the first voltage sample (optional) and then triggers the ARB Module to output the waveform stored in memory.

Description: After the T command is sent, the programmed waveform is output as defined by the SETSINE, SETSAWTOO, SETSQUARE, or SETTRIANG pre-programmed waveform command, or at the sample rate specified by the F, D, or P commands, and repeated for the number of times specified by the R command.

[z] is either zero or one, specifying the following:

0 resets the memory pointer to the first voltage sample and then triggers the ARB Module to output the waveform stored in memory.

1 triggers the output without resetting the memory pointer. The next voltage sample sent will be the one following a breakpoint, or as selected by the M command.

If no number is specified, [z] is assumed to be zero. A 1T command should be issued to continue output from a programmed breakpoint, or to transmit from a specified location in memory.

The Hardware External Trigger operates the same as a 1T command. It allows triggering from a breakpoint without moving the memory pointer. The X command (external trigger enable) may be issued to reset the memory pointer to the first location in memory. The external hardware trigger will then start the waveform from the first location. The X command may be sent after V, B, W, or Z commands to reset the memory pointer to zero, or the M command may be used to set the pointer to any desired location.

Example: 1T trigger the ARB from the current memory pointer position.

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Command: U (User sync)

Syntax: [z]U

Purpose: The User sync enable command selects the end of wave pulse or programmed sync pulse for connection to the SYNC* front panel connector.

Description: The sync pulse as defined by the Y command, or the End of Wave pulse as programmed by the W or Z command, is selected for output to the front panel.

[z] selects the source for the sync output as follows:

[z]	Description
0	outputs the end of wave pulse to the SYNC* connector.
1	outputs the user programmed sync pulse, programmed by the Y command, to the SYNC* connector.

Example: 0U connects the end of wave pulse to the front panel SYNC* connector.

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Command: V (Voltage)

Syntax: [pv]V

Purpose: The V (Voltage) command loads the memory with the voltage to be output during a sample period.

Description: [pv], the programmed voltage, is a number within the selected voltage range. When entering [pv], a minus sign must prefix negative values; a plus sign is optional for positive values. Leading spaces are ignored. The programmed voltage can be either a floating point or integer value, with or without exponent. If the value of the number is greater than the selected voltage range, an error is generated. The programmed voltage assumes a 50-Ohm load at the output of the ARB module.

The V command also instructs the module's memory pointer to advance to the next memory position (following the voltage load) in preparation for receiving the next voltage sample.

Example: 5.00V programs the voltage sample to 5 volts.

Variations: [pv]B

The B (Breakpoint voltage) command is used to load the memory with the voltage to be output during a sample period with a programmed breakpoint.

Use of the [pv] number is the same as described for the V command. The B command loads the memory with the voltage described for the V command and in addition designates it as a memory breakpoint. The output will stop after the programmed voltage sample until a 1T (continue trigger) or external trigger (assuming the external trigger is armed) is received.

[pv]W

The W (end of waveform voltage) command is used to load the memory with the desired voltage to be output during a sample period and designates this sample as the last sample in the waveform.

Use of the [pv] number is the same as described for the V command. The W loads the memory with the voltage as explained in the V command and in addition defines this sample as the last sample in the waveform. The output will stop after this programmed voltage sample when the programmed R (Repeat) count is reached. If the programmed repeat count of the waveform has not been reached, the ARB continues outputting the waveform from the first voltage sample again.

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Multiple waveform segments may be defined for the ARB, and randomly accessed and transmitted. Each segment must have its last location programmed as an end-of-wave value. The selected segment may be transmitted by setting the memory pointer at the first location of the waveform segment using the M command and then triggering the module with a 1T command. This capability is limited to applications where a repeat count of one is acceptable. The VX4790A continues transmission from the first location in memory for a repeat count greater than one following any end-of-wave location.

[pv]Z

The Z (breakpoint and end of waveform) command loads the memory with the voltage to be output during a sample period with a programmed breakpoint, and also defines this sample as the last sample in the waveform.

The [pv] number is the same as described for the V command. The Z command loads the memory with the voltage as explained in the V command and in addition designates both a breakpoint and end of waveform indicator. The output will stop at the programmed voltage sample until a 1T (continue trigger) is received. When the trigger command is received, it will stop the output if the repeat count has been reached, otherwise it will start the waveform over again at the first voltage sample.

Consecutive V (or B, W or Z) commands load into consecutive memory locations. To program a waveform, send a 0M or 0N command to reset the memory pointer so that programming begins in the first memory location. The memory pointer is automatically incremented by 1 after each V, B, W or Z command is issued.

The contents of memory, as programmed by the V, B, W or Z command are not altered unless power is cycled, a RESET input is sent to the module (see Appendix A) or a K (Kill) command is programmed. In these cases, a value of 0V dc is programmed in the first two locations with an end of waveform indication in the second location. The remainder of memory is undefined.

NOTE: When the ARB Module is halted at a breakpoint, caution is required in the use of any command which changes the memory pointer. If V commands are issued to a breakpoint-halted module, they will be loaded into memory by the module and the memory pointer changed. As a result, the breakpoint "continue at" address will change.

For an application which requires commands that change the memory pointer during a breakpoint, the memory pointer must be returned to the desired location with the M command before the module is triggered.

A higher speed method of programming the ARB memory is available to the experienced user, and is described in Appendix D.

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Examples: Example of a memory load:

0N800E-9P00R0.00V1.00V2.00V3.00V4.00V5.00W

The above command is decoded as follows:

0N sets the memory pointer to zero.

800E-9P programs a sample rate of 800 ns between samples.

00R programs a continuous repeat count.

0.00V1.00V2.00V3.00V4.00V5.00W programs a step function for 0V, 1V, 2V, 3V, 4V, and 5V.

To start the ARB Module outputting the waveform defined above, the system controller would send the command string: T

The memory pointers are reset and the module is triggered, with output starting at the voltage defined in memory location 0.

When the module is triggered, the waveform will continuously repeat until a Q or K command is received by the module.

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Command: X (eXternal trigger)

Syntax: [z]X

Purpose: The X (eXternal trigger) command enables or disables the ARB Module's external-trigger function.

Description: The external trigger source may be selected from an internal trigger, an external front panel trigger, or any of the VXIbus TTLTRG inputs. The X command is also used to specify connection of a trigger to any of the eight TTLTRG lines for use by another VXIbus module.

The following table shows trigger connections for various programmed values of [z]. The VX4790A Trigger Source is the trigger source for the VX4790A being programmed. Trigger sources are the on-board internal trigger, front panel EXT TRG IN connection, and the VXIbus TTLTRG lines. Additional connections shown permit a common trigger source to be used in multiple modules in various configurations.

A discussion of the various trigger connections follows the table.

[z]	VX4790A Trigger Source	Additional Front Panel or TTLTRG Connections
0	External Trigger disabled.	
1	External Trigger directly from the front panel	
10	TTLTRG0*	Front panel External Trigger In to TTLTRG0*.
11	TTLTRG1*	Front panel External Trigger In to TTLTRG1*.
12	TTLTRG2*	Front panel External Trigger In to TTLTRG2*.
13	TTLTRG3*	Front panel External Trigger In to TTLTRG3*.
14	TTLTRG4*	Front panel External Trigger In to TTLTRG4*.
15	TTLTRG5*	Front panel External Trigger In to TTLTRG5*.
16	TTLTRG6*	Front panel External Trigger In to TTLTRG6*.
17	TTLTRG7*	Front panel External Trigger In to TTLTRG7*.
20	TTLTRG0*	None
21	TTLTRG1*	None
22	TTLTRG2*	None

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23	TTLTRG3*	None
24	TTLTRG4*	None
25	TTLTRG5*	None
26	TTLTRG6*	None
27	TTLTRG7*	None

NOTE: User cabling of front panel Sync Output to front panel External Trigger Input is required for [z] = 30 through 37.

30	Internal Software Trigger	Front panel External Trigger Input to TTLTRG0*.
31	Internal Software Trigger	Front panel External Trigger Input to TTLTRG1*.
32	Internal Software Trigger	Front panel External Trigger Input to TTLTRG2*.
33	Internal Software Trigger	Front panel External Trigger Input to TTLTRG3*.
34	Internal Software Trigger	Front panel External Trigger Input to TTLTRG4*.
35	Internal Software Trigger	Front panel External Trigger Input to TTLTRG5*.
36	Internal Software Trigger	Front panel External Trigger Input to TTLTRG6*.
37	Internal Software Trigger	Front panel External Trigger Input to TTLTRG7*.

Trigger selection 1X allows the least time delay and does not restrict you to the VXI 12.5 MHz maximum limitation of the VXIbus TTLTRG back-plane signals.

With trigger selections 10 through 17, operation is limited to the 12.5 MHz backplane limitation of the VXI Specification. Multiple ARB modules can be triggered with the same timing delays for each module, since this selection takes the trigger from the backplane TTLTRG line. To do this, make a selection of 10 to 17 for the ARB Module that has the external trigger connected to the front panel and select the corresponding 20 to 27 external trigger command for all ARB Modules that require the same trigger signal.

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External trigger selections 20 through 27 accept the trigger from the backplane TTLTRG lines.

Trigger selections 30 through 37 allow use of the internal trigger of this VX4790A Module to drive other modules. The module uses its own internal trigger and by external connection of the module's front panel Sync Output to its front panel External Trigger Input, other modules may use this module's sample trigger. The External Trigger front panel input is connected internally on the module to the specified VXIbus TTLTRG line to provide this capability.

This capability also requires programming the 1U command to connect the user programmed sync output to the front panel SYNC Output connector, and programming the synchronization bit in the data transmission (see Y command) at the point at which the trigger to other modules is desired. There will be an approximate 100 nanosecond delay from the time this module is triggered to the time other modules are triggered if the Synchronization bit is programmed for the first location in this module's transmission.

When the external trigger is enabled, the ARB Module can be triggered either by sending a T command to the module or by sending an external-trigger pulse to the module.

The external trigger function will remain at its last programmed value unless power is cycled, a RESET input is sent to the module (see Appendix A) or a K (Kill) command is received by the module, in which case the external trigger function will be disabled.

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Command: Y (sYnc)

Syntax: Y

Purpose: The sYnc command allows a synchronization bit to be output at the SYNC output at the front panel of the VX4790A Module concurrent with any voltage sample.

Description: The single character Y is sent prior to the V, B, W, or Z command for any voltage sample requiring a SYNC output. A U command is also required to enable the output. To cancel a Y command it is necessary to reprogram the voltage sample without a Y command prior to the voltage command.

Example: 1U500E-6P0N0.00V1.00YW0R0T

1U selects the synchronization bit for output to the front panel.

500E-6 programs a 500 microsecond sample rate.

0N resets the memory pointer.

0.00V1.00YW00RT programs a square wave with a low value of 0 volts and a high value of 1 Volt for continuous output, and triggers it.

The Y preceding the W will cause an active low output at the SYNC front panel connector during the 1 Volt sample time during every cycle.

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Command: ? (Status request)

Syntax: ?

Purpose: The ? (Status) command causes the ARB to return the current status of the module when the system controller next requests input from the module.

Description: The module's internal Status register is automatically updated at the time the system controller's input request is received by the module.

The ARB status is returned as five ASCII digits, $D_1D_2D_3D_4D_5$, followed by <CR><LF> characters:

Digit	Value	Status
D_1	1	if ARB is triggered and additional waveform points remain to be output.
	0	if ARB is awaiting a new trigger.
D_2	1	if ARB output is halted at a breakpoint.
	0	if output is not halted at a breakpoint.
D_3	0	D_3 is always 0.
D_4D_5		The digits D_4D_5 indicate any programming errors detected by the module since the last time status was requested or a K (Kill) command was received by the module. Only the first error detected is reported.

The error code in D_4D_5 is provided for software compatibility with the 53A-243 Card. It is recommended that the GETERR? command be used for error reporting for this module.

Error Codes:

D_4D_5	Error Description
00	No error
11	Floating point error
12	Period command error
14	Repeat command is out of range
16	Invalid Interrupt command
17	Divide command is out of range
18	External Trigger command is invalid
19	External Clock command is invalid
20	Low Pass Filter command is invalid
21	W command voltage is out of range
24	B command voltage is out of range
27	V command voltage is out of range
30	Z command voltage is out of range

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The ? command can be used to determine when the waveform generator has completed processing all the setup commands in its input buffer, in buffered mode. If a ? is sent at the end of a command string, when the status is returned, the buffer has been completely processed.

The ? command can also be used to determine when the waveform output has actually triggered. To do this, issue a trigger command at the end of a setup sequence and then poll the status of the module until a triggered condition is reported.

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Command: % (Percent)

Syntax: [z]%

Purpose: The % (percent) command controls attenuation of the output.

Description: [z] an integer or floating point number from 0.00 to 100.00 that specifies the percent of the programmed output that will be transmitted.

The command does not change any memory values that have been programmed, but reduces the output by means of a 12-bit D/A convertor controlling a multiplier on the ARB output.

A value of 100% transmits the output with no attenuation (at 100% of level). A value of 0% attenuates the output to a 0 Volt level (0% of programmed level). The default level of the attenuator at power-up or after a reset is 100%.

The attenuation level programmed by the % command may be read from the VX4790A using the GETATT? command.

The % is only active if the internal reference has been selected as programmed by the A (Attenuator Select) command.

The attenuator command should not be confused with the fixed attenuator settings that may be selected with the SETVOLTR command. The % command may still be used to attenuate the output prior to the SETVOLTR command fixed attenuation settings.

Examples: A value for [z] of 100 programs no attenuation (the wavelength output will be as programmed in the ARB memory).

75% programs the output waveform to 75% of the level of that programmed in ARB memory.

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SYSFAIL, Self Test, And Initialization

The VX4790A Module will execute a self test at power-up, or upon detection of a VXIbus hard or soft reset condition, or upon command. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4790A's commander, sets the Reset bit in the VX4790A's Control register. The self test is in two parts: the interface self test and the instrument self test.

At power-up, as well as during self test, the ARB output remains isolated from the module's front panel connector.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing an interface self test, and the Failed LED is lit. On completion of the interface self test, SYSFAIL* is de-asserted. If the test fails, the SYSFAIL* line remains active.

2) The instrument self test, as described in the STEST command, is then executed. This tests the first 16K of ARB RAM, waveform amplitude, and frequency accuracy.

The default condition of the VX4790A Module after the completion of power-up self test is specified in the K command in the Command Descriptions subsection.

Self test can also be run at any time during normal operation by using the STEST command. At the end of a self test initiated by the STEST command, the module is restored to its pre-test state (with the exception of the ARB waveform memory contents).

During an STEST commanded self test:

1) SYSFAIL* is not asserted.

2) The module executes the same instrument self test as in the power-up case.

3) Any error messages will be queued by the module for later reporting with the GETERR? command.

SYSFAIL* Operation

SYSFAIL* becomes active during power-up, hard or soft reset, self test, or if one of the module's fuses blows. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4790A Module to deactivate SYSFAIL* in all cases except for a blown +5 Volt fuse.

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Synchronizing Multiple Instrumentation Modules

When designing a test procedure, it is important to be aware of the problems that can arise if the individual instrument modules are not properly synchronized. For example, if a relay on one module switches a signal to a voltmeter on another module, and the voltmeter reads the value before the relay has settled, an improper reading will result.

There are two primary methods of implementing proper synchronization:

1) One is to send data to one or more modules as quickly as possible and then check to see if all on-module operations are complete before performing the secondary operation (for example, reading the voltage).

2) The second method is to have the module hold off any more data coming from the controller until the on-module operation is complete. In this case, the voltmeter can be read immediately after the first module is programmed.

The particular application generally determines the method used. The first method results in faster throughput, but requires that some kind of polling sequence take place to assure that on-module operations are complete. The second method is easier to implement and insures that no module will be programmed before operations on a previously addressed module are complete. However, this method may cause one module to hold up data transfer during an interval when other modules could be programmed.

The VX4790A allows using either method. The first method can be initiated by sending the GOTOBUF (buffered mode) command, which allows data collection and data processing to occur in parallel, thus allowing optimal data transfer rates. The VXI fast handshake protocol is used during this time. To be sure that all VX4790A operations are complete, send the ?, GETERR? or GETREV? command and then read the response. The response will not be returned until all commands in the VX4790A's input buffer have been executed.

The second method uses the default setting on the VX4790A, the nonbuffered mode. In this case, it can be assumed that the ARB is running immediately after sending the T command.

When using synchronized nonbuffered mode, it is important that the system controller or the module's commander maintain byte-to-byte synchronization between modules. Tektronix/CDS VXIbus embedded controllers and IEEE-488/VXIbus interface modules typically buffer no more than two characters to provide a high level of byte-to-byte synchronization.

Increased throughput in non-buffered mode can be obtained b sending data in binary format to gain some of the advantages of both methods. In this mode, the data bypasses the onboard processor and is transferred directly to the ARB memory. Binary format is also accepted in buffered mode. However, some of its advantages are lost because the data is buffered before being sent to the ARB memory.

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Section 4
Programming Examples

This section contains example programs which demonstrate how the various programmable features of the VX4790A are used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller.

Definition of BASIC Commands

The programming examples in this manual are written in Microsoft GW BASIC. These examples use the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

Command	Result
CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)	The CALL ENTER statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the VX4790A.
CALL SEND (ADDRESS%, WRT$, STATUS%)	The CALL SEND statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.
END	Terminates the program.
<CR>	Carriage return character, decimal 13.
<LF>	Line feed character, decimal 10.

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Programming Examples In BASIC

The following sample BASIC programs show how commands for the VX4790A might be used. These examples assume that the VX4790A has logical address 24 and is installed in a VXIbus mainframe that is controlled via an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent using a Capital Equipment Corp. IEEE-488 interface. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 21 and to have converted the VX4790A Module's logical address to an IEEE-488 primary address of decimal 24.

Following each example, the data sent to and returned from the module is shown, with data returned by the module shown underlined.

Example 1:

The following program causes the VX4790A to generate a 10 Volt peak-to-peak 5 KHz sine wave, send back an error message, and then prints the response.

Lines 10 through 40 initialize the PC's IEEE-488 interface module as a system controller with an IEEE-488 address of decimal 24.

Line 50 assigns the decimal IEEE-488 address of the VX4790A to the variable ADDR4790A%.

Line 280 reads back the error message. Note that in line 260 RD$ had been initialized. This is important since the ENTER function needs to have a previously initialized string long enough to hold the received data.

```
10 DEF SEG = &HC400 ' Segment of the CEC ROM
```
Line 10 sets a variable to the CEC ROM segment address.

```
20 INIT% = 0: ENTER% = 21: SEND% = 9
```
Line 20 sets variables to offsets into the CEC ROM where the jump vectors for the various functions are located.

```
30 PCADDR% = 21 : CONTROL% = 0
```
Define IEEE-488 Interface Module's IEEE-488 address and define it to be a controller.

```
40 CALL INIT% (PCADDR%, CONTROL%)
```
Initialize.

```
50 ADDR4790A% = 24
```
Lines 240 through 250 send out the sequence to generate the sine wave. Note that a line feed <LF> is automatically added by the SEND function.

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240 WRT$ = "K;SETVOLTR 5;SETSINE 5 5E3;1O;0T"
Generate a 10 Volt peak-to-peak (±5 volts peak value) 5 KHz sine wave, assuming a 50 ohm load.

250 CALL SEND% (ADDR4790A%,WRT$,STATUS%)

260 WRT$ = "GETERR?" : RD$ = SPACE$(100)
Lines 260 through 270 send the command telling the card to send back error responses. (This is the default and is put here for example only.)

270 CALL SEND% (ADDR4790A%,WRT$,STATUS%)

280 CALL ENTER% (RD$,LENGTH%,ADDR4790A%,STATUS%)
Inputs the error message into the string RD$.

290 PRINT RD$
Line 300 prints the received data.

300 END

The output to the VX4790A Module would be:

K;SETVOLTR 5;SETSINE 5 5E3;1O;0T<LF>
GETERR?<LF>

The response from the module should be:

00,NO ADDITIONAL ERRORS TO REPORT

Example 2:

The following program causes the VX4790A to generate a 1Khz ramp from +5 V to -5 V in one Volt steps, send back an error message, and prints the response.

This example is the same as the previous example, except that a series of voltage steps is programmed in lines 260 and 270 to generate the ramp.

10 DEF SEG = &HC400 ' Segment of the CEC ROM
Line 10 sets a variable to the CEC ROM segment address.

20 INIT = 0: ENTER% = 21: SEND% = 9
Line 20 sets variables to offsets into the CEC ROM where the jump vectors for the various functions are located.

30 PCADDR% = 21 : CONTROL% = 0
Define IEEE-488 Interface Module's IEEE-488 address and define it to be a controller.

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40 CALL INIT% (PCADDR%, CONTROL%)
Initialize.

50 ADDR4790A% = 24
Lines 240 through 250 send out the sequence to generate the sine wave. Note that a line feed <LF> is automatically added by the SEND function.

240 WRT$ = "K;SETVOLTR 5;1O"
K resets the module. SETVOLTR 5 selects the 5 Volt ranges. 1O connects the output to the connector.

250 CALL SEND% (ADDR4790A%,WRT$,STATUS%)

260 WRT$ = "0N5V4V3V2V1V0V-1V-2V-3V-4V-5W;11E3F;0T"
0N resets the memory pointer. 5V4V3V2V1V0V-1V-2V-3V-4V-5W programs eleven successive outputs from 5 to -5 V in 1 Volt steps. 11E3F specifies an 11 KHz sample frequency which, with eleven data points, results in a 1 KHz ramp frequency. 0T triggers the transmission. The default count of 0R will result in continuous transmissions.

270 CALL SEND% (ADDR4790A%,WRT$,STATUS%)

280 WRT$ = "GETERR?" : RD$ = SPACE$(100)

290 CALL SEND% (ADDR4790A%,WRT$,STATUS%)

300 CALL ENTER% (RD$,LENGTH%,ADDR4790A%,STATUS%)

310 PRINT RD$

320 END

The output to the VX4790A Module would be:

K;SETVOLTR 5;1O<LF>
0N5V4V3V2V1V0V-1V-2V-3V-4V-5W;11E3F;0T<LF>
GETERR?<LF>

The response from the module should be:

00,NO ADDITIONAL ERRORS TO REPORT

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Appendix A
VXIbus Operation

The VX4790A Module is a C size single slot VXIbus Message-Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4790A Module is neither a VXIbus commander or VMEbus master, and therefore it does not have a VXIbus Signal register. The VX4790A is a VXIbus message based servant.

The module supports the Normal Transfer Mode of the VXIbus, using the Write Ready, Read Ready, Data In Ready (DIR), and Data Out Ready (DOR) bits of the module's Response register.

A Normal Transfer Mode read of the VX4790A Module proceeds as follows:

1. The commander reads the VX4790A's Response register and checks if the Write Ready and DOR bits are true. IF they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

2. The commander writes the Byte Request command (0DEFFh) to the VX4790A's Data Low register.

3. The commander reads the VX4790A's Response register and checks if the Read Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

4. The commander reads the VX4790A's Data Low register.

A Normal Transfer Mode Write to the VX4790A Module proceeds as follows:

1. The commander reads the VX4790A's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready and DIR bits until they are true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX, depending on the End bit) to the VX4790A's Data Low register.

The VX4790A Module also supports the Fast Handshake Mode during readback. In this mode, the module is capable of transferring data at optimal backplane speed without the need of the commander's testing any of the handshake bits. The VX4790A Module

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asserts BERR* to switch from Fast Handshake Mode to Normal Transfer Mode, per VXI Specification. The VX4790A's Read Ready, Write Ready, DIR and DOR bits react properly, in case the commander does not support the Fast Handshake Mode.

A Fast Handshake Transfer Mode Read of the VX4790A Module proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the VX4790A's Data Low register.

2. The commander reads the VX4790A's Data Low register.

The VX4790A Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the VX4790A's address space may cause incorrect operation of the module.

As with all VXIbus devices, the VX4790A Module has registers located within a 64 byte block in the A16 address space.

The base address of the VX4790A device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches.

VX4790A Configuration Registers.

Below is a list of the VX4790A Configuration registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address:

REGISTER DEFINITIONS

Register	Address	Type	Value (Bits 15-0)
ID Register	0000H	RO	1011 1111 1111 1100 (BFFCh)
Device Type	0002H	RO	See Device Type definition below
Status	0004H	R	Defined by state of interface
Control	0004H	W	Defined by state of interface
Offset	0006H	WO	Not used
Protocol	0008H	RO	1111 0111 1111 1111 (F7FFh)
Response	000AH	RO	Defined by state of the interface
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below
Data Low	000EH	R	See Data Low definition below

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REGISTER BIT DEFINITIONS

ID:	BFFCh
Device:	F4E9h
Protocol:	F7FFh

Word Serial Commands

A write to the Data Low register causes this module to execute some action based on the data written. This section describes the device-specific Word Serial commands this module responds to and the results of these commands.

Read Protocol command response: FE6Bh

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Appendix B
Input/Output Connections

SMB connectors are used for both input and output connections. The input/output connectors, from top to bottom, are as follows:

Signal Name	Function
EXT CLK*	External Clock (sample rate) Input
EXT TRG*	External Trigger Input
SMP CLK*	Sample Clock Output
SYNC*	Sync Output
AM IN	Amplitude Modulation Input
ARB OUT	Arbitrary Waveform Output

* = low true

EXT CLK* (External Clock Input)

The External Clock (sample rate) Input is enabled when the External Clock Function is enabled with the C command (see Operation section). The input accepts a TTL-compatible signal from 0 Hz to 25 MHz. The clock must be high for a minimum of 14 ns and low for a minimum of 17 ns.

EXT TRG* (External Trigger Input)

This input provides external-triggering capability if the input is enabled by the X (eXternal trigger) command (see Operation section). The input requires a TTL-compatible, active low signal. The ARB Module is triggered on the falling edge of the input signal. The minimum pulse width is 160 ns. Actual ARB Module triggering will occur within 1 to 160 ns after the falling edge of the external-trigger signal.

SMP CLK* (Sample Clock Output)

The sample clock of the ARB is output as a TTL active low signal.

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SYNC* (Sync Output)

This is a TTL active low output that provides a pulse which is synchronous with the analog-output step that identified it as an end-of-wave location (see W or Z command) or with the user programmed sync bit (see Y command). The U command selects the end-of-wave function or sync function for connection to the SYNC output.

ARB OUT (Arbitrary Waveform Output)

This is the analog output of the arbitrary waveform generator. This output can drive a load of 50 Ohms at ±5.11 V or at ±10.22 V. Option 01 allows the output to drive a 50 Ohm load at ±0.1022 Volts.

AM IN (Amplitude Modulation Input)

This is an analog input that accepts a user-provided voltage in the ±1.5 Volt range that attenuates the programmed voltage output. The A command enables the amplitude modulation input.

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Appendix C
VXI Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted. Not all terms appear in every manual.

Term	Definition
Accessed Indicator	An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.
ACFAIL*	A VMEbus backplane line that is asserted under these conditions: 1) by the mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.
A-Size Card	A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.
Asynchronous Communication	Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.
Backplane	The printed circuit board that is mounted in a VXIbus mainframe to provide the interface between VXIbus modules and between those modules and the external system.
B-Size Card	A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.
Bus Arbitration	In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.
Bus Timer	A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-

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existent Slave location could result in an infinitely long wait for the Slave response.

Client — In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10 — A 10-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

CLK100 — A 100-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

Commander — In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command — A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers — In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers — A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card — A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

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Custom Device A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

Data Transfer Bus One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

DC SUPPLIES Indicator A red LED indicator that illuminates when a DC power fault is detected on the backplane.

Device Specific Protocol A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 x 14.4 in x 1.2 in).

DTB See Data Transfer Bus.

DTB Arbiter A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT Device Under Test.

ECLTRG Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.

Embedded Address An address in a communications protocol in which the destination of the message is included in the message.

ESTST Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Self Test Any self test or diagnostic power-up routine that executes after the initial kernel self test program.

External System Controller The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

IACK Daisy Chain Driver The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

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ID-ROM An NVRAM storage area that provides for non-volatile storage of diagnostic data.

Instrument Module A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

Interface Device A VXIbus device that provides one or more interfaces to external equipment.

Interrupt Handler A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus mainframe or several mainframes. See Resource Manager.

Local Processor The processor on an instrument module.

Logical Address The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

Mainframe

Card Cage For example, the Tektronix VX1400 Mainframe, an operable housing that includes 13 C-size VXIbus instrument module slots.

Memory Device A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

Message Based Device A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines Module/system identity lines.

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Physical Address The address assigned to a backplane slot during an access.

Power Monitor A device that monitors backplane power and reports fault conditions.

P1 The top-most backplane connector for a given module slot in a vertical mainframe such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal mainframe.

P2 The bottom backplane connector for a given module slot in a vertical C-size mainframe such as the VX1400; or the middle backplane connector for a given module slot in a vertical D-size mainframe such as the VX1500.

P3 The bottom backplane connector for a given module slot in a vertical D-size mainframe such as the Tektronix VX1500.

Query A form of command that allows for inquiry to obtain status or data.

READY Indicator A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-Volt power will extinguish this indicator.

Register Based Device A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.

Requester A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.

Resource Manager A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.

Self Calibration A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.

Self Test A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-up.

Servant A VXIbus message-based device that is controlled by a commander.

Server A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.

Shared Memory

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Protocol A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

Slot 0 Controller See Slot 0 Module. Also see Resource Manager.

Slot 0 Module A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.

SMP See Shared Memory Protocol.

STARX Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STARY Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STST STart/STop protocol; used to synchronize modules.

SYNC100 A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2ns of skew.

Synchronous Communications A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL* A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

System Clock Driver A functional module that provides a 16-MHz timing signal on the Utility Bus.

System Hierarchy The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

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Test Monitor	An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.
Test Program	A program, executed on the system controller, that controls the execution of tests within the test system.
Test System	A collection of hardware and software modules that operate in concert to test a target DUT.
TTLTRG	Open collector TTL lines used for inter-module timing and communication.
VXIbus Subsystem	One mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.
Word Serial Protocol	A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).
Word Serial Communications	Inter-device communications using the Word Serial Protocol.
WSP	See Word Serial Protocol.
10 MHz Clock	A 10 MHz, ±100 ppm timing reference. Also see CLK10.
100 MHz Clock	A 100 MHz, ±100 ppm clock synchronized with CLK10. Also see CLK100.
488-To-VXIbus Interface	A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

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Appendix D
Advanced Program Capabilities

The following command is provided to extend the range of programming capabilities for the VX4790A Module.

Command: # (binary)

Syntax: #[z][m][b,..b_n]

Purpose: The # (binary) command places the module in binary mode to load voltage waveform data points at a much faster rate than is possible with the V command.

Description: [z] is the binary address the memory pointer is to be set to. It is a 2-byte number, high byte first, with a value from $\{00000000\}\{00000000\}_B$ to $\{01111111\}\{11111111\}_B$, or 0 to 16383 decimal. See the STARTBIN command for larger binary transfers.

[m] is the number of binary bytes (2 bytes per voltage) in binary that the module will receive from the user. The value of [m] is in two bytes, high byte first.

The voltage data (b ..... b_n) is sent in binary as a string of two byte binary values, high order byte first, following the two byte value of [m]. The sixteen bit data (bits 15 to 0) are in the format of 12 bits of voltage data in the lowest twelve bits (bits 11 to 0 where zero is the least significant bit) of the data. Bit twelve is set if the voltage sample is the last sample in the waveform. Bit thirteen is set if the output is to be programmed for a breakpoint. Bit fourteen is set for a user defined sync pulse.

The 12-bit value is a binary value offset from 0000000000 to 111111111111 and programs a value from negative full scale to positive full scale of the selected voltage range (-10.23 V to +10.22 V, -5.12 V to +5.11 V, or -.1023 V to +.1022 V) into a 50 ohm load.

The download rate of the module is 370K bytes/second. Note that the effective download rate may be limited by the controller.

Use the following algorithms to determine the two 8-bit bytes for a particular voltage. It effectively divides the desired voltage by the voltage steps size (0.0025 V for 5 V range, 0.005 V for 10 V range, 0.00005 V for 0.1 V range) and adds 2048. Examples are given for using the algorithm for each voltage range, and Example 4 gives an example of the Binary command itself.

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For the Voltage Range of 10 Volts

Value = (Voltage * 200) + 2048
Low Byte = Value - INT(Value/256) * 256
High Byte = INT(Value/256) + 16 (if end-of-wave) + 32 (if breakpoint) + 64 (if user programmed sync pulse).

Example 1:

a) A voltage of 3.00 V, with an end-of-wave would give a value of 2648; a low byte of 2648 - 2560 or 88 decimal, and a high byte value of 10 + 16 or 26 decimal.

b) A value of 1.00 Volt without an end-of-wave would require a low byte of 200 and a high byte of 8.

For the Voltage Range of 5 Volts

Value = (Voltage * 400) + 2048
Low Byte = Value - INT(Value/256) * 256
High Byte = INT(Value/256) + 16 (if end-of-wave) + 32 (if breakpoint) + 64 (if user programmed sync pulse).

Example 2:

a) A voltage of 3.00V, with an end-of-wave would give a value of 3248; a low byte of 3248 - 3072 or 176 decimal, and a high byte value of 12 + 16 or 28 decimal.

b) A value of 1.00 Volt without an end-of-wave would require a low byte of 144 and a high byte of 9.

For the Voltage Range of 0.1 Volt (Option 01)

Value = (Voltage * 20000) + 2048
Low Byte = Value - INT(Value/256) * 256
High Byte = INT(Value/256) + 16 (if end-of-wave) + 32 (if breakpoint) + 64 (if user programmed sync pulse).

Example 3:

a) A voltage of 0.03V, with an end-of-wave would give a value of 2648; a low byte of 2648 - 2560 or 88 decimal, and a high byte value of 10 + 16 or 26 decimal.

b) A value of 0.001 Volt without an end-of-wave would require a low byte of 20 and a high byte of 8.

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Binary Command

Example 4:
Binary values may be sent in many programming languages by building a string with a CHR$ function. The argument of the CHR$ function is a decimal value of 0 to 255 or a hexadecimal value of 00 to FF to provide any 8-bit binary value.

To program a 2-point waveform of 1.0 V followed by 3.0 V with an end of wave the following string would be built and transmitted to the module.

```
VOLT$ = "#" + CHR$(0) + CHR$(0) + CHR$(0) + CHR$(4)
 + CHR$(9) + CHR$(144) + CHR$(28) + CHR$(176)
```

The first character # defines a binary command. The following two bytes define the start address for the memory pointer (in this case zero). The next two bytes, 0 and 4, define four bytes (two words) to be transmitted, and the last four values define the two voltage samples for the 5 Volt range, as described earlier in the example. See the STARTBIN command for larger binary transfers.

NOTE: For best performance during binary transfers, make sure the module is not in buffered mode.

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Appendix E
Frequency Source Accuracy

The frequency source has a worst case accuracy of 0.025% of the programmed value, yet in virtually all cases it will be equivalent to the accuracy of the crystal at 0.005%.

The accuracy to which the frequency source is programmed can be guaranteed to be equivalent to the crystal accuracy (0.005%) if the number of significant digits sent with the F (Frequency) command is small enough, as in the following cases:

1) All values that have only three or fewer significant digits: 25E6 Hz, 2.34 Hz, 99.9e3 Hz. (99.98e3 Hz would not be an example).

2) Values that have four significant digits and are between 2502 and 4998 and are an even number: 4.234E6 Hz, 2998E3 Hz. (3991E3 Hz would not be an example).

3) Values that have five significant digits that begin with 1 to 4 and the fifth digit is a 5: 13.0050E6 Hz.

For example, the frequency 13.005 MHz can be programmed to the crystal accuracy, but 13.0025 MHz can only be programmed to within 0.019% of the programmed frequency.

The GETFREQ? command can be used to determined the actual accuracy for a given frequency. This command returns the value that the frequency source was actually programmed to.

For example, 13.005E6FGETFREQ?; will return 13005000 Hz, which indicates that it was programmed to within the crystal frequency.

13.0025E6FGETFREQ?; will return 13005000 Hz, which indicates that it was programmed to within (1 - 13.005/13.0025) = 0.019% (+0.005% crystal accuracy) = 0.024% of the programmed frequency.

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Appendix F (Option 1M)
MATE Programming

This Appendix defines the programming commands to be used with the VX4790A when the module has been ordered with Option 1M. With Option 1M installed, the VX4790A includes an embedded TMA (Test Module Adapter) that fulfills the United States Air Force MATE system IAC (Instrument-on-A-Card) requirements for isolated self test and remote programming via MATE CIIL (Control Interface Intermediate Language) commands.

The following subjects are covered in this manual section:

CIIL / Commercial Differences (A - 21)
CIIL Command Mnemonics and Definitions (A - 22)
CIIL Command Structures and Formats (A - 25)
Error Descriptions (A - 33)
ATLAS and CIIL Syntax (A - 27)
ATLAS Field Limits (A - 34)

The user is assumed to be familiar with the ATLAS (Abbreviated Test Language for All Systems) programming language as it is applied to MATE systems.

CIIL / Commercial Differences

The CIIL implementation of this module differs from operations described in the body of the VX4790A document in some respects.

CIIL does not allow interrupts to be enabled for IEEE-488 Service Requests. It always operates in the nonbuffered mode, and supports the standard CIIL commands and data syntax, which excludes the binary data syntax.

Because the self test takes under five seconds, the confidence and self test are identical on this module.

SYSFAIL* operates the same as for the commercial unit. Refer to the SYSFAIL, Self Test and Initialization subsection in the Operation section of this manual.

The following specifications differ with the CIIL option installed:

VXI Data Rate:
400 bytes/sec minimum

VXIbus Protocol Events Supported:

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VXIbus events are returned by this module via VME interrupts. This module supports the following event:

UNRECOGNIZED COMMAND

Conversion Rate:

Throughput is the maximum number of conversions per second which can be accomplished by the DAC on a continuous basis. This module is capable of a conversion rate in excess of 500 conversions per second per channel.

CIIL Command Mnemonics and Definitions

The VX4790A Module is controlled by CIIL commands issued to the module by the module's VXIbus commander over the VXIbus mainframe backplane. The commander module is interfaced to the MATE station computer via an IEEE-488 interface bus. A typical control sequence for the module is as follows:

1) Set up the waveform output of the VX4790A with an FNC command.

2) Connect the output pins of the module to the UUT (Unit Under Test) via the MATE switching system with a CON command to the test station switch assembly.

3) Close the VX4790A's output isolation relay, connecting the waveform's output to the VX4790A's front panel connector with a CLS command.

4) Reset the waveform output with a RST command.

5) Disconnect the output pins of the module to the UUT (Unit Under Test) via the MATE switching system with a DIS command to the test station switch assembly.

Each CIIL command consists of an op code and up to three different types of operands. The operands are nouns, noun-modifiers, and modifier values. Depending on the op code, a given operand may or may not be required.

If the module detects syntax errors in a transmission, the entire transmission and all future transmissions are ignored until a STA (Status) command is received. Following a STA command, the station computer requests input from the module and receives an ASCII message, identifying the module status as error or no error.

Op Codes

Mnemonic	Definition
GOTOCIIL	Return from alternate language: This command should be sent to return to the CIIL environment after a GAL instruction. Any pending errors are discarded, request true interrupts are disabled, and buffered mode is

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terminated if previously entered while in the alternate language. This command will cause an error if executed before the GAL command.

CLS — Close: commands the module to close the isolation relay.

CNF — Confidence Test: commands the module to perform a confidence test. An error message is queued if hardware malfunctions are encountered during the test. The queued error message is returned to the station computer when the module receives an STA command. The confidence test takes less than 5 seconds to execute. The test performed is described under the STEST command in the Operation section of this manual. The same test is performed for both the CIIL CNF and STEST commands.

FNC — Function: identifies a channel to be set up and indicates the start of a setup sequence.

GAL — Go to alternate language: Allows any command listed in the Operation section of this manual to be executed. Any pending errors are discarded.

IST — Internal Self Test: commands the module to perform a self test. An error message is queued if hardware malfunctions are encountered during the self test. The queued error message is returned to the station computer when the module receives an STA command. The internal self test takes less than 5 seconds to execute. The test performed is described under the STEST command in the Operations Section of the standard instrument manual. The same test is performed for both the CIIL CNF and STEST commands.

OPN — Open: commands the module to open its output isolation relay.

RST — Reset: opens the module's output isolation relay and sets the waveform output to 0.000 volts.

SET — Setup: This op code is used to specify a characteristic (noun-modifier) of any CIIL nouns specified in the FNC command string, and its associated value, if any.

SID — Self Identification: commands the module to return an identification string in the following format:

<SP>COLORADO DATA SYSTEMS;VX4790A;0;<REV>; <STATUS RESPONSE><CR><LF>

where:

<SP> = space
<CR> = carriage return
<LF> = line feed
<REV> = revision level (e.g. 1.0)

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<STATUS RESPONSE> = the ASCII message that would normally be returned in response to a STA command, in accordance with MATE-STD-2806763, paragraphs 5.3.4 and 5.3.4.2.

STA Status: commands the module to report its current status and/or any error that has been queued to the station computer.

Nouns

WAV Waveform: defines the general class of the output as an arbitrary waveform output.

ACS AC signal: defines the output signal as a standard ac sine wave waveform.

SQW Square Wave: defines the output signal as a standard square wave waveform.

TRI Triangle Wave: defines the output signal as a standard triangle wave waveform.

RPS Ramp Signal: defines the output signal as a standard ramp signal output.

Noun-Modifiers

STIM Stimulus: data storage location for an arbitrary waveform stimulus. The stimulus waveform data to be output to the UUT.

VLTS Voltage Stepped: permits output as a set of amplitude samples for use of the VX4790A in an Arbitrary Waveform Generation mode.

VLTL Voltage Limit: permits specification of a maximum voltage output from the VX4790A for protection of the UUT.

CLSC Clock Source: defines the clock to be an internal or external signal.

FREQ Frequency: The rate at which a periodic waveform is repeated.

CLFR Clock Frequency: defines the frequency of a clock signal.

PERI Period: defines the period of a repetitive waveform.

TRSC Trigger Source: defines the trigger source to be internal or external.

BURS Burst: defines the number of cycles of the stimulus to be performed.

ATTN Attenuation: the ratio between the output level transmitted and that programmed on the waveform.

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TIMP Test Equipment Impedance: the impedance of the load. Permits application of the specified voltage at the UUT load based on the UUT input impedance.

SYNC Sync Out: allows for output on the Sync Output at an end-of-waveform data location.

AMOD Amplitude Modulation: enables control by an external modulation source.

MDSC Modulation Source: defines the modulation source to be external or internal.

NOTE: Only external is available on this product.

POSS Positive Slope: defines the ramp portion of a ramp signal to have a positive slope.

NEGS Negative Slope: defines the ramp portion of a ramp signal to have a negative slope.

VPKP Voltage Peak Positive: specifies the positive peak voltage for an asymmetrical repetitive signal.

VPKN Voltage Peak Negative: specifies the negative peak voltage for an asymmetrical repetitive signal.

VLPP Voltage Peak-To-Peak: indicates the peak-to-peak voltage of the signal measured from the positive peak to the negative peak.

VLPK Voltage Peak: the maximum voltage of a repetitive symmetrical waveform referenced to zero volts.

DCOF DC Offset: the DC voltage level reference of a waveform.

CIIL Command Structures and Formats

This sub-section defines the ordering of commands that are sent to this module. Except for the "FNC ..." command, each command is transmitted separately and terminated with a <CR><LF>.

The "FNC ..." in this module follows the standard CIIL format for a stimulus instrument. The "FNC" is followed by a noun (WAVE, ACS, SQW, TRC, or RPS) and a channel number (this module has a single channel, so CH00 is the only valid channel number). The channel number is followed by a string of SET op codes with noun-modifiers and associated values as required. A single <CR><LF> termination for the FNC statement follows the last SET statement.

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Examples of the CIIL command structure are shown in the section on ATLAS and CIIL Syntax later in this Appendix.

Error Descriptions

The following error descriptions are supported:

SELF TEST FAILURE: FREQUENCY
The frequency test described under the STEST command has failed, although there were transitions of the test waveform.

SELF TEST FAILURE: NO CLOCK
The test waveform is remaining at a steady voltage level.

SELF TEST FAILURE: DELAYED TRIGGER
The frequency test described under the STEST command passed, but only after waiting over 200 µsecs for the ARB to trigger. This indicates a problem with the trigger circuit.

SELF TEST FAILURE: AMPLITUDE: PROGRAMMED <VOLTS>V, READ <VOLTS>V
The ARB voltage self test returned an incorrect voltage level. If the READ value is approximately 0 volts, this could indicate a problem in the triggering circuitry.

SELF TEST FAILURE: SELF TEST A/D INOPERATIONAL
The A/D used during the amplitude portion of the self test is not operational.

VOLTAGE OUT OF RANGE
The voltage value sent is too large for the current voltage range.

DIVIDE COUNT TOO LARGE
The programmed divide count (D command) was more than 16,777,218.

FREQUENCY UNDERRANGE
The programmed frequency resulted in an attempt to program the sample clock to below 0.75Hz.

FREQUENCY OVERRANGE
The programmed frequency resulted in an attempt to program the sample clock to more than 25MHz.

PERIOD UNDERRANGE
The programmed period resulted in a sample clock with a period below 40ns.

PERIOD OVERRANGE
The programmed period resulted in a sample clock with a period greater than 1.3333 seconds.

UNRECOGNIZED COMMAND
The received command was unrecognized.

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RECEIVED UNEXPECTED <CHAR> WHILE <REASON>

<CHAR> = <single quote> <character> <single quote> for printable characters (20 hex through 7f hex), for example 'G'.
or
<CHAR> = <SP> <ASCII hex digit> <ASCII hex digit> for nonprintable characters (00 hex through 19 hex and 80 hex through FF hex), for example, 0A.

<REASON> = one of the following:

- EXPECTING A LINE FEED, SEMICOLON OR COMMA.
- EXPECTING A NUMERIC.
- PARSING MANTISSA.
- PARSING EXPONENT.

TOO MANY DIGITS IN EXPONENT

More than 3 digits were received in an exponent.

VOLTAGE OUT OF RANGE FOR TEST IMPEDANCE OF <VALUE> OHMS

The specified output voltage cannot be created with a test impedance of <VALUE>. The specified output impedance must be reduced or the test impedance must be increased. Refer to the equation in the ATLAS Field Limits sub-section of this Appendix for the relationship between maximum output voltage and test impedance.

TOO MANY ERRORS

More error messages have occurred since the last GETERR? command, than can fit in the VX4790A's output buffer.

ATLAS and CIIL Syntax for VX4790A with Option 1M

This sub-section defines the ordering of commands allowed by the VX4790A with Option 1M. The symbol definitions used in the syntax expansions are as follows:

Symbol	Definition
< >	Numeric value defined later (enclosed between symbols)
[ ]	Optional item of structure (enclosed between symbols)
::	Is defined to be
{ }	Set of choices or boundaries of a structure of inseparable items (enclosed between symbols)
:	Exclusive OR
...	Optional repetition

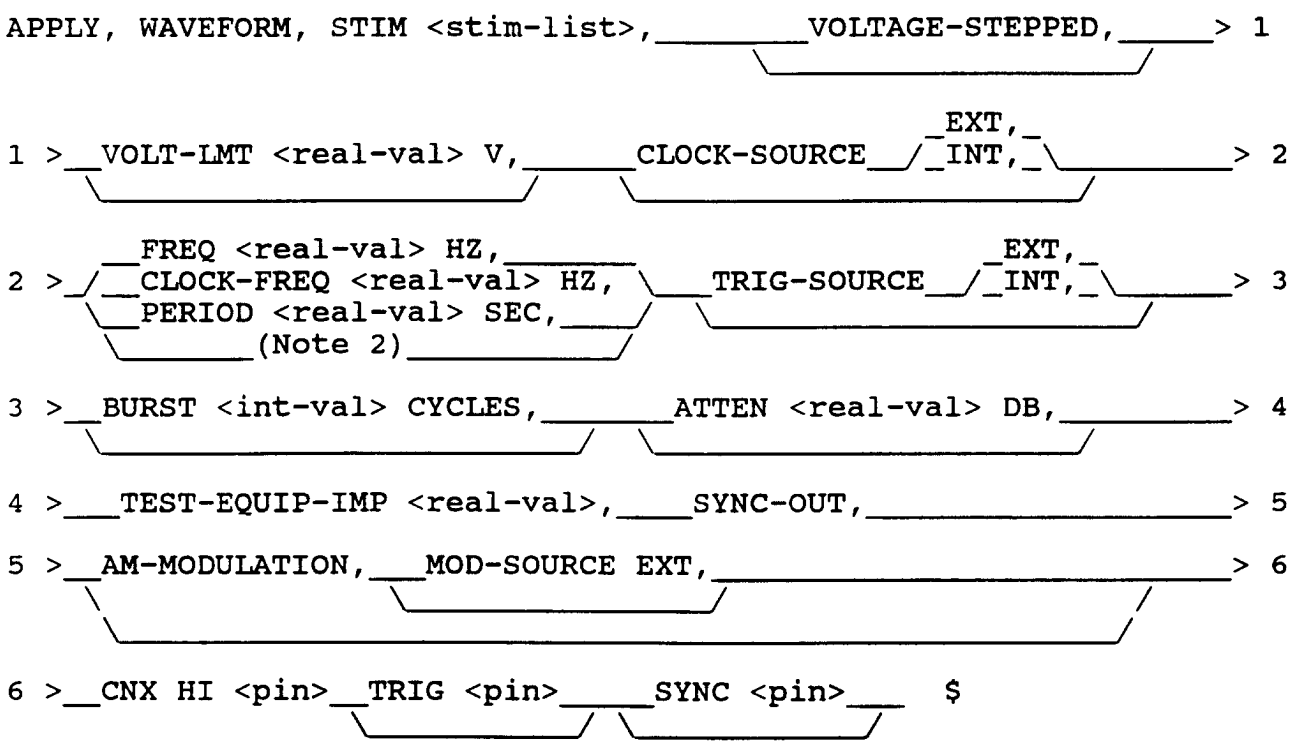
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Term Definitions:

<integer-val>	Integer
<integer-list>	A list of integers
<real-val>	Decimal number
<real-list>	A list of decimal numbers
<connection>	Connection field as defined in ATLAS program.
<chan-num>	Channel number
<statno>	Statement number
<CR>	Carriage return
<LF>	Line feed
<SP>	Space
<units>	Units of measure of specified value

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Applying an arbitrary waveform using the multi-action verb "APPLY" (Note 1).



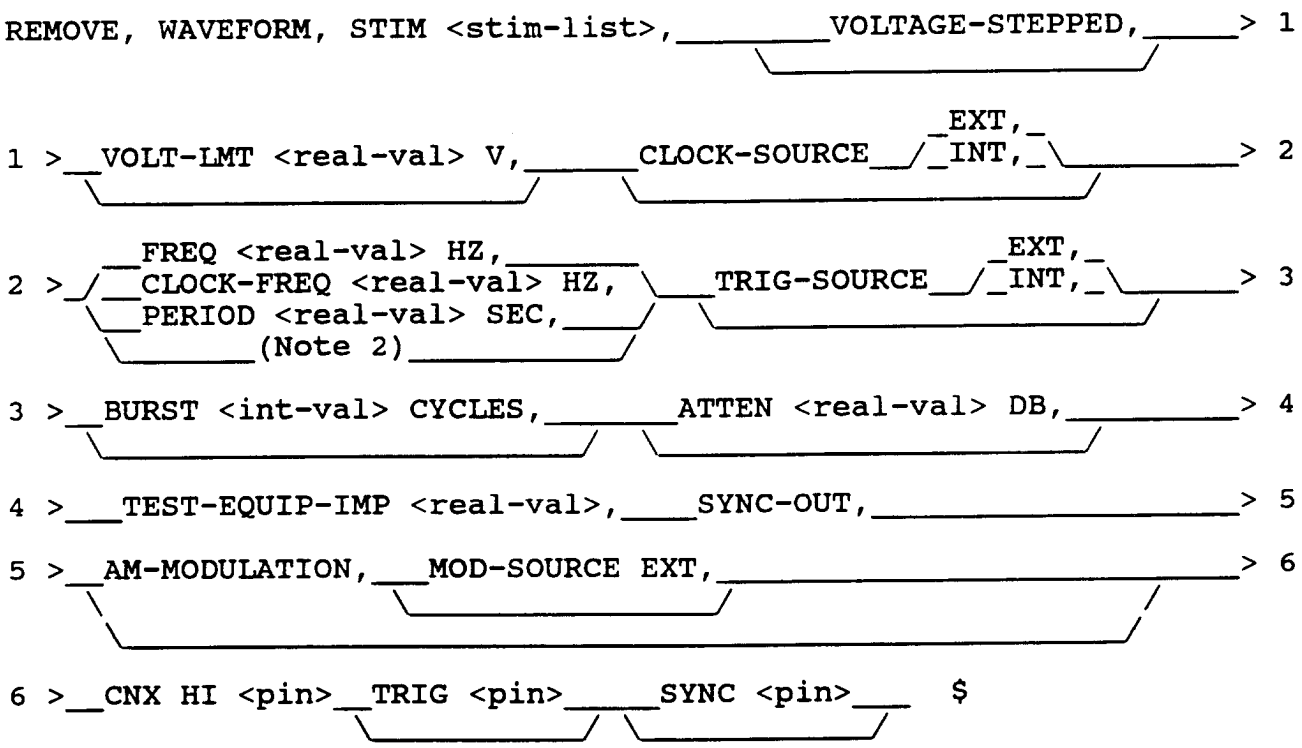
CIIL Expansion

```
FNC WAV :CH00
SET STIM <real-val> [<real-val>...]
[SET VLTS]
[SET VLTL <real-val>]
[SET CLSC (INT|EXT)]
[SET (FREQ|CLKR|PERI) <real-val>]                    See Note 4
[SET TRSC (INT|EXT)]
[SET BURS <integer-val>]
[SET ATTN <real-val>]
[SET TIMP <real-val]
[SET SYNO]
[SET AMOD [SET MDSC EXT]]
<cr><lf>

CON <path-data><cr><lf>                              See Note 5
CLS :CH00<cr><lf>
```


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Removing an arbitrary waveform using the multi-action verb "REMOVE" (Note 1).



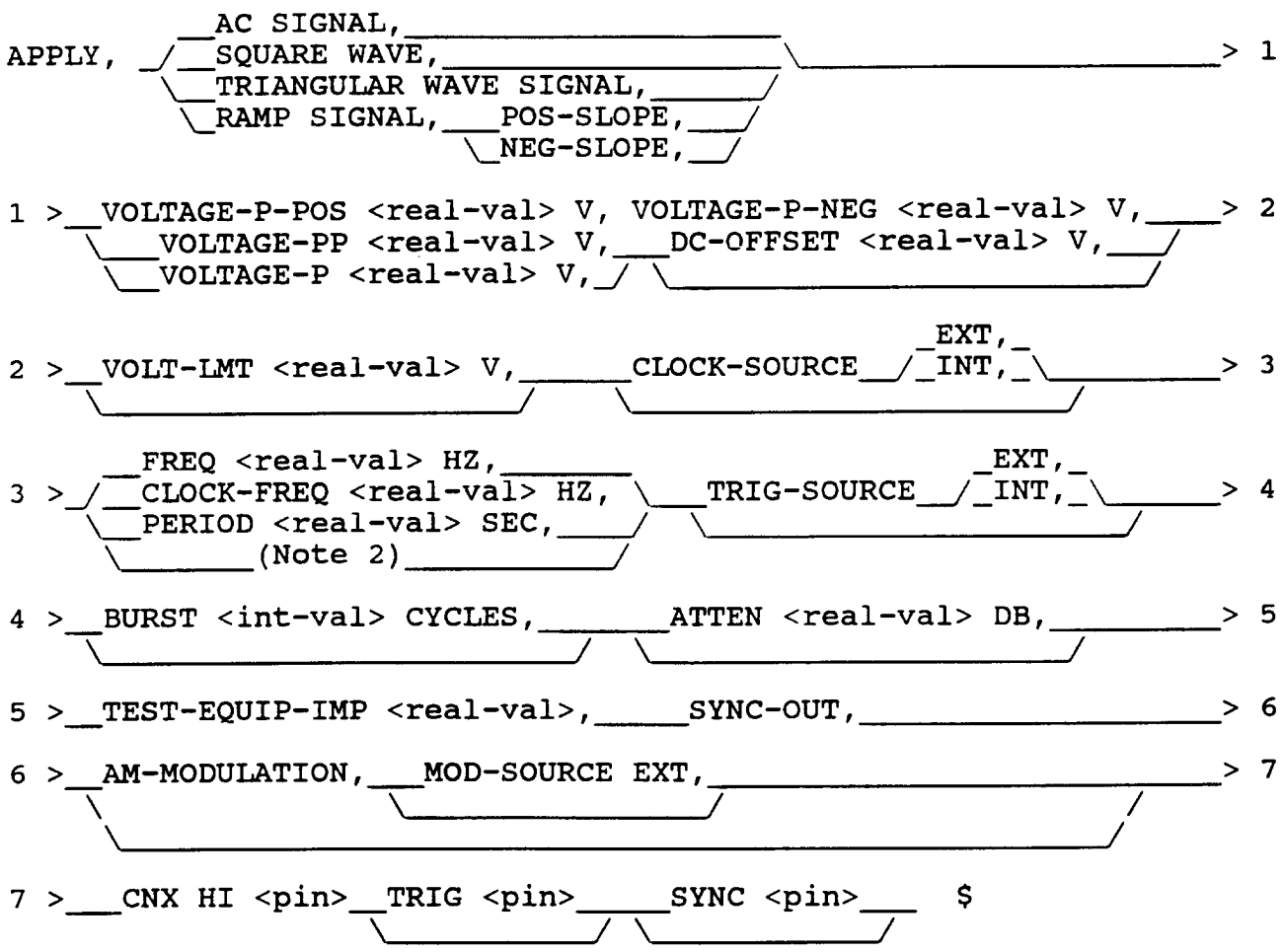
CIIL Expansion

RST WAV :CH00 <cr> <lf>

DIS <path-data> <cr> <lf> See Note 5

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Applying a standard waveform using the multi-action verb "APPLY" (Note 1).



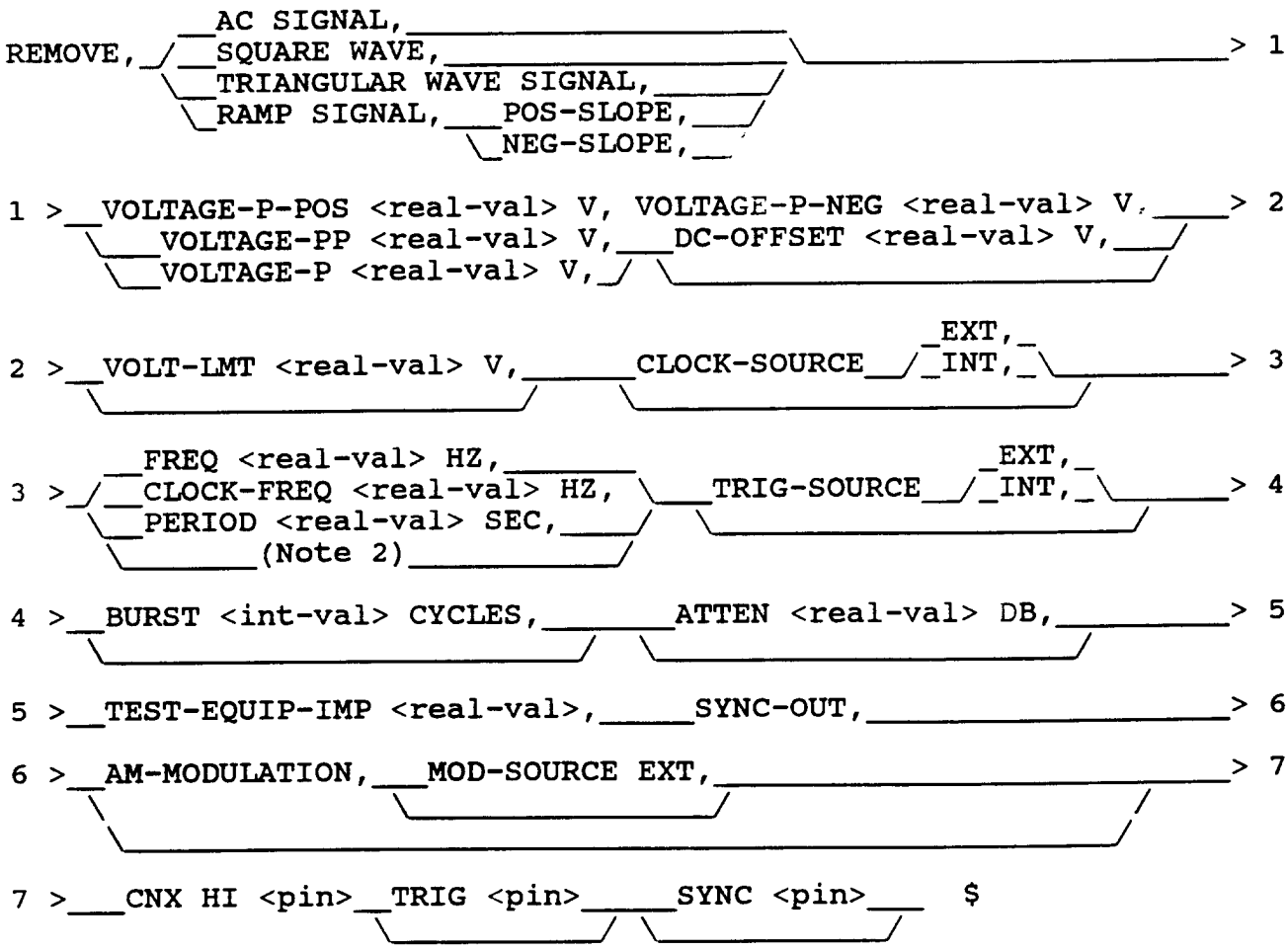
CIIL Expansion

```
FNC (ACS|SQW|TRI|RPS) :CH00
[SET (POSS|NEGS)]                                   See Note 3
[(SET VPKP <real-val> SET VPKN <real-val>)
  | ((SET VLPP <real-val>) | (SET VLPK <real-val>)
  [SET DCOF <real-val>])]
[SET VLTL <real-val>]
[SET CLSC (INT|EXT)]
[SET (FREQ|CLFR|PERI) <real-val>]                   See Note 4
[SET TRSC (INT|EXT)]
[SET BURS <integer-val>]
[SET ATTN <real-val>]
[SET TIMP <real-val>]
[SET SYNO]
[SET AMOD [SET MDSC EXT]]
<cr><lf>

CON <path-data><cr><lf>                             See Note 5
CLS :CH00<cr><lf>
```


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Removing a standard waveform using the multi-action verb "REMOVE" (Note 1).



CIIL Expansion

RST (ACS|SQW|TRI|RPS) :CH00 <cr><lf>

DIS <path-data><cr><lf> See Note 5

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NOTES:

1. This example uses a multi-action verb. It is possible to use single-action verbs. These will issue only subsets of the CIIL string for each ATLAS statement. For further details, consult the ATLAS Compiler manual.

2. The FREQ, CLOCK-FREQ, or PERIOD field is only optional for CLOCK-SOURCE EXT. With an external clock, the field is ignored and only serves as a comment field.

3. SET (POSS|NEGS) is only used with FNC RMP.

4. SET (FREQ|CLFR|PERI) is optional only for CLSC EXT. With an external clock, no action is taken by the VX4790A.

5. The CIIL mnemonics CON and DIS are issued to the test station switching system and are included here only for completeness.

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ATLAS Field Limits

The following section defines the valid ranges for the Arbitrary Waveform Generator programming parameters, as they apply to ATLAS.

TABLE 1: Arbitrary Waveforms

Field	Sub-Field	Range	Increments	Default	Notes
STIM	N/A	±10.22V	5 mV	None	1
		±5.11V	2.5 mV	None	1
		±0.1V	0.05 mV	None	1,2
VOLTAGE-STEPPED	N/A	N/A	N/A	VOLTAGE-STEPPED	3
VOLT-LMT	N/A	0V - 10.22V	5 mV	Full Scale	1,4
CLOCK-SOURCE	INT or EXT	N/A	N/A	CLOCK-SOURCE INT	5
FREQ or CLOCK-FREQ	N/A	0.75 Hz to 25 MHz	Any Value	None	5,6
PERIOD	N/A	40 nsec to 1.33 sec	Any Value	None	5,6
TRIG-SOURCE	INT or EXT	N/A	N/A	TRIG-SOURCE INT	7
BURST	N/A	1 to 255	1	Continuous	8
ATTEN	N/A	0 to 47 dB	Any Value	0 dB	9,10
TEST-EQUIP-IMP	N/A	0 to $10e^{8}$ Ohms	Any Value	50 Ohms	11
SYNC-OUT	N/A	N/A	N/A	No Sync	12
AM-MODULATION	N/A	N/A	N/A	No Modulation	10,13
MOD-SOURCE	EXT	N/A	N/A	MOD-SOURCE EXT	14

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TABLE 2: Standard Waveforms

Field	Sub-Field	Range	Increments	Default	Notes
POS-SLOPE	N/A	N/A	N/A	None	15
NEG-SLOPE	N/A	N/A	N/A	None	15
VOLTAGE-P-POS VOLTAGE-P-NEG VOLTAGE-P	N/A	±10.22V	5 mV	None	1,16,17
		±5.11V	2.5 mV	None	1,16,17
		±0.1V	50 µV	None	1,2,16,17
VOLTAGE-PP	N/A	0V - 20.44V	5 mV	None	1,17
		0V - 10.22V	2.5 mV	None	1,17
		0V - 0.2V	50 µV	None	1,2,17
DC-OFFSET	N/A	±10.22V	5 mV	0V	1,18
		±5.11V	2.5 mV	0V	1,18
		±0.1V	50 µV	0V	1,2,18
VOLT-LMT	N/A	0V - 10.22V	5 mV	Full Scale	1,4
CLOCK-SOURCE	INT or EXT	N/A	N/A	CLOCK-SOURCE INT	5
FREQ or CLOCK-FREQ	N/A	Table 4	Any Value	None	5,6
PERIOD	N/A	Table 4	Any Value	None	5,6
TRIG-SOURCE	INT or EXT	N/A	N/A	TRIG-SOURCE INT	7
BURST	N/A	1 TO 255	1	Continuous	8
ATTEN	N/A	0 to 47 dB	Any Value	0 dB	9,10
TEST-EQUIP-IMP	N/A	0 TO $10e^8$	Any Value	50 Ohms	11
SYNC-OUT	N/A	N/A	N/A	No Sync	12
AM-MODULATION	N/A	N/A	N/A	No Modulation	10,13
MOD-SOURCE	EXT	N/A	N/A	MOD-SOURCE EXT	14

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TABLE 3: VX4790A Attenuator

Attenuation	Resolution	Accuracy
0 - 7 dB	0.005 dB	±0.01 dB
7 - 13 dB	0.01 dB	±0.01 dB
13 - 19 dB	0.02 dB	±0.02 dB
19 - 27 dB	0.05 dB	±0.05 dB
27 - 33 dB	0.1 dB	±0.1 dB
33 - 39 dB	0.2 dB	±0.2 dB
39 - 47 dB	0.5 dB	±0.5 dB

TABLE 4: Standard Waveform Frequency and Period Ranges

Mode	Period		Frequency	
	Range	Minimum Recommended	Range	Maximum Recommended
AC SIGNAL	160 nsec to 1000 sec	333 nsec	0.001 Hz to 6.2499 MHz	3 MHz
SQUARE WAVE	80 nsec to 1000 sec	333 nsec	0.001 Hz to 12.5 MHz	3 MHz
TRIANGULAR WAVE	160 nsec to 1000 sec	1 µsec	0.001 Hz to 6.2499 MHz	1 MHz
RAMP SIGNAL	160 nsec to 1000 sec	1 µsec	0.001 Hz to 6.2499 MHz	1 MHz

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NOTES:

1. The voltage ranges and increments listed in Tables 1 and 2 assume the UUT is a 50 ohm load. Actual ranges and increments vary with UUT load and are discussed below. The VX4790A with Option 1M will take care of making sure the voltages specified in the ATLAS program are what is supplied at the UUT if the value of the UUT load is programmed in the "TEST-EQUIP-IMP" field. Based on the range of voltage outputs programmed and the UUT load specified, the VX4790A will also automatically select either the 10.22 Volt range or the 5.11 Volt range as the most appropriate range.

   The maximum range of 10.22 V specified for the VX4790A with a 50 ohm load increases as a function of the load as shown in the following equation:

$$V_{max} = \frac{\pm 11.242\ IMP}{IMP + 5}$$

   where IMP is the load at the UUT (see "TEST-EQUIP-IMP").

   To determine the actual increment value, first calculate the interim peak voltage (V_i). V_i is the largest absolute (unsigned) value of the sum of the signal points (or peak points in waveforms other than "APPLY, WAVEFORM"), plus the "DC-OFFSET", limited to the voltage limit specified in the "VOLT-LMT" field.

   Next, calculate V_{p1} using the following equation:

$$V_{p1} = \frac{V_i(IMP + 50)}{2\ IMP}$$

   If $V_{p1} > 5.11V$, the increment value will be:

$$\frac{5.5\ IMP}{IMP + 5} mV$$

   If $V_{p1} \leq 5.11V$, the increment value will be:

$$\frac{5\ IMP}{IMP + 50}\ mV$$

   Example:

   100000 APPLY, AC SIGNAL, VOLTAGE-P 5V, DC-OFFSET 2V,
   TEST-EQUIP-IMP 1000 OHMS

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$V_i = 7V$

$$V_{p1} = \frac{7 \times (1000 + 50)}{2 \times 1000} = 3.675V$$

$V_{p1} \leq 5.11V$

$$IncrementValue = \frac{5 \times 1000}{1000 + 50} = 4.762mV$$

2. The ±0.1022 V dc range is valid only with VX4790A Option 01. The voltage ranges and increments listed in Tables 1 and 2 assume the UUT is a 50 ohm load. Actual ranges and increments vary with UUT load and are discussed below. The VX4790A with Option 1M will take care of making sure the voltages specified in the ATLAS program are what is supplied at the UUT if the value of the UUT load is programmed in the "TEST-EQUIP-IMP" field. Based on the range of voltage outputs programmed and the UUT load specified, the VX4790A will also automatically select either the 10.22 Volt range, the 0.1022 Volt range, or the 5.11 Volt range as the most appropriate range. Use V_{p1} as calculated in Note 1.

   If $V_{p1} \leq 0.1022V$, the increment value will be:

$$\frac{0.1\ IMP}{IMP + 50}\ mV$$

   Otherwise, determine the increment value in as shown in Note 1.

3. The VX4790A is always in the "VOLTAGE-STEPPED" mode. The VX4790A will accept the resultant CIIL (SET VLTS). However, no action is taken, and the field only serves as a comment.

4. The "VOLT-LMT" field will cause the internal processor of the VX4790A to "clip" any specified voltage to the peak value specified (positive or negative). For example, if "APPLY, AC SIGNAL, VOLTAGE-PP 6.0V, DC-OFFSET -4.0V, VOLT-LMT 5.0V" is specified, the lower portion of the resultant sine wave, which would have had a -7.0 Volt negative peak, is "clipped" at -5.0 volts instead. A 10 V peak-to-peak sine wave with a 4.0 V VOLT-LMT would clip both the upper and lower portions of the sine wave at 4.0 and -4.0 volts. When this field is not specified, no software limits are applied.

5. With "CLOCK-SOURCE EXT", the "FREQ", "CLOCK-FREQ", and "PERIOD" fields are optional and only serves as a comment field. The VX4790A will ignore the resultant CIIL. When "CLOCK-SOURCE INT", or no "CLOCK-SOURCE" is specified, these fields are required.

6. The VX4790A will accept any programmed frequency or period within the specified range. The VX4790A will select the closest sample clock rate that it can achieve. For more information regarding the accuracy of this sample clock rate interpolation algorithm, refer to Appendix E.

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7. When "TRIG-SOURCE INT" or no "TRIG-SOURCE" is specified, the VX4790A will begin outputting the waveform immediately upon receipt of the "CLS :CH00<cr><lf>". When "TRIG-SOURCE EXT" is selected, the VX4790A will be armed upon receipt of "CLS :CH00<cr><lf>", but will not transmit the waveform until after an external trigger pulse is applied. For more information, refer to the External Trigger description in the Specifications section of this manual.

8. The "BURST" field allows the waveform to be output from 1 to 255 times. If no BURST is specified, the waveform will continue to transmit until an "RST" command is issued. If an "OPN" command is issued, the ARB will continue to generate the waveform, but the isolation relay will prevent the signal from being present at the signal connector.

9. The VX4790A will accept any programmed attenuation. The VX4790A will select the closest attenuation that it can achieve. For more information regarding the accuracy and resolution, refer to Table 3.

10. The attenuator and AM modulation cannot be used together.

11. The VX4790A will compensate the output voltage for UUT loads of greater than 50 ohms by using the "TEST-EQUIP-IMP" field. This field should contain the UUT load impedance (resistive vector only). The VX4790A will then program the output voltage for the voltage value times the compensation factor, up to the point of maximum output voltage. For more information, refer to Notes 1 and 2.

12. The SYNC-OUT field directs the VX4790A to output a pulse at each occurrence of an end-of-waveform. For more information, refer to the signal definitions in the Specifications section of this manual.

13. The AM-MODULATION field enables external control of the attenuation control port. For more information, refer to the A command description.

14. The VX4790A will accept the resultant CIIL (SET MDSC EXT). However, no action is taken, and this only serves as a comment field.

15. "POS-SLOPE" and "NEG-SLOPE" are exclusive required noun modifiers. One or the other must be specified for "APPLY, RAMP SIGNAL" ATLAS statements.

16. VOLTAGE-P-POS must have a greater value (more positive) than VOLTAGE-P-NEG.

17. VOLTAGE-P-POS and VOLTAGE-P-NEG or VOLTAGE-PP or VOLTAGE-P are required. VOLTAGE-P is one half of the VOLTAGE-PP value.

18. The absolute value of the combination of DC-OFFSET and VOLTAGE-P (or one half VOLTAGE-PP) must be less than 10.22 V (for a 50 ohm load).

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Appendix G
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

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User-Replaceable Parts

Part Description	Part Number
User Manual	070-9152–02
Label, Tek CDS	950-0943-00
Label, VXI	950-1068-00
Fuse, Micro 5 Amp 125 V Fast	159-0207-00
Fuse, Micro 2 Amp 125 V Fast	159-0128-00
Fuse, Micro 1 Amp 125 V Fast	159-0116-00
Fuse, Sub-min 0.500 Amp 125 V Fast	159-0221-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-6604-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00

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Appendix H
Options

Option 01

Option 01 adds up to 512 KSample Memory

Option 02

Option 02 adds up to 1 MSample Memory

Option 1M

Option 1M adds programming per CIIL Specification (MATE-STD-CIL).

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Appendix I: Performance Verification

This procedure verifies the performance of the VX4790A Arbitrary Waveform Generator. The test sequences may be performed in your current VXIbus system if it meets the requirements described in Table I–2. It is not necessary to complete the entire procedure if you are only interested in certain performance parameters. However, the verification of some parameters depends on the operation of functions which were checked before them so it is best to follow the order presented.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

Please familiarize yourself with the following conventions which apply throughout this procedure:

- Each test sequence begins with a table, similar to the one below, which provides information and requirements specific to that section. Following the table, you will be given instructions for interconnecting the VX4790A-under-test and the test equipment and for checking the performance parameters.

Equipment Requirements	Digital Volt Meter (item 3) Pattern Generator (item 4)
Prerequisites	All prerequisites listed on page A–46

The item number appearing after each piece of equipment refers to a line in Table I–1, *Required Test Equipment*, on page A–46.

- This procedure assumes that you will be using the National Instruments PC GPIB controller, and software (NI-488.2M). Within the test sequences you will be instructed to issue Interface Bus Interactive Control (ibic) commands to set up the VX4790A under-test system and other associated VXIbus test instruments. Please refer to the NI-488.2M User Manual for additional

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information. If you are using a different controller, simply substitute the equivalent command and response syntax in the test sequences.

Prerequisites

The test sequences in this procedure are valid when the following requirements are met:

- The VX4790A module covers are in place and the module is installed in an approved VXIbus mainframe according to the procedures in Section 2 *Preparation For Use,* of the Operating Manual.
- The VX4790A has passed the self test.
- The VX4790A is operating in an ambient temperature between 0° C and +50° C and has been operating for a warm-period of ten minutes.

Equipment Required

This verification procedure uses traceable signal sources and measurement instruments to check performance. Table I–1 lists the required equipment. You may use equipment other than the recommended examples if it meets the minimum requirements listed.

Table I–1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. Digitizing Oscilloscope	300 MHz bandwidth; 50 Ω input impedance; ≥ 1.5% DC vertical accuracy, with frequency readout.	Tektronix TDS 460	Checking signal timing, amplitude, and phase
2. Oscilloscope Probe	250 MHz, 10X, 10 MΩ, 12.7 pF	Tektronix P6130	Checking signal timing, amplitude, and phase
3. Digital Volt Meter (DVM) with Test Lead Set	5-1/2 digit, 100 VDC range, accuracy > 0.002 %.	FLUKE 8842A	Checking isolation and voltage accuracy
4. Pattern Generator	25 MHz, TTL, ±1.5 VDC	Tektronix VX4750	Checking external clock, modulation, and trigger
5. SMB to BNC Adapter Cable (two required)	50 Ω, SMB male to BNC male	Tektronix VX1729 Data Cable	Interconnect electrical signals
6. 50 Ω BNC Coxial Cable	50 Ω, BNC male connectors	Tektronix part number 012-0057-01	Interconnect electrical signals
7. BNC Female to Dual Banana	50 Ω impedance; BNC female, Dual Banana plug	Tektronix part number 103-0090-00	Interconnecting electrical signals
8. Feed Through Termination	50 Ω impedance; BNC female to BNC male connectors	Tektronix part number 011-0129-00	Provides 50 Ω load to signals

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Table I–1: Required Test Equipment (Cont.)

Item Number and Description	Minimum Requirements	Example	Purpose
9. BNC Female to BNC Female (barrel connector)	50 Ω impedance; BNC female to BNC female	Tektronix part number 103-0028-00	Interconnect electrical signals
10. BNC T	50 Ω impedance; BNC female to BNC female to BNC male	Tektronix part number 103-0030-00	Interconnect electrical signals

VX4790A-Under-Test Configuration

In order to perform this verification procedure, the VX4790A must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table I–2.

Table I–2: Elements of a Minimum VX4790A Under-Test System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	Two available slots, one for the VX4790A and one for the Pattern Generator in addition to the Slot 0 controller	Tektronix VX1401, VX1400A, VX1405, VX1410	Power, cooling, and backplane for VXIbus modules
2. Slot 0 Controller	Resource Mgr., Slot 0 Device Functions, IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Slot 0 functions., Resource Mgr., and GPIB/VXIbus interface
3. IBM PC or compatible	286 Processor; Talker/Listener/ Controller GPIB card, and software	IBM 486 PC National Instruments GPIB PC2A card & NI-488.2M software	System Controller
4. GPIB Cable	≈ 2 m length, GPIB connectors on each end	Tektronix part number 012–0991-00	Connecting PC GPIB to Slot 0
5. VX4790A Under-Test	Not applicable	Not applicable	Verify its performance

Test System Configuration

Table I–3 describes the VXIbus system configuration which is assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in the test results in place of those recommended in Table I–3.

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Table I–3: VXIbus Test System Configuration

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	13 (0d, hexadecimal)	13
VX4790A under-test	VX4790	Slot 1	01	1
VX4750	VX4750	Slot 2	02	2

Test Record

Photocopy the Test Record, and use it to record the performance verification results for your module.

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Table I–4: VX4790A Test Record

VX4790A Serial Number:	Temperature and Relative Humidity:
Date of Last Calibration:	Verification Performed by:
Certificate Number:	Date of Verification:

VXIbus Interface		**Logical Address, IEEE Address, Slot No., MFG., Model, etc.**	
Table Command Response	1st. Response		
	2nd Response		
	3rd Response		
		Passed	**Failed**
Program Command Response	Memory Test		
	Interrupt SRQ		

DC Voltage Accuracy (50 Ω)	**Program**	10.22 V	6.81 V	3.40 V	0..000 V	–3.400 V	–6.81 V	–10.23 V
10 V Range	**Max.**	10.42 V	7.01 V	3.60 V	0.200 V	–3.200 V	–6.61 V	–10.03 V
	Measure							
	Min.	10.02 V	6.61 V	3.20 V	–0.200 V	–3.600 V	–7.01 V	–10.43 V
5 V Range	**Program**	5.11 V	3.41 V	1.705 V	0.000 V	–1.705 V	–3.41 V	–5.11 V
	Max.	5.15 V	3.45 V	1.745 V	0.040 V	–1.665 V	–3.37 V	–5.07 V
	Measure							
	Min.	5.07 V	3.37 V	1.665 V	–0.040 V	–1.745 V	–3.45 V	–5.15 V
0.1 V Range	**Program**	0.1022 V	0.0681 V	0.0341 V	0.000 V	–0.0341 V	–0.0682 V	–0.1023 V
	Max.	0.1056 V	0.0715 V	0.0375 V	0.0034 V	–0.0307 V	–0.0648 V	–0.0989 V
	Measure							
	Min.	0.0988 V	0.0647 V	0.0307 V	–0.0034 V	–0.0375 V	–0.0716 V	–0.1057 V

ARB OUT Control Functions		**Passed**	**Failed**
Function Generator	Sine		
	Square		
	Triangle		
	Sawtooth		
Low Pass Filter	5 MHz		
	500 kHz		
	50 kHz		

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ARB OUT Control Functions		Passed	Failed
Attenuation	100%		
	75%		
	50%		
	20%		
	0%		
Modulation	+1.5 VDC		
	+0.75 VDC		
	+0.0 VDC		
	–0.75 VDC		
	–1.5 VDC		
SYNC* Out Pulse	0 V Step		
	1 V Step		
	2 V Step		
	3 V Step		
Clock and Trigger		**Passed**	**Failed**
Phase Lock Loop	25 MHz		
	22 MHz		
	19 MHz		
	15 MHz		
	12.5 MHz		
Frequency Scaling	1/1		
	1/2		
	1/32		
	1/128		
EXT CLK*	10 kHz		
	100 kHz		
	1 MHz		
EXT TRIG*	Triggered Sine Wave		

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VXIbus Trigger		Triggered by VXIbus		Triggered Asserted to VXIbus		
		Passed	Failed	Passed	Failed	
	TTLTRG0*					
	TTLTRG1*					
	TTLTRG2*					
	TTLTRG3*					
	TTLTRG4*					
	TTLTRG5*					
	TTLTRG6*					
	TTLTRG7*					

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Self Test

The VX4790A includes a built-in self test feature (BITE) which executes automatically each time the power is turned on and also when the Internal Self Test (STEST) command is issued. BITE utilizes internal test patterns and references to test memory, voltage, and frequency accuracy, and basic functionality. No external test equipment is required.

During the self test, front panel signals are disconnected by isolation relays. A limited RAM test is performed on the first 16k bytes of ARB memory. Next a frequency and voltage test is performed by loading a test waveform and sampling with an internal A/D converter (468 kHz rate for 160k samples). Finally a voltage amplitude test is performed by running the ARB pattern at a variety of levels and verifying the resulting voltage with an internal reference.

The limited memory test is due to the five second time constraint of the VXIbus initialization specification. The entire RAM memory may be tested following system initialization with the SMEMTEST command.

In addition to BITE, front panel indicator lights display the current status of power, the assertion of SYSFAIL*, and module ERROR conditions. The GETERR? command may be used at any time during operation to determine the current state of the module.

Following the VXIbus system startup sequence, the green PWR light on the VX4790A front panel indicates that the self test has passed and that the power supplies are operational. If the +5 V, ±24 V (including the derived ±17.5 V), or –5.2 V power supplies fail, or if the +5 V, ±24 V, or –5.2 V fuses open, the PWR light will be off and the red FAILED light will be on. This condition indicates that SYSFAIL* has been asserted due to the module failure.

NOTE. *If you experience an error indication from the Slot 0 Resource Manager, the VX4790A-under-test, or other VXIbus modules, investigate and correct the problem before proceeding. Common items to check are possible logical address conflicts, breaks in the VXIbus daisy chain signals, improper seating of a module, loose GPIB cable, improperly set Slot 0 single step switch, or loose or blown fuses.*

Performance Verification Tests

The verification sequences in this procedure contain setup instructions for the example test equipment listed in Table I–1, on page A–46. You may use equipment other than the recommended examples if it meets the minimum requirements listed. The order of execution of the test sequences has been chosen to minimize system setup and programming requirements. Although not

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essential, it is recommended that you follow the order presented, as some tests rely on parameters which were verified before them.

VXIbus Interface

This sequence verifies that the VX4790A configures correctly and communicates properly with your GPIB system controller.

Equipment Requirements	No additional test equipment is required for this sequence.
Prerequisites	All prerequisites listed on page A–46

***NOTE**. If you are using National Instruments NI-488.2 software you may wish to select the buffer 1 mode to allow viewing of the complete ASCII device response. Just type buffer 1.*

1. To verify the system configuration, send the TABLE command to the Slot 0 Resource Manager and confirm the responses shown in Table I–5. Your configuration may not be identical, but the responses should be similar.

Table I–5: VXIbus System Configuration

Command to Type	Response to Verify
`ibic`	
`ibfind VX4521`	
`ibwrt "table"`	
`ibrd 200`	`03`
`!`	`LA 0, IEEE 13, Slot 0, MFG FFDh, MODEL VX4521, PASS, , RM..`
`!`	`LA 1, IEEE 01, Slot 1, MFG FFDh, MODEL VX4790A, PASS TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL`
`!`	`LA 2, IEEE 02, Slot 2, MFG FFDh, MODEL VX4750, PASS TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL`

2. Perform the extended memory test and verify that there are no pending errors with the following commands:

   ```
   ibfind VX4790

   ibwrt "smemtest"
   ```
   (Observe XTRG light blinks for each 64K tested)

   ```
   ibwrt "geterr?"
   ```


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```
ibrd 100
```
(Observe 00,NO ADDITIONAL ERRORS TO REPORT...)

3. Verify the VX4790A VXIbus interrupt capability with the following steps:

NOTE*. Make sure your Slot 0 controller and the VX4790A-under-test are set to the same interrupt level. Also, if you are using National Instruments NI-488.2 software, make sure Auto Serial Polling is disabled to prevent the SRQ from being reset prior to a visual check.*

a. Enable the VX4790A to generate a VXIbus Request True interrupt and force an interrupt due to a command syntax error as follows:

```
ibwrt "15i"
```

```
ibwrt "error"
```
(Observe VX4790A ERROR light on)

```
ibrd 0
```
(Observe VX4521 Slot 0 2nd digit indicates S for SRQ)

NOTE*. The zero length read command serves to unaddress the Slot 0 controller allowing it to detect the VXIbus interrupt and assert the SRQ.*

b. Check that the ERROR light is on and that the VX4521 indicates an S in the second digit of the front panel display, indicating an SRQ pending.

c. Perform a Serial Poll of the VX4790A and verify that the Slot 0 SRQ is no longer asserted (Note a 48 hexadecimal response indicating that the VX4790A was the interrupting module).

```
ibrsp
```
(Observe VX4521 no longer displays S.)

d. Read the VX4790A error and verify that the ERROR light turns off.

```
ibrd 100
```
(Observe 40,UNRECOGNIZED COMMAND...)

```
!
```
(Observe 00,NO ADDITIONAL ERRORS TO REPORT...)

DC Voltage Accuracy

This sequence verifies the programmable DC level of the ARB OUT signal driving a 50 Ω load.

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Equipment Requirements	Digital Volt Meter (item 3) BNC to Dual Banana (item 7) SMB to BNC Cable (item 5) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. Connect the VX4790A ARB OUT signal to the DVM using the SMB to BNC cable, the 50 Ω terminator, and the BNC to Dual Banana adaptor.

2. With the commands below, reset the VX4790A to its power-up state, select the 10 V range, and close the ARB OUT relay. Then set up an output voltage of 10.22 VDC, and assert a trigger (z is the breakpoint and end of waveform voltage designator). Verify the accuracy to be within ±1.0% of full scale (±200 mV):

   ```
   set VX4790

   ibwrt "k;setvoltr10;1o"

   ibwrt "10.22z;t"
   ```
   (Observe 10.22 VDC ±200 mV)

3. Check the additional voltages listed in Table I–6.

Table I–6: 10 V Range Verification

Command to Send	DC Voltage to Verify
`ibwrt "q;6.81z;t"`	6.610 to 7.010 VDC
`ibwrt "q;3.4z;t"`	3.200 to 3.600 VDC
`ibwrt "q;0z;t"`	–0.200 to 0.200 VDC
`ibwrt "q;-3.4z;t"`	–3.600 to –3.200 VDC
`ibwrt "q;-6.81z;t"`	–7.010 to –6.610 VDC
`ibwrt "q;-10.23z;t"`	–10.43 to –10.03 VDC

4. Reset the VX4790A to the 5 VDC range and verify the voltages in Table I–7 to be within ±0.4% of full scale (±40 mV).

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Table I–7: 5 V Range Verification

Command to Send	DC Voltage to Verify
`ibwrt "setvoltr5"`	
`ibwrt "q;5.11z;t"`	5.070 to 5.150 VDC
`ibwrt "q;3.41z;t"`	3.370 to 3.450 VDC
`ibwrt "q;1.705z;t"`	1.665 to 1.745 VDC
`ibwrt "q;0.00z;t"`	–0.040 to 0.040 VDC
`ibwrt "q;-1.705z;t"`	–1.745 to –1.665 VDC
`ibwrt "q;-3.41z;t"`	–3.450 to 3.370 VDC
`ibwrt "q;-5.11z;t"`	–5.150 to –5.070 VDC

5. Reset the VX4790A to the 0.1 VDC range and verify the voltages in Table I–8 to be within ±1.7% of full scale (±3.4 mV).

Table I–8: 0.1 V Range Verification

Command to Send	DC Voltage to Verify
`ibwrt "setvoltr0.1"`	
`ibwrt "q;0.1022z;t"`	0.0988 to 0.1056 VDC
`ibwrt "q;0.0681z;t"`	0.0647 to 0.7150 VDC
`ibwrt "q;0.0341z;t"`	0.0307 to 0.0375 VDC
`ibwrt "q;0.00z;t"`	–0.0034 to 0.0034 VDC
`ibwrt "q;-0.0341z;t"`	–0.0375 to –0.0307 VDC
`ibwrt "q;-0.0682z;t"`	–0.0716 to –0.0648 VDC
`ibwrt "q;-0.1023z;t"`	–0.1057 to –0.0989 VDC

Stored Waveforms

This sequence verifies the functional generation of the stored Sine, Square, Triangle, and Sawtooth waveforms. The patterns are tested at 1 kHz in order to present a clean and undistorted appearance. The quality of the waveforms will diminish as the frequency approaches the maximum sample frequency of 25 MHz.

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Equipment Requirements	Oscilloscope (item 1) SMB to BNC Cable (item 5) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. Connect the VX4790A ARB OUT signal to CH1 of the oscilloscope using the SMB to BNC cable and the 50 Ω terminator. Set the oscilloscope for a 1 MΩ input, 2 V/div. and 200 µs/div.
2. Reset the VX4790A to its power-up state and close the ARB OUT relay. Then set up a 5 V_p (10 V_{pp}), 1 kHz sine wave, assert a trigger and verify the waveform on the oscilloscope.

   ```
   set VX4790

   ibwrt "k;1o"

   ibwrt "setsine 5 1e3;t"
   ```
   (Observe 10 V_{pp} , 1 kHz sine wave)
3. Check the additional waveforms listed in Table I–9:

Table I–9: Stored Waveform Verification

Command to Send	Waveform to Verify
`ibwrt "q;setsine 5 1e3;t"` (step 2 above repeated for table continuity)	10 $V_{pp,}$ 1 kHz sine wave
`ibwrt "q;setsquare 5 -5 1e3;t"`	±5 V, 1 kHz square wave
`ibwrt "q;settriang 5 -5 1e3;t"`	±5 V, 1 kHz triangular wave
`ibwrt "q;setsawtoo 5 -5 1e3;t"`	±5 V, 1 kHz sawtooth wave

Low Pass Filter

This sequence verifies the functionality of the 5 MHz, 500 kHz, and 50 kHz low pass filter to smooth the ARB OUT waveform while having minimal effect on its amplitude.

Equipment Requirements	Oscilloscope (item 1) SMB to BNC Cable (item 5) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

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1. Connect the VX4790A ARB OUT signal to CH1 of the oscilloscope using the SMB to BNC cable and the 50 Ω terminator. Set the oscilloscope for a 1 MΩ input, 5 V/div, and 10 ms/div.

2. Reset the VX4790A to generate a 10 V_p (20 $V_{pp)}$, 1 MHz sine wave and verify the waveform on the oscilloscope. Then assert the 5 MHz lowpass filter and verify that the steps in the sine wave are smoothed and that the amplitude is not noticeably reduced. Finally unassert the 5 MHz filter and observe the original waveform roughness.

   ```
   set VX4790

   ibwrt "k;Setsine 10 1e6;1o;t"
   ```
   (Observe rough sine wave)

   ```
   ibwrt "1L"
   ```
   (Observe smooth waveform, < 10% amplitude reduction)

   ```
   ibwrt "0L"
   ```
   (Observe original waveform roughness)

3. Reset the VX4790A to generate a 100 kHz sine wave and verify the waveform on the oscilloscope. Then assert the 500 kHz lowpass filter and verify that the steps in the sine wave are smoothed and that the amplitude is not noticeably reduced. Finally unassert the 500 kHz filter and observe the original waveform roughness.

   ```
   ibwrt "k;Setsine 10 1e5;1o;t"
   ```
   (Observe rough sine wave)

   ```
   ibwrt "3L"
   ```
   (Observe smooth waveform < 5% amplitude reduction)

   ```
   ibwrt "2L"
   ```
   (Observe original waveform roughness)

4. Reset the VX4790A to generate a 10 kHz sine wave and verify the waveform on the oscilloscope. Then assert the 50 kHz lowpass filter and verify that the steps in the sine wave are smoothed and that the amplitude is not noticeably reduced. Cancel the 50 kHz filter and observe the original waveform roughness.

   ```
   ibwrt "k;Setsine 10 1e4;1o;t"
   ```
   (Observe sine wave)

   ```
   ibwrt "5L"
   ```
   (Observe smooth waveform, < 5% amplitude reduction)

   ```
   ibwrt "4L"
   ```
   (Observe original roughness)

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Attenuation & Modulation

This sequence verifies the programmable attenuation and external modulation/attenuation of the ARB OUT signal.

Equipment Requirements	Oscilloscope (item 1) Pattern Generator (VX4750, item 4) SMB to BNC Cable, two required (item 5) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. Connect the VX4790A ARB OUT signal to CH1 of the oscilloscope using the SMB to BNC cable and the 50 Ω terminator. Set the oscilloscope for a 1 MΩ input, 2 V/div, and 200 µs/div.
2. Connect the VX4750 FUNC OUT signal to the VX4790A AM IN using a second SMB to BNC cable.
3. Reset the VX4790A to its power-up state and close the ARB OUT relay. Set up a 10 V_p (20 V_{pp}), 1 kHz sine wave and verify the waveform on the oscilloscope. Finally, set the attenuation to 75% and verify the corresponding amplitude reduction of waveform.

   ```
   set VX4790

   ibwrt "k;1o"

   ibwrt "Setsine 10 1e3;t"
   ```
   (Observe 1 kHz, 20 V_{pp} sine wave)

   ```
   ibwrt "75%"
   ```
   (Observe 1 kHz 15 V_{pp} sine wave)
4. Check the additional internal attenuation values as shown in Table I–10.

Table I–10: Internal Programmable Attenuation Verification

Command to Send	Waveform to Verify
`ibwrt "100%"` (step 3 above repeated for table continuity)	20 V_{pp} sine wave
`ibwrt "75%"` (step 3 above repeated for table continuity)	15 V_{pp} sine wave
`ibwrt "50%"`	10 V_{pp} sine wave
`ibwrt "20%"`	4 V_{pp} sine wave
`ibwrt "0%"`	0.0 V_{pp} sine wave

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5. Reset the VX4790A to enable external modulation. Then set up the VX4750 to provide an initial +1.5 VDC reference. Verify that the VX4790A sine wave amplitude is 20 V_{pp}.

   ```
   ibwrt "1a"

   ibfind VX4750

   ibwrt "Wave Sine;Freq 100;Ampl 0;Imp 10e6;Ofst 1.5"
   ```

   (Observe 20 V_{pp} sine wave)

6. Check the additional external attenuation values listed in Table I–11.

Table I–11: External Attenuation/Modulation Verification

Command to Send to the VX4750	Waveform to Verify
`ibwrt "Ofst 1.5"` `(step 5 repeated for continuity)`	20 V_{pp} sine wave
`ibwrt "Ofst 0.75"`	15 V_{pp} sine wave
`ibwrt "Ofst 0"`	10 V_{pp} sine wave
`ibwrt "Ofst -0.75"`	5 V_{pp} sine wave
`ibwrt "Ofst -1.5"`	0.0 V_{pp} sine wave

SYNC* Output

This sequence verifies the SYNC* output signal and its programmable positioning within the ARB OUT pattern memory.

Equipment Requirements	Oscilloscope (item 1) SMB to BNC Cable, two required (item 5) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. Connect the VX4790A ARB OUT signal to CH1 of the oscilloscope using the SMB to BNC cable and the 50 Ω terminator. Set the oscilloscope for a 1 MΩ input, 2 V/div and 10 µs/div.

2. Connect the VX4790A SYNC* signal to CH2 of the oscilloscope using a second SMB to BNC cable. Set the oscilloscope for a 1 MΩ input and 2 V/div.

3. Reset the VX4790A to power-up default parameters, enable a user-defined SYNC* pulse address designation, set the sample clock for 100 kHz, and enable the output relay. Then load the ARB memory with a 0, 1, 2, and 3 V

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step waveform having a SYNC* pulse coincident with the 0 V step. Verify that the negative-going SYNC* pulse is coincident with the 0 V step.

```
set VX4790

ibwrt "k;1u;1e5f;1o"

ibwrt "0n;0yv;1v;2v;3w;t"
```
(Observe SYNC*aligned with 0V step)

4. Set the SYNC* pulse to be coincident with the additional voltage steps and verify alignment as indicated in Table I–12:

Table I–12: SYNC* Verification

Command to Send to the VX4790	Waveform to Verify
`ibwrt "0n;0yv;1v;2v;3w;t"` (step 3 above repeated for table continuity)	SYNC* coincident with the 0 V step
`ibwrt "0n;0v;1yv;2v;3w;t"`	SYNC* coincident with the 1 V step
`ibwrt "0n;0v;1v;2yv;3w;t"`	SYNC* coincident with the 2 V step
`ibwrt "0n;0v;1v;2v;3yw;t"`	SYNC* coincident with the 3 V step

Phase Lock Loop and Frequency Scaling

This sequence verifies Phase Locked Loop frequency synthesis from 12.5 MHz to 25 MHz and frequency scaling.

Equipment Requirements	Oscilloscope (item 1) SMB to BNC Cable (item 5) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. Connect the VX4790A SMP CLK signal to CH1 of the oscilloscope using the SMB to BNC cable and the 50 Ω terminator. Set the oscilloscope for a 1 MΩ input, 2 V/div, and 20ns/div.

2. Reset the VX4790A first memory location to a negative 5 V level, the second location to a positive 5 V level (w designates end of waveform voltage), and enable the ARB OUT relay. Then set the sample clock to 25 MHz, assert a trigger, and verify the 25 MHz SMP CLK* on the oscilloscope.

```
set vx4790

ibwrt "k;0n-5v5w;1o"
```


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```
ibwrt "25e6f;t"
```
(Observe 25 MHz SMP CLK*)

3. Check the additional frequencies as indicated in Table I–13:

Table I–13: Phase Locked Loop Verification

Command to Send to the VX4790	Waveform to Verify
`ibwrt "25e6f;t"` (step 2 above repeated for table continuity)	25 MHz
`ibwrt "22e6f;t"`	22 MHz
`ibwrt "19e6f;t"`	19 MHz
`ibwrt "15e6f;t"`	15 MHz
`ibwrt "12.5e6f;t"`	12.5 MHz

4. To verify the frequency division function, reset the VX4790A to a ±5 V, 25 MHz square wave. Then specify a scaling integer and verify the resulting SMP CLK* frequency as indicated in Table I–14.

```
ibwrt "k;On-5v5w;t;1o"
```
(Observe 25 MHz square wave)

Table I–14: Clock Division Verification

Command to Send to the VX4790	Frequency to Verify
`ibwrt "1d"` `(step 4 repeated for continuity)`	25 MHz
`ibwrt "2d"`	12.5 MHz
`ibwrt "32d"`	781 kHz
`ibwrt "128d"`	195 kHz

External Clock

This sequence verifies the operation of the front panel EXT CLK*. When enabled, the external clock is used as the sample clock to generate the ARB OUT pattern. The waveform frequency does not depend on the frequency set by the f, d, or p commands.

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Equipment Requirements	Oscilloscope (item 1) VX4750 external clock source (item 4) SMB to BNC cable, two required (item 5) BNC to BNC cable (item 6) BNC T adaptor (item 10) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. Connect the VX4790A ARB OUT signal to CH1 of the oscilloscope. Set the oscilloscope to a 1 MΩ input, 5 V/div, 500 µs/div, and CH1 trigger.
2. Connect the VX4750 FUNC OUT signal to the VX4790A EXT CLK input and also to CH2 of the oscilloscope using a BNC T, a BNC to BNC cable, and an SMB to BNC cable. Set CH2 of the oscilloscope for a 1 MΩ input and 2 V/div.
3. Reset the VX4790A first memory location to a negative 5 V level, the second location to a positive 5 V level, enable the EXT CLK input as the sample clock, close the output relay, and trigger the waveform.

   ```
   set VX4790

   ibwrt "k;On-5v5w;1C;1o;t"
   ```

4. Set up the VX4750 to generate a 5 V_{pp}, 1 kHz square wave with an offset of 2.5 VDC, and an output impedance of 1 MΩ.

   ```
   set VX4750

   ibwrt "Rst;Wave Sqr;Ampl 5Vpp;Freq 1kHz;Ofst 2.5V;Imp 1e6
   Ohm"
   ```

5. Verify that the ARB OUT signal changes state coincident with the externally supplied sample clock, resulting in a waveform frequency which is one half the frequency of the EXT CLK.
6. Check the additional EXT CLK input frequencies as indicated in Table I–13:

Table I–15: EXT CLK Input Verification

Command to Send to the VX4750	ARB OUT Frequency to Verify
`ibwrt "Freq 10kHz"`	5 kHz
`ibwrt "Freq 100kHz"`	50 kHz
`ibwrt "Freq 1MHz"`	500 kHz

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External Trigger

This sequence verifies the functionality of the front panel EXT TRG* input and the VXIbus TTLTRG* signals.

Equipment Requirements	Oscilloscope (item 1) Oscilloscope Probe (item 2) VX4750 external clock source (item 4) SMB to BNC cable, two required (item 5) BNC to BNC barrel adaptor (item 9) BNC to BNC cable (item 6) 50 Ω BNC Feed Through Termination (item 8)
Prerequisites	All prerequisites listed on page A–46

1. To verify the front panel EXT TRG input perform the following steps:

   a. Connect the VX4790A ARB OUT signal to CH1 of the oscilloscope using an SMB to BNC cable and a 50 Ω Terminator. Set the oscilloscope for a 1 MΩ input, 5 V/div, and 500 µs/div.

   b. Connect the VX4750 TRIG OUT signal to the VX4790A EXT TRIG* input with a second SMB to BNC cable.

   c. Reset the VX4790A to generate a ±5 V, 1 kHz square wave, to enable the external trigger, and enable the output relay.

   ```
   set VX4790

   ibwrt "k;setsquare 5 -5 1000;1x;1o"
   ```

   d. Reset the VX4750 to generate a sine wave which concurrently generates a trigger on the TRIG OUT connector. Verify on the oscilloscope that the VX4790A triggers concurrently.

   ```
   set VX4750

   ibwrt "rst;wave sine"
   ```
   (Observe initiation of square wave)

2. To verify recognition of VXIbus TTLTRG* signals perform the following steps:

   a. Disconnect theVX4790A EXT TRIG input from the VX4750 TRIG OUT

   b. Reset the VX4790A to generate a ±5 V, 1 kHz square wave, enable a trigger from TTLTRG0*, and enable the output relay.

   ```
   set VX4790
   ```


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```
ibwrt "k;setsquare 5 -5 1000;20x;1o"
```

c. Reset the VX4750 to generate a sine wave which concurrently generates a trigger on the VXIbus TTLTRG0* line. Verify on the oscilloscope that the VX4790A triggers concurrently.

```
set VX4750

ibwrt "rst;trgo vxi 0;wave sine"
```
(Observe VX4790A square wave)

d. Check the additional TTLTRG* lines by repeating steps b and c, substituting `2#x` in step b and `VXI #` in step c where # = 1, 2, 3, 4, 5, 6, and 7.

3. The following steps verify the ability of the VX4790A to drive the VXIbus TTLTRG* lines. The process uses the VX4790A front panel SYNC* output signal connected back into the front panel EXT TRIG* input and is then connected to the VXIbus TTLTRG* backplane signals. The VX4790A SYNC* signal will then be used to repetitively trigger (or gate) the VX4750.

a. Connect the VX4790A SYNC* output to its EXT TRIG* input using two SMB to BNC cables and a barrel connector.

b. Connect the VX4750 FUNC OUT to CH2 of the oscilloscope. Set the oscilloscope for a 50 Ω input, 5 V/div, and 500 µs/div.

c. Connect a probe to CH1 of the oscilloscope and monitor the VX4790A. ARB OUT signal.

d. Set up the VX4750 to generate a 10 $V_{pp,}$ 1 kHz sine wave to be repetitively triggered from the VXIbus TTLTRG0* backplane signal.

```
set VX4750

ibwrt "Rst;Wave Sine;Freq 2kHz;Ampl 10Vpp;Trgi VXI 0"
```

e. Reset the VX4790A to generate a ±5V, 1 kHz square wave, to enable the front panel EXT TRIG* input signal to be coupled to the VXIbus, TTLTRG0*, to enable the ARB OUT relay, and to assert a trigger.

```
set vx4790

ibwrt "k;setsquare 5 -5 1000;30X;1o;t"
```

f. Using the oscilloscope probe, observe the VX4790A ARB OUT signal and verify that a VX4750 sine wave is triggered during each occurrence of the 5 V level of the square wave from the VX4790A and not triggered during the –5 V level.

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g. Check the additional TTLTRG* lines by repeating steps d and e, and substituting `VXI # ` in step d and `3#x` in step e where the # = 1, 2, 3, 4, 5, 6, and 7.

This completes the VX4790A verification procedure.

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Warning

The following servicing instructions are for use only by qualified personnel. To avoid personal injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to General Safety Summary and Service Safety Summary prior to performing any service.

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Appendix J: Adjustment Procedure

In order to meet its published specification, the VX4790A must be adjusted every twelve months. The adjustment should be performed at the temperature at which the module will be operating. If this is not feasible, or the module will be operating over a wide temperature variation, consult the temperature drift specification in the Operating Manual.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

This procedure assumes a system configuration as described in Table J–3 and that you will be using the National Instruments PC-GPIB controller and software (NI-488.2M). The adjustment steps instruct you to issue the corresponding Interface Bus Interactive Control (ibic) commands to set up the VX4790A and other associated VXIbus test instruments. Please refer to the NI-488.2M User Manual for additional information. If you are using a different system controller, simply substitute the equivalent commands in the adjustment steps. Command characters may be sent in upper or lower case.

Prerequisites

Proper adjustment of the VX4790A may be achieved when the following requirements are met:

- The VX4790A module is installed in an approved VXIbus mainframe according to the procedures in Section 2 of the Operating Manual (The module may be operated on an extender board to allow access to the adjustments)
- The VX4790A has passed its self test
- The VX4790A is operating in an ambient temperature between 0°C and +55°C and has been operating for a warm-up period of ten minutes

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Equipment Required

This procedure uses traceable signal sources and measurement instruments. Table J–1 lists the required equipment. You may use equipment other than the recommended examples if it meets the minimum requirements listed.

Table J–1: Required Adjustment Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. Digital Volt Meter (DVM) with test leads	5-1/2 digit, 0.1 mV at 1 V, 1 mV at 10V	FLUKE 8842A	Checking DC voltage accuracy
2. SMB to BNC Adapter Cable	50 Ω SMB male to BNC male	Tektronix VX1729 Data Cable	Interconnecting electrical signals
3. BNC Female to Dual Banana	50 Ω impedance; BNC female to Dual Banana	Tektronix part number 103-0090-00	Interconnecting electrical signals
4. 50 Ω BNC Feed Through Termination	50 Ω impedance; 0.1%, 1 W	Tektronix part number 011-0129-00	Loading ARB OUT signal
5. VXIbus Extender Board	Full length C size	Tektronix 73A–850	Providing adjustment access

System Requirements

In order to perform this procedure, the VX4790A must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table J–2.

Table J–2: Elements of a Minimum VX4790A Adjustment System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	One available slot, for the VX4790A in addition to the Slot 0 controller	Tektronix VX1400A	Power, cooling, and backplane for VXIbus modules
2. Slot 0 Controller	Resource Mgr., Slot 0 Functions, IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Slot 0 functions, Resource Mgr., GPIB-VXIbus interface
3. IBM PC or compatible with GPIB controller	286 Processor; GPIB Software and Talker/Listener/Controller card	IBM 486 PC, National Instruments GPIB PC2A card & NI-488.2M Software	System Controller
4. GPIB Cable	≈ 2 m length, GPIB connectors on each end	Tektronix part number 012–0991-00	Connecting PC-GPIB to Slot 0
5. VX4790A	Not applicable	Not applicable	Adjustment

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System Configuration

Table J–3 describes the VXIbus system configuration which is assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in place of those recommended in Table J–3.

Table J–3: VXIbus Adjustment System Configuration

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	0D (Hexadecimal)	13
VX4790A	VX4790	Slot 1	01	1

Adjustment Procedure

This procedure adjusts the DC reference and offset voltages of the DAC and the Gain of the ARB OUT amplifier. You may adjust the module on a VXIbus extender card, or in the mainframe if there are sufficient vacant slots to allow access to the adjustments. If you are not using an extender card, remove the right cover of the VX4790A module before installation to allow attachment of the DVM test leads. Refer to the module cover notations for adjustment location. Allow the module to warm up for at least 15 minutes.

***NOTE**. If you are using National Instruments NI-488.2 software you may wish to select the buffer 1 display mode to allow more comfortable viewing of the ASCII response (Just type buffer 1).*

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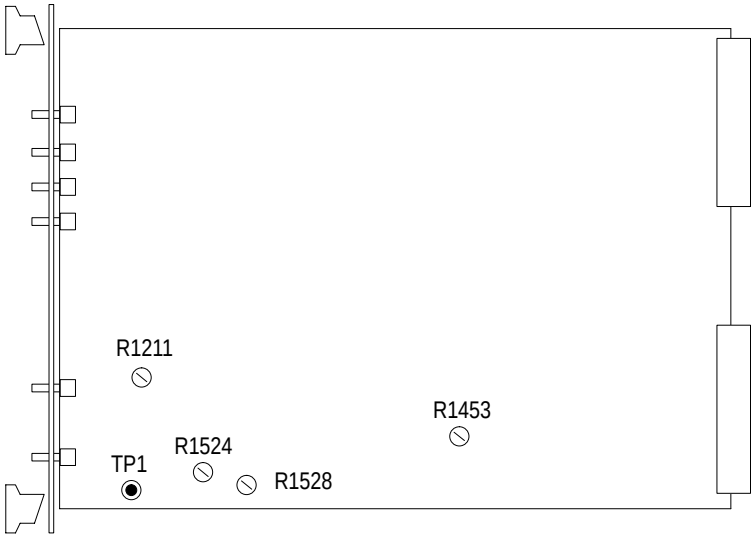


Figure 6: Adjustment Locations

1. Adjust the 3 V DAC reference voltage with the following steps:

   a. Attach the positive DVM lead to the VX4790A Test Point 1, located on the bottom edge of the circuit board, about 1.5 inches from the front panel (small plated through hole labeled TP1). Attach the negative test lead to the adjacent cover mounting post. Set the DVM to read DC volts.

   b. Using the following commands, reset the VX4790A to its power-on default state and for a 100% output amplitude (no attenuation):

   ```
   ibfind VX4790

   ibwrt "k;100%"
   ```

   c. Adjust the potentiometer labeled `MULT REF ADJ` (R1211), for a DVM reading of 3.000 ±0.002 VDC.

2. Adjust the DAC offsets (two) with the following steps:

   a. Attach the DVM to the VX4790A ARB OUT signal using an SMB to BNC cable and a BNC to Dual Banana adaptor.

   b. Using the following command, reset the VX4790A to its power-on default state, to the 10 V range, for a 0 V waveform, for 0% of programmed output to be generated, to close the output relay, and to trigger a continuous waveform starting at memory location 0:

   ```
   ibwrt "k;setvoltr 10;0n0v0w;0%;1o;0t"
   ```


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c. Adjust the potentiometer labeled OFFSET #2 (R1524), for a DVM reading of 0.000 ±0.002 VDC.

d. Using the following command, reset the VX4790A for the same parameters as step 1b, but for 100% of the programmed output to be generated:

```
ibwrt "k;setvoltr 10;0n0v0w;100%;1o;0t"
```

e. Adjust the potentiometer labeled OFFSET #1 (R1528), for a DVM reading of 0.000 ±0.002 VDC.

3. Repeat step 2.

4. Adjust the VX4790A ARB OUT signal gain with the following steps:

a. Attach the DVM to the VX4790A ARB OUT signal using the SMB to BNC cable, a 50 Ω feed-through terminator, and a BNC to Dual Banana adaptor.

b. Using the following command, reset the VX4790A to its power-on default state, to the 5 V range, for a 5 VDC waveform, for 100% of programmed output to be generated, to close the output relay, and to trigger a continuous waveform starting at memory location 0:

```
ibwrt "k;setvoltr 5;0n5v5w;100%;1o;0t"
```

c. Adjust the potentiometer labeled DAC REF ADJ (R1453), for a DVM reading of 5.000 ±0.002 VDC.

5. Reset the VX4790A to its power-on default state:

```
ibwrt "k"
```

This completes the VX4790A adjustment procedure.

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