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User Manual

Tektronix

VX4802
Programmable Digital I/O Module

070-9154-03

This document applies for firmware version 1.00
and above.

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EC Declaration of Conformity

We

Tektronix Holland N.V.
Marktweg 73A
8444 AB Heerenveen
The Netherlands

declare under sole responsibility that the

VX4802 and options 01 and 02
(Option 1D has not been qualified yet.)

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

To ensure compliance with EMC requirements this module must be installed in a mainframe which has backplane shields installed which comply with Rule B.7.45 of the VXIbus Specification. Only high quality shielded cables having a reliable, continuous outer shield (braid & foil) which has low impedance connections to shielded connector housings at both ends should be connected to this product.

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PROGRAMMING

The programming examples in the manual are written in Microsoft GW BASIC, using the following commands. For programming examples, see page 4 - 1.

CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)
Inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is in the variable ADDRESS%. LENGTH% = the number of bytes read from the instrument. STATUS% = '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. To use the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the VX4802.

CALL SEND (ADDRESS%, OUT$, STATUS%)
Outputs the contents of the string variable OUT$ to the IEEE-488 instrument whose decimal primary address is in the variable ADDRESS%. The variable STATUS% is a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.

END Terminates the program.

FOR/NEXT Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.

GOSUB n Runs the subroutine beginning with line n. The end of the subroutine is marked with a RETURN statement. When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.

GOTO n Program branches to line n.

IF/THEN Sets up a conditional IF/THEN statement. Used with other commands, so that IF the stated condition is met, THEN the command following is effective.

REM or ' All characters following the REM command or a ' are not executed.

RETURN Ends a subroutine and returns operation to the line after the last executed GOSUB command.

<CR> Carriage Return character, decimal 13.

<LF> Line Feed character, decimal 10.

VX4802 PROGRAMMABLE DIGITAL I/O CARD QUICK REFERENCE GUIDE

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 1 - 4)
Follow Installation guidelines. (p. 2 - 1)
The default condition of the VX4802 Module after the completion of power-up self test is as follows:

- All I/O pins tri-stated
- All bytes defined as inputs, active high
- All external handshake lines disabled
- Request True interrupts disabled

LEDs

When lit, the LEDs indicate the following:

Power power supplies functioning
Failed module failure
MSG module is processing a VMEbus cycle
RFI a VXI backplane interrupt is requested
RFD the external device strobes ready for data
DAV Data AVailable line is low
DRD the external device strobes data ready
DAK Data AcKnowledge line is low
ERR a programming error has occurred
I/O the current byte is programmed as an output
TRI the current byte is tri-stated
B7-B0 indicate the state of each bit of the currently displayed byte. Lit indicates the bit is high (TTL logic 1)
BYTE indicate which of the ten bytes the bit LEDs (B7-B0 LEDs) are currently displaying, as follows:

Byte Selected	LED status: Byte 3	Byte 2	Byte 1	Byte 0
0	unlit	unlit	unlit	unlit
1	unlit	unlit	unlit	lit
2	unlit	unlit	lit	unlit
3	unlit	unlit	lit	lit
4	unlit	lit	unlit	unlit
5	unlit	lit	unlit	lit
6	unlit	lit	lit	unlit
7	unlit	lit	lit	lit
8	lit	unlit	unlit	unlit
9	lit	unlit	unlit	lit

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SYSTEM COMMANDS

The following VXIbus Instrument Protocol commands are initiated by the VX4802's commander and will affect the VX4802:

CLEAR - The module clears its VXIbus interface and any pending commands. Current module operations are unaffected.

TRIGGER - The trigger command has no effect on the VX4802 card.

BEGIN NORMAL OPERATION - The module will begin operation if it has not already done so.

READ PROTOCOL - The module will return its protocol to its commander.

READ STATUS - The module will return its status to its commander.

COMMAND SYNTAX

Command protocol and syntax for the VX4802 Module is as follows:

1) Each command consists of a string of up to 255 characters. Every command must end with either a line-feed <LF> or a semi-colon (;) delimiter. A <CR> is treated as a white space character, and is ignored if received.

2) All commands are operated on in the order they are received, and executed when the delimiter is received.

3) If a given parameter is omitted within a command, either its default state or its last programmed state will be in effect (depending on the particular command issued).

4) Any character may be sent in either upper or lower case form.

5) Any of the following white space characters are allowed within the command string, and are ignored by the module:
00-09, 0B-20; 80-89, 8B-90

6) Any command syntax or programming errors will cause the command to be ignored, and an error will be flagged. All commands up to the occurrence of the error will remain valid. The invalid command and all subsequent commands will be lost, and no commands will be accepted until the error condition is cleared.

7) All responses from the module are terminated by a <CR><LF>.

MODULE COMMANDS

I specifies which bytes are to be read, the order in which they are to be read (and reported), and any masks to be overlaid onto the data prior to reporting it. Returns ASCII hex data representing all input bytes, selected input and/or output bytes, or selected bits of a byte (by using a mask). (3 - 5)

L specifies the data to be output, the order of output, and any masks to be overlaid onto the data prior to output. The ASCII hex data representing all output bytes, selected output bytes, single bits of a byte, or mask overlays onto the byte(s) can be used to update the card's output data latches. (3 - 8)

M command defines which bytes are inputs and which are outputs, and their active logic sense (active high true or active low true). (3 - 12)

N enables or disables the external tri-state line (ETS0) for bytes 0 - 4. (3 - 14)

P specifies the active edge of the handshake signals (positive or negative edge triggered). (3 - 15)

Q reads the current state of the module: (3 - 16)
error data; the state of the external handshake lines (DRD,RFD); the current tri-state condition of the I/O latches; the programmed I/O configuration; the programmed active edges of the handshake signals, and whether the handshake(s) are active; the programmed logic sense of each latch; the programmed external tri-state level of each latch.

R resets the board to its power-up state. (3 - 19)

S executes a self test, and then returns to its power-up state. (3 - 20)

T specifies whether output bytes are tri-stated (high-impedance), or active. This command is logically OR'ed with the external tri-state lines. (3 - 21)

U specifies the conditions for which the inputs and outputs are updated (update on command, or update on external handshake control). (3 - 23)

VER returns the current software revision level of the board. (3 - 25)

X enables or disables the VXI Request True interrupt. This interrupt can be programmed to be active when an error occurs, when either external handshake is valid (DRD,RFD), or when any combination of the three occurs. (3 - 26)

Z specifies the active level of the external tri-state control lines ETS0, ETS5 - ETS9 (active high true or active low true). (3 - 27)

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Immerse in Liquids

Clean the probe using only a damp cloth. Refer to cleaning instructions.

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Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:



DANGER
High Voltage



Protective Ground
(Earth) Terminal



ATTENTION
Refer to Manual



Double
Insulated

Certifications and Compliances

EMC Compliance

This product has demonstrated compliance to the Electromagnetic Compatibility (EMC) specifications when attached to the instrument identified in the product specifications. If this probe is attached to an instrument other than the one identified in the product specifications, the EMC performance may exceed the EMC specifications published with the instrument.

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Overvoltage Category

Overvoltage categories are defined as follows:

CAT III: Distribution level mains, fixed installation

CAT II: Local level mains, appliances, portable equipment

CAT I: Signal level, special equipment or parts of equipment, telecommunication, electronics

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Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

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VX4802
Programmable Digital I/O Module

Section 1
General Information and Specifications

Introduction

The VX4802 Programmable Digital I/O Module is a printed circuit board assembly for use in a mainframe conforming to the VXIbus Specification, such as the VX1400 "C" size mainframe used in the Tek/CDS IAC System. The VX4802 provides 80 TTL- or CMOS-compatible bidirectional digital I/O lines. The 80 programmable I/O signal lines are organized as ten 8-bit bytes.

Each of the ten bytes can be independently configured under full program control. All commands and responses are in ASCII hex notation for ease of programming, and to insure compatibility with the widest range of systems controllers. Program controlled parameters include:

- selection of any byte as either input or output,
- definition of masks for input and output data,
- control on command basis or on external handshake,
- logic sense of input, output, and handshake lines, and
- full reporting of operating parameters at any time.

The data output can be controlled as bits, as individual bytes, and as groups of bytes. Output is controlled on a command basis, or on a qualified basis using external handshakes.

Data input is also fully under program control. The module can report the state of all input bytes, groups of input and/or output bytes, and single bits of a byte. Input data can be updated on a command request basis, or on a qualified basis using external handshakes.

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User-defined masks can be overlaid on the data prior to output. Masks may also be applied to individual input bytes before they are returned to the system controller to improve data post-processing speed and ease of data interpretation.

The sense of inputs, outputs, and handshake lines can be set to either active high or active low under program control. The active edge can also be programmed for handshake lines. All I/O lines are both TTL- and CMOS-compatible, with up to 24 mA of sink current provided for each output.

External (handshake) control signals are provided for output and input data control. Output data control signals are Ready For Data (RFD), Data Available (DAV), and External Tri-State control (ETS0, ETS5 - ETS9). Input data control signals are Data Ready (DRD) and Data Acknowledge (DAK).

The VX4802 provides full access to system status information, which is especially helpful during system trouble-shooting, software de-bugging, and operational system checks. At any time, the system controller can read the state of the external handshake lines, the programmed I/O configuration, the programmed active edges of all handshake signals, which handshake signals are active, the programmed logic sense of each I/O byte, the tri-state condition of each output byte, and up-to-date error data.

Built-in-Test-Equipment (BITE) is provided by an internal loop-back path that allows the module to be tested with its outputs tri-stated, verifying I/O paths for each byte. A self test is automatically performed on power-up, and can also be commanded. Front panel LEDs indicate the status of power, assertion of the VMEbus signal SYSFAIL*, backplane cycles, data handshake signals, and individual I/O bits. In addition, the Query command can be used to determine the current state of the module during operation.

Note that certain terms used in this manual have very specific meanings in the context of a VXIbus System. These terms are defined in the VXIbus Glossary (Appendix C).

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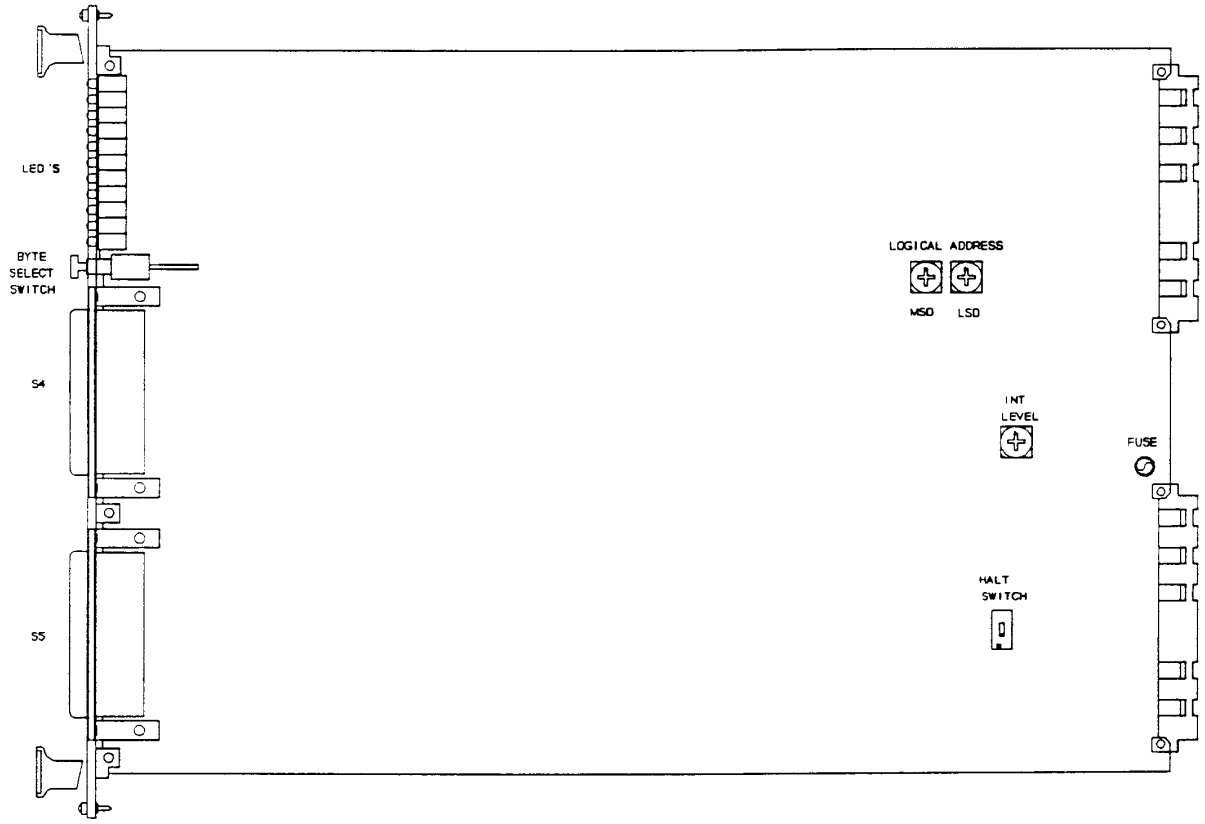


Figure 1: VX4802 Controls and Indicators

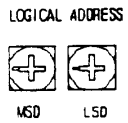
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Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4802 Module's operating environment. See Figures 1 and 2 for their physical locations.

Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4802 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

The actual physical address of the VX4802 module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4802 will be [(64d * XYh) + 49152d]. For example:

L. A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

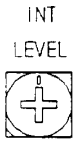
Using the VX4802 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the VX4802 is being used in a Tek/CDS IEEE-488 IAC system, consult the operating manual of the VX4520 Slot 0 Device/Resource Manager.

If the VX4802 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC). This algorithm is described in detail in the 73A-156 Operating Manual.

If the VX4802 is not being used in a Tek/CDS IAC System, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the logical address.

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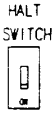


VMEbus Interrupt Level Select Switch

Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander (for example, the VX4520 Slot 0 Device/Resource Manager in a VX7401 IEEE-488 Interface System). The VMEbus interrupt level on which the VX4802 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4802's interrupt handler, typically the module's commander. Setting the switch to an invalid interrupt level (0, 8, or 9) will disable the module's interrupts. When using the VX4802 in a VX7401 System, set the interrupt level to the same level chosen on the VX4520.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.



Halt Switch

This two-position slide switch selects the response of the VX4802 Module when the Reset bit in the module's VXIbus Control register is set.

If the Halt switch is in the ON position, then the VX4802 Module is reset to its power-up state and all programmed module parameters are reset to their default values.

If the Halt switch is in the OFF position, the module will ignore the Reset bit and no action will take place.

Note that the module is not in strict compliance with the VXIbus Specification when the Halt switch is OFF.

Control of the Reset bit depends on the capabilities of the VX4802's commander. In a VX7401 System, for example, the Reset bit is set if the VX4520 Module receives a STOP command through the IEEE-488 bus.

Byte Select Switch

The Byte Select switch located on the front panel is a momentary action switch that controls which of the ten I/O bytes is currently being displayed on the LEDs. Each time the switch is depressed, the state of the next byte in sequence is displayed on the LEDs. For example, if the state of byte 0 is currently displayed, the state of byte 1 will be displayed after the switch is depressed. The Byte LEDs will display the number of the selected byte (see BYTE in the listing of LEDs below).

Fuses

The VX4802 Module has a single +5V fuse. The fuse protects the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

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If the +5V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If the +5V fuse blows, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section of this manual.

LEDs

The following LEDs are visible at the top of the VX4802 Module's front panel to indicate the status of the module's operation:

POWER LED
This green LED is normally lit and is extinguished if the +5V power supply fails, or if the +5V fuse blows.

FAIL LED
This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete a self test, loss of a power rail, or failure of the module's central processor.

NOTE:
If the module loses any of its power voltages, the Fail LED will be lit and SYSFAIL asserted. A module power failure is indicated when the module's Power LED is extinguished.*

MSG LED
This green LED is normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

RFI
Request for Interrupt. This LED lights when a VXI backplane interrupt is requested. Like the MSG LED, the pulse width is stretched to make it visible.

RFD
Indicates the state of the Ready for Data handshake signal. This LED lights when the external device strobes ready for data indicating it is ready for more data. It is cleared when new data is output by the module.

DAV
Indicates the level of the Data Available handshake signal. This LED lights when the DAV line is low. It clears when DAV goes high.

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DRD

Indicates the state of the Data Ready handshake signal. This LED lights when the external device strobes data ready indicating new input data is valid. It is cleared when the controller reads the input data.

DAK

Indicates the level of the Data Acknowledge handshake signal. This LED lights when the DAK line is low. It is cleared when the DAK line is high.

BYTE

Four LEDs that indicate which of the ten bytes (0 through 9) the bit LEDs (B7-B0 LEDs) are currently displaying, as follows:

LED status: Byte 3	Byte 2	Byte 1	Byte 0	Byte Selected
unlit	unlit	unlit	unlit	0
unlit	unlit	unlit	lit	1
unlit	unlit	lit	unlit	2
unlit	unlit	lit	lit	3
unlit	lit	unlit	unlit	4
unlit	lit	unlit	lit	5
unlit	lit	lit	unlit	6
unlit	lit	lit	lit	7
lit	unlit	unlit	unlit	8
lit	unlit	unlit	lit	9

ERR

Indicates a programming error has occurred. This LED will remain lit until the error condition is cleared.

I/O

Indicates the programmed input/output state of the current byte being displayed. The LED is lit if the byte is programmed as an output, and unlit if programmed as an input byte.

TRI

Indicates the tri-state condition of the byte currently being displayed. A lit LED indicates the byte is tri-stated.

B7 - B0

These LEDs indicate the state of each bit of the currently displayed byte. The LED being lit indicates the bit is high (TTL logic "1"). An unlit LED indicates the bit is low (TTL logic "0"). B7 is the most significant bit, and B0 the least significant bit.

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BITE (Built-in-Test-Equipment)

BITE is provided on the module by an internal loop-back path, which allows the module to be tested with the outputs tri-stated. The self test automatically tests and verifies all loop-back paths for each byte.

Self test is automatically performed on power-up, and can also be commanded. All the outputs are checked with their corresponding inputs, and with the output drivers in tri-state.

Front panel LEDs indicate the status of power, assertion of the VMEbus signal SYSFAIL*, backplane cycles, handshake signals, and other system operating parameters. In addition, the Query command can be used to determine the current state of the module during operation, including error codes (see the Query command in the Command Descriptions subsection).

Glossary

A glossary of VXIbus terms is provided in Appendix C. In addition, the following terms specific to the VX4802 Module are defined:

External Handshake Controls

Output Data

Ready For Data (RFD)
: Ready For Data is an input from an external device indicating it is ready for data. This signal is programmable to be either positive or negative edge triggered true.

Data Available (DAV)
: Data Available is an output to an external device indicating valid data is available on the outputs. This signal is programmable to be either positive or negative edge triggered true.

External Tri-State Control (ETS0, ETS5 - ETS9)
: Six external tri-state control lines are provided, one for bytes 0 through 4, and one each for bytes 5 through 9. These lines are inputs from an external device which cause the corresponding byte to go into tri-state (high impedance). For bytes 0 through 4, the external tri-state-line (ETS0) can be individually enabled or disabled for each byte, under program control (N command). The tri-state control lines are programmable to be either active high or active low.

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Input Data Control

Data Ready (DRD)

Data ready is an input from an external device indicating valid data is at the inputs. This signal is programmable to be either positive or negative edge triggered true.

Data Acknowledge (DAK)

Data acknowledge is an output to an external device indicating the input data has been accepted. This signal is programmable to be either positive or negative edge triggered true.

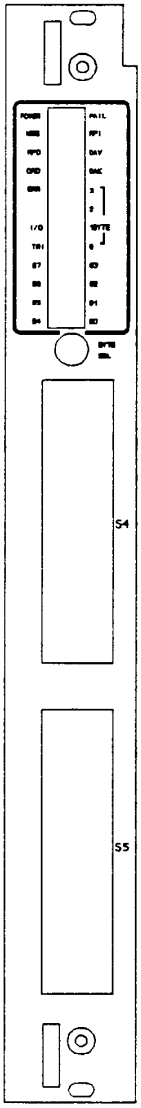


Figure 2: VX4802 Front Panel

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Specifications

Number of I/O Channels:	80.
Configuration:	I/O lines selectable as input or output on an 8-bit byte basis. Also tri-state programmable on an 8-bit byte basis.
Byte Transfer Polarity:	All input and output bytes individually selectable as active high or active low.
Input Data:	Returned as two hexadecimal ASCII characters per byte.
Input Control:	On program command, or with external Data Ready and Data Acknowledge handshake.
Output Data:	Programmed as two hexadecimal ASCII characters per byte, or by an H or L character on an individual bit basis.
Output Control:	On program command, or with external Ready for Data and Data Available handshake.
Tri-State Control:	On program command on an individual byte, or by external tri-state control signals.
Mask Capability:	On an individual byte basis, for input or output. AND, OR, and XOR masking provided.
Byte Ordering:	A predefined sequence for input or output byte transfer may be programmed. Bytes may be transferred in any required order.
Interrupt Modes:	Program selectable, on programming error, Ready For Data handshake, and/or Data Ready handshake.
External Control Logic Sense:	Data Available, Ready For Data, Data Acknowledge, and Data Ready control line polarities are all individually program selectable as low or high true.
I/O Signal Type:	TTL and CMOS compatible (74AHCT245 driver).
D.C. Electrical Characteristics:	-10° to +55° C., typical specs at 25° C. A minus sign indicates current flowing out of the card.

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	min	typ	max	units
Output high voltage (Voh)				
Io = -20 µA	4.4	5.0		V
Io = -6 mA	3.84	4.2		V
Output low voltage (Vol)				
Io = 20 µA		0	0.1	V
Io = 24 mA		0	0.5	V
Output low current (Iol)			24	mA
Input high voltage (Vih)	2.0			V
Input low voltage (Vil)			0.8	V
* Input current (Iin)			230	µA
Tri-state leakage current (Ioz)		0.5	5.0	µA

* There are 22K pull-up resistors to +5V on all I/O and handshake lines to account for floating inputs. The input IC uses 1.0 µA max, while the pull-down resistors require 5V / 22K = 227.6 µA.

External Control Lines:

External Tri-state Input to Tri-state Active:	ETS5 - ETS9	typ. 30 nS	max. 63 nS
	ETS0	typ. 70 nS	max. 115 nS
Valid Output Data to Data Available Strobe:	0 nS.		
Data Acknowledge to Data Ready Strobe Delay:	0 nS.		

VXIbus Compatibility: Fully compatible with the VXIbus Specification for message-based instruments with the Halt switch in the ON position.

VXI Device Type: VXI message based instrument, Revision 1.3.

VXI Protocol: Word Serial.

VXI Module Size: C size, one slot wide.

Module-Specific Commands: All module-specific commands and data are sent via the VXIbus Byte Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.

VMEbus Interface: Data transfer bus (DTB) slave - A16, D16 only.

Interrupt Level: Switch selectable, levels 1 (highest priority) through 7 (lowest).

Interrupt Acknowledge: D16, lower 8 bits returned are the logical address of the module.

VXIbus Data Rate: Write: 20 Kbytes/sec maximum.
Read: 400 Kbytes/sec maximum.

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VXIbus Commands Supported:

All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command event:

BYTE AVAILABLE (with or without END bit set)
BYTE REQUEST
BEGIN NORMAL OPERATION
READ PROTOCOL
READ STATUS
CLEAR
* GRANT DEVICE
* TRIGGER
* SET LOCK
* CLEAR LOCK
* IDENTIFY COMMANDER

* These commands are accepted, but have no effect on the module.

VXIbus Protocol Events Supported:

VXIbus events are returned via VME interrupts. The following event is supported and returned to the VX4802 Module's commander:

REQUEST TRUE (In IEEE-488 systems such as the 73A-IBX, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.

VXIbus Registers:

ID
Device Type
Status
Control
Protocol
Response
Data Low

See Appendix A for definition of register contents.

Device Type Register Contents:

F4DD (ones complement of binary value of model number with bit 11 set low).

Power Requirements:

All required dc power is provided by the Power Supply in the VXIbus mainframe.

Voltage:	+5 Volt supply:	4.75V dc to 5.25V dc.
Current (Peak Module, I_{PM}):	+5 Volt supply:	3.6 A (all outputs fully loaded).
Current (Quiescent):	2.1 A	
Current (Dynamic Module, I_{DM}):	+5 Volt supply:	1.6 A RMS (4.6 A PTP) - 80 outputs fully loaded.

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Power-up Defaults:	All I/O pins tri-stated. All bytes defined as inputs, active high. All external handshake lines disabled. Request True interrupts disabled.
Fuses:	Replacement fuse: Littlefuse P/N 273004
Cooling:	Provided by the fan in the VXIbus mainframe. Less than 10°C temperature rise with 1.2 liters/sec. of air at a pressure drop of 0.03 mm of H_2O.
Temperature:	0°C to +50°C, operating. -40°C to +85°C, storage.
Humidity:	Less than 95% R.H. non-condensing, -10°C to +30°C. Less than 75% R.H. non-condensing, +31°C to +40°C. Less than 45% R.H. non-condensing, +41°C to +55°C.
VXI Bus Radiated Emissions:	Complies with VXIbus Specification.
VXI Bus Conducted Emissions:	Complies with VXIbus Specification.
Module Envelope Dimensions:	VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in)
Dimensions, Shipping:	When ordered with a Tek/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, the module's shipping dimensions are: 406 mm x 305 mm x 102 mm. (16 in x 12 in x 4 in).
Weight:	1.3 kg. (2.96 lb).
Weight, Shipping:	When ordered with a Tek/CDS mainframe, this module will be installed and secured in one of the instrument module slots (slots 1-12). When ordered alone, the module's shipping weight is: 1.8 kg. (4 lb).
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)

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Front Panel Signal Connectors:	2 - 50 pin (DD 50S) connector, socket. Refer to Appendix B for connector pinouts.
Equipment Supplied:	1 - VX4802 Module.
Software Revision:	V1.5
Optional Equipment:	2 - 73A-657P 5 meter, 50 pin cable, unterminated. Option 01: 64 mA TTL outputs. Option 02: Open collector outputs. See Appendix D for a description of the options.

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Section 2
Preparation For Use

Installation Requirements And Cautions

The VX4802 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's logical address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the VX4802 Module's logical address.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

NOTE

Note that there are two printed ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector marked "VX4802" is at the top.

In order to maintain proper mainframe cooling, unused mainframe slots must be covered with the blank front panels supplied with the mainframe.

Based on the number of instrument modules ordered with the mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot and C size double-slot blank front panels can be ordered from your Tektronix supplier.

NOTE

Verify that the mainframe is able to provide adequate cooling and power with this module installed. Refer to the mainframe Operating Manual for instructions.

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If the VX4802 is used in a VX1X Series Mainframe, all VX4802 cooling requirements will be met.

NOTE

If the VX4802 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VX4802 Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.

If a Tek/CDS VX1400 or VX1401 mainframe is being used, the jumper points may be reached through the front of the mainframe. There are five (5) jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

Installation Procedure

NOTE

The VX4802 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the module's Revision Level, Serial Number (located on the label on the top shield of the VX4802), and switch settings on the Installation Checklist. Only qualified personnel should install the VX4802 Module.

2) Verify that the switches are switched to the correct values. The Halt switch should be in the ON position unless it is desired to not allow the resource manager to reset this module.

   Note that with either Halt switch position, a "hard" reset will occur at power-up and when SYSRST* is set true on the VXIbus backplane. If the module's commander is a VX4520 or VX4521 Slot 0 Device/Resource Manager, SYSRST* will be set true whenever the Reset switch on the front panel of the VX4520 or VX4521 is depressed. Also note that when the Halt switch is in the OFF position, the operation of this module is not VXIbus compatible.

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3) The module can now be inserted into any slot of the chassis other than slot 0.

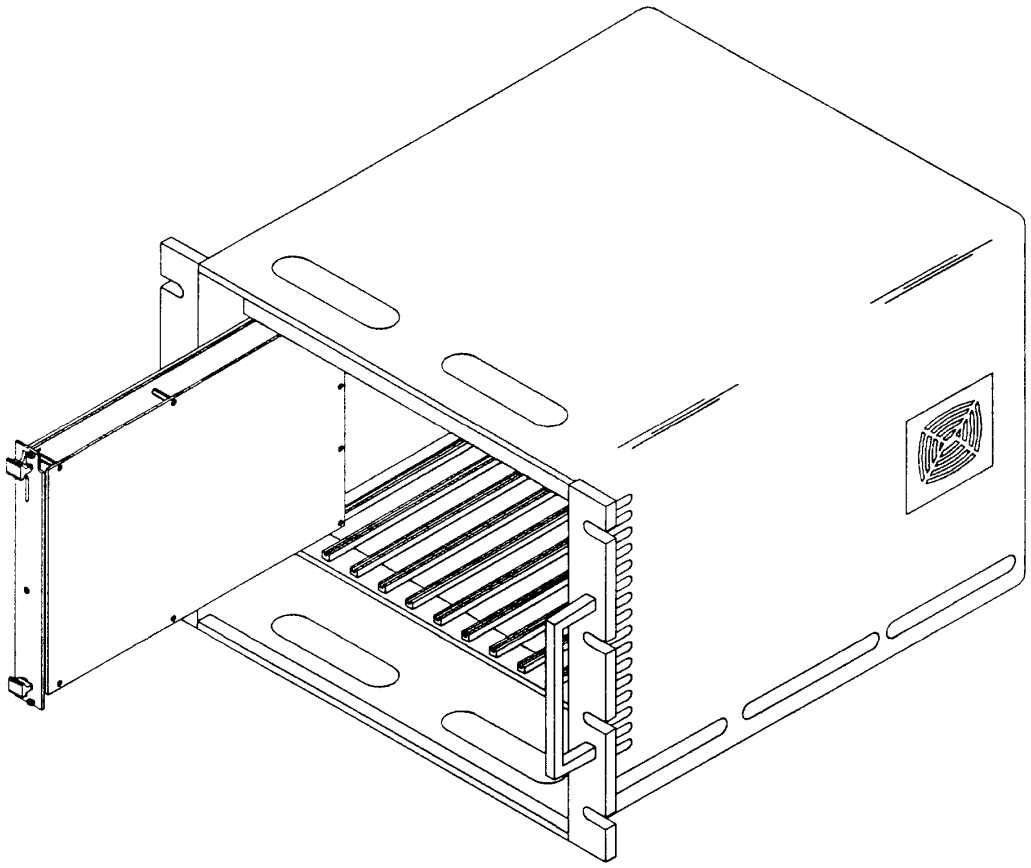


Figure 3: Module Installation

4) Install Cables:
If the module is being installed in a Tek/CDS VX1400 or VX1401 Mainframe, route the cables from the front panel of the module down through the cable tray at the bottom of the mainframe and out the rear of the mainframe. Connect the cable to the VX4802 Module's S4/S3 interface.

If a special cable is needed, 73A-657P Hooded Connectors may be used to cable between the module's output connectors and the Unit Under Test (UUT).

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Installation Checklist

Installation parameters may vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the VX4802 Module.

Revision Level: _____

Serial No.: _____

Mainframe Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Halt Switch: _____

Cabling Installed:

S4 Cable: _____

S5 Cable: _____

Performed by: _____ Date: _____

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Section 3
Operation

Overview

The VX4802 Module is programmed by ASCII characters issued from the system controller to the VX4802 Module via the module's VXIbus commander and the VXIbus mainframe backplane. The module is a VXIbus Message Based instrument and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the VX4802 Module's commander for details on the operation of that device.

If the module is being used in a Tek/CDS IEEE-488 IAC System, the module's commander will be the VX4520 or VX4521 Slot 0 Device/Resource Manager. Refer to the VX4520 or VX4521 Operating Manual and the Programming Examples in this manual for information on how the system controller communicates with the module.

Power-up

The VX4802 Module will complete its self test and be ready for programming five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay to this time. The Power LED will be on, and the Fail LED off. The MSG LED will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the mainframe. The default condition of the module after power-up is described in the SYSFAIL, Self Test and Initialization subsection.

System Commands

Although these non-data commands are initiated by the VX4802's commander (for example, the VX4520 or VX4521 Module) rather than the system controller, they have an effect on the VX4802 Module. The following VXIbus Instrument Protocol commands will affect the VX4802:

Command	Effect
Clear	The module clears its VXIbus interface and any pending commands. Current module operations are unaffected.
Trigger	The Trigger command has no effect on the VX4802 Module.
Begin Normal Operation	The module will begin operation if it has not already done so.

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Read Protocol	The module will return its protocol to its commander.
Read Status	The module will return its status to its commander.

Module Commands

A summary of the VX4802's Module's commands is listed below. This is followed by detailed descriptions of each of the commands. A sample BASIC program using these commands is shown in the Programming Examples section.

Command Syntax

Command protocol and syntax for the VX4802 Module is as follows:

1) Each command consists of a string of up to 255 characters. Every command must end with either a line feed <LF> or a semi-colon (;) delimiter. A <CR> is treated as a white space character, and is ignored if received.

2) All commands are operated on in the order they are received, and executed when the delimiter is received.

3) If a given parameter is omitted within a command, either its default state or its last programmed state will be in effect (depending on the particular command issued).

4) Any character may be sent in either upper or lower case form.

5) Any of the following white space characters, whose 8-bit hexadecimal values are given below, are allowed within the command string, and are ignored by the module:

   00-09, 0B-20
   80-89, 8B-90

6) Any command syntax or programming errors will cause the command to be ignored, and an error will be flagged. All commands up to the occurrence of the error will remain valid. The invalid command and all subsequent commands will be lost, and no commands will be accepted until the error condition is cleared, either through a hardware or software reset, or by reading the error out with the Q command.

7) All responses from the module are terminated by a carriage return and line-feed <CR><LF>.

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Command Summary

Detailed descriptions of each command (in alphabetical order) are given following the summary. An overview of the commands is as follows:

I The Input Data command specifies which bytes are to be read, the order in which they are to be read (and reported), and any masks to be overlaid onto the data prior to reporting it. ASCII hex data representing all input bytes, selected input and/or output bytes, or selected bits of a byte (by using a mask) can be returned to the system controller using this command.

L The Load Output command specifies the data to be output, the order of output, and any masks to be overlaid onto the data prior to output. The ASCII hex data representing all output bytes, selected output bytes, single bits of a byte, or mask overlays onto the byte(s) can be used to update the card's output data latches.

M The Mode command defines which bytes are inputs and which are outputs, and their active logic sense (active high true or active low true).

N The Enable command enables or disables the external tri-state line (ETS0) for bytes 0 through 4.

P The Strobe Pulse Sense command specifies the active edge of the handshake signals (positive or negative edge triggered).

Q The Query Status command reads the current state of the module. The information which can be obtained includes:

- error data;
- the state of the external handshake lines (DRD, RFD);
- the current tri-state condition of the I/O latches;
- the programmed I/O configuration;
- the programmed active edges of the handshake signals, and whether the handshake(s) are active;
- the programmed logic sense of each latch; and
- the programmed external tri-state level of each latch.

R The Reset command resets the board to its power-up state.

S The Self Test command causes the module to execute a self test, and then return to its power-up state.

T The Tri-state Control command specifies whether the output bytes are tri-stated (high-impedance), or active. This command is logically OR'ed with the external tri-state lines.

U The Update command specifies the conditions for which the inputs and outputs are updated (update on command, or update on external handshake control).

VER The Version command returns the current software revision level of the board.

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X The X command enables or disables the VXI Request True interrupt. This interrupt can be programmed to be active when an error occurs, when either external handshake is valid (DRD, RFD), or when any combination of the three occurs.

Z The Tri-state Level command specifies the active level of the external tri-state control lines ETS0, ETS5 - ETS9 (active high true or active low true).

A detailed description of each command, in the same order as listed above, is given on the following pages. The syntax used in the command descriptions is:

( ) optional parameter
{ } group of parameters
' ' ASCII character
... optional repetition

Note that the (), {}, ' ', and ... characters are not part of the command.

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Command Descriptions

Command: I (Input command)
IO (Input Override command)

Syntax: I{b(o)(d)(/) }...
IO{b(o)(d)(/) }...

Purpose: The Input command specifies the data to be input, the order in which it is be input, and any masks which are to be overlaid onto the data prior to reporting it. The Input Override command provides the capability to read a different input sequence one time, without destroying the last defined I command input sequence.

Description:

I input command
IO input override
b one to ten digits which specify the byte number, '0' through '9', or '*' for all bytes.
o one of the following:
  & AND the data specified by (d) to the specified input byte(s).
  # OR the data specified by (d) to the specified input byte(s).
  X XOR the data specified by (d) to the specified input byte(s).
d ASCII mask value '00' through 'FF' (required with 'o')
/ an optional character, allowed to make the command more readable.

Default: I* (input all bytes)

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically redefined by another I command, or by a Reset or Self Test command. Input can be requested for both input and output bytes.

Typical use of the I command simply defines a sequence of bytes to be read, with the sequence defined by the order of the digits following the I command. For example, "I123" specifies that the data from bytes 1, 2, and 3 are to be reported in the order of byte 1 first, byte 2 second, and byte 3 third (followed by <CR><LF>).

Additional input of the same sequence does not require redefining the I command. Successive reads from the module will return new data in the defined sequence, each terminated by <CR><LF>.

For example, "I321" specifies an input sequence of 3-2-1. If bytes 1, 2, and 3 contained 11, 22, and 33 hex, the module would report '332211<CR><LF>' when read. Subsequent reads of the module will report the updated state of bytes 3, 2, and 1.

A '*' in the I command automatically defines the byte sequence to be 0-1-2-3-4-5-6-7-8-9.

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Each time an I command is issued, it defines a new input sequence. The input override command (IO) is used to look at a specific byte(s) without affecting the I command's sequence, as shown in the example below. Once the I command has been issued, its setup and sequence (including masks) remain valid until overridden by another I command, a QR or QD command, or reset or self test.

If external Data Ready Strobe has been defined as the condition to latch input data into the card, and no strobe has been received since the last input request, an 'N<CR><LF>' will be returned for both the I and IO commands, indicating no new data is available.

The state of the data returned represents the logic sense programmed with the mode (M) command.

NOTE: All responses from the I and IO commands are terminated in <CR><LF>.

Errors: If an I command is issued with no arguments ((b) is omitted), the sequence will be cleared and the module will respond with a <CR><LF> only. If (o) and (d) are omitted, the command specifies data in its new input form. If (o) is specified without (d), an Invalid Input Command error will be generated. If any error is queued, the module will respond with a QE<CR><LF> on the subsequent input requests.

Example: The example cases on the following page show how a sequence of I commands and implicit inputs will be reported (each case assumes the I/O lines are at 00, 11, 22, 33, 44, 55, 66, 77, 88, and 99 for bytes 0 to 9 respectively):

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Case	Command	Byte Sequence	Module Response
1	Power-up State	0-1-2-3-4-5-6-7-8-9	
00112233445566778899<CR><LF>			
2	I123<LF>	1-2-3	112233<CR><LF>
3	read (no I command)	1-2-3	112233<CR><LF>
4	I*&55<CR><LF>	0-1-2-3-4-5-6-7-8-9	
00110011445544550011<CR><LF>			
5	read (no I command)	0-1-2-3-4-5-6-7-8-9	
00110011445544550011<CR><LF>			
6	I*;	0-1-2-3-4-5-6-7-8-9	
00112233445566778899<CR><LF>			
7	IO3X11;	3	22<CR><LF>
8	read (no I command)	0-1-2-3-4-5-6-7-8-9	
00112233445566778899<CR><LF>			
9	I5430126789;	5-4-3-0-1-2-6-7-8-9	
55443300112266778899<CR><LF>			
10	I0#55/1XAA/2345;	0-1-2-3-4-5	55BB22334455<CR><LF>

Case 1 is the initial default condition.
Case 2 requests the input from bytes 1, 2, and 3 in that order.
Case 3 reports the data from the input sequence set up in case 2.
Case 4 masks (ANDs) each input byte with a 55 hex prior to reporting it.
Case 5 reports the data using the sequence and mask set up in case 4.
Case 6 overrides the mask from case 4 and reports the data in its raw form.
Case 7 uses the override command to look at byte 3 XOR'd with an 11 hex.
Case 8 reports the data from the sequence defined in case 6.
Case 9 reports the data in the newly defined sequence 5430126789.
Case 10 reports the data in the newly defined sequence 012345, ORs byte 0 with a 55 hex, XORs byte 1 with an AA hex, and reports bytes 2, 3, 4, and 5 in their raw form. The "/" is used to make the command more readable.

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Command: L (Load Output)
LO (Load Output Override)

Syntax: L{b(o)(d)(/) }...
LO{b(o)(d)(/) }...

Purpose: The Load Output command specifies the data bytes to be output, the sequence in which it is be output, and any masks which are to be overlaid onto the data prior to output by the module. The Load Override command provides the capability to output a different sequence of bytes one time, without destroying the last defined L command output sequence.

Description:

L load output command

LO load override

b one to ten digits which specify the byte number, 0 through 9, or * for all bytes.

o one or more of the following letters which specify various parameters:

- D Load the data specified by (d) to the specified output byte(s).
- S Set the bit indicated by (d) to a logic high (the eight bits of a byte are defined as '00' through '07', with bit '00' being the least significant bit).
- R Reset the bit indicated by (d) to a logic low (the eight bits of a byte are defined as '00' through '07', with bit '00' being the least significant bit).
- & AND the data specified by (d) to the specified output byte(s).
- # OR the data specified by (d) to the specified output byte(s).
- X XOR the data specified by (d) to the specified output byte(s).

d ASCII value '00' through 'FF' (required with (o)). Note that (d) is an 8-bit wide byte value if the (o) parameter is a D, $, or X, and a bit number if the (o) parameter is an S or R.

/ optional character which is allowed to make the command more readable.

Default: NONE [all bytes are initially defined as inputs (M command), set to TTL logic 0, and tri-stated (T command)].

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another L command, by redefining the I/O configuration (M command), or by a Reset or Self Test command. If any bytes are not programmed, they will remain in their default (or previously programmed) state. The Set, Reset, and Mask parameters (S, R, X, #, and &) all operate on the last data output to a byte(s), and are valid only for the current command.

An (*) automatically defines the sequence 0-1-2-3-4-5-6-7-8-9.

Typical use of the L command specifies an output byte and the data to be output. For example, "L2D55" specifies that a '55' hex is to be output to byte 2.

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Once an output sequence has been defined with the L command, ASCII hex data (00 - FF) may be written to the module without additional L commands. The order in which the outputs were specified in the last Load command defines an output sequence. For example, "L321D55" specifies that a '55' is to be output to bytes 3, 2, and 1. This command also defines the output sequence to be bytes 3-2-1. ASCII hex data sent to the module will then be buffered until the amount of data received matches the amount required by the output sequence. All bytes are thus physically updated at the same time when the total amount of data is received. In this example, six ASCII hex bytes are required since two bytes are required for each output byte. If "123456" were then sent to the card, byte 3 would be loaded with "12", byte 2 with "34", and byte 1 with "56", to match the 3-2-1 sequence. If an L command had not been previously issued, this data would be ignored.

Each time an L command is issued, it defines a new output sequence. The Load Override (LO) command is used to change specific data without affecting the L command's sequence, as shown in the examples below. Note that whenever a new L command is issued, any buffered data in an incompleted buffer is lost. The output sequence is also cleared whenever a new Mode (M) command is issued.

Note that a particular byte should only be defined once within the L command, because it can appear only once in the sequence. If a byte is defined more than once within the command, only the last specified action is taken. For example, "L0D55/0D44" would load a 44 hex into byte 0, and the load 55 hex action is ignored. Similarly, "L0S01/0S03" would only set bit 3 of byte 0. Setting both bits can be accomplished by using the mask command "L0#05".

The byte(s) will be physically output based on the conditions defined by the U command.

Note that when using the RFD external handshake, the most recent data received by the module is always the next to be output. If two L commands, or two full buffers of data are received before a strobe occurs, the first data will be lost, and the most recent data will be output. To prevent this overwriting of data, read the state of Ready For Data (RFD) with the QR command (see Query Status command) before sending additional data to the module. If the data reported back by the QR command is a '0', then the last data output has not yet been accepted by the external device. If a '1' is reported back, then the outputs can be updated with no loss of data.

Errors: If output is commanded to a byte which is defined as an input (M command), an error will be flagged, and the command ignored. If the (b) parameter is omitted, the command will have no effect. The (o) and (d) parameters are optional. However, if (o) is specified without (d), an Invalid Hex Value error will be generated. If an invalid parameter is specified, an Invalid Load Command error will be generated.

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Example: **The following examples show how a sequence of L commands and data will be output.**

Case	Command	Byte Sequence	Output Data Bytes (hex) 0 1 2 3 4 5 6 7 8 9
1	Power on (default)	none	-- -- -- -- -- -- -- -- -- --
2	M*O;T*I;I*;	N/A	00 00 00 00 00 00 00 00 00 00
3	L*D55<CR><LF>	0-1-2-3-4-5-6-7-8-9	55 55 55 55 55 55 55 55 55 55
4	00112233445566778899	0-1-2-3-4-5-6-7-8-9	00 11 22 33 44 55 66 77 88 99
5	L1D0150DFA2D204D883DCC<LF> or L1D01/50DFA/2D20/4D88/3DCC<LF>	1-5-0-2-4-3	FA 01 20 CC 88 FA 66 77 88 99
6	001122334455	1-5-0-2-4-3	22 00 33 55 44 11 66 77 88 99
7	LO1S04;	no change	22 10 33 55 44 11 66 77 88 99
8	L123#80<CR><LF>	1-2-3	22 90 B3 D5 44 11 66 77 88 99
9	001122	1-2-3	22 00 11 22 44 11 66 77 88 99
10	L1502439876;	1-5-0-2-4-3-9-8-7-6	22 00 11 22 44 11 66 77 88 99
11	00112233445566778899	1-5-0-2-4-3-9-8-7-6	22 00 33 55 44 11 99 88 77 66
12	L*D33;	0-1-2-3-4-5-6-7-8-9	33 33 33 33 33 33 33 33 33 33
13	L0S02/1R04/2&22/3X22/4#44<CR><LF>	0-1-2-3-4	37 23 22 11 77 33 33 33 33 33
14	0011		37 23 22 11 77 33 33 33 33 33
15	223344		00 11 22 33 44 33 33 33 33 33
16	LO41D55;		00 55 22 33 55 33 33 33 33 33
17	AABBCCDDEE		AA BB CC DD EE 33 33 33 33 33

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Case 1 is the initial state of the outputs. All outputs are in a tri-state condition.
Case 2 defines all bytes as outputs and un-tri-states them. The I* command at the end of the line can be used to read back the output data and verify that it is all 0s, if an input request is issued following this command.
Case 3 loads all outputs with 55 hex, with the '*' defining the sequence as 0123456789.
Case 4 is data received from the system controller. The data is output in the order it is received according to the current sequence.
Case 5 loads each byte individually, and redefines the sequence to be 150243. The line below case 5 shows the same command using the optional '/' character.
Case 6 is more data, again output in the order it is received, according to the current sequence.
Case 7 uses the load override command to force bit 4 of byte 1 high without changing the sequence.
Case 8 OR's the current data of bytes 1, 2, and 3 with an 80 hex, and redefines the output sequence to 123.
Case 9 loads new data into bytes 1, 2, and 3.
Case 10 redefines the output sequence without affecting the data.
Case 11 loads data for the newly defined sequence.
Case 12 loads all bytes with 33 hex.
Case 13 sets bit 2 of byte 0, resets bit 4 of byte 1, AND's byte 2 with hex 22, XOR's byte 3 with hex 22, and OR's byte 4 with a hex 44.
Case 14 has no effect on the outputs because not enough data has been received based on the last sequence defined (01234).
Case 15 supplies the rest of the data needed for the sequence, and the new data is output.
Case 16 uses the override command to force bytes 4 and 1 to a hex 55.
Case 17 outputs new data based on the sequence from case 12, which is still in effect.

Note that each time a Load command is received, a new sequence is defined for any subsequent data, and that the Load Override command does not affect the output sequence.

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Command: **M (Mode)**

Purpose: The Mode command defines which bytes are inputs and which are outputs, and their active sense.

Syntax: M {(b)(m)(l)}...

Description:

b	byte number, 0 through 9, or * for all bytes.
m	I or O, Input or Output respectively
l	H or L, Logic state, High or Low true respectively.

Default: M*IH (all inputs, active high true)

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another M command, or by a Reset or Self Test command. If any bytes are not programmed, they will remain in their default (or previously programmed) state.

If the logic state is programmed as active high true, then a "1" on an input or output command reflects a TTL logic "1" on the I/O pin. If the logic state is programmed as active low true, then a "1" on an input or output command reflects a TTL logic "0" on the I/O pin.

NOTE: The Mode command automatically resets the sequence set up by the L (Load) command to 'null', and clears any pending RFD handshakes.

Errors: If (m) or (l) is omitted, the default (or previously programmed state) will be used for the omitted parameter of the byte(s) being programmed. If (b) is omitted, the command will have no effect. If both (m) and (l) are omitted or an invalid parameter is sent, an Invalid Mode Command error will be generated.

Example: The following examples show how a sequence of mode commands will affect the configuration setup of the card:

Case	Command	Byte I/O and Sense (H or L)									
		0	1	2	3	4	5	6	7	8	9
1	Power-up (default)	I/H	I/H	I/H	I/H	I/H	I/H	I/H	I/H	I/H	I/H
2	M3O;	I/H	I/H	I/H	O/H	I/H	I/H	I/H	I/H	I/H	I/H
3	M105L<CR><LF>	I/L	I/L	I/H	O/H	I/H	I/L	I/H	I/H	I/H	I/H
4	M012OH345IL6789OH<LF>	O/H	O/H	O/H	I/L	I/L	I/L	O/H	O/H	O/H	O/H
5	M*OL<CR><LF>	O/L	O/L	O/L	O/L	O/L	O/L	O/L	O/L	O/L	O/L
6	M23I*H; or M23I/*H;	O/H	O/H	I/H	I/H	O/H	O/H	O/H	O/H	O/H	O/H

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Case 1 is the power-up default state.

Case 2 sets up byte 3 as an output. Since the logic sense was not specified, it remains in its previously programmed (default) state. A ';' is used to delimit this command.

Case 3 sets up bytes 1, 0, and 5 as active low. All other bytes remain in their previously programmed state. A <LF> is used to delimit this command with the <CR> being ignored.

Case 4 sets up bytes 0, 1, and 2 as outputs, active high; bytes 3, 4, and 5 as inputs, active low; and bytes 6, 7, 8, and 9 as outputs, active high. A <LF> is used to delimit this command.

Case 5 sets all bytes to outputs, active low. For this command, the <LF> is again the delimiter, while the <CR>is ignored.

Case 6 sets up bytes 2 and 3 as inputs, and all bytes as active high. The variation of the command with the / delimiter illustrates that the (l) portion of the argument is omitted in the first part of the command, and the (m) portion of the argument is omitted in the second part of the command.

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Command: N [External Tri-State Enable (bytes 0 through 4)]

Purpose: The Enable command enables or disables whether the external tri-state line ETS0 will tri-state bytes 0 through 4.

Syntax: N {(b)(l)}...

Description:
b byte number, 0 through 4, or * for all five bytes.
l D or E, indicating:
D = disable
E = enable

Default: N*D (ETS0 disabled for all five bytes)

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another 'N' command, or by a Reset or Self Test command. Any bytes which are not programmed will remain in their default (or previously programmed) state.

NOTE: The N, T, and Z commands may all be used to control the tri-state condition of bytes 0 through 4. The N command defines which bytes will be affected by the external tri-state line ETS0. The Z command defines the active polarity of the external tri-state lines, and the T command can be used to tri-state a byte independently of the state of the external tri-state line.

Errors: If (b) is omitted, the command will have no effect. If (l) is omitted, or an invalid parameter is specified, an Invalid External Tri-state Command error will be generated.

Example: The following example shows how a sequence of N commands will control the external tri-state enable (ETS0) for bytes 0 through 4.

Case	Command	Individual Byte Enable/Disable ETS0				
		0	1	2	3	4
1	Power up (Default)	D	D	D	D	D
2	N*E<LF>	E	E	E	E	E
3	N123D;	E	D	D	D	E
4	N04D12E<CR><LF>	D	E	E	D	D

Case 1 is the power-up (default) condition, which disables ETS0 from tri-stating any of its bytes.
Case 2 enables ETS0 to tri-state the bytes.
Case 3 disables ETS0 for bytes 1, 2, 3. Bytes 0 and 4 remain in their previously programmed state.
Case 4 disables ETS0 for bytes 0 and 4, and enables ETS0 for bytes 1 and 2.

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Command: P (Strobe Pulse Senses)

Syntax: P {(p)...(e)}

Purpose: The Strobe Pulse Sense command specifies the active edge of the handshake signals.

Description:

p one of the following single letters which specifies the strobe pulse:

- A Data Available Strobe
- R Ready for Data Strobe
- D Data Ready Strobe
- K Data Acknowledge Strobe
- * All strobes

e specifies the active edge of the specified strobe as follows:

- \+ positive edge triggered strobe pulse
- \- negative edge triggered strobe pulse

Default: P* + (all pulse senses positive edge triggered)

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another P command, or by a Reset or Self Test command.

This command assumes the U (Update) command has specified the use of the handshake signals. If not, this command will have no effect until a U command is issued.

Errors: If an edge is not programmed, it will remain in its default (or previously programmed) state. If (e) or (p) is omitted, the command will have no effect. If an invalid parameter is specified, an Invalid Pulse Command error will be generated.

Example: The following examples show how a sequence of pulse commands will control the pulse trigger active edges:

		Pulse Edges			
Case	Command	A	R	D	K
1	Power-up (default)	+	+	+	+
2	PAK-<CR><LF>	-	+	+	-
3	P*-<LF>	-	-	-	-
4	PKD+;	-	-	+	+
5	PAR+DK-<CR><LF>	+	+	-	-

Case 1 is the power-up (default) condition, which sets all handshake lines as positive edge triggered.

Case 2 sets the DAV and DAK pulses as negative edge true, leaving RFD and DRD in their previously programmed (default) state.

Case 3 sets all handshake lines negative edge triggered.

Case 4 sets the DAK and DRD strobes as positive edge triggered.

Case 5 sets the DAV and RFD strobes as positive edge triggered, and the DRD and DAK strobes as negative edge triggered.

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Command: Q (Query Status)

Syntax: Q(s)

Purpose: The Query Status command returns the status of various hardware and software states.

Description: s one of the following letters, which specifies what is to be returned:

A returns an ASCII error message (see also the (N) parameter).

D returns the state of the external Data Ready Strobe. 0 indicates the handshake has not occurred, and 1 indicates it has.

I returns the programmed state of the VXIbus Request True interrupts, and which conditions were active at the time the VX4802's commander last acknowledged an interrupt from the module. The response is formatted as a two character hexadecimal string. Bit 0 represents a programming error, bit 2 is RFD, and Bit 3 is DRD. A 1 in any of these bit positions indicates the interrupt is enabled, while a 1 in bit positions 4, 6, and 7 indicate respectively which conditions were active when the interrupt was acknowledged. Bit 7 is the most significant bit of the first hexadecimal character.

L returns the programmed state of the external tri-state inputs. The response is formatted as a three character hexadecimal string ('000' through '3FF'). A 1 in a bit position represents tri-state level active high, and a 0 active low. Bit 0 ('001') represents byte 0, and bit 9 ('200') represents byte 9.

M returns the module's programmed mode. The response is formatted as a three character hexadecimal string (000-3FF). A 1 in a bit position represents an output and a 0 an input. Bit 0 ('001') represents byte 0, and bit 9 ('200') represents byte 9.

N returns an ASCII '00' - '99' numeric error code. The codes and their messages are listed below.

P returns the program selected edge of the external handshake signals, and whether or not a handshake signal is active. The response is formatted as a two character hexadecimal string ('00' - '3F'). Bit 0 represents DRD, bit 1 RFD, bit 2 DAV, and bit 3 DAK. A 1 in the bit position represents negative edge triggered and a 0 represents positive edge triggered. Bits 4 and 5 indicate whether the input (DRD) and output (RFD) handshakes respectively are enabled (1 = enabled; 0 = disabled).

R returns the state of the external Ready for Data Strobe. 0 indicates the handshake has not occurred, and 1 indicates it has.

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S returns the programmed logic sense for each byte. The response is formatted as a three character hexadecimal string ('000' through '3FF'). A 1 represents logical low true, and a 0 represents logical high true. Bit 0 ('001') represents byte 0, and bit 9 ('200') represents byte 9.

T returns the actual current tri-state condition of each output byte (the OR of each byte's external tri-state control line and its tri-state condition as programmed by the N and T commands). The response is formatted as a three character hexadecimal string ('000' - '3FF'). Bits 0 through 8 represent bytes 0 through 8. Bit 0 ('001') represents byte 0, and bit 9 ('200') represents byte 9. A 1 in a bit position indicates the corresponding byte is tri-stated.

For the QR and QD commands, once the Q command has been issued, subsequent input requests will continuously return the respective information until overridden by another Q command, by an I command, or by reset or self test.

Errors:

If an error is queued while the I command or any Q command other than QA or QN is the active input request mode, the module will respond with a QE<CR><LF> until either a QA or QN command is issued to acknowledge the error condition. If (s) is not one of the specified characters, the module will respond with 'READY'.

Examples:

The following examples show how each of the above commands will respond on power-up:

Command	Response
read (no command)	READY<CR><LF>
QA;	NO ERRORS<CR><LF>
QD;	1<CR><LF>
QI;	00<CR><LF>
QL;	000<CR><LF>
QM;	000<CR><LF>
QN;	00<CR><LF>
QP;	00<CR><LF>
QR;	1<CR><LF>
QS;	000<CR><LF>
QT;	3FF<CR><LF>

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Error Responses:

Number	Error Message
00	NO ERRORS
01	SELF TEST FAILURE BYTE X COUNT Y where X is an ASCII 0 through 9, indicating the byte failing self test, and Y is an ASCII 000 to 255, indicating the decimal value of the bit pattern causing the failure.
02	SYNTAX ERROR
03	INPUT BUFFER OVERFLOW
04	INVALID MODE COMMAND 'X' where X is the invalid character.
05	INVALID PULSE COMMAND 'X' where X is the invalid character.
06	INVALID TRI-STATE LEVEL COMMAND 'X' where X is the invalid character.
07	INVALID TRI-STATE COMMAND 'X' where X is the invalid character.
08	INVALID UPDATE COMMAND 'X' where X is the invalid character.
09	INVALID INPUT COMMAND 'X' where X is the invalid character.
10	OUTPUT SPECIFIED ON AN INPUT BYTE - X where X is the invalid byte specified.
11	INVALID LOAD COMMAND 'X' where X is the invalid character.
12	INVALID (OR MISSING) HEX VALUE 'X' where X is the invalid hex character.
13	INVALID BIT SPECIFIED 'X' where X is the invalid bit number.
14	INVALID INTERRUPT COMMAND 'X' where X is the invalid character.
15	MAXIMUM SEQUENCE LENGTH EXCEEDED - XX where XX is the length of the sequence (up to ten sequence numbers are valid).
16	INVALID EXTERNAL TRI-STATE COMMAND 'X' where X is the invalid character.
99	UNKNOWN ERROR

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Command: R (Reset)

Syntax: R

Description: The Reset command resets the board to its power-up state:

All I/O pins tri-stated.
All bytes defined as inputs, active high.
All external handshake lines disabled.
Request True interrupts disabled.

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Command: S (Execute Self Test)

Syntax: S

Purpose: The Self Test command causes the module to execute a self test, and then return to its power-up state.

Description: The self test consists of internal circuitry tests, and I/O wraparound tests. The results of a self test can be read using the Query Status commands QA or QN. If the self test fails, error '01' will be generated, and the module's Fail LED will be lit.

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Command: T (Tri-state Control)

Syntax: T {(b)...(a)}...

Purpose: The Tri-state Control command specifies under software control whether individual output bytes are tri-stated (high-impedance), or not tri-stated. This command is logically OR'ed with the external tri-state control lines ETS0, ETS5 - ETS9, so if either is active, the byte(s) will be tri-stated. The tri-state command does not cause bytes to become output bytes, or imply that bytes are output bytes.

Description:

b byte number, 0 through 9, or * for all bytes

a A or I:

A = tri-state control active (high impedance)

I = tri-state control inactive (not tri-stated)

Default: T*A (all bytes tri-stated, high impedance)

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another T command, or by a Reset or Self Test command.

This command is logically OR'ed with the external tri-state lines ETS0, ETS5 - ETS9, so if either is active, the byte(s) will be tri-stated. Bytes 0 through 4 share ETS0 as the external tri-state line. The tri-state line ETS0 can be enabled or disabled for bytes 0 to 4 using the N command, and the resulting enable state will be logically OR'ed with the programming of the T command for these bytes. The tri-state command does not cause bytes to become output bytes, or imply that bytes are output bytes.

Errors: If any bytes are not programmed, they will remain in their default state (high impedance). If (b) is omitted, the command will have no effect. If (a) is omitted, an Invalid Tri-State error will be generated.

Example: The following examples show how a sequence of tri-state commands will control the output state of each byte. For this example, it is assumed that all external tri-state command inputs (ETS0 - ETS5) are inactive.

Case	Command	Byte Tri-state Control									
		0	1	2	3	4	5	6	7	8	9
1	Power up (default)	A	A	A	A	A	A	A	A	A	A
2	T123I<CR>	A	I	I	I	A	A	A	A	A	A
3	T01A23I45A6789I<LF>	A	A	I	I	A	A	I	I	I	I
4	T*I;	I	I	I	I	I	I	I	I	I	I

A = tri-state control active (high impedance)
I = tri-state control inactive (not tri-stated)

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Case 1 is the power-up (default) condition, which tri-states all bytes (high impedance).

Case 2 sets the tri-state control inactive for bytes 1, 2, and 3, leaving 0, 4, 5, 6, 7, 8, and 9 in their previously programmed state.

Case 3 tri-states bytes 0 and 1, enables bytes 2 and 3 (non-tri-stated), and tri-states bytes 4 and 5, and enables bytes 6 through 9.

Case 4 tri-states all bytes (tri-state control active).

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Command: U (Update)

Syntax: U (c)...

Purpose: The update command specifies whether inputs and outputs are updated immediately on receiving a programming command (I or L command) or following a programming command when external handshake signals (Data Ready or Ready For Data strobes) occur.

Description: c a single letter which specifies the update conditions. Valid entries are:

- L Update the output data immediately on command (see the L (load output) command).
- R Update the output data with the latest received command when the Ready For Data strobe (RFD) occurs.
- I Update the input data immediately on command (see the I (input) command).
- D Update the input data specified by the last command when the Data Ready strobe (DRD) occurs.

Default: ULI (update the output on command, update the input on command).

Any or all of the update parameters can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another U command, or by a reset or self-test command. If a condition is not programmed, it will remain in its default (or previously programmed) state.

For the L condition, the output data is updated based on the L (Load) command.

For the R condition, the latest data received by the module will be output when an RFD strobe occurs or immediately if an RFD strobe has occurred since the last output command.

Note that output data may easily be overwritten and lost, since the most recent data received is always output. For example, if two L commands are received before a strobe occurs, the first data will be lost, and the most recent data will be output. To prevent this overwriting of data from occurring, use the Data Available (DAV) handshake and the QR command to read the state of Ready For Data (RFD). Each time the output data is updated, DAV is strobed to tell the external device that new data is available. The external device will then set RFD when it's ready for another output.

If the data reported back by the QR command is a 0, then the last data output has not yet been accepted by the external device. If a 1 is reported back, then the outputs can be updated with no loss of data (the external device has indicated a Ready For Data state).

For the I condition, input data is updated immediately when the I (Input) command is received.

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For the D condition, data is strobed in when the DRD strobe occurs (the external device indicates it has data ready). The module will respond with a data acknowledge (DAK) strobe when the input data is read from the module. The external device may then use the data acknowledge to update its data input for the VX4802 Module and indicate that it has new data ready for the VX4802 Module by setting the DRD line.

Note that once a DRD handshake occurs, the module will ignore subsequent DRD handshakes until the data is read by the controller. Use of the DAK handshake by the external device will prevent any DRD handshakes and data from being lost.

The DRD and RFD LEDs light when the handshake occurs (edge triggered), and do not reflect the active logic state of the handshake. A lit LED indicates that a valid handshake has occurred on the DRD or RFD handshake lines. The DAK and DAV LEDs do reflect the logic state of the signal. A lit LED indicates the handshake signal is at a TTL logic high for DAK and DAV.

When the DRD handshake is programmed, the module will immediately drive DAK active to signal the external device that it is ready for input data.

When the RFD handshake is programmed, the DAV signal will go active when a DRD strobe has occurred and data is output by the card.

Errors: If (c) is omitted, the command will have no effect. If an invalid parameter is specified, an Invalid Update Command error will be generated.

Example: The following example shows how a sequence of update commands will control the update condition(s):

		Update Conditions:	
Case	Command	Output	Input
1	Power-up (default)	L	I
2	UD<LF>	L	D
3	UR;	R	D
4	UIL<LF>	L	I
5	ULD<CR><LF>	L	D

Case 1 is the power-up (default) condition, which updates both outputs and inputs on command.
Case 2 updates the input on the DRD strobe, the output remains in its previously programmed condition to update on command.
Case 3 will update the output on an RFD strobe.
Case 4 will update the inputs and outputs on command.
Case 5 will update the output on command, and the input on a DRD strobe.

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Command: VER (Version)

Syntax: VER

Purpose: The version command returns the current software revision level of the module.

Description: The format of the returned data is:

VERSION X.X

where 'X.X' is the current revision level (1.0, for example).

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Command: X (interrupt enable or disable control)

Syntax: X(n)(c)...

Purpose: The X command enables and disables VXIbus request true interrupts.

Description: n is either A or I:

A = enable request true interrupt
I = disable request true interrupt

c specifies one of the following:

E = enable interrupt on error
R = enable interrupt on RFD handshake
D = enable interrupt on DRD handshake
* = enable interrupt on any of the above conditions

Default: XI (interrupt disabled)

The data can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another X command or by a Reset or Self Test command. If an interrupt is not specified, it will be disabled.

When a VXIbus Read Status command is sent to the VX4802, the module will set bit 6 of the returned status byte if the Request True Interrupt is set.

In IEEE-488 controller applications, where the VX4802 is a slave to an IEEE-488 Communications/Resource Manager Module such as the Tek/CDS VX4521, the Request True interrupt is used to generate an IEEE-488 Service Request (SRQ).

Errors: If (c) is invalid, an Invalid Interrupt Command error will be generated.

Examples:

XAE;	interrupts when a programming error occurs
XAR<CR><LF>	interrupts when the RFD handshake occurs
XARDE<LF>	interrupts when any of the three conditions occur
XI*<CR><LF>	disables all interrupts

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Command: Z [Tri-state (high impedance) level]

Purpose: The tri-state level command specifies the active level of the external tri-state control lines ETS0, ETS5 - ETS9.

Syntax: Z {(b)...(l)}

Description:
- b byte number, 0 through 9, or * for all bytes
- l H or L, Tri-state line active high (TTL logic 1) or low (TTL logic 0) respectively, where tri-state active is the state that puts the output lines in a high impedance state.

Default: Z*L (all bytes, external tri-state active low)

The bytes can be programmed in any order, and once programmed, the setup remains valid unless specifically overridden by another Z command, or by a Reset or Self Test command. Any bytes which are not programmed will remain in their default (or previously programmed) state. Note that all external tri-state lines have 22K pull-ups on them, so the external tri-states (by default) are not active if left unconnected.

NOTE: The external Tri-state lines are logically OR'd with the Tri-state Control command (T), so if either is active, the byte(s) will be tri-stated. Also note that even though bytes 0 - 4 share ETS0 as the external tri-state, their active levels can be individually programmed.

Errors: If (b) is omitted, the command will have no effect. If (l) is omitted or an invalid parameter is specified, an Invalid Tri-state Level Command error will be generated.

Example: The following example shows how a sequence of tri-state level commands will control the external tri-state active levels of each byte:

Case	Command	Individual Byte Tri-state Active Levels									
		0	1	2	3	4	5	6	7	8	9
1	Power-up (default)	L	L	L	L	L	L	L	L	L	L
2	Z123H<CR><LF>	L	H	H	H	L	L	L	L	L	L
3	Z01H23L456789H<LF>	H	H	L	L	H	H	H	H	H	H
4	Z*H;	H	H	H	H	H	H	H	H	H	H

Case 1 is the power-up (default) condition, which sets all external tri-state level inputs to active low.
Case 2 sets external tri-states for bytes 1, 2, and 3 as active high, leaving 0, 4, and 5 in their previously programmed state.
Case 3 sets 0 and 1 high, 2 and 3 low, and 4 through 9 high.
Case 4 sets all external tri-states for all ten bytes active high.

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SYSFAIL, Self Test, and Initialization

The VX4802 Module will execute a self test at power-up, or upon direction of a VXIbus hard or soft reset condition, or upon command. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4802's commander, sets the Reset bit in the VX4802's Control register.

At power-up, as well as during self test, all module outputs are tri-stated.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing a self test, and the Fail LED is lit.

2) Self test consists of outputting to each byte, binary 0 through 255, and verifying via loopback circuitry that the data is correct.

3) If the self test completes successfully, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). SYSFAIL* will be released within five seconds in normal operation.

   If the self test fails, the SYSFAIL* line remains active, and the module makes an internal record of what failure(s) occurred. It then enters the VXIbus FAILED state, which allows an error message to be returned to the module's commander.

The default condition of the VX4802 Module after the completion of power-up self test is as follows:

- All I/O pins tri-stated
- All bytes defined as inputs, active high
- All external handshake lines disabled
- Request True interrupts disabled (these interrupts cause an SRQ on IEEE-488 systems).

Self test can also be run at any time during normal operation by using the S command. The self test consists of internal circuitry tests, and I/O wraparound tests. The results of self test can be read using the query status commands QA or QN. If the self test fails, error '01' will be generated, and the module's Error LED will be lit.

SYSFAIL* Operation

SYSFAIL* becomes active during power-up, hard or soft reset, self test, or if the module loses any of its power voltages. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4802 Module to deactivate SYSFAIL* in all cases except when +5 volt power is lost.

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Section 4
Programming Examples

This section contains example programs which demonstrate how the various programmable features of the VX4802 are used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller.

Definition of BASIC Commands

The programming examples in this manual are written in Microsoft GW BASIC. These examples use the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

Command	Result
CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)	The CALL ENTER statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the VX4802.
CALL SEND (ADDRESS%, WRT$, STATUS%)	The CALL SEND statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.
END	Terminates the program.
FOR/NEXT	Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.
GOSUB n	Runs the subroutine beginning with line n. EX: GOSUB 750 - runs the subroutine beginning on line 750. The end of the subroutine is delineated with a RETURN statement. When the subroutine reaches the RETURN

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statement, execution will resume on the line following the GOSUB command.

GOTO n — Program branches to line n. EX: GOTO 320 - directs execution to continue at line 320.

IF/THEN — Sets up a conditional (IF/THEN) statement. Used with other commands, such as PRINT or GOTO, so that IF the stated condition is met, THEN the command following is effective. EX: IF I = 3 THEN GOTO 450 - will continue operation at line 450 when the value of variable I is 3.

REM or ' — All characters following the REM command or a ' are not executed. THese are used for documentation and user instructions. EX: REM **CLOSE ISOLATION RELAYS**

RETURN — Ends a subroutine and returns operation to the line after the last executed GOSUB command.

<CR> — Carriage Return character, decimal 13.

<LF> — Line Feed character, decimal 10.

Programming Example In BASIC

The following sample BASIC program shows how commands for the VX4802 might be used. This example assumes that the VX4802 has logical address 24 and is installed in a VXIbus mainframe that is controlled via an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent using a Capital Equipment Corp. IEEE-488 interface. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 21 and to have converted the VX4802 Module's logical address to an IEEE-488 primary address of decimal 24.

Lines which are indented and not numbered are comments which clarify what the program is doing at those points.

Example 1

Lines 10 through 70 initialize the PC's IEEE-488 interface card.

```
10 DEF SEG = &HCC00
     Defines memory location for IBM PC IEEE-488 Interface Module.
15 GOSUB 1000
     Determine memory location of CEC card.
20 INIT = 0
     Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
30 SEND = 9:ENTER = 21
```


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```
40 PC.ADDRESS% = 21
```
Defines PC controller's IEEE-488 address.
```
50 ADDR412% = 24
```
Defines VX4802's IEEE-488 address.
```
60 CONTROL% = 0
```
Defines I/O card as a bus controller.
```
70 CALL INIT(PC.ADDRESS%,CONTROL%)
80 RD$ = SPACE$(100)
```
Allocate space for the input string variable.
```
90 TM$ = CHR$(10)
```
Define the command terminator to be a line feed.
```
100 CLS
```
Clear the screen.
```
110 WRT$ = "R" + TM$
```
Reset the card.
```
120 CALL SEND(ADDR412%,WRT$,STATUS%)
```
Output the reset command.
```
130 CALL ENTER(RD$,LENGTH%,ADDR412%,STATUS%)
```
Read the default message. The card should respond with "READY".
```
140 PRINT "DEFAULT MESSAGE -> " + RD$
```
Print the default message.
```
150 WRT$ = "S;QA" + TM$
```
Issue a self test command to the card ("S"), and read the result back using the query ("QA") command. A semi-colon is used as the command terminator for the S command, and a line-feed as the terminator for the QA command.
```
160 CALL SEND(ADDR412%,WRT$,STATUS%)
```
Output the command.
```
170 CALL ENTER(RD$,LENGTH%,ADDR412%,STATUS%)
```
Read and print the results. The card should respond with "NO ERRORS".
```
180 PRINT "SELF TEST RESULT -> " + RD$
190 WRT$ = "M*O;T*I;L*D55" + TM$
```
Output a "55" hex to all bytes. The commands being issued do the following:

M*O M*O Defines all bytes as outputs

T*I T*I Un-tri-state outputs

L*D55 Load a 55 hex into all outputs
```
200 CALL SEND(ADDR412%,WRT$,STATUS%)
```
Output the command. The LED's on the front panel should display HEX "55" for all bytes. Read back the data using the Input command.
```
210 WRT$ = "I*" + TM$
220 CALL SEND(ADDR412%,WRT$,STATUS%)
```
Output the command.
```
230 CALL ENTER(RD$,LENGTH%,ADDR412%,STATUS%)
```
Read and print the results.
```
240 PRINT "THE DATA IS -> " + RD$
```
The card should respond with "55555555555555555555" as the data.
Output a 77,88,99,AA,BB, and CC,DD,EE,FF, AND 00 HEX to bytes 0 through 9 respectively.

```
250 WRT$ = "778899AABBCCDDEEFF00"
```


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```
260 CALL SEND(ADDR412%,WRT$,STATUS%)
      Output the command.
270 CALL ENTER(RD$,LENGTH%,ADDR412%,STATUS%)
      Read and print the results.
280 PRINT "THE DATA IS -> " + RD$
      The card should respond with "778899AABBCCDDEEFF00" as the data.

1000 '  SUB ROUTINE IDENTIFIES THE MEMORY LOCATION OF
1010 '  CEC IEEE-488 INTERFACE CARD ROM
1020 '
1030 FOR I = &H40 TO &HEC STEP &H4
1040 FAILED =0: DEF SEG = (I * &H100)
1050 IF CHR$ ( PEEK (50) ) <> "C" THEN FAILED =1
1060 IF CHR$ ( PEEK (51) ) <> "E" THEN FAILED =1
1070 IF CHR$ ( PEEK (52) ) <> "C" THEN FAILED =1
1080 IF FAILED = 0 THEN CECLOC = (I * &H100 ): I = &HEC
1090 NEXT I
1100 RETURN
```

Example 2

This is a more advanced program for the experienced user which demonstrates the use of the Load and Input commands. Lines 10 through 80 are required to initialize the IEEE-488 Bus Interface Module.

```
10 DEF SEG = &HCC00
      Defines memory location for IBM PC IEEE-488 Interface Module.
15 GOSUB 1000
      Determine memory location of CEC card.
20 SEND = 9:ENTER = 21:INIT = 0
30 PC.ADDRESS% = 21
      Defines I/O card address.
40 ADDR412% = 24
      Defines VX4802's IEEE-488 address.
50 CONTROL% = 0
      Defines I/O card as a bus controller.
60 TM$ = CHR$(10)
      Define line feed terminator.
70 CALL INIT(PC.ADDRESS%,CONTROL%)
80 IF STATUS% <> 0 THEN PRINT "*** 488 FATAL ERROR ***": STOP
90 RD$ = SPACE$(100)
      Allocate space for the input string variable.
      Reset the card, and then read its default message. The LEFT$ function is used to suppress
      the carriage return and line feed characters from the response data for printing to the screen.
      The default message response is "READY".
100 CLS
      Clear the screen.
110 WRT$ = "R" + TM$
```


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Reset the card.

```
120 CALL SEND(ADDR412%,WRT$,STATUS%)
130 CALL ENTER(RD$,LENGTH%,ADDR412%,STATUS%)
140 PRINT ("DEFAULT MESSAGE -> " + LEFT$(RD$,LENGTH%))
```

The commands being issued do the following:

M*O M*I Defines all bytes as outputs
T*I T*I Un-tri-state all bytes
I* Read back all bytes in the order 0-1-2-3-4-5-6-7-8-9.

The following lines show how the Load (L) command functions. They track steps 2-17 of the example following the L command in this manual.

```
150 STEPNUM = 2
160 WRT$ = "M*O;T*I;I*" + TM$
170 GOSUB 1500
```

Prints the command string, the step number, and the data. Output a 55 hex to all bytes. The expected readback data is "5555555555555555".

```
180 WRT$ = "L*D55;"
190 GOSUB 1500
```

Output a 00,11,22,33,44,55,66,77,88, and 99 hex to bytes 0 through 9 respectively. The expected readback data is "00112233445566778899". Note that no command terminator is needed.

```
200 WRT$ = "00112233445566778899"
```

Implicit load data (no command or terminator needed).

```
210 GOSUB 1500
```

Output a 01 hex to byte 1, an FA hex to bytes 5 and 0, a 20 hex to byte 2, an 88 hex to byte 4, and a CC hex to byte 3. This redefines the implicit output sequence to 1-5-0-2-4-3. The expected readback data is "FA0120CC88FA66778899".

```
220 WRT$ = "L1d01/50dfa/2d20/4d88/3dcc;"
230 GOSUB 1500
```

Output implicit data per the current sequence. The expected readback data is "22003355441166778899".

```
240 WRT$ = "001122334455"
```

Implicit load data.

```
250 GOSUB 1500
```

Use the load override command to set bit 4 of byte 1 high, without affecting the implicit output sequence. The expected readback data is "22103355441166778899".

```
260 WRT$ = "LO1S04;"
270 GOSUB 1500
```

Use the OR mask to set bit 7 of bytes 1, 2, and 3. The new load sequence is now defined as 1-2-3. The expected readback data is "2290B3D5441166778899".

```
280 WRT$ = "L123#80;"
290 GOSUB 1500
```

Output a 00,11, and 22 hex to bytes 1, 2, and 3 respectively. The expected readback data is "22001122441166778899".

```
300 WRT$ = "001122"
```

Implicit load data.

```
310 GOSUB 1500
```


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Redefine the output sequence to be 1-5-0-2-4-3-9-8-7-6. The expected readback data is "22001122441166778899".

```
320 WRT$ = "L1502439876;"
```

Define a new sequence.

```
330 GOSUB 1500
```

Output data per the new sequence. The expected readback data is "22003355441199887766".

```
340 WRT$ = "00112233445566778899"
```

Implicit load data.

```
350 GOSUB 1500
```

Output a 33 hex to all bytes. Note that this redefines the sequence to be 0-1-2-3-4-5-6-7-8-9. The expected readback data is "33333333333333333333".

```
360 WRT$ = "L*D33;"
```

Output 33 hex to all bytes.

```
370 GOSUB 1500
```

Set bit 2 of byte 0, reset bit 4 of byte 1, AND a 22 hex to byte 2 XOR a 22 hex to byte 3, and OR a 44 hex to byte 4. The expected readback data is "37232211773333333333".

```
380 WRT$ = "L0s02/1r04/2&22/3X22/4#44;"
390 GOSUB 1500
```

Output data per the new sequence 0-1-2-3-4. Note that data is not output until the required number of bytes is received. The expected readback data is "00112233443333333333".

```
400 WRT$ = "0011"
```

Implicit load (not enough data to be output).

```
410 GOSUB 1500
420 WRT$ = "223344"
```

Fill out the required data.

```
430 GOSUB 1500
```

Use the load override command to set bytes 4 and 1 to a 55 hex. The expected readback data is "00552233553333333333".

```
440 WRT$ = "Lo41d55"
450 GOSUB 1500
```

Output an AA,BB,CC,DD, and EE hex to bytes 0 through 4 respectively. The expected readback data is "AABBCCDDEE3333333333".

```
460 WRT$ = "AABBCCDDEE"
```

Implicit load.

```
470 GOSUB 1500
480 PRINT:INPUT "TYPE ENTER TO CONTINUE",DUMMY$
```

The following lines show how the Input (I) command is used. They track lines 2 through 10 of the example following the I command in this manual.

```
490 CLS:STEPNUM = 2
```

Define all bytes as outputs, un-tri-stated, data = 00112233445566778899.

```
500 WRT$ = "R;M*O;T*I;L*;00112233445566778899"
510 CALL SEND(ADDR412%,WRT$,STATUS%)
```

Read back the state of all bytes. The expected data is "00112233445566778899".

```
520 WRT$ = "I*;"
530 GOSUB 1500
```


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```
      Read back the states of bytes 1, 2, and 3 in that order.  The expected readback data is
      "112233".
540 WRT$ = "I123;"
      Input bytes 1, 2, and 3.
550 GOSUB 1500
      Read back the data without issuing a command (implicit read).
560 WRT$ = ""
570 GOSUB 1500
      Read back the data using the AND mask.  The expected data is "00110011445544550011".

580 WRT$ = "I*&55;"
      Input all bytes AND'ed with a 55 hex.
590 GOSUB 1500
      Do another implicit read.  Note that the data is still reported back with the mask overlaid.
600 WRT$ = ""
      Implicit read.
610 GOSUB 1500
      Read back all bytes without any masks.  The expected data is "00112233445566778899".
620 WRT$ = "I*;"
      Input all bytes.
630 GOSUB 1500
      Use the input override command to read byte 3 XOR'ed with an 11 hex, without affecting the
      input sequence.  The expected data is "22".
640 WRT$ = "IO3X11;"
650 GOSUB 1500
      Read back the data.  Note the preceding override command now has no effect.  The expected
      data is "00112233445566778899".
660 WRT$ = ""
      Implicit read.
670 GOSUB 1500
      Redefine the read sequence to be 5-4-3-0-1-2-6-7-8-9.  The expected data is
      "55443300112266778899".
680 WRT$ = "I5430126789"
      Change the input sequence.
690 GOSUB 1500
      Read byte 0 OR'ed with a 55 hex, byte 1 XOR'ed with an AA hex, and bytes 2, 3, 4, and 5.
      The expected readback data is "55BB22334455".
700 WRT$ = "I0#55/1XAA/2345"
710 GOSUB 1500
720 PRINT:INPUT "TYPE ENTER TO RETURN TO THE SYSTEM",DUMMY$
730 SYSTEM


1000 '  SUB ROUTINE IDENTIFIES THE MEMORY LOCATION OF
1010 '  CEC IEEE-488 INTERFACE CARD ROM
1020 '
1030 FOR I = &H40 TO &HEC STEP &H4
1040 FAILED =0: DEF SEG = (I * &H100)
1050 IF CHR$ ( PEEK (50) ) <> "C" THEN FAILED =1
```


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```
1060 IF CHR$ ( PEEK (51) ) <> "E" THEN FAILED =1
1070 IF CHR$ ( PEEK (52) ) <> "C" THEN FAILED =1
1080 IF FAILED = 0 THEN CECLOC = (I * &H100 ): I = &HEC
1090 NEXT I
1100 RETURN
```

The following subroutine outputs the contents of the string WRT$ to the VX4802 and then inputs data from the module into the string RD$. Both the input and output data are printed on the PC's display.

```
1500   LOCATE STEPNUM,1
1510   PRINT "cmd = " + WRT$
1520   CALL SEND(ADDR412%,WRT$,STATUS%)
1530   CALL ENTER(RD$,LENGTH%,ADDR412%,STATUS%)
1540   LOCATE STEPNUM,40
1550   PRINT "step " + STR$(STEPNUM) + ": DATA = " + LEFT$(RD$,LENGTH%)
1560   STEPNUM = STEPNUM + 1
1570   RETURN
```


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Appendix A
VXIbus Operation

The VX4802 Module is a C size single slot VXIbus Message-Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4802 Module is neither a VXIbus commander or VMEbus master, and therefore it does not have a VXIbus Signal register. The VX4802 is a VXIbus message based servant.

The module supports the Normal Transfer Mode of the VXIbus, using the Write Ready, Read Ready, Data In Ready (DIR), and Data Out Ready (DOR) bits of the module's Response register.

A Normal Transfer Mode read of the VX4802 Module proceeds as follows:

1. The commander reads the VX4802's Response register and checks if the Write Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

2. The commander writes the Byte Request command (0DEFFh) to the VX4802's Data Low register.

3. The commander reads the VX4802's Response register and checks if the Read Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

4. The commander reads the VX4802's Data Low register.

A Normal Transfer Mode Write to the VX4802 Module proceeds as follows:

1. The commander reads the VX4802's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready and DIR bits until they are true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX, depending on the End bit) to the VX4802's Data Low register.

The VX4802 Module also supports the Fast Handshake mode during readback. In this mode, the module is capable of transferring data at optimal backplane speed without the need of the commander's testing any of the handshake bits. The VX4802 Module asserts BERR* to switch from Fast Handshake mode to Normal Transfer mode, per VXI

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Specification. The VX4802's Read Ready, Write Ready, DIR and DOR bits react properly, in case the commander does not support the Fast Handshake Mode.

A Fast Handshake Transfer Mode Read of the VX4802 proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the VX4802's Data Low register.

2. The commander reads the VX4802's Data Low register.

The VX4802 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the VX4802's address space may cause incorrect operation of the module.

As with all VXIbus devices, the VX4802 module has registers located within a 64 byte block in the A16 address space.

The base address of the VX4802 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches.

VX4802 Configuration Registers

Below is a list of the VX4802 Configuration registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address:

REGISTER DEFINITIONS

Register	Address	Type	Value (Bits 15-0)
ID Register	0000H	RO	1011 1111 1111 1100 (BFFCh)
Device Type	0002H	RO	See Device Type definition below
Status	0004H	R	Defined by state of interface
Control	0004H	W	Defined by state of interface
Offset	0006H	WO	Not used
Protocol	0008H	RO	1111 0111 1111 1111 (F7FFh)
Response	000AH	RO	Defined by state of the interface
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below
Data Low	000EH	R	See Data Low definition below

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BIT DEFINITIONS

Register	Bit Location	Bit Usage	VX4802 Value	VX4802 Usage
ID	15-14	Device Class	10	Message Based
	13-12	Address Space	11	A16 only
	11-0	Manufact. ID	1111 1111 1100	Tek/CDS
Device Type	15-0	Device Type	1111 0100 1101 1101	Ones comp. of 802 with bit 11 set low.
Status	15	A24/32 Active	x	Not used
	14	MODID*	1	MODID line not active
			0	MODID line active
	13-4	Device dependent	xx xxxx xxxx	Not used
	3	Ready	0 or 1	Per VXI Spec.
	2	Passed	1	Passed
			0	VXI Interface failure
	1-0	Device dependent	xx	Not used
Control	15	A24/32 Enable	x	No effect
	14-2	Device dependent	xx xxxx xxxx xx	Not used
	1	SYSFAIL Inhibit	1	Disables module from driving Sysfail
			0	Enables module to drive Sysfail
	0	Reset	1	Reset
			0	Not reset
Protocol	15	CMDR*	1	Servant only
	14	Signal Reg.*	1	No Signal Reg.
	13	Master*	1	Slave only
	12	Interrupter	1	Interrupter
	11	FHS*	0	Fast Handshake capability
	10	Shared Memory*	1	No Shared Memory capability
	9-4	Reserved	11 1111	Not used
	3-0	Device dependent	1111	Not used
Response	15	Defined value of 0	0	Per VXI
	14	Reserved	1	Per VXI
	13	DOR	1 or 0	1 indicates that instrument data may be read at this time.
	12	DIR	1 or 0	1 indicates that instrument data may be sent to this module.
	11	ERR*	1	No VXI error has occurred
			0	VXI error has occurred.

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BIT DEFINITIONS

Register	Bit Location	Bit Usage	VX4802 Value	VX4802 Usage
Response	10	Read Ready	1 or 0	Indicates that data may be read from this module at this time. Set by the instrument following a "Byte Request" or any other VXI command requiring readback. Cleared on reset or when no data is left to send.
	9	Write Ready	1 or 0	Indicates that VXI commands or instrument data may be written at this time.
	8	FHS Active*	1	Indicates that this module is capable of supporting fast handshake (not requiring handshake) at this point in time.
	7	Locked*	1 or 0	Follows the state of the Clear Lock and Set Lock VXIbus commands.
	6-0	Device dependant	xxx xxxx	Not used

Data High - not implemented.

Data Low (read/write)

Word Serial Commands

A write to the Data Low register causes this module to execute some action based on the data written. This section describes the device specific Word Serial commands this module responds to and the results of these commands.

Read Protocol Command:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 1  1  0  1  1  1  1  1  1  1  1  1  1  1  1  1
```

If the Data Low register is read after this command, the contents are as follows:

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BIT DEFINITIONS

Register	Bit Location	Bit Usage	VX4802 Value	VX4802 Usage
Read Protocol	15	VXI Rev.	1	VXI Revision 1.3
	14-11	Device Dependant	1111	not used
	10	Reserved	1	Reserved
	9	RG*	1	response generation not supported
	8	EG*	0	event generation supported
	7	Zero	0	must be 0, per VXI specification.
	6	PI*	1	programmable interrupts not supported
	5	PH*	1	programmable interrupt handlers not supported
	4	TRG*	0	Word Serial Trigger command supported
	3	I4*	1	488.2 protocol not supported
	2	I*	0	VXIbus Instrument Protocol supported
	1	ELW*	1	Extended Long Word protocol not supported
	0	LW*	1	Long Word protocol not supported
Read STB	15-8	Upper byte	1111 1111	not used
	7	not used	0	not used
	6	RQS	1 or 0	set when a request true interrupt has been generated. Cleared upon the execution of this command.
	5-0	not used	0	not used
Async Mode Control	15-12	Status	1111 0111	command successful command unsuccessful. this occurs if bits 0 or 1 of this command are 1 indicating that a request is being made to have responses and/or events sent as signals. This module supports interrupts rather than signals.
	11-4	not used	1111 1111	not used
	3	Resp En*	0 or 1	if bits 15-12 are 1111, echoes bit 3 of the command.

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Register	Bit Location	Bit Usage	VX4802 Value	VX4802 Usage
	2	Event En*	0 or 1	if bits 15-12 are 1111, echoes bit 2 of the command.
	1	Resp Mode	0	interrupts are supported
	0	Event Mode	0	interrupts are supported
Control Response	15-12		1111	command passed
	11-7	not used	11111	not used
	6-0		1111111	no responses supported

VX4802 Interrupts

The VX4802 will interrupt its commander with the following "event" if any of the errors described by the ERR? command occur and an INT command has been issued to the VX4802 Module to enable interrupts.

Request True:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 1  1  1  1  1  1  0  1  <--Logical Address--->
```


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Appendix B
Input/Output Connections

Pinouts

S4-	1	byte 0 bit 0 (LSB)
	2	byte 0 bit 1
	3	byte 0 bit 2
	4	byte 0 bit 3
	5	byte 0 bit 4
	6	byte 0 bit 5
	7	byte 0 bit 6
	8	byte 0 bit 7 (MSB)
	9	ground
	10	byte 1 bit 0 (LSB)
	11	byte 1 bit 1
	12	byte 1 bit 2
	13	byte 1 bit 3
	14	byte 1 bit 4
	15	byte 1 bit 5
	16	byte 1 bit 6
	17	byte 1 bit 7 (MSB)
	18	ground
	19	byte 2 bit 0 (LSB)
	20	byte 2 bit 1
	21	byte 2 bit 2
	22	byte 2 bit 3
	23	byte 2 bit 4
	24	byte 2 bit 5
	25	byte 2 bit 6
	26	byte 2 bit 7 (MSB)
	27	ground
	28	byte 3 bit 0 (LSB)
	29	byte 3 bit 1
	30	byte 3 bit 2
	31	byte 3 bit 3
	32	byte 3 bit 4
	33	byte 3 bit 5
	34	byte 3 bit 6
	35	byte 3 bit 7 (MSB)
	36	ground

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	37	byte 4 bit 0 (LSB)
	38	byte 4 bit 1
	39	byte 4 bit 2
	40	byte 4 bit 3
	41	byte 4 bit 4
	42	byte 4 bit 5
	43	byte 4 bit 6
	44	byte 4 bit 7 (MSB)
	45	ground
	46	Data Acknowledge output
	47	Data Available output
	48	Data Ready input
	49	Ready for Data input
	50	ETS0 External Tri-State for bytes 0 through 4
S5-	1	byte 5 bit 0 (LSB)
	2	byte 5 bit 1
	3	byte 5 bit 2
	4	byte 5 bit 3
	5	byte 5 bit 4
	6	byte 5 bit 5
	7	byte 5 bit 6
	8	byte 5 bit 7 (MSB)
	9	ground
	10	byte 6 bit 0 (LSB)
	11	byte 6 bit 1
	12	byte 6 bit 2
	13	byte 6 bit 3
	14	byte 6 bit 4
	15	byte 6 bit 5
	16	byte 6 bit 6
	17	byte 6 bit 7 (MSB)
	18	ground
	19	byte 7 bit 0 (LSB)
	20	byte 7 bit 1
	21	byte 7 bit 2
	22	byte 7 bit 3
	23	byte 7 bit 4
	24	byte 7 bit 5
	25	byte 7 bit 6
	26	byte 7 bit 7 (MSB)
	27	ground

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28	byte 8 bit 0 (LSB)
29	byte 8 bit 1
30	byte 8 bit 2
31	byte 8 bit 3
32	byte 8 bit 4
33	byte 8 bit 5
34	byte 8 bit 6
35	byte 8 bit 7 (MSB)
36	ground
37	byte 9 bit 0 (LSB)
38	byte 9 bit 1
39	byte 9 bit 2
40	byte 9 bit 3
41	byte 9 bit 4
42	byte 9 bit 5
43	byte 9 bit 6
44	byte 9 bit 7 (MSB)
45	ground
46	External Tri-State for byte 9
47	External Tri-State for byte 8
48	External Tri-State for byte 7
49	External Tri-State for byte 6
50	External Tri-State for byte 5

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Appendix C
VXI Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted.

Term	Definition
Accessed Indicator	An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.
ACFAIL*	A VMEbus backplane line that is asserted under these conditions: 1) by the mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.
A-Size Card	A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.
Asynchronous Communication	Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.
Backplane	The printed circuit board that is mounted in a VXIbus mainframe to provide the interface between VXIbus modules and between those modules and the external system.
B-Size Card	A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.
Bus Arbitration	In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.
Bus Timer	A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.

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Client — In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10 — A 10-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

CLK100 — A 100-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

Commander — In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command — A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers — In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers — A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card — A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

Custom Device — A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

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Data Transfer Bus	One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.
DC SUPPLIES Indicator	A red LED indicator that illuminates when a DC power fault is detected on the backplane.
Device Specific Protocol	A protocol for communication with a device that is not defined in the VXIbus specification.
D-Size Card	A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 x 14.4 in x 1.2 in).
DTB	See Data Transfer Bus.
DTB Arbiter	A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.
DUT	Device Under Test.
ECLTRG	Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.
Embedded Address	An address in a communications protocol in which the destination of the message is included in the message.
ESTST	Extended STart/STop protocol; used to synchronize VXIbus modules.
Extended Self Test	Any self test or diagnostic power-up routine that executes after the initial kernel self test program.
External System Controller	The host computer or other external controller that exerts overall control over VXIbus operations.
FAILED Indicator	A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.
IACK Daisy Chain Driver	The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.
ID-ROM	An NVRAM storage area that provides for non-volatile storage of diagnostic data.

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Instrument Module — A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

Interface Device — A VXIbus device that provides one or more interfaces to external equipment.

Interrupt Handler — A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter — A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ — The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus — A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller — The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus mainframe or several mainframes. See Resource Manager.

Local Processor — The processor on an instrument module.

Logical Address — The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

Mainframe

Card Cage — For example, the Tektronix VX1400 Mainframe, an operable housing that includes 13 C-size VXIbus instrument module slots.

Memory Device — A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message — A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

Message Based Device — A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines — Module/system identity lines.

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Physical Address	The address assigned to a backplane slot during an access.
Power Monitor	A device that monitors backplane power and reports fault conditions.
P1	The top-most backplane connector for a given module slot in a vertical mainframe such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal mainframe.
P2	The bottom backplane connector for a given module slot in a vertical C-size mainframe such as the VX1400; or the middle backplane connector for a given module slot in a vertical D-size mainframe such as the VX1500.
P3	The bottom backplane connector for a given module slot in a vertical D-size mainframe such as the Tektronix VX1500.
Query	A form of command that allows for inquiry to obtain status or data.
READY Indicator	A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-volt power will extinguish this indicator.
Register Based Device	A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.
Requester	A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.
Resource Manager	A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.
Self Calibration	A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.
Self Test	A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-up.
Servant	A VXIbus message-based device that is controlled by a commander.
Server	A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.

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Shared Memory Protocol — A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

Slot 0 Controller — See Slot 0 Module. Also see Resource Manager.

Slot 0 Module — A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.

SMP — See Shared Memory Protocol.

STARX — Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STARY — Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STST — STart/STop protocol; used to synchronize modules.

SYNC100 — A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2ns of skew.

Synchronous Communications — A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL* — A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

System Clock Driver — A functional module that provides a 16-MHz timing signal on the Utility Bus.

System Hierarchy — The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

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Test Monitor	An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.
Test Program	A program, executed on the system controller, that controls the execution of tests within the test system.
Test System	A collection of hardware and software modules that operate in concert to test a target DUT.
TTLTRG	Open collector TTL lines used for inter-module timing and communication.
VXIbus Subsystem	One mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.
Word Serial Protocol	A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).
Word Serial Communications	Inter-device communications using the Word Serial Protocol.
WSP	See Word Serial Protocol.
10-MHz Clock	A 10 MHz, ±100 ppm timing reference. Also see CLK10.
100-MHz Clock	A 100 MHz, ±100 ppm clock synchronized with CLK10. Also see CLK100.
488-To-VXIbus Interface	A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

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Appendix D
Options

Option 01

This option changes the output drivers from CMOS to TTL with 64mA drive capability. There are no changes in operation.

Specification Changes:

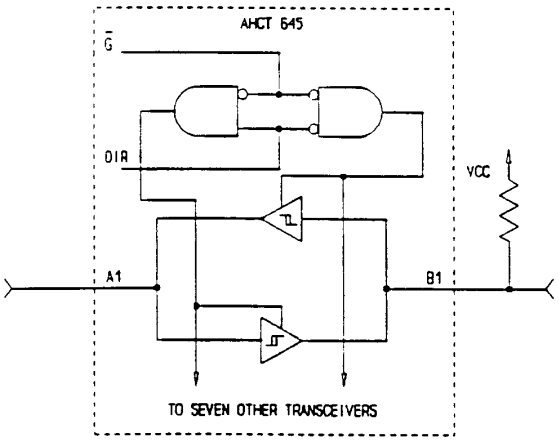
Output low current	64 mA
Input low current	0.75 mA
Output high voltage with supplying 15 mA:	2.4V
Output low voltage sinking 64 mA:	0.55V

Option 02

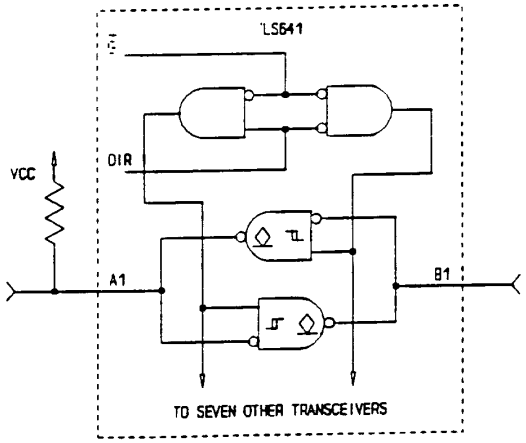
This option changes the output drivers to open collector drivers and removes the pullups from the output. There are no changes in operation.

Specification Changes:

Output high voltage	(customer supplied) 5.5 maximum
Output low current	64 mA
Input current	0.75 mA



Standard Board
Output Driver



Option 02 Installed
Output Driver

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Option 1D

Option 1D for the VX4802 Programmable Digital I/O Module changes selected channels for +24V input or output capability.

On channels 1, 2, 3, and 4 the 74HCT245 transceiver is replaced with a Darlington transistor array and pullup resistors. This changes these channels to output only and inverts the state of the outputs. The output inversion can be compensated for by specifying active low true logic with the M (Mode) command and by interchanging the & (AND) and # (OR) in the commands L (Load Output) and LO (Load Output Override).

Channel 0 is converted to input only with a 10,000 ohm/1500 ohm divider replacing the 74HCT245 transceiver to make it compatible with +24 volt logic inputs. Bit 7 (S07 - pin 8 of connector S4) is used for bringing in the external +24VDC for the output pullup resistors.

Specification Changes for Channel 0:

Changed to input only	
Input high voltage (Vih)	16V min.
Input low voltage (Vih)	6V max.

Specification Changes for Channels 1, 2, 3, and 4:

Changed to output only	Polarity inverted
Output high through 2.35K ohm	Customer-supplied +24V
Output low voltage (Vol)	1.1V max. @ 100 mA

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Appendix E: Performance Verification

This procedure verifies the performance of the VX4802 Programmable Digital I/O Module. The test sequences may be performed in your current VXIbus system if it meets the requirements described in Table 2. Also, it is not necessary to complete the entire procedure if you are only interested in a specific performance area. Some tests depend on the proper operation of previously verified functions so it is best to follow the order as presented.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

Please familiarize yourself with the following conventions which apply throughout this procedure:

- Each test sequence begins with a table, similar to the one below, which provides information and requirements specific to that section. The item number appearing after each piece of equipment refers to an entry in Table 1 *Required Test Equipment.* Immediately following the table, you will be given instructions for interconnecting the VX4802 under-test and for checking the performance parameters. Results may then be recorded on a photocopy of the Test Record on page A–25.

Equipment Requirements	Loop-Back Cable Assembly (item 2)
Prerequisites	All prerequisites listed on page A–22

- This procedure assumes that you will be using the National Instruments PC GPIB controller and software (NI-488.2M) configured as described in Table 3. In the test sequences, you will be instructed to issue Interface Bus Interactive Control (ibic) commands to set up the VX4802 under-test and other associated VXIbus test instruments. Please refer to the NI-488.2M User Manual for additional information. If you are using a different controller or software, simply substitute the equivalent commands.

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- Commands to the VX4802 may be entered in upper or lower case. However, to avoid confusion between the alphanumeric characters; e.g. one (1) and L or zero (0) and o, all commands are shown in the case which provides the greatest distinction. Use special care when interpreting these characters.

NOTE. *If at any time you observe a QE response or an ERR light from the VX4802 or VX4801, you must perform a status query (ibwrt "qa", ibrd 100) to read and clear the error condition.*

Prerequisites

The verification sequences in this procedure are valid when the following requirements are met:

- The VX4802 module covers are in place and the module is installed in an approved VXIbus mainframe as described in Section 2 of the Operating Manual
- The VX4802 has passed the power-on self test
- The VX4802 has been operating for a warm-up period of at least 10 minutes in an ambient environment as specified in Section 1 of the Operating Manual

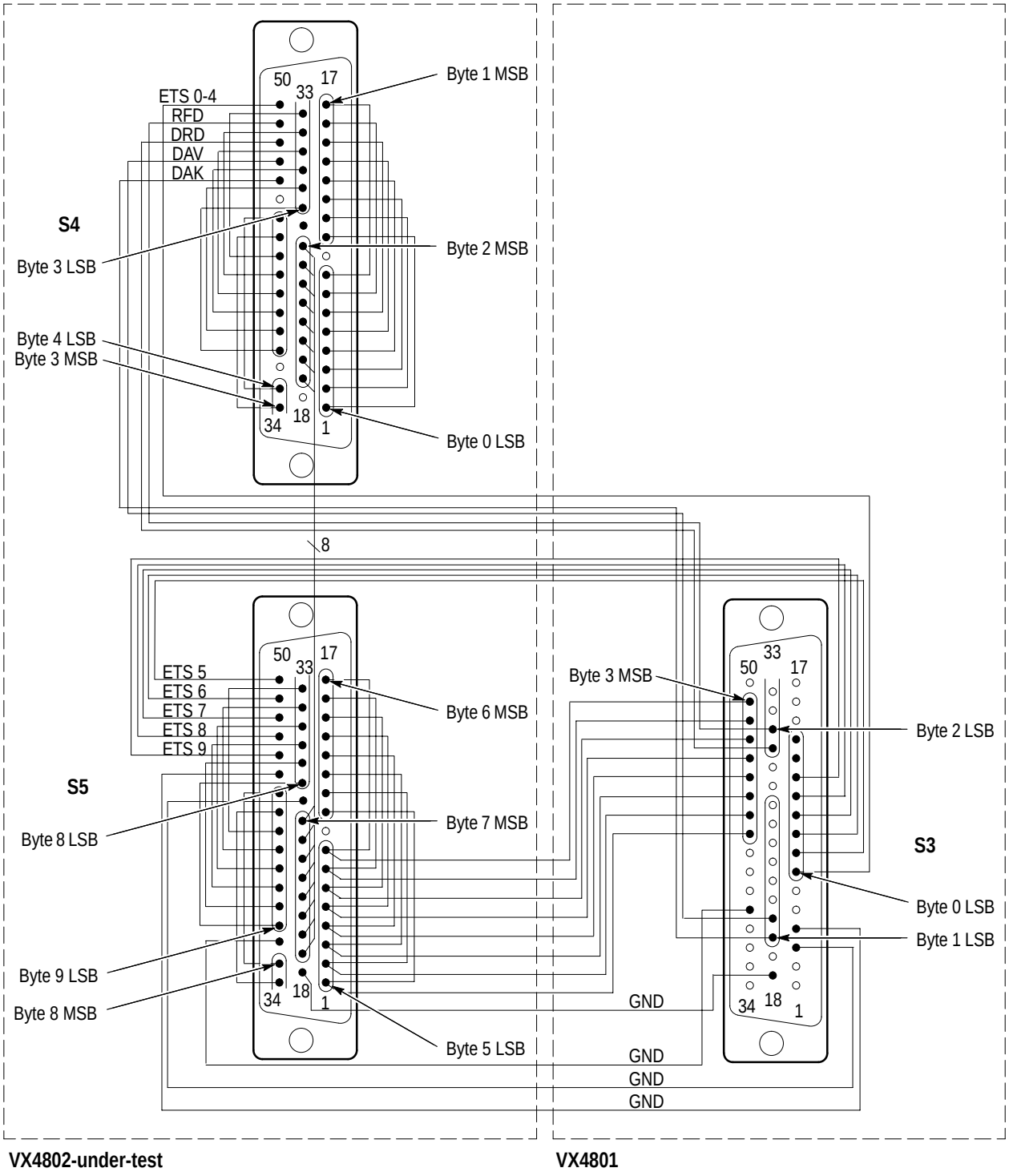
Equipment Required

Table 1 lists the equipment required for this procedure. You may use instrumentation other than the recommended example if it meets the minimum requirements.

Table 1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. Digital I/O Module	4 byte TTL/CMOS data I/O	Tek/CDS VX4801	Checking external functions
2. Loop-Back Cable Assembly	Male DD-50 Connector, three required (Tektronix part number 131-1344-00)	Assemble as shown in figure 4 using 26 AWG ribbon wire	Checking TTL/CMOS Data I/O, Tri-State, and Handshake.

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View of Solder Side. Allow approximately 4 in. length of interconnect wire between modules.

Figure 4: Loop-Back Cable Assembly

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VX4802 Under-Test Configuration

In order to perform this procedure, the VX4802 under-test must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table 2.

Table 2: Elements of a Minimum VX4802-Under-Test System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	Two available slots for VX4802 under-test and the VX4801 digital signal source in addition to the Slot 0 controller	Tektronix VX1400A, VX1410	Provides power, cooling, and backplane for VXIbus modules
2. Slot 0 Controller	Resource Mgr, Slot 0 Functions, IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Provides Slot 0 and Resource Mgr functions, and GPIB interface
3. VXIbus System Controller	VXIbus-Talker/Listener/Controller	IBM 486 PC with National Insruments GPIB PC2A card & NI-488.2M software, GPIB cable (Tek P/N 012-0991-00)	Provides VXIbus command and response interface
4. VX4802 Under-Test	Not applicable	Not applicable	Verify its performance
5. Digital I/O Module	4 byte TTL/CMOS I/O	VX4801	Provides test signal I/O

Test System Configuration

Table 3 describes the VXIbus system configuration assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in test sequences. (Note that no secondary addressing is assumed.)

Table 3: Test System Configuration (Assumed)

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	0D (hex)	13
VX4802-under-test	VX4802	Slot 1	01	1
VX4801	VX4801	Slot 2	02	2

Test Record

Photocopy the Test Record which follows and record the performance verification results for your module.

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Table 4: VX4802 Test Record

VX4802 Serial Number:	Temperature and Relative Humidity:
Date of Last Calibration:	Verification Performed by:
Certificate Number:	Date of Verification:

Table 5: VX4802 Performance Tests

VXIbus Interface Checks		**Logical Address, IEEE Address, Slot No., MFG., Model, etc.**	
Table Command Response	1st. Response		
	2nd Response		
	3rd Response		
		Passed	**Failed**
Preliminary Tests	Self Test		
	Interrupt SRQ		
TTL/CMOS I/O Data Bytes	Even to Odd		
	Odd to Even		
Tri-State Control Signals	Internal		
	External		
Handshake Control Signals	Transmit		
	Receive		

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Self Test

The VX4802 includes a built-in self test function (BITE) which is automatically executed each time the power is turned on and when the Internal Self Test (S) command is issued. BITE uses internal routines and circuitry to confirm basic I/O functionality. No external test equipment is required.

During the self test, all outputs are set to a high impedance mode (tri-state) and then internal loop-back circuitry and test patterns are used to verify all I/O channels.

In addition to BITE, the front panel indicator lights display the current status of power, the assertion of SYSFAIL*, backplane cycles, data handshake signals, and individual I/O data for each byte. The Query command may also be used at any time during operation to determine the current state of the module.

Following the VXIbus system startup sequence, the green PWR light on the VX4802 front panel indicates that the self test has passed and that the +5 V power supply is operational. If the +5 V power supply fails, or its fuse opens, the PWR light will be off, the FAILED light will be on, and SYSFAIL* will be asserted indicating a module failure.

NOTE. *If you experience an error indication from the Slot 0 Resource Manager, the VX4802-under-test, or any other VXIbus module, investigate and correct the problem before proceeding. Common items to check are logical address conflicts (primary and secondary; see Table 3), breaks in the VXIbus daisy chain signals, improper seating of a module, loose GPIB cable, improperly set Slot 0 single-step switch, or loose or blown fuses.*

Performance Verification Tests

The order of execution of this procedure has been chosen to minimize system setup and functional dependency. Because some tests rely on the success of their predecessors, it is recommended that you perform all sequences in order.

VXIbus Interface

This sequence verifies that the VX4802 configures correctly and communicates properly with your GPIB system controller.

Equipment Requirements	No additional test equipment is required.
Prerequisites	All prerequisites listed on Page A–22

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***NOTE**. If you are using National Instruments NI-488.2 software you may wish to select the buffer 1 mode to allow more comfortable viewing of the ASCII response. Just type buffer 1 as directed in Table 6.*

1. To verify the system configuration, send the TABLE command to the Slot 0 Resource Manager and confirm the responses shown in Table 6. Your configuration may not be identical, but the responses should be similar.

Table 6: VXIbus System Configuration

Command to Type	Response to Verify
ibic	
buffer 1	
ibfind VX4521	
ibwrt "table"	
ibrd 200	03
!	LA 0, IEEE 13, Slot 0, MFG FFDh, MODEL VX4521, PASS, , RM. .
!	LA 1, IEEE 01, Slot 1, MFG FFCh, MODEL VX4802, PASS, TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL ..
!	LA 2, IEEE 02, Slot 2, MFG FFCh, MODEL VX4801, PASS, TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL ..

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***NOTE**. Make sure your Slot 0 controller and the VX4802-under-test are set to the same interrupt level (see User Manual for location of interrupt setting). Also, if you are using National Instruments NI-488.2 software, make sure Auto Serial Polling is disabled to prevent the SRQ from being reset prior to a visual check.*

2. Verify the VX4802 VXIbus interrupt capability with the following steps:

a. Enable the generation of the VXI Request True interrupt and force a VXIbus interrupt by sending an illegal command:

```
ibfind VX4802

ibwrt "xae"
```
(Enable VXI Request True interrupt)

```
ibwrt "vxi"
```
(Observe: VX4802 ERR light on)

```
ibrd 100
```
(Observe: QE response and S in 2nd digit of VX4521)

***NOTE**. The read statement above serves to un-address the Slot 0 controller which allows it to detect the VXIbus interrupt and assert the SRQ (indicated by the S).*

b. Check that the ERR light on the VX4802 is on and that the VX4521 displays an S in the second digit of the front panel indicating an SRQ pending. The QE response indicates an error message pending.

c. With the following commands, perform a serial poll with the VX4802 and verify a response of 40 hexadecimal, which indicates that it was the interrupting device. Also, verify that the VX4521 Slot 0 controller SRQ is no longer asserted. Finally, send a query and read the error message:

```
ibrsp
```
(Observe: VX4521 no longer displays S.)

```
ibwrt "qa"

ibrd 100
```
(Observe: SYNTAX ERROR and ERR light off)

TTL/CMOS I/O This test sequence verifies that each eight bit port (10) of the VX4802 can function as both an active high and an active low TTL/CMOS input/output port.

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Equipment Requirements	Loop-back assembly (item 2)
Prerequisites	All prerequisites listed on page A–22

1. Attach the loop-back assembly as shown in Figure 4, which connects the odd bytes to the even bytes respectively (0 to 1, 2 to 3, 4 to 5).
2. Perform a self test and query for any error codes (in ASCII format) with the VX4802 device-under-test and the VX4801:

   ```
   ibfind VX4801

   ibwrt "s;qa"

   ibrd 100
   ```
   (Observe: NO ERRORS)

   ```
   set VX4802

   ibwrt "s;qa"

   ibrd 100
   ```
   (Observe: NO ERRORS)

NOTE. *If at any time in this procedure you do not observe the result expected, check the front panel error light and/or perform an error Status Query* (`ibwrt "qa"<cr> ibrd 100<cr>`)*. No additional commands will be accepted until an error condition is cleared.*

3. Verify the odd byte data inputs and the even byte data outputs with the following steps:

   a. Reset the VX4802 to its power-up state, set the mode for the odd bytes (1, 3, 5, 7, 9) to be active low inputs, for the even bytes (0, 2, 4, 6, 8) to be active high outputs initialized with a Load Output value of 55, and set the tri-state function to be inactive (* => all bytes, i => inactive):

   ```
   set VX4802

   ibwrt "r;m13579iL02468oh;L02468d55;t*i"
   ```

   b. Perform an input and verify a response of 55AA on even/odd channels:

   ```
   ibwrt "i*"

   ibrd 100
   ```
   (Observe: 55AA55AA55AA55AA55AA)

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c. Repeat the previous test with the logic sense reversed; i.e. odd bytes (1, 3, 5) set to active high and the even bytes set to active low. Verify the complementary response:

```
ibwrt "m13579ih02468oL"

ibwrt "i*"

ibrd 100
```
(Observe: AA55AA55AA55AA55AA55)

4. To verify the even byte data inputs and the odd byte data outputs, reset the VX4802 to its power-up state, set the mode for the even bytes (0, 2, 4, 6, 8) to be active low inputs, for the odd bytes (1, 3, 5, 7, 9) to be active high outputs initialized with a Load Output value of 55, and set the tri-state function to be inactive. Perform an input of all bytes and verify an AA55 response on even/odd channels. Finally, reverse the logic sense mode of the even and odd bytes and verify the complementary response of 55AA:

```
ibwrt "r;m02468iL13579oh;L13579d55;t*i"

ibwrt "i*"

ibrd 100
```
(Observe: AA55AA55AA55AA55AA55)

```
ibwrt "m02468ih13579oL"

ibwrt "i*"

ibrd 100
```
(Observe: 55AA55AA55AA55AA55AA)

Tri-State Function

This test sequence verifies that the internal tri-state commands and the external tri-state signals are functioning properly for each I/O byte.

NOTE. *The Tri–State test sequence does not apply to VX4802 modules having Option 02. Modules which do not have Option 02 utilize an internal 22 kΩ pull-up to +5 V which will appear as a high logic level when in the tri-state mode.*

Equipment Requirements	Loop-back assembly (item 2)
Prerequisites	All prerequisites listed on page A–22

1. Install the loop-back assembly on the VX4802 under-test and the VX4801 as shown in Figure 4.

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2. Verify the internal tri-state command with the following steps:

   a. Reset the VX4802 to the power-on default state (all bytes initially tri-stated). Then set the mode for the odd bytes to be active high inputs and for even bytes to be active high outputs with a Load Output value of 00. Finally, leave the even (output) bytes tri-stated, but set the odd (input) byte tri-states to be inactivate. Perform an input of all bytes and verify that the even bytes are in tri-state mode and not driving the odd byte inputs (odd inputs not pulled low):

   ```
   set VX4802

   ibwrt "r;m13579ih02468oh;L02468d00;t13579i"

   ibwrt "i*"

   ibrd 100
   ```
   (Observe: response of 00FF00FF00FF00FF00FF)

   b. Repeat the test with the even bytes set as inputs and the odd bytes set as tri-stated outputs. Verify that the odd bytes are in tri-state mode and not driving the even byte inputs (even inputs not pulled low):

   ```
   ibwrt "r;m02468ih13579oh;L13579d00;t02468i"

   ibwrt "i*"

   ibrd 100
   ```
   (Observe: response of FF00FF00FF00FF00FF00)

3. Verify the external tri-state signals with the following steps:

   a. Set up the VX4801 to unassert the external tri-state signals (ETS0, ETS5–ETS9) to the VX4802:

   ```
   ibfind VX4801

   ibwrt "r;m0oh;L0d3F;t0i;i*"
   ```

   b. Set up the VX4802 for odd bytes to be inputs and for even bytes to be outputs with a Load Output value of 00, and for external tri-state ETS0 to be enabled for bytes 0, 2, and 4. Read all bytes and verify the 00 output value on all bytes (internal and external tri-state unasserted):

   ```
   set VX4802

   ibwrt "r;m13579ih02468oh;L02468d00;t*i;N024E;i*"

   ibrd 100
   ```
   (Observe: response of 00000000000000000000)

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c. Set the VX4801 to assert the even byte external tri-state signals to the VX4802 and verify a response of 00FF00FF00FF00FF00FF..:

```
set VX4801

ibwrt "L0dEA;i*"

set VX4802

ibwrt "i*"

ibrd 100
```
(Observe: response of 00FF00FF00FF00FF00FF..)

d. Set the VX4801 to assert the odd byte external tri-state signals to the VX4802 and then set the VX4802 for the even bytes to be inputs, for the odd bytes to be outputs with a Load Output value of 00, and for external tri-state ETS0 to be enabled for bytes 1 and 3. Finally, verify a response of FF00FF00FF00FF00FF00 (odd bytes tri-stated):

```
set VX4801

ibwrt "L0dD4;i*"

set VX4802

ibwrt "r;m02468ih13579oh;L13579d00;t*i;N13E"

ibwrt "i*"

ibrd 100
```
(Observe: response of FF00FF00FF00FF00FF00..)

Check Handshake

This test sequence verifies that data can be transferred to and from the VX4802 using the four handshake signal lines Data Ready (DRD), Data Acknowledge (DAK), Ready for Data (RFD), and Data Available (DAV).

NOTE. *Typing errors will result in a VX4802 error condition which must be cleared before subsequent commands will be recognized. If at any time you suspect that an error condition exists, send an error query and read the result before continuing with the test sequence* (`ibwrt "qa" <cr>, ibrd 100 <cr>`).

Equipment Requirements	Loop-back assembly (item 2)
Prerequisites	All prerequisites listed on page A–22

1. Connect the loop-back assembly as shown in Figure 4.

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2. Using the following steps, verify a data byte transfer (55 hex) from the VX4802 (byte 5) to the VX4801 (byte 3) using the Ready for Data (RFD) from the VX4801 and the Data Valid (DAV) from the VX4802:

   a. Set the VX4802 for a positive edge handshake, to update the output data on receipt of a Ready For Data (RFD) strobe, to update the input data on receipt of a Data Ready (DRD) strobe, and for byte 5 to be an active high output, initialized with a Load Output data value of 55 (hex), and with the tri-state inactive:

   ```
   set VX4801

   ibwrt "r"

   set VX4802

   ibwrt "r;p*+;urd;m5oh;L5d55;t5i"
   ```

   b. Set the VX4801 mode for byte 2 to be an active high output (for assertion of RFD), for bytes 1 and 3 to be active high inputs (byte 1 to detect DAV and byte 3 to input data), and for all tri-states to be inactive:

   ```
   set VX4801

   ibwrt "r;m2oh13ih;t*i"
   ```

   c. Set the VX4801 to input byte 1 (with all bits masked except bit 1) and byte 3 (data) and verify that DAV is un–asserted (i.e. byte 1, bit 0 = 0) and consequently, that there is no data (byte 3 = 00):

   ```
   ibwrt "i1&01/3"

   ibrd 100"
   ```
   (Observe: 0000 and VX4802 DAV light off)

   d. To assert RFD to the VX4802, set the VX4801 to load byte 2 with an Output Data value of 01 (asserts RFD to the VX4802) and verify that the VX4802 correspondingly asserts DAV:

   ```
   ibwrt "L2d01"
   ```
   (Observe: VX4802 DAV light on)

   e. Set the VX4801 to input bytes 1 and 3 and verify receipt of DAV (byte 1 bit 1 = 1) and data (byte 3 = 55):

   ```
   ibwrt "i1&01/3"

   ibrd 100
   ```
   (Observe: 0155 return value)

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3. Using the following steps, verify a data byte transfer (AA hexadecimal) from the VX4801 (byte 3) to the VX4802 (byte 5) using the Data Ready (DRD) and Data Acknowledge (DAK) handshake lines:

   a. Set the VX4801 mode for bytes 2 (handshake) and 3 (data) to be active high outputs, with byte 3 initialized to a Load Output data value of AA, and set all tri-states to be inactive:

   ```
   ibwrt "r;m23oh;L3dAA;t*i"
   ```

   b. Set the VX4802 for a positive edge handshake, to update the output data on receipt of a DRD strobe, to update the input data on receipt of a DRD strobe, and for byte 5 to be an active high input with its tri-state inactive (note that after the data is strobed in with DRD from the slave, the VX4802 will in turn generate the DAK):

   ```
   set VX4802

   ibwrt "r;p*+;urd;m5ih;t5i"
   ```

   c. Send a byte 5 input command to the VX4802, and verify that a response of N, indicating that the module is waiting for a DRD strobe:

   ```
   ibwrt "i5"

   ibrd 100
   ```
   (Observe N; waiting for DRD strobe)

   d. Set the VX4801 to send a DRD strobe (byte 2, bit 2) and then verify that the VX4802 DAK light is off:

   ```
   set VX4801

   ibwrt "L2d02"
   ```
   (Send DRD to VX4802; observe DAK light off)

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e. Send a byte 5 input command to the VX4802 and verify that the DAK light is on. Then read the data, observe a response of AA, perform a second read and observe that the VX4802 is again waiting for a DRD strobe:

```
set VX4802
```
(Observe VX4802 DAK light off)

```
ibwrt "i5"
```
(Observe DAK light on)

```
ibrd 100
```
(Observe AA response)

```
ibwrt "i5"
```

```
ibrd 100
```
(Observe N response, indicating waiting for DRD)

This completes the VX4802 verification procedure.

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Appendix F
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

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User-Replaceable Parts

Part Description	Part Number
User Manual	070-9154-XX
Label, Tek CDS	950-0940-00
Label, VXI	950-1105-00
Fuse, Micro 4 Amp 125 V Fast	159-0374-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-1329-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00

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