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Service Manual

Tektronix

2232
Digital Storage Oscilloscope
Serial Numbers B010100 to B029999

070-7067-01

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

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OPERATORS SAFETY SUMMARY

The safety information in this summary is for operating personnel. Warnings and cautions will also be found throughout the manual where they apply.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual



This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1–1.

Symbols as Marked on Equipment



DANGER—High voltage.



Protective ground (earth) terminal.



ATTENTION—Refer to manual.

Power Source

This product is intended to operate from a power source that does not apply more than 250 V rms between the supply conductors or between either supply conductor and ground. A protective ground connection, by way of the grounding conductor in the power cord, is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the product input or output terminals. A protective ground connection, by way of the grounding conductor in the power cord, is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts, including knobs and controls that may appear to be insulating, can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see Figure 2–2.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of the correct type, voltage rating and current rating as specified in the parts list for your product.

Do Not Operate in an Explosive Atmosphere

To avoid explosion, do not operate this instrument in an explosive atmosphere.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

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SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

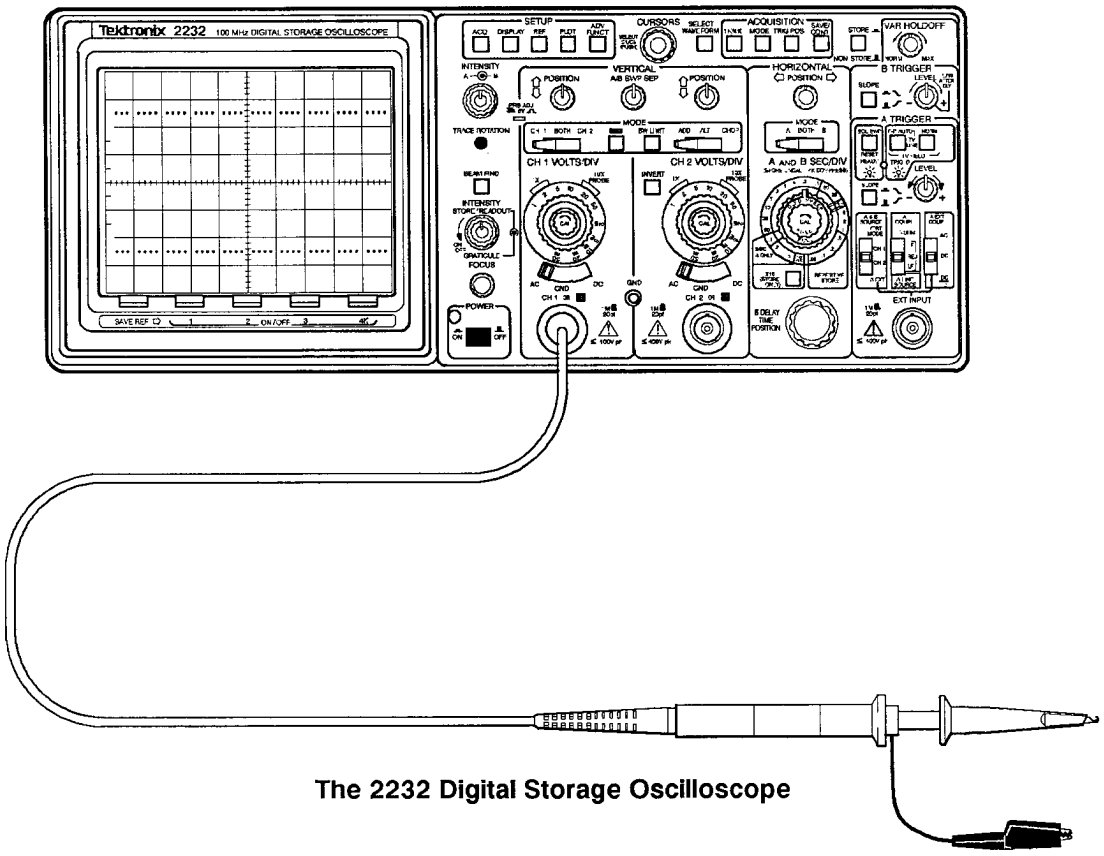
Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding connector in the power cord is essential for safe operation.

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The 2232 Digital Storage Oscilloscope

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SPECIFICATION

INTRODUCTION

The TEKTRONIX 2232 is a combination nonstorage and digital storage portable, dual-channel oscilloscope with 100 MHz analog bandwidth and up to 100 MS/s digital sampling rate. The vertical channels have calibrated deflection factors from 2 mV to 5 V per division. The Variable VOLTS/DIV gain control increases the deflection factor at least 2.5 to 1 on any VOLTS/DIV setting. Vertical display modes are CH 1, CH 2, and BOTH, with a choice in BOTH of ADD, ALT, or CHOP. A BW LIMIT feature limits the vertical amplifier system and the A Trigger system to 20 MHz.

The horizontal deflection system calibrated A Sweep speeds range from 0.5 s to 50 ns per division; calibrated B Sweep speeds range from 50 ms to 50 ns per division. A X10 MAG control decreases sweep time per division of the A and B Sweeps by a factor of 10. The fastest sweep-speed time of 50 ns per division is extended to 5 ns per division in X10 MAG. The Variable SEC/DIV control may be used to increase the non-store sweep time per division by a factor of up to four times from the calibrated time per division determined by the SEC/DIV switch setting. In STORE Mode, rotating the Variable SEC/DIV control out of the CAL detent position compresses a 4K sample acquisition record into a record of 1K samples (called 4K compress mode). Also in STORE Mode, the A SEC/DIV X10 Multiplier adds calibrated storage time bases of 1, 2, and 5 s per division to the NON STORE A Sweep speed range for low-frequency signal acquisitions.

The digital storage and display portion of the 2232 is microprocessor controlled. Selecting the digital storage features is done with a combination of front-panel controls and menu choices. Selected front-panel controls are read by the microprocessor to determine their settings. Those settings are reported to the user in a crt readout display generated for the CH 1 and CH 2 VOLTS/DIV switch, the A and B SEC/DIV switch, the DELAY TIME Position control, the Voltage and Time cursor differences (on STORE Mode displays only), the position of AC-GND-DC switches, and the A Trigger LEVEL voltage level. All the parametric information for the waveform display is therefore visible when a hard copy is made to maintain a permanent record of the display. When in STORE (digital) mode, additional readout information is displayed showing storage acquisition mode, SAVE REF memories, if displayed, SAVE mode, and SWEEP LIMIT, if active.

Digital storage maximum sampling rate is 100 megasamples per second with a maximum stored record length per waveform of either 4096 bytes (4K) for single-channel acquisitions or 2048 bytes (2K) for dual-channel acquisitions (ALT or CHOP). In CHOP mode, both channels are sampled simultaneously. The digital storage acquisition system has glitch-catching capabilities for glitch widths as narrow as 10 ns.

Up to three waveform sets (CH 1 and/or CH 2) of 1K record length (512 data points each waveform for dual-channel acquisitions) or one waveform set of 4K record length (2K when dual-channel) may be stored in the SAVE REF memories. In either case, previous data is over-written. A saved waveform may be recalled for display and comparison with the current acquisition waveform and any or all of the other saved waveforms. The X10 MAG control is also functional for STORE waveforms and provides for horizontal expansion of 10 times. The CURSOR Control may be used to reposition the display window on X10 expanded STORE waveforms to view the entire acquisition.

On stored waveforms (current acquisition and saved displays), voltage and time measurements may be made using CURSORS. The cursors are positioned to the waveform of interest and then to the points of interest in the waveform. The ΔV and Δt crt readouts indicate the voltage difference and timing difference between the positions of the cursors on the waveform selected. Horizontal positioning of the 1K display window within a 4K acquisition record is also provided by the CURSOR Positioning control. In this manner, the entire 4K record length may be scrolled through for display on the crt. The displayed 1K window of a 4K record length acquisition waveform is the data stored when using the SAVE REF memory to save 1K waveform data. A 4K record length acquisition may also be compressed to a 1K record length by rotating the variable SEC/DIV control away from the CAL detent position. The complete waveform is then only one display window in length. A 4K compress waveform may be saved in any of the three 1K SAVE REF memories.

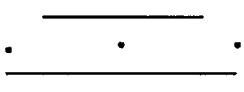
ACCURACY AND RESOLUTION

Finite resolution affects any measurement using discrete numbers. All digital storage stores amplitude values as discrete numbers and associates those amplitude

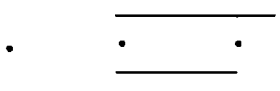
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numbers with discretely numbered times. Many measurements must be rounded or truncated. The size of the truncation or rounding becomes a part of the measurement error. For example, the following line is 1.5 units long. If it must be drawn as a line connecting points one unit apart, then it may be drawn as a line one unit long or two units long, depending on how it occurs relative to the points.

Case 1: Line approaches three points:



Case 2: Line approaches two points:



There are several places where measurements are quantified, and a one-count error in the measurement cannot be detected. The input channels are digitized to an 8-bit resolution, where one division is (ignoring expansion and compression) 25 counts. This means there is an inherent error of 1/25 of a division in any voltage measurement at acquisition time. Averaging can increase the resolution of a voltage measurement above the sampler's eight-bit limit. To use the increased resolution, the display has a 10-bit dynamic range in the vertical axis, as well as the horizontal axis. An averaged signal has a resolution of 100 points per division (ignoring expansion and compression). In addition, the averaged number is stored with up to twelve bits of resolution. Expansion is required to view the eleventh and twelfth bits of increased resolution.

Time is quantified to determine when each sample occurred and which display interval gets each sample. Time is resolved by storing, for example, 4K points. If 4K points are stored, 4K time intervals are represented. However, in 4K mode, not all of the 4K-point resolution may be displayed on the 10-bit (1K-point) screen. Therefore, if 4K COMPRESS is selected to present the whole picture on-screen at once, only 1K resolution remains in the display. When peak-detected information is acquired, events with high-frequency content such as fast steps, or short pulses, can only be located within the time interval from which the peaks came. Even though two display points result from the interval, the event cannot be tied with certainty to the first or second point in the interval.

Time is also quantified to determine where to put points in REPETITIVE acquisitions, where the points acquired at 50 ns intervals fill only part of the screen. A counting device produces a number to represent the portion of 50 ns between the samples acquired and the ones that would have included the trigger. This number ranges from 0 to about 205, which allows accurate placement into the display record. The display record will have at most 100 slots to choose from on the basis of the 0–205 number (this is where each slot represents 0.5 ns of acquisition time, and the counter's resolution is about 0.244 ns per count).

STANDARD ACCESSORIES

The following items are standard accessories shipped with the 2232 instrument:

1 Operators Manual
1 Users Reference Guide
2 Probe Packages
1 Front Panel Cover
1 Accessory Pouch
1 Power Cord
1 Fuse
1 DB-9 Male Connector and Connector Shell
1 Loop Clamp
1 Flat Washer
1 Self-Tapping Screw

For part numbers and further information about both standard and optional accessories, refer to "Options and Accessories" (Section 7) of this manual. Your Tektronix representative, local Tektronix Field Office, or Tektronix products catalog can also provide additional accessories information.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1–1) are valid when the instrument has been adjusted at an ambient temperature between +20°C and +30°C (+68°F and 86°F), has had a warm-up period of at least 20 minutes, and is operating at an ambient temperature between 0°C and +50°C (32°F and 122°F) (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1–2. This instrument meets the requirements of MIL-T-28800D for Type III, Class 5 equipment, except where noted otherwise.

Physical characteristics of the instrument are listed in Table 1–3.

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Table 1-1
Electrical Characteristics

Characteristics	Performance Requirements
VERTICAL DEFLECTION SYSTEM	
Deflection Factor	
Range	2 mV per division to 5 V per division in a 1-2-5 sequence.
DC Accuracy (NON-STORE)	
+15°C to +35°C	±2%.
0°C TO +50°C	±3%.[a] For 5 mV per division to 5 V per division VOLTS/DIV switch settings, the gain is set at a VOLTS/DIV switch setting of 10 mV per division. 2 mV per division gain is set with the VOLTS/DIV switch set to 2 mV per division.
On Screen DC Accuracy (STORE)	
+15°C to +35°C	±2%.
0°C TO +50°C	±3%.[a] Gain set with the VOLTS/DIV switch set to 5 mV per division.
Storage Acquisition Vertical Resolution	8-bits, 25 levels per division. 10.24 divisions dynamic range.[a]
Range of VOLTS/DIV Variable control	Continuously variable between settings. Increases deflection factor by at least 2.5 to 1.
Step Response (NON-STORE Mode)	
Rise Time	
0°C TO +35°C	
5 mV per division to 5 V per division	3.5 ns or less.[a]
2 mV per division	4.4 ns or less.[a]
+35°C to +50°C	
5 mV per division to 5 V per division	3.9 ns or less.[a]
2 mV per division	4.4 ns or less.[a] Rise time is calculated from: $\text{Rise Time} = \frac{0.35}{\text{Bandwidth (-3 dB)}}$

[a] **Performance Requirement not checked in manual.**

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Table 1-1 (cont)

Characteristics	Performance Requirements
Step Response (STORE Mode)	
Useful Storage Rise Time	
SAMPLE	**Single Trace** $\frac{\text{SEC/DIV X 1.6}^{a}}{100}$ s; **CHOP/ALT** $\frac{\text{SEC/DIV X 1.6}^{a}}{50}$ s
PEAKDET or ACCPEAK with SMOOTH	$\frac{\text{SEC/DIV X 1.6}^{a}}{50}$ s; $\frac{\text{SEC/DIV X 1.6}^{a}}{25}$ s Rise time is limited to 3.5 ns minimum with derating over temperature (see NON-STORE Rise Time).
Aberrations (NON-STORE and STORE in Default Modes)	
2 mV per division to 50 mV per division	+4%, -4%, 4% p-p.
0.1 V per division to 0.2 V per division	+6%, -6%, 6% p-p.
0.5 V per division	+6%, -6%, 6% p-p.[a]
1 V per division to 5 V per division	+12%, -12%, 12% p-p.[a] Measured with a five-division positive-going reference signal, from a 50-Ω coaxial cable terminated in 50 Ω at the input connector with the VOLTS/DIV Variable control in the CAL detent. Vertically center the top of the reference signal. Set A Trigger SLOPE switch to positive.
NON-STORE Bandwidth (-3 dB)	
0°C to +35°C	
5 mV per division to 5V per division	DC to at least 100 MHz.
2 mV per division	DC to at least 80 MHz.
+35°C to +50°C	
2 mV per division to 5V per division	DC to at least 80 MHz.[a] Measured with a vertically centered six-division reference signal, from a 50-Ω source driving a 50-Ω coaxial cable terminated in 50 Ω at the input connector; with the VOLTS/DIV Variable control in the CAL detent.
BW LIMIT (-3dB)	20 MHz ±10%.
AC Coupled Lower Cutoff Frequency	10 Hz or less at -3 dB.[a]

[a] **Performance Requirement not checked in manual.**

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Table 1-1 (cont)

Characteristics	Performance Requirements	
Useful Storage Performance		
RECORD, SCAN and ROLL Store Modes		
SAMPLE Acquisition, no AVERAGE		
1 μs per division to 5 s per division	**Single Trace**	**CHOP/ALT**
	$\frac{10}{\text{SEC/DIV}}$ Hz[a]	$\frac{5}{\text{SEC/DIV}}$ Hz[a]
EXT CLOCK (up to 100 kHz)	$\frac{\text{EXT}}{10}$ Hz[a]	$\frac{\text{EXT}}{20}$ Hz[a]
	Useful storage performance is limited to the frequency where there are 10 samples per sine wave signal period at the maximum sampling rate. (Maximum sampling rate is 100 MHz.) This yields a maximum amplitude uncertainty of 5%. Accuracy at the useful storage bandwidth limit is measured with respect to a six-division 50 kHz reference sine wave.	
PEAK DETECT		
Sine-Wave Amplitude Capture (5% p-p maximum amplitude uncertainty)	10 MHz.[a]	
Pulse Width Amplitude Capture (50% p-p maximum amplitude uncertainty)	10 ns.	
REPETITIVE Store Mode		
SAMPLE and AVERAGE	**Single Trace**	**CHOP/ALT**
0.05 μs per division	100 MHz (-3 dB)[b]	100 MHz (-3 dB)[b]
0.1 μs per division	100 MHz (-3 dB)[a,b]	50 MHz (-3 dB)[a]
0.2 μs per division to 2 μs per division (5% maximum amplitude uncertainty)	$\frac{10}{\text{SEC/DIV}}$ Hz[a]	$\frac{5}{\text{SEC/DIV}}$ Hz[a]
ACCPEAK		
0.05 μs per division to 5 s per division	Same as NON-STORE Bandwidth.[a]	

[a] **Performance Requirement not checked in manual.**

[b] **One hundred MHz bandwidth derated for temperatures outside 0°C to +35°C and at 2 mV per division VOLTS/DIV setting as for NON-STORE.**

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Table 1-1 (cont)

Characteristics	Performance Requirements
AVERAGE Mode	
Sweep Limit	Adjustable from 1 to 998,000 or NO LIMIT. Resolution is 1 from 1 to 200; 2 from 202 to 1000; 10 from 1010 to 2000; 20 from 2020 to 10,000; 100 from 10,100 to 20,000; 200 from 20,200 to 100,000; 1,000 from 101,000 to 200,000; 2,000 from 202,000 to 998,000.[a]
Weight of Last Acquisition	1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, or 1/256 (MENU selections). AVERAGE mode default weight is 1/4.[a]
NON-STORE CHOP Mode Switching Rate	500 kHz ±30%.[a]
A/D Converter Linearity	Monotonic with no missing codes.[a]
Analog CH1/CH2 Delay Match	±1.0 ns.[a]
NON-STORE Common-Mode Rejection Ratio (CMRR)	At least 10 to 1 at 50 MHz. Checked at 10 mV per division for common-mode signals of six divisions or less with the VOLTS/DIV Variable control adjusted for the best CMRR at 50 kHz.
Input Current	1 nA or less (0.5 division or less trace shift when switching between DC and GND input coupling with the VOLTS/DIV switch set to 2 mV per division).[a]
Input Characteristics	
Resistance	1 MΩ ±2%.[a]
Capacitance	20 pF ±2 pF.[a]
Maximum Safe Input Voltage (CH 1 and CH 2)	See Figure 1-1 for maximum input voltage vs frequency derating curve.
DC and AC Coupled ⚠	400 V (dc + peak ac) or 800 V ac p-p at 10 kHz or less.[a]
Channel Isolation STORE and NON-STORE	Greater than 100 to 1 at 50 MHz.
POSITION Control Range	At least ±11 divisions from graticule center.
A/B SWP SEP Control Range (NON-STORE Mode Only)	±3.5 divisions or greater.
Trace Shift with VOLTS/DIV Switch Rotation	0.75 division or less; VOLTS/DIV Variable control in the CAL detent.[a]
Trace Shift as the VOLTS/DIV Variable Control is Rotated	1 division or less.[a]
Trace Shift with INVERT	1.5 divisions or less.[a]

[a] **Performance Requirement not checked in manual.**

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Table 1–1 (cont)

Characteristics	Performance Requirements
TRIGGERING SYSTEM	
A Trigger Sensitivity	
P–P AUTO and NORM	**10 MHz** / **60 MHz** / **100 MHz**
Internal	0.35 div / 1.0 div / 1.5 div
External	40 mV / 120 mV / 150 mV
	External trigger signal from a 50-Ω source driving a 50-Ω coaxial cable terminated in 50 Ω at the input connector.
HF REJ Coupling	Reduces trigger signal amplitude at high frequencies by about 20 dB with rolloff beginning at 40 kHz ±25%. Should not trigger with a one-division peak-to-peak 250 kHz signal when HF REJ is ON.
LF REJ Coupling	Attenuates signals below 40 kHz (–3 dB point at 40 kHz ±25%). Should not trigger with a 0.35 peak-to-peak 25 kHz signal when LF REJ is on.
P–P AUTO Lowest Usable Frequency	20 Hz with 1 division internal or 100 mV external.[a]
TV LINE	
Internal	0.35 div.[a]
External	35 mV p-p.[a]
TV FIELD	≥1 division of composite sync.[a]
B Trigger Sensitivity (Internal Only)	**10 MHz** 0.35 div; **60 MHz** 1.0 div; **100 MHz** 1.5 div
EXT INPUT Maximum Input Voltage ⚠	400 V (dc + peak ac) or 800 V ac p-p at 10 kHz or less.[a] See Figure 1–1 for maximum input voltage vs frequency derating curve.
Input Resistance	1 MΩ ±2%.[a]
Input Capacitance	20 pF ±2.5 pF.[a]
AC Coupled Lower Cutoff Frequency	10 Hz or less at –3 dB.[a]
LEVEL Control Range	
A Trigger (NORM)	
INT	May be set at any voltage level of the trace that can be displayed.[a]
EXT, DC	At least ±1.6 V, 3.2 V p-p.
EXT, DC ÷ 10	At least ±16 V, 32 V p-p.[a]
B Trigger (Internal)	May be set at any point of the trace that can be displayed.[a]

[a] **Performance Requirement not checked in manual.**

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Table 1-1 (cont)

Characteristics	Performance Requirements		
VAR HOLDOFF Control (NON-STORE Holdoff)	Increases A Sweep holdoff time by at least a factor of 10. STORE holdoff is a function of microprocessor activity and the pretrigger acquisition. The VAR HOLDOFF control maintains some control over the STORE holdoff by preventing a new trigger from being accepted by the storage circuitry until the next (or current, if one is in progress) NON-STORE holdoff has completed.		
Trigger Level Readout Accuracy +15 °C to +35 °C	±(0.3% division, +5% of reading). Applies to ±10 divisions from zero volts.		
Acquisition Window Trigger Points			
Pretrigger	Seven-eighths of the waveform acquisition window is prior to the trigger (other trigger points are selectable via the MENU).		
Midtrigger	One-half of the waveform acquisition window is prior to the trigger (other trigger points are selectable via the MENU).		
Post Trigger	One-eighth of the waveform acquisition window is prior to the trigger (other trigger points are selectable via the MENU).		
Point-Selectable Triggering	PRETRIG[a]	MIDTRIG[a]	POST TRIG[a]
1K Record Length	128	512	896
4K Record Length	512	2048	3584
HORIZONTAL DEFLECTION SYSTEM			
NON-STORE Sweep Rates			
Calibrated Range			
A Sweep	0.5 sec per division to 0.05 µs per division in a 1-2-5 sequence of 22 steps.[c]		
B Sweep	50 ms per division to 0.05 µs per division in a 1-2-5 sequence of 19 steps.[c]		
STORE Mode Ranges			
REPETITIVE	0.05 µs per division to 0.5 s per division.[a,d]		
RECORD	1 µs per division to 50 ms per division.[a,d]		
ROLL/SCAN	0.1 s per division to 5 s per division. (A Sweep only).[a,d]		

[a] Performance Requirement not checked in manual.
[c] The X10 MAG control extends the maximum sweep speed to 5 ns per division.
[d] The X10 MAG control extends the maximum sweep speed to 5 ns per division. The 4k COMPRESS control multiplies the SEC/DIV by 4.

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Table 1-1 (cont)

Characteristics	Performance Requirements	
NON-STORE Accuracy	**Unmagnified**	**Magnified**
+15°C to +35°C		
0.5 s per division to 0.1 μs per division	±2%	±3%
0.05 μs per division	±2%	±4%
0°C to +50°C		
0.5 s per division to 0.1 μs per division	±3%[a]	±4%[a]
0.05 μs per division	±3%[a]	±6%[a]
	Sweep accuracy applies over the center eight divisions. Exclude the first 40 ns of the sweep for magnified sweeps and anything beyond the 100th magnified division.	
STORE Accuracy	See Horizontal Differential Accuracy and Cursor Time Difference Accuracy.[a]	
NON-STORE Sweep Linearity		
0.5 s per division to 10 ns per division	±0.1 division.	
5 ns per division	±0.15 division. Linearity measured over any two of the center eight divisions. Exclude the first 40 ns and anything past the 100th division of the X10 magnified sweeps.	
Digital Sample Rate	**Single Trace**	**CHOP/ALT**
SAMPLE (1 μs per division to 5 s per division)	$\frac{100}{\text{SEC/DIV}}$ Hz[a]	$\frac{50}{\text{SEC/DIV}}$ Hz[a]
PEAKDET or ACCPEAK (1 μs per division to 5 s per division)	100 MHz[a]	100 MHz[a]
REPETITIVE Store (0.05 μs per division to 0.5 μs per division)	100 MHz[a]	100 MHz[a]
External Clock		
Input Frequency		
Slow	Dc to 1 kHz.	
Fast	Dc to 100 kHz.	
Digital Sample Rate	100 MHz in ACCPEAK and PEAKDET, otherwise it is equal to the input frequency.[a]	
Screen Update Rate		
Slow	One data pair for every second falling clock edge.[a]	
Fast	Varies with record length and sweep speed.[a]	

[a] **Performance Requirement not checked in manual.**

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Table 1-1 (cont)

Characteristics	Performance Requirements
External Clock (cont)	
Duty Cycle	10% or greater (1 μs minimum hold time).[a]
Ext Clock Logic Thresholds	Logic Thresholds are TTL compatible.[a]
Maximum Safe Input Voltage ⚠	25 V (dc + peak ac) or 25 V p-p ac at 1 kHz or less.[a]
Input Resistance	Greater than 10 kΩ (LSTTL compatible).[a]
STORE Mode Resolution	
Acquisition Record Length	1024 or 4096 data points.[a]
Single Waveform Acquisition Display	1024 data points (100 data points per division across the graticule area).[a]
CHOP or ALT Acquisition Display	512 data points (50 data points per division across the graticule area).[a]
Horizontal POSITION Control Range	Start of the 10th division will position past the center vertical graticule line in X1; 100th division in X10 magnified and NON-STORE.
Horizontal Variable Sweep Control Range	
NON-STORE	Continuously variable between calibrated settings of the SEC/DIV switch. Extends the A and the B Sweep speeds by at least a factor of 2.5 times over the calibrated SEC/DIV settings.
STORE	Horizontal Variable Sweep has no affect on the STORE Mode time base. Rotating the Variable SEC/DIV control out of the CAL detent position horizontally compresses a 4K point acquisition record to 1K points in length, so that the whole record length can be viewed on screen. Screen readout is altered accordingly.
Displayed Trace Length	
NON-STORE	Greater than 10 divisions.
STORE	10.24 divisions.[a]
Delay Time	
0.5 μs per division to 0.5 s per division (A Sweep)	
Delay POSITION Range	Less than (0.5 div + 300 ns) to greater than 10 divisions. Delay Time is functional, but not calibrated, at A Sweep speeds faster than 0.5 μs per division.
NON-STORE Delay Jitter	One part or less in 5,000 (0.02%) of the maximum available delay time.

[a] Performance Requirement not checked in manual.

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Table 1-1 (cont)

Characteristics	Performance Requirements
Delay Time Differential Measurement Accuracy (Runs After Delay only)	
+15°C to +35°C	±1% of reading, ±0.5% of full scale (10 divisions).
0°C to +50°C	±2% of reading, ±0.5% of full scale (10 divisions).[a] Exclude delayed operation when the A and B SEC/DIV knobs are locked together at any sweep speed or when the A SEC/DIV switch is faster than 0.5 μs per division. Accuracy applies over the B DELAY TIME POSITION control range.
DIGITAL STORAGE DISPLAY	
Vertical	
Resolution	10 bits (1 part in 1024).[a] Display waveforms are calibrated for 100 data points per division.
Position Registration	
NON-STORE to STORE	±0.5 division at graticule center at VOLTS/DIV switch settings from 2 mV per division to 5 V per division.
CONTINUE to SAVE	±0.5 division at VOLTS/DIV switch settings from 2 mV per division to 5 V per division.
SAVE Mode Expansion or Compression Range	Up to 10 times as determined by the remaining VOLTS/DIV switch positions up or down. 2 mV per division acquisitions cannot be expanded, and 5 V per division acquisitions cannot be compressed. Any portion of a stored waveform vertically magnified or compressed up to 10 times can be positioned to the top and to the bottom of the graticule area.
Storage Display Expansion Algorithm Error	±0.1% of full scale.[a]
Storage Display Compression Algorithm Error	+0.16% of reading ±0.4% of full scale.[a]
Horizontal	
Resolution	10 bits (1 part in 1024).[a] Calibrated for 100 data points per division.
Differential Accuracy	Graticule indication of time cursor difference is ± 2% of the readout value, measured over the center eight divisions.
SAVE Mode Expansion Range	10 times as determined by the X10 MAG switch.
Expansion Accuracy	Same as the Vertical.[a]

[a] **Performance Requirement not checked in manual.**

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Table 1-1 (cont)

Characteristics	Performance Requirements
DIGITAL READOUT DISPLAY	
CURSOR Accuracy	
Voltage Difference	± 3% of the ΔV readout value, ±0.4% of full scale (8 divisions). Applies within center 6 divisions.
Time Difference	
RECORD or ROLL/SCAN	
SAMPLE or AVERAGE	±1 display interval.
PEAKDET or ACCPEAK	±2 display interval.[a]
REPETITIVE	
SAMPLE or AVERAGE	±(2 display interval + 0.5 ns).[a]
ACCPEAK	±(4 display interval + 0.5 ns).[a] A display interval is the time between two adjacent display points on a waveform.
X-Y OPERATION (X1 MAGNIFICATION ONLY)	
Deflection Factors	Same as vertical deflection system with the VOLTS/DIV Variable controls in the CAL detent position.
NON-STORE Accuracy	Measured with a dc-coupled, five-division reference signal.
X-Axis	
+15°C to +35°C	±3%.
0°C to +50°C	±4%.[a]
Y-Axis	Same as vertical deflection system.[a]
NON-STORE Bandwidth (-3 dB)	Measured with a five-division reference signal.
X-Axis	DC to at least 2.5 MHz.
Y-Axis	Same as vertical deflection system.[a]
NON-STORE Phase Difference Between X-Axis and Y-Axis Amplifiers	±3 degrees from dc to 150 kHz.[a] Vertical Input Coupling set to DC.
STORE Accuracy	
X-Axis and Y-Axis	Same as digital storage vertical deflection system.[a]
Useful Storage Bandwidth	
RECORD and REPETITIVE Store Modes	$\frac{5}{\text{SEC/DIV}}$ Hz[a]

[a]Performance Requirement not checked in manual.

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Table 1-1 (cont)

Characteristics	Performance Requirements
STORE Mode Time Difference Between Y-Axis and X-Axis Signals	
RECORD, SCAN, and ROLL Modes	±1.0 ns.[a]
REPETITIVE Store	$\frac{\text{SEC/DIV}}{100} \times 4$ [a]
PROBE ADJUST	
Output Voltage on PRB ADJ Jack	0.5 V ±5%.
Probe Adjust Signal Repetition Rate	1 kHz ±20%.[a]
Z-AXIS	
Sensitivity (NON-STORE Only)	5 V causes noticeable modulation. Positive-going input decreases intensity. Usable frequency range is dc to 20 MHz.
Maximum Input Voltage ⚠	30 V (dc + peak ac) or 30 V p-p at 1 kHz or less.[a]
Input Resistance	Greater than 10 kΩ.[a]
POWER SUPPLY	
Line Voltage Range	90 Vac to 250 Vac.[a]
Line Frequency	48 Hz to 440 Hz.[a]
Maximum Power Consumption	85 watts (150 VA).[a]
Line Fuse	2 A, 250 V, slow blow.[a]
Primary Circuit Dielectric Requirement	Routine test to 1500 V rms, 60 Hz, for 10 seconds without breakdown.[a]
CRT DISPLAY	
Display Area	8 cm X 10 cm.[a]
Standard Phosphor	P31.[a]
Nominal Accelerating Voltage	14 kV.[a]
X-Y PLOTTER OUTPUT	
Maximum Safe Applied Voltage, Any Connector Pin ⚠	25 V (dc + peak ac) or 25 V p-p ac at 1 kHz or less.[a]
X and Y Plotter Outputs	
Pen Lift/Down	Fused relay contacts, 100 mA maximum.[a]
Output Voltage Levels	500 mV per division ±10%. Center screen is 0 V ±1 division. Measured with a dc-coupled, five-division reference signal.
Series Resistance	2 kΩ ±10%.[a]
4.2 V Output	±10% through 2 kΩ.[a]

[a] Performance Requirement not checked in manual.

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Table 1-1 (cont)

Characteristics	Performance Requirements
MEMORY	
Non-Volatile Memory	26 Kbytes.[a]
Power-Down	
Battery Voltage	Memory retained for battery voltages greater than 2.3 V.[a]
Data Retention	Memory maintained at least 6 months without instrument power.[a]
Battery Life	Power-down data retention specification shall be maintained for 3 years without battery change.[a]
Power-down Detection	
Threshold	Fail asserted for supply drop to less than 4.5 V.[a] Reset held until supply is greater than 4.75 V.[a]
Reset Delay	Power-down interrupt to reset delay ≥1 ms.[a]
GPIB OPTION	
GPIB Requirements	Complies with ANSI/IEEE Standard 488-1978.[a]
RS-232-C OPTION	
RS-232-C Requirements	Complies with EIA Standard RS-232-C.[a]
Baud Rates	
Available Rates	110, 300, 600, 1200, and 2400 baud.[a]
Accuracy	<1% error.[a]

[a] **Performance Requirement not checked in manual.**

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Table 1–2
Environmental Characteristics

Characteristics	Performance Requirements
Environmental Requirements	The instrument meets the following MIL–T–28800D requirements for Type III, Class 5, Style D equipment, except where noted otherwise.[a]
Temperature	
Operating	0°C to +50°C (+32°F to +122°F).[a]
Nonoperating	–40°C to +71°C (–40°F to +160°F).[a] Tested to MIL–T–28800D, para 4.5.5.1.3 and 4.5.5.1.4, except that in para 4.5.5.1.3 steps 4 and 5 (–10°C operating test) are performed before step 2 (–40°C nonoperating test). Equipment shall remain off upon return to room ambient temperature during step 6. Excessive condensation shall be removed before operating during step 7.
Altitude	
Operating	To 4,500 meters (13,716 feet).[a] Maximum operating temperature decreases 1°C per 1,000 feet above 5,000 feet.
Nonoperating	To 15,240 meters (50,000 feet).[a] Exceeds requirements of MIL–T–2880D, para 4.5.5.2.
Humidity	
Operating and Nonoperating	5 cycles (120 hours) referenced to MIL–T–28800D para 4.5.5.1.2.2 for Type III, Class 5 instruments. Operating and nonoperating at 95%, –5% to +0%, relative humidity. Operating, +30° C to +50°C; nonoperating, +30°C to +60°C.[a]
EMI (electromagnetic interference)	Meets radiated and conducted emission requirements per VDE 0871, Class B.[a] To meet EMI regulations and specifications, use the specified shielded cable and metal connector housing with the housing grounded to the cable shield on the AUXILIARY CONNECTOR.
Vibration	
Operating	15 minutes along each of three major axes at a total displacement of 0.015 inch p–p (2.3 g at 55 Hz) with frequency varied from 10 Hz to 55 Hz to 10 Hz in one–minute sweeps. Hold for 10 minutes at 55 Hz in each of the three major axes. All major resonances are above 55 Hz. Meets requirements of MIL–T–22800D, para 4.5.5.3.1.[a]

[a] **Performance Requirement not checked in manual.**

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Table 1-2 (cont)

Characteristics	Performance Requirements
Shock	
Operating and Nonoperating	30 g half-sine, 11 ms duration, three shocks per axis each direction, for a total of 18 shocks.[a] Meets requirements of MIL-T-22800D, para 4.5.5.4.1, except limited to 30 g.
Bench Handling Test	Each edge lifted four inches and allowed to free fall onto a solid wooden bench surface.[a] Meets requirements of MIL-T-22800D, para 4.5.5.4.3.

[a] Performance Requirement not checked in manual.

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Table 1–3
Physical Characteristics

Characteristics	Performance Requirements
Weight	
With Power Cord, Cover, Probes, and Pouch	9.4 kg (20.7 lb).
With Power Cord Only	8.2 kg (18 lb).
Domestic Shipping Weight	12.2 kg (26.9 lb).
Dimensions	See Figure 1–2 for dimensional drawing.
Height	137 mm (5.4 in).
Width	
With Handle	360 mm (14.2 in).
Without Handle	328 mm (12.9 in).
Depth	
With Front Cover	445 mm (17.5 in).
Without Front Cover	440 mm (17.3 in).
With Handle Extended	511 mm (20.1 in).

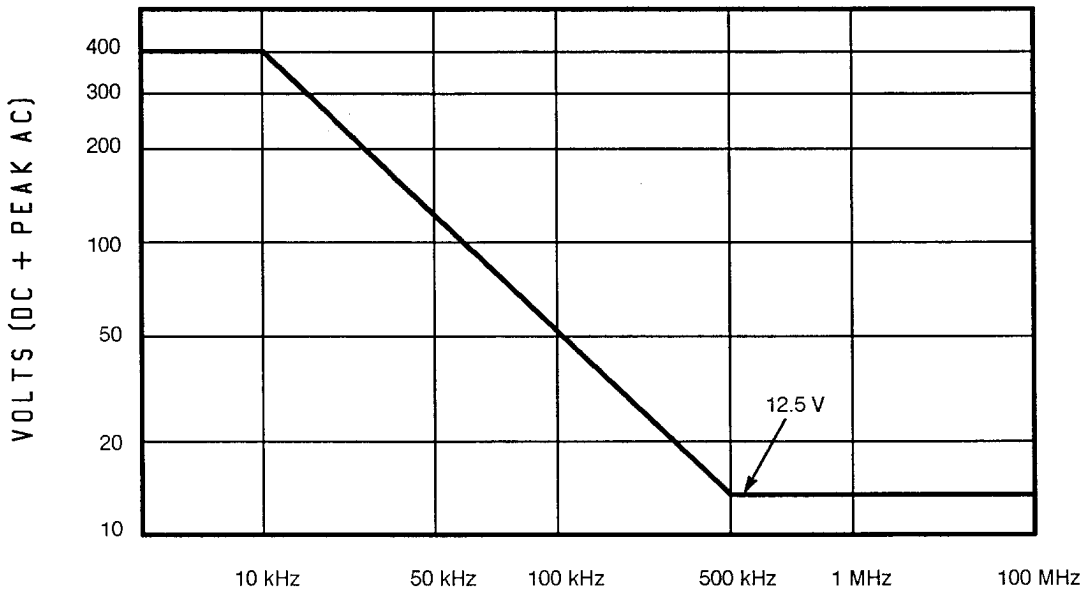


Figure 1–1. Maximum input voltage versus frequency derating curve for the CH 1 OR X, CH 2 OR Y, and EXT INPUT connectors.

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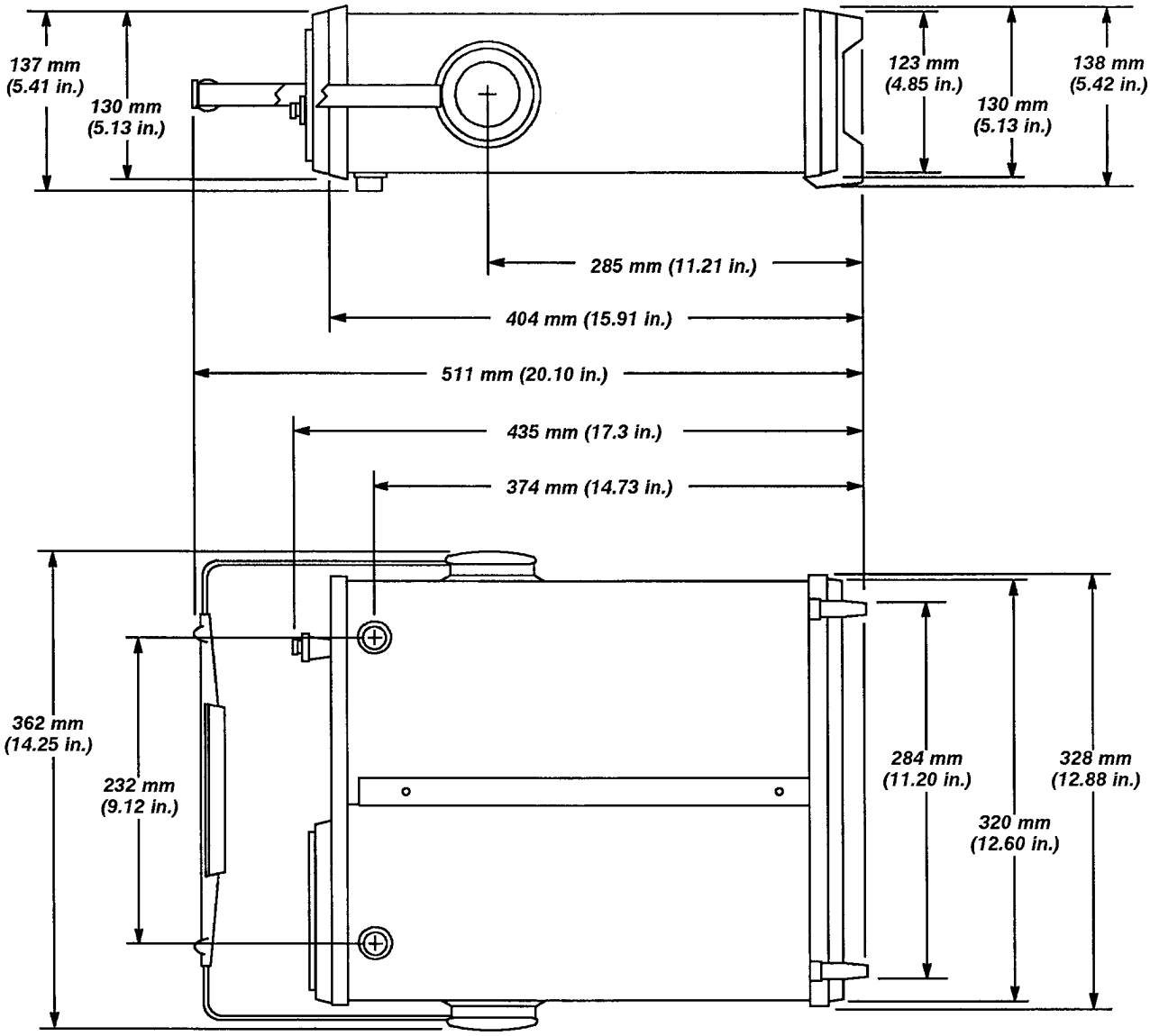


Figure 1–2: Physical dimensions of the 2232 Oscilloscope.

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OPERATING INFORMATION

SAFETY

This part of the manual tells how to prepare for and to proceed with the initial start-up of the instrument.

Refer to the Safety Summary at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read entirely both this section and the Safety Summary.

LINE VOLTAGE

This instrument is capable of continuous operation with input voltages that range from 90 V to 250 V with source voltage frequencies from 48 Hz to 440 Hz.

POWER CORD

A detachable three-wire power cord with a three-contact plug is provided with each instrument for connecting to both the power source and protective ground. The power cord may be secured to the rear panel by a cord-set-securing clamp (see Figure 2-1). The protective-ground contact in the plug connects (through the protective-ground conductor) to the accessible metal parts of the instrument. For electrical-shock protection, insert this plug only into a power-source outlet that has a properly grounded protective-ground contact.

Instruments are shipped with the power cord specified by the customer. Available power-cord information is presented in Figure 2-2, and part numbers are listed in Options and Accessories (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

LINE FUSE

The instrument fuse holder is located on the rear panel (see Figure 2-1) and contains the line-protection fuse. The following procedure may be used either to verify that the proper fuse is installed or to install a replacement fuse.

1. Unplug the power cord from the power-input source (if plugged in).
2. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.

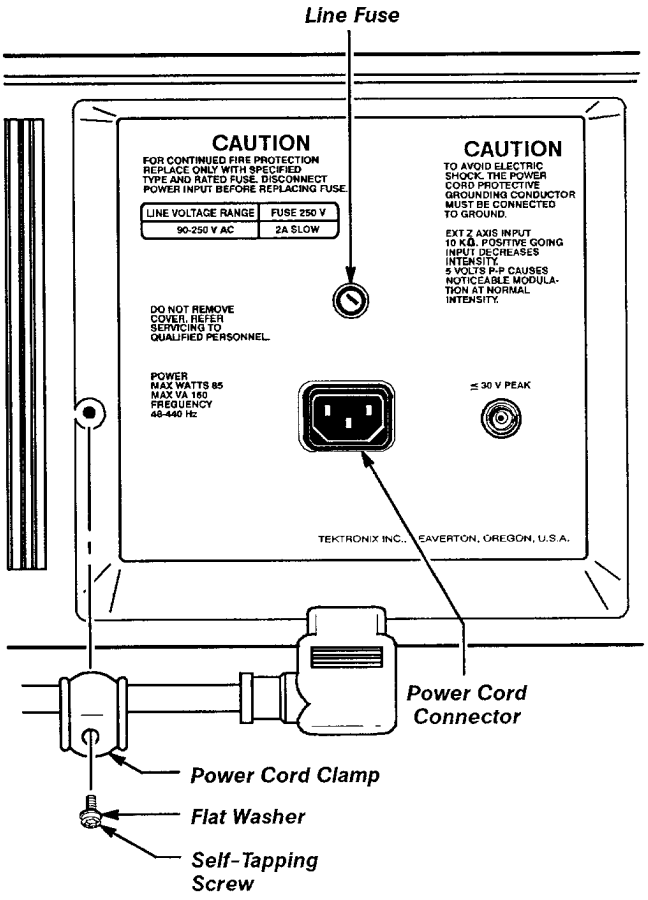
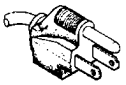
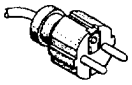
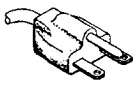
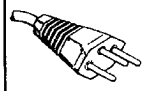


Figure 2-1. Securing the detachable power cord to the instrument.

3. Pull the cap (with the attached fuse inside) out of the fuse holder.
4. Verify that the proper fuse is installed (see the rear-panel fuse nomenclature).
5. Reinstall the proper fuse in the fuse cap and replace the cap and fuse in the fuse holder by pressing in and giving a slight clockwise rotation of the cap.

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Plug Configuration	Option	Power Cord/ Plug Type	Line Voltage	Reference Standards [b]
	U.S. Std.	U.S. 120V	120V	ANSI C73.11 NEMA 5-15-P IEC 83 UL 198.6
	A1	EURO 220V	220V	CEE(7), II, IV, VII IEC 83 IEC 127
	A2	UK [a] 240V	240V	BS 1363 IEC 83 IEC 127
	A3	Australian 240V	240V	AS C112 IEC 127
	A4	North American 240V	240V	ANSI C73.20 NEMA 6-15-P IEC 83 UL 198.6
	A5	Switzerland 220V	220V	SEV IEC 127

[a] A 6A, type C fuse is also installed inside the plug of the Option A2 power cord.

[b] Reference Standards Abbreviations:

ANSI—American National Standards Institute
AS—Standards Association of Australia
BS—British Standards Institution
CEE—International Commission on Rules for the Approval of Electrical Equipment
IEC—International Electrotechnical Commission
NEMA—National Electrical Manufacturer's Association
SEV—Schweizervischer Elektrotechnischer Verein
UL—Underwriters Laboratories Inc.

Figure 2-2. Optional power cords.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained at all times. Before turning on the power, first verify that both the fan-exhaust holes on the rear panel and the air-intake holes on the side panel are free from any obstructions to airflow. After turning on the instrument, verify that the fan is exhausting air.

START-UP

The instrument automatically performs power-up tests of the digital portion of the circuitry each time the instrument is turned on. The purpose of these tests is to provide the user with the highest possible confidence level that the instrument is fully functional. If no faults are encountered during the power-up testing, the instrument will enter the normal operating mode. If the instrument fails one of the power-up tests, the instrument attempts to indicate the cause of the failure.

If a failure of any power-up test occurs, the instrument may still be usable for some applications, depending on the nature of the failure. If the instrument functions for your immediate measurement requirement, it may be used, but refer it to a qualified service technician for repair of the problem at the earliest convenience. Consult your service department, your local Tektronix Service Center, or your nearest Tektronix representative if additional assistance is required.

REPACKAGING

If this instrument is shipped by commercial transportation, use the original packaging material. Unpack the instrument carefully from the shipping container to save the carton and packaging material for this purpose.

If the original packaging is unfit for use or is not available, repackage the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions and having a carton test strength of at least 275 pounds.

2. If the instrument is being shipped to a Tektronix Service Center for repair or calibration, attach a tag to the instrument showing the following: owner of the instrument (with address), the name of a person at your firm who may be contacted if additional information is needed, complete instrument type and serial number, and a description of the service required.

3. Wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of packing materials into the instrument.

4. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing for three inches of padding on each side (including top and bottom).

5. Seal the carton with shipping tape or with an industrial stapler.

6. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

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THEORY OF OPERATION

SECTION ORGANIZATION

This section contains a functional description of the 2232 Digital Storage Oscilloscope. The discussion begins with a summary of instrument functions. Following the general description, each major circuit is explained in detail. Functional block diagrams and schematic diagrams are used to show the interconnections between parts of the circuitry, to indicate circuit components, and to identify interrelationships with the front-panel controls.

Schematic diagrams and the overall block diagrams are located in the tabbed "Diagrams" section at the back of this manual. The schematic diagram associated with each description is identified in the text and indicated on the tab of the appropriate foldout page by a numbered diamond symbol. For best understanding of the circuit being described, refer to both the appropriate schematic diagram and the functional block diagram.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within the instrument. Functions and operation of the logic circuits are represented by logic symbology and terminology. Most logic functions are described using the positive-logic convention. Positive logic is a system where the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In this logic description, the TRUE state is HI, and the FALSE state is LO. The specific voltages which constitute a HI or a LO state vary between specific devices. For specific device characteristics, refer to the manufacturer's data book.

Linear Devices

The operation of individual linear integrated circuit devices is described in this section using waveforms or graphic techniques to illustrate their circuit action.

GENERAL DESCRIPTION

Introduction

In the following overall functional description of the instrument, refer to the basic block diagram, Figure 3-1, and to the detailed block diagrams located in the "Diagrams" section of this manual. Each major block in the diagram represents a major circuit within the instrument. In Figure 3-1, the numbered diamond symbol in each block indicates the schematic diagram number. Much of the analog portion of the oscilloscope operates without direction from the Microprocessor circuitry. These portions of the instrument are described first, with appropriate references to areas that either provide information to the Microprocessor or are controlled by the instrument's storage circuitry. The Microprocessor and Storage circuit descriptions follow the more conventional portions of the instrument's circuitry.

Vertical

Signals to be displayed on the crt (cathode-ray tube) are applied to either or both the CH 1 OR X and the CH 2 OR Y input connectors. The signals may be coupled to the attenuator either directly (DC) or through an input-coupling capacitor (AC). The inputs may also be disconnected, and the input to the attenuators grounded, by switching to the GND position of the input coupling switch. In the GND position, the ac-coupling capacitor is allowed to precharge to the dc level present at the input connector. This precharging prevents large trace shifts of the display when switching from GND to AC coupling. The Attenuators are switched by the front-panel VOLTS/DIV switches and scale the applied signal level to obtain the desired display amplitude. Information about the Input Coupling switch and the channel VOLTS/DIV switch positions is read by the Microprocessor. These signals control the STORE mode ground-reference acquisition and the crt readout displays of the Input Coupling and VOLTS/DIV switch settings of the active channel(s).

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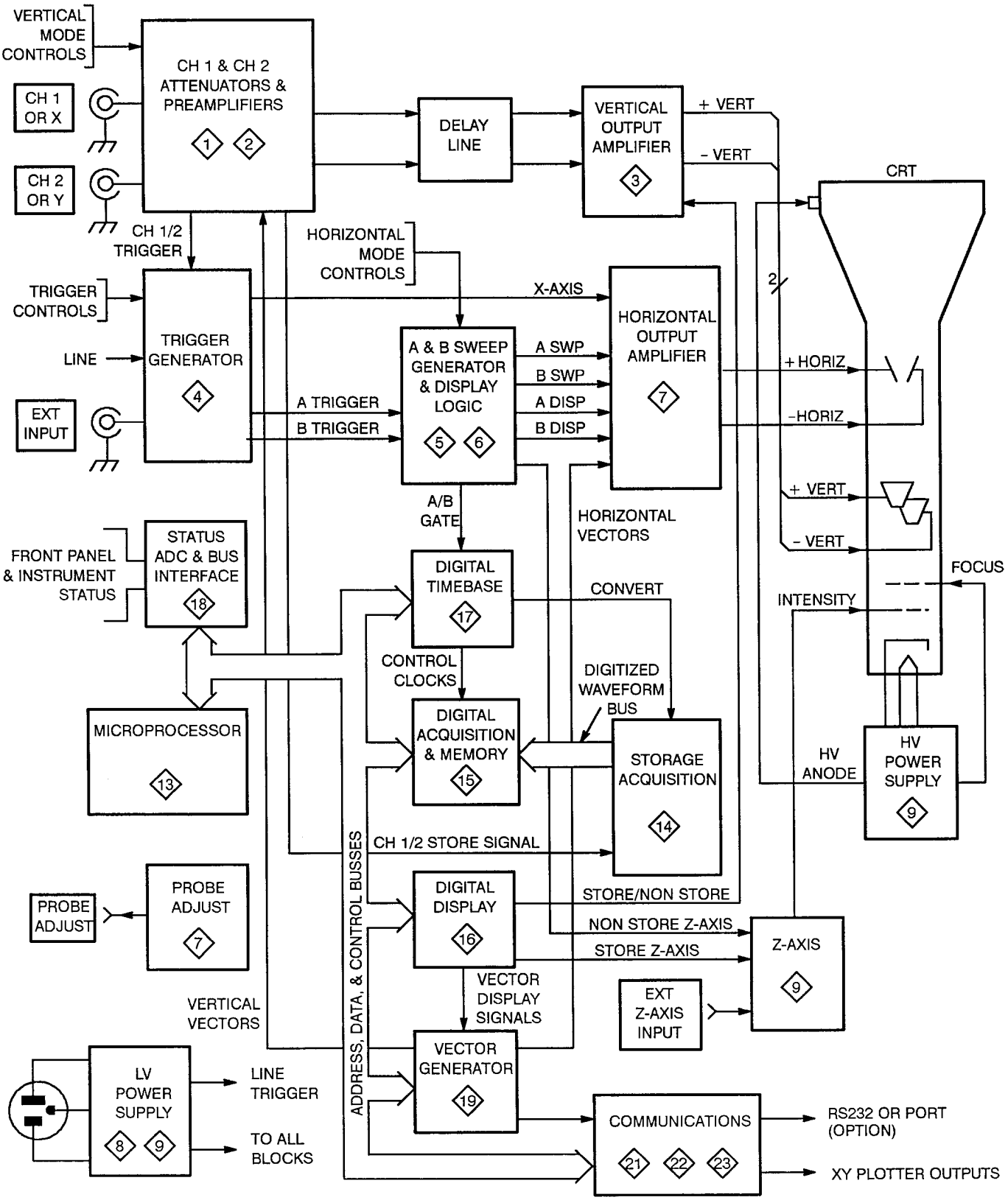


Figure 3–1. Simplified block diagram.

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Scaled output signals from the Attenuators are applied to the Vertical Preamplifiers for amplification. The Channel 2 Preamplifier has additional circuitry, permitting the operator to invert the Channel 2 display on the cathode-ray tube (crt). Each Vertical Preamplifier has a bandwidth limit circuit controlled by the BW LIMIT switch on the front panel. Either the full 100 MHz bandwidth or limited 20 MHz bandwidth may be selected. Trigger pickoffs in each channel supply a trigger signal to the Trigger Amplifier when internal triggering is selected. Other signal pickoffs provide vertical position information to the Position Signal Conditioning circuitry for vertically positioning the stored signal. The final stage of the Vertical Preamplifier for each channel provides one of two signals; either the vertical channel signal for the analog presentation on the crt or the vertical acquisition signal to be digitized by the storage circuitry.

Channel signals either for direct analog presentation on the crt or for application to the Storage digitizing circuitry are selected by the analog Channel Switch under control of the front-panel Vertical MODE switches. The switching signals from the Channel Switch Logic control a diode gate (Channel Switch) that selects the channel signal(s) to be applied to the Delay-line Driver. If ADD is selected, both channel signals are applied to the Delay-line Driver where the signals are summed together. The Delay-Line Driver provides the proper signal-driving level and impedance match to the Delay Line, where the vertical signal is delayed approximately 100 ns with respect to the trigger signal. The vertical signal delay allows time for the Horizontal circuitry to start the sweep before the vertical signal is applied to the crt.

Whenever STORE mode is selected, analog signals from the Storage circuitry are supplied to the Channel Switch circuit. Under control of the Channel Switch Logic, which is in turn switched by signals from the Display Controller, the analog display signal out of the final Vertical Preamplifier stage in each channel is biased off. The Channel 1 and Channel 2 Acquisition signals from the final preamplifiers are then biased on to pass the signals to be digitized to the Storage circuitry. At the same time, the Channel Switch (diode gate) is switched to pass the Storage vertical signal to the Delay Line Driver input.

Final amplification of the vertical signal (either STORE or NON-STORE) is done by the Vertical Output Amplifier. This stage produces the signal levels that vertically deflect the crt electron beam. This amplifier stage also contains the vertical trace separation circuitry that separates the NON-STORE A Intensified trace from the B Delayed trace when Alternate Horizontal display mode is selected. The amount of trace separation is controlled using the front panel A/B SWP SEP knob.

Triggering

The Triggering circuitry uses either the Internal Trigger signal obtained from the input signal(s), an External Trigger signal, or a Line Trigger signal derived from the ac-power-source to develop trigger signals for the Sweep Generator. The Auto Trigger circuit sets the range of the Trigger Level to conform approximately to the peak-to-peak amplitude of the selected trigger signal when either AUTO or TV FIELD A TRIGGER Mode is selected. In NORM mode, the TRIGGER LEVEL control must be adjusted to the signal level before a sweep will be triggered. ROLL mode (menu selected and used at the slower sweep speeds in STORE mode) overrides the triggering circuit functions; a continuous signal acquisition is made and the signal is displayed without the need of a trigger signal.

The triggering circuitry contains the TV Field Sync circuit. This circuit provides stable triggering on television vertical-sync pulses when in the TV Field triggering mode. TV Line triggering is possible using P-P AUTO trigger mode.

Signal pickoffs from the Internal Trigger circuitry provide the X-Axis signal for the nonstore X-Y display mode and the B trigger signal for triggered B Sweeps.

A Sweep

The A Sweep Generator and Logic circuits control the nonstore sweep generation and both the Store and the nonstore A Sweep timing. When the A TRIGGER Mode switches are set to either P-P AUTO or TV FIELD and no trigger signal is present, the Auto Baseline circuit causes the Sweep Logic circuit to produce a sweep for reference purposes. In the NORM setting, the Auto Baseline circuit is disabled and NON-STORE sweeps are not generated until a trigger event occurs. NORM trigger mode is used to obtain stable triggering on low-repetition rate signals that do not provide a trigger before an auto baseline is generated. SGL SWP (single sweep) trigger mode allows only one sweep to be generated after being reset and is used to obtain the waveform from a one-shot event.

ROLL and SCAN Storage modes are useful in capturing low-frequency and low-repetition rate waveforms. In SCAN mode, receiving a trigger causes the pretrigger portion of the waveform to update as a block. The post-trigger waveform updates from the trigger point to the right edge of the screen as new data is acquired. ROLL

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Storage acquisitions differ from the NON-STORE sweeps and SCAN Storage mode in that a trigger signal is not used for acquisition of the signal or displaying the waveform. The A Sweep Logic circuitry provides gating and holdoff signals used by the Storage circuitry to control its acquisition and display cycles for all storage modes, except ROLL.

The A_GATE(L) signal applied to the A Miller Sweep Generator circuit starts the Nonstore linear sweep with a ramp time that is controlled by the A SEC/DIV switch setting. Switch position pickoffs supply the SEC/DIV switch setting information to the Microprocessor for use in STORE mode horizontal timing. The A SEC/DIV switch setting is also displayed on the crt for both Store and Nonstore operation.

B Sweep

The Alternate B Sweep Circuitry controls the Nonstore BOTH and B Delayed Horizontal mode displays. This circuitry includes the B Miller Sweep Generator and B Sweep Logic circuitry. STORE mode B timing is controlled by the B SEC/DIV switch. BOTH Horizontal MODE is not available with STORE. In STORE mode, the BOTH selection displays an A Intensified Trace only. The intensified zone on the A trace indicates the position and approximate amount of the A trace that is displayed by the B Delayed Display.

Horizontal

NON-STORE A and B Sweep signals (or the X-Axis signal from the X-Y Amplifier in the NON-STORE X-Y Display mode) are applied to the Horizontal Preamplifier where one is selected and amplified. Gain in the Preamplifier is switchable between X1 and X10. The X10 gain is used for NON-STORE X10 Magnification. STORE mode X10 expansion is done digitally and reflected in the horizontal deflection signals supplied after the Horizontal Preamplifier. Horizontal positioning of both the STORE and the NON-STORE display is done by applying a horizontal position dc offset to the Horizontal Preamplifier. The amplified NON-STORE horizontal signal is applied to the Horizontal Mux circuit where it is available for selection.

STORE mode horizontal deflection signals are also applied to the Horizontal Mux. Selection of either the NON-STORE sweep signals or the STORE deflection signals is done by control signals from the Channel Switch Logic in the Vertical circuitry. The selected horizontal deflection signals are then amplified by the Horizontal Output Amplifier to the levels needed to drive the crt's horizontal deflection plates.

Microprocessor

The Microprocessor (MPU) controls the digital storage and display sections of the oscilloscope. Under firmware control (firmware is the programmed instructions contained in read-only memory), the Microprocessor monitors the operation of the instrument and sets up the circuitry to perform as dictated by the front-panel control settings. Data transfer to and from the Microprocessor and address selection of a device to be communicated with are done over a 20-line I/O bus. Eight of the lines (PAD0 through PAD7) form a combined address/data bus while the remaining 12 lines (A8 through A19) are for addressing only. Timing for the execution of instructions, addressing, and data transfers is provided by an external, crystal-controlled oscillator and divider that drives the Microprocessor clock generator.

Storage front-panel control settings are passed to the Microprocessor via eight-bit bus drivers. Settings of the analog front-panel controls and switches are also provided to the MPU, but via different bus drivers. The Status ADC and Bus Interface circuitry provides the interfaces from the analog front-panel controls to the data bus.

Status ADC and Bus Interface

Switch settings and status bits are applied directly to bus drivers. Each data bit then corresponds to a switch setting (either open or closed) or a status bit logic level (either HI or LO). Analog front-panel information is multiplexed to an analog-to-digital converter where it is converted to a digital value and applied to a bus driver. When the Microprocessor reads the bus, it obtains a data byte that represents the position value for a single control rather than the switch or status data bits of the digital-type information. The Microprocessor determines the control settings from the value of the data bytes or status bits received and sets up the digital storage circuits accordingly.

Storage Acquisition

Input signals to be digitized are selected by the Channel Switch. Either or both (for ADD) of the input signals picked off from the Vertical Preamplifier may be selected. The acquisition signal conditioning circuitry consists of A/D conversion modules, that provides gain control, offset control, level shifting, signal addition, and high frequency compensation. The analog-to-digital conversion modules acquire the conditioned analog

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input signal and perform the conversion functions required to provide an 8-bit digital representation of the input signal which is supplied to the digital acquisition memory system for digital signal processing.

Digital Acquisition and Memory

The digitized waveforms are applied to the digital acquisition memory system via the two data buses from the A/D conversion modules. The digital acquisition memory system consists of digital acquisition IC and eight 2-K by 8-bit random-access memory devices.

The digitized waveforms are clocked into the digital acquisition IC which demultiplexed the acquisition data and writes it into the acquisition IC at a rate determined by the A or B SEC/DIV switch setting. The digital acquisition IC contains several internal circuits that controls the way the digitized waveforms to be transferred to the acquisition memory. The acquisition data is controlled in part by the Microprocessor that select the channel or channels to be displayed and enables the XY mode.

When waveform data is to be read out of the Acquisition Memory, the digital acquisition IC is loaded with the address of the data for the waveform. The Microprocessor sequences through the addresses reading out the data bytes.

Digital Time Base

An accurate frequency source for synchronizing the Microprocessor with the other digital devices on the bus is provided by a 100 MHz oscillator. That frequency is divided down by the Clock Generator to produce the various clocking rates. The Time Base Mode Register latches control data bits from the Microprocessor data bus to set the operating mode of the time base. These control bits switch the Trigger Mux circuit to either A or B Trigger, enable the trigger logic circuit, switch the clock multiplexer to change the clock rate, start a storage acquisition, and enable interrupts to the Microprocessor. The programmable Time Base Divider, under control of the Microprocessor via the Time Base Divider Register, generates a sampling rate that corresponds to the front-panel SEC/DIV switch setting.

The Digital Time Base Trigger Logic circuit looks at whether the pretrigger data portion of the record has been filled. If the pretrigger portion is full, then the A or B Gate generates the trigger. When a trigger is generated in Repetitive Storage mode, the Clock Delay Timer measures the time delay between the arrival of the trigger and the 100 MHz clock. The time difference value is used by the Microprocessor to accurately position the acquired data with respect to the actual trigger point.

The delay difference between the start of the acquisition and the occurrence of the B trigger is also measured. This value is only used in BOTH Horizontal MODE when running the B Horizontal display in Triggerable After Delay to provide a readout of the time delay between the A Trigger and the B Trigger points.

Acquisition samples are counted to determine when a full record of data has been stored and to keep track of the beginning and ending memory locations of the record. The Record Counter in the Digital Acquisition IC is also programmable to provide for the different record lengths for one-channel or two-channel acquisitions, different Pretrigger selections, and either 4K-byte or 1K-byte record length.

Digital Display

A custom IC handles the digital display generation. The Display Controller functions as an interface between the processor bus, display memory (RAM), and vector generators to form waveform and character displays on the crt. The controller reads a display list from the Display Memory and drives X- and Y-Vector Generators to create the waveform and readout displays. Z-Axis control signals are also generated to drive the crt Z-Axis Amplifier for Stored waveform and Readout intensity control. Control signals to the Microprocessor and Display Memory are generated in response to a processor read/write request.

Digital-to-analog converters take the digital data bytes supplied from the Display Memory via the Display Controller and change them to the X- and Y-Axis analog signals that drive the Horizontal and Vertical Vector Generators. The vector signals are applied to the Horizontal and Vertical Output Amplifiers to produce the STORE mode deflection signals and NON-STORE mode character readout.

The Display Memory is two 32-K X 8-bit static random access memories (SRAM). One RAM provides the 8-bit waveform bytes of the stored waveform, and the other RAM stores attribute bits that are used to define the waveform point intensity and mark the end of the record. Data is either stored or read out, as the operation in progress requires.

Vector Generator

X- and Y-Axis analog signals from the Digital Display are converted by the Vector Generators into the vector

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signals used to drive the crt deflection plates. Vector signals are produced for the stored waveforms, the menu displays, and the readouts. The Vector Generator is switched to the dot-display mode for equivalent-time sampling waveforms and X-Y displays.

The X-Y Plotter driver circuit is included in this portion of the circuitry. When the X-Y Plotter is enabled, x-axis and y-axis signals are switched via the plot multiplexer to the x-axis and y-axis plot amplifiers. The VECT_SMPL(L) signal is switched via the same multiplexer to drive the Pen-Down amplifier.

Z-Axis

The Z-Axis Amplifier has input signals from multiple sources that control the crt intensity on a time-shared basis. NON-STORE intensity signals are the level inputs from the A and B INTENSITY controls that are controlled by the Alternate Display switching and B Z-Axis Logic circuits. Additional Z-Axis drive current is supplied during the intensified portion of an A trace during the B Sweep when BOTH Horizontal display mode is selected. The remaining nonstore signals that have control of the display brightness are the EXT Z-AXIS INPUT signal, the CHOP mode blanking signal, and the XY(L) control signal. All of these sources are added to provide the time-shared nonstore displays.

For the Store waveform and the Menu and Readout character displays, an additional Z-Axis drive signal from the STORAGE/READOUT INTENSITY control is switched on and off by the Display Controller. The controller signals determine when the stored waveforms and the readout characters are turned on and if any portions of the display will be intensified more than the rest. Further amplification of the combined signal sources provides the amplitude levels required to drive the crt.

The Z-Axis signal is applied to the crt DC Restorer circuit where it is shifted to the large negative potential used by the crt. The potential controls the amount of current supplied by the electron beam to the crt phosphors.

Power Supply

Operating potentials for the instrument are obtained from a power supply that consists of the Preregulator, Inverter and Transformer, and Rectifiers and Filters. Approximately +42 V is supplied by the Preregulator to drive the 20 kHz Inverter stage through the Transformer primary windings. The transformer secondary windings produce the various ac levels that are rectified and filtered to provide the supply voltages for the instrument's circuitry. A High Voltage Multiplier circuit produces the accelerating, focus, and cathode potentials used by the crt.

Probe Adjust

A front-panel PRB ADJ output is provided for use in adjusting probe compensation. The voltage at the PRB ADJ connector is a negative-going square wave that has a peak-to-peak amplitude of approximately 0.5 V with a repetition rate of approximately 1 kHz.

Communications Options

Options for this instrument provide a choice of either an IEEE-488 GPIB (General Purpose Interface Bus) or an RS-232-C serial output port. The options allow the transfer of stored waveforms and the control of certain instrument functions.

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DETAILED CIRCUIT DESCRIPTION

INTRODUCTION

The detailed circuit description of the 2232 first describes the analog operating portion of the oscilloscope followed by the digital portion. During the description of the analog circuitry, references are made to circuitry that either provides information to the microprocessor or is controlled by the instrument's storage circuitry.

The instrument has full conventional oscilloscope capabilities with all the associated analog circuitry. Signal pickoff points and signal insertion points connect the analog portion of the instrument to the digital operating system to acquire and display the stored waveforms. The digital circuitry enhances the analog display by providing crt readouts of the VOLTS/DIV, SEC/DIV, and Delay Time Position control settings.

VERTICAL ATTENUATORS

The Channel 1 and Channel 2 Attenuators circuitry, shown on Diagram 1, are identical with the exception of the additional Invert circuitry in the Channel 2 Paraphase Amplifier. Therefore, only the Channel 1 Attenuator is described, with the Invert circuitry of Channel 2 discussed separately.

The Attenuator circuit and switches (see Figure 3–2) provide control of the input coupling, the vertical deflection factor, and the variable volts/division gain. Vertical input signals for display on the crt or for acquisition by the storage circuitry may be connected to either or both the CH 1 OR X and the CH 2 OR Y input connectors. In the X-Y mode of operation, the signal applied to the CH 1 OR X connector provides horizontal (X-axis) deflection for the display, and the signal applied to the CH 2 OR Y connector provides the vertical (Y-axis) deflection for the display.

Switch contacts on the A14 CH 1 Logic board are read by the microprocessor to determine the CH 1 VOLTS/DIV switch and Input Coupling switch settings. A switch contact associated with CH 1 CAL (Variable VOLTS/DIV) control, R43, is also read to see whether that control is in or out of the calibrated (CAL) detent.

Input Coupling (AC–GND–DC Switch)

A signal from the CH 1 OR X input connector may be ac or dc coupled to the High-Impedance Attenuator circuit or disconnected completely by the Input Coupling Switch. Signals from the CH 1 OR X input connector are routed through resistor R1 to Input Coupling Switch, S1. When S1 is set for dc coupling, the Channel 1 signal goes directly to the input of the High-Impedance Attenuator stage. When ac coupled, the input signal must go through dc-blocking capacitor, C2. The blocking capacitor stops the dc component of the input signal from reaching the Attenuator circuit. When switched into the signal path, attenuators AT1 and AT2 attenuate the input signal by factors of 100 and 10 respectively. When S1 is set to GND, the input of the Buffer Amplifier is connected to ground through R8. This provides a ground reference for the analog display and the microprocessor without removing the applied signal from the input connector. The coupling capacitor precharges through R2, R4, and R8 to prevent large trace shifts when switching from GND to AC.

A probe coding ring on the CH 1 OR X input connector is used to read the attenuation factor of the attached probe to automatically adjust the VOLTS/DIV scale factors in the readout. The default setting is for X1 attenuation when either coaxial cables or uncoded probes are connected to the vertical inputs.

Buffer Amplifier and Low-Impedance Attenuator

The Buffer Amplifier presents a high-impedance, low-capacitance load to the signal from the High-Impedance Attenuator and a low output impedance to the Low-Impedance Attenuator. The dual-path buffer amplifier (slow path and fast path) combines dc stability with high-speed performance.

The input signal connects to the gate of source-follower Q13 through R6 and C6 (the fast path) and to the inverting input of operational amplifier U10 from the resistive voltage divider formed by R3 and R5 (the slow path). Source-follower Q13 and emitter-follower Q18 have high-impedance inputs that isolate the applied signal from the loading effects of the Low-Impedance Attenuator. A voltage divider formed by R46, R47, and R48 at the emitter output of Q18 applies feedback to the noninverting input of slow-path amplifier U10. The two input voltages to amplifier U10 are compared, and the conductivity of current-source transistor Q15 is changed to correct for any frequency-gain error at the source of Q13. The bandwidth of U10 is limited by capacitor C10 so that the slow path responds only to frequencies below 100 kHz. Input offset voltage compensation for U10, provided by R10, eliminates trace shift between VOLTS/DIV

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switch settings. Gain in both paths is matched by adjusting MF/LF Gain Bal potentiometer R47. The path gains then remain matched by the corrective action of U10 and Q15 if gain differences in the two paths start to develop.

Low-Impedance Attenuator R19 divides down the Buffer Amplifier output signal for application to Paraphase Amplifier U30. The attenuator's output impedance is 75 ohms at all VOLTS/DIV switch settings. The VOLTS/DIV switch (S10) determines whether the Paraphase Amplifier receives a signal attenuated by a factor of 1 (no attenuation), 2, 4, or 10.

Paraphase Amplifier

Paraphase Amplifier U30 converts the single-ended signal from the Low-Impedance Attenuator into a differential signal for the Vertical Preamplifier. Included in the circuitry is switching that provides additional gain for the 2 mV position of the VOLTS/DIV switch, adjustments for amplifier dc balance, and circuitry for the Variable VOLTS/DIV function. Additionally, Channel 2 Paraphase Amplifier U80 contains circuitry to invert the Channel 2 display.

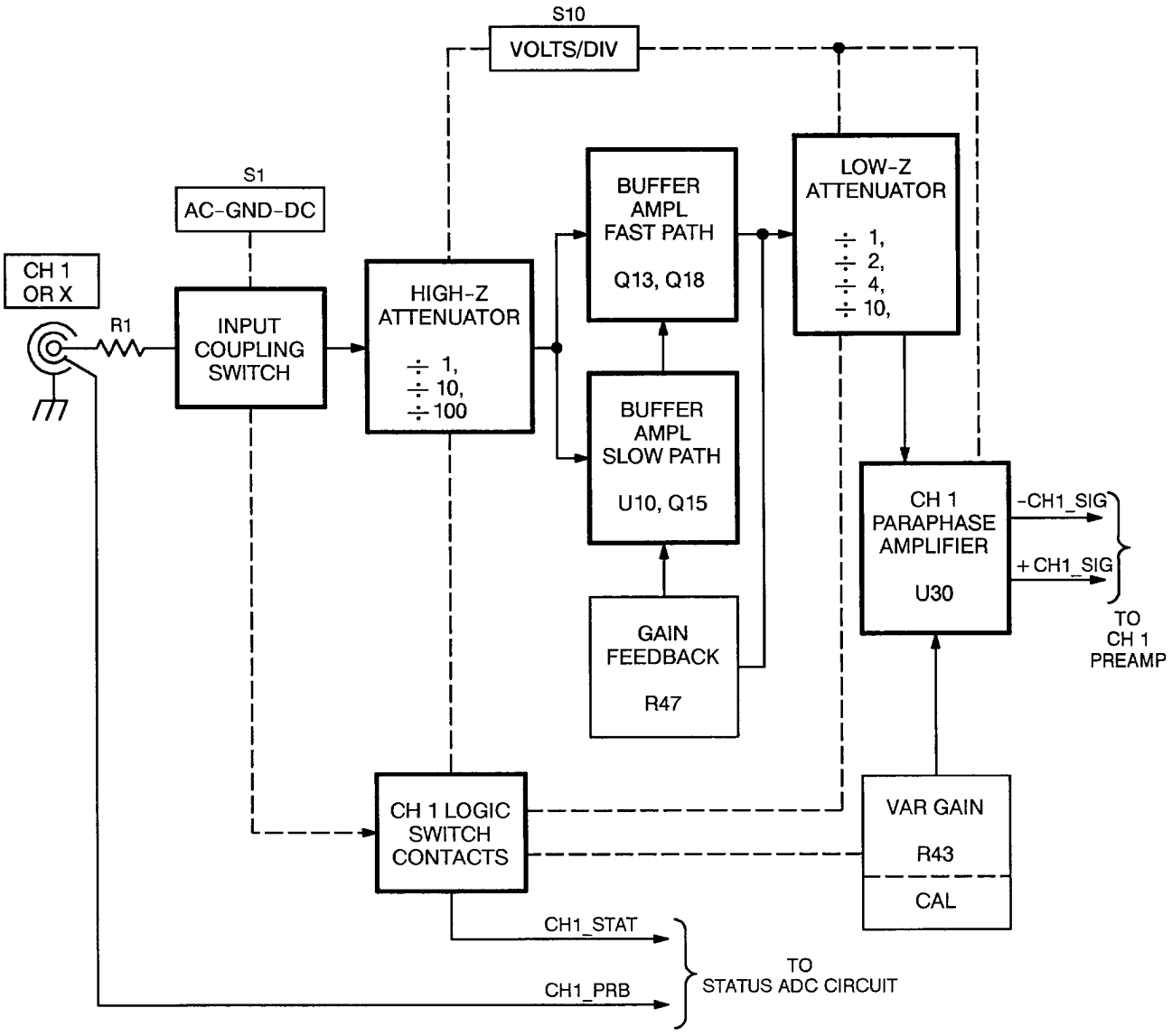


Figure 3-2. Block diagram of the Channel 1 Attenuator circuit.

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The signal from the Low-Impedance Attenuator goes to the base of one transistor in U30. The other input transistor is biased by the divider network formed by R30, R31, and R33 to a level that produces a null between the outputs of U30 (no trace shift on the crt screen) when the VOLTS/DIV control is switched between 5 mV and 2 mV. Emitter current for the two input transistors is supplied by R21, R22, R23, and VAR BAL potentiometer R25. Resistor R29 is the gain-setting resistor between the two emitters. High-frequency compensation of the amplifier is provided by the series combination of R27 and C27 shunting R29. In the 2 mV position, amplifier gain is increased because contact 15 of S10 is closed to place 2 mV Gain potentiometer R26 and compensating capacitor C26 in parallel with R29.

The collector current from the two input transistors in U30 serves as emitter current for the two differential output transistor pairs. Base-bias voltages for the two output pairs are developed by the divider network formed by R39, R41, R42, and Variable VOLTS/DIV potentiometer R43. The transistors of U30 have matched characteristics, so the ratio of currents in the two IC diodes connected to pin 11 determines the current ratios in the output transistor pairs. As Variable VOLTS/DIV potentiometer R43 is rotated from calibrated to uncalibrated, the conduction level of the transistors connected to R35 increases. Since the transistor pairs are cross-connected, the increased conduction in one pair subtracts from the output current produced by the transistor pair connected to R38, and the overall gain of the amplifier decreases. VAR BAL potentiometer R25 is adjusted to balance the amplifier for minimal dc trace shift as the Variable VOLTS/DIV control is rotated.

Incorporated in the Channel 2 Paraphase Amplifier is circuitry that allows the user to invert the polarity of the Channel 2 signal. When INVERT switch S90 is out, the transistor pairs in U80 are biased as they are in U30, and CH 2 trace is not inverted. When S90 is in, connections to the bases of the output transistor pairs are reversed, reversing the polarity of the output signal to produce an inverted Channel 2 trace and Channel 2 storage acquisition signal. The inverted/noninverted state is read by the microprocessor, and an indicator (↓) is displayed in the crt readout adjacent to the CH 2 VOLTS/DIV readout to indicate to the user when INVERT is in effect. Invert Bal potentiometer R75 is adjusted for minimal dc trace shift when the INVERT button is switched between the In and Out positions.

VERTICAL PREAMPLIFIERS

The Channel 1 and Channel 2 Vertical Preamplifiers, shown on Diagram 2, are identical in operation. Operation of the Channel 1 amplifier is described. Differential signal current from the Paraphase Amplifier is amplified to produce drive current to the Delay Line Driver and supply the Channel 1 signal to the Storage Acquisition circuitry. Internal trigger signals for the Trigger circuitry are picked off prior to the Vertical Preamplifier. The Channel Switch circuitry controls channel selection for the NON-STORE crt display. STORE mode signal acquisition and display, and the selection of either STORE or NON-STORE, is controlled by the Display Controller circuitry (Diagram 16).

Common-base transistors Q102 and Q103, which complete the Paraphase Amplifier portion of the circuitry shown on Diagram 1, convert differential current from the Paraphase Amplifier into level-shifted voltages that drive the bases of the input transistors of Vertical Preamplifier U130. Differential internal trigger signals are picked off at this point from the collector signals of Q102 and Q103 before Vertical POSITION dc offset is added to the input signals.

The collector current of each input transistor of U130 is the emitter current for two of the differential output transistors. One of the collectors of each output pair supplies one side of the differential Non-store signal to the Delay Line Driver, and the other collector in each pair supplies one side of the differential Channel signal to the Storage Acquisition circuitry. The base bias voltages of the output transistors are controlled by the Channel Switch Logic circuitry. The switching circuitry determines which channel is active (CH 1, CH 2 or both for ADD) in NON-STORE, and which channel supplies the Storage Acquisition signal in STORE.

Bandwidth Limit

BW LIMIT switch, S226A (Diagram 3), C117, C118, and the diode bridge formed by CR116, CR117, CR118 and CR119 reduce the bandwidth of the amplifier when desired. With full 100 MHz bandwidth, R116 is grounded through BW LIMIT switch S226A, and the nonconducting diode bridge isolates C117 and C118 from the vertical signal. With bandwidth limit on, R116 is connected to the +8.6 V supply, and the diode bridge is forward biased. The two bandwidth limiting capacitors are then in the vertical signal path, and high-frequency signals above 20 MHz are attenuated.

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S226B (Diagram 12), the other half of the bandwidth limit switch, is scanned by the microprocessor, and when the bandwidth limit is selected, it tells the display system to put the BWL symbol on the screen.

Vertical POSITION control R112 adds an offset voltage to the pair of differential transistors, Q114 and Q115, that supply the emitter current to the Preamplifier input transistors. Unequal collector currents from Q114 and Q115 go to the input transistors to introduce the vertical position offset to the Channel 1 Non-store signal. Output signals from Q114 and Q115 are applied to a Storage Vertical Position conditioning circuit where dc offset adjustments provide tracking corrections between the vertical positions of the Non-store and the Store signals.

When Channel 1 is selected to drive the Delay Line Driver, the Q output (pin 5) of U540A is HI. That HI is switched through U7201 to the bases of the Non-store signal transistors (connected to pin 14 of U130). These transistors are then forward-biased, and the Channel 1 signal is conducted to the Channel Switch circuit. If Channel 1 is not selected, then the Q output of U540A is LO, and the Non-store signal transistors are reverse-biased to prevent the Channel 1 Non-store signal from being displayed. The gain of the Preamplifier is set by adjusting R145 to control the signal current that is shunted between the two differential outputs. Amplifier gain is reduced by the current shunted between the two halves of the Preamplifier.

Channel Switch Logic

The Channel Switch Logic circuitry, shown on Diagram 2, utilizes the front-panel VERTICAL MODE and STORE/NON-STORE mode switches to select the crt display format. See Figure 3-3 for a block diagram of the circuit.

When any display mode other than X-Y is selected, the XY line connected to S550 is at ground potential. VERTICAL MODE switches S545 and S550 control the connection between the XY control line and the Set and Reset inputs of flip-flop U540A for the NON-STORE display formats.

CHANNEL 1 DISPLAY ONLY. The CH 1 position of S550 grounds the Set input (pin 4) of U540A while the Reset input (pin 1) is held HI by pull-up resistor R539. This produces a HI and a LO on the Q and $\overline{Q}$ outputs of U540A respectively. The levels are selected by multiplexer U7201, biasing on the Channel 1 Non-store output transistors in U130, allowing the Channel 1 input signal to drive the Delay Line Driver. The Channel 2 Preamplifier Non-store output transistors in U180 are biased off.

CHANNEL 2 DISPLAY ONLY. The CH 2 position of S550 holds the Reset input of U540A LO through CR538, and the Set input is held HI by pull-up resistor R538. The outputs of U540A are then Q LO and $\overline{Q}$ HI biasing on the Channel 2 Preamplifier Non-store output transistors (in U180) and biasing off the Channel 1 Preamplifier Non-store output transistors (in U130). Channel 2 then supplies the signal to drive the Delay Line Driver.

To display the ADD, ALT, or CHOP formats, S550 must be in the BOTH position to ground the A, C, and F pins of S545.

ADD DISPLAY. In the ADD position of S545, both the Set and Reset inputs of U540A are held LO by CR534 and CR537. The Q and $\overline{Q}$ outputs of U540A are then both HI, and signal currents from the Channel 1 and Channel 2 Preamplifiers add together to drive the Delay Line Driver.

CHOP DISPLAY. In the CHOP position, the CHOP(L) line is held LO, keeping the Q output of flip-flop U540B HI. This enables CHOP multivibrator U537D to begin switching. The switching rate is determined primarily by the component values of R544, R545, and C545. The output of U537C (the inverted output of the multivibrator circuit) drives U537A and supplies the CHOP clock to flip-flop U540A. The output of U537C also drives U537B, the CHOP Blanking Pulse Generator (see Diagram 9).

Coupling capacitor C547 and resistors R547 and R548 on pin 5 of U537B (see Diagram 9) form a differentiating circuit that produces short duration pulses during the switching of U540A. These pulses are inverted by U537B to generate the Chop Blank signal to the Z-Axis Amplifier. The pulses blank the crt during CHOP switching times.

The ALT_SYNC signal on pin 2 of U537A (see Diagram 2) is HI except during hold off. While pin 2 is HI, the output of U537C is inverted and passed by U537A to the clock input (pin 3) of U540A. Since the $\overline{Q}$ output of U540A is connected back to the D input, and both the Set and Reset inputs are HI, the outputs of U540A switch (change states) with each clock input. The Delay Line Driver is then supplied alternately from the Channel 1 and Channel 2 Preamplifiers at the CHOP rate.

ALTERNATE DISPLAY. In ALT, the CHOP(L) line is held HI, disabling CHOP multivibrator U537D. The output of U537C, the chop blanking signal, is HI. Input signals to U537A are the HI from U537C and ALT_SYNC from the Hold-Off circuitry in the A Sweep Generator. The output of U537A is then the inverted ALT_SYNC signal that clocks Channel Select flip-flop U540A. The ALT_SYNC(L) clock toggles the outputs of U540A at the end of each sweep so that the Channel 1 and Channel 2 Preamplifiers alternately drive the Delay Line Driver.

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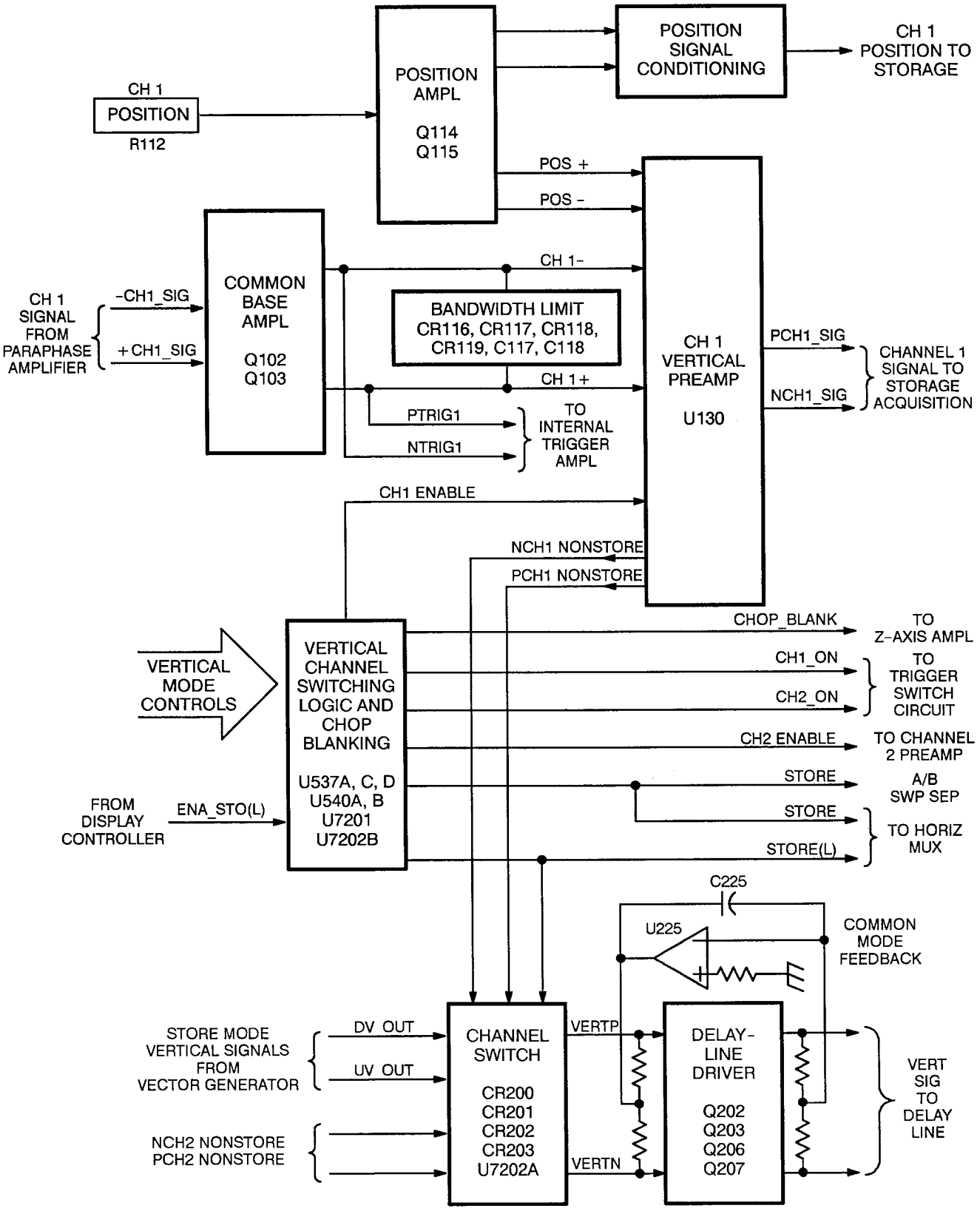


Figure 3–3. Store/Non-Store Vertical Switching.

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STORE MODE DISPLAYS. Under direction from the Display Controller, multiplexer U7201 selects either non-store or store signals to drive the Delay Line Driver. In NON-STORE, the multiplexer switches the Q and $\overline{Q}$ outputs of U540A to the Channel Switch to allow the switching sequences just described. However, when STORE is selected, the non-store analog signal to the Channel Switch is turned off, and the store vertical deflection analog signals are applied to the Delay Line Driver input. The store waveform display is determined by the Display Controller (Diagram 16).

The non-store output transistors are biased off by setting pins 9 and 12 of U7201 LO. The forward bias is removed, and the non-store path is disabled. Pin 7 of U7201 is switched LO in STORE mode. Inverter U7202B inverts the LO, supplying forward bias to the store output transistors in both Preamplifiers. Selection of either channel signal for digitizing is done by a channel switch IC in the Storage Acquisition circuit (Diagram 14).

The STORE signal from U7202B also goes to the Sweep Sep circuit to disable that circuit during STORE mode and to the Horizontal MUX circuit (Diagram 7) to block the non-store sweep signals from going to the Horizontal Output Amplifier. To complete the switching to STORE mode, Pin 7 of U7201 is switched HI and applied to Inverter U7202B. The LO output signal from U7202B (STORE) is applied to the Vertical Channel Switch circuit to pass the STORE mode vertical deflection signal to the Delay Line Driver. That same LO signal also goes to the Horizontal Mux to pass the STORE mode horizontal deflection signal to the Horizontal Output Amplifier.

A Z-Axis disabling signal DIS_Z(L) applied to NAND-gate U537B (see Diagram 9) disables the Chop Blanking circuitry for STORE mode displays. DIS_Z(L) holds the output of the Chop Blanking circuit HI to block the non-store Z-axis signals from the Z-Axis Amplifier.

VERTICAL OUTPUT AMPLIFIER

Vertical Output Amplifier circuitry, shown on Diagram 3, amplifies the vertical signal and drives the crt deflection plates. The Delay Line Driver converts the signal into a signal voltage to drive the Delay Line. Delay Line DL9210 delays the vertical signal so that the leading edge of the triggering signal can be viewed. The Vertical Output Amplifier drives the vertical deflection plates of the crt. The A/B Sweep Separation circuit vertically positions the Non-store B trace with respect to the Non-store A trace in BOTH Horizontal mode displays.

Delay Line Driver

The Delay Line Driver converts the signal current from the Vertical Preamplifiers or the STORE mode Vector Generator circuitry into a signal voltage to drive the Delay Line. Transistors Q202, Q203, Q206, and Q207 form a differential shunt feedback amplifier with the gain controlled by feedback resistors R216 and R217. Amplifier compensation is provided by C210 and R210, and output common-mode dc stabilization is provided by U225. Should the dc voltage at the junction of R222 and R223 move off zero, U225 changes the base current supplied to Q202 and Q203 through R202 and R203 to return the output of the Delay Line Driver to an average dc voltage of zero.

Delay Line DL9210 adds about 90 ns of delay to the vertical signal. In that time, the Sweep Generator has sufficient time to start producing a sweep before the vertical signal that triggered the sweep reaches the crt. This permits viewing the leading edge of the triggering signal.

Vertical Output Amplifier

The Vertical Output Amplifier drives the vertical deflection plates of the crt. Signals from the Delay Line go to a differential amplifier formed by Q230 and Q231 with low- and high-frequency compensation provided by the RC networks between the emitters. Thermal compensation is provided by thermistor RT236, and overall circuit gain is set by R233. The output stage of the Amplifier is two totem-pole transistor pairs, Q254-Q256 and Q255-Q257, that convert the collector currents of Q230 and Q231 to proportional output voltages. Resistors R256, R258, R257, and R259 are feedback elements and bias voltage dividers. Biasing is set so each transistor in a pair develops one-half the final output voltage on a side. The amplifier output signals drive the vertical crt deflection plates.

Beam Find is used to keep the vertical trace within the graticule area for locating off-screen and over-scanned traces. When the front-panel BEAM FIND switch opens the contacts of S390 (found on Diagram 9), the direct -8.6 V supply to R261 is removed, and emitter current goes through R261 and R262 in series. The added series resistance reduces the amount of available emitter current and limits the amplifier's dynamic range. In normal amplifier operation, S390 connects the -8.6 V supply directly to R261, and full emitter current is possible in the output transistors.

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A/B Sweep Separation Circuit

The circuit formed by Q283, Q284, Q285, and associated components acts to vertically position the Non-store B trace with respect to the Non-store A trace in BOTH Horizontal mode. In the B Sweep interval, the SEP(L) signal from the Alternate Display Switching circuit (Diagram 6) is LO, and Q283 is biased off. This puts A/B SWP SEP potentiometer R280 in the circuit where it can affect the bias level on one side of the differential current source formed by Q284 and Q285. Changing the bias adds a dc offset current to the Vertical Output Amplifier that moves the B trace vertically with respect to the A trace.

During the Non-store A sweep interval, the SEP(L) signal is HI, and Q283 is turned on to isolate potentiometer R280 from the biasing circuit of Q284. The base voltages of Q284 and Q285 are then equal. With the same bias to both sides of the Vertical Output Amplifier, no offset is added to the A trace. In STORE mode, the HI STORE signal placed on the base of Q282 keeps Q283 off, and the A/B Sweep Sep circuit on.

TRIGGERING

The Trigger Amplifiers, shown on Diagram 4, provide trigger signals to the Sweep Generators from the Vertical Preamplifiers, the EXT INPUT connector, or the power line. The A&B SOURCE switch selects Channel 1, Channel 2, or an external trigger as the trigger source. Also, the A COUPL switch can select the power line signal as the A trigger source. See Figure 3-4 for the block diagram of the trigger amplifiers and switching circuitry.

Internal Trigger Pickoff

Signals from the Vertical Preamplifiers drive the CH1 and CH2 Internal Trigger Amplifiers with channel selection determined by the VERTICAL and HORIZONTAL MODE switches. Trigger signal pickoff from Channel 1 is done by Q302 and Q303. Q327 and Q328 pick off the Channel 2 internal trigger signal. The circuitry associated with Channel 2 is the same as that for Channel 1 except for a trigger offset adjustment. Channel 1 trigger signal circuitry is described; equivalent components in Channel 2 perform identically.

Differential vertical signals from the Channel 1 Preamplifier go to Q302 and Q303. These emitter-follower transistors each drive one input transistor in trigger preamplifier IC U310. The collectors of the U310 input transistors in turn supply emitter current to a pair of two current-steering transistors. A compensation and biasing network is connected between the emitters of the input transistors. Trigger Offset potentiometer R309 in the emitter circuit adjusts the bias levels of the two input transistors of U310 to match the dc offsets of the Channel 1 and Channel 2 Trigger Amplifiers.

One transistor in each side of the output differential amplifier pairs of U310 has its base bias set to a fixed level by the divider network formed by R321 and R322. The bias voltage of the other transistor in each pair is controlled by the CH1_TRIG(L) signal from the Trigger Switch circuitry. When the CH1_TRIG(L) signal is HI, the transistors in each output pair with the collectors connected together (pin 6 and pin 14) are biased on, and the other transistors in the output pairs are off. The collector signal currents of the conducting transistors are equal in amount but of opposing polarity, so the signal is canceled. When the CH1_TRIG(L) signal is LO, the other transistors in each pair are biased on, and a differential signal is developed across output load resistors R314 and R315 to drive the Internal Trigger Amplifier.

Internal Trigger Amplifier

The Internal Trigger Amplifier converts the differential trigger signals from the Vertical Preamplifiers into a single-ended signal that drives the X-Axis Amplifier and the A and B Trigger Level Comparators.

Differential signal current is applied to the emitters of U350D and U350E. The collector current of U350D is changed to a voltage signal and inverted by U350C. The opposite-phase collector current of U350E produces a voltage drop across R359 which is in phase with and adds to the voltage across R360 at the collector of U350C. The summed voltages appear at the base of U350A. Feedback resistor R357 provides thermal bias stabilization for U350C.

Emitter-follower U350A buffers the signal and shifts the dc level back to 0 V. The emitter output signal of U350A drives the X-Axis Amplifier, the B Trigger Level Comparator, and the base of emitter-follower U350B. The emitter signal of U350B in turn supplies the A Internal Trigger signal. The circuit arrangement of U350A and U350B, with the common collector current path through R363, produces thermal bias stabilization of the two transistors.

Trigger Switching Logic

CH 1, CH 2, A EXT, or VERT MODE Internal Trigger signals may be selected by A & B SOURCE switch S555. The A Internal Trigger Signal from the emitter of U350B is passed to the A Trigger Level Comparator through forward-biased diode CR372 and Q401.

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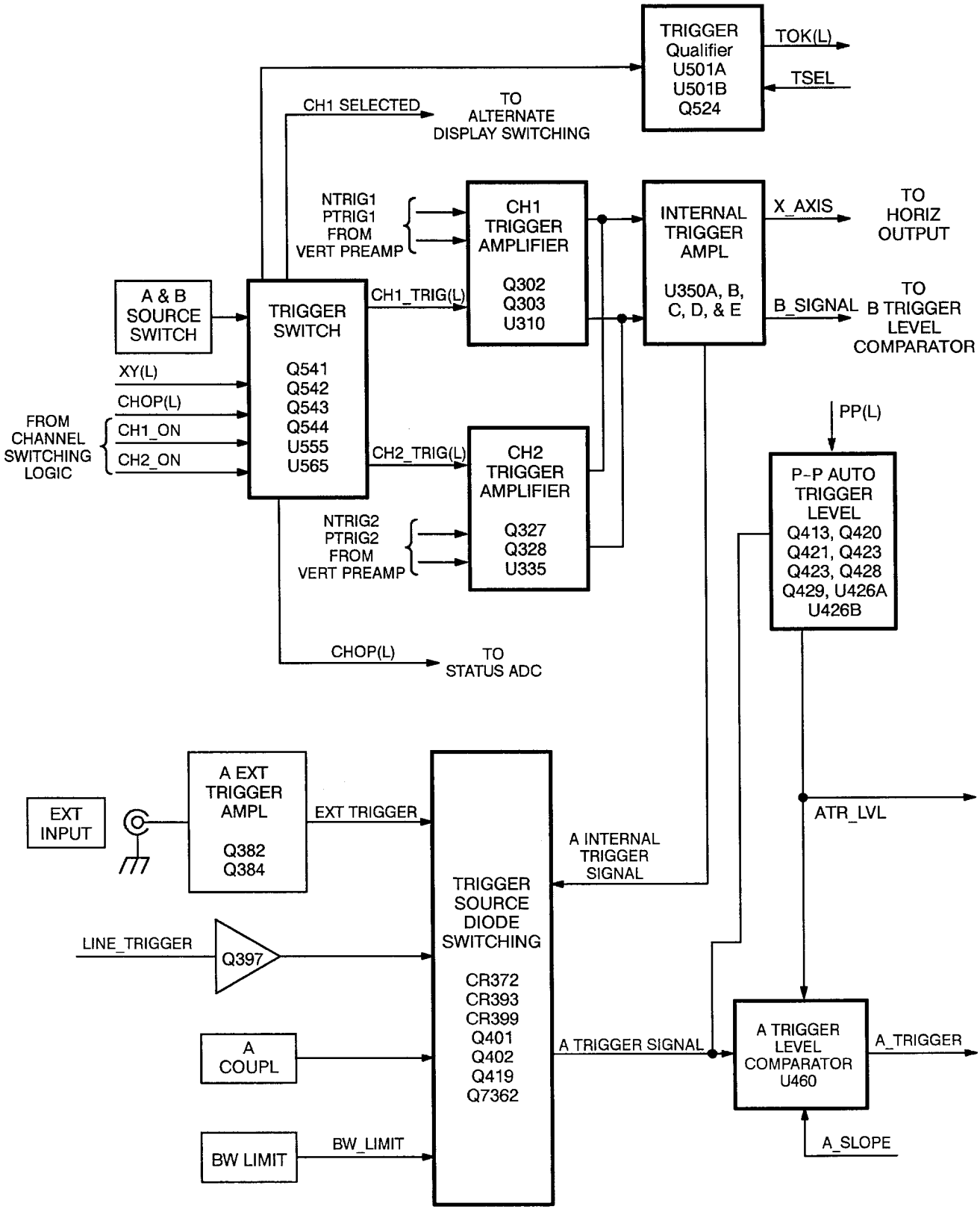


Figure 3–4. Block Diagram of Trigger Amplifiers and Switching.

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CHANNEL 1. For triggering from Channel 1, the A & B SOURCE switch is set to CH 1. The XY line connected to S555 is at ground potential, holding pin 4 of U555B LO. The output of U555B is then also LO, and the Channel 1 signal has a path through U310. At the same time, the Channel 2 signal path through U335 is shut off by the outputs of U555C and U565B both being HI.

CHANNEL 2. For triggering from Channel 2, the A & B SOURCE switch is set to CH 2, and U555C pin 10 and U555D pin 12 are LO. The outputs of both AND gates are then forced LO. A LO output from U555C enables the Channel 2 signal path through U335, and the HI outputs from U555B and U565C disable the Channel 1 path through U310.

VERT MODE. When the A & B SOURCE switch is set to VERT MODE, the trigger source is selected by the two VERTICAL MODE switches. For all VERTICAL MODE switch combinations except BOTH-CHOP, the base of Q541 is HI. The inputs and outputs of U555B, U555C, and U555D are then all HI, and trigger signal selection is done by flip-flop U540A in the Channel Switch Logic circuit (Diagram 2) using the CH1_ON and CH2_ON control signals going to U565B and U565C.

With Channel 1 selected (VERTICAL MODE switch set to CH 1), both inputs to NAND gate U565C are HI. The output of U565C is then LO, and U310 is biased on to select Channel 1 as the Internal Trigger signal source. The LO CH2_ON signal from the $\overline{Q}$ output of U540A is applied to U565B, and the CH2_TRIG(L) line at the output of U565B is forced HI to shut off the Channel 2 Trigger signal path.

When Channel 2 is selected (VERTICAL MODE switch set to CH 2), the outputs of U540A, U565B, and U565C will be the reverse of the states described for Channel 1 selection. The Channel 2 signal is then selected as the Internal Trigger signal source, and the Channel 1 Trigger signal path through U310 is shut off.

With ALT VERTICAL MODE selected, the inputs of NAND gates U565B and U565C toggle (change state) with each sweep. The outputs of the two gates also toggle, and U310 and U335 are alternately biased on to select the displayed channel signal as the Internal Trigger source.

In the ADD VERTICAL MODE position, both inputs to U565B and to U565C are HI, making the outputs of both gates LO. Both the Channel 1 and the Channel 2 signal path are turned on by biasing on U310 and U335 together. The output currents of both Trigger Preamplifiers are summed in the Internal Trigger Amplifier to produce the Internal Trigger signal.

The CHOP VERTICAL MODE position grounds the base of Q541 and puts a LO on an input of both U555B and U555C. The outputs of these two gates are then LO, and the signal to the Internal Trigger Amplifier is the summed Channel 1 and Channel 2 trigger signals, the same as with ADD VERTICAL MODE.

The A EXT position applies 8.6 V to the base of Q393, which turns off. The EXT(L) signal on the collector of Q393 forward biases CR393, passing the EXT_INPUT signal from the A External Trigger Amplifier through Q460, pin 4 (Trig In).

The A EXT position also applies 8.6 V to the anode of CR396, which causes the INT(L) signal line to go high. CR372 is turned off, preventing the internal trigger signal from reaching Q401.

The high on the INT(L) signal line is also coupled through CR391 to U9401 (diagram 12).

Trigger Qualifier

The Trigger Qualifier circuit synchronizes the storage acquisition vertical channel to the alternate sweep logic on the Main board, during ALT Vertical Mode operation. If the microprocessor is ready to acquire channel 1, it writes a low to TSEL via output port U4119, pin 12 (Diagram 17). If channel 2 acquisition is required, TSEL will be set high. In ALT Vertical Mode, the CH1_TRIG(L) and CH2_TRIG(L) lines alternately toggle after each sweep. When CH1_TRIG(L) is low, CH2_TRIG(L) will be high. The outputs of U501A and U501B are "wire-ORed" together. If TSEL is low, U501A is enabled by applying +0.7 V to pin 2, and U501B is disabled by applying -0.1 V to pin 6. CH1_TRIG(L) goes low enabling the CH 1 Trigger Amplifier and forcing TOK(L) low through U501A. TOK(L) is routed to U4104 to enable the storage trigger multiplexer U4227 (Diagram 17). When TSEL is high, Q524 is driven on, and the functions of U501A and U501B are reversed.

A External Trigger Amplifier

The A External Trigger Amplifier buffers signals from the EXT INPUT connector to drive the A Trigger Level Comparator. Input signal coupling is determined by A EXT COUPL switch S380 which selects AC, DC, or $\frac{DC}{10}$ & B coupling.

When S380 is in the AC position, the input signal is ac-coupled through C376. In the DC position, the input signal is connected directly to the Amplifier. The $\frac{DC}{10}$ position attenuates the input signal by a factor of 10 through the compensated divider formed by R377, R378, C380, and C381.

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Line Trigger Amplifier

The Line Trigger Amplifier supplies a line-frequency trigger signal to the A Trigger Level Comparator when the A COUPL switch is in the A LINE SOURCE position. Transformer T390 in the Power Supply (Diagram 8) provides the line-frequency trigger signal through R397 to Q397. Diode CR399 is forward biased when S392 is in the A LINE SOURCE position, and the emitter signal of Q397 drives the A Trigger Level Comparator.

Trigger Signal BW LIMIT, HF REJ, and LF REJ

The upper frequency of the trigger signal and the vertical channel bandpass are limited to 20 MHz when the front-panel BW LIMIT switch is pressed in. The BW Limit signal voltage forward biases Q419, and capacitor C419 shunts the higher trigger signal frequencies to ground through the transistor. With full 100 MHz bandwidth, Q419 is biased off to remove the shunting effect from the trigger signal line.

The HF REJ bandwidth limiting circuit provides high-frequency rejection of the trigger signal. When HF REJ is enabled, Q7362 is biased on and capacitor C7362 shunts trigger signal frequencies above 40 kHz to ground through the transistor.

The LF REJ circuitry provides low-frequency rejection of the trigger signal. When A COUPL switch S392 is set to the LF REJ position, +8.6 V is applied to the base of Q402, forward biasing it. The gate of Q401 is LO, turning Q401 off. The trigger signal is coupled to U460 through capacitor C402 which attenuates trigger signals below 40 KHz. The LF REJ and INT(L) signals are also read by U9401 (Schematic 12), which is scanned by the microprocessor for trigger coupling status information. This data is used by the display system for trigger level readout conditioning.

P-P Auto Trigger Level

The P-P Auto Trigger Level circuit sets voltage levels at the ends of the A TRIGGER LEVEL potentiometer (R438) as a function of the A Trigger mode selection and the trigger signals selected by the A & B SOURCE switch.

In the P-P AUTO and TV FIELD Trigger modes, Q413 is biased off, and CR414 and CR415 are reverse biased. Trigger signals selected by the A & B SOURCE switch are sent to peak detector circuits formed by Q420-Q422 and Q421-Q423 via R420. These peak detectors track dc levels and have high voltage-transfer efficiency. The circuit arrangement of the transistors produces very low thermal drift and reduces the effect of differences in transistor characteristics.

The positive- and negative-peak signal levels are stored by hold capacitors C414 and C415. The charge on the capacitors is held near the peak voltage levels between trigger signal peaks by the long time constant discharge path through R426 and R427. Amplifiers U426A and U426B are voltage followers with feedback supplied by transistors Q428 and Q429. These feedback transistors compensate the P-P Auto Trigger Level circuit for any thermal drift of Q420 and Q421 and shift the output levels of the voltage followers back to the original dc levels of the input trigger signal peaks. The output of U426A is the positive peak voltage of the input trigger signal, and the output of U426B is the negative peak voltage. Auto Level Adjustment potentiometers R434 and R435 provide dc offset corrections to make certain that the output voltages applied to the ends of LEVEL potentiometer R438 remain at or just below the actual peaks of the input trigger signal. In this way, the range of the LEVEL control is held within the peak-to-peak limits of the applied trigger signal for ease in triggering the oscilloscope.

In NORM Trigger mode, +8.6 V is applied to the junction of R411 and R414. Diode CR414 is forward biased. Transistor Q413 is also turned on inverting the applied signal and forward biasing CR415. Input transistors Q420 and Q421 are then biased off, and no trigger signals reach the P-P Auto Trigger Level circuit. In this case, the inputs to U426A and U426B are fixed voltages, and the voltage levels applied to the ends of the LEVEL potentiometer are independent of trigger-signal amplitude. The user must then adjust the LEVEL control to the correct level to obtain triggering.

The Microprocessor is informed of the trigger mode by Q7440 (Diagram 5) and its associated biasing resistors. When the P_P(L) signal line is a LO at -8.3 V (indicating that the P-P AUTO Trigger mode is in effect), Q7440 is biased off, and its collector (and the P_P signal line to the I/O circuit board) is pulled up to the +5 V supply via R7442. When the P_P(L) signal is a HI at +8.5 V for NORM Trigger mode, Q7440 is biased on, and the P_P signal is pulled LO by the conducting transistor.

A Trigger Level Comparator and Schmitt Trigger

The A Trigger Level Comparator compares the level of trigger signals selected by the A TRIGGER SOURCE switch to the voltage set by the A TRIGGER LEVEL control and produces an output trigger signal at the correct

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level. Rising or falling slope triggering is selected by the front-panel A TRIGGER SLOPE switch.

Integrated circuit U460, contains the A Trigger Level Comparator and Schmitt Trigger circuitry. The output voltage of the trigger amplifiers are applied to U460 pin 4. The other input to the comparator is the wiper voltage on the A Trigger LEVEL control, applied to pin 2 of U460. The resistor R452 and the voltage at pin 5 of U460 sets the emitter current for the comparator.

The Trigger Slope is determined by the relative voltages on U460 pins 7 and 8. If pin 8 is at a higher level than pin 7, the plus output of U460 will change to a HI state when a positive-going input signal crosses the threshold at pin 2 of U460. With pin 8 more negative than pin 7, the Schmitt fires on a negative-going input. The voltage at pin 7 is fixed, while that at pin 8 is selected by the A TRIGGER SLOPE switch S460 through R459, R461, and R462.

The sensitivity of the Schmitt Trigger is controlled by the current at pin 9. The setting of R471 determines the circuit hysteresis.

The outputs of the Schmitt Trigger are at pins 10 and 12 of U460. The outputs are at ECL levels and are from emitter followers internal to U460. Collector voltage to U460 is supplied through pins 11 and 14. When TV FIELD is not selected, the SS(L) line connected to CR476 and R473 is LO. Transistors Q473 and Q474 are biased off which also biases Q487 off. Resistor R477 biases CR467 and CR477 on and the +Out Trigger signal from pin 10 of U460 passes through the diodes to U506-6 of the A Sweep Generator.

TV Trigger Circuit

When TV FIELD mode is selected the SS(L) line is HI. This disconnects the high-speed trigger path by reverse-biasing CR467 and CR477. Setting the A Trigger level threshold near the center of the horizontal-sync-pulse swing establishes the untriggered level. This in combination with the peak detectors makes the circuit insensitive to the video information. The A TRIGGER and LEVEL controls are set to provide a pulse-train corresponding to the sync pulses of the TV signal. This pulse train is filtered by R467, C467, R468, R469, C469, and R470, resulting in dc levels at the bases of Q473 and Q474. The untriggered level (horizontal pulses) turns Q474 on, which causes Q487 to conduct, providing a LO to the sweep generator. When the TV-Vertical-Sync block occurs the polarity reverses, turning Q487 off and providing a positive-going signal to U506 pin 6 to initiate a sweep.

A SWEEP GENERATOR AND LOGIC

The A Sweep Generator and Logic circuitry, shown on Diagram 5, produces a linear voltage ramp that drives the Horizontal Preamplifier in the Non-store mode. The Sweep Generator circuits also produce gate signals that time the crt unblanking and intensity levels for viewing the Non-store displays. In STORE mode, the A Sweep Generator and Logic circuitry continues to produce timing gates used by the Storage circuitry for triggering the analog signal acquisitions. See Figure 3-5 for the block diagram of the A Sweep Generator and Logic circuitry.

The Sweep Logic circuitry controls the Non-store hold-off time and generates gating signals that start the sweep when a trigger signal occurs and end the sweep at the proper level. When using P-P AUTO or TV FIELD triggering, the Sweep Logic circuitry causes the Sweep Generator to free run if a trigger signal is not received or does not come often enough.

A Miller Sweep Generator and SEC/DIV Switching

The A Miller Sweep Generator is an integrator circuit that produces a linear voltage ramp to drive the Horizontal Amplifier for the Non-store A Sweep deflection. It produces the ramp voltage by maintaining a constant current through timing capacitors, causing a linear voltage rise across them as they charge.

Field-effect transistors Q704A and Q704B are matched devices with Q704B acting as the current source for Q704A. Since the gate and source of Q704B are connected together with no voltage difference between them, the source current available to Q704A is just enough so that there is no voltage drop across the gate-source junction of Q704A.

When the sweep is not running, Q701 is biased on, holding the selected timing capacitors discharged. The low impedance of Q701 in the feedback path holds the A Miller Sweep output (A_SWEEP) near ground potential. The voltage across Q701, in addition to the base-emitter voltage of Q706, prevents Q706 from becoming saturated.

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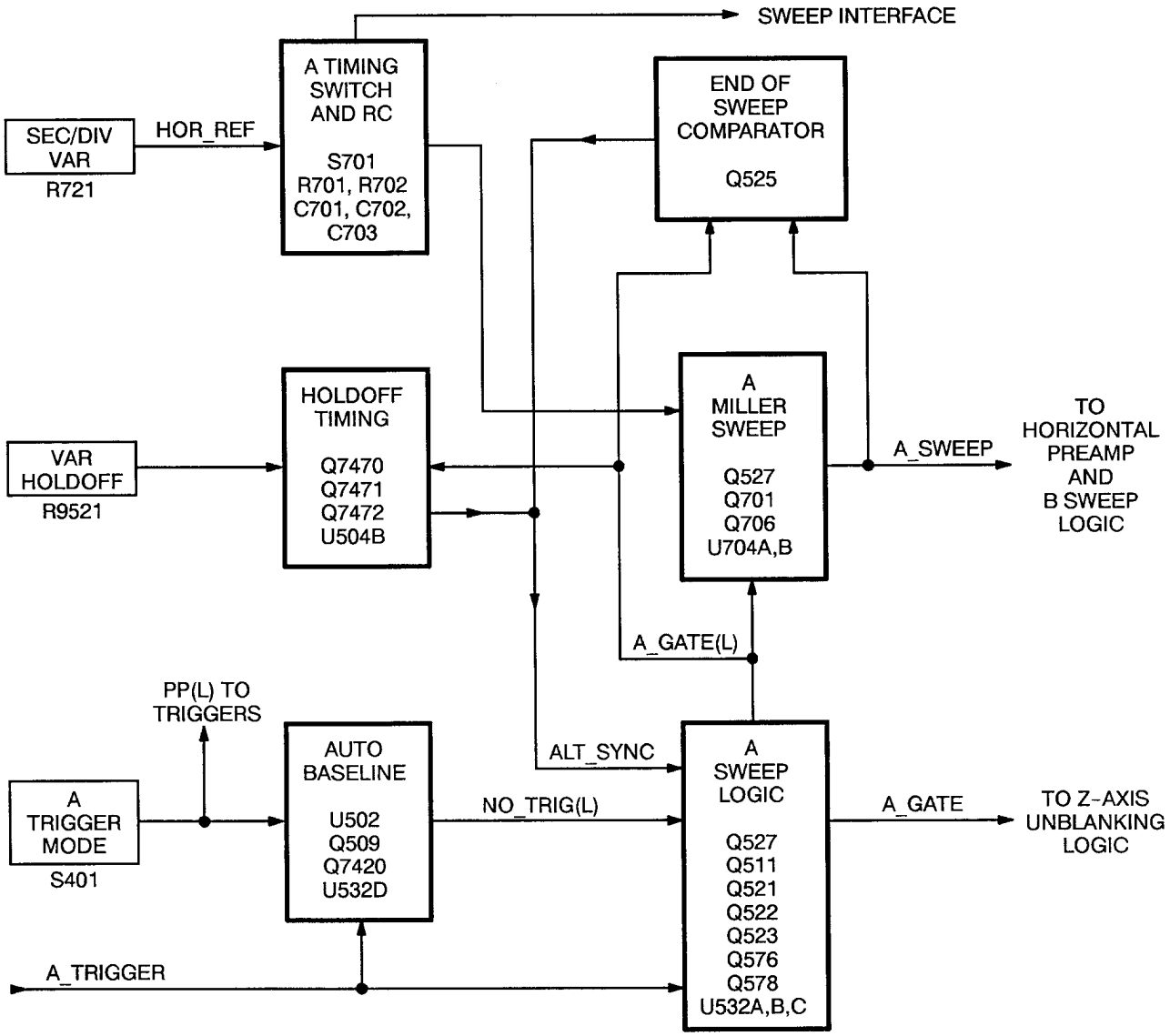


Figure 3–5. A Sweep Generator and Logic circuitry.

A sweep ramp is started when Q576 is biased off. The A_GATE(L) signal going to the base of Q701 from the Sweep Logic circuit turns Q701 off. The timing capacitors then begin charging at a rate set by timing resistors R701, R702, and the selected timing capacitors. Due to feedback from the circuit output through the timing capacitors, the integrator input voltage at the gate of Q704A remains fixed and sets a constant voltage across the timing resistors. This constant voltage produces a constant charging current through the timing capacitors, which results in a linearly increasing voltage ramp as they charge. The ramp is the A_SWEEP output signal at the collector of Q706.

Parallel timing capacitors C702 and C703 remain in the charging circuit for all SEC/DIV switch settings and are used mostly for high sweep speeds. Capacitors C701A and C701B are added in series at medium sweep speeds, and C701B alone is added to the charging path for slow sweep speeds.

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When the ramp reaches approximately 12 V, the End-of-Sweep Comparator transistor (Q525) becomes forward biased. This action switches the A_GATE(L) HI and starts the analog hold-off period. During hold off the A Sweep Generator is reset. The A_GATE(L) signal going HI biases on Q701, and the timing capacitors are fully discharged before another sweep starts.

One end of timing resistor array R701 is connected to the HOR_REF signal, and the other end is connected to the input of the Miller integrator by the SEC/DIV switch contacts. The voltage applied to the timing resistor array via the HOR_REF signal varies with the setting of the front-panel Variable SEC/DIV control (R721, located on Diagram 7). The STORE mode time base is not affected by the variable potentiometer setting. In the CAL position of R721, a fixed reference level is applied to R701 to produce the calibrated Non-store sweep speed ranges. Switch contacts actuated using the knob of R721 control the STORE mode 4K/1K Compress and the X10 MAG features. The X10 MAG feature works in both Non-store and STORE.

Coded analog signals developed by circuitry connected to the SEC/DIV switch contacts inform the Microprocessor of the A SEC/DIV switch setting. The Microprocessor then directs the Digital Time Base circuitry to set the correct STORE mode sampling rate.

A Sweep Logic

The A Sweep Logic circuitry controls sweep generation, as a function of incoming trigger signals and the A Trigger mode selected.

Incoming trigger signals from the output of U460 clock U502, a one-shot multivibrator, and cause the Q output of U502 to go HI. If another trigger signal is not received by U502 within the time limit determined by R503 and C501, the Q output (U502 pin 3) will go LO. Whenever trigger signals are being received, the $\overline{Q}$ output of U502 biases on Q509 to turn on DS518, the TRIG'D LED. The output of U502 is also used in the Auto Baseline circuit as described in the "P-P AUTO and TV FIELD" part of the discussion that follows.

NORM. When NORM Trigger mode is selected, input pin 12 of U532D is held HI by S401B, causing the gate output to also be HI. The output of U532C is then LO, and U506 pin 3 is not held HI. Input pin 4 of U532A is held HI by S401C, causing the output to be LO, placing a LO on input pin 7 of dual flip-flop U506. Trigger signals received at input pin 6 (a clock input) of U506 then clock this LO to the Q output (pin 2).

During the previous hold-off period, U506 pin 2 was set HI by U532B. This made the $\overline{Q}$ output (pin 3) LO. The LO biased Q576 on, preventing the A Miller Sweep from running. Whenever U506 pin 6 is clocked by a trigger signal following hold off, the LO on the D input (pin 7) is transferred to the Q output (pin 2), and the $\overline{Q}$ output (pin 3) goes HI. This biases Q576 off, and the A Miller Sweep generates the sweep ramp as described in the previous "A Miller Sweep Generator" discussion. When the ramp voltage reaches about 12 V, End-of-Sweep transistor Q525 is biased on. The output of U532B then changes from LO to HI, setting U506 pin 2 HI and biasing on A_GATE(L) transistor Q576. This triggers Hold-off One-shot U504B to start the hold-off period, turning off Q525. Transistor Q701 in the A Miller Sweep generator is also biased on to discharge the timing capacitors during hold-off time.

With U504B triggered, output pin 10 changes from LO to HI, where it stays for a time set by the Hold-Off Timing circuitry and the A SEC/DIV switch position. VAR HOLDOFF potentiometer R9521 sets the amount of current that is available to charge C518, C519, or C520 to the threshold voltage on pin 14. During the time pin 10 is HI, pin 5 (the set input) of U506 is held HI so that trigger pulses cannot start a new sweep. When pin 15 of U504B reaches the threshold level on pin 14, pin 10 goes LO to end hold off and release U506 from the set condition. The circuit is then reset to start another sweep on the next trigger pulse that appears at the clock input (pin 6) of U506. The holdoff capacitors are switched by transistors Q7470 and Q7471 according to the states of the timing switch. Q7472 serves as a dual diode to carry the discharge current. Logic signals AC1 and AC2 provide part of the timing switch information for the I/O board, where their states are read at an input port.

P-P AUTO and TV FIELD. When P-P Auto or TV Field trigger is in use, the Auto Baseline circuitry is active. Pin 12 of U532D is held LO by R569, and the output at pin 9 follows the signal provided by the Q output (pin 3) of U502. If trigger signals are being received, U502 remains set. As long as U502 is set, the output of U532D is HI, causing the output of U532C to be LO. Dual flip-flop U506 then responds to trigger signals at Clock input pin 6 as described in the "NORM" part of this discussion. If trigger signals are not being received by U502, its output and the output of U532D are both LO. With a LO on pin 10 of U532C, its output is the inverse of the input signal applied to pin 11. At the end of hold-off, that output goes LO, making U506 pin 2 LO and pin 3 HI. This automatically generates the A_GATE and A_GATE(L) signals, generating a sweep. The Auto Baseline continues holding NOR-gate U532C enabled so that new

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sweeps are generated at the end of hold-off as long as trigger signals are not received at U502.

SGL SWP. The following discussion presumes Non-store mode. In Sgl Swp mode, both the P-P AUTO and NORM front-panel buttons are in their out position. This results in a LO at the output of U532C that does not permit flip-flop U506 pin 3 to be held HI. A LO is also on input pin 4 of U532A.

During hold-off, U532B makes U506 pin 14 HI and pin 15 LO, causing pin 7 (the D input) of U506 to be HI. After hold-off ends, clock signals (triggers) to U506 pin 6 keep U506 pin 3 LO, keeping the sweep generator held off. When the SGL SWP button is pushed in, pin 7 of U504A goes LO for a time period determined by the time constant of R504 and C504 and then returns HI. The HI clocks the HI on input pin 10 of U506 to output pin 15. Consequently the output of U532A goes LO, and CR514 is reverse biased to bias Q511 on, lighting the READY LED. The next trigger pulse applied to input pin 6 of U506 starts a sweep as described previously. At the end of the sweep, U506 pin 15 goes LO and pin 14 goes HI, causing the TRIG'D LED to go out and placing a HI on the input pin 7 of U506. A new sweep cannot be started until the SGL SWP button is again pressed, resetting the sweep.

In STORE mode, the major difference is that the STO_RDY line is not true until the processor recognizes that a trigger has occurred. This prevents the SGL SWP button from affecting the circuit directly. Instead, the processor determines the button was depressed, releases STO_RDY, causing the effect described above when a button is depressed in Non-store mode.

X-Y. In the Non-store X-Y mode, the XY(L) signal is LO and Q522 is biased on, pulling pin 7 of U532B LO. The output of U532B holds U506 pin 3 LO and pin 2 HI, and no sweeps can be started during X-Y mode. Non-store X-Axis deflection (horizontal) is determined by the CH 1 OR X input signal. In STORE mode, the A Sweep Logic circuit must run to produce the gating required to synchronize the Storage signal acquisition. The STORE_ON signal forward biases CR501 to override the XY(L) signal, and the A Sweep Logic circuitry operates as in Y-T Non-store mode.

B TIMING AND ALTERNATE B SWEEP

The Alternate B Sweep circuitry, shown on Diagram 6, produces a linear voltage ramp that drives the Horizontal Preamplifier for Non-store B Sweeps. The Alternate B Sweep circuitry also produces the sweep-switching signals that control the display of the A and B Non-store Sweeps and the gate signals used by the Intensity and Z-Axis circuits to set the crt unblanking and intensity levels for the Non-store A Intensified and the B Sweep displays. The B_GATE signal goes to the Digital Time Base circuitry and is the Storage trigger signal for B Delayed Horizontal Display mode. See Figure 3-6 for a block diagram of the B Sweep Generator and Logic circuitry.

The B Sweep ramp is started by the B Sweep Logic circuit either at the end of the set delay time (RUNS AFTER DELAY) or when the first trigger signal occurs after the delay time has elapsed (Trigger After Delay). This delay time is a function of the B Delay Time Position Comparator circuit and the A Sweep.

B Miller Sweep Generator

The B Miller Sweep Generator is an integrator circuit formed by Q709, Q710A, Q710B, Q712, and associated timing components. This circuit produces the B Sweep signal and works the same as the A Miller Sweep Generator. See the "A Miller Sweep Generator" section for a description of circuitry operation. The output at the collector of Q712 drives the Horizontal Amplifier for Non-store B Sweeps and is applied to the B end-of-sweep transistor, Q643.

B Trigger Level Comparator and Schmitt Trigger

The B Trigger Level Comparator and Schmitt Trigger are contained in U605. This circuit determines both the trigger level and slope at which the B triggering signal is produced. It functions in the same manner as the A Trigger Level Comparator and Schmitt Trigger with the exclusion of the TV trigger circuitry. See the "A Trigger Level Comparator and Schmitt Trigger" section for a description of circuit operation. The +OUT terminal of U605 is directly connected to the clock input of U670A to initiate the B Sweep when the B Trigger is utilized.

Run After Delay

The Run After Delay circuit lets the B Sweep Logic start a B Sweep without the need for a B Trigger signal. For the RUNS AFTER DELAY mode, B TRIGGER LEVEL control R602 is rotated fully clockwise. In this position of R602, transistor Q637 is biased off, and a LO is present at its collector. Inverter U660D then has a HI output at pin 8. Resistor R640 provides positive feedback to obtain rapid switching of the transistor. This HI output reverse biases CR626 so that the state of U670A is determined by the level at U660F pin 12.

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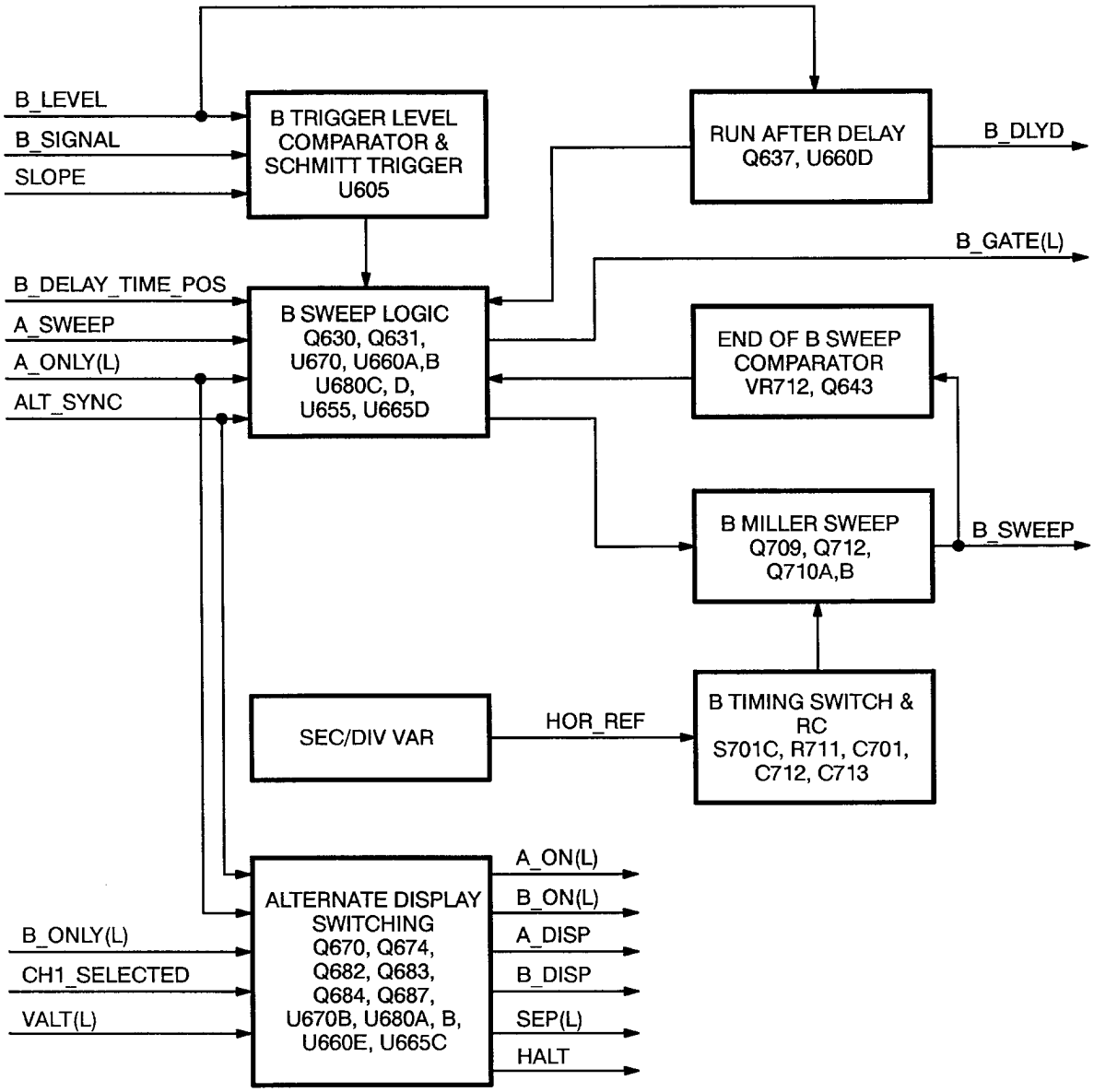


Figure 3–6. B Sweep Generator and Logic circuitry.

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If the B TRIGGER LEVEL control is not fully clockwise, Q637 is biased on, and the B Sweep is in the triggerable-after-delay mode. The output of U660D is then LO which keeps the S input of U670A LO, preventing the flip-flop from being set by the output of U660F.

The output of U660D is also connected to U6103 (Diagram 18), which is scanned by the microprocessor to sense when Runs After Delay has been selected for delayed readout conditioning.

Operation of the B Sweep Logic circuitry under both triggering modes is described in the "B Sweep Logic" part of the following discussion.

Delay Time Position Comparator

The Delay Time Position Comparator circuit compares the amplitude of the A Sweep voltage ramp to the dc voltage level set by the position of B DELAY TIME POSITION potentiometer R9644. The output of the comparator enables the B Sweep Logic circuit to start the B Sweep after the end of the delay time.

The input voltages to Comparator U655 to be compared are the voltage from the wiper of B Delay Time Position potentiometer R9644 and the A Sweep voltage from the divider formed by R651, Delay Dial Gain potentiometer R652, and R653. Maximum and minimum input voltages are established by VR645 and R646 respectively for the noninverting input and by R652 for the inverting input. Delay Start potentiometer R646 is adjusted in conjunction with Delay End potentiometer R652 to set the B DELAY TIME POSITION crt readout calibration.

The comparator is controlled by the A_ONLY(L) gate signal connected to pin 6. When the A_ONLY(L) signal is HI, the comparator is able to make a comparison. While the A Sweep signal on pin 3 is below the wiper voltage on pin 2, the comparator output is at a HI level. When the A Sweep ramp reaches the comparison level, the output at pin 7 goes LO. If A_ONLY(L) is LO, the comparator is switched to a high impedance output state. The comparator output level is then a HI that goes to pin 9 of NAND gate latch U680C and U680D.

B Sweep Logic

The B Sweep Logic circuitry utilizes signals from associated B Sweep circuitry to generate control signals for both the B Miller Sweep and the B Z-Axis Switching Logic circuits.

In the RUNS AFTER DELAY mode, the Run After Delay circuit holds the D input of flip-flop U670A LO via U660B. At the start of hold off when the A Sweep is reset, U680D pin 13 is strobed with an Alt Sync pulse negative transition. The output of the NAND-gate latch formed by U680C and U680D is latched HI, and the output of U660F goes LO. This places a LO on the S input of U670A and a HI on the R input causing the flip-flop to reset. The LO on pin 2 and a HI on pin 3 of U670A are converted to TTL levels by Q630 and Q631. The resulting HI on the collector of Q630 turns Q709 on. This discharges the B Miller Sweep timing capacitors to reset the B Sweep Generator and keeps a new B Sweep from starting. During the next A Sweep ramp when the voltage at U655 pin 3 exceeds the voltage at pin 2, the comparator output goes LO. The NAND-gate latch changes output states and causes the Set input of U670A to go HI. The LO on the Set input then controls the flip-flop, and the $\overline{Q}$ output of U670A goes LO. Shunting transistor Q709 shuts off, and the B Miller Sweep Generator runs to produce a sweep ramp.

When the ramp voltage reaches a level of about 12 V, B end-of-sweep transistor Q643 turns on and blanks the rest of the B Sweep trace by reverse biasing CR817 in the Z-Drive signal line (Diagram 9). The B Sweep Generator continues to run either until the ramp reaches about 13 V, at which time VR712 conducts to prevent the ramp voltage from increasing further, or until the A Sweep ends. In either case, the B Sweep generator is reset when the A Sweep ends.

The B Sweep Generator becomes reset when the ALT_SYNC signal goes from HI to LO to switch the output state of the U680C-U680D latch. The Reset input of U670A then goes LO, causing the $\overline{Q}$ output (pin 3) to switch HI and reset the Sweep Generator. Depending on the settings of the A and B SEC/DIV switches, the A Sweep may end before the B Sweep. In that case, the ALT_SYNC signal going LO at the end of the A Sweep immediately resets the B Sweep Generator even if the sweep ramp has not reached its maximum amplitude. A new B Sweep starts the next time the B Delay Time Comparator goes LO.

When not in the Runs After Delay mode, the output of U660D is LO, and U670A has a LO on the Set and a HI on the D input. The circuitry connected to the Reset input of U670A functions as described before. When the output of U660F goes HI, U670A is no longer held reset. In this case, the first B Trigger signal from U605, after the end of the delay time, clocks the HI on the D input, setting flip-flop U670A. The $\overline{Q}$ output of U670A is then LO, and a B Sweep is started by reverse biasing Q709 in the B Miller Sweep as before.

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Alternate Display Switching Logic

The Alternate Display Switching Logic circuitry controls both the Non-store Horizontal Amplifier sweep switching and the Non-store Z-Axis Logic switching for A Intensified and B Only traces. The B Sweep ramp and gates are produced for every A Sweep when the HORIZONTAL MODE is set to either ALT or B. In ALT, the intensified zone on the A Sweep trace is shown for one B Sweep interval, and during the next A Sweep interval, a B Sweep trace is displayed during the B Sweep interval. For B Only traces, the A Sweep must still run to produce the A gating signals used throughout the circuitry for timing, but it is not displayed.

HORIZONTAL MODE switch S648 selects the input logic levels that drive the display switching circuitry. In the A Horizontal mode, the Set input of U670B is LO, and the Reset input is HI. This holds U670B reset with the A_DISP signal HI, passing only the A Sweep to the Horizontal Amplifier (by the A Sweep selection transistor, Q742, located on Diagram 7). In the B Horizontal mode, the set input of U670B is HI, and the reset input is LO. This holds U670B set with the B_DISP signal HI, allowing only the B Sweep to reach the Horizontal Amplifier (via the B Sweep selection transistor, Q732).

With S648 set to BOTH, and for all settings of the VERTICAL MODE switches except BOTH-ALT, the VALT(L) signal applied to U660E is HI and the Set and Reset inputs of U670B are both LO. The LO out of U660E causes the output of U680B to be HI. Each HI to LO transition of the ALT_SYNC signal applied to pin 1 of U680A causes the NAND gate output at pin 3 to change from LO to HI, clocking U670B. The Q and $\overline{Q}$ outputs of U670B therefore toggle, and the A_DISP and B_DISP signals cause the sweep selection transistors (Diagram 7) to alternately pass the A and B Sweep signals to the Horizontal Amplifier.

When CH 1-BOTH-CH 2 VERTICAL MODE switch S550 is set to BOTH, ADD-ALT-CHOP switch S545 (Diagram 2) becomes active. In the ALT VERTICAL MODE position, the VALT(L) signal is LO, the HALT signal is HI, and the CH1_SELECTED signal is a TTL square-wave signal that switches states at the end of the A Sweep. Input pin 4 of U680B is HI, and the gate output is the inverted CH1_SELECTED signal. This output signal is combined with the ALT_SYNC signal by NAND gate U680A to clock U670B. Whenever the ALT_SYNC signal goes LO at the end of a sweep and the CH1_SELECTED signal (at U680B pin 5) switches from LO to HI, U670B is clocked. Since only positive transitions on the clock input causes the flip-flop to change output states, two A Sweeps must occur to cause the flip-flop output levels to switch. Switching this way, the crt first displays two A Intensified Sweeps, then two Alternate B Sweeps.

SWP SEP. Whenever the B Sweep is selected to drive the Horizontal Amplifier, the Q output of U670B is HI. This HI goes to U665C pin 10 through Q683 and Q687, and since pin 9 is also HI, the SEP(L) signal from U665C is LO to enable the A/B Sweep Separation circuitry (located on Diagram 3).

B SWEEP Z-Axis Logic

The B SWEEP Z-Axis Logic circuitry switches signal current levels to drive the Z-Axis Amplifier for the Non-store B Sweep and the A Intensified Sweep displays. The current supplied is summed with the other signal inputs on the Z-DRIVE line to set the Non-store display intensity levels.

With the HORIZONTAL MODE switch in the BOTH position, pin 5 of U665B (Diagram 9) is HI.

Then, the Q and $\overline{Q}$ outputs of U670B, the B_GATE(L) signal from the output of U665D, and the B INTENSITY potentiometer, set the intensity levels of the Non-store A Intensified and B Sweep traces. When the A Sweep trace is displayed, the $\overline{Q}$ output of U670B is HI, and the Q output is LO. These output levels bias Q683 on and bias Q682 off. The collector voltage of Q683 reverse biases CR817 (Diagram 9) to stop Z-Axis drive current from flowing through the diode. With Q683 reverse biased, additional Z-Axis drive current to intensify the A Sweep is supplied whenever CR685 (Diagram 9) is biased off by the gating action of U665B. Since input pin 5 of U665B is HI, the gate output and therefore the conduction state of CR685 is set by the B_GATE signal from U660C. While the B_GATE is HI, the output of U665B is LO, and CR685 is biased off to add B INTENSITY current to the Z-DRIVE line via CR816. During periods that the B_GATE is LO (B Sweep not running), the output of U665B is HI, and CR685 is biased on. Diode CR816 becomes reverse biased, and the extra current that was being supplied to the Z-DRIVE line to intensify the A Sweep is removed.

With the Q and $\overline{Q}$ outputs of U670B switched to display the B Sweep ($\overline{Q}$ LO and Q HI), Q683 is biased off, and Q682 is biased on. The collector voltage of Q682 reverse biases CR816 to block any Z-Axis drive current from being supplied through that diode. With CR687 off, the B Sweep is displayed if CR680 is reverse biased. During the B Sweep interval, the B_GATE(L) output at pin 11 of U665D is LO. Diode CR680 is then reverse biased, and Z-Axis drive current from B INTENSITY flows through CR817. If the B Sweep is not running, the B_GATE(L) output of U665D is HI. That HI forward biases CR680 and

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reverse biases CR817. No B Z-AXIS drive current flows through CR817.

Sweep Interface

U780 and U781 (Diagram 5) form digital-to-analog converters to encode the position of A SEC/DIV switch for microprocessor control of the readout and storage timebase. U782 and U783 (Diagram 6) perform the same function for the B SEC/DIV switch. The analog outputs—ARES1, ARES2, and B_RES—are listed in Table 6-4 as a function of A AND B SEC/DIV switch settings. These voltages are routed to the Status A/D (Diagram 18).

HORIZONTAL

The Horizontal Amplifier circuit, shown on Diagram 7, provides the signals that drive the horizontal deflection plates of the crt. Signals applied to the Horizontal Preamplifier may come from either the A or the B Miller Sweep Generator (for sweep deflection) or from the XY Amplifier (when Non-store X-Y display mode is selected). A and B Sweep switching is controlled by signals from the Alternate Display Switching Logic circuit discussed earlier. Either the Non-store sweeps or the Storage horizontal deflection signals are passed to the Horizontal Output Amplifier via a diode gating circuit. Signal selection by the Horizontal Mux circuit is controlled by the Channel Switch Logic output signals (located on Diagram 2). See Figure 3-7 for the block diagram of the Horizontal Amplifier.

The Horizontal POSITION control, X10 Magnifier circuitry, and the horizontal portion of the Beam Find circuitry are also part of the Horizontal Amplifier circuitry

Horizontal Preamplifier

The Horizontal Preamplifier switches the Non-store horizontal drive signals and amplifies input signals for application to the Horizontal Output Amplifier.

The A and B Sweeps are applied to the emitters of Q742 and Q732, through Sweep Gain potentiometers R740 and R730. Switching of the A and B Sweeps is controlled with these transistors. Using the A_DISP and B_DISP signals obtained from the Alternate Display Switching Logic circuitry (Diagram 6), Q732 and Q742 are either biased into the active or cutoff regions via CR732 and CR742. The POSITION control (R726) horizontally adjusts the crt trace position by supplying a variable dc offset voltage, through pin 14, to the output of the preamplifier. The position offset voltage from the wiper of R726 also goes to the Vector Generator circuitry (Diagram 19) to horizontally position the STORE mode waveform displays. Readout displays are not affected by the Horizontal POSITION control. Preamplifier output bias current levels are set by R751 at pin 5, and frequency compensation for X-axis signals is provided by C751, connected to pin 13.

Non-store horizontal X10 Gain is set by the resistor network between pins 3 and 6 of U760. When the X10 Magnifier is on, S721 is closed, and the amplifier gain increases by ten times. Magnified timing accuracy is adjusted using X10 Gain potentiometer R754. MAG potentiometer R749 is adjusted for no horizontal shift at the center of the graticule as X10 Magnifier is switched on and off. A second set of contacts on S721 informs the Microprocessor whether X10 Magnification is off or on. The SEC/DIV readout is automatically set to the correct scale factor, and STORE mode waveforms are digitally modified to reflect X10 magnification.

X-Y Amplifier

The X-Y Amplifier amplifies the Non-store Channel 1 signal (X_AXIS) from the Internal Trigger circuitry (Diagram 4) and passes it to the Horizontal Preamplifier.

When the Non-store X-Y mode is selected, Q737 is biased on to place a HI on U760 pin 12 to internally disconnect the A and B Sweep and the HORIZ POS input pins. The XY(L) signal line is LO, biasing Q756 off to let the X_AXIS signal drive the noninverting input of U758. The output of U758 is a combination of the X_AXIS signal on pin 3 and the Horizontal POSITION voltage applied to pin 2 via R758. The X-Axis deflection accuracy is adjusted by X-GAIN potentiometer R760. The single-ended X-AXIS signal at pin 11 of U760 is changed to a differential signal at the preamplifier output pins. The differential signal is passed through the Horizontal Mux circuit to the Horizontal Output Amplifier for final amplification. When the X-Y mode is not selected, Q756 is biased on, and the X_AXIS signal is shunted to ground through the transistor.

Horizontal Output Amplifier

The Horizontal Output Amplifier provides final amplification of the horizontal Non-store sweep signals or the STORE mode deflection signals to drive the horizontal crt deflection plates.

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In Non-store mode, signals from the (+) and (–) SWP outputs of U760 drive the Horizontal Output Amplifier. In STORE mode, horizontal LH_OUT or RH_OUT deflection signals are passed through the diode gate to drive the amplifier. Drive signals for STORE mode and readout character displays are selected by the Display Controller. Either Non-store sweeps or Store deflection signals are selected by the diode gating using signals from the Store/Non-store Multiplexer (U7201 on Diagram 2) through Inverter U7202A and U7202B.

The selected signals drive a differential shunt-feedback amplifier. Due to the feedback, the input impedance of the amplifier is low. The base voltages of Q770 and Q780 are biased at nearly the same dc level by forward-biased diodes CR765 and CR768 located between the two emitters.

Transistors Q770, Q775, and Q779, as one-half of the complementary differential circuit, form a cascode-feedback amplifier for driving the right crt horizontal deflection plate. Amplifier gain is set by R775, with C775 providing high-frequency compensation. For low-speed signals, Q779 serves as a current source for Q775. At high sweep rates, the deflection signal is coupled through C779 to the emitter of Q779 to provide added pull-up output current to drive the crt. The amplifier formed by Q780, Q785, and Q789 drives the left crt horizontal deflection plate in the same manner as described above, with zener diode VR782 shifting the collector signal level of Q780 to the correct level to drive the emitter Q785.

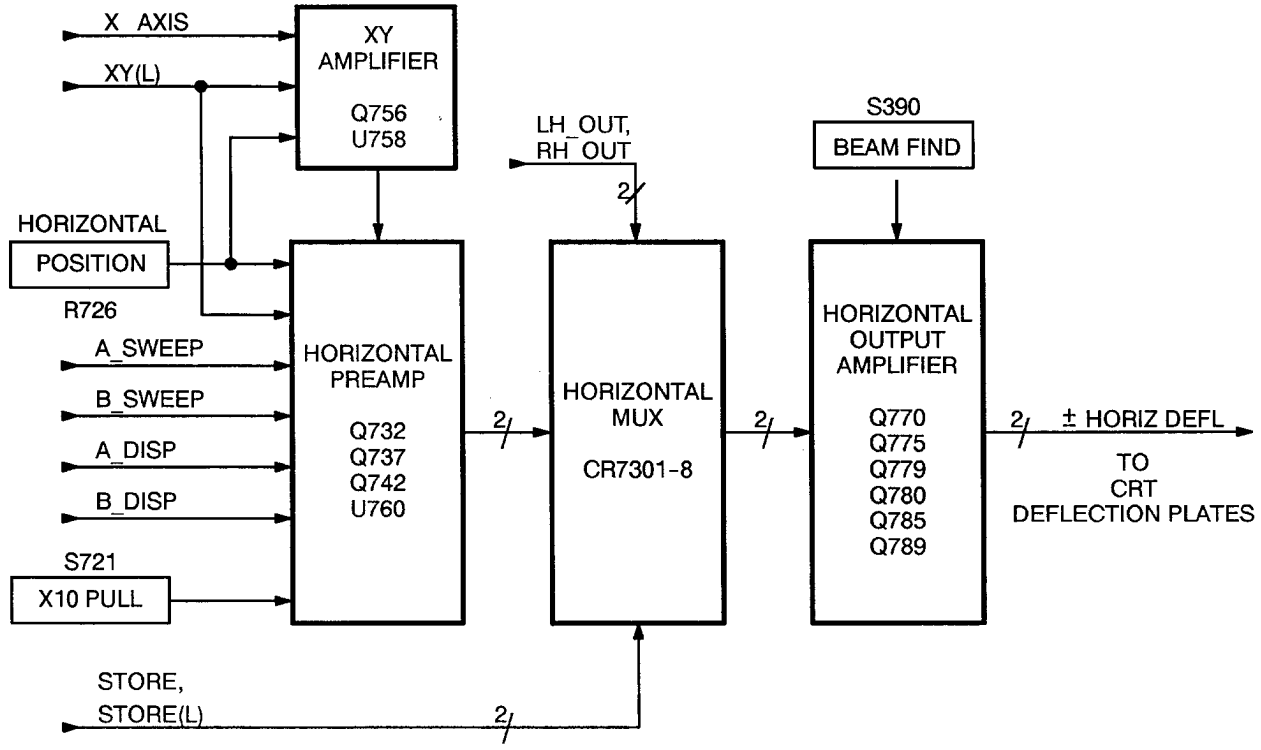


Figure 3-7. Horizontal Amplifier block diagram.

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The BEAM FIND function is active when S390 (Diagram 9) is pushed in to disconnect the cathode of CR764 from the -8.6 V supply. The voltage on the cathode of VR764 goes positive, causing CR780 and CR770 to be forward biased. Current from R764 causes the output common-mode voltage of the two shunt-feedback amplifiers to be shifted negative to reduce the available voltage swing at the crt plates. This stops the trace from being deflected off-screen horizontally. The BEAM FIND voltage also goes to the Vertical Output Amplifier, and the vertical deflection is limited in that circuit when the voltage is removed.

Sweep Reference

A circuit formed by Q7501 and Q7502 supplies reference voltages for the 1 K and 4 K storage acquisitions and for the variable SEC/DIV control, R721. Transistor Q7502 provides a 0.6 V drop from the -8.6 V supply to generate a -8 V reference for the 1K REF and one end of potentiometer R721. The 4K REF is produced by Q7501 and is adjusted by using the RATIO ADJ potentiometer to set the correct ratio for the two reference voltages. This reference level also goes to the other end of R721. The wiper voltage of R721 is the HOR REF voltage for the A and B Sweep timing resistors in Non-store mode. In STORE mode, either the 1K REF or the 4K REF voltage level is applied to the A and B Sweep timing resistors. Switching between reference levels for the different modes is done by K7501, which is controlled by U4119, and by the STORE/NON-STORE switch, S9403B.

Probe Adjust

The Probe Adjust circuitry, shown on Diagram 7, is a square-wave generator and diode switching network that produces a negative-going square-wave signal at PROBE ADJUST connector J9900. Amplifier U985 forms a multivibrator that has an oscillation period set by the time constant of R987 and C987. When the output of the multivibrator is at the positive supply voltage, CR988 is forward biased. This reverse biases CR989, and the PROBE ADJUST connector signal is held at ground potential by R990. When the multivibrator output switches states, and is at the negative supply voltage level, CR988 is reverse biased. Diode CR989 becomes forward biased, and the circuit output level drops to approximately -0.5 V.

MICROPROCESSOR

The Microprocessor, shown on Diagram 13, directs the operation of the Storage and digital circuitry in the oscilloscope by following firmware control instructions stored in the Microprocessor memory. The Store-Panel Controls are monitored by the Microprocessor to detect when a Storage operation is selected. The rest of the significant front-panel controls are monitored through the Front-Panel A-to-D converter and I/O interface circuitry. Circuit operation is then directed by the Microprocessor to perform the selected operation.

Microprocessor, Clock, and Timer

Microprocessor U9111, is the center of control activities. It is an eight-bit processor with its data bus multiplexed with the low eight bits of the address bus. The eight-bit combination bidirectional data bus for data transfer and addressing (AD0 through AD7) and the additional 12-bits of address bus for selecting the source or destination of the data transfers (A8 through A19). Precise timing of instruction execution, addressing, and data transfer is provided by an external, crystal-controlled oscillator, and Clock Generator (shown on Diagram 17).

The Digital Time Base produces a 13.4MHz clock for clocking the Microprocessor. The microprocessor divides the 13.4 MHz clock signal by two and applies the clock signal to the clock input of the Display Controller (U9208 on Diagram 16). The 6.7 MHz signal is also included in the Control Bus to provide a clock signal for future options.

The RESET output of the Microprocessor provides a power-on reset signal under normal operation or a manual reset using jumper connector P9104. U9117 provides the RESET signal to the processor and other circuitry based on appropriate levels of the 5 V supply. This holds the Microprocessor in the reset state until the power supply voltages are high enough to permit normal operation of the digital circuitry. The Microprocessor is held reset during the delay period. Manually moving jumper P9104 to the RESET position forces a reset of the Microprocessor and the Display Controller. The RAMs U9130 and U9131 are provided battery power when RESET is true, and are used for the non-volatile waveform storage feature.

Two additional RAMs available for general use are the Display RAMs, U9231 and U9232. Their access is mediated by the Display Controller and associated circuitry. To allow the Display Controller to have first priority access to the RAM, the RDY signal from the Display Controller is used to tell the Microprocessor to wait for access to the RAM.

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In addition, when one of the Communication Options is installed, the RDY signal is used to synchronize (RESET signal on U9111 pin 57) the operation of the Microprocessor with the asynchronous activity of the GPIB (General Purpose Interface Bus) or RS-232-C Options for parallel or serial data transfer via the external communications port.

Resistor pack R9113 is a data bus pull-up. During normal operation, the resistor pack generates the interrupt vector pointer. During the hardware kernel test, the resistor pack generates a NOP instruction that allows easy-to-troubleshoot signals to be available around the microprocessor.

Latch and Buffer

Addressing is done using dedicated address bus lines. Address latch U9112 demultiplexes the address bus (separates the address and data bytes). When an address is valid, the Microprocessor sets the address-latch enable (ALE/QSO) HI (U9111 pin 61). Both U9112 and U9114 are enabled to latch the address bits. The latched bits are held until the Microprocessor places a new address on the busses and again sets the ALE/QSO signal HI. Some bits passing through U9114 have status information multiplexed with the address, so U9114 also functions as a demultiplexer.

The Microprocessor communicates with the other devices on the data bus via Octal Bus Transceiver U9113. Two signals from the Microprocessor control enabling of the Transceiver and direction of the data flow. When the DEN(L) signal is LO U9113 is enabled for transfers, and the DT/R(L signal sets the direction of the transfer. Signal from U9115 qualifies the transfer to allow pull-ups to assert an interrupt number on the bus during interrupt cycles. While the address and data are available on the bus side of this transceiver, only the data time slot is used.

Decoder

In addition to providing specific addresses to internal locations within memory devices, the addresses are decoded to provide enabling signals for blocks of addresses and to control the selection of I/O (Input/Output) devices. Table 3-1 shows the instrument's memory map. U9115 and U9119 provide most of the general-purpose address decoding.

ROM

The operating system firmware is contained in two 128K by 8-bit read-only memories (U9120 and U9121). Immediately after the power-up reset ends, the Microprocessor automatically fetches the first command from the reset vector (address 0FFFF0), and begins program execution. Other interrupts to the Microprocessor cause vectoring to addresses that start the interrupt handling routines. The NMI (non-maskable interrupt) vector is at 00008, and the Maskable Interrupt (INTR) is vectored to 03FC (both interrupt vectors are in RAM).

Store Panel Controls and Buffer

The selection of the Storage Panel Controls is passed to the Microprocessor via two octal bus drivers, U6102 and U6103 (Diagram 18). Each bus driver transfers eight individual data bits to the data bus when enabled. Enabling of the bus drivers is done by EDE(L) line via U6111.

The Microprocessor communicates with the other devices on the data bus via Octal Bus Transceiver U9113. Two signals from the Microprocessor control enabling of the Transceiver and direction of the data flow. When the DEN(L) signal to U9115 is LO, U9113 is enabled for transfers, and the DT/R(L) signal sets the direction of the transfer.

Non-Storage Front-Panel Controls

Some front-panel controls do two things at the same time; control the real-time scope mode, and tell the Microprocessor what is being selected or modified. These controls include the vertical position controls, the vertical gain controls, the A and B time per division controls, the trigger mode controls, the vertical coupling controls, the sweep mode control, and the delay-time control. In addition, the probe-coding ring is read to determine true Volts per Division. The 1K/4K and STORE/NON-STORE switches select the reference voltage applied the A and B timing resistors in the Sweep Generator circuitry.

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Table 3-1
Memory Space Allocation

Block Designation	Block Address (Hex)	Space Allocation Purpose
RAM SEG	00000-1FFFF	Two images of Memory Segment.
RAM Primary	00000-07FFF	8-bit display RAM—waveforms, interrupt vectors, miscellaneous.
	08000-0FFFF	8 bits of display RAM for waveform attributes (LSB).
	10000-1FFFF	RAM Images.
IO SEG	20000-3FFFF	Four images of Memory Segment 1\fH.
	20000-2007F	Diagnostics 7-Seg Display U9118.
	20080-200FF	Display Chip Next Frame U9208.
	20100-2017F	Display Chip Interrupt reset U9208.
	20180-201FF	Acquisition Status U3401.
	20200-2027F	Acquisition Mode U4119.
	20280-202FF	Acquisition Mode 2 U4120.
	20300-20303	Front Panel Switch Matrix Rows 0-3.
	20304	Instrument Status port 0 U6102.
	20305	Instrument Status port 1 U6103.
	20306	A to D Mux Control U6104.
	20307	Front Panel A/D data U6105.
	20308-2037F	Image of Above.
COM IO SEG	40000-4FFFF	Comm I/O Segment.
	4067C (IO-2 A7,8)	Option Status Latch (in).
	406BC (IO-2 A6,8)	Option Parameters Latch (in).
	406F0 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F1 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F2 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F3 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F4 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F5 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F6 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F7 (IO-2 A3,8)	Option UART/GPIB chips (I/O).
	406F8 (IO-2 A2,8)	Option Interrupt Mask Latch (out).
COMM SEG	50000-5FFF	Reserved.
NV SEGMENT	60000-6FFFF	
	60000-677FF	26 Extended Nonvolatile Waveforms.
	67800-67FFF	Option ram.
	68000-697FF	System Stack.
	69800-69FFF	Non Volatile Settings.
	6A000-6BFFF	NV Back up of standard References.
	6C000-6FFFF	Rasterizer memory for Plot.

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Table 3-1 (cont)

ACQ SEG	70000-7FFFF	
Memory	70000-73FFF	Two images of CH1 Acquisition Memory Acquisition RAM U3410 and U3411, U3412, and U3413.
	74000-77FFF	Two images or CH2 Acquisition Memory Acquisition RAM U3418 and U3419, U3422, and U3423.
Control	78000-7801F	Acquisition Control CH1 U4000.
	78020-7BFFF	Multiple Images CH1 Acq Control.
	7C000-7C01F	Acquisition Control CH2 U4000.
	7C020-7FFFF	Multiple Images CH2 Acq Control.
ROM SEGMENT	C0000-FFFFF	
ROM Main Image	C0000-DFFFF	System ROM 0—U9121.
	E0000-FFFFF	System ROM 1—U9120.

STATUS ADC AND BUS INTERFACE

The system data bus and associated control signals are sent to the Status ADC and Interface circuitry (Diagram 18).

BUS INTERFACE

Input ports U6102 and U6103 transfer logic signals representing instrument status, U6103 operates as a port for eight of the status lines and U6102 has 7 status inputs. During part of the status scanning cycle, the Microprocessor reads these status lines through U6102 or U6103. Multiplexer selection register U6104 drives U6106 and U6108, which select the analog status signals to be measured. U6111 provides the address selection logic for U6102, U6103, U6104, and U6105.

STATUS A/D

A/D converter U6105 allows measurement of analog status signals. After each conversion it produces an interrupt FPINTR(L) signal. This signal produces a processor interrupt to indicate completion of its task. Buffer amplifier U6107A drives the input resistance of U6105 while maintaining fairly high load impedance for U6106 and U6108. Differential amplifiers U6107B and U6107C converts the differential vertical position signals to single-ended voltage levels within the range of the measuring system.

STORAGE ACQUISITION

The Storage Acquisition system, shown on Diagram 14 conditions the input signals for analog-to-digital conversion. The circuitry consists of signal conditioning circuits and A/D conversion modules.

Input Signal Conditioning

The signals for the two inputs channels of the storage acquisition system are supplied from the vertical preamplifier circuitry. The differential signals are routed to the instrument storage system via two-four wire ribbon cables. The two sets of input signals are applied to the bases of two input differential transistor amplifiers. The differential signals of CH1 + and CH1- are applied to the bases of transistors Q2210 and Q2211 and the differential signals CH2 + and CH2- are applied to the bases of transistors Q2202 and Q2204. Impedance matching between the input cables and transistor amplifiers is provided by resistors R2249 and R2250 for Channel 1, and R2219 and R2220 for Channel 2. The DC biasing voltage level at the bases of the input amplifiers is set by R2248 and R2217 for Channels 1 and 2, respectively.

The two amplifier circuits consist of differential pairs of cascode connected PNP transistors. The common emitter connected transistors Q2210 and Q2211, with the common base transistors Q2224 and Q2225, form the cascode configuration of Channel 1. The common emitter transistors Q2202 and Q2204, along with the common base connected transistors Q2220 and Q2221, form the Channel 2 cascode configuration. The Channel 2 amplifier also provides the signal switching of Channel 2 to the Channel 1 analog-to-digital module for signal addition

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of Channel 1 and Channel 2. The signal switching is performed by applying the add mode logic levels to the base biasing resistors pairs R2263–R2264 of Channel 2 and R2266–R2265 of the add circuit. The applied add mode logic signals select either the common base transistors Q2220 and Q2221 of Channel 2 or Q2222 and Q2223 of the add circuit. The transistor pair selection is done by turning one pair on and the other pair off, effectively routing the signal to either the Channel 1 or Channel 2 analog–to–digital module.

The emitter circuits of the differential amplifiers contain the current source bias resistors, gain setting resistors and high frequency compensation resistors and capacitors. The emitter–collector currents of the cascode transistor pairs are set by resistors R2246 and R2247 for Channel 1, and resistors R2215 and R2216 for Channel 2. The gain of the transistor amplifiers is set by resistors R2242, R2300 and RT2202 for Channel 1, and R2211, R2299, and RT2201 for Channel 2. RT2202 and RT2201 are temperature dependent thermistors, used to provide temperature compensated gain over the specified operating temperature range of the instrument. High frequency compensation for Channel 1 is provided by the RC networks of R2344–C2206 and R2298–C2207, and capacitor C2295. The HF compensation components of Channel 2 consists of R2213–C2203 and R2297–C2202 and C2296.

The collector circuits of the cascode common base transistors of Channel 1, channel–2 and ADD network provide gain control, DC bias level shifting and additional frequency compensation. Resistors R2280 and R2283 combine with the level shifting resistors and the analog–to–digital termination resistors to provide gain control for Channel 1. Resistor pairs R2270–R2273 and R2275–R2278 provide gain control for Channel 2 and the add channel, respectively. The capacitors C2273, C2272, and C2271 are used to provide a dominate pole in the response of each network to control the bandwidth and noise.

Calibration of the storage acquisition section is performed by the adjustment of DC offset, gain and frequency response of each amplifier network. The DC offset bias levels of Channels 1 and 2 are adjusted with potentiometers R2245 and R2214 respectively. These potentiometers control the balance of current supplied to each side of the differential pairs. The gain control adjustment for Channel 1 is provided by R2283 which combines with other resistances in the collector circuit to set the total resistance and gain. Potentiometers R2273 and R2278 provide gain control for Channel 2 and add channel, respectively. The high frequency compensation adjustments are provided by R2298 and C2207 for Channel 1 and R2297 and C2202 for Channel 2. These adjustments are used to set the step response and bandwidth of each channel.

Analog–to–Digital Conversion

The Analog–to–Digital Conversion modules, U2200 and U2201, each contain Sample–and–Hold (S/H) and Analog–to–Digital (A/D) Converter circuits. Along with the integrated circuits are input and output termination resistors, and power supply decoupling resistors and capacitors.

The U2200 and U2201 S/H circuits sample and amplify the input signal, and hold a dc level representing the sampled input for processing by the A/D Converter circuits. The A/D Converter circuit acquires the dc level from the S/H circuit and converts it to an 8–bit binary number representing the input level. The 8–bit binary outputs, pins 16,17, 19, 20, 22, 23, 26 and 27, are supplied to the digital acquisition system at ECL S/H circuits, pins 2–3 and 46–47 of U2200 and U2201, which can be used individually or together to add the two input signals. The Channel 1, module, U2201, uses together to add the two input signal. The Channel 1 module U2201, uses both sets of inputs so Channel 1 and Channel 2 signals can be added together and processed by the Channel 1 A/D Converter circuit.

The S/H and A/D conversion processes cycle at a 100–MHz clock rate. The S/H differential clock lines, pins 35 and 36, and A/D differential clock lines, pins 13 and 14, are designed for ECL compatible logic levels. The S/H clock phase leads the A/D Converter clock phase by a portion of a clock cycle so the sampled input level will be settled at the output of the S/H circuit when the A/D conversion process is performed. The 8–bit binary outputs are also at ECL compatible logic levels and are clocked to the digital memory system at a 100–MHz data rate. Two voltage regulators are used to provide the A/D Conversion module with a –2V reference level for the A/D Integrated circuit, pins 6 and 7, and another –2V supply for logic levels, pin 29. The voltage regulators consist of an operational amplifier regulator and drive transistor, U2202A and Q2200 for the –2V logic supply and U2202B and Q2201 for the –2V A/D reference supply.

DIGITAL TIME BASE

An accurate frequency source for synchronizing the Microprocessor with the other digital devices on the bus is provided by the Digital Time Base on Diagram 17.

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Clock Generator

Accurate clock signals are needed to transfer the data and to control the timing of each operation. The main clocking signals are produced by an oscillator and clock generator circuit. A 100 MHz signal is produced by crystal oscillator Y4100. The 100 MHz signal clocks all the flip-flops in the Clock Generator, setting the clock edge timing of all the other clocks.

The prescaler U4100A divides the 100 MHz input clock appropriately in conjunction with U4101, and U4102 to provide a 13.4MHz clock to the Microprocessor circuitry.

The 100 MHz outputs clock the acquisition system. Appropriate phasing is used to provide clocks to the Analog-to-Digital Conversion modules, and Digital Acquisition as ADCLK, SHCLK, and MCLK differential signals. In order to adjust timing variations of digital acquisition chips, DL4100 and the associated jumper J4101 are provided. These will not normally require adjustment outside of the factory.

Time Base Mode Registers

The Microprocessor controls the Digital Time Base via the Time Base Mode Registers, U4119 and U4120. These registers are used to set the appropriate trigger sources, or calibration sources, depending on the time base mode.

Clock Delay Timer

The circuitry forming the Clock Delay Timer is used only during equivalent-time sampling (0.5 μs/div to 0.05 μs/div). The purpose of the timer is to determine the time interval between the trigger event and the next rising edge of the SHCLK signal. The Microprocessor must know the information to place the data samples into the correct locations in Display Memory. Since the trigger is asynchronous to the clock, no fixed timing relationship exist between the trigger and the data samples taken as a result of the trigger. Therefore the relationship must be determined for each trigger in equivalent-time sampling.

The timer is formed by a dual-slope capacitor charging circuit. A fast- charging current source composed of Q4203 and Q4204 charges capacitor C4201 when FET Q4207 is turned off, removing its shunting effect (short) from the capacitor. If a STORE mode trigger is enabled (by prefull generated from the Digital Acquisition IC), Q4207 is held off to allow C4201 to charge. The fast-charging current source through Q4204 is then shut off by the second rising edge of the SHCLK rate signal putting a LO onto the $\overline{Q}$ output of flip-flop U4226B. The LO turns Q4203 on and shuts off the fast-charging current source, Q4204.

A slow-charging current source (Q4205 and associated resistors) then begins discharging C4201 towards the -8.6 V supply through Q4205 and R4212. This discharge path has a long time constant so that the discharge time is much longer than the capacitor's charge time. The voltage on C4201 is applied to the inverting input of comparator U4229. A comparison voltage with a threshold of about 0.6 V is on the noninverting input of the comparator.

When the capacitor's voltage drops to the comparison voltage, the output of the comparator goes HI. That HI is sent to the digital acquisition system, where a counter measures the total time to cycle the ramp.

In order for the Microprocessor to place the data samples into the correct display locations, the Microprocessor needs to know the maximum and minimum counts produced by the Clock Delay Timer. A calibration routine is activated when the SEC/DIV switch is changed. The calibration routine determines the maximum and minimum counts and calculates the calibration constant used by the equivalent-time sampling firmware using appropriate selections on U4104 and U4227.

The calibration routine initiated by the Microprocessor writes a byte to U4119 pin 11 via MODE(L) signal line. U4119 Pin 13 CALTIMER(L) goes low enabling 100 MHz clock to pass through multiplexer U4227 and clock U4228A, producing a trigger. When a test bit at U4119 pin 15 is low, the trigger passes through both U4228A and B, inserting a one clock period delay in the path generating SYNTRIG, the synchronized trigger. The corresponding value of the clock interpolator counter in the Digital Acquisition IC corresponds to the maximum count possible during an acquisition. The processor than sets the test bit low and initiates another acquisition. This cause U4228B to be held set, and the delay in the STBTRIG path is reduced by one clock period. The microprocessor interprets the value of the clock interpolator counter as the minimum count. After the calibration cycle, the normal acquisitions are processed using the maximum count and minimum count values to calculate the address offset of the acquisition samples.

DIGITAL DISPLAY

A custom LSI integrated circuit (Diagram 16) controls the stored waveform and readout displays. Two 32K x 8-bit static random-access memories (RAM), U9231 and U9232, make up the Display Memory. U9231 provides

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32K × 8-bit waveform data, and U9232 holds the 32K × 8-bit waveform-attribute data. Waveform data may be stored in the RAM from data on the Microprocessor bus or data may be read from the RAM and transferred to a Communication Option. For waveform displays, data is read from the RAM (display memory) by the display controller. The display controller then processes the data, and then drives the Vertical (Y) and Horizontal (X) digital-to-analog converters (DAC) where the data is converted to analog voltages used to drive the X- and Y-Axis vector generators.

Data Transceivers

Communication between the Microprocessor and the display memory is via two bus transceivers, U9206 and U9207. Waveform data from the Acquisition Memory is transferred to the display memory where the data is always available to the Display Controller for refreshing the display. The data transceivers are enabled by logic gating in U9211 that decodes the A14 and A15 signals from the Microprocessor and the PROC_EN(L) signal from the Display Controller to determine when a transfer is possible. The direction of transfer is controlled by the BWE(L) and BRD(L) signals from the Microprocessor via U9115. The BWE(L) and BRD(L) signals also enable U9211 to allow either a read from memory (for outputting data) or a write to memory (for transferring in the data from the Acquisition Memory). Bus transceiver U9206 is enabled for data transfers to U9321; transceiver U9207 is enabled for data transfers to U9232.

Address Decoder

To access a byte in RAM, the lower 8 bits of the address followed by the upper 6 bits of the address is applied. The lower and upper memory addresses are written together as one address word from the Microprocessor. Address multiplexers U9204 and U9205 are switched by the ROW/COL(L) signal from the Display Controller to select either the lower row address or the upper column address from the Microprocessor address bus. The Display Controller RAS(L) and CAS(L) signals (inverted by U9116E and F) enable the address latches U9202 and U9203, to latch the selected row and column addresses. The Display Controller has direct access to addresses in the RAM using the RA bus. The row address is applied on RA0-RA7, then the column address is applied on RA1-RA6 and RA14.

RAM

Two 32K by 8-bit memories make up the display RAM. The 8-bit waveform bytes are stored in U9231. The remaining RAM, U9232, stores attribute bits that are used to define the waveform point intensity and mark the end of the record. The data stored in the Display Memory is either readout characters or waveforms. The microprocessor also uses the display memory for operational data storage. In either case a 9-byte field-attribute preamble is read first. The preamble defines the data type and sets up the display attributes. Readout information is displayed using short vector X-Y displays positioned to specified field locations.

Display Controller

The Display Controller, U9208, runs the display system for the STORE waveform and STORE and NON-STORE readout displays. It takes control of the RAM to read the waveform or readout data. Besides the waveform data, the Display Controller runs the Store Z-Axis, selects the type of display (vector, dots, or X-Y plotter output), and drives the horizontal and vertical channel switches.

When reading data out of the RAM, the Display Controller has direct access to the memory address bus (RA). RAM row and column addresses to be read from are sequenced through in order.

When the Display Controller has completed a display frame, it signals the Microprocessor (using the DISPINTR(L) signal from U9208 pin 6) that the last field is finished and waits for the next frame request. After the interrupt is received, the Microprocessor can request the next frame (FRAME(L)), then the Display Controller resumes control of the RAM for the next frame of data. When RAMSEG(L) to U9208 pin 3 is HI, the Display Controller is in the middle of a display cycle and the Microprocessor is denied access to the display RAM. The Microprocessor can request access to the Display RAM using the RAMSEG(L) signal line to either write in new waveform data or read out data for the Communication Option. The Display Controller allows the Microprocessor to access the display RAM by setting the PROC_EN(L) (U9208 pin 5) signal line LO. A LO PROC_EN(L) signal enables the circuitry that allows the BWE(L), BRD(L), A14, and A15 signals, from the Microprocessor, to control the display RAM. Even though the memory addresses are under control of the Microprocessor, the inverted RAS and CAS signals are generated by the Display Controller.

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YDAC and XDAC

Data from Display Controller U9208 is applied to X- and Y-axis DACs U9210 and U9220. These DACs are biased to provide output currents (approximately 0 to 2 mA) proportional to the digital data. Potentiometers R9214 and R9224 aligns the storage signals on the crt. The DAC currents along with various control signals are applied to the Vector Generator.

VECTOR GENERATOR

Vector Generators

Vector Generator circuitry is shown on Diagram 19. U6303 and U6304 convert the DAC currents into bipolar voltages (approximately −2.5 V to +2.5 V) which are applied to sample and hold circuits U6305 and U6306. Outputs of the sample and hold circuits are applied to integrator stages U6307 and U6308 through electronic switches in U6301A and C. The integrator output signals are continuously fed back to the sample and hold inputs, causing these input voltages to be equal to the difference between the drive inputs and the integrator outputs. When the vector sample (VECT_SMPL(L) control line (via U6315A and B) is actuated, the outputs of the sample and hold circuits store these difference signals. Since the integrator output slopes are proportional to these signals, the net result is to effectively connect the dots which are equivalent to the digital data values.

These circuits also have a dot mode available so that the integrator outputs are stepped (dots) rather than continuous (vectors). When the VECT/DOT(L) signal is LO, U6301A and C switch the integrator inputs directly to the difference signals while also disconnecting the integration capacitors C6315 and C6314. The feedback loops are thus closed continuously, resulting in normal amplifier action.

Although the Vertical and Horizontal vector generators operate the same, there are some differences between the circuits and between their signal characteristics. To end up with the proper signal polarities at the crt, current on the X VECT line from X DAC circuit (Horizontal) is from 2 mA to 0 mA, while the current on the Y VECT line from Y DAC circuit (Vertical) is from 0 mA to 2 mA. Also, the vertical integrator output is −2 V to +2 V while the horizontal integrator output is −2.5 V to +2.5 V. The reduced vertical dynamic range allows proper interface to the main deflection system. Since the vertical signal eventually passes through the vertical delay line before reaching the crt, it is necessary to delay the horizontal signal as well. This is done in the vector mode by slightly delaying the vector sample signal applied to U6306 via R6320 and C6312 at pin 4 of U6315B. In the dot mode the crt beam is blanked during the transitions so the dots are only displayed after the signals have arrived and settled.

INPUT AMPLIFIER. The Y-axis (vertical) current from the D/A Converter goes to the inverting input of operational amplifier U6303. The amplifier is biased to produce a bipolar output voltage, from −2.5 V to +2.5 V, that is proportional to the input current. Negative feedback from the parallel combination of R6303 and C6311 stabilizes the amplifier.

Biasing of the non-inverting input of both the X-axis and the Y-axis amplifiers is identical and supplied by a resistive divider formed by R6304 and R6305 between ground and the +5 V reference. Both resistors are equal value to produce a bias voltage of +2.5 V. Resistor R6308 provides a summing node for the input vector current and the feedback current and develops the voltage on the inverting input of U6303. Full current range of the vector signal is from 0 to 2 mA. With no vector current in, the feedback current supplies the full current through R6308, and the output voltage of U6303 goes to −2.5 V. At maximum vector current input, the sum of the current through R3608 must remain the same as with no vector current; therefore, the feedback current is reduced by the amount of the vector current, and the output voltage goes to +2.5 V.

SAMPLE-AND-HOLD. The voltage output of U6303 is applied via R6309 to sample-and-hold circuit U6305. Sample-and-Hold (S/H) switching is controlled by the VECT_SMPL(L) signal from the Display Controller applied to U6305 pin 14 via U6315A. That signal in turn is controlled by the PLT_EN(L) signal (U6301B pin 9) that switches section B of multiplexer U6301. When displaying storage waveforms and readout characters, the PLT_EN(L) signal is not active, and the VECT_SMPL(L) signal is switched to control the S/H circuit. For producing X-Y Plots, U6301C is activated, and the VECT_SMPL(L) signal drives the X-Y Plotter Pen-Down circuit (shown on Diagram 21).

SAMPLE INTEGRATOR. During digital storage waveform displays, the S/H circuit and the Y-Integrating circuit formed by U6307 and associated components produce either vectors or dots. When U6301C connects pin 13 to pin 14, U6307 integrates each step output of the S/H circuit into a smooth ramp signal. This integrated signal is the vertical deflection signal (still single-ended) that connects the data points of the stored waveform display. When the user selects either dot displays or X-Y Mode, multiplexer U6301C connects pin 12 to pin 14. The long time constant integrating function of

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U6308 is switched out, and U6307 acts as an amplifier only for the voltage being held by the S/H circuit, causing the crt display to be dots. For readout character displays both during STORE and NONSTORE modes, the S/H and integrator work only in the vector mode because readout characters are vector displays.

The integrator output is subtracted from the input voltage at all times. When VECT_SMPL(L) goes LO, the difference value is sampled and held by S/H U6305. The held voltage value sets the slope of the integrator and effectively connects the dots since the slope of the output vector is proportional to the difference between the input voltage and the output voltage of the integrator.

Diode clamps CR6301, CR6303, CR6305, and CR6307 prevent voltage transients that could cause U6301C latch up.

Vector Amplifiers

The integrator outputs are applied to vector amplifiers U6401 and U6402, which are differential voltage-to-current converters. Their outputs are differential currents which are sent to the main deflection multiplex circuitry via J6100. Vertical positioning information is processed by display controller U9208 on diagram 16, but horizontal position information is not. Therefore, the horizontal position voltage is applied to U6402D to affect horizontal position control of stored waveforms. At times when readout characters are being drawn, this position signal is shunted by transistor U6403A to reduce the positioning effect on the characters. This action is controlled by the HPOS_DIS(L) signal from the display controller.

Plot Drive

When plot mode is on, the display controller activates the PLT_EN(L) signal, causing U6301B to apply the VECT_SMPL(L) signal to the PEN_DN(L) line via U6404A and U6402E, and the display controller internal modes change so that VECT_SMPL(L) provides the pen down control function. The PEN_DN(L) signal is sent via J6100 to the Z-axis section and to the X-Y board or installed communication option board. When U6301B activates plot mode, U6315A and B pull the sample control lines of U6305 and U6306 HI putting them in tracking mode. This closes the vector generator feedback loops regardless of vector/dot mode selection. The PLT_EN(L) signal also turns on operational transconductance amplifiers U6404A, B, and C via transistor U6403E. Normally, their outputs are off, and the plotter signals are zero (held at ground by R6433, R6434). In plot mode, the X_PLOT, Y_PLOT, and PEN_ON(L) lines turn on and act as voltage followers for the vector signals. The Y amplifier input is connected ahead of the Y vector generator to preserve the ±2.5 V range and correct polarity. The X_PLOT and Y_PLOT signals are sent via J6100 to the X-Y board or installed communication option board.

Readout Off Detector

To detect when the STORE/READOUT INTENSITY knob is at its counter clockwise end, U6405A (Diagram 19) monitors the readout (RO) voltage from J6100. Since RO voltage is normally negative, but goes slightly positive at the end of its rotation, U6405A output will go positive, turning on transistor U6403B, causing the NORO line to be LO. This signal is sent to the Instrument Status Port (Diagram 18) as status information.

Signal Conditioning

The signals ARES1, ARES2, B_RES, and B_CAPS on J6100 from the Sweep Interface board are encoded analog currents which contain most of the information about the positions of the A and B Timing switches. Since the sum of the possible changes in these currents is larger than U6302 (5VREFB) can accommodate, U6405B (Diagram 20) is used to buffer the 5V reference to supply the termination resistors (Diagram 18). As these currents change, the resulting voltages are measured by the Status ADC and Bus Interface so that the Microprocessor can determine the state of the timing switch.

+5 VOLT REFERENCE. The 5 Volt Reference (5VREFC) is generated by U6302. It is used by the vector generator circuits, status A/D circuit, display DAC circuit, and acquisition system. Associated with each of these circuits is a local pull-up resistor from the +8.6VA supply to the 5VREFC line to supply nominal load current so that U6302 does not have to supply the total load current. This also greatly reduces the reference line current which could cause excessive voltage drops at the far ends of its travel.

DIGITAL ACQUISITION AND MEMORY

Diagram 15 shows the Digital Acquisition and Memory system. The functional blocks are the Digital Acquisition IC, the Acquisition Memory, Microprocessor Access, and External Clock Divider.

The Digital Acquisition IC, U4000, is a CMOS VLSI circuit containing acquisition data processors for two input channels, acquisition address counter, trigger position

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counters, equivalent time interpolator counter, post trigger address counter, acquisition control state machines, mode registers, and microprocessor interface. All operations within the IC are synchronized to the 100 MHz differential clock inputs MCLK and MCLK(L). U4000 is initialized on power up when RESET (pin 121) is driven high.

Data from the A/D converter modules is continuously applied to the Digital Acquisition IC on the AAD and ABD buses. The acquisition data is clocked into the input registers on U4000 at the clock rate of the MCLK signal line. The acquisition data is demultiplexed within U4000 and written into the Acquisition Memory ICs at a rate determined by the A or B SEC/DIV switch setting. The maximum acquisition memory write cycle rate is 25 MHz.

For A or B SEC/DIV settings of 50 ms to .05 μs, record acquisition mode is used. To initiate a record mode acquisition, the microprocessor writes into the U4000 control registers via the data bus transceiver U4001, address bus A(0..17), and control lines ACQSEG(L) and BWE(L). At the beginning of the acquisition cycle, pre-trigger data is transferred through U4000 to the Acquisition Memory. Data from both channels is written simultaneously into the Acquisition Memory using the AM1D and AM2D buses. The acquisition data is stored as consecutive samples in SAMPLE or AVERAGE acquisition mode or as min/max pairs in PEAKDET or ACCPEAK acquisition mode. The acquisition address is applied to the acquisition memory over the AMA bus.

Data on the AM1D and AM2D buses is latched in the acquisition memory when the AMWE strobe goes low. When the pre-trigger portion of the record is complete, EPTHO(L) goes low, enabling the trigger circuit. When a trigger is accepted, SYNTRIG goes high and the acquisition continues until the post-trigger data record is complete, then ACQINTR(L) goes low, generating an interrupt to the microprocessor. After processing the interrupt, the microprocessor reads the acquisition memory by outputting an address on A(0..17), and driving ACQSEG(L) and BRD(L) low. Address lines A(2..12) are buffered by U3400 and U3401A which drives the Acquisition Memory address lines during a microprocessor access cycle. The Digital Acquisition IC drives UPADBEN low enabling the Acquisition Memory to drive the AM1D and AM2D data buses. The memory byte selected by A(0..2) is routed through U4000 and is read by the microprocessor on the D(0..7) data bus.

For A SEC/DIV settings from 5 sec to 0.1 sec, SCAN or ROLL acquisition mode may be menu selected. An interrupt to the microprocessor occurs each time a word (8 bytes) is written into the Acquisition Memory. In SGL SWP or NORM trigger mode, an interrupt is also generated at the end of the acquisition record.

For A or B SEC/DIV settings from 0.5 μs to 0.05 μs, REPETITIVE storage mode is used. The Time Base Interpolator Counter in the Digital Acquisition chip counts MCLK cycles beginning with the rising edge of SYNTRIG and ending with the rising edge of TBICSTP. The count value is used as an address offset to correctly position the acquisition record in display memory.

The external clock divider routes the external clock signal directly to the Digital Acquisition chip in SAMPLE or AVERAGE acquisition mode or divides the external clock by 2 in PEAKDET and ACCPEAK modes. This selection is controlled by the EXTSMP signal.

U3401B is a status input port to the microprocessor. When ACQSTAT(L) is low the microprocessor reads the state of TOK(L), and the configuration jumpers W3400, W3401, and W3402.

POWER INPUT, PREREGULATOR AND INVERTER

The Power Supply (see Diagram 8 and Diagram 9) changes the ac power-line voltage into the voltages needed for instrument operation. It consists of the Power Input, Preregulator, and Inverter circuits (which drive the primary of the power transformer) and secondary circuits (which produce the necessary supply voltages for the instrument). Refer to Figure 3-8 for a block diagram of the Power Supply.

Power Input

The Power Input circuit changes the ac power-line voltage to filtered dc for use by the Preregulator.

POWER switch S901 connects the ac power line through fuse F9001 to bridge rectifier CR901. The full-wave bridge rectifies the source voltage, and the output is filtered by C906. Input surge current at instrument power-on is limited by thermistors RT901 and RT906. The thermistors' resistances are moderately high when the power is first turned on, but decrease as the input current warms the device.The instrument is protected from large voltage transients by suppressor VR901. Conducted interference originating within the power supply is attenuated by common-mode transformer T901, differential-mode transformer T903, line filter FL9001, and capacitors C900, C902, and C903.

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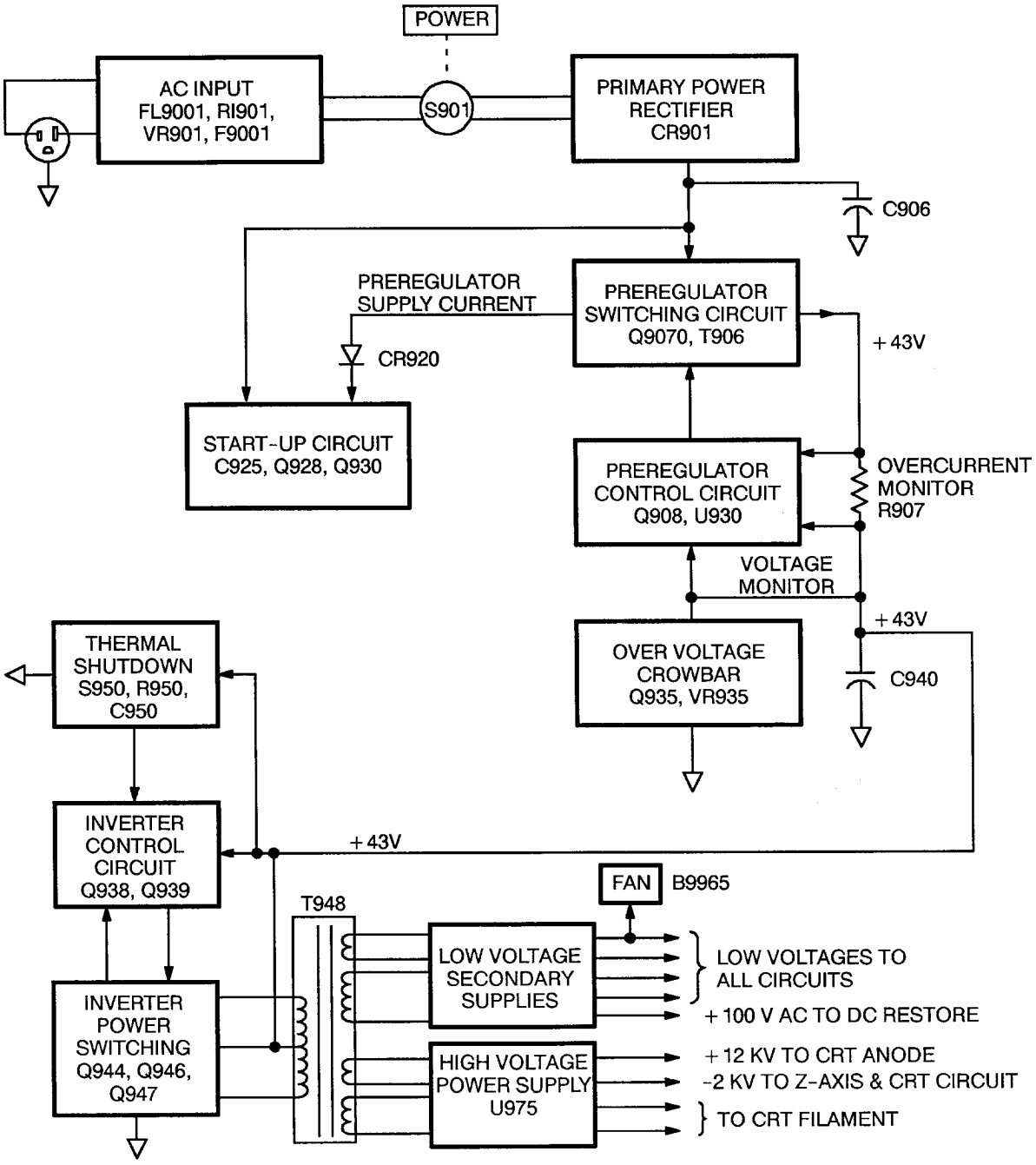


Figure 3–8. Power Supply block diagram.

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Preregulator

The Preregulator provides a regulated dc output voltage for use by the Inverter circuitry.

When the instrument is turned on, the voltage developed across C906 charges C925 through R926. When the voltage across C925 has risen to a level high enough that Pulse-Width Modulator U930 can reliably drive Q9070, U930 receives operating supply voltage through Q930. This voltage level is set by zener diode VR925 in the emitter of Q928 and by the voltage divider formed by R925 and R927. The zener diode keeps Q928 biased off until the base voltage reaches approximately 6.9 V. At that point, Q928 is biased into conduction, and the resulting collector current causes a voltage drop across R929 that biases on Q930. The positive feedback through R930 reinforces the turn-on of Q928, which quickly drives both Q928 and Q930 into saturation. Once Q930 is on, the Pulse-Width Modulator begins to function.

Pulse-Width Modulator U930 controls the output voltage of the Preregulator by regulating the duty cycle of the pulse going to the gate of Q9070. The modulator has an oscillator that operates at a frequency set by R919 and C919 (approximately 60 kHz). A sawtooth voltage produced at pin 5 of U930 is compared internally with the output voltage produced by the two internal error amplifiers. Whenever the sawtooth voltage is greater than the error amplifier output voltage, Q9070 is biased on to supply current to the remaining portions of the switching circuitry and charge C940. The two error amplifiers maintain a constant output voltage and monitor the output current of the Preregulator. One input of each amplifier is connected through a divider network to the IC internal +5 V reference. The output voltage of the Preregulator is monitored by the voltage divider at pin 2. The voltage drop across R907, produced by the Preregulator output current, is applied to the internal current-limit amplifier at pin 16.

When the instrument is first turned on, the current-limit amplifier controls the conduction time of Q9070. While Q9070 is conducting, the output current increases until a voltage large enough to permit the current-limit circuitry to function is developed across R907. The current-limit amplifier then holds the output current below the limiting thresh old of approximately 1 A. When the voltage across C940 reaches approximately 43 V, the internal voltage amplifier starts controlling the duty cycle of Q9070, and the Preregulator will not limit current unless there is excessive current demand.

With Q9070 off, C907 charges to the output voltage of the Power Input circuit. When Q9070 turns on, current through the FET comes from the winding connected to pins 1 and 2 of T906 and from C907. Current to C907 is supplied by the winding connected to pins 4 and 5 of T906. When U930 shuts off Q9070, the collapsing magnetic field raises the voltage at the anode of CR907. This diode then becomes forward biased and passes the currents supplied by C907 and the winding connected to pins 4 and 5 of T906. For this part of the cycle, current to C907 is supplied by the winding connected to pins 1 and 2 of T906. This process continues for each period of the oscillator, and the duty cycle controlling the conduction period of Q9070 is altered as necessary to maintain 43 V across C940. During each oscillator period, Q908 is used to discharge the gate-drain capacitance of Q9070. At the shutoff point, Pin 10 of U930 goes LO to reverse bias CR908 and turn on Q908 to switch off the FET.

Once the supply is running, power to U930 is supplied from the winding connected to pins 6 and 7 of T906. Diode CR920 half-wave rectifies the voltage across pins 6 and 7 to keep filter capacitor C925 charged and to maintain supply voltage to U930 through Q930.

Instrument protection from excessive output voltage is supplied by silicon-controlled rectifier Q935. Should the Preregulator output voltage exceed 51 V, zener diode VR935 conducts, causing Q935 to also conduct. The Preregulator output current is then shunted through Q935, and the output voltage quickly drops to zero. With the 43 V rail clamped to 0 V, U930 senses an overcurrent condition and shuts down the drive to Q9070, the Preregulator shuts down, and Q935 becomes reset. The supply then attempts to power up, but it will shut down again if the overvoltage condition reoccurs. This sequence continues until the overvoltage condition is corrected. A thermal shutdown circuit is included to protect the instrument from damage in case of fan failure or air flow restriction at high ambient temperatures. Overheating causes thermal switch S950 to close, stealing drive from inverter base driver Q944, thus reducing total power dissipation. To reset the circuit, remove the cause of the temperature fault.

Inverter

The Inverter circuit changes the dc voltage from the Preregulator to ac for use by the supplies that are connected to the secondaries of T948.

The output of the Preregulator circuit is applied to the center tap of T948. Power-switching transistors Q946 and Q947 alternate conducting current from the Preregulator output through the primary windings of

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T948. The transistor switching action is controlled by T944, a saturating base-drive transformer.

When the instrument is first turned on, one or the other of the switching transistors starts to conduct. As the collector voltage of the conducting transistor drops toward the common voltage level, a positive voltage is induced from T944 to the base of the conducting transistor that reinforces conduction. Eventually T944 saturates; and, as the voltage across T944 (and T948) begins to reverse, the conducting transistor is cut off by the drop in base drive. The other transistor does not start conduction until the voltage on the leads of T944 reverse enough to bias it on. The saturation time of T944 plus the transistor-switching time determine the frequency of Inverter operation (typically about 20 kHz). After the initial Inverter start up, the switching transistors do not saturate; they remain in the active region during switching.

Diodes CR946 and CR947 serve as a negative-peak detector to generate a voltage for controlling the output of the error amplifier. Capacitor C943 charges to a voltage equal to the negative peak voltage at the collectors of Q946 and Q947, referenced to the Preregulator input voltage. This voltage level is applied to the divider formed by R937, R938, and R939. The error amplifier, formed by Q938 and Q939, is a differential amplifier that compares the reference voltage of VR943 with the wiper voltage of potentiometer R938. The current through Q939 sets the base drive of Q944 and, thereby, controls the voltage on C944. This voltage biases Q946 and Q947 to a level that maintains the peak-to-peak input voltage of T948. The amplitude of the voltage across the transformer primary winding, and thus that of the secondary voltages of T948, is set by adjusting 8.6V ADJ potentiometer R938.

At turn-on, Q938 is biased off, and Q939 is biased on. All the current of the error amplifier then goes through Q939 to bias on Q944. The current through Q944 controls the base drive for Q946 and Q947. Base current provided by base-drive transformer T944 charges C944 negative with respect to the Inverter circuit floating ground (common) level.

To safeguard against an inverter fault which could cause overvoltage at the secondaries, R949 senses the current drive in Q946 and Q947 and feeds back a voltage to the SCR crowbar. CR948, R948, and R935 level shift the feedback voltage and set the trip point for SCR Q935.

POWER SUPPLY SECONDARIES, Z-AXIS AND CRT

XFMER and LV Power Supplies

The Low-Voltage supplies, shown on Diagram 9, use center-tapped secondary windings of T948 (XFMR). The +100 V supply is rectified by CR954 and CR955 and filtered by C954. Diodes CR956 and CR957 rectify ac from taps on the 100 V winding, and C956 filters the output to produce +30 V dc. The full-wave diode bridge formed by CR960, CR961, CR962, and CR963 produces the +8.6 V and -8.6 V supplies. Filtering of the +8.6 V is done by C960, L960, and C962. Filtering of the -8.6 V is done by C961, L961, and C963. Ac voltage from the 8.6 V primary is rectified by CR965 and CR967, and then filtered by C965 and R965 to provide the fan power source. The +5 V supply is produced by CR970, C968, L968, C958 and C970. The -5 V supply is produced by CR980, CR981, C964, L962, and C959.

Unblanking Logic, Intensity, and Z-Axis Ampl

The Z-Axis Amplifier controls the crt intensity level via several input-signal sources. The effect of these input signals is either to increase or decrease trace intensity or to completely blank portions of the display. The Nonstore Z-Axis drive signal currents, as set by the A and B Z-Axis switching logic and the input current from the EXT Z AXIS INPUT connector (if in use), are summed at the emitter of common-base amplifier Q825. The total sets the collector current of the stage. The common-base amplifier provides a low-impedance termination for the input signals and isolates the signal sources from the rest of the Z-Axis Amplifier.

For the Nonstore Z-Axis signals, common-base transistor Q829 passes a constant current through R832. This current is divided between Q825 and Q829, with the portion through Q829 driving the shunt-feedback output amplifier formed by Q835, Q840, and Q845. Therefore, the bias level of Q825 controls the emitter current available to Q829. Feedback-resistor R841 sets the transresistance gain for changing the input current to a proportional output voltage. Emitter-follower Q835 is dc coupled to Q840, and for low-speed signals, Q845 acts as a current source. Fast transitions couple through C845, providing added current gain through Q845 for fast voltage swings at the output of the Amplifier.

Store Z-Axis signals, controlled by the Display Controller (Diagram 16), are applied to the Z-Axis amplifier at the emitter of Q829. The Nonstore Z-Axis signals are shunted away from Q829 by CR824, which is forward

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biased from the CHOP Blanking circuit (Diagram 2) during STORE mode displays. The overall store waveform and readout character intensity level is set by the STORAGE/READOUT INTENSITY control. The level setting of that control sets the Z-Axis drive current supplied to the Z-Axis Amplifier by Q829 during digitally controlled displays. When the Display Controller turns off Q7203, Q7202, or Q7201, the current normally shunted away from the emitter of Q829 is added via the forward biased diode connected to the emitter of the cutoff transistor. With more current available from Q7204, more current flows in Q829 to intensify the crt display.

The intensity of the Nonstore crt display in the A, B, and Alt Horizontal modes is set by the INTENSITY controls and associated circuitry. The A INTENSITY potentiometer controls the base voltage of Q804 to set the amount of emitter current that flows through that transistor and, therefore, the level of the Z-Axis signal. Likewise the B INTENSITY potentiometer controls the base voltage of Q814 and the intensity of the B and Alt Sweep displays.

When only the Nonstore A Sweep is displayed, Q586 and Q583 are biased off. The current through R818, set by the A INTENSITY potentiometer, flows through CR818 and Q825 to fix the voltage level at the Z-Axis Amplifier output. For a B-Only display, Q586 is biased on to reverse bias CR818 and prevent A-Intensity current from reaching Q825. Current set by the base voltage of Q814 flows through CR817 to Q825 and sets the B Sweep intensity. For an alternating A and B display, Q586 is biased off when the A Sweep is displayed. During the portion of the A Sweep in which the B Sweep runs, current from R816 is passed through CR816 by the Alternate Display Switching and the Unblanking Logic circuitry to produce an intensified zone on the A Sweep trace.

When CHOP VERTICAL MODE is selected, the Chop Blanking signal is sent to the collector of Q825 through U537B and CR824 during the Nonstore display-switching time. Signal current is shunted away from CR825, and the forward bias of Q829 rises to the blanking level. When blanked, the output of the Z-Axis Amplifier drops to reduce the crt beam current below viewing intensity.

For a Nonstore X-Y display, CR818, CR817, and CR816 are reverse biased. The XY signal is LO to reverse bias CR551 and allow current in R820 to flow through CR820. The crt intensity is then controlled by the A INTENSITY potentiometer which sets the current in R820 through Q804.

During Nonstore operation, any applied External Z-Axis input voltages drive proportional input currents through R822 and R823 to the Z-Axis Amplifier. Sensitivity to external signals is determined by the transresistance gain of the shunt-feedback amplifier. Diode CR823 protects the Z-Axis Amplifier if excessive voltage levels are applied to the EXT Z AXIS INPUT connector. External Z-Axis modulation does not function for STORE MODE displays.

BEAM FIND switch S390 controls the base bias voltages of Q825 and Q829. When the BEAM FIND button is out, 8.6 V is supplied to the normal base-biasing network. When the button is held in, the 8.6 V supply is removed, and the voltage at the anode of VR828 rises to about 5.6 V. This voltage level turns off the current supply from Q829. The Z-Axis amplifier output voltage is then fixed by R835 and the voltage at the BEAM FIND switch, as set by other parts of the Beam Find circuitry. The output voltage of Q835 is set to a level that displays either a bright trace or dot (depending on whether the sweep is triggered or not), and the INTENSITY controls and the Z-Axis drive signals have no control over the crt intensity.

Hv Multiplier, Dc Restorer, and Crt

The Dc Restorer circuit sets the crt control-grid bias and couples the ac and dc components of the Z-Axis Amplifier output to the crt control grid. Direct coupling of the Z-Axis Amplifier output to the crt control grid is not employed due to the high potential differences involved. Refer to Figure 3-9 during the following discussion.

Ac drive to the Dc Restorer circuit is obtained from pin 16 of T948. The drive voltage has a peak amplitude of about 100 V at a frequency of about 20 kHz and is coupled into the Dc Restorer circuit through C853 and R853. The cathode of CR851 is biased by the wiper voltage of Grid Bias potentiometer R851, and the ac-drive voltage is clamped whenever the positive peaks reach a level that forward biases CR851.

The Z-Axis Amplifier output voltage, which varies between +10 V and +75 V, is applied to the Dc Restorer at the anode of CR853. The ac-drive voltage holds CR853 reverse biased until the voltage falls below the Z-Axis Amplifier output voltage level. At that point, CR853 becomes forward biased and clamps the junction of CR851, CR853, and R854 to the Z-Axis output level. Thus, the ac-drive voltage is clamped at two levels to produce a square-wave signal with a positive dc-offset level.

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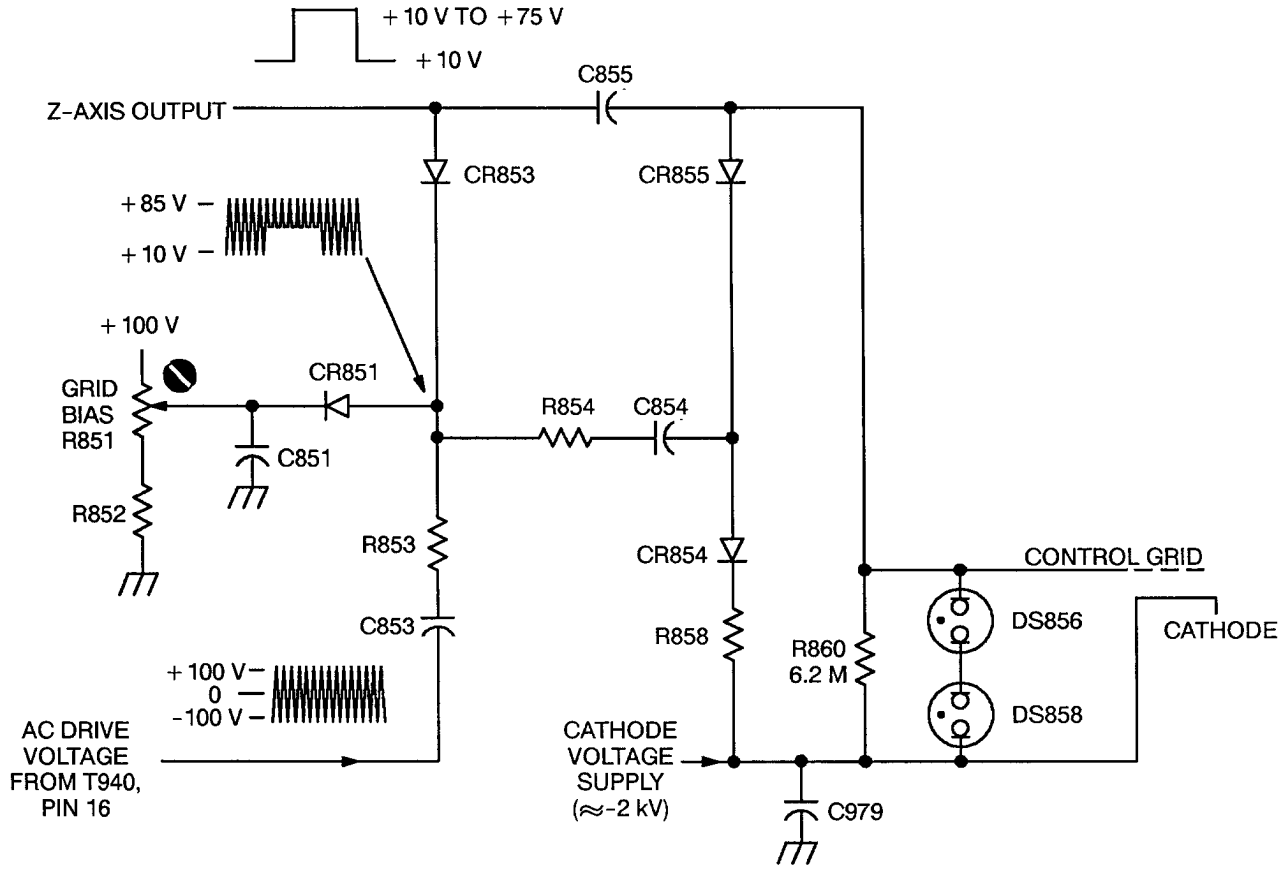


Figure 3-9. Simplified diagram of the Dc Restorer circuitry.

The Dc Restorer is referenced to the 2 kV crt cathode voltage through R858 and CR854. Initially, both C855 and C854 charge up to a level determined by the difference between the Z-Axis output voltage and the crt cathode voltage. Capacitor C855 charges from the Z-Axis output through R858, CR854, and CR855, to the crt cathode. Capacitor C854 charges through R858, CR854, R854, and CR853 to the crt cathode.

During the positive transitions of the ac drive, from the lower clamped level toward the higher clamped level, the charge on C854 increases due to the rising voltage. The voltage increase across C854 is equal to the amplitude of the positive transition. The negative transition is coupled through C854 to reverse bias CR854 and to forward bias CR855. The increased charge of C854 is then transferred to C855 as C854 discharges toward the Z-Axis output level. Successive cycles of the ac input to the Dc Restorer charge C855 to a voltage equal to the initial level plus the amplitude of the clamped square-wave input.

The charge held by C855 sets the control-grid bias voltage. If more charge is added to that already present on C855, the control grid becomes more negative, and less crt writing-beam current flows. Conversely, if less charge is added, the control-grid voltage level becomes closer to the cathode-voltage level, and more crt writing-beam current flows.

During periods that C854 is charging, the crt control-grid voltage is held constant by the long time-constant discharge path of C855 through R860.

Fast-rise and fast-fall transitions of the Z-Axis output signal are coupled to the crt control grid through C855 to start the crt writing-beam current toward the new intensity level. The Dc Restorer output level then follows the Z-Axis output-voltage level to set the new bias voltage for the crt control grid.

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Neon lamps DS858 and DS856 protect the crt from excessive grid-to-cathode voltage if the potential on either the control grid or the cathode is lost for any reason.

High-voltage multiplier U975 uses the 2-kV winding of T948 to generate 12 kV to drive the crt anode. An internal half-wave rectifier diode in the multiplier produces 2 kV for the crt cathode. The 2 kV supply is filtered by a low-pass filter formed by C975, C976, R976, R978, and C979. Neon lamp DS870 protects against excessive voltage between the crt heater and crt cathode by conducting if the voltage exceeds approximately 75 V.

Focus voltage is also developed from the 2 kV supply by a voltage divider formed by R894, R892, FOCUS potentiometer R893, R891, R890, R889, R888, and R886.

X-Y PLOTTER

The X-Y plotter circuitry (see Diagram 21) drives the internal circuitry for the external clock, and an external XY Plotter, if connected.

External Clock

The TTL compatible (active LO) EXT_CLK(L) signal, accessed through the AUXILIARY CONNECTOR (J1011 pin 1), drives the external clock circuitry (active HI) of the oscilloscope through internal connector J4110 pin 1.

Operational amplifier U1001A, PNP transistor Q1011, and associated components buffer and invert the external clock signal EXT_CLK(L). Input bias resistors R1011, R1014, and R1015 condition the EXT_CLK(L) input signal. The same three resistors protect the external clock circuitry from over-voltage and reverse-voltage inputs. Resistor R1016 provides hysteresis.

Operational amplifier U1001A serves as a buffer and amplifier. Even though EXT_CLK(L) only swings from 0 V to +5 V maximum, the input bias resistors produce plus and minus voltage swings of ≥ 2 V at non-inverting input U1001A pin 3. The amplifier output U1001A pin 1 has a plus and minus 7 V range which, through current limit resistor R1017, overdrives the base of Q1011. This base current overdrive assures a fast clean rise and fall time of the EXT_CLK output signal (J4110 pin 1) required by the oscilloscopes external clock circuit input.

The emitter of Q1011 goes to +5 V_K and the collector goes to both the EXT_CLK output and to level-shift resistor R1012. Level-shift resistor R1012 makes the EXT_CLK output a valid TTL LO when Q1011 is shut off. The EXT_CLK output is an active HI TTL drive.

Shield Ground

The SHIELD GND connection (J1011 pin 4) is the chassis ground connection for cable shield connections.

Signal Ground

The AUXILIARY CONNECTOR SIG_GND connection (J1011 pin 9) is the ground point for all signal path ground returns.

Pen-Down Circuit

The Pen-Down circuitry controls the pen mechanism of an external X-Y plotter or the motor drive of a Y-T strip chart recorder. The Pen-Down circuit is comprised of operational amplifier U1001B, transistor Q1012, relay K1001, and related components. The PEN_DN(L) signal (J6423 pin 1) drives the non-inverting input of the operational amplifier (U1001B pin 5). The inverting input of the operational amplifier (U1001B pin 6) is tied to ground. The operational amplifier output, U1001B pin 7, goes to the base of PNP relay-drive transistor Q1012, through current limiting resistor R1005. This amplifier has no negative feedback resistor and operates in an open-loop gain configuration. Small input signals therefore drive the output near one rail or the other. The output signal resembles a square wave, regardless of the input waveform.

Transistor Q1012 inverts the signal and drives relay K1001. Diode CR1016 protects the transistor from inductive kick-back voltages generated by the relay's collapsing magnetic field as the transistor turns off. Fuse F1001, in the RELAY COMM signal path, provides over-current protection for all relay contact configurations.

When the PEN_DN(L) signal on U1001B pin 5 goes negative, the output on pin 7 of the operational amplifier also goes negative, turning on transistor Q1012 and energizing the relay coil. When the relay is energized, the relay common to normally closed connection opens and the relay common to normally open connection closes. When PEN_DN(L) returns to a positive level, the transistor shuts off. The relay's coil discharges its kick-back current through diode CR1016, and the relay common returns to its normally closed position.

In order to drive both an X-Y plotter and a Y-T strip chart recorder, the Pen-Down circuitry does double duty. With an X-Y plotter, the circuitry simply lowers the plotter pen. with a Y-T strip chart recorder, the pen-down circuitry is

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actually a motor drive control circuit. This double duty is accomplished by providing the Pen-Down signal to the operational amplifier about 1 s prior to the signals being provided to X & Y plot output circuitry. This allows the motor to have time to start up before signals are applied to the Y plot output circuit. The circuit can not differentiate between X-Y plotters and Y-T strip chart recorders, therefore the time delay from PEN_DN(L) to X and Y channel information output is the same in each case.

X and Y Amplifiers

The X and Y amplifiers drive the X and Y outputs. Because both amplifiers operate the same, only the X-PLOT amplifier is discussed in detail.

Input signal X_PLOT goes to the non-inverting input of unity gain amplifier U1001C pin 10. The output of the operational amplifier is fed to auxiliary connector J1011 pin 3 through resistor R1002. The resistor limits the output current and is part of the amplifier's protection network. The X_PLOT protection network consists of diodes CR1003, CR1011, R1002, VR1012, and VR1011. If the X output goes above 5.8 V peak, VR1011 and CR1011 turn on, clipping U1001C pin 8 to about +6 V. If output goes below -5.8 V peak, VR1012 and CR1003 turn on, clipping U1001C pin 8 to about -6 V. The Y_PLOT protection components are CR1001, CR1002, R1001, VR1012, and VR1011.

Power Supplies

The filters for all supplies are pi filters, consisting of two filter caps to ground, one on each side of a series choke.

Each filter circuit for the three supplies filter in both directions. The filters reduce noise on the power supply lines generated elsewhere in the instrument, and they also reduce noise generated by the X-Y plotter board as the noise goes back out to the supplies in the rest of the instrument. Capacitors C1003, C1004, and C1005 decouple and by-pass the supplies.

The +4.2 V output makes interfacing to various X-Y and Y-T devices easier. The +5 V_g goes to the anode of reverse voltage protection diode CR1014. The diode drops the voltage to +4.2 V. The +4.2 V goes through current limit resistor R1013 to the auxiliary connector output (J1011 pin 6).

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PERFORMANCE CHECK PROCEDURE

INTRODUCTION

PURPOSE

The Performance Check Procedure is used to verify the instrument's Performance Requirements statements listed in Table 1–1 and to determine the need for calibration. The performance checks may also be used as an acceptance test or as a preliminary troubleshooting aid.

PERFORMANCE CHECK INTERVAL

To ensure instrument accuracy, check its performance after every 2000 hours of operation or once each year, if used infrequently. A more frequent interval may be necessary, if the instrument is subjected to harsh environments or severe usage.

STRUCTURE

The Performance Check Procedure is structured in subsections to permit checking individual sections of the instrument, whenever a complete Performance Check is not required. At the beginning of each subsection there is an equipment–required list showing only the test equipment necessary for performing the steps in that subsection.

Also at the beginning of each subsection is a list of all the front–panel control settings required to prepare the instrument for performing Step 1 in that subsection. Each succeeding step within a particular subsection should then be performed, both in the sequence presented and in its entirety, to ensure that control–setting changes will be correct for ensuing steps.

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 4–1 is a complete list of the equipment required to accomplish the Performance Check Procedure in this section. Test equipment specifications described in Table 4–1 are the minimum necessary to provide accurate results. Therefore, equipment used must meet or exceed the listed specifications. Detailed operating instructions for test equipment are not given in this procedure. If more operating information is required, refer to the appropriate test equipment instruction manual.

When equipment other than that recommended is used, control settings of the test setup may need to be altered. If the exact item of equipment given as an example in Table 4–1 is not available, check the Minimum Specification column to determine if any other available test equipment might suffice to perform the check or adjustment.

LIMITS AND TOLERANCES

The tolerances given in this procedure are valid for an instrument that is operating in and has been previously calibrated in an ambient temperature between +20°C and +30°C. The instrument also must have had at least a 20–minute warm–up period. Refer to Table 1–1 for tolerances applicable to an instrument that is operating outside this temperature range. All tolerances specified are for the instrument only and do not include test–equipment error.

PREPARATION FOR CHECKS

It is not necessary to remove the instrument cover to accomplish any subsection in the Performance Check Procedure, since all checks are made using operator–accessible front– and rear–panel controls and connectors.

The most accurate display adjustments are made with a stable, well–focused, low–intensity display. Unless otherwise noted, adjust the A and B INTENSITY, STORAGE/READOUT INTENSITY, FOCUS, and TRIGGER LEVEL controls as needed to view the display.

To ensure performance accuracies stated in the Specification (Section 1), for the digital portion of the instrument, select the Factory Reset routine. The Factory Reset routine sets the digital part of the instrument to factory default settings.

To select the Factory Reset routine:

Press the ADV FUNCT SETUP button to display the Advanced Functions setup menu. Press Menu Item Select button to select Factory Reset. Return the instrument to display mode by pressing the ADV FUNCT SETUP button a second time.

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Table 4–1
Test Equipment Required

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
Calibration Generator	Standard–amplitude signal levels: 5 mV to 50 V. Accuracy ± 0.3%. High–amplitude signal levels: 1 V to 60 V. Repetition rate: 1 kHz. Fast–rise signal level: 1 V. Repetition rate: 1 MHz. Rise time: 1 ns or less. Flatness: ± 2%.	Signal source for gain and transient response.	TEKTRONIX PG 506A Calibration Generator.[a]
Leveled Sine–Wave Generator	Frequency: 250 kHz to above 100 MHz. Output amplitude: variable from 10 mV to 5 V p–p. Output impedance: 50 Ω. Reference frequency: 50 kHz. Amplitude accuracy: constant within 3% of reference frequency as output frequency changes.	Vertical, horizontal, and triggering checks and adjustments. Display adjustments and Z–Axis check.	TEKTRONIX SG 503 Leveled Sine–Wave Generator.[a]
Time–Mark Generator	Marker outputs: 10 ns to 0.5 s. Marker accuracy: ±0.1%. Trigger output: 1 ms to 0.1 ms, time–coincident with markers.	Horizontal checks and adjustments. Display adjustment.	TEKTRONIX TG 501 Time–Mark Generator.[a]
Low–Frequency Generator	Range: 1 kHz to 500 kHz. Output amplitude: 300 mV. Output impedance: 600 Ω. Reference frequency: constant within 0.3 dB of reference frequency as output frequency changes.	Low–frequency trigger checks.	TEKTRONIX SG 502 Oscillator.[a]
Pulse Generator	Repetition rate: 1 kHz. Output amplitude: 5 V.	External clock and storage checks	TEKTRONIX PG 501 Pulse Generator.[a]
Test Oscilloscope with 10X Probes	Bandwidth: dc to 100 MHz. Minimum deflection factor: 5 mV/div. Accuracy: ±3%.	General troubleshooting, holdoff check.	TEKTRONIX 2235A Oscilloscope.
Digital Voltmeter	Range: 0 to 140 V. Dc voltage accuracy: ±0.15%. 4 1/2 digit display.	Power supply checks and adjustments. Vertical adjustment.	TEKTRONIX DM 501A Digital Multimeter.[a]
Coaxial Cable (2 required)	Impedance: 50 Ω. Length: 42 in. Connectors: BNC	Signal interconnection.	Tektronix Part Number 012–0057–01.
Precision Coaxial Cable	Impedance: 50 Ω. Length: 36 in. Connectors: BNC.	Vertical bandwidth and aberrations checks.	Tektronix Part Number 012–0482–00.
Dual–Input Coupler	Connectors: BNC female–to–dual–BNC male.	Signal interconnection.	Tektronix Part Number 067–0525–02.
Coupler	Connectors: BNC female–to–BNC female.	Signal interconnection.	Tektronix Part Number 103–0028–00.
T–Connector	Connectors: BNC.	Signal interconnection.	Tektronix Part Number 103–0030–00.
Termination	Impedance: 50 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011–0049–01.
Termination	Impedance: 600 Ω. Connectors: BNC.	Signal termination	Tektronix Part Number 011–0092–00.

[a]Requires a TM500–Series Power Module.

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Table 4–1 (cont)

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
10X Attenuator	Ratio: 10X. Impedance: 50 Ω. Connectors: BNC.	Vertical compensation and triggering checks.	Tektronix Part Number 011–0059–02.
2X Attenuator	Ratio: 2X. Impedance: 50 Ω. Connectors: BNC.	External triggering checks.	Tektronix Part Number 011–0069–02.
Adapter	Connectors: BNC male–to–miniature–probe tip.	Signal interconnection.	Tektronix Part Number 013–0084–02.
Adapter	Connectors: BNC male–to–tip plug.	Signal interconnection.	Tektronix Part Number 175–1178–00.
Low–Capacitance Alignment Tool	Length: 1–in. shaft. Bit size: 3/32 in.	Adjust variable capacitors.	J.F.D. Electronics Corp. Adjustment Tool Number 5284.
Screwdriver	Length: 3–in. shaft. Bit size: 3/32 in.	Adjust variable capacitors.	Xcelite R–3323.

[a]Requires a TM500–Series Power Module.

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VERTICAL

Equipment Required (see Table 4–1):

Calibration Generator	50–Ω BNC Precision Cable
Leveled Sine–Wave Generator	Dual–Input Coupler
Pulse Generator	50–Ω BNC Termination
50–Ω BNC Cable	10X Attenuator

INITIAL CONTROL SETTINGS

Vertical (Both Channels)

POSITION	Midrange
MODE	CH 1
X–Y	Off (button out)
BW LIMIT	On (button in)
VOLTS/DIV	2 mV
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC–GND–DC	DC

Horizontal

POSITION	Midrange
MODE	A
A SEC/DIV	0.5 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P–P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A & B SOURCE	VERT MODE
A COUPL	NORM

Storage

STORE/NON–STORE	NON–STORE (button out)

PROCEDURE STEPS

1. Check Deflection Accuracy and Variable Range

a. Connect the standard–amplitude signal from the calibration generator via a 50–Ω cable to the CH 1 OR X input connector.

b. CHECK—Deflection accuracy is within the limits given in Table 4–2 for each CH 1 VOLTS/DIV switch setting and corresponding standard–amplitude signal. When at the 20–mV VOLTS/DIV switch setting, rotate the CH 1 VOLTS/DIV Variable control fully counterclockwise and CHECK that the display decreases to 2 divisions or less. Then return the CH 1 VOLTS/DIV Variable control to the CAL detent and continue with the 50–mV check.

Table 4–2
Deflection Accuracy Limits

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Accuracy Limits (Divisions)
2 mV	10 mV	4.90 to 5.10
5 mV	20 mV	3.92 to 4.08
10 mV	50 mV	4.90 to 5.10
20 mV	0.1 V	4.90 to 5.10
50 mV	0.2 V	3.92 to 4.08
0.1 V	0.5 V	4.90 to 5.10
0.2 V	1 V	4.90 to 5.10
0.5 V	2 V	3.92 to 4.08
1 V	5 V	4.90 to 5.10
2 V	10 V	4.90 to 5.10
5 V	20 V	3.92 to 4.08

c. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

d. Repeat part b using the Channel 2 controls.

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2. Check Store Deflection Accuracy

a. Set:

CH 2 VOLTS/DIV	2 mV
STORE/NON–STORE	STORE (button in)
ACQUISITION MODE	AVERAGE

b. Set the generator to produce a 5–division standard amplitude signal.

c. Use the CURSORS control and SELECT C1/C2 switch (push in the CURSORS controls knob) to set one cursor at the bottom of the square wave and the other cursor at the top of the square wave.

d. CHECK—Deflection accuracy is within the limits given in Table 4–3 for each CH 2 VOLTS/DIV switch setting and corresponding standard–amplitude signal.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the Vertical MODE switch to CH 1.

f. Repeat parts b and c using the Channel 1 controls.

3. Check Save Expansion and Compression

a. Set the CH 1 VOLTS/DIV switch to 0.1 V.

b. Set the generator to produce a 0.5 div standard–amplitude signal.

c. Press in the SAVE/CONT button to select SAVE.

d. Set the CH 1 VOLTS/DIV switch to 10 mV and reposition the display.

e. CHECK—The display is expanded to 5 division in amplitude.

f. Set:

CH 1 VOLTS/DIV	0.1 V
SAVE/CONT	CONT

g. Set the generator to produce a 5 division standard–amplitude signal.

h. Press in the SAVE/CONT button to select SAVE.

i. Set the CH 1 VOLTS/DIV switch to 1 V.

j. CHECK—The display is compressed to 0.5 division in amplitude.

k. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

l. Set:

Vertical MODE	CH 2
SAVE/CONT	CONT

m. Repeat parts a through j.

Table 4–3
Storage Deflection Accuracy

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Divisions of Deflection	Voltage Readout Limits
2 mV	10 mV	4.90 to 5.10	9.70 to 10.30 mV
5 mV	20 mV	3.92 to 4.08	19.40 to 20.60 mV
10 mV	50 mV	4.90 to 5.10	48.5 to 51.5 mV
20 mV	0.1 V	4.90 to 5.10	97.0 to 103.0 mV
50 mV	0.2 V	3.92 to 4.08	194.0 to 206.0 mV
0.1 V	0.5 V	4.90 to 5.10	0.485 to 0.515 V
0.2 V	1 V	4.90 to 5.10	0.970 to 1.030 V
0.5 V	2 V	3.92 to 4.08	1.940 to 2.060 V
1 V	5 V	4.90 to 5.10	4.85 to 5.15 V
2 V	10 V	4.90 to 5.10	9.70 to 10.30 V
5 V	20 V	3.92 to 4.08	19.40 to 20.60 V

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4. Check Position Range

a. Set:

VOLTS/DIV (both)	10 mV
AC–GND–DC (both)	AC
STORE/NON–STORE	NON–STORE (button out)

b. Set the generator to produce a 0.2–V standard–amplitude signal.

c. CHECK—The bottom of the waveform can be vertically positioned at least 1 division above the center horizontal graticule line when the Channel 2 POSITION control is rotated fully clockwise, and that the top of the waveform can be vertically positioned 1 division below the center horizontal graticule line when the Channel 2 POSITION control is rotated fully counterclockwise.

d. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector and set the Vertical MODE switch to CH 1.

e. Repeat part c using the Channel 1 controls.

5. Check Acquisition Position Registration

a. Set:

AC–GND–DC (both)	GND
A SEC/DIV	10 µs

b. Position the trace exactly on the center horizontal graticule line using the Channel 1 POSITION control.

c. Set:

STORE/NON–STORE	STORE (button in)
SAVE/CONT	CONT

d. CHECK—Trace remains within 0.5 division of the center graticule line.

e. Set:

Vertical MODE	CH 2
STORE/NON–STORE	NON–STORE (button out)

f. Repeat parts b through d for Channel 2 trace.

g. Position the trace 0.5 division below the top horizontal graticule line using the Channel 2 POSITION control.

h. Press in the SAVE/CONT button to select SAVE.

i. CHECK—Trace shift of 0.5 division or less.

j. Press in the SAVE/CONT button to select CONT.

k. Position the trace 0.5 division above the bottom horizontal graticule line using the Channel 2 POSITION control.

l. Press in the SAVE/CONT button to select SAVE.

m. CHECK—Trace shift of 0.5 division or less.

n. Press in the SAVE/CONT button to select CONT.

o. Set the Vertical MODE switch to CH 1.

p. Repeat steps g through m for Channel 1 trace.

6. Check Bandwidth

a. Set:

VOLTS/DIV (both)	2 mV
AC–GND–DC (both)	DC
A SEC/DIV	0.2 ms
STORE/NON–STORE	NON–STORE (button out)

b. Connect the leveled sine–wave generator output via a 50–Ω precision cable and a 50–Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50–kHz, 6–division display.

d. CHECK—Display amplitude is 4.2 divisions or greater as the generator output frequency is increased up to the value shown in Table 4–4 for the corresponding VOLTS/DIV switch setting.

Table 4–4
Settings for Bandwidth Checks

VOLTS/DIV Switch Setting	Generator Output Frequency
2 mV	80 MHz
5 mV to 0.5 V	100 MHz

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e. Repeat parts c and d for all indicated CH 1 VOLTS/DIV switch settings, up to the output–voltage upper limit of the sine–wave generator being used.

f. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

g. Set the Vertical MODE switch to CH 2.

h. Repeat parts c and d for all indicated CH 2 VOLTS/DIV switch settings, up to the output–voltage upper limit of the sine–wave generator being used.

7. Check Repetitive Store Mode and Bandwidth

a. Set:

CH 1 VOLTS/DIV	10 mV
A SEC/DIV	0.2 ms

b. Set the generator to produce a 50–kHz, 6–division display.

c. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

d. Set the generator to produce a 100–MHz display.

e. Set:

STORE/NON–STORE	STORE (button in)
SAVE/CONT	CONT

NOTE

Allow the points to accumulate for a few seconds before saving the display.

f. Press in the SAVE/CONT button to select SAVE.

g. CHECK—The 100–MHz display is saved.

h. CHECK—Display amplitude is 4.2 divisions or greater.

i. Press in the SAVE/CONT button to select CONT.

j. Set the Vertical MODE switch to BOTH and ALT.

k. Repeat parts f through h.

8. Check Single Sweep Sample Acquisition

a. Set:

Vertical MODE	CH 2
A SEC/DIV	5 μs
X10 Magnifier	Off (knob in)
A TRIGGER Mode	NORM
A & B SOURCE	CH 2
SAVE/CONT	CONT

b. Set the generator to produce a 50–kHz, 6–division display.

c. Press in the A TRIGGER Mode SGL SWP button.

d. Set the generator output to 2 MHz.

e. Press in the A TRIGGER Mode SGL SWP button.

f. CHECK—the minimum peak–to–peak envelope amplitude is greater than 5.6 divisions.

9. Check Bandwidth Limit Operation

a. Set:

BW LIMIT	On (button in)
VOLTS/DIV (both)	10 mV
AC–GND–DC (both)	DC
A SEC/DIV	20 μs
A TRIGGER Mode	P–P AUTO
A & B SOURCE	VERT MODE
STORE/NON–STORE	NON–STORE (button out)

b. Set the generator to produce a 50–kHz, 6–division display.

c. Adjust the generator output frequency until the display amplitude decreases to 4.2 divisions.

d. CHECK—Generator output frequency is between 18 and 22 MHz.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

f. Set the Vertical MODE switch to CH 1.

g. Repeat parts c and d.

h. Disconnect the test equipment from the instrument.

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10. Check Common–Mode Rejection Ratio

a. Set:

BW LIMIT	Off (button out)
INVERT	On (button in)

b. Connect the leveled sine–wave generator output via a 50–Ω cable, a 50–Ω termination, and a dual–input coupler to the CH 1 OR X and the CH 2 OR Y input connectors.

c. Set the generator to produce a 50–MHz, 6–division display.

d. Vertically center the display using the Channel 1 POSITION control. Then set the Vertical MODE switch to CH 2 and vertically center the display using the Channel 1 POSITION control.

e. Set the Vertical MODE switches to BOTH and ADD.

f. CHECK—Display amplitude is 0.6 division or less.

g. If the check in part f meets the requirement, skip to part p. If it does not, continue with part h.

h. Set the Vertical MODE switch to CH 2.

i. Set the generator to produce a 50–kHz, 6–division display.

j. Set the Vertical MODE switch to BOTH.

k. Adjust the CH 1 or CH 2 VOLTS/DIV Variable control for minimum display amplitude.

l. Set the Vertical MODE switch to CH 2.

m. Set the generator to produce a 50–MHz, 6–division display.

n. Set the Vertical MODE switch to BOTH.

o. CHECK—Display amplitude is 0.6 division or less.

p. Disconnect the test equipment from the instrument.

11. Check Non–Store and Store Channel Isolation

a. Set:

Vertical MODE	CH 1
VOLTS/DIV (both)	0.1 V
VOLTS/DIV Variable (both)	CAL detent
INVERT	Off (button out)
Channel 1 AC–GND–DC	DC
Channel 2 AC–GND–DC	GND
A SEC/DIV	0.1 μs

b. Connect the leveled sine–wave generator output via a 50–Ω cable and a 50–Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50–MHz, 5–division display.

d. Set the Vertical MODE switch to CH 2.

e. CHECK—Display amplitude is 0.05 division or less.

f. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

g. Set:

Vertical MODE	CH 1
Channel 1 AC–GND–DC	GND
Channel 2 AC–GND–DC	DC

h. CHECK—Display amplitude is 0.05 division or less.

i. Set:

CH 2 VOLTS/DIV	50 mV
STORE/NON–STORE	STORE (button in)
SAVE/CONT	CONT

j. CHECK—Display amplitude is 0.1 division or less.

k. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

l. Set:

Vertical MODE	CH 2
CH 1 VOLTS/DIV	50 mV
CH 2 VOLTS/DIV	0.1 V
Channel 1 AC–GND–DC	DC
Channel 2 AC–GND–DC	GND

m. CHECK—Display amplitude is 0.1 division or less.

n. Disconnect the test equipment from the instrument.

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12. Check Store Pulse Width Amplitude

a. Set:

CH 2 VOLTS/DIV	0.5 V
Channel 2 AC–GND–DC	AC
A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)
STORE/NON–STORE	NON–STORE (button out)

b. Connect the pulse generator pulse–period output via a 50–Ω coaxial cable and a 50–Ω termination to CH 2 OR Y input connector.

c. Set the generator to produce a 0.1–ms period, 10–ns pulse duration, 5–division display.

d. Set X10 Magnifier off (knob in).

e. Set the Pulse Generator period to 1 ms.

f. Set A SEC/DIV to 1 ms.

g. Set:

STORE/NON–STORE	STORE(button in)
ACQUISITION MODE	PEAKDET

h. Adjust HORIZONTAL POSITION control to center trace horizontally.

i. Press the DISPLAY SETUP button to select the DISPLAY menu. Choose SCAN with the Menu Item Select button. Return to the standard (non–menu) display by pressing the DISPLAY SETUP button again.

j. CHECK—The amplitude of the display is 2.5 divisions or greater.

k. Set the A SEC/DIV switch to 0.1 sec.

l. CHECK—The amplitude of the display is 2.5 divisions or greater.

m. Disconnect the test equipment from the instrument.

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HORIZONTAL

Equipment Required (see Table 4–1):

Calibration Generator	50–Ω BNC Cable
Leveled Sine–Wave Generator	50–Ω BNC Termination
Time–Mark Generator	

INITIAL CONTROL SETTINGS

Vertical

Channel 1 POSITION	Midrange
MODE	CH 1
X–Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	0.5 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC–GND–DC	DC

Horizontal

POSITION	Midrange
MODE	A
A SEC/DIV	0.05 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counter–clockwise

B TRIGGER

SLOPE	Positive (button out)
LEVEL	Fully clockwise

A TRIGGER

VAR HOLDOFF	NORM
Mode	P–P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A & B SOURCE	VERT MODE
A COUPL	NORM
A EXT COUPL	DC

Storage

STORE/NON–STORE	NON–STORE (button out)

PROCEDURE STEPS

1. Check Timing Accuracy and Linearity

a. Connect the time–mark generator output via a 50–Ω cable and a 50–Ω termination to the CH 1 OR X input connector.

b. Select 50–ns time markers from the time–marker generator.

c. Use the Channel 1 POSITION control to center the display vertically. Adjust the A TRIGGER LEVEL control for a stable, triggered display.

d. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

e. CHECK—Timing accuracy is within 2% (0.16 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions). For checking the timing accuracy of the A SEC/DIV switch settings from 50 ms to 0.5 s, watch the time marker tips only at the 2nd and 10th vertical graticule lines while adjusting the Horizontal POSITION control.

f. Repeat parts c through e for the remaining A SEC/DIV and time–mark generator setting combinations shown in Table 4–5 under the Normal (X1) column.

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Table 4–5
Settings for Timing Accuracy Checks

SEC/DIV Switch Setting	Time–Mark Generator Setting	
	Normal (X1)	X10 Magnified
0.05 µs	50 ns	10 ns
0.1 µs	0.1 µs	10 ns
0.2 µs	0.2 µs	20 ns
0.5 µs	0.5 µs	50 ns
1 µs	1 µs	0.1 µs
2 µs	2 µs	0.2 µs
5 µs	5 µs	0.5 µs
10 µs	10 µs	1 µs
20 µs	20 µs	2 µs
50 µs	50 µs	5 µs
0.1 ms	0.1 ms	10 µs
0.2 ms	0.2 ms	20 µs
0.5 ms	0.5 ms	50 µs
1 ms	1 ms	0.1 ms
2 ms	2 ms	0.2 ms
5 ms	5 ms	0.5 ms
10 ms	10 ms	1 ms
20 ms	20 ms	2 ms
50 ms	50 ms	5 ms
A Sweep Only		
0.1 s	0.1 s	10 ms
0.2 s	0.2 s	20 ms
0.5 s	0.5 s	50 ms

g. Set:

A SEC/DIV	0.05 µs
X10 Magnifier	On (knob out)

h. Select 10–ns time markers from the time–mark generator.

i. Use the Horizontal POSITION control to align the 1st time marker that is 40 ns beyond the start of the sweep with the 2nd vertical graticule line.

j. CHECK—Timing accuracy is within 3% (0.24 division at the 10th vertical graticule line), and linearity is within 7.5% (0.15 division over any 2 of the center 8 divisions). Exclude any portion of the sweep past the 100th magnified division.

k. Repeat parts i and j for the remaining A SEC/DIV and time–mark generator setting combinations shown in Table 4–5 under the X10 Magnified column.

l. Set:

Horizontal MODE	B
A SEC/DIV	0.1 µs
B SEC/DIV	0.05 µs
X10 Magnifier	Off (knob in)

m. Repeat parts b through k for the B Sweep.

2. Check Store Differential and Cursor Time Difference Accuracy

a. Set:

Channel 1 AC–GND–DC	GND
Horizontal MODE	A
A SEC/DIV	0.1 ms
X10 Magnifier	Off (knob in)
STORE/NON–STORE	STORE (button in)

b. Use the Channel 1 POSITION control to center the base line vertically and the Horizontal POSITION control to align the start of the trace with the 1st vertical graticule line.

c. Use the CURSORS control and SELECT C1/C2 (push in the CURSORS control knob) switch to set one cursor exactly on the 2nd vertical graticule line and position the active cursor to the right using the CURSORS control until ΔT readout displays 0.800 ms.

d. CHECK—Graticule indication of cursor difference at the 10th vertical graticule line is within 0.16 division.

e. Set the Channel 1 AC–GND–DC switch to DC.

f. Select 0.1–ms time markers from the time–mark generator.

g. Align the 2nd time marker with the 2nd vertical graticule line using the Horizontal POSITION control.

h. Press in the SAVE/CONT button to select SAVE for a stable display.

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i. Use the CURSORS control and SELECT C1/C2 (push in the CURSORS control knob) switch to set the first cursor on the trailing edge of the 2nd time marker.

j. Press in the CURSORS control knob again to activate the second cursor.

k. Set the second cursor on the trailing edge of the 10th time marker at the same voltage level as on the 2nd time marker.

l. CHECK—The ΔT readout is between 0.798 ms and 0.802 ms.

m. Press in the SAVE/CONT button to select CONT.

n. Set the A SEC/DIV switch to 0.5 μs.

o. Select 0.5—μs time markers from the time—mark generator.

p. Align the 2nd time marker with the 2nd vertical graticule line using the Horizontal POSITION control.

NOTE

Allow the points to accumulate for a few seconds before saving the display.

q. Repeat parts h through k.

NOTE

Pulses with fast rise and fall times have only a few sample points and it may not be possible to place the cursors at exactly the same voltage levels.

r. CHECK—The ΔT readout is between 3.990 μs and 4.010 μs.

3. Check Variable Range and Sweep Separation

a. Set:

A and B SEC/DIV	0.2 ms
SEC/DIV Variable	Fully counter—clockwise
STORE/NON—STORE	NON—STORE (button out)

b. Select 0.5—ms time markers from the time—mark generator.

c. CHECK—Time markers are 1 division or less apart.

d. Set:

Channel 1 AC—GND—DC	GND
SEC/DIV Variable	CAL detent
Horizontal MODE	BOTH
B TRIG	Fully clockwise (Runs After Delay)

e. Use the Channel 1 POSITION control to set the A Sweep at the center horizontal graticule line.

f. CHECK—The B Sweep can be positioned more than 3.5 divisions above and below the A Sweep when the A/B SWP SEP control is rotated fully clockwise and counterclockwise respectively.

4. Check Delay Time Differential Accuracy

a. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

b. Set the B DELAY TIME POSITION control fully counterclockwise.

c. CHECK—Intensified portion of the trace starts within 0.5 division of the start of the sweep.

d. Rotate the B DELAY TIME POSITION control fully clockwise.

e. CHECK—Intensified portion of the trace is past the 11th vertical graticule line.

f. Set:

A and B SEC/DIV	0.5 μs
B DELAY TIME POSITION	Fully counter—clockwise

g. Align the start of the A Sweep with the 1st vertical graticule line using the Horizontal POSITION control.

h. CHECK—Intensified portion of the trace starts within 1.1 divisions of the start of the sweep.

i. Repeat parts d and e.

j. Set:

Channel 1 AC—GND—DC	DC
B SEC/DIV	0.05
B DELAY TIME POSITION	Fully counter—clockwise

k. Select 0.5—μs time markers from the time—mark generator.

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l. Rotate the B DELAY TIME POSITION control so that the top of the 2nd time marker on the B Sweep is aligned with a selected reference vertical line. Record the DLY= readout for part n.

m. Rotate the B DELAY TIME POSITION control fully clockwise until the top of the 10th time marker on the B Sweep is aligned with the same selected reference vertical line as in part l. Record the DLY= readout for part n.

n. CHECK—Delay time readout is within the limits given in Table 4–6 (Delay Readout Limits column) by subtracting the delay time reading in part l from part m.

o. Repeat parts j through n for the remaining B SEC/DIV and time–mark generator settings given in Table 4–6, check the 8–division delay time accuracy for each A SEC/DIV switch setting given in column 1 of the table.

5. Check Delay Jitter

a. Set:

A SEC/DIV	0.5 ms
B SEC/DIV	1 μs

b. Select 0.5 ms time markers from the time–mark generator.

c. Rotate the B DELAY TIME POSITION control to position the intensified zone on the 10th time marker.

d. Set the Horizontal MODE switch to B.

e. CHECK—The jitter on the leading edge of the time marker does not exceed 1 division. Disregard slow drift.

6. Check Position Range

a. Set:

Horizontal MODE	A
A SEC/DIV	10 μs

b. Select 10–μs time markers from the time–mark generator.

c. CHECK—Start of the sweep can be positioned to the right of the center vertical graticule line by rotating the Horizontal POSITION control fully clockwise.

d. CHECK—The 11th time marker can be positioned to the left of the center vertical graticule line by rotating the Horizontal POSITION control fully counterclockwise.

e. Select 50–μs time markers from the time–mark generator.

f. Align the 3rd time marker with the center vertical graticule line using the Horizontal POSITION control.

Table 4–6
Settings for Delay Time Differential Checks

Time–Mark Generator and A SEC/DIV Settings	B SEC/DIV Setting	Eight Division Delay	Delay Readout Limits
0.5 μs	0.05 μs	4.000 μs	3.935 μs to 4.065 μs
5 μs	0.5 μs	40.00 μs	39.35 μs to 40.65 μs
50 μs	5 μs	400.0 μs	393.5 μs to 406.5 μs
0.5 ms	50 ms	4.000 ms	3.935 ms to 4.065 ms
5 ms	0.5 ms	40.00 ms	39.35 ms to 40.65 ms
50 ms	5 ms	400.0 ms	393.5 ms to 406.5 ms
0.5 s	50 ms	4.000 s	3.935 s to 4.065 s

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g. Set the X10 Magnifier knob to On (knob out).

h. CHECK—Magnified time marker can be positioned to the left of the center vertical graticule line by rotating the Horizontal POSITION control fully counterclockwise.

i. CHECK—Start of the sweep can be positioned to the right of the center vertical graticule line by rotating the Horizontal POSITION control fully clockwise.

7. Check Store Expansion Range

a. Set:

A SEC/DIV	0.1 ms
X10 Magnifier	Off (knob in)

b. Select 10−μs time markers from the time−mark generator.

c. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

d. Set the STORE/NON−STORE switch to STORE (button in).

e. Set the X10 Magnifier knob to On (knob out).

f. CHECK—The time markers are 1 division apart.

8. Check 4K to 1K Display Compress

a. Set:

A SEC/DIV	50 μs
X10 Magnifier	Off (knob in)
1K/4K	4K

b. Select 0.1−ms time markers from the time−mark generator and check that the time markers are 2 divisions apart.

c. Rotate the SEC/DIV Variable control out of detent.

d. CHECK—For 2 time markers per division over the center 8 divisions.

9. Check Non−Store Sweep Length

a. Set:

SEC/DIV Variable	CAL detent
STORE/NON−STORE	NON−STORE (button out).

b. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

c. CHECK—End of the sweep is to the right of the 11th vertical graticule line.

d. Disconnect the test equipment from the instrument.

10. Check X Gain

a. Set:

X−Y	On (button in)
CH 1 VOLTS/DIV	10 mV
Horizontal POSITION	Midrange

b. Connect the standard−amplitude signal from the Calibration Generator via a 50−Ω cable to the CH 1 OR X input connector.

c. Set the generator to produce a 50−mV signal.

d. Use the Channel 2 POSITION and Horizontal POSITION controls to center the display.

e. CHECK—Display is 4.85 to 5.15 horizontal divisions.

f. Disconnect the test equipment from the instrument.

11. Check X Bandwidth

a. Connect the leveled sine−wave generator output via a 50−Ω cable and a 50−Ω termination to the CH 1 OR X input connector.

b. Set the generator to produce a 5−division horizontal display at an output frequency of 50 kHz.

c. Increase the generator output frequency to 2.5 MHz.

d. CHECK—Display is at least 3.5 horizontal divisions.

e. Disconnect the test equipment from the instrument.

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TRIGGER

Equipment Required (see Table 4–1):

Calibration Generator	Dual–Input Coupler
Leveled Sine–Wave Generator	50–Ω BNC Termination
Low Frequency Generator	600–Ω BNC Termination
50–Ω BNC Cable	

INITIAL CONTROL SETTINGS

Vertical

POSITION (both)	Midrange
MODE	CH 1
X–Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	5 mV
CH 2 VOLTS/DIV	50 mV
VOLTS/DIV Variable (both)	CAL detent
INVERT	Off (button out)
AC–GND–DC (both)	DC

Horizontal

POSITION	Midrange
MODE	A
A and B SEC/DIV	0.2 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counter clockwise

B TRIGGER

SLOPE	Positive (button out)
LEVEL	Midrange

A TRIGGER

VAR HOLDOFF	NORM
Mode	P–P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A & B SOURCE	CH 1
A COUPL	NORM
A EXT COUPL	DC

Storage

STORE/NON–STORE	NON–STORE (button out)

PROCEDURE STEPS

1. Check Internal A and B Triggering

a. Connect the leveled sine–wave generator output via a 50–Ω cable and a 50–Ω termination to the CH 1 OR X input connector.

b. Set the generator to produce a 10–MHz, 3.5–division display.

c. Set the CH 1 VOLTS/DIV switch to 50 mV.

d. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 4–7.

e. Set the Horizontal MODE switch to B.

Table 4–7
Switch Combinations for A Triggering Checks

A TRIGGER Mode	A TRIGGER SLOPE
NORM	Positive
NORM	Negative
P–P AUTO	Negative
P–P AUTO	Positive

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f. CHECK—Stable display can be obtained by adjusting the B TRIGGER LEVEL control in a position other than the B RUNS AFTER DLY position for both the positive and negative positions of the B TRIGGER SLOPE switch.

g. Set:

Vertical MODE	CH 2
Horizontal MODE	A
A & B SOURCE	CH 2

h. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

i. Repeat parts d through f.

j. Set:

Horizontal MODE	A
A SEC/DIV	0.1 μs
X10 Magnifier	On (knob out)

k. Set the generator to produce a 60−MHz, 1.0−division display.

l. Repeat parts d through f.

m. Set:

Vertical MODE	CH 1
Horizontal MODE	A
A & B SOURCE	CH 1

n. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

o. Repeat parts d through f.

p. Set:

Horizontal MODE	A
A SEC/DIV	0.05 μs

q. Set the generator to produce a 100−MHz, 1.5−division display.

r. Repeat parts d through f.

s. Set:

Vertical MODE	CH 2
Horizontal MODE	A
A & B SOURCE	CH 2

t. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

u. Repeat parts d through f.

v. Disconnect the test equipment from the instrument.

2. Check HF Reject A Triggering

a. Set:

Vertical MODE	CH 1
VOLTS/DIV (both)	50 mV
Horizontal MODE	A
A SEC/DIV	5 μs
X10 Magnifier	Off (knob in)
A TRIGGER Mode	NORM
A TRIGGER LEVEL	Midrange
A & B SOURCE	CH 1

b. Connect the low frequency generator output via a 50−Ω cable and a 600−Ω termination to the CH 1 OR X input connector.

c. Set the low frequency generator output to produce a 250−kHz, 1−division display.

d. Adjust the A TRIGGER LEVEL control for a stable display.

e. Set the A COUPL switch to HF REJ position.

f. CHECK—Stable display cannot be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 4−7.

g. Set:

Vertical MODE	CH 2
A & B SOURCE	CH 2

h. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

i. Repeat part f.

3. Check LF Reject A Triggering

a. Set:

A TRIGGER LEVEL	Midrange
A COUPL	LF REJ

b. Set the generator to produce a 25−kHz, 0.35−division display.

c. CHECK—The display cannot be obtained by adjusting the A TRIGGER LEVEL control.

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d. Set the generator to produce a 50–kHz, 0.35–division display.

e. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control.

f. Set:

Vertical MODE	CH 1
A & B SOURCE	CH 1

g. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

h. Repeat parts b through e.

i. Disconnect the test equipment from the instrument.

4. Check External Triggering

a. Set:

CH 1 VOLTS/DIV	5 mV
A SEC/DIV	0.1 μs
A & B SOURCE	A EXT
A COUPL	NORM

b. Connect the leveled sine–wave generator output via a 50–Ω cable, a 50–Ω termination, and a dual–input coupler to both the CH 1 OR X and EXT INPUT connectors.

c. Set the leveled sine–wave generator output voltage to 40 mV and the frequency to 10 MHz.

d. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 4–7.

e. Set:

CH 1 VOLTS/DIV	50 mV
X10 Magnifier	On (knob out)

f. Set the generator output voltage to 120 mV and the frequency to 60 MHz.

g. Repeat part d.

h. Set the generator output voltage to 150 mV and the frequency to 100 MHz.

i. Repeat part d.

5. Check External Trigger Ranges

a. Set:

CH 1 VOLTS/DIV	0.5 V
A SEC/DIV	20 μs
X10 Magnifier	Off (knob in)
A TRIGGER SLOPE	Positive (button out)
A TRIGGER Mode	NORM

b. Set the generator to produce a 50–kHz, 6.4–division display.

c. CHECK—Display is triggered along the entire positive slope of the waveform as the A TRIGGER LEVEL control is rotated.

d. CHECK—Display is not triggered (no trace) at either extreme of rotation.

e. Set the A TRIGGER SLOPE button to Negative (button in).

f. CHECK—Display is triggered along the entire negative slope of the waveform as the A TRIGGER LEVEL control is rotated.

g. CHECK—Display is not triggered (no trace) at either extreme of rotation.

6. Check Single Sweep Operation

a. Adjust the A TRIGGER LEVEL control to obtain a stable display.

b. Set:

Channel 1 AC–GND–DC	GND
A TRIGGER SLOPE	Positive (button out)
A & B SOURCE	CH 1
A COUPL	NORM
A SEC/DIV	20 ms

c. Press in the SGL SWP button. The READY LED should illuminate and remain on.

d. Set the Channel 1 AC–GND–DC switch to DC.

NOTE

The A INTENSITY control may require adjustment to observe the single–sweep trace.

e. CHECK—READY LED goes out and a single sweep occurs.

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f. Press in the SGL SWP button several times.

g. CHECK—Single-sweep trace occurs, and the READY LED illuminates briefly every time the SGL SWP button is pressed in and released.

h. Disconnect the test equipment from the instrument.

7. Check Acquisition Window Trigger Points

a. Set:

Channel 1 AC-GND-DC	GND
A TRIGGER Mode	P-P AUTO
A SEC/DIV	0.1 μs
STORE/NON-STORE	STORE (button out)
1K/4K	1k

b. Use the Horizontal POSITION control to align the start of the display acquisition with the 1st vertical graticule line.

c. Press in the TRIG POS button until the store trigger point (T) is located on the left side of the screen.

d. CHECK—The POST TRIG point (T) is 1.28 divisions from the start of the display acquisition.

e. Press the TRIG POS button a second time to position the trigger point to the middle of the display acquisition.

f. CHECK—The MIDTRIG point (T) is 5.12 divisions from the start of the display acquisition.

g. Press the TRIG POS button a third time to position the trigger point to the right of the display acquisition.

h. CHECK—The PRETRIG point (T) is 8.96 divisions from the start of the display acquisition.

8. Check Trigger Level Readout

a. Set:

Vertical MODE	CH 1
Channel 1 VOLTS/DIV	20 mV
Channel 1 AC-GND-DC	GND
SEC/DIV	0.5 ms
A TRIGGER Mode	P-P AUTO
A TRIGGER LEVEL	Midrange
A TRIGGER SOURCE	VERT MODE
STORE/NON-STORE	NON-STORE (button out)

b. Center the trace on the screen.

c. CHECK—The trigger readout is between −3 mV and +3 mV.

d. Connect the standard-amplitude signal from the calibration generator via a 50-Ω cable to the CH1 OR X input connector.

e. Set:

Channel 1 AC-GND-DC	DC
A TRIGGER Mode	NORM

f. Set the generator to produce a 5 division standard-amplitude signal.

g. Adjust the A Trigger LEVEL control for a stable display and center the waveform on the screen.

h. Set the Channel 1 VOLTS/DIV switch to 10 mV for a 10-division display.

i. Vertically position the top of the waveform display on the center horizontal graticule line.

j. Set the A Trigger SLOPE switch to Negative (button in).

k. Rotate the A Trigger LEVEL control clockwise until the triggering of the waveform display becomes unstable.

l. CHECK—The trigger readout is between 92 mV and 108 mV.

m. Repeat procedure for CH 2 using CH 2 controls.

n. Disconnect the test equipment from the instrument.

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EXTERNAL Z–AXIS, PROBE ADJUST, EXTERNAL CLOCK, AND X–Y PLOTTER

Equipment Required (see Table 4–1):

- Leveled Sine–Wave Generator
- Pulse Generator
- Digital Voltmeter
- Two 50–Ω BNC Cables
- BNC T–Connector
- 50–Ω BNC Termination
- BNC male–to–tip plug
- 10X Probe (provided with instrument)

INITIAL CONTROL SETTINGS

Vertical

Channel 1 POSITION	Midrange
MODE	CH 1
X–Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	1 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC–GND–DC	DC

Horizontal

POSITION	Midrange
MODE	A
A SEC/DIV	20 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P–P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A & B SOURCE	VERT MODE
A COUPL	NORM
A EXT COUPL	AC

Storage

STORE/NON–STORE	NON–STORE (button out)

PROCEDURE STEPS

1. Check External Z–Axis Operation

a. Connect the leveled sine–wave generator output via a 50–Ω cable and a T–connector to the CH 1 OR X input connector. Then connect a 50–Ω cable and a 50–Ω termination from the T–connector to the EXT Z–AXIS INPUT connector on the rear panel.

b. Set the generator to produce a 5–V, 50–kHz signal.

c. CHECK—For noticeable intensity modulation. The positive part of the sine wave should be of lower intensity than the negative part.

d. Disconnect the test equipment from the instrument.

2. Check Probe Adjust Operation

a. Set:

CH 1 VOLTS/DIV	10 mV
A SEC/DIV	0.5 ms

b. Connect the 10X Probe to the CH 1 OR X input connector and insert the probe tip into the PROBE ADJUST jack on the instrument front panel. If necessary, adjust the probe compensation for a flat–topped square–wave display.

c. CHECK—Display amplitude is 4.75 to 5.25 divisions.

d. Disconnect the probe from the instrument.

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3. Check External Clock

a. Set:

CH 1 VOLTS/DIV	1 V
A SEC/DIV	1 ms

b. Connect the Pulse Generator high amplitude output via a 50−Ω cable and a 50−Ω termination to CH 1 OR X input connector.

c. Set the generator to produce a 10−μs, 5−μs duration, 5−division display.

d. Disconnect the cable from the CH 1 OR X input connector and connect it to the BNC male−to−tip plug via BNC female to BNC female connector.

e. Insert the BNC male−to−tip plug signal lead and ground lead into pin 1 and pin 9 respectively of the X−Y Plotter connector.

f. Set the A SEC/DIV switch to 0.1 sec.

g. Connect the Calibration Generator high amplitude output via a 50−Ω cable and a 50−Ω termination to CH 1 OR X input connector.

h. Set the generator to produce a 100−Hz, 5−division display.

i. Set:

A SEC/DIV	EXT CLK
STORE/NON−STORE	STORE (button in)

j. Press the SETUP ACQ button to display the ACQUISITION menu and select Fast with the Ext Clock button. Return the instrument to display mode by pressing the SETUP ACQ button a second time.

k. CHECK—The 100−Hz signal is displayed on the screen and updated.

l. Press in the SAVE/CONT button to select SAVE.

m. CHECK—The display is save.

n. Press in the SAVE/CONT button to select CONT.

o. Disconnect the test equipment from the instrument.

4. Check X−Y Plotter

a. Set the A SEC/DIV switch to 10 ms.

b. Connect the digital voltmeter low lead to either chassis ground or pin 9 (signal ground) of the X−Y Plotter connector. Connect the volts lead to pin 3 (X Output) of the X−Y Plotter connector.

c. Set the digital voltmeter to the 20 V scale.

d. Press the SETUP PLOT button to display the PLOT menu. Set Plotter Type to XY, Grat to ON, Auto Plot to OFF, and Plot speed to 10.

e. Press in the Start button to activate the X−Y Plotter.

NOTE

Voltage reading of the X Output will be negative left of the center vertical graticule line and positive to the right of the center vertical graticule line. Voltage reading of the Y output will be negative below the center horizontal graticule line and positive above the center horizontal graticule line.

f. Record the voltage reading as the instrument plots the 1st and the 10th graticule line (as the intensity spot moves along the graticule line).

g. CHECK—The voltage difference between the 1st and 10th graticule line is between 4.5 V and 5.5 V.

h. Move the volts lead of the voltmeter from pin 3 (X Output) to pin 5 (Y Output) to the X−Y Plotter connector.

i. Press the Start button in again to activate the X−Y Plotter.

j. Record the voltage reading as the instrument plots the top and the bottom of the graticule lines (as the intensity spot moves along the graticule line).

k. CHECK—The voltage difference between the top and bottom graticule line is between 3.6 V and 4.4 V.

l. Disconnect the test equipment from the instrument.

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ADJUSTMENT PROCEDURE

INTRODUCTION

PURPOSE

The Adjustment Procedure is a set of logically sequenced instructions intended to return the instrument to conformance with the Performance Requirement statements listed in Table 1–1. Adjustments contained in this procedure should only be performed after checks from the Performance Check Procedure (Section 4) have indicated a need for readjustment or after repairs have been made to the instrument.

STRUCTURE

This procedure is structured into subsections, each of which can be performed independently to permit adjustment of individual sections of the instrument. For example, if only the Vertical section fails to meet the Performance Requirements or has been repaired, it can be readjusted with little or no effect on other sections of the instrument.

The Power Supply section, however, affects all other sections of the instrument. Therefore, if repairs or readjustments have been made that change the absolute value of any of the supply voltages, the entire Adjustment Procedure should be performed.

At the beginning of each subsection is a list of all the front-panel control settings required to prepare the instrument for performing Step 1 in that subsection. Each succeeding step within a subsection should be performed in sequence and in its entirety to ensure that control settings will be correct for ensuing steps. All steps within a subsection should be completed.

TEST EQUIPMENT REQUIRED

Table 4–1 is a complete list of the test equipment required to accomplish both the Performance Check Procedure in Section 4 and the Adjustment Procedure in this section. To assure accurate measurements, it is important that test equipment used for making these checks meet or exceed the specifications described in Table 4–1. When considering use of equipment other than that recommended, utilize the Minimum Specification column to determine whether available test equipment will suffice.

Detailed operating instructions for test equipment are not given in this procedure. If more operating information is required, refer to the appropriate test-equipment instruction manual.

LIMITS AND TOLERANCES

The limits and tolerances stated in this procedure are instrument specifications only if they are listed in the Performance Requirements column of Table 1–1. Tolerances given are applicable only to the instrument undergoing adjustment and do not include test equipment error. Adjustment of the instrument must be accomplished at an ambient temperature between +20°C and +30°C, and the instrument must have had a warm-up period of at least 20 minutes.

ADJUSTMENTS AFFECTED BY REPAIRS

Repairs to a circuit may affect one or more adjustment settings of the instrument. Table 5–1 identifies the adjustment(s) affected due to repairs or replacement of components on a circuit board. Refer to Table 5–1 if a partial procedure is performed or if a circuit requires readjustment due to repairs to a circuit. To use this table, first find, in the leftmost column, the circuit that was repaired. Then move to the right, across that row, until you come to a darkened square, move up the column and check the accuracy of the adjustment found at the heading of that column. Readjust if necessary.

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Table 5–1
Adjustments Affected by Repairs

REPAIRS MADE	INTERNAL ADJUSTMENTS AFFECTED																									
	–8.6 V ADJ	GRID BIAS, ASTIG, & GEOM	STEP ATTEN BAL	2/5 MV DC BAL, VAR BAL, & INVERT BAL	MF/LF COMP & MF/LF GAIN BAL	CH 1, CH 2, & 2 mV GAIN	STORE Y GAIN & OFFSET	ACQ OFFSET	CH 1 & CH 2 GAIN	CH 1 & CH 2 ACQ POS OFFSET	10X ATTEN & 100X ATTEN	HF COMP, CH 2 HF COMP, & 2 mV PEAK	CH 1 & CH 2 ACQ HF PEAK	A & B SWEEP GAIN	X10 GAIN	MAGNIFIER REGISTRATION	DELAY START, D-END, & READOUT	A & B HIGH SPEED TIMING & 5 ns TIMING	4K TO 1K RATIO ADJ	X & Y VECTOR/DOT ALIGNMENT	STORE X GAIN & OFFSET	CDT XY & CDT X	X-GAIN	TRIG OFFSET, SENS, B SENS, & P-P AUTO	TRIGGER READOUT GAIN & OFFSET
POWER SUPPLIES	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
VERTICAL ATTENUATORS			▨	▨	▨	▨		▨	▨	▨	▨	▨	▨											▨	▨	▨
PREAMPS & CHANNEL SW				▨	▨	▨		▨	▨	▨		▨	▨											▨	▨	▨
VERTICAL OUTPUT				▨	▨	▨	▨		▨	▨		▨	▨											▨	▨	▨
TRIGGER CIRCUITS																							▨	▨	▨	▨
A SWEEP GENERATOR														▨	▨	▨	▨	▨	▨			▨		▨		
B SWEEP GENERATOR														▨	▨		▨	▨	▨			▨		▨		
HORIZONTAL AMPLIFIER														▨	▨	▨	▨	▨	▨			▨		▨		
DIGITAL TO ANALOG							▨		▨	▨												▨				
STORE ACQUISITION							▨	▨	▨	▨			▨													
VECTOR GENERATOR							▨		▨	▨											▨	▨				
I/O CIRCUIT										▨							▨									
DIGITAL TIMEBASE																							▨			
CRT		▨				▨	▨	▨	▨	▨				▨								▨		▨		

PREPARATION FOR ADJUSTMENT

The instrument cabinet must be removed to perform the Adjustment Procedure. See the Cabinet remove and replace instructions located in the Maintenance section of the manual. When making adjustments inside the instrument, the Storage circuit board has to be lifted up and latched to allow access to the internal adjustments. See the Storage Circuit Board in Servicing Position procedure in the Removal and Replacement Instructions part of the Maintenance section.

To facilitate the adjustment procedure, it may be necessary to remove the support chassis from the instrument. To remove and reinstall the support chassis, see the Removal and Replacement instruction in Section 6 of this manual.

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All test equipment items listed in Table 4–1 are required to accomplish a complete Adjustment Procedure. At the beginning of each subsection there is an equipment-required list showing only the test equipment necessary for performing the steps in that subsection.

Before performing this procedure, do not preset any internal adjustments and do not change the –8.6 V power-supply adjustment. Altering this adjustment may necessitate a complete readjustment of the instrument, whereas only a partial adjustment might otherwise be required. Only change an internal adjustment setting if a Performance Characteristic cannot be met with the original setting.

Before performing any procedure in this section, set the POWER switch to ON and allow a 20-minute warm-up period.

To ensure performance accuracies stated in the Specification (Section 1), for the digital portion of the instrument, select the Factory Reset routine. The Factory Reset routine sets the digital part of the instrument to factory default settings.

The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted, adjust the INTENSITY, FOCUS, and TRIGGER LEVEL controls as needed to view the display.

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POWER SUPPLY AND CRT DISPLAY

Equipment Required (See Table 4-1):

Leveled Sine-Wave Generator	50-Ω BNC Coaxial Cable
Time-Mark Generator	50-Ω BNC Termination
Digital Voltmeter	Screwdriver

See **ADJUSTMENT LOCATIONS 1**

at the back of this manual for location of test points and adjustments.

INITIAL CONTROL SETTINGS

Vertical

POSITION (both)	Midrange
MODE	CH 1
X-Y	On (button in)
CH 1 VOLTS/DIV Variable	Cal detent
Channel 1 AC-GND-DC	GND

Horizontal

POSITION	Midrange
MODE	A
SEC/DIV	5 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
MODE	P-P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A&B SOURCE	VERT MODE
A COUPL	NORM

Storage

STORE/NON-STORE	NON-STORE (button out)

PROCEDURE STEPS

1. Check/Adjust Power Supply DC Levels (R938)

NOTE

Review the information at the beginning of the Adjustment Procedure before starting this step.

a. Connect the digital voltmeter low lead to chassis ground and connect the volts lead to the -8.6 V supply (W961).

b. CHECK—Voltmeter reading is -8.56 to -8.64 V. If the reading is within these limits, skip to part d.

c. ADJUST—The -8.6 V ADJ potentiometer (R938) for a voltmeter reading of -8.6 V.

d. CHECK—Voltage levels of the remaining power supplies listed in Table 5-2 are within the specified limits.

e. Disconnect the test equipment from the instrument.

Table 5-2
Power Supply Limits

Power Supply	Test Point	Reading (Volts)
-8.6 V	W961	-8.56 to -8.64
-5.0 V	W9020	-4.75 to -5.25
+5.0 V	W9068	+4.75 to +5.25
+8.6 V	W960	+8.43 to +8.77
+30 V	W956	+29.1 to +30.9
+102 V	W954	+99.0 to +105.0

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2. Adjust CRT Grid Bias (R851)

a. Connect a 50-Ω termination to the EXT Z AXIS INPUT connector located on the rear panel.

b. Adjust the front-panel FOCUS control to produce a well-defined dot.

c. Rotate the A INTENSITY control fully counter-clockwise.

d. ADJUST—GRID BIAS (R851) for a visible dot. Then back off the Grid Bias potentiometer until the dot just disappears.

e. Disconnect the 50-Ω termination from the EXT Z AXIS INPUT connector.

3. Adjust Astigmatism (R874)

a. Set:

A INTENSITY	Visible display
X-Y	Off (button out)
CH 1 VOLTS/DIV	50 mV
Channel 1 AC-GND-DC	DC

b. Connect the leveled sine-wave generator output via a 50-Ω cable and a 50-Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50 kHz, 4-division display.

d. ADJUST—ASTIG (R874) and the front-panel FOCUS control for the best defined waveform.

e. Disconnect the test equipment from the instrument.

4. Adjust Trace Alignment

a. Position the trace to the center horizontal graticule line.

b. ADJUST—The front-panel TRACE ROTATION control for optimum alignment of the trace with the center horizontal graticule line.

5. Adjust Geometry (R870)

a. Set the A SEC/DIV switch to 0.1 ms.

b. Connect 50 μs time markers from the time-mark generator via a 50-Ω cable and a 50-Ω termination to the CH 1 OR X input connector.

c. Adjust the Channel 1 POSITION control to position the baseline part of the display below the bottom horizontal graticule line.

d. Adjust the SEC/DIV Variable control for 5 markers per division.

e. ADJUST—GEOM (R870) for minimum curvature of the time markers at the left and right edges of the graticule.

f. Set the Channel 1 AC-GND-DC switch to GND.

g. ADJUST—Geom (R870) for minimum curvature of the baseline trace when positioned at the top and bottom horizontal graticule lines using the Channel 1 POSITION control.

h. Set the Channel 1 AC-GND-DC switch to DC.

i. Repeat parts e through h for optimum compromise between the vertical and horizontal displays.

j. Disconnect the test equipment from the instrument.

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VERTICAL

Equipment Required (See Table 4-1):

- Calibration Generator
- Leveled Sine-Wave Generator
- 50-Ω BNC Coaxial Cable
- 50-Ω Precision BNC Cable
- Dual-Input Coupler
- 50-Ω BNC Termination
- 10X Attenuator
- BNC Male-to-Miniature-Probe Tip Adapter
- Low-Reactance Alignment Tool
- Screwdriver
- 10X Probe (Included with instrument

See **ADJUSTMENT LOCATIONS 1**, **ADJUSTMENT LOCATIONS 2**, and **ADJUSTMENT LOCATIONS 4** *at the back of this manual for locations of test points and adjustments.*

INITIAL CONTROL SETTINGS

Vertical (Both Channels)

POSITION	Midrange
MODE	CH 1
X-Y	Off (button out)
BW LIMIT	On (button in)
VOLTS/DIV	10 mV
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC-GND-DC	GND

Horizontal

POSITION	Midrange
MODE	A
A SEC/DIV	0.5 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A Trigger

VAR HOLDOFF	NORM
MODE	P-P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A&B SOURCE	VERT MODE
A COUPL	NORM

Storage

STORE/NON-STORE	NON-STORE (button out)

PROCEDURE STEPS

1. Adjust Step Attenuator Balance (R10 and R60)

a. Position the trace on the center horizontal graticule line using the Channel 1 POSITION control.

b. Set the CH 1 VOLTS/DIV switch to 5 mV.

c. ADJUST—STEP ATTN BAL (R10) to set the trace on the center horizontal graticule line.

d. Set the CH 1 VOLTS/DIV switch to 10 mV.

e. Repeat parts a through d until there is no trace shift when changing the CH 1 VOLTS/DIV switch from 50 mV to 5 mV.

f. Set the Vertical MODE switch to CH 2.

g. Repeats parts a through e for Channel 2, adjusting Step Attn Bal (R60) in part c.

2. Adjust 2/5 mV DC Balance (R83 and R33)

a. Set the CH 2 VOLTS/DIV switch to 5 mV.

b. Position the trace on the center horizontal graticule line using the Channel 2 POSITION control.

c. Set the CH 2 VOLTS/DIV switch to 2 mV.

d. ADJUST—2/5 mV DC BAL (R83) to set the trace on the center horizontal graticule line.

e. Repeat parts a through d until there is no trace shift when changing the CH 2 VOLTS/DIV switch from 5 mV to 2 mV.

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f. Set the Vertical MODE switch to CH 1.

g. Repeat parts a through e for Channel 1, adjusting 2/5 mV Dc Bal (R33) in part d.

3. Adjust Channel 1 Variable Balance (R25)

a. Set both VOLTS/DIV switches to 2 mV.

b. Rotate the CH 1 VOLTS/DIV Variable control fully counterclockwise.

c. Position the trace on the center horizontal graticule line using the Channel 1 POSITION control.

d. Rotate the CH 1 VOLTS/DIV Variable control clockwise to the CAL detent.

e. ADJUST—VAR BAL (R25) to set the trace to the center horizontal graticule line.

f. Repeat parts b through e until there is no trace shift between the fully clockwise and the fully counterclockwise positions of the CH 1 VOLTS/DIV Variable control.

g. Return the CH 1 VOLTS/DIV Variable control to the CAL detent.

4. Adjust Channel 2 Invert Balance (R75)

a. Set the Vertical MODE switch to CH 2.

b. Position the trace on the center horizontal graticule line using the Channel 2 POSITION control.

c. Set the INVERT button to On (button in).

d. ADJUST—INVERT BAL (R75) to set the trace to the center horizontal graticule line.

e. Set the INVERT button to Off (button out).

f. Repeat parts b through e until there is no trace shift when switching the INVERT button between the On and Off positions.

5. Adjust MF/LF Compensation and Gain Balance (C53, R97, C3, and R47)

a. Set:

VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	DC
A SEC/DIV	20 μs

b. Connect the high-amplitude square wave output via a 50-Ω cable, a 10X attenuator, and a 50-Ω termination to the CH 2 OR Y input connector.

c. Set the generator to produce a 10-kHz, 5-division display.

d. Set the top of the display on the center horizontal graticule line using the Channel 2 POSITION control.

e. ADJUST—MF/LF COMP (C53) and MF/LF Gain Bal (R97) for the best front corner and flat top.

f. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the Vertical MODE switch to CH 1.

g. Set the top of the display on the center horizontal graticule line using the Channel 1 POSITION control.

h. ADJUST—MF/LF COMP (C3) and MF/LF Gain Bal (R47) for the best front corner and flat top.

i. Disconnect the test equipment from the instrument.

6. Adjust Vertical Gain (R145, R195, R76, and R26)

a. Connect a 50 mV standard-amplitude signal from the calibration generator via a 50-Ω cable to the CH 1 OR X input connector.

b. Set the A SEC/DIV switch to 0.2 ms.

c. Center the display within the graticule using the Channel 1 POSITION control.

d. ADJUST—CH1 GAIN (R145) for an exact 5-division display.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

f. Center the display within the graticule using the Channel 2 POSITION control.

g. ADJUST—CH2 GAIN (R195) for an exact 5-division display.

h. Repeat parts d and g until the gain of the two channels are identical.

i. Change the generator output to 10 mV.

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j. Set:

Vertical MODE	CH 2
VOLTS/DIV	2 mV

k. ADJUST—2mV GAIN (R76) for an exact 5-division display.

l. Set Channel 2 AC-GND-DC switch to GND.

m. CHECK—That no trace shift occurs when switching between the 5 mV and 2 mV positions of the CH 2 VOLTS/DIV switch. If trace shift is observed, repeat Step 2 of this procedure.

n. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the Vertical MODE switch to CH 1.

o. ADJUST—2mV GAIN (R26) for an exact 5-division display.

p. Set Channel 1 AC-GND-DC switch to GND.

q. CHECK—That no trace shift occurs when switching between the 5 mV and 2 mV positions of the CH 1 VOLTS/DIV switch. If trace shift is observed, repeat Step 2 of this procedure.

7. Check Deflection Accuracy and Variable Range

a. Set both AC-GND-DC switches to DC.

b. CHECK—Deflection accuracy is within the limits given in Table 5-3 for each CH 1 VOLTS/DIV switch setting and corresponding standard-amplitude signal. When at the 20 mV VOLTS/DIV switch setting, rotate the CH 1 VOLTS/DIV Variable control fully counter clockwise and CHECK—that the display decreases to 2 divisions or less. Then return the CH 1 VOLTS/DIV Variable control to the CAL detent and continue with the 50 mV check.

c. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

d. Repeat part b using the Channel 2 controls.

Table 5-3
Deflection Accuracy Limits

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Accuracy Limits (Divisions)
2 mV	10 mV	4.90 to 5.10
5 mV	20 mV	3.92 to 4.08
10 mV	50 mV	4.90 to 5.10
20 mV	0.1 V	4.90 to 5.10
50 mV	0.2 V	3.92 to 4.08
0.1 V	0.5 V	4.90 to 5.10
0.2 V	1 V	4.90 to 5.10
0.5 V	2 V	3.92 to 4.08
1 V	5 V	4.90 to 5.10
2 V	10 V	4.90 to 5.10
5 V	20 V	3.92 to 4.08

8. Adjust Acquisition Position Registration (R2214 and R2245)

a. Set:

VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	GND
A SEC/DIV	10 μs

b. Position the Channel 2 trace exactly on the center horizontal graticule line using the Channel 2 POSITION control.

c. Set:

STORE/NON-STORE	STORE (button in)
SAVE/CONT	CONT
Acquisition MODE	AVERAGE
1K/4K	1K

d. ADJUST—CH2 OFFSET (R2214) to position the Channel 2 trace exactly on the center horizontal graticule line.

e. CHECK—Channel 2 trace remains within 0.5 division of the center horizontal graticule line when switching from NON-STORE to STORE at VOLTS/DIV switch settings from 2 mV/div to 5 V/div.

f. Set:

Vertical MODE	CH 1
STORE/NON-STORE	NON-STORE (button out)

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g. Position the Channel 1 trace exactly on the center horizontal graticule line using the Channel 1 POSITION control.

h. Set STORE/NON-STORE switch to STORE (button in).

i. ADJUST—CH1 OFFSET (R2245) to position the Channel 1 trace exactly on the center horizontal graticule line.

j. CHECK—Channel 1 trace remains within 0.5 division of the center horizontal graticule line when switching from NON-STORE to STORE at VOLTS/DIV switch settings from 2 mV/div to 5 V/div.

9. Adjust Acquisition Gain (R2283 and R2273)

a. Set:

VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	DC
A SEC/DIV	0.2 ms
STORE/NON-STORE	STORE (button in)

b. Set the calibration generator output to 50 mV.

c. Center the display within the graticule using the Channel 2 POSITION control.

d. ADJUST—CH1 GAIN (R2283) for an exact 5-division display.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

f. Center the display within the graticule using the Channel 2 POSITION control.

g. ADJUST—CH2 GAIN (R2273) for an exact 5-division display.

h. Disconnect the test equipment from the instrument.

10. Adjust Acquisition Add Mode (R2278)

a. Set:

Vertical MODE	BOTH and ALT
VOLTS/DIV (both)	20 mV

b. Connect a 50 mV standard-amplitude signal from the calibration generator via a 50-Ω cable and a dual-input coupler to the CH 1 OR X and CH 2 OR Y input connectors.

c. Center both displays equally above and below the center horizontal graticule line using the Channel 1 and Channel 2 POSITION controls.

NOTE

Repeat step 9 if the amplitude of the Channel 1 and Channel 2 displays are not the same.

d. Set the Vertical MODE switch to ADD.

e. ADJUST—ADD GAIN (R2278) for an exact 5 divisions of display.

f. Disconnect the test equipment from the instrument.

11. Check Store Deflection Accuracy

a. Set:

Vertical MODE	CH 1
VOLTS/DIV (both)	2 mV

b. Connect a 10 mV standard-amplitude signal from the calibration generator via a 50-Ω cable to the CH 1 OR X input connector.

c. Use the CURSORS control and SELECT C1/C2 switch (push in the CURSORS control knob) to set one cursor at the bottom of the square wave and the other cursor at the top of the square wave.

d. CHECK—Deflection accuracy is within the limits given in Table 5-4 for each CH 1 VOLTS/DIV switch setting and corresponding standard-amplitude signal.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

f. Repeat parts c and d for each CH 2 VOLTS/DIV switch setting.

g. Disconnect the test equipment from the instrument.

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Table 5-4
Store Deflection Accuracy

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Divisions of Deflection	Voltage Readout Limits
2 mV	10 mV	4.90 to 5.10	9.70 to 10.30 mV
5 mV	20 mV	3.92 to 4.08	19.40 to 20.60 mV
10 mV	50 mV	4.90 to 5.10	48.5 to 51.5 mV
20 mV	0.1 V	4.90 to 5.10	97.0 to 103.0 mV
50 mV	0.2 V	3.92 to 4.08	194.0 to 206.0 mV
0.1 V	0.5 V	4.90 to 5.10	0.485 to 0.515 V
0.2 V	1 V	4.90 to 5.10	0.970 to 1.030 V
0.5 V	2 V	3.92 to 4.08	1.940 to 2.060 V
1 V	5 V	4.90 to 5.10	4.85 to 5.15 V
2 V	10 V	4.90 to 5.10	9.70 to 10.30 V
5 V	20 V	3.92 to 4.08	19.40 to 20.60 V

12. Adjust Store Y Offset and Gain (R9224 and R9222)

a. Press in the SETUP ADV FUNCT button to select ADVANCED FUNCTIONS menu.

b. Press in the Diag Menu button to select DIAGNOSTICS menu and then select Cal and Box. Press RUN to select the box.

c. ADJUST-YGAIN (R9222) to size the inner cal box to exactly 6 vertical divisions.

d. ADJUST-YOFFSET (R9224) to align the horizontal center cross-hair with the horizontal center graticule.

e. INTERACTION: Repeat parts c and d until the height of the inside box is exactly 6 vertical divisions and the horizontal cross-hair is aligned with the center graticule line.

f. Press the EXIT button and return to the DIAGNOSTICS menu.

13. Adjust Acquisition Position Offset (R7325 and R7335)

a. Set:

Vertical MODE	BOTH and ALT
AC-GND-DC (both)	GND

b. Select Cal and Vert in the DIAGNOSTICS menu and press the RUN button. The display will consist of three short and two baseline traces on the screen.

c. Vertically position the two baseline traces exactly on the center horizontal graticule line.

d. Press in momentary the CURSORS control knob to vertically centered the two short movable traces near the two overlapping baseline traces.

e. Vertically position Channel 1 baseline trace to the top and bottom of the screen using the Channel 1 POSITION control. Note the separation of the short trace from the baseline trace at the top and bottom of the screen.

f. ADJUST—CH1 ACQ POS OFFSET (R7325) for minimum separation of the Channel 1 baseline and the short trace at the top and bottom of the screen.

g. Repeat part e for Channel 2 baseline trace.

h. ADJUST—CH2 ACQ POS OFFSET (R7335) for minimum separation of the Channel 2 baseline and the short trace at the top and bottom of the screen.

i. Press the EXIT and SETUP ADV FUNCT buttons to return the instrument to a display mode.

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14. Adjust Attenuator Compensation (C12, C11, C5, C4, C62, C61, C55, C54)

a. Set:

Vertical MODE	CH 1
VOLTS/DIV (both)	0.1 V
AC-DC-GND	DC
SEC/DIV	20 μs
STORE/NON-STORE	NON-STORE (button out)

b. Connect the high-amplitude square wave output via a 50-Ω termination, a probe-tip-to-BNC adapter, and the 10X probe to the CH 1 OR X input connector.

c. Set the generator to produce a 1-kHz, 5-division display and compensate the probe using the probe compensation adjustment (see the probe instruction manual).

d. Replace the probe and probe-tip-to-BNC adapter with a 50-Ω cable, connect the 50-Ω termination to the end of the cable.

e. Set the generator to produce a 5-division display.

NOTE

Use Table 5-5 to identify the correct capacitor for each channel adjustment.

f. ADJUST—The 10X ATTN (C12) for best front corner.

g. Replace the 50-Ω cable and 50-Ω termination with the probe and probe-tip-to-BNC adapter. Connect the 50-Ω termination to the high-amplitude square wave output.

Table 5-5
Attenuator Compensation Adjustments

Adjustment	Channel 1	Channel 2
10X ATTN (LF Comp)	C12	C62
10X ATTN (Input C)	C11	C61
100X ATTN (LF Comp)	C5	C55
100X ATTN (Input C)	C4	C54

h. Set the generator to produce a 5-division display.

i. ADJUST—The 10X ATTN (C11) for best flat top.

j. Repeat parts d through i until no further improvement is noted.

k. Set the CH 1 VOLTS/DIV switch to 1 V.

l. Replace the probe and probe-tip-to-BNC adapter with the 50-Ω cable. Connect the 50-Ω termination to the end of the cable.

m. Set the generator to produce a 5-division display.

n. ADJUST—The 100X ATTN (C5) for best front corner.

o. Replace the 50-Ω cable and 50-Ω termination with the probe and probe-tip-to-BNC adapter.

p. Set the generator to produce a 5-division display.

q. ADJUST—The 100X ATTN (C4) for best flat top.

r. Repeat parts l through q until no further improvement is noted.

s. Set the Vertical MODE switch to CH 2.

t. Repeat parts b through r for Channel 2 attenuators.

u. Disconnect the test equipment from the instrument.

15. Adjust High-Frequency Compensation (C237, R240 and R241) and Channel 2 High-Frequency Compensation (C180)

a. Set:

Vertical MODE	CH 1
BW LIMIT	Off (button out)
VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	DC
A SEC/DIV	0.05 μs
A & B SOURCE	VERT MODE

b. Connect the positive-going fast-rise square wave output via a 50-Ω precision cable, a 10X attenuator, and a 50-Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 1-MHz, 5-division display.

d. Set the top of the display to the center horizontal graticule line using the Channel 1 POSITION control.

e. ADJUST—HF COMP (C237) for 2% overshoot (0.1 division) on the displayed signal.

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f. ADJUST—HF COMP (R240 and R241) for best flat top on the front corner.

g. Repeat parts e and f until no further improvement is noted.

h. Set the CH 1 VOLTS/DIV switch to 5 mV.

i. Set the generator to produce a 5-division display.

j. CHECK—Display aberrations are within 4% (0.2 division or less) for the following VOLTS/DIV switch settings: 5 mV through 50 mV. Adjust the generator output and add or remove the 10X attenuator as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

k. CHECK—Display aberrations are within 6% (0.25 division or less) for the following VOLTS/DIV switch settings: 0.1 V and 0.2 V. Adjust the generator output and add or remove the 10X attenuator as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

l. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector and reconnect the 10X attenuator. Set the Vertical MODE switch to CH 2.

m. Set the generator to produce a 5-division display.

n. Set the top of the display to the center horizontal graticule line using the Channel 2 POSITION control.

o. ADJUST—CH2 HF COMP (C180) to match the Channel 2, 10 mV compensation to the Channel 1 10 mV compensation.

p. Set the CH 2 VOLTS/DIV switch to 5 mV.

q. Repeat parts i through k for Channel 2.

16. Adjust 2-mV Peaking Compensation (C76 and C26)

a. Set both VOLTS/DIV switches to 2 mV.

b. Set the generator to produce a 5-division display. Add X10 attenuator as necessary.

c. Set the top of the display to the center horizontal graticule line using the Channel 2 POSITION control.

d. ADJUST—2mV PEAK (C76) for 4% (0.2 divisions or less) aberrations of the displayed signal.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the Vertical MODE switch to CH 1.

f. ADJUST—2mV PEAK (C26) for 4% (0.2 divisions or less) aberrations of the displayed signal.

17. Adjust Acquisition High Frequency Peaking (C2207, C2202, R2298, and R2297)

a. Set:

VOLTS/DIV (both)	10 mV
STORE/NON-STORE	STORE (button in)
SAVE/CONT	CONT
TRIG POS	Post Trigger
Acquisition MODE	AVERAGE

b. Set the generator to produce a 5-division display.

c. Set the top of the display to the center horizontal graticule line using the Channel 1 POSITION control.

d. ADJUST—CH1 HF PEAK (C2207 and R2298) for best front corner.

e. Press in the SAVE/CONT button to select SAVE.

f. CHECK—Display aberrations are within 4% (0.2 division or less).

g. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

h. Press in the SAVE/CONT button to select CONT.

i. ADJUST—CH2 HF PEAK (C2202 and R2297) for best front corner.

j. Press in the SAVE/CONT button to select SAVE.

k. CHECK—Display aberrations are within 4% (0.2 division or less).

l. Disconnect the test equipment from the instrument.

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NOTE

Install the instrument cabinet for the remaining vertical checks and allow a 20-minute warm-up period before continuing with the Adjustment Procedure. See the "Cabinet" remove and replace instructions located in the "Maintenance" section of the manual.

18. Check Bandwidth Limit Operation

a. Set:

Vertical POSITION (both)	Midrange
BW LIMIT	On (button in)
VOLTS/DIV Variable (both)	CAL detent
AC-GND-DC (both)	DC
A SEC/DIV	20 μs
STORE/NON-STORE	NON-STORE (button out)

b. Connect the leveled sine-wave generator output via a 50-Ω cable and a 50-Ω termination to the CH 2 OR Y input connector.

c. Set the generator to produce a 50-kHz, 6-division display.

d. Adjust the generator output frequency until the display amplitude decreases to 4.2 divisions.

e. CHECK—Generator output frequency is between 18 MHz and 22 MHz.

f. Move the cable from CH 2 OR Y input connector to the CH 1 OR X input connector.

g. Set the Vertical MODE to CH 1.

h. Repeat parts d and e.

19. Check Bandwidth

a. Set:

BW LIMIT	Off (button out)
VOLTS/DIV (both)	2 mV

b. Set the generator to produce a 50-kHz, 6-division display.

c. CHECK—Display amplitude is 4.2 divisions or greater as the generator output frequency is increased up to the value shown in Table 5-6 for the corresponding VOLTS/DIV switch setting.

Table 5-6
Settings for Bandwidth Checks

VOLTS/DIV Switch Setting	Generator Output Frequency
2 mV	80 MHz
5 mV to 0.5 V	100 MHz

d. Repeat parts b and c for all CH 1 VOLTS/DIV switch settings, up to the output-voltage upper limit of the sine-wave generator being used.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the Vertical MODE switch to CH 2.

f. Repeat parts b and c for all CH 2 VOLTS/DIV switch settings, up to the output-voltage upper limit of the sine-wave generator being used.

20. Check Repetitive Store Mode and Bandwidth

a. Set:

CH 2 VOLTS/DIV	10 mV
A SEC/DIV	0.2 ms

b. Set the generator to produce a 50-kHz, 6-division display.

c. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

d. Set the generator to produce a 100-MHz display.

e. Set:

STORE/NON-STORE	STORE (button in)
SAVE/CONT	CONT

NOTE

Allow the points to accumulate for a few seconds before saving the display.

f. Press in the SAVE/CONT button to select SAVE.

g. CHECK—The 100-MHz display is saved.

h. CHECK—The display amplitude is 4.2 divisions or greater.

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i. Set:

Vertical MODE	BOTH and ALT
SAVE/CONT	CONT

j. Repeat parts f through h.

k. Disconnect the test equipment from the instrument.

NOTE

To continue with the Adjustment Procedure, remove the instrument cabinet and allow a 20–minute time period to elapse before continuing with the Adjustment Procedure. See the Cabinet removal instructions located in the Maintenance section of the manual.

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HORIZONTAL

Equipment Required (See Table 4-1):

Calibration Generator	50-Ω Coaxial Cable
Leveled Sine-Wave Generator	50-Ω BNC Termination
Time-Mark Generator	Low-Capacitance Alignment Tool
Test Oscilloscope	Screwdriver

See **ADJUSTMENT LOCATIONS 1, ADJUSTMENTS 3** and **ADJUSTMENT LOCATIONS 4**

at the back of the manual for test points and adjustment locations.

INITIAL CONTROL SETTINGS

Vertical

POSITION (both)	Midrange
MODE	CH 1
X-Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	0.5 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC-GND-DC	DC

Horizontal

POSITION	Midrange
MODE	A
A and B SEC/DIV	0.1 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counter-clockwise

B TRIGGER

SLOPE	Positive (button out)
LEVEL	Fully clockwise

A TRIGGER

VAR HOLDOFF	NORM
MODE	P-P AUTO
SLOPE	Positive (button in)
LEVEL	Midrange
A&B SOURCE	VERT MODE
A COUPL	NORM
A EXT COUPL	DC

Storage

STORE/NON-STORE	NON-STORE (button out)

PROCEDURE STEPS

1. Adjust Horizontal Amplifier Gain (R740 and R730)

a. Connect 0.1-ms time markers from the time-mark generator via a 50-Ω cable and a 50-Ω termination to the CH 1 OR X input connector.

b. Use the Horizontal POSITION control to align the 1st time marker with the 1st vertical graticule line.

c. ADJUST—A SWEEP GAIN (R740) for 1 time marker per division over the center 8 divisions.

NOTE

When making timing measurements, use as a reference the tips of the time markers positioned at the center horizontal graticule line.

d. Set the Horizontal MODE switch to B.

e. ADJUST—B SWEEP GAIN (R730) for 1 time marker per division.

2. Adjust X10 Horizontal Amplifier Gain (R754)

a. Set:

Horizontal MODE	A
X10 Magnifier	On (knob out)

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b. Select 10-μs time markers from the time-mark generator.

c. Align the nearest time marker to the 1st vertical graticule line with the 1st graticule line.

d. ADJUST—X10 GAIN (R754) for 1 time marker per division over the center 8 divisions.

3. Adjust Magnifier Registration (R749)

a. Set the A SEC/DIV switch to 0.2 ms.

b. Select 1-ms time markers from the time-mark generator.

c. Position the middle time marker to the center vertical graticule line using the Horizontal POSITION control.

d. Set the X10 Magnifier to Off (knob in).

e. ADJUST—MAG (R749) to position the middle time marker to the center vertical graticule line.

f. Set the X10 Magnifier to On (knob out) and CHECK—for no horizontal shift in the time marker.

g. Repeat parts c through f until no further improvement is noted.

4. Adjust/Check 4K to 1K Display Compress (R7507)

a. Set:

A SEC/DIV	50 μs
STORE/NON-STORE	STORE (button in)
SAVE/CONT	CONT
1K/4K	4K

b. Set Store Reset plug (P9104) to reset position.

c. Select 0.2-ms time markers from the time-mark generator.

d. ADJUST—RATIO ADJ (R7507) for 1 time marker per division over the center 8 divisions.

e. Set the Store Reset plug (P9104) to normal position.

f. Select 0.1-ms time markers from the time-mark generator and check that the time markers are 2 divisions apart.

g. Rotate the SEC/DIV Variable control out of detent.

h. CHECK—For 2 time markers per division over the center 8 divisions.

5. Adjust Delay Timing and Readout (R646, R652, and R6119)

a. Set:

Horizontal MODE	BOTH
A SEC/DIV	0.1 ms
B SEC/DIV	1 μs
SEC/DIV Variable	CAL detent
STORE/NON-STORE	NON-STORE (button out)

b. Select 0.1-ms time markers from the time-mark generator.

c. Adjust the A/B SWP SEP control to separate the A and B Sweeps.

d. Position the start of the trace exactly on the 1st vertical graticule line using the Horizontal POSITION control.

e. Rotate the B DELAY TIME POSITION control fully counter clockwise.

f. ADJUST—DELAY START (R646) so that the intensified zone starts at 0.1 divisions.

g. Rotate the B DELAY TIME POSITION control fully clockwise.

h. ADJUST—D-END (R652) so that the intensified zone starts at 10.1 divisions.

i. Repeat parts e through h until no further improvement is noted.

j. Rotate the B DELAY TIME POSITION control until the 2nd A-Sweep time marker is aligned with a selected reference vertical graticule line on the B Sweep. Record the DLY = readout for part l.

k. Rotate the B DELAY TIME POSITION control until the 10th A-Sweep time marker is aligned with the same selected reference vertical graticule line on the B Sweep as in part j.

l. ADJUST—DLY RO (R6119) until the DLY = readout display between the 2nd time marker and the 10th time marker is 0.800 ms.

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6. Adjust High-Speed Timing (C703 and C713)

a. Set:

Horizontal MODE	A
A SEC/DIV	1 μs
A SEC/DIV Variable	CAL detent
B DELAY TIME POSITION	Fully counter-clockwise

b. Select 1-μs time markers from the time-mark generator.

c. ADJUST—A HIGH SPEED TIMING (C703) for 1 time marker per division

d. Set:

Horizontal MODE	B
A SEC/DIV	2 μs
B SEC/DIV	1 μs

e. ADJUST—B HIGH SPEED TIMING (C713) for 1 time marker per division over the center 8 divisions.

7. Adjust 5 ns Timing and Linearity (C775 and C785)

a. Set:

CH 1 VOLTS/DIV	0.2 V
Horizontal POSITION	Midrange
Horizontal MODE	A
A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

b. Select 10-ns time markers from the time-mark generator.

c. Align the time markers with the vertical graticule lines using the Horizontal POSITION control.

d. ADJUST—5 ns Timing (C775 and C785 alternately) for one time marker every 2 divisions over the center 8 divisions of the magnified sweep.

e. CHECK—Time markers between the 2nd and 4th vertical graticule lines should be aligned within 0.05 division. If not, a slight compromise between timing and linearity should be made by readjusting the 5-ns Timing capacitors (C775 and C785).

8. Check Timing Accuracy and Linearity

a. Set:

CH 1 VOLTS/DIV	0.5 V
X10 Magnifier	Off (knob in)

b. Select 50-ns time markers from the time-marker generator.

c. Adjust the A TRIGGER LEVEL control for a stable, triggered display.

d. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

e. CHECK—Timing accuracy is within 2% (0.16 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions).

NOTE

For checking the timing accuracy of the A SEC/DIV switch settings from 50 ms to 0.5 μs, watch the time marker tips only at the 2nd and 10th vertical graticule lines while adjusting the Horizontal POSITION control.

f. Repeat parts c through e for the remaining A SEC/DIV and time-mark generator setting combinations shown in Table 5-7 under the Normal (X1) column.

g. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

h. Select 10-ns time markers from the time-mark generator.

i. Use the Horizontal POSITION control to align the 1st time marker that is 25 ns beyond the start of the sweep with the 2nd vertical graticule line.

j. CHECK—Timing accuracy is within 3% (0.24 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions). Exclude any portion of the sweep past the 100th magnified division.

k. Repeat parts i and j for the remaining A SEC/DIV and time-mark generator setting combinations shown in Table 5-7 under the X10 Magnified column.

l. Set:

Horizontal MODE	B
A SEC/DIV	0.1 μs
B SEC/DIV	0.05 μs
X10 Magnifier	Off (knob in)

m. Repeat parts b through k for the B Sweep. Keep the A SEC/DIV switch one setting slower than the B SEC/DIV switch.

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Table 5-7

Settings for Timing Accuracy Checks

SEC/DIV Switch Setting	Time-Mark Generator Setting	
	Normal (X1)	X10 Magnified
0.05 μs	50 ns	10 ns
0.1 μs	0.1 μs	10 ns
0.2 μs	0.2 μs	20 ns
0.5 μs	0.5 μs	50 ns
1 μs	1 μs	0.1 μs
2 μs	2 μs	0.2 μs
5 μs	5 μs	0.5 μs
10 μs	10 μs	1 μs
20 μs	20 μs	2 μs
50 μs	50 μs	5 μs
0.1 ms	0.1 ms	10 μs
0.2 ms	0.2 ms	20 μs
0.5 ms	0.5 ms	50 μs
1 ms	1 ms	0.1 ms
2 ms	2 ms	0.2 ms
5 ms	5 ms	0.5 ms
10 ms	10 ms	1 ms
20 ms	20 ms	2 ms
50 ms	50 ms	5 ms
A Sweep Only		
0.1 s	0.1 s	10 ms
0.2 s	0.2 s	20 ms
0.5 s	0.5 s	50 ms

9. Check Delay Time Differential Accuracy

a. Set:

Channel 1 AC-GND-DC	GND
Horizontal MODE	BOTH
A and B SEC/DIV	0.2 ms
X10 Magnifier	Off (knob in)
A TRIGGER MODE	P-P AUTO

b. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

c. Rotate the B DELAY TIME POSITION control fully counterclockwise.

d. CHECK—Intensified portion of the trace starts within 0.5 division of the start of the sweep.

e. Rotate the B DELAY TIME POSITION control fully clockwise.

f. CHECK—Intensified portion of the trace is past the 11th vertical graticule line.

g. Set the A and B SEC/DIV switch to 0.5 μs.

h. Repeat parts b through f.

i. Set:

Channel 1 AC-GND-DC	DC
B SEC/DIV	0.05 μs
B DELAY TIME POSITION	Fully counter-clockwise

j. Select 0.5-μs time markers from the time-mark generator.

k. Rotate the B DELAY TIME POSITION control so that the top of the 2nd time marker on the B Sweep is aligned with a selected reference vertical line. Record the DLY = readout for part m.

l. Rotate the B DELAY TIME POSITION control fully clockwise until the top of the 10th time marker on the B Sweep is aligned with the same selected reference vertical line as in part k. Record the DLY = readout for part m.

m. CHECK—Delay time readout is within the limits given in Table 5-8 (Delay Readout Limits column) by subtracting the delay time reading in part k from part l.

n. Repeat parts k through m for the remaining B SEC/DIV and time-mark generator settings given in Table 5-8, check the 8-division delay time accuracy for each A SEC/DIV switch setting given in column 1 of the table.

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Table 5-8
Settings for Delay Time Differential Checks

Time-Mark Generator and A SEC/DIV Settings	B SEC/DIV Setting	Eight Division Delay	Delay Readout Limits
0.5 μs	0.05 μs	4.000 μs	3.935 μs to 4.065 μs
5 μs	0.5 μs	40.00 μs	39.35 μs to 40.65 μs
50 μs	5 μs	400.0 μs	393.5 μs to 406.5 μs
0.5 ms	50 ms	4.000 ms	3.935 ms to 4.065 ms
5 ms	0.5 ms	40.00 ms	39.35 ms to 40.65 ms
50 ms	5 ms	400.0 ms	393.5 ms to 406.5 ms
0.5 s	50 ms	4.000 s	3.935 s to 4.065 s

10. Adjust Vector Generator (R6312 and R6321)

a. Press in the SETUP ADV FUNCT button to display the ADVANCED FUNCTIONS menu.

b. Press the Diag Menu button to select the DIAGNOSTICS menu and then select Cal and Box. Press RUN to select the box.

c. ADJUST—XVECT (R6321) and YVECT (R6312) to achieve the best corners of the inner 6x8 cal box.

d. ADJUST—XVECT (R6321) and YVECT (R6312) for best displays of the delta symbols (no tails or tilting) located at each of the four corners on the screen.

11. Adjust Store X Offset and Gain (R9214 and R9212)

a. ADJUST—XGAIN (R9212) to size the inner cal box to exactly 8 horizontal divisions.

b. ADJUST—XOFFSET (R9214) to align the vertical cross-hair with the vertical center graticule.

c. INTERACTION: Repeat parts a and b until the inside cal box is exactly 8 horizontal divisions wide and the vertical cross-hair is aligned with the center graticule line.

d. Press the EXIT and the SETUP ADV FUNCT buttons to return the instrument to a display mode.

12. Adjust Horizontal Position Registration (R739)

a. Set:

Channel 1 AC-GND-DC	GND
Horizontal MODE	A
A SEC/DIV	0.1 ms
STORE/NON-STORE	STORE (button in)
1K/4K	1K

b. Position the trace on the center horizontal graticule line using the Vertical POSITION control.

c. Position the sweep start of the display exactly on the extreme left vertical graticule line using the Horizontal POSITION control.

d. Set the STORE/NON-STORE switch to NON-STORE (button out)

e. ADJUST—HORIZ POS REG (R739) to position the start of the trace exactly on the extreme left vertical graticule line.

13. Check Store Differential and Cursor Time Difference Accuracy

a. Set the STORE/NON-STORE switch to STORE (button in)

b. Use the Channel 1 POSITION control to center the base line vertically and the Horizontal POSITION control to align the start of the trace with the 1st vertical graticule line.

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c. Use the CURSORS control and SELECT C1/C2 switch (push in the CURSORS control knob) to set one cursor exactly on the 2nd vertical graticule line and position the active cursor to the right using the CURSORS control until ΔT readout displays 0.800 ms.

d. CHECK—Graticule indication of cursor difference at the 10th vertical graticule line is within 0.16 division.

e. Set the Channel 1 AC-GND-DC switch to DC.

f. Select 0.1-ms time markers from the time-mark generator.

g. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

h. Press in the SAVE/CONT button to select SAVE for a stable display.

i. Use the CURSORS control and SELECT C1/C2 switch (push in the CURSORS control knob) to set the first cursor on the trailing edge of the 2nd time marker.

j. Press in the CURSORS control knob to activate the second cursor.

k. Set the second cursor on the trailing edge of the 10th time marker at the same voltage level as on the 2nd time marker.

l. CHECK—The ΔT readout is between 0.798 ms and 0.802 ms.

m. Press in the SAVE/CONT button to select CONT.

n. Set the A SEC/DIV switch to 0.5 μs.

o. Select 0.5-μs time markers from the time-mark generator.

p. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

NOTE

Allow the points to accumulate for a few seconds before saving the display.

q. Repeat parts h through k.

NOTE

Pulses with fast rise and fall times have only a few sample points, and it may not be possible to place the cursors at exactly the same voltage levels.

r. CHECK—The ΔT readout is between 3.97 μs and 4.03 μs.

s. Disconnect the test equipment from the instrument.

14. Adjust X Gain (R760)

a. Set:

X-Y	On (button in)
CH 1 VOLTS/DIV	10 mV
Horizontal POSITION	Midrange
STORE/NON-STORE	NON-STORE (button out)

b. Connect the standard-amplitude signal from the Calibration Generator via a 50-Ω cable to the CH 1 OR X input connector.

c. Use the Channel 2 POSITION and Horizontal POSITION controls to center the display.

d. Set the generator to produce a 50 mV signal.

e. ADJUST—X-GAIN (R760) for exactly 5 divisions of horizontal deflection.

f. Disconnect the test equipment from the instrument.

15. Check A-Sweep Holdoff

a. Set:

X-Y	Off (button out)
Horizontal MODE	A
A SEC/DIV	1 ms
VAR HOLDOFF	NORM

b. Connect the test oscilloscope and its 10X probe tip to the front end of R707 (toward the front panel) which is located on the Timing circuit board.

c. CHECK—The A-Sweep holdoff is greater then 3 ms but less than 7 ms.

d. Rotate the VAR HOLDOFF control to the maximum clockwise position (MAX).

e. CHECK—The A-Sweep holdoff has increased by a factor of 10 or more.

f. Disconnect the test oscilloscope 10X probe from R707.

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TRIGGER

Equipment Required (See Table 4-1):

- Calibration Generator
- Leveled Sine-Wave Generator
- Low-Frequency Generator
- 50-Ω BNC Coaxial Cable
- Dual-Input Coupler
- BNC T-Connector
- 50-Ω BNC Termination
- 600-Ω BNC Termination
- Screwdriver

See **ADJUSTMENT LOCATIONS 1** and **ADJUSTMENT LOCATIONS 3** at the back of the manual for test points and adjustment locations.

INITIAL CONTROL SETTINGS

Vertical (Both Channels)

POSITION	Midrange
MODE	BOTH-ALT
X-Y	Off (button out)
BW LIMIT	Off (button out)
VOLTS/DIV	0.5 V
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC-GND-DC	GND

Horizontal

POSITION	Midrange
MODE	A
A and B SEC/DIV	1 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counter-clockwise

B TRIGGER

SLOPE	Positive (button out)
LEVEL	Midrange

A TRIGGER

VAR HOLDOFF	NORM
MODE	P-P AUTO
SLOPE	Positive (button out)
LEVEL	Midrange
A & B SOURCE	VERT MODE
A COUPL	NORM
A EXT COUPL	AC

Storage

STORE/NON-STORE	NON-STORE (button out)

PROCEDURE STEPS

1. Adjust Channel 1 Trigger Offset (R309)

a. Set the Channel 1 trace and the Channel 2 trace to the center horizontal graticule line using the Channel 1 and Channel 2 POSITION controls.

b. Connect the digital voltmeter low lead to chassis ground and the high (volts) lead to TP460, located on the bottom side of the Main circuit board.

c. CHECK—Note the offset voltage reading at TP460 for use in part e.

d. Set the A & B SOURCE switch to CH 1.

e. ADJUST—TRIG OFFSET (R309) so that the voltage reading is the same as that obtained in part c.

f. Set the A & B SOURCE switch to CH 2.

g. Repeat parts c through f until there is 1 mV or less difference in the voltmeter readings between the CH 1 and CH 2 positions of the A & B SOURCE switch.

h. Disconnect the test equipment from the instrument.

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2. Adjust A and B Trigger Sensitivity (R471 and R627)

a. Set:

Vertical MODE	CH 1
CH 1 VOLTS/DIV	0.1 V
AC–GND–DC (both)	AC
A SEC/DIV	10 μs
A & B SOURCE	VERT MODE

b. Connect the leveled sine-wave generator output via a 50-Ω cable and a 50-Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50-kHz, 2.2-division display.

d. Set the CH 1 VOLTS/DIV switch to 1 V.

e. ADJUST—TRIG SENS (R471) while rotating the A TRIGGER LEVEL control slowly so that the A Trigger is just able to be maintained.

f. Set the Horizontal MODE switch to B.

g. ADJUST—B TRIG SENS (R627) while rotating the B TRIGGER LEVEL control slowly so that the B Trigger is just able to be maintained.

3. Adjust P-P Auto Level (R434 and R435)

a. Set:

CH 1 VOLTS/DIV	50 mV
A TRIGGER SLOPE	Positive (button out)
A TRIGGER LEVEL	Fully clockwise
Horizontal MODE	A

b. Set the leveled sine-wave generator to produce a 50-kHz, 6-division display.

c. Set the CH 1 VOLTS/DIV switch to 0.5 V.

d. ADJUST—(+) P-P AUTO LEVEL (R434) so that the vertical display just solidly triggers on the positive peak of the signal.

e. Set:

A TRIGGER SLOPE	Negative (button in)
A TRIGGER LEVEL	Fully counter-clockwise

f. ADJUST—(-) P-P AUTO LEVEL (R435) so that the display just solidly triggers on the negative peak of the signal.

g. Disconnect the test equipment from the instrument.

4. Adjust Trigger Level Readout (R6155 and R6156)

a. Set:

Vertical MODE	CH 1
Channel 1 VOLTS/DIV	mV
Channel 1 AC–GND–DC	GND
A SEC/DIV	0.5 ms
A TRIGGER Mode	P-P AUTO
A TRIGGER LEVEL	Midrange
A TRIGGER SOURCE	VERT MODE
STORE/NON–STORE	NON–STORE (button out)

b. Center the trace on the screen.

c. ADJUST—TOFFSET (R6156) for a trigger readout of 0.00 mV.

d. Connect the standard-amplitude signal from the calibration generator via a 50-Ω cable to the CH 1 OR X input connector.

e. Set:

Channel 1 AC–GND–DC	DC
A TRIGGER Mode	NORM

f. Set the generator to produce a 5 division standard-amplitude signal.

g. Adjust the A Trigger LEVEL control for a stable display and center the waveform on the screen.

h. Set the channel 1 VOLT/DIV switch to 10 mV for a 10-division display.

i. Vertically position the top of the waveform display on the center horizontal graticule line.

j. Set the A Trigger SLOPE switch to Negative (button in).

k. Rotate the A Trigger LEVEL control clockwise until the triggering of the waveform display becomes unstable.

l. ADJUST —TGAIN (R6155) for a trigger readout of 100 mV.

m. INTERACTION—Repeat parts a through l, adjusting TOFFSET (R6156) and TGAIN (R6155).

n. Disconnect the test equipment from the instrument.

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MAINTENANCE

This section contains information for conducting preventive maintenance, troubleshooting, and corrective maintenance on the instrument. Circuit board removal procedures are included in the corrective maintenance part of this section.

STATIC-SENSITIVE COMPONENTS

The following precautions are applicable when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.
3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by their bodies, never by their leads.
7. Do not slide the components over any surface.

Table 6-1
Relative Susceptibility to Static-Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFET	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a] **Voltage equivalent for levels (voltage discharged from a 100-pf capacitor through resistance of 100 Ω):**

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est)
8 = 900 V
9 = 1200 V

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

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PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When performed regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to accomplish preventive maintenance is just before instrument adjustment.

GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the oscilloscope. The front cover supplied with the instrument provides both dust and damage protection for the front panel and crt. The front cover should be on whenever the instrument is stored or is being transported.

INSPECTION AND CLEANING

The instrument should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under high-humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6–2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Deficiencies found that could cause personal injury or could lead to further damage to the instrument should be repaired immediately.

CAUTION

To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

Table 6–2
External Inspection Checklist

Item	Inspect For	Repair Action
Cabinet, Front Panel, and Cover	Cracks, scratches, deformations, and damaged hardware or gaskets.	Touch up paint scratches and replace defective components.
Front-panel controls	Missing, damaged, or loose knobs, buttons, and controls.	Repair or replace missing or defective items.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts. Clean or wash out dirt.
Carrying Handle	Correct operation.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective parts.

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Table 6-3
Internal Inspection Checklist

Item	Inspect For	Repair Action
Circuit Boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Clean solder corrosion with an eraser and flush with isopropyl alcohol. Resolder defective connections. Determine cause of burned items and repair. Repair defective circuit runs.
Resistors	Burned, cracked, broken, or blistered.	Replace defective resistors. Check for cause of burned component and repair as necessary.
Solder Connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Replace defective capacitors. Clean solder connections and flush with isopropyl alcohol.
Semiconductors	Loosely inserted in sockets. Distorted pins.	Firmly seat loose semiconductors. Remove devices having distorted pins. Carefully straighten pins (as required to fit the socket) using long-nose pliers, and reinsert firmly. Ensure that straightening action does not crack pins, causing them to break.
Wiring and Cables	Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace defective wires or cables.
Chassis	Dents, deformations, and damaged hardware.	Straighten, repair, or replace defective hardware.

CLEANING. Loose dust on the outside surface of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners. A plastic light filter is provided with the oscilloscope. Clean the light filter and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

Interior

To gain access to internal portions of the instrument for inspection and cleaning, refer to the Removal and Replacement Instructions in the Corrective Maintenance part of this section.

INSPECTION. Inspect the internal portions of the instrument for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, conduct a complete Performance Check and, if so indicated, an instrument readjustment (see Sections 4 and 5).

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CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards. If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

1. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see Removal and Replacement Instructions).
2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.
3. Dry all parts with low-pressure air.
4. Dry all components and assemblies in an over or drying compartment using low-temperature (125°F to 150°F) circulating air.

SWITCH CONTACTS. The VOLTS/DIV and SEC/DIV switches are mounted on circuit boards within the instrument. Care must be exercised to preserve the high-frequency characteristics of these switches. Switch maintenance is seldom necessary, but if required, use this procedure.

1. Cam-activated VOLTS/DIV Attenuator switches.

CAUTION

Most spray-type circuit coolants contain Freon 12 as a propellant. Because many Freons adversely affect switch contacts, do not use spray-type coolants on the switches or attenuators.

The only recommended circuit coolants for the VOLT/DIV attenuators are dry ice (CO2) and isopropyl alcohol.

   a. Use only isopropyl alcohol as a cleaning agent for switches, especially in the area of the Vertical Attenuator circuit board. Carbon based solvents will damage the board material.

   b. Apply the alcohol with a small, camel-hair brush. Do not use cotton tipped applicators as the cotton tends to snag and possibly damage the switch contacts.

2. Rotary-activated SEC/DIV switch contacts.

CAUTION

Use only deionized or distilled water at about 55°C (131°F) to clean the SEC/DIV timing switch. Tap water contains impurities that remain as residual deposits after evaporation.

   a. Spray hot water into the slots at the top of each switch housing while rotating the switch control knob. Use an atomizing spray device, and spray for only about five seconds.

   b. Dry the switch and circuit board on which it is mounted with dry low-pressure air.

   c. Bake the switch and circuit board in an oven or drying compartment using dry circulating air at about 75°C (167°F) for 15 minutes.

LUBRICATION

Most of the potentiometers used in this instrument are permanently sealed and generally do not require periodic lubrication. All switches, both rotary- and lever-type, are installed with proper lubrication applied where necessary and will rarely require any additional lubrication. A regular periodic lubrication program for the instrument is therefore, not recommended.

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

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PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment instructions are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument. In some cases, minor problems may be revealed or corrected by readjustment. If only a partial adjustment is performed, see the interaction chart, Table 5-1, for possible adjustment interaction with other circuits.

TROUBLESHOOTING

INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the Theory of Operation and Diagrams sections of this manual may be helpful while troubleshooting.

TROUBLESHOOTING AIDS

Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions of the digital storage portions of the instrument. When instrument power is applied, power-up kernel tests are performed to verify proper operation of the instrument's microprocessor, RAM and ROM. If a failure is detected, this information is passed on to the operator, if possible. The failure information directs the operator to the failing block of memory. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the Diagrams section. Portions of circuitry mounted on each circuit board are enclosed by heavy black lines. The assembly number and name of the circuit are shown near either the top or the bottom edge of the enclosed area.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The Theory of Operation uses these functional block names when describing circuit operation as an aid in cross-referencing between the theory and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the Diagrams section for the reference designators and symbols used to identify components. Important voltages and waveform reference numbers (enclosed in hexagonal-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the Diagrams section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonal outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

Also provided in the Diagrams section is an illustration of the bottom side of the Main circuit board. This illustration aids in troubleshooting by showing the connection pads for the components mounted on the top side of the circuit board. By using this illustration, circuit tracing and probing for voltages and signals that are inaccessible from the top side of the board may be achieved without dismantling portions of the instrument.

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Circuit Board Locations

The placement of each circuit board in the instrument is shown in board locator illustrations. These illustrations are located on foldout pages along with the circuit board illustration.

Circuit Board Interconnections

A circuit board interconnection diagram is provided in the Diagrams section to aid in tracing a signal path or power source between boards. All wire, plug, and jack numbers are shown along with their associated wire or pin numbers.

Power Distribution

Power Distribution diagrams (diagrams 10 and 20) are provided to aid in troubleshooting power supply problems. These diagrams show the service jumper connections used to apply power to the various circuit boards. Excessive loading on a power supply by a circuit board fault may be isolated by disconnecting the appropriate service jumpers.

Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration. Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram in which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the Diagrams section.

RESISTOR COLOR CODE. Resistors used in this instrument are carbon-film, composition, or precision metal-film types. They are usually color coded with the EIA color code; however, some metal-film type resistors may have the value printed on the body. The color code is interpreted starting with the stripe nearest to one end of the resistor. Composition resistors have four stripes; these represent two significant digits, a multiplier, and a tolerance value. Metal-film resistors have five stripes representing three significant digits, a multiplier, and a tolerance value.

CAPACITOR MARKINGS. Capacitance values of common disc capacitors and small electrolytics are marked on the side of the capacitor body. White ceramic capacitors are color coded in picofarads, using a modified EIA code.

Dipped tantalum capacitors are color coded in microfarads. The color dot indicates both the positive lead and the voltage rating. Since these capacitors are easily destroyed by reversed or excessive voltage, be careful to observe the polarity and voltage rating when replacing them.

DIODE COLOR CODE. The cathode end of each glass-encased diode is indicated by either a stripe, a series of stripes or a dot. For most diodes marked with a series of stripes, the color combination of the stripes identifies three digits of the Tektronix Part Number, using the resistor color-code system. The cathode and anode ends of a metal-encased diode may be identified by the diode symbol marked on its body.

Semiconductor Lead Configurations

Figure 9-2 in the Diagrams section shows the lead configurations for semiconductor devices used in the instrument. These lead configurations and case styles are typical of those used at completion of the instrument design. Vendor changes and performance improvement changes may result in changes of case styles or lead configurations. If the device in question does not appear to match the configuration shown in Figure 9-2, examine the associated circuitry or consult the manufacturer's data sheet.

Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).

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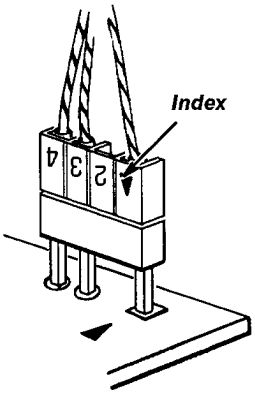


Figure 6-1. Multi-connector holder orientation.

Storage Board Latch

WARNING

Turn off POWER switch before placing the Storage circuit board in Servicing Position.

While servicing the interior of the instrument, the Storage circuit board may be latched in the servicing position. See the Storage Circuit Board in Servicing Position in the Removal and Replacement Instructions part of this section. The two signal leads of the four-wire connectors P2111 and P2112 need to be grounded when disconnected from the Storage circuit board. Grounding the signal leads of P2111 and P2112 permits the VERTICAL POSITION controls to work properly.

The center signal leads may be connected to the outside ground leads of P2111 and P2112 by using four 1-inch long number 22 tinned copper wires (two wires for each connector). Bend the wires in a U-shape and insert the wires between pins 1 and 2 and between pins 3 and 4 of the connectors (see Figure 6-2).

Analog Isolation

To simplify troubleshooting, the analog portion of the instrument may be isolated from the digital portion. Once the analog portion is working properly, the digital portion can be reconnected and troubleshot. Use the following procedure to isolate the analog section from the digital section.

1. Disconnect the following connectors from the Storage circuit board:

   a. P9411, a 24-wire connector, from the front, right edge of the circuit board.

   b. P6100, a 60-wire connector, from the center, right edge of the circuit board.

   c. P9211, a 10-wire connector, from the center of the circuit board.

   d. P4211, a 12-wire connector, from the right, rear corner of the circuit board.

   e. P2111 and P2112, 4-wire connectors, from the left edge of the circuit board. Ground the two signal leads of each connector so the Vertical POSITION controls work properly (see preceding "Storage Board Latch").

2. Disconnect P9410, a nine-wire connector, from the right side of the Sweep Reference circuit board (located at the rear of the Timing circuit board).

   a. Install a jumper wire between J9410, pin 6, and J9410, pin 8, on the Sweep Reference circuit board.

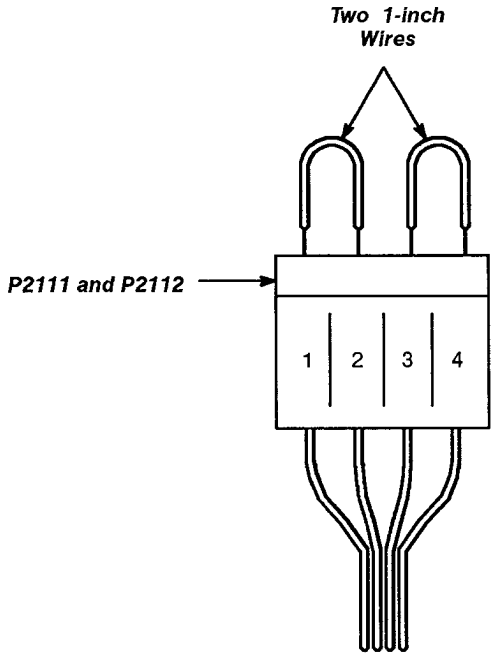


Figure 6-2. Grounding the signal lines of P2111 and P2112.

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3. Disconnect P9010, an 8-wire connector, from the right side of the Main circuit board (in front of the power supply shield).

4. Latch the Storage circuit board in the service position (see "Storage Circuit Board in Servicing Position" in the "Removal and Replacement Instructions" portion of this section).

Kernel Isolation

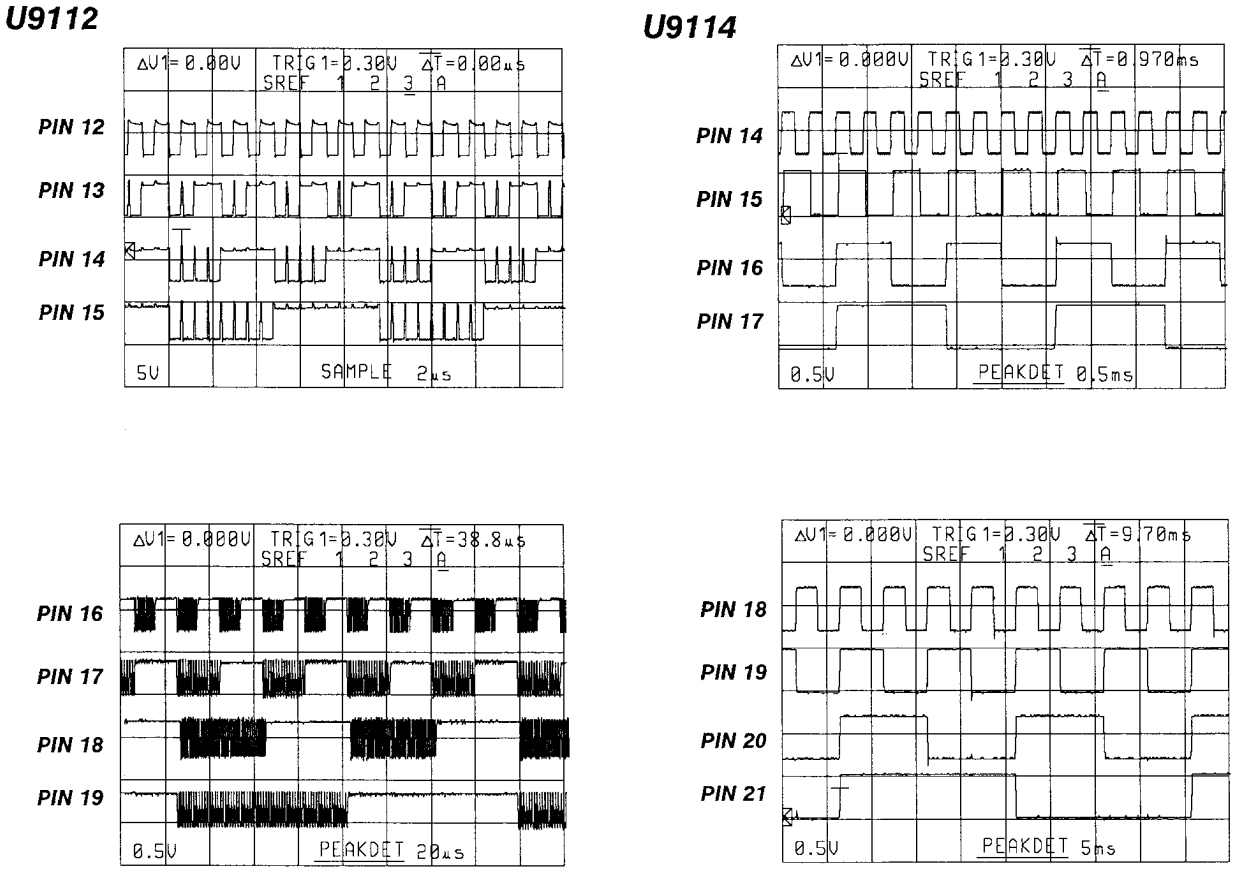
To facilitate troubleshooting, the kernel (microprocessor, clock, and address latch) may be isolated from the rest of the circuitry. When the kernel is functional, the power-up diagnostics may be used to further troubleshoot the digital circuitry. To isolate the kernel:

1. Turn off the POWER switch.

2. Move the black shunt assembly (jumper) located at the front edge of the Storage board from J9105B (NORM) to J9105A (DIAG).

3. Turn on the POWER switch.

Figure 6-3 shows the isolated kernel timing waveforms. After the kernel is repaired, restore normal operation by performing the reverse of the previous procedure.



TRIGGER TEST SCOPE ON U9114, PIN 21 (NORM TRIGGER MODE.)

Figure 6-3. Isolated Kernel timing.

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Switch Interface Voltages

Voltages generated by the interface to front-panel switches may be used to troubleshoot the instrument. Timing switch interface voltages are shown in Tables 6-4A and 6-4B, VERTICAL VOLTS/DIV switch interface voltages are shown in Table 6-5, and Input Coupling (AC-GND-DC) switch interface voltages are shown in Table 6-6.

The tables also list hexadecimal ranges for the FP IO Exerciser Diagnostics (see Diagnostics in this section). When a front-panel problem is suspected, run the FP IO Exerciser. If an incorrect hexadecimal value is found (see tables), measure the corresponding switch voltage to determine whether or not a problem exists.

FP IO Exerciser hexadecimal values for the Probe Coding are shown in Table 6-7.

Table 6-4A
Timing Switch Interface Voltages

A SEC per DIV	ARES1 J6421 pin 2 Voltage Range	ARES1 Hexadecimal Range from FP IO Diagnostics	AC1 W6123 pin 2	AC2 W6123 pin 3	ARES2 J6421 pin 1 Voltage Range	ARES2 Hexadecimal Range from FP IO Diagnostics
EXT CLK	4.591 to 5.100	3AB to 3FF	5 V	5 V	3.742 to 4.590	2FD to 3AA
0.5 s	4.591 to 5.100	3AB to 3FF	0 V	5 V	4.591 to 5.100	3AB to 3FF
0.2 s	4.591 to 5.100	3AB to 3FF	0 V	5 V	3.742 to 4.590	2FD to 3AA
0.1 s	4.591 to 5.100	3AB to 3FF	0 V	5 V	2.716 to 3.742	22B to 2FC
50 ms	-0.250 to 1.150	000 to EA	0 V	5 V	4.591 to 5.100	3AB to 3FF
20 ms	4.591 to 5.100	3AB to 3FF	0 V	5 V	1.109 to 2.715	E2 to 22A
10 ms	4.591 to 5.100	3AB to 3FF	0 V	5 V	-0.350 to 1.108	000 to E1
5 ms	1.151 to 2.715	EB to 22A	0 V	5 V	4.591 to 5.100	3AB to 3FF
2 ms	3.743 to 4.590	2FE to 3AA	0 V	5 V	4.591 to 5.100	3AB to 3FF
1 ms	2.716 to 3.742	22B to 2FC	0 V	5 V	4.591 to 5.100	3AB to 3FF
0.5 ms	-0.250 to 1.150	000 to EA	5 V	0 V	4.591 to 5.100	3AB to 3FF
0.2 ms	4.591 to 5.100	3AB to 3FF	5 V	0 V	1.109 to 2.715	E2 to 22A
0.1 ms	4.591 to 5.100	3AB to 3FF	5 V	0 V	-0.350 to 1.108	000 to E1
50 µs	1.151 to 2.715	EB to 22A	5 V	0 V	4.591 to 5.100	3AB to 3FF
20 µs	3.743 to 4.590	2FE to 3AA	5 V	0 V	4.591 to 5.100	3AB to 3FF
10 µs	2.716 to 3.742	22B to 2FC	5 V	0 V	4.591 to 5.100	3AB to 3FF
5 µs	-0.250 to 1.150	000 to EA	0 V	0 V	4.591 to 5.100	3AB to 3FF
2 µs	4.591 to 5.100	3AB to 3FF	0 V	0 V	1.109 to 2.715	E2 to 22A
1 µs	4.591 to 5.100	3AB to 3FF	0 V	0 V	-0.350 to 1.108	000 to E1
0.5 µs	1.151 to 2.715	EB to 22A	0 V	0 V	4.591 to 5.100	3AB to 3FF
0.2 µs	3.743 to 4.590	2FE to 3AA	0 V	0 V	4.591 to 5.100	3AB to 3FF
0.1 µs	2.716 to 3.742	22B to 2FC	0 V	0 V	4.591 to 5.100	3AB to 3FF
0.05 µs	4.591 to 5.100	3AB to 3FF	0 V	0 V	4.591 to 5.100	3AB to 3FF

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Table 6-4B
Timing Switch Interface Voltages

B SEC per DIV	B_RES J6421 pin 5 Voltage Range	B_RES Hexadecimal Range from FP IO Diagnostics	B_CAPS J6421 pin 4	B_CAPS Hexadecimal Range from FP IO Diagnostics
EXT CLK	2.510 to 3.546	201 to 3FE	3.2 to 5.0	288 to 3EC
0.5 s	2.510 to 3.546	201 to 3FE	3.2 to 5.0	288 to 3EC
0.2 s	2.510 to 3.546	201 to 3FE	3.2 to 5.0	288 to 3EC
0.1 s	2.510 to 3.546	201 to 3FE	3.2 to 5.0	288 to 3EC
50 ms	2.510 to 3.546	201 to 3FE	3.2 to 5.0	288 to 3EC
20 ms	1.548 to 2.509	130 to 200	3.2 to 5.0	288 to 3EC
10 ms	-0.200 to 0.612	000 to 7C	3.2 to 5.0	288 to 3EC
5 ms	0.613 to 1.547	7D to 13B	3.2 to 5.0	288 to 3EC
2 ms	4.227 to 4.752	360 to 3CB	3.2 to 5.0	288 to 3EC
1 ms	3.547 to 4.226	2D5 to 359	3.2 to 5.0	288 to 3EC
0.5 ms	2.510 to 3.546	201 to 3FE	1.3 to 3.2	107 to 288
0.2 ms	1.548 to 2.509	13C to 200	1.3 to 3.2	107 to 288
0.1 ms	-0.200 to 0.612	000 to 7C	1.3 to 3.2	107 to 288
50 µs	0.613 to 1.547	7D to 13B	1.3 to 3.2	107 to 288
20 µs	4.227 to 4.752	360 to 3CB	1.3 to 3.2	107 to 288
10 µs	3.547 to 4.226	2D5 to 359	1.3 to 3.2	107 to 288
5 µs	2.510 to 3.546	201 to 3FE	-1.0 to 1.3	000 to 107
2 µs	1.548 to 2.509	13C to 200	-1.0 to 1.3	000 to 107
1 µs	-0.200 to 0.612	000 to 7C	-1.0 to 1.3	000 to 107
0.5 µs	0.613 to 1.547	7D to 13B	-1.0 to 1.3	000 to 107
0.2 µs	4.227 to 4.752	360 to 3CB	-1.0 to 1.3	000 to 107
0.1 µs	3.547 to 5.226	2D5 to 359	-1.0 to 1.3	000 to 107
0.05 µs	4.753 to 5.100	3CC to 3FF	-1.0 to 1.3	000 to 107

TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

TROUBLESHOOTING TECHNIQUES

The following procedure is arranged in an order that enables checking simple trouble possibilities before requiring more extensive troubleshooting. The first two steps use diagnostic aids inherent in the instrument's operating firmware and will locate many circuit faults. The next four steps ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under Corrective Maintenance in this section.

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Table 6–5
Vertical VOLTS/DIV Switch Interface Voltages

SWITCH SETTING	CH1_ATN and CH2_ATN (J6111 pin 2 and J6112 pin 2)	CH1_ATN and CH2_ATN Hexadecimal Range from FP IO Diagnostics
2 mV per division	2.104 to 2.340	1AE to 1DE
5 mV per division	4.167 to 4.712	354 to 3C4
10 mV per division	3.199 to 4.440	28E to 2BF
20 mV per division	2.502 to 2.702	1FF to 228
50 mV per division	0 to 2.104	000 to 1AE
0.1 V per division	2.938 to 3.199	259 to 28E
0.2 V per division	2.340 to 2.502	1DE to 1FF
0.5 V per division	4.712 to 5.000	3C4 to 3FF
1 V per division	3.731 to 4.167	2FB to 354
2 V per division	3.440 to 3.731	2BF to 2FB
5 V per division	2.702 to 2.938	228 to 259

CAUTION

Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

1. Power-up Tests

The instrument performs automatic verification of the instrument's Microprocessor, ROM, and RAM (the operating kernel) when power is first applied. If all Kernel tests pass, a second level of diagnostic tests are performed. The Diagnostic tests, when passed, give the user a high degree of assurance that the instrument's storage circuitry is functioning properly.

If a diagnostic test fails, the faulty circuitry is identified by a message on the crt (if the instrument is able to produce a display), and, for Kernel tests, by an LED display. If a failure occurs, refer to the Diagnostics discussion later in this section for definitions of error messages.

2. Diagnostic Test Routines

Many of the diagnostic routines may be selected from the front panel to further clarify the nature of a suspected failure. The desired test is selected using the MENU. The Diagnostics are explained in the Diagnostics discussion later in this section.

Table 6–6
AC GND DC Switch Interface Voltages

Variable VOLTS/DIV	SWITCH POSITION	CH1_STAT and CH2_STAT (J6111 pin 3 and J6112 pin 3	CH1_STAT and CH2_STAT Hexadecimal Range from FP IO Diagnostics
OUT OF DETENT	AC	0 to 2.423	000 to 1EE
	GND	2.696 to 0.070	227 to 273
	DC	3.623 to 4.457	2E4 to 391
IN DETENT	AC	2.423 to 2.696	1EE to 227
	GND	3.070 to 3.623	273 to 2E4
	DC	4.457 to 5.000+	391 to 3FF

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Table 6–7
Probe Coding

Probe Attenuation	Probe Hexadecimal Range from FP IO Diagnostics
1X	3Ff to 370
10X	221 to 20D
100X	19B to 18F
1000X	B2 to A1
IDENTIFY	89 to 7C

3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the Operating Information in Section 2 of this manual or to the Operators Manual.

4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the instrument is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

5. Visual Check

WARNING

To avoid electrical shock, disconnect the instrument from the ac power source before making a visual inspection of the internal circuitry.

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

6. Check Instrument Performance and Adjustment

Check the performance of either those circuits where trouble appears to exist or the entire instrument. The apparent trouble may be the result of misadjustment. Complete performance check and adjustment instructions are given in Sections 4 and 5 of this manual.

7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the Diagnostics discussion in this section as an aid in locating a faulty circuit.

8. Check Power Supplies

WARNING

For safety reasons, an isolation transformer must be connected whenever troubleshooting is done in the Preregulator and Inverter Power Supply sections of the instrument.

When trouble symptoms appear in more than one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply. These voltages are measured between the power supply test points and ground (see the associated circuit board illustration and Table 6–8).

Voltage levels may be measured either with a DMM or with an oscilloscope. Voltage ripple amplitudes must be measured using an oscilloscope. Before checking power-supply circuitry, set the INTENSITY control to normal brightness, the A AND B SEC/DIV switch to 0.1 ms, the HORIZONTAL MODE to B, the ON/OFF READOUT toggle to display the readout, the A TRIGGER Mode to P-P AUTO, and set the VERTICAL MODE switch to CH 1.

When measuring ripple (see Table 6–8), use a 1X probe with the ground lead connected to the chassis. To minimize stray pickup, keep the ground lead as short as possible. The ripple values listed are based on a system limited in bandwidth to 30 kHz. Using a system with wider bandwidth will result in higher readings.

If the power-supply voltages and ripple are within the ranges listed in Table 6–8, the supply can be assumed to be working correctly. If they are outside the range, the supply may be either misadjusted or operating incorrectly. Use the Power Supply and CRT Display subsection in the Adjustment procedure to adjust the −8.6 V supply.

A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits.

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9. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

10. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonal-outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

NOTE

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, see the Voltage and Waveform Setup Conditions preceding the waveform illustrations in the Diagrams section.

Table 6-8
Power Supply Voltage and Ripple Limits

Power Supply	Test Point	Reading (Volts)	P-P Ripple (mV)
-8.6 V	W961	-8.56 to -8.64	<1.5
-5.0 V	W9020	-4.75 to -5.25	<20
+5.0 V	W9068	+5.75 to +5.25	<20
+8.6 V	W960	+8.43 to +8.77	<8
+30 V	W956	+29.1 to +30.9	<30
+100 V	W954	+97.0 to +103.0	<100

Note the recommended test equipment, front-panel control settings, voltage and waveform conditions, and cable-connection instructions. Any special control settings required to obtain a given waveform are noted under the waveform illustration. Changes to the control settings from the initial setup, other than those noted, are not required.

11. Check Individual Components

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.

The following procedures describe methods of checking individual components. Two-lead components that are soldered in place are most accurately checked by first disconnecting one end from the circuit board. This isolates the measurement from the effects of the surrounding circuitry. See Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

CAUTION

When checking semiconductors, observe the static-sensitivity precautions located at the beginning of this section.

TRANSISTORS. A good check of a transistor is actual performance under operating conditions. A transistor can most effectively be checked by substituting a known-good component. However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic-type transistor checker for testing. Static-type transistor checkers are not recommended, since they do not check operation under simulated operating conditions.

When troubleshooting transistors in the circuit with a voltmeter, measure both the emitter-to-base and emitter-to-collector voltages to determine whether they are consistent with normal circuit voltages. Voltages across a transistor may vary with the type of device and its circuit function.

Some of these voltages are predictable. The emitter-to-base voltage for a conducting silicon transistor will normally range from 0.6 V to 0.8 V. The emitter-to-collector voltage for a saturated transistor is about 0.2 V. Because these values are small, the best way to check them is by connecting a sensitive voltmeter across the junction rather that comparing two voltages taken with respect to ground. If the former method is used, both leads of the voltmeter must be isolated from ground.

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If voltage values measured are less that those just given, either the device is shorted or no current is flowing in the external circuit. If values exceed the emitter-to-base values given, either the junction is reverse biased or the device is defective. Voltages exceeding those given for typical emitter-to-collector values could indicate either a nonsaturated device operating normally or a defective (open-circuited) transistor. If the device is conducting, voltage will be developed across the resistors in series with it; if open, no voltage will be developed across the resistors unless current is being supplied by a parallel path.

CAUTION

When checking emitter-to-base junctions, do not use an ohmmeter range that has a high internal current. High current may damage the transistor. Reverse biasing the emitter-to-base junction with a high current may degrade the current-transfer ratio (Beta) of the transistor.

A transistor emitter-to-base junction also can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The junction resistance should be very high in one direction and much lower when the meter leads are reversed.

When troubleshooting a field-effect transistor (FET), the voltage across its elements can be checked in the same manner as previously described for other transistors. However, remember that in the normal depletion mode of operation, the gate-to-source junction is reverse biased; in the enhanced mode, the junction is forward biased.

INTEGRATED CIRCUITS. An integrated circuit (IC) can be checked with a voltmeter, test oscilloscope, or by direct substitution. A good understanding of circuit operation is essential when troubleshooting a circuit having IC components. Use care when checking voltages and waveforms around the IC so that adjacent leads are not shorted together. An IC test clip provides a convenient means of clipping a test probe to an IC.

CAUTION

When checking a diode, do not use an ohmmeter scale that has a high internal current. High current may damage a diode. Checks on diodes can be performed in much the same manner as those on transistor emitter-to-base junctions. Do not check tunnel diodes or back diodes with an ohmmeter; use a dynamic tester, such as the TEKTRONIX 576 Curve Tracer.

DIODES. A diode can be checked for either an open or a shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The diode resistance should be very high in one direction and much lower when the meter leads are reversed.

Silicon diodes should have 0.6 V to 0.8 V across their junctions when conducting; Schottky diodes about 0.2 V to 0.4 V. Higher readings indicate that they are either reverse biased or defective, depending on polarity.

RESISTORS. Check resistors with an ohmmeter. Refer to the Replaceable Electrical Parts list for the tolerances of resistors used in this instrument. A resistor normally does not require replacement unless its measured value varies widely from its specified value and tolerance.

INDUCTORS. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by checking the waveform response when high-frequency signals are passed through the circuit.

CAPACITORS. A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter set to one of the highest ranges. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after the capacitor is charged to the output voltage of the ohmmeter. An open capacitor can be detected with a capacitance meter or by checking whether the capacitor passes ac signals.

12. Repair and Adjust the Circuit

If any defective parts are located, follow the replacement procedures given under Corrective Maintenance in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. Since the power supplies affect all circuits, performance of the entire instrument should be checked if work has been done on the power supplies or if the power transformer has been replaced. Readjustment of the affected circuitry may be necessary. Refer to the Performance Check and Adjustment Procedure, Sections 4 and 5 of this manual and to Table 5-1 (Adjustment affected by repairs).

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DIAGNOSTICS

Introduction

A list of the instrument diagnostic tests and messages is shown in Table 6–9. The diagnostics are run automatically during power-up or manually via the menu. The location in the menu of each test is shown in Figure 6–4. Only the digital storage portion of the instrument is checked. Circuitry checked, and/or used by each test is shown in Table 6–10. During a normal power-up, only the first error of each test is displayed. If the instrument contains the RS–232–C Option, an ASCII version of all errors found during power-up is sent to the option. In addition to displaying the errors on the crt, the errors are also displayed on U9101, a seven-segment LED lamp on the Storage circuit board.

Table 6–9
Diagnostic Tests and Messages

Power-up	Menu	Message
X		PU : ROM/RAM: <hex value>
	X	Rom0 : PASSED Rom0 : <actual_check_sum> <> <expected_check_sum> Rom1 : PASSED Rom1 : <actual_check_sum> <> <expected_check_sum>
X		NV SETUP : Using factory default
X		SAVE REF : Storage failed: <list>
X		CMOS : reformatted CMOS : recovered
	X	FP A/D : ILLEGAL VALUE FP A/D : MISSING FP INTERRUPT FP A/D : PASSED
	X	Com RB : rb(1) = <value> & rb(0) = <value>
	X	Com LB: PASSED Com LB : CAN'T TEST RS232 Com LB : FGET NOT SET Com LB : FGET NOT CLEAR
	X	ACQ IC (Items indicated by * effective SN B012825 and above)
		ACQ IC TEST PASSED*
		ACQ IC TEST FAILED*
		011Cannot talk to ADG209
		012 Bad ADG209, further tests aborted
		TRIGGER TEST PASSED*
		034 No minimum or maximum clock trigger
		032 No A_GATE
		033 No B_GATE
		035 No A_GATE or B_GATE
		CLOCK INTERPOLATOR TEST PASSED*
		Minimum count after 1 MCLK = <hex value>
	X	Maximum count after 2 MCLKS = <hex value>
		Difference between counts = <hex value>
		CLOCK INTERPOLATOR TEST FAILED*

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Table 6-9 (Cont.)
Diagnostic Tests and Messages

Power-up	Menu	Message
	X	Minimum count after 1 MCLK = <hex value>
		Maximum count after 2 MCLKS = <hex value>
		Difference between counts = <hex value>
		ACQUISITION RAM TEST PASSED*
		ACQUISITION RAM TEST FAILED*
		<diag> bad ram part <component>
	X	A to D <message>
		<n> missing codes

ADVANCED FUNCTIONS
- Diag Menu
  - Tests
    - Mem
      - Rom 0
      - Rom 1
      - NV Ram
    - System
      - Fp A/D
      - Com RB
      - Com LB
    - Acq
      - ACQ IC *
        - more
          - Trigger
          - Clock Interpolator
          - Acquisition Ram
      - A To D
        - CH1
        - CH2
  - Cal
    - Box
    - Vert
  - Exer
    - Config
    - IO
      - FP IO
      - Iports
      - Oports

*Effective SN B012825 and above

Figure 6-4. Diagnostic Menu Map.

The following sequence of events occurs during power-up:

Set up temporary interrupt vectors (single task).

Do the power-up (PU) Kernel tests (each sets a bit in a buffer).

ROM tests (Send error codes to U9101 LED lamp on the Storage board once for each detected error).

RAM tests (Send error codes to U9101 once for each detected error).

Initialize system.

If a SETUP button is pressed:

Enable RS-232-C error reporting.

Do power-up calibration/diagnostic routines:

Rotate ones in control ports (Oports).

Display the Box without maskable interrupt support (Box).

Run Vert (Acquisition Position Offset adjustment aid).

Start building the power-up fault display.

Generate text about PU test results found in PU buffer.

Do System Diagnostic tests:

(when a failure is found, one line of text is generated for later display).

If there were power-up faults:

Display the power-up faults on the crt without maskable interrupt support.

Until a SETUP button is pressed.

Start normal instrument operation.

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Tests

PU TEST. At power-up, this kernel test does a quick check of the instrument's RAM (random access memory) and ROM (read only memory). If no errors are found, additional diagnostic tests are run.

When an error is detected during the PU test, diagnostics information is displayed (at power-up before NMI or MI go HI and before other tests are run) by two methods. If possible, a message "PU:ROM/RAM/NMI: <hexadecimal value>" is displayed by the crt readout. In case the crt display is disabled by the failure, an error code (or sequence of error codes) is also displayed by an LED lamp (U9101) mounted on the Storage circuit board.

The number displayed on the LED can be directly related to a component using Table 6-10. The hexadecimal number displayed by the crt readout must be converted to a binary number to determine which bits are high. These may then be directly related to components using Table 6-10. The same information is provided by either display method.

For example:

LED Readout Display (U9101):

On power-up the LED readout on the Storage board displays this sequence of numbers: 1, 3, 5.

Referring to Table 6-10, it is noted that these numbers relate to U9121, U9231, and U9131. These components and their circuitry should be checked for problems.

CRT Readout Display:

The crt readout displays the message "PU:ROM/RAM/NMI: 15". Converting this hexadecimal number to binary results in the following:

0 0 0 1 0 1 0 1

Bits 0, 2, and 4 are high. Consulting the Corresponding Binary Bit column in Table 6-10, it is noted that U9121, U9231, and U9131 failed the test. These components and their circuitry should be checked for problems.

NOTE

More than one bad RAM usually means that something else is causing the problem.

The following three tests are executed at power-up after the PU test.

NV SETUP. This test checks the data in the stored front panel settings. A message "Using factory default" indicates that the data in the front panel settings was corrupted and the factory default settings are being used. The most likely cause for this failure is a bad battery (BT1101) or a loss of power to the non-volatile RAM since the last use of the instrument.

SAVE REF. The SAVE REF memories (1, 2, 3, and 4K) are checked. Failed memories are listed on the screen (1/4K, 2, 3). Failure causes are the same as for NV SETUP.

CMOS. This test checks the 26K of non-volatile memory. If an error is found, one of two messages is displayed: "recovered" indicates that errors were found but were few and not drastic; "reformatted" indicates that a drastic error was found—all non-volatile waveform data was lost.

ROM 0 and ROM 1. The ROM test checks each ROM by calculating and then comparing its checksum to what is stored in the ROM.

If an error is found, the calculated value and the value expected are displayed on the crt:

Rom0: actual_check_sum < > expected_check_sum
Rom1: actual_check_sum < > expected_check_sum

For example, if the calculated value is A4D2 and the value stored in the ROM is 23DA the following error message is displayed on the crt:

Rom1: A4D2 < > 23DA

NV Ram. The non-volatile RAM test is not implemented.

Com RB. Bit paths within the communications option are checked. GPIB circuitry checked includes U1335B and U1323. RS-232-C circuitry checked includes U1236 and U1223. Refer to OPTION MAINTENANCE INFORMATION in the OPTIONS section for further information.

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Table 6-10
Error Codes for PU Test

U9109 (LED Lamp Readout)	Corresponding Binary Bit	Test	RAM Address	Component
1	0	Rom 0	---	U9121
2	1	Rom 1	---	U9120
3	2	Ram	0-7FFF	U9231
4	3	Ram	8000-FFFF	U9232
5	4	Ram	67800-67FFF	U9131
6	5	Ram	68000-697FF	U9130
7	6	Ram	60000-6FFFF	U9130
8	7	Not Used	----	----

Com LB. This test checks the GPIB controller U1321 and associated circuitry by commanding the controller to change its TR output and then checking the TR output for this change. If an error is found, it is displayed on the crt. Refer to OPTION MAINTENANCE INFORMATION in the OPTIONS section for further information.

ACQ IC*. This diagnostic sequence tests the digital acquisition and memory, and the digital timebase. After the sequence has completed, further detailed information about the test results can be displayed by pressing the bezel button labeled "more."

ACQ IC TEST*. This tests the microprocessor interface to the digital acquisition IC U4000, then tests the data path to the acquisition memory. If a failure is detected in the microprocessor interface, further tests are aborted and results reported.

During the microprocessor interface test, the control registers in U4000 are checked against the power-up values. The hexadecimal value A5A5 is written to a set of control registers. The registers are then read back and compared to the value written. The test is repeated with the hexadecimal value 5A5A.

During the data path test, a diagnostic counter in U4000 applies a pseudorandom data sequence to both acquisition input channels. A sequence of 4096 values are read from the data registers in U4000 and compared with predicted values.

TRIGGER TEST*. Before performing this test, set the 2232 controls as follows:

AND B SEC/DIV	< 20 ms
Trigger MODE	BOTH
A TRIG	P-P AUTO
B TRIG LEVEL	RUNS AFTER DLY

Several tests are performed during the trigger test to check the Trigger Mux circuit. The diagnostic routine is terminated after the first failure and the results are reported. Using the timebase clock as the trigger source, an acquisition is started by the microprocessor and the acquisition status register of U4000 is monitored. If the acquisition does not terminate after a predetermined time-out period, a failure is reported. If this test passes, another acquisition is started using the ATRIG as the trigger source. Again the acquisition status register is monitored, checking to see if the acquisition terminates after the time-out period. If not, an A_GATE failure is reported. This test is repeated again using BTRIG as the trigger source.

CLOCK INTERPOLATOR TEST*. This tests the operation of the Clock Delay Timer circuit and the Timebase Interpolator Counter in U4000 using the timebase clock as the trigger source. The delay between the trigger and the clock delay timer fast ramp stop is programmed for one or two timebase clock periods. The interpolator counter is read for each case and the difference is calculated. The count difference must be between the hexadecimal values of 172 and 1AE.

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ACQUISITION RAM TEST*. This tests the operation of the acquisition RAM chips using the diagnostic counter in U4000 as a data source for both input channels. An acquisition is started and the acquisition RAMs are filled with a pseudorandom data sequence. Data is clocked through the chip at 100 MHz, testing the part at full speed. The contents of each RAM chip are read and compared to predicted values. A failure in any RAM is listed by circuit number.

FP A/D. This test checks the front panel A/D converter circuitry. A conversion is done on three of the analog inputs (A CURS, U6106 pin 12, B CURS, U6106 pin 13, and ground, U6108 pin 5). The algebraic sum of A CURS and B CURS are checked. Their sum should be between 0x100 and 0x700. Ground is also checked. It should be between 0 and 5 front panel A/D converter counts (5 1024 of VREF).

During power-up this test defines a variable (FP POLLED) that controls how the microprocessor works with the front panel. If during testing a MI is not generated, it is assumed that the front panel will never generate a MI and the microprocessor must poll the front panel to see when to transfer front-panel data.

If an error is found one of the following messages is displayed on the crt:

FP A/D : cursor :a= <actual> & b= <actual>

FP A/D : gnd = <actual> <> 5

FP A/D : TIME-OUT

Where:

Actual is a 3-digit hexadecimal number representing the result of a front-panel digitization.

TIME-OUT indicates A/D INT FLAG (U6101D pin 13) did not occur within 0x800 polls by the micro processor.

CAL. The instrument calibration aids are used to help calibrate the instrument.

Box. This calibration aid displays a box (rectangle) on the crt. Gains and offsets of the storage display system integrators are set using the Box display (see the Adjustment Procedure). The Display Controller (U9208) is synchronously stimulated (at a multiple of NMI) to display the box not using MIs.

Vert. This calibration aid is used to calibrate the Acquisition Position Offset adjustments (see the VERTICAL Adjustment Procedure).

CAL PU. Pressing one of the SETUP buttons during power-up runs three calibration routines: Box, Oports, and Vert. Each routine is run until one of the menu buttons is pushed again. The Box and Oports routines are run at the same time. Oports is used to check instrument circuitry (see Oports).

Exercisers. Instrument exercisers are used to aid in the repair of the instrument.

Config. This exerciser lists the ROM circuit numbers and part numbers used in the instrument. It also lists any communications option installed in the instrument.

FP IO. Raw internal front-panel data is displayed on the crt by this exerciser. Table 6-11 shows which data is displayed in the different positions (display format) and the controls that affect the data.

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Table 6-11
Display Format for Front Panel IO Exerciser

Data	Signal Names (Controls)			
Curs =	CUR1 (CURSORS)	CUR2 (CURSORS)	B_DELAY (B DELAY TIME POSITION)	
Ch1 =	E114, E115 (POSITION)	CH1_ATN (VOLTS/DIV)	CH1_STAT (CAL, Input Coupling)	CH1_PRB (Probe Coding)
Ch2 =	E164, E165 (POSITION)	CH2_ATN (VOLTS/DIV)	CH2_STAT (CAL, Input Coupling)	CH2_PRB (Probe Coding)
Asw =	ARES1 (A SEC/DIV)	ARES2 (A SEC/DIV)		
Bsw =	B_RES (B SEC/DIV)	B_CAPS (B SEC/DIV)		
Trig =	ATR_LVL (A TRIGGER LEVEL)			

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NOTE

Digital data is intensified when a control is changed. All other data is intensified if the data has changed more than 5 counts since the last display update.

Front Panel hexadecimal information displayed by the exerciser should be used as an aid in detecting front panel problems. If a hexadecimal number is outside the range listed, the associated voltage level should be checked to determine if a problem exists.

Front Panel diagnostic hexadecimal ranges and associated actual voltage ranges are found in the following tables:

Table 6-4A	ARES1, ARES2
Table 6-4B	B_RES, B_CAPS
Table 6-5	CH1_ATN, CH2_ATN
Table 6-6	CH1_STAT, CH2_STAT

The hexadecimal codes for the CH 1 POSITION (E114, E115), CH 2 POSITION (E164, E165), and A TRIGGER LEVEL (ATR_LVL) controls should vary as the controls are rotated. If no change is noted, then there is a problem in the front panel circuitry.

Hexadecimal ranges for probe coding (CH1_PRB, CH2_PRB) are listed in Table 6-7.

Oports. All microprocessor output ports of the instrument are exercised by this exerciser. If entered from power-up, the exerciser is run with the box display. Test patterns used in each port are shown in Table 6-12.

NOTE

The ones and zeros patterns are observed using an LED dip clip on the registers.

Iports. This exerciser displays the input data for all microprocessor input ports.

A to D. This exerciser tests the acquisition A/D converters for missing bits. This test requires a function generator with at least 99% triangle wave linearity (Tektronix FG503 or equivalent). Use the following procedure to test the A/D converters with the exerciser:

1. Exit all Menus.

2. Connect the output of the Function Generator to the CH 1 OR X input connector via a 50-Ω cable, 10X attenuator, and 50-Ω terminator.

Table 6-12
Output Ports Exerciser

U4119 Pins

19	18	17	16	15	14	13	12
1	0	0	0	0	0	0	1
0	1	0	0	0	0	1	0
0	0	1	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	1	0	0	0	0	1	0
1	0	0	0	0	0	0	1

U4120 Pins

19	18	17	16	15	14	13	12
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	0	0	1	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1

U6104 Pins

19	18	17	16	15	14	13	12
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0
1	1	1	1	1	1	0	0
1	1	1	1	1	0	0	0
1	1	1	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0

3. Set Function Generator controls to produce a 25 KHz triangle wave.

4. Set the 2232 controls as follows:

STORE/NON-STORE	STORE (button in)
VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	20 mV
CH 1 COUPLING	DC
A AND B SEC/DIV	10 μs

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5. Adjust the Function Generator VAR ATTENUATOR to display a 6-division peak-to-peak signal. Adjust CH 1 VERTICAL POSITION to center the waveform.

6. Change the CH 1 VOLTS/DIV setting to 10 mV.

7. Press the ADV FUNCT SETUP button. Select Diag Menu.

8. In the DIAGNOSTICS Menu, use the bezel buttons to select in the following order: Tests, Acq, A to D, and CH1.

9. Select RUN. The readout indicates the number of missing codes. If the number is greater than 0, there is a fault in the CH 1 digitizer module.

10. Repeat steps 2 through 9 for Channel 2.

11. To rerun test, select Reset. To return to normal operation, select EXIT, then press the ADV FUNCT SETUP button.

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CORRECTIVE MAINTENANCE

INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the Repackaging information in Section 2 of this manual.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions.

1. Disconnect the instrument from the ac-power source before removing or installing components.
2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.
3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).
4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the Replaceable Electrical Parts list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, some special parts are used in the instrument. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufacturers can be identified by referring to the Cross Index-Manufacturer's Code number to Manufacturer at the beginning of the Replaceable Electrical Parts list. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

1. Instrument type (include all modification and option numbers).
2. Instrument serial number.
3. A description of the part (if electrical, include its full circuit component number).
4. Tektronix part number.

MAINTENANCE AIDS

The maintenance aids listed in Table 6-13 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for those given, provided their characteristics are similar.

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Table 6-13
Maintenance Aids

Description	Specification	Usage	Example
1. Soldering Iron	15 to 25 W.	General Soldering and unsoldering.	Antex Precision Model C.
2. Torx Screwdriver Tips and Handle	Torx tips: #T7, #T9, #T10, #T15, and #T20. Handle: 1/4 inch hex drive.	Assembly and disassembly.	Tektronix Part Numbers: Torx Tips #T7 003-1293-00 #T9 003-0965-00 #T10 003-0814-00 #T15 003-0966-00 #T20 003-0866-00 Handles: 8 1/2 in. 003-0293-00 3 1/2 in. 003-0445-00.
3. Nutdrivers	1/4 inch, 5/16 inch, 1/2 inch, and 9/16 inch.	Assembly and disassembly.	Xcelite #8, #10, #16, and #18.
4. Open-end Wrench	9/16 inch and 1/2 inch.	Channel Input and Ext Trig BNC Connectors.	Tektronix Part Numbers: 9/16 003-0502-00 1/2 003-0882-00.
5. Hex Wrenches	0.050 inch, 1/16 inch.	Assembly and disassembly.	Allen Wrenches.
6. Long-nose Pliers		Component removal and replacement.	Diamalloy Model LN55-3.
7. Diagonal Cutters		Component removal and replacement.	Diamalloy Model M554-3.
8. Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.
9. Contact Cleaner	No-Noise R.	Switch and pot cleaning.	Tektronix Part Number 006-0442-02.
10. Pin-Replacement Kit		Replace circuit board connector pins.	Tektronix Part Number 040-0542-01.
11. IC-Removal Tool		Removing DIP IC packages.	Augat T114-1.
12. Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front panel assemblies.	2-Isopropanol.
13. Isolation Transformer		Isolate the instrument from the ac power source for safety.	Tektronix Part Number 006-5953-00.
14. 1X Probe		Power supply ripple check.	TEKTRONIX P6101A.
15. Bayonet Ground Assembly		Signal interconnect for power supply ripple checks.	Tektronix Part Number 013-0085-00.
16. LED Dip Clip		Troubleshooting.	HP 548A.

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INTERCONNECTIONS

Interconnections in this instrument are made with pins soldered onto the circuit boards. Several types of mating connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various types of connectors.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled (see Figure 6-1).

LITHIUM BATTERY (BT1101)

The lithium battery that supplies backup power to the non-volatile memory should last for three years or more. When the battery must be replaced, observe the following warning.

WARNING

To avoid personal injury, follow proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. Do not recharge, crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of the battery in compliance with local, state, and national regulations.

Typically, small quantities (less than 20) can be safely discarded with ordinary garbage in a landfill. Send larger quantities by surface transport to a hazardous waste disposal facility. Individually package batteries in a sturdy container that is clearly labeled "Lithium Batteries—DO NOT OPEN."

TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the Diagrams section for lead-configuration illustrations.

The chassis-mounted power supply transistor is insulated from the chassis by a heat-transferring mounting block. Reinstall the mounting block and bushings when replacing these transistors. Use a thin layer of heat-transferring compound between the insulating block and chassis when reinstalling the block.

NOTE

After replacing a power transistor, check that the collector is not shorted to the chassis before applying power to the instrument.

To remove a socketed dual-in-line packaged (DIP) integrated circuit (IC), pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

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WARNING

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and wait at least three minutes for the line-rectifier filter capacitors to discharge.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

Circuit boards in this instrument may have many conductive layers. Conductive paths between the top and bottom board layers may connect to one or more inner layers. If any inner-layer conductive path becomes broken due to poor soldering practices, the board becomes unusable and must be replaced, Damage of this nature can void the instrument warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument.

Desoldering parts from multilayer circuit boards is especially critical. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded, antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of a circuit board may cause damage to the reverse side of the circuit board. The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.

2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.

4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.

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5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in step 3).

7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

REMOVAL AND REPLACEMENT INSTRUCTIONS

The exploded view drawings in the Replaceable Mechanical Parts list (Section 9) may be helpful during the removal and reinstallation of individual sub-assemblies or components. Circuit board and component locations are shown in the Diagrams section.

Cabinet

WARNING

To avoid electric shock, disconnect the instrument from the ac-power-input source before removing or replacing any component or assembly.

To remove the instrument cabinet, perform the following steps:

NOTE

For instruments with a power-cord securing clamp, remove the Phillips-head screw holding the power-cord securing clamp before disconnecting the power cord.

1. Disconnect the power cord from the instrument.

2. Remove two screws, one each from the right-rear side and bottom front of the cabinet.

3. Remove two screws from each side of the rear panel and remove the panel from the instrument.

4. Remove four screws from the left rear side of the cabinet that secure the side panel to the instrument side chassis.

5. Remove the side panel from the instrument.

6. Pull the front panel and attached chassis forward and out of the cabinet.

NOTE

To ensure that the cabinet is properly grounded to the instrument chassis, the screws at the right-rear side and the bottom front of the cabinet must be tightly secured.

To reinstall the cabinet, perform the reverse of the preceding steps. Ensure that the cabinet is flush with the rear of the chassis and that the cabinet and rear-panel holes are aligned with the screw holes in the chassis frame.

Bezel Buttons Flex Circuit

The Bezel Buttons Flex Circuit that connects between the Front Panel circuit board and the bezel buttons can be removed as follows:

1. Set the instrument on its right side. Pull the Bezel Button Flex Circuit out of J9005 on the Front-Panel circuit board (J9005 is located directly below the POWER switch extension shaft).

2. Set the instrument down. Remove the two front-panel screws that secure the plastic crt bezel frame and light filter to the front panel.

3. Pull the bottom of the crt bezel frame out until it clears the front panel; remove the frame.

4. Remove the light filter from the crt bezel frame.

5. Set the crt bezel frame face down on a flat work surface.

6. Insert a small, flat-bladed screwdriver in one of the slots located on either side of the flex circuit, and carefully twist the screwdriver blade until the end of the button spacer unsnaps. Repeat the procedure, using the other slot, to free the button spacer from the crt bezel frame.

7. Remove the button spacer from the crt bezel frame.

8. Use a small, flat-bladed screwdriver to carefully lift the Bezel Buttons Flex Circuit from the two plastic studs, and remove it from the crt bezel frame.

9. If desired, the bezel button assembly may now be separated from the crt bezel frame.

To reinstall the Bezel Button Flex Circuit, perform the reverse of the preceding steps.

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Scale Illumination Circuit Board

The Scale Illumination circuit board can be removed and reinstalled as follows:

1. Perform steps 1 through 3 of the Bezel Button Flex Circuit removal procedure.

2. Remove the screw and shouldered washer from the center of the plastic graticule light reflector; remove the light reflector.

3. Set the instrument on its right side. Disconnect the Scale Illumination connector from J9882 on the Main circuit board. (J9882 is located at the front edge of the Main circuit board, directly below the crt.)

4. Remove the Scale Illumination circuit board from the front subpanel.

To reinstall the Scale Illumination circuit board, perform the reverse of the preceding steps.

Storage Circuit Board in Servicing Position

The following procedure describes how to secure the Storage circuit board into the servicing position to facilitate instrument disassembly and reinstallation for individual components or subassemblies.

1. Disconnect the following connectors from the Storage circuit board.

   a. P2111, a four-wire connector located near the middle left edge of the circuit board.

   b. P2112, a four-wire connector located near the middle left edge of the circuit board.

2. Remove four Storage circuit board screws that secure the circuit board to the chassis. (see Figure 6-5 for the location of the screws).

3. Remove the screw near the middle left edge of the circuit board that secures the metal Storage circuit board shield to the chassis.

4. Remove the screw near the front left edge of the circuit board that secures the metal Storage circuit board shield to the chassis.

5. Use one hand to lift the end of the black board latch on the Storage circuit board above the chassis while lifting the left edge of the Storage circuit board upwards with the other hand. Place the board latch tab in the chassis slot to hold the Storage circuit board in the servicing position.

To lower the Storage circuit board into the instrument and to reconnect the connectors, perform the reverse of the preceding steps.

Support Chassis

The support chassis divides the inside of the instrument into two parts by connecting the center of the rear chassis and the front chassis together. The support chassis can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Remove the crt anode lead and High-Voltage Multiplier lead connectors from the anode clip on the Power-Supply shield.

3. Remove the anode clip from the Power-Supply shield through the hole in the support chassis. The clip can be removed by using a small flat-bladed screwdriver to pry apart the mounting prongs and the body of the clip.

4. Remove the two recessed screws from the rear chassis (located directly above the Z-AXIS connector) securing the support chassis.

5. Remove the three screws securing support chassis to the top attenuator shield.

6. Remove the screw securing the front of the support chassis to the aluminum angle bracket attached to the front chassis.

7. Remove the support chassis from the instrument.

To reinstall the support chassis, perform the reverse of the preceding steps.

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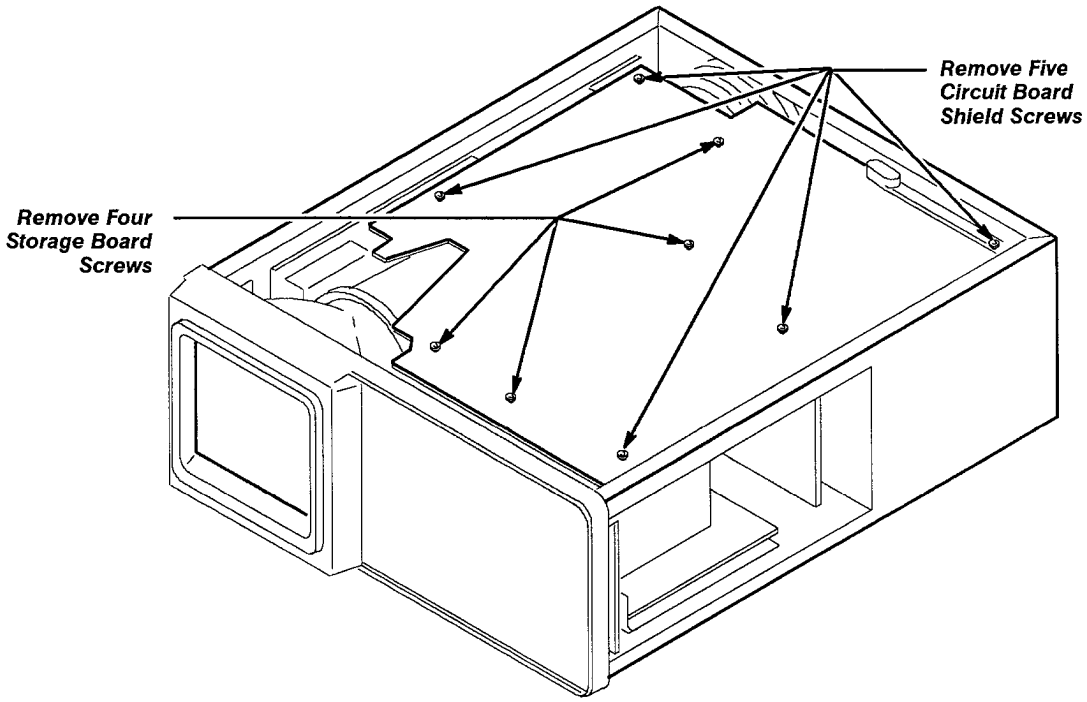


Figure 6–5. Location of screws and spacers on the Storage circuit board.

Side–Chassis Assembly

The Side–Chassis Assembly can be removed and reinstalled as follows:

1. Disconnect the following three connectors from the Side–Chassis Assembly.
   a. P4110, a two–wire connector located at the rear of the Side–Chassis Assembly.
   b. P6423, a four–wire connector located at the rear of the Side–Chassis Assembly.
   c. P9301, a five–wire connector located at the rear of the Side–Chassis Assembly.
2. Remove the two screws from the top of the side chassis and the two screws from the bottom of the side chassis that secure the Side–Chassis Assembly to the instrument.
3. Remove the Side–Chassis Assembly from the instrument.

To reinstall the Side–Chassis Assembly, perform the reverse of the preceding steps.

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Storage Circuit Board and Shield

The Storage circuit board and shield can be removed and reinstalled as follows:

1. Perform steps 1 through 4 of the Storage Circuit Board in Servicing Position procedure.

2. Disconnect P9010, an eight-wire connector located near the right edge of the Main circuit board, in front of the Power-Supply shield.

3. Disconnect the following from the right side of the Storage circuit board:

   a, P9411, a twenty-four-wire connector.

   b. P6100, a sixty-wire connector.

   c. P9211, a ten-wire connector.

   d. P4211, a twelve-wire connector.

4. Remove the recessed screw and chassis-mounted rear hinge nearest to the Board Latch from the instrument (see Figure 6-6 for removal of the chassis recessed screw and hinge).

5. In a similar manner, remove the recessed screw and chassis-mounted front hinge from the instrument.

6. Lift the Storage circuit board assembly slightly and slide it back until the middle hinge separates; lift the assembly out of the instrument.

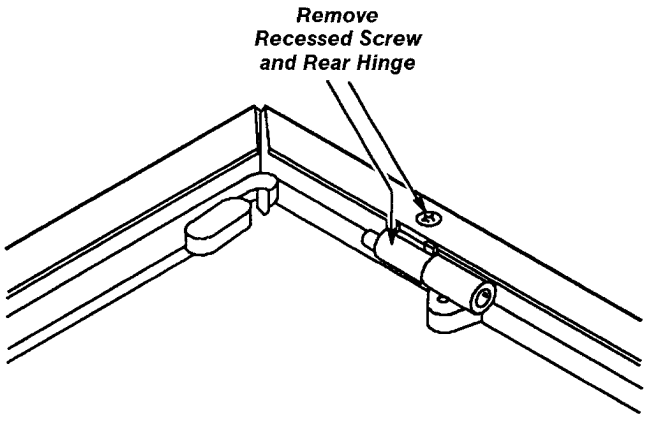


Figure 6-6. Recessed screw and rear hinge removal.

7. To separate the Storage circuit board from the shield, first disconnect P9111 (battery power cable). Then, remove the five screws securing the circuit board to the shield; lift the Storage circuit board away from the shield.

To reinstall the Storage circuit board and shield, perform the reverse of the preceding steps.

Cathode-Ray Tube

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the crt on any object which may cause it to crack or implode. When storing a crt, either place it in a protective carton or set it face down on a smooth surface in a protected location with a soft mat under the faceplate.

The crt can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Perform the Side-Chassis Assembly removal procedure.

3. Disconnect the four deflection-plate wires from the neck pins near the middle of the crt, noting locations for reassembly reference.

4. Unplug the Trace Rotation connector (P9006) from the Front-Panel circuit board (note the location and orientation for reinstallation reference).

WARNING

The crt anode lead and the High-Voltage Multiplier output lead retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, disconnect the High-Voltage Multiplier lead from the crt anode lead and ground both leads to the main instrument chassis.

5. Unplug the crt anode lead connector from the High-Voltage Multiplier lead located between the support chassis and the crt shield. Discharge both the anode lead connector and the High-Voltage Multiplier lead to chassis ground.

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6. Remove two front-panel screws that secure the plastic crt bezel frame and light filter to the front panel.

7. Lower the crt bezel frame until the top clears the front panel. Tip the top of the crt bezel frame out and lay the frame flat on the work surface.

8. Remove the crt socket cap from the rear of the crt socket. Retain the cap for reinstallation.

9. With the rear of the instrument facing you, place the fingers of both hands over the front edge of the front subpanel. Then, using both thumbs, press forward gently on the crt funnel near the front of the crt. When the crt base pins disengage from the socket, remove the crt and the crt shield through the instrument front panel. Place the crt in a safe place until it is reinstalled. If the plastic, crt corner cushion pads fall out, save them for reinstallation.

NOTE

When installing the crt into the instrument, reinstall any loose plastic crt corner pads that are out of place. Ensure all crt pins are straight and that the indexing keys on the crt base, socket, and shield are aligned. Ensure that the ground clip makes contact only with the outside of the crt shield.

To reinstall the crt, perform the reverse of the preceding steps.

Power-Supply Shield

The Power-Supply shield can be removed and reinstalled as follows:

1. Turn the instrument top side down (Main circuit board up).

2. Remove the screw securing the Power-Supply shield to the Main circuit board that is located directly in front of the plastic power supply cover (near the middle of the side chassis frame).

3. Remove the screw located near the center of the board that secures the plastic power-supply cover. Insert a small pointed tool into the hole in the left-rear corner of the rear chassis and gently push down on the power-supply cover tab. Remove the power-supply cover by sliding it out from underneath the rear and side chassis.

4. Set the instrument right side up.

5. Perform the Storage Circuit Board in Servicing Position procedure.

6. Perform the Support Chassis removal procedure.

7. Remove one pan-head and two recessed screws securing the Power-Supply shield to the rear chassis frame. See Figure 6-7 for the location of the three screws on the rear chassis frame.

8. Remove the screw from the front, upper-right hand corner of the Power-Supply shield.

9. Remove the cables from the retaining clips on the front of the power supply shield.

10. Remove the Power-Supply shield from the chassis frame.

NOTE

When reinstalling the Power-Supply shield, ensure that the shield is placed in the frame guides on the rear chassis above the fuse holder and that the crt socket-wire assembly and crt anode lead are properly placed in their respective cutouts.

To reinstall the Power-Supply shield, perform the reverse of the preceding steps.

Line Filter Circuit Board and Cover

To remove the Line Filter circuit board and cover, perform the following steps:

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Perform the Power-Supply Shield removal procedure.

3. Remove the two recessed screws that secure the Line Filter circuit board to the rear chassis; lift the Line Filter circuit board out and away from the filter capacitor.

4. Unclip the plastic cover from the Line Filter circuit board.

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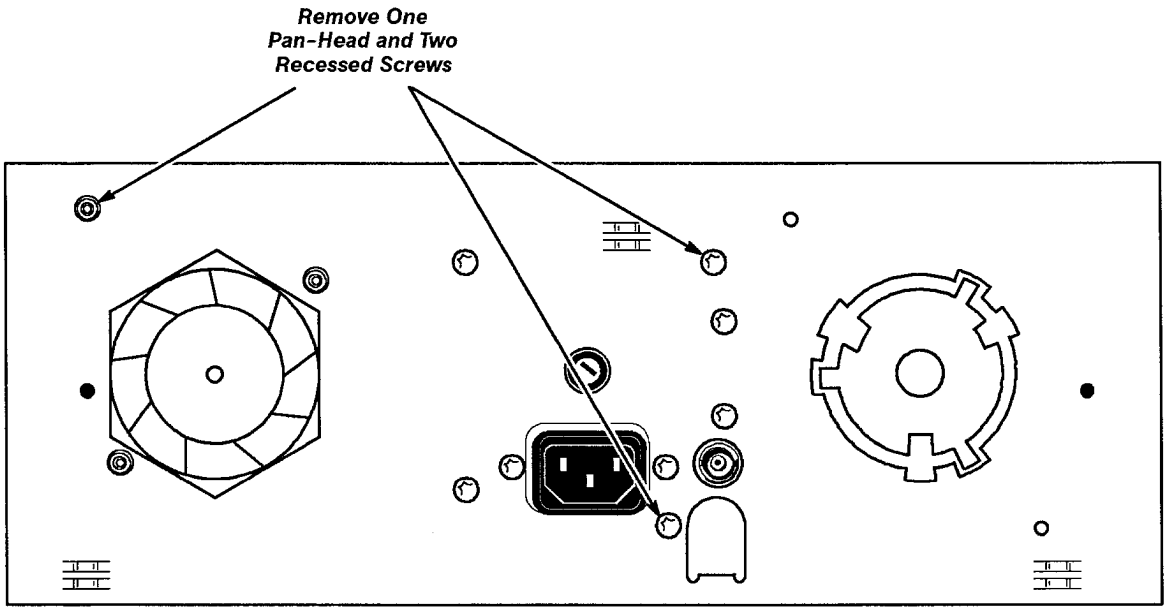


Figure 6-7. Location of screws securing Power Supply shield and the support bracket to the rear chassis frame.

5. Unsolder the following:

   a. The wire from the line fuse holder that connects to W9011 on the Line Filter circuit board.

   b. The wire from Line Filter FL9001 that connects to W9091 on the Line Filter circuit board.

   c. The wire from W9190 on the Main circuit board (labeled on circuit view side) that connects to W9191 on the Line Filter circuit board.

   d. The wire from W9040 on the Main circuit board (labeled on circuit view side) that connects to W9041 on the Line Filter circuit board.

6. Remove the Line Filter circuit board from the instrument.

To reinstall the Line Filter circuit board and cover, perform the reverse of the preceding steps.

Fan

The fan can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Perform the Power-Supply Shield removal procedure.

3. Unsolder the two fan driver leads from the Main circuit board (the solder pads are labeled W9965 R and B).

4. Remove two screws securing the fan to the rear chassis and two recessed screws securing the fan driver to the side chassis. Remove the fan and driver assembly.

To reinstall the fan, perform the reverse of the preceding steps.

Thermal Shutdown Circuit Board

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Perform the Power-Supply Shield removal procedure.

3. Perform the Fan removal procedure.

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4. Set the instrument on its left side. Use a vacuum-desoldering tool to unsolder the three Thermal Shutdown circuit board interconnecting pins from the Main circuit board. (The pins are labeled W950 on the circuit view side of the Main circuit board.)

To reinstall the Thermal Shutdown circuit board, perform the reverse of the preceding steps.

Alternate Sweep Circuit Board

The Alternate Sweep circuit board can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.
2. Disconnect P4220, a four-wire connector located on the right side of the Alternate Sweep circuit board.
3. Set the instrument on its left side.
4. Use a vacuum-desoldering tool to unsolder the 27 Alternate Sweep circuit board pins from the Main circuit board. (The pins are labeled W9400 on the circuit view side of the board.)
5. Unclip the Alternate Sweep circuit board from the plastic holder mounted on the Power-Supply shield; remove the Alternate Sweep circuit board from the instrument.

To reinstall the Alternate Sweep circuit board, perform the reverse of the preceding steps.

Channel 1 Logic and Channel 2 Logic Circuit Boards

The Channel 1 Logic and Channel 2 Logic Circuit Boards can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.
2. Perform the Support Chassis removal procedure.
3. Remove the remaining six screws that secure the top attenuator shield to the Attenuator circuit board and bottom shield.
4. Remove the top attenuator shield from the instrument.
5. Disconnect the following connectors from the Channel 1 Logic and Channel 2 Logic circuit boards, noting their locations for reinstallation reference:
   a. P6111, a three-wire connector from Channel 1 Logic circuit board.
   b. P6112, a three-wire connector from Channel 2 Logic circuit board.
6. Remove one screw each from the front of the Channel 1 Logic and Channel 2 Logic circuit boards.
7. Unsolder the two 0 Ω dummy resistors connected between the CAL variable resistor/switch assemblies and the rear of the Channel 1 and Channel2 Logic circuit boards.
8. Remove the Channel 1 Logic and Channel 2 Logic circuit boards from the instrument.

To reinstall the Channel 1 Logic and Channel 2 Logic circuit boards, perform the reverse of the preceding steps.

Attenuator, Channel 1 Logic and Channel 2 Logic Circuit Boards Assembly

The Attenuator, Channel 1 and Channel 2 Logic Circuit Boards Assembly can be removed and reinstalled as follows:

1. Turn the instrument over (Main circuit board up). Remove the two screws securing the Attenuator circuit board to the BNC bracket (located underneath the CH 1 OR X and CH 2 OR Y input connectors).
2. Unsolder the resistor leads connected to the center pins of the CH 1 OR X and CH 2 OR Y input connectors. Set the instrument right side up.
3. Perform the Storage Circuit Board in Servicing Position procedure.
4. Use a 1/16-inch hex wrench to loosen the set screws on both the CH 1 and CH 2 VOLTS/DIV Variable knobs and remove the knobs.
5. Set the CH 1 and CH 2 VOLTS/DIV switches to the same position. Note switch positions for reinstallation reference. Remove the knobs by pulling them straight out from the front panel.
6. Perform the Support Chassis removal procedure.
7. Remove the remaining six screws that secure the top attenuator shield to the Attenuator circuit board and bottom shield.
8. Remove the top attenuator shield from the instrument.

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9. Disconnect the following connectors from the Channel 1 Logic, Channel 2 Logic and Attenuator circuit boards, noting their locations for reinstallation reference:

   a. P6111, a three-wire connector from Channel 1 Logic circuit board.

   b. P6112, a three-wire connector from Channel 2 Logic circuit board.

   c. P9103, a four-wire connector located behind the CH 1 VOLTS/DIV switch assembly and underneath the Channel 1 Logic circuit board.

   d. P9108, a four-wire connector located behind the CH 2 VOLTS/DIV switch assembly and underneath the Channel 2 Logic circuit board.

   e. P9991, a three-wire connector located at the rear of the Attenuator circuit board between the Channel 1 and Channel 2 Logic circuit boards.

10. Remove the screw from the left rear corner of the Attenuator circuit board.

11. Pull the Attenuator, Channel 1 Logic and Channel 2 Logic circuit boards assembly straight back from the front of the instrument until the circuit boards' interconnecting pins are disengaged and the switch shafts are clear of both the Front-Panel circuit board and the two Input Coupling switch shafts (located between the front panel and the subpanel). Then lift out the entire assembly through the top of the instrument.

12. If removal of Channel 1 Logic and Channel 2 Logic circuit boards from the assembly is desired, perform the Channel 1 Logic and Channel 2 Logic Circuit Boards removal procedure steps 6 through 8.

NOTE

When reinstalling the Attenuator, Channel 1 and Channel 2 Logic circuit boards Assembly, ensure that the interconnecting pins are aligned with the Front-Panel circuit board connectors and that the two resistors (soldered to the bottom of the Attenuator circuit board) are not touching the Front-Panel circuit board. Push the Attenuator circuit board forward and, at the same time, press the front end of the board down slightly. Align the two Input Coupling switch shafts with the front-panel holes by moving either the Channel 1 or the Channel 2 Input Coupling switch knob.

To reinstall the Attenuator, Channel 1 and Channel 2 Logic circuit boards assembly, perform the reverse of the preceding steps.

Sweep Reference Circuit Board

The Sweep Reference circuit board can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Disconnect the following from the Sweep Reference circuit board:

   a. P9410, a nine-wire connector located near the right rear corner of the circuit board.

   b. P5201, a three-wire connector located near the right front corner of the circuit board.

3. Locate the two resistors that connect between the Timing circuit board and the Sweep Reference circuit board near the right side of the SEC/DIV variable control. Unsolder the leads of the two resistors from the Timing Circuit board.

4. Loosen the setscrews that secure the extension shaft connected to the SEC/DIV variable control (S721/R721) with a 0.050-hex wrench.

5. Remove the SEC/DIV variable control nut with a 9/16 inch open-end wrench.

6. Remove the Sweep Reference circuit board.

To reinstall the Sweep Reference circuit board, perform the reverse of the preceding steps.

Timing, Sweep Interface, and Sweep Reference Circuit Boards Assembly

The Timing, Sweep Interface, and Sweep Reference circuit boards assembly can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.

2. Use a 1/16-inch hex wrench to loosen the set screw of the SEC/DIV Variable knob. Remove the SEC/DIV Variable knob.

3. Set both A and B SEC/DIV knobs to the EXT CLK position. Use a 1/16-inch hex wrench to loosen the two set screws that secure the A and B SEC/DIV knob; pull the knob from the shaft assembly.

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4. Use a 1/16-inch hex wrench to loosen two set screws securing the A SEC/DIV dial to the shaft assembly. Remove the dial from the shaft.

5. Disconnect the following connectors from the assembly, noting their locations for reinstallation reference:

   a. P9700, a 10-wire connector located on the right edge of the Timing circuit board.

   b. P6421, an five-wire connector located on the Sweep Interface circuit board.

   c. P9410, a nine-wire connector located near right rear corner of the Sweep Reference circuit board.

6. Disconnect P9705, an eight-wire connector located on the Main circuit board between the Attenuator board and the left edge of the Alternate Sweep board.

7. Remove the screw located at the right rear of the Attenuator circuit board (securing both the Attenuator and the Timing circuit boards to the Bottom shield).

8. Remove the three securing screws from the Timing circuit board (the screws are located at the right front corner, left front side by the SEC/DIV switch shaft, and at the right rear corner of the circuit board).

9. Pull the Timing circuit board straight back from the front of the instrument until the circuit board interconnecting pins are disengaged and the switch shaft is clear of the Front-Panel circuit board.

10. If removal of the Sweep Reference circuit board from the assembly is desired, perform the Sweep Reference Circuit Board removal procedure, steps 2b through 6.

NOTE

Ensure that the Timing circuit board interconnecting pins are aligned to the Front-Panel circuit board connectors before reinstallation.

To reinstall the Timing, Sweep Interface, and Sweep Reference circuit boards assembly, perform the reverse of the preceding steps.

Sweep Interface Circuit Board Separation

To remove the Sweep Interface circuit board from the Timing circuit board perform the following steps.

1. Use a vacuum-desoldering tool to unsolder the 22 interconnecting pins (W1304) from the Sweep Interface to the Timing circuit board.

2. Remove the Sweep Interface circuit board and clean the wire-strap holes in the Timing circuit board.

To reinstall the Sweep Interface circuit board, perform the reverse of the preceding steps.

Bottom Shield, Attenuator and Timing Circuit Boards Assembly

The Bottom Shield, Attenuator, and Timing circuit boards assembly can be removed and reinstalled as follows:

1. Set the instrument upside down. Remove the three screws and one spacer post securing the Bottom shield to the Main circuit board.

2. Perform steps 1 through 9 of the Attenuator, Channel 1 Logic and Channel 2 Logic Circuit Boards Assembly removal procedure.

3. Perform steps 2 through 6 of the Timing, Sweep Interface, and Sweep Reference Circuit Boards Assembly removal procedure.

4. Disconnect the extension shaft from the FOCUS control and pull the extension shaft out through the front panel.

5. Pull the Bottom shield, along with the attached circuit boards straight back from the front of the instrument until the interconnecting pins on the circuit boards are disengaged and the switch shafts are clear of the holes in the Front-Panel circuit board; then lift out the entire assembly through the top of the instrument.

6. If accessibility to the bottom of either the Attenuator or the Timing circuit board is desired, perform step 10 of the Attenuator, and Channel 1 and Channel 2 Logic Circuit Boards Assembly removal procedure and step 8 of the Timing, Sweep Interface, and Sweep Reference Circuit Boards Assembly removal procedure.

To reinstall the Bottom Shield, Attenuator, and Timing circuit boards assembly, perform the reverse of the preceding steps.

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Front-Panel Circuit Board

The Front-Panel circuit board can be removed and reinstalled as follows:

1. Set the instrument upside down. Unsolder the resistor lead connected to the EXT INPUT center connector and the wire strap connected to the EXT INPUT ground lug terminal.
2. Unsolder the resistors from the CH 1 and CH 2 input bnc connectors (two resistors from each connector), noting locations for reassembly reference.
3. Pull the bezel button flex circuit out of J9005 on the Front-Panel circuit board (J9005 is located directly below the POWER switch extension shaft).
4. Set the instrument right side up and perform the Storage Circuit Board in Servicing Position procedure.
5. Perform the Support Chassis removal procedure.
6. Perform the Cathode-Ray Tube removal procedure.
7. Perform the Bottom shield, Attenuator and Timing Circuit Boards Assembly removal procedure.
8. Remove the following friction-fit knobs by pulling them straight out from the front panel:
   a. Channel 1 POSITION.
   b. A/B SWP SEP.
   c. Channel 2 POSITION.
   d. Horizontal POSITION.
   e. B TRIGGER LEVEL.
   f. A TRIGGER LEVEL.
9. Remove the following knobs after loosening their setscrews using a 1/16-inch hex wrench:
   a. B INTENSITY.
   b. A INTENSITY.
   c. CURSORS.
   d. VAR HOLDOFF.
   e. GRATICULE INTENSITY.
   f. STORE/READOUT INTENSITY.
10. Disconnect the following multi-pin connectors from the Main circuit board:
    a. P9003, located at the front right corner of the circuit board.
    b. P9002, located at the front of the circuit board, near the CH 2 Input bnc.
    c. P9001, located at the front of the circuit board, near the power switch shaft extension. After disconnecting the plug, guide it under the shaft extension to allow removal of the Front Panel assembly.
11. Remove the four screws securing the Front Panel circuit board to the front chassis.
12. To facilitate removal of the Front Panel circuit board, remove the two recessed screws that secure the chassis halves together at the front right corners of the instrument.
13. Pull the Front-Panel circuit board straight back until the control shafts clear the subpanel. Remove the Front-Panel circuit board from the instrument.

To reinstall the Front-Panel circuit board, perform the reverse of the preceding steps.

Main Circuit Board

All components on the Main circuit board are accessible either directly or by removing either the Storage circuit board, the crt, the Bottom shield, Attenuator, Timing circuit-boards assembly, and the Power-Supply shield. Removal of the Main circuit board is required only when it is necessary to replace the circuit board with a new one.

The Main circuit board can be removed and reinstalled as follows:

1. Perform the Storage Circuit Board in Servicing Position procedure.
2. Perform the Support Chassis removal procedure.
3. Perform the Side-Chassis Assembly removal procedure.
4. Disconnect the three-wire B DELAY TIME POSITION potentiometer connector P9644 from the Main circuit board (located near the right edge of the circuit board adjacent to the DELAY START potentiometer).
5. Perform the Alternate Sweep Circuit Board removal procedure.

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6. Disconnect the connectors from the Attenuator and Timing circuit boards assembly by performing steps 7 through 9 of the Attenuator, Channel 1 Logic and Channel 2 Logic Circuit Boards Assembly removal procedure and steps 5 and 6 of the Timing, Sweep Interface and Sweep Reference Circuit Boards Assembly removal procedure.

7. Disconnect P9001, a twenty-wire connector located between the crt and the CH 1 Attenuator assembly, from the Main circuit board.

8. Set the instrument on its left side. Disconnect the graticule lights cable from J9882 on the Main circuit board.

9. Remove the three screws and one spacer securing the Bottom shield to the Main circuit board.

10. Perform the Power-Supply Shield removal procedure.

11. Unsolder the two wires from W9190 and W9040 on the Main circuit board that connect to the Line Filter circuit board, noting locations for reassembly reference.

12. Unsolder the rear-panel EXT Z AXIS connector wire from the Main circuit board.

13. Unsolder the two leads on the Main circuit board from the fan driver (labeled W9965 R and B on the circuit view side of the board).

14. Unsolder the three leads on the chassis mounted CR970 from the Main circuit board (labeled W9080 R, B, and O).

15. Remove the FOCUS control shaft assembly by pulling it straight out from the front panel.

16. Remove the POWER switch extension-shaft assembly by first pressing in the POWER button to the ON position. Then insert a scribe (or similar tool) into the notch between the end of the switch shaft and the end of the extension shaft and gently pry the connection apart. Push the extension shaft forward, then sideways, to clear the switch shaft. Finally, pull the extension shaft back and out of the instrument.

17. Remove two recessed screws securing the power-supply transistor heat-sink assembly to the right side of the chassis frame.

WARNING

The crt anode lead and the output terminal to the High-Voltage Multiplier will retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, ground the crt side of the anode lead to the main instrument chassis.

18. Disconnect the crt anode lead from the High-Voltage Multiplier anode lead by carefully pulling the anode plug out of the jack. Discharge the plug tip to the chassis.

19. Unsolder two sets of crt socket wires from the Main circuit board, noting wire colors and positions for reinstallation reference. The solder pads for the two sets of wires are labeled W9870 on the Main circuit board.

20. Unsolder two sets of delay-line wires from the Main circuit board, noting wire colors and positions for reinstallation reference.

21. Remove three screws securing the Main circuit board to the instrument chassis frame (one under the EXT Z AXIS connector and two along the left side of the Main circuit board).

22. Release the board latch holding the Storage circuit board in the servicing position and lower the Storage circuit board. Carefully turn the instrument upside down (Main circuit board up).

23. Lift the front of the Main circuit board far enough to disconnect the two twenty-wire connectors, P9003 and P9002, from the component side of the Main circuit board. (The remaining cable from the Front Panel circuit board was disconnected in step 7.)

24. Carefully lift the Main circuit board and attached cables from the bottom of the chassis.

NOTE

When installing the Main circuit board, ensure that the circuit board is in the guides at the rear and right side of the frame.

To reinstall the Main circuit board, perform the reverse of the preceding steps.

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OPTIONS

INTRODUCTION

This section is divided into two subsections. The first contains a general description of available instrument options and the second contains servicing information for the Option 10 and Option 12 Communications interfaces.

Additional information about instrument options or option availability can be obtained either by consulting the current Tektronix Product Catalog or by contacting your local Tektronix Field Office or representative.

OPTIONS DESCRIPTION

INTERNATIONAL POWER CORD OPTIONS

Instruments are shipped with the detachable power–cord option ordered by the customer. Descriptive information about the international power–cord options is provided in Section 2, Preparation for Use. The following list identifies the Tektronix option number for the available power cords.

Standard	120 V	United States
Option A1	220 V	Universal Euro
Option A2	240 V	United Kingdom
Option A3	240 V	Australian
Option A4	240 V	North American
Option A5	220 V	Switzerland

OPTION 10

Option 10 provides a GPIB (General Purpose Interface Bus) communications interface. The interface implemented conforms to the specifications contained in IEEE Standard Digital Interface for Programmable Instrumentation (ANSI/IEEE Std 488–1978). It also complies with a Tektronix Standard relating to GPIB Codes, Formats, Conventions and Features. For description of the operating information on the Option 10, refer to the Options and Accessories section of the 2232 Operators Manual.

OPTION 12

Option 12 provides an RS–232–C serial communications interface. The interface provides both DTE and DCE capability to aid in hooking up the various types of printers, plotters, personal computers, and modems that may be encountered. For description of the operating information on the Option 12, refer to the Options and Accessories section of the 2232 Operators Manual.

OPTION 33

Option 33, the Travel Line option, provides impact protection needed for rough industrial and service environments. When the instrument is ordered with Option 33, it comes equipped with the Accessory Pouch, the Front Panel cover, shock–absorbing rubber guards mounted on the front and rear of the cabinet, an easy–to–use power–cord wrap, and a carrying strap.

SERVICING INFORMATION

OPTION 10 THEORY OF OPERATION

The General Purpose Interface Bus (GPIB) option (see Diagram 23) provides a general purpose interface for the exchange of waveform data and instrument–state information. Temporary storage and program memory for the option is provided by the host instrument RAM and ROM.

The XY Plotter circuitry is unchanged from the standard instrument. The circuit descriptions covering the standard XY Plotter still apply, and are not repeated

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here. The following discussion refers only to the GPIB portion of the board.

The board contains an interface to the GPIB port. Supporting the GPIB port are two 8–bit input ports for status signals and parameter switches, and a 1–bit output port used for diagnostics. The remainder of the circuitry provides signal buffering and address decoding.

The microprocessor bus extends to this option through W8100. The address bus, the data bus, the bus control signals, and several address decode lines which are generated on the storage board are included. Power supplies are also brought in through this connector, and J9301 in the XY Plotter portion of the board is not used.

Bus Buffers

The address lines are buffered by U1341 and U1333. The buffers are always enabled. Bidirectional data bus buffer U1331 isolates the circuitry from the storage board and provides improved signal drive capability. Also buffered are the RD(L), WR(L), 6.7MHZCLK, and RESET signals.

The I/O devices occupies several addresses in the I/O–SEG range (40000 to 4FFFF). Table 3–1 lists the actual addresses used.

Primary address decoding is accomplished by U1345. It provides a one–of–eight, active–LO signal when BA12, BA13, I/O_SEG(L), and BLK0(L), are all LO. Three address lines, BA3, BA6, and BA7, are decoded to produce the eight strobes. Four of the strobes enable the GPIB controller U1351, Parameter buffer U1322, Status buffer U1323, and Diagnostic latch U1335. Also generated by U1345 is a signal that is LO whenever one of the strobes is enabled and BA8 is LO. This signal is gated with COM_SEG(L) and DEN(L) in U1332 to produce an enable for data buffer U1331 via U1344C.

Half of U1332 generates the DATEN(L) enable for the data bus buffer. When DEN(L) is LO and either I/O_20PT(L) or COM_SEG(L) is LO, pin 8 of U1332 goes HI. U1344 inverts this signal, producing DATEN(L). The data bus buffer is enabled only for references in COM SEG or to I/O ports used by the GPIB option.

GPIB Controller

The GPIB controller, U1351, handles much of the protocol required to interface to the IEEE STANDARD 488 bus. The controller has eight internal registers decoded by RS0, RS1, and RS2. Under certain conditions it generates an interrupt to the microprocessor which appears as a LO_INT(L) (U1351 pin 9). This pin is an open drain output connected to the microprocessor's maskable interrupt.

Data bus lines are reversed, BD0 for BD7, to accommodate the internal convention of the GPIB controller.

Trigger signal TR, U1351 pin 39, is used only for diagnostics and is read by the microprocessor via U1322 pin 2.

Line Drivers

Bus buffers U1324 and U1325 provide the drive characteristics required by IEEE 488 bus standards. They also control characteristics of the drive circuitry during bus operation.

All of the signal lines that are at GPIB levels are protected by diode arrays CR1321, CR1322, and zener diode VR1321. These networks clip voltage transients greater than +6.8 volts or less than 0.6 volts.

Connector J1314 is a standard GPIB interface connector.

Clock Divider and Diagnostic Latch

U1335 is a dual J–K flip–flop that performs two independent functions. U1335A divides the 6.7 MHz clock by two for GPIB controller U1351. U1335B provides a one–bit latch for diagnostic use. When its enable (clock), U1335B pin 12, is strobed LO, the data on BD0 is latched.

Parameter Buffer

Parameter buffer U1322 provides an eight–bit input port for selecting parameters associated with the GPIB option such as address and terminator. It consists of U1322, S1321, and part of resistor pack R1322. The switch is sensed by enabling buffer U1322 which gates its inputs onto the data bus. Bit 7 is used to sense TR, U1351 pin 39, for diagnostic use.

Status Buffer

Status buffer U1323 is used to sense three of the GPIB PARAMETER switch positions as well as miscellaneous other signals. Buffer circuitry consists of U1323, S1321, R1321, and part of resistor pack R1322. Status buffer functions are shown in Table 7–1.

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Table 7–1
GPIB Status Buffer Functions

BIT	Signal Name	Function
Bit 0	PWR-IN(L)	Power going down interrupt
Bit 1	$+5V_P$	Logic HI
Bit 2	TRIG	GPIB chip diagnostic
Bit 3		PARAMETER SWITCH position 8
Bit 4		PARAMETER SWITCH position 10
Bit 5		PARAMETER SWITCH position 9
Bit 6	$+5V_P$	Logic HI
Bit 7	DIAG	Diagnostic latch

OPTION 12
THEORY OF OPERATION

The RS–232–C communication option (see Diagram 22) provides a general–purpose interface for the exchange of waveforms and instrument–state information. Temporary storage and program memory for the option is provided by the instrument RAM and ROM.

The RS–232 option replaces the XY Plotter board of the standard instrument but includes the XY Plotter circuitry. The following discussion refers only to the RS–232–C portion of the board.

Supporting the RS232 port are two 8–bit input ports for status signals and parameter switches, and a 4–bit output port used mainly for interrupt masking. The remaining circuitry either decodes addresses or buffers signals.

Microprocessor bus signals are extended to this board through W8101. The address bus, data bus, bus control signals, several address decode lines, and power supplies all pass through this connector.

Bus Buffers

The address lines are buffered by U1241 and U1233. These buffers are always enabled. Data bus buffer U1231 is bidirectional. It isolates the option from the storage board and improves signal driving capabilities. Also buffered are the RD(L) (U1233), WR(L) (U1234D), and RESET (U1244E) signals.

Several addresses in the I/O–SEG range (40000 to 4FFFF) are used by option I/O circuitry. Table 3–1 lists the actual addresses used.

Primary address decoding is accomplished by U1245. It provides a one–of–eight, low–asserting signal when BA12, BA13, IO_SEG(L), and BLK0(L), are all LO. Address lines BA3, BA6, and BA7 are decoded to produce eight strobes. Three of the strobes are used to enable Universal Asynchronous Receiver/Transmitter (UART) U1251, parameter buffer U1222, and Status buffer U1223. A fourth strobe is gated with BWR(L) at U1234A to produce a write strobe for the interrupt mask latch (U1236). Also generated by U1245 is a signal that is LO whenever one of the strobes is enabled and BA8 is LO. This signal is gated with COM_SEG(L) and DEN(L) in U1232A to produce an enable for the data bus buffer (U1231).

Half of U1232 and inverter U1244C generate the DATEN(L) signal for the bidirectional data bus buffer U1231. DATEN(L) is LO for any reference in COM–SEG and for references to the option I/O ports. It is LO when DEN(L), the data enable from the processor, is LO and either COM_SEG(L) or I/O(L) (U1245 pin 3) is LO.

UART

The UART U1251 communicates with the Microprocessor, providing serial–to–parallel conversion and handling some of the RS232 protocol. Also included is an internal baud rate generator. Crystal Y1251 provides a time base which is divided by software selectable ratios to provide the required bit transfer speeds. Three interrupt lines, INTR, TBRE, and DR, inform the Microprocessor that intervention is required.

Line Drivers

Driver U1225 translates from TTL logic levels to the levels required by the EIA RS–232–C standard. It requires positive and negative supplies which are derived by diodes isolation (CR1224 and CR1223) on the +8.6 V and −8.6 V supplies. Diode isolation protects the instrument from transients or faults coupled through the RS–232–C connectors. The RLSD signal is generated by Interrupt Mask Latch U1236.

The RS–232–C receiver is U1224. It translates from RS–232–C levels to TTL logic levels and also has a protected supply. Its +5 V supply is generated by dropping the +8.6 V supply through zener diode VR1232. The IRSLD2 signal goes to Status Buffer U1223.

All of the RS–232–C signals are protected by diode arrays CR1221 and CR1222, and zener diodes VR1221 through VR1224. Any transients that exceed a ±25 V range are clipped by the networks.

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Two connectors, J1212 and J1214, are provided to make interfacing easier. The male DB−25 connector conforms to the DTE (data terminal equipment) specifications of RS−232−C, and the female DB−25 connector conforms to the DCE (data communications equipment) specification. Only one of the connectors may be used at one time.

Interrupt Circuitry

Two interrupt lines from the UART, INTR and DR, are combined via OR gate U1234B, generating the DR+INTR interrupt line. That signal is then routed to U1232A, an AND−OR−INVERT gate, where it is gated with DR+INTR MASK, which comes from the Interrupt Mask Latch (U1236). When DR+INTR MASK is LO, DR+INTR can not propagate through to the output. TBRE is similarly masked by TBRE MASK, then they are ORed together and inverted within the AND−OR−INVERT gate. Inverter U1244D inverts the signal and applies it to the base of Q1221. Transistor Q1221 inverts the signal to INTR(L), driving the Microprocessor maskable interrupt.

Interrupt Mask Latch

Interrupt Mask Latch U1236 provides four signals that are directly controlled by the Microprocessor. It is enabled when the Microprocessor writes to the addresses decoded as LATCH(L). This latch uses BA0 and BA1 to select either 0D, 1D, 2D, or 3D, and latches the data present on U1236 pin 13 into the selected output when enabled. Two of the outputs are used for interrupt masking, one for the RS−232−C port, and one for diagnostics. The outputs are forced LO by the VI(L) line to insure that interrupts are masked when the Microprocessor powers up.

Parameter Buffer

This circuit is an eight−bit input port for selecting parameters associated with the option such as baud rate and parity. It consists of buffer U1222, switch S1221, and resistor pack R1222. The switch is sensed by enabling the buffer which gates the buffer inputs onto the data bus. Bit 7 is used to sense serial data out (SDO) from U1251 for diagnostic use.

Status Buffer

Status buffer U1223 is used to sense three positions of Parameter switch S1221 as well as miscellaneous other signals. Functions of the Status buffer are shown in Table 7−2.

Table 7−2
RS−232−C Status Buffer Functions

BIT	Signal Name	Function
Bit 0	PWR_IN(L)	Power going down interrupt
Bit 1	DR+INT(L)	Logic HI
Bit 2	TBR	GPIB chip diagnostic
Bit 3		PARAMETER SWITCH position 8
Bit 4		PARAMETER SWITCH position 10
Bit 5		PARAMETER SWITCH position 9
Bit 6	DIAG	Logic HI
Bit 7	DCD2(L)	Diagnostic latch

PERFORMANCE CHECK PROCEDURE

Introduction

This part of Section 7 contains the GPIB Option and RS−232−C portion of the instrument's performance check procedures. The Performance Check Procedure is used to check the GPIB Option performance against the requirements listed in Table 1−1. It is not necessary to remove the instrument cover to accomplish any of the performance checks.

The Option performance check intervals are identical to the basic instrument as indicated in Performance Check Interval in the Performance Check Procedure Section 4 of this manual.

Limits and Tolerances

The limits and tolerances stated in this procedure are GPIB and RS−232−C specifications only if they are listed in the Performance Requirements column of Table 1−1. The tolerances given in this procedure are valid for an instrument that is operating in and has been previously calibrated in an ambient temperature between +20°C and +30°C. The instrument also must have had at least a 20−minute warm−up period. Refer to Table 1−1 for tolerances applicable to an instrument that is operating outside this temperature range. All tolerances specified are for the instrument only and do not include test−equipment error. When performing either the GPIB or the RS−232 checks, it is assumed that the standard instrument meets all of its Performance Requirements as stated in the Specification (Section 1) of the Service manual.

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Test Equipment Required

Test equipment listed in Table 7–3 is required to perform this procedure. Test equipment specifications described in Table 7–3 are the minimum necessary to provide accurate results. Therefore, equipment used must meet or exceed the listed specifications. Detail operating instructions for test equipment are not given in this procedure.

When equipment other than that recommended is used, control settings of the test setup may need to be altered. If the exact item of equipment given as an example in Table 7–3 is not available, check the Minimum Specification column to determine if any other available test equipment might suffice for the performance check procedure.

1. GPIB Performance Check

a. Set the RS–232–C Parameter switch to match the requirements of your controller, GPIB Address 1.

b. Set the oscilloscope's front panel controls to obtain a baseline trace.

c. Set the oscilloscope's POWER button to OFF and then to ON.

d. CHECK The SRQ indicator is on when the power–up sequence is finished.

e. Connect the Controller via GPIB cable to the IEEE STD 488 PORT connector.

f. Enter the following program to the Controller.

```
100  Init
110  ! Initialize gpib
120  Gpib adr = 1
130  Open #1:"gpib0(pri="&str$
     (gpib adr)&",EOM=<0>):"
140  ! Poll the instrument
150  Poll srq_stat, srq_addr; gpib_adr
160  ! Get its EVENT code
170  Print #1: "EVENT?"
180  Input #1: eve_code
190  ! Print responses
200  Print "SRQ : ";srq_stat
210  Print " EVENT : ";eve_code
220  Close all
230  end
```

g. Run the program entered in Part f.

h. CHECK The SRQ indicator is turned off.

i. CHECK The controller for SRQ: 65.0 and EVEN: 401.0.

j. Disconnect the test equipment from the instrument.

Table 7–3
Test Equipment Required

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
1. Controller	IEEE–488–1978 compatible.	Signal source.	TEKTRONIX 4041 System Controller
2. GPIB Cable	IEEE–488–1978 compatible.	Signal interconnection.	Tektronix Part Number 012–0630–00
3. RS–232 Cable	Connectors, Male–to–female, 2 meter, 25 wires, general purpose.	Signal interconnection.	Tektronix Part Number 012–0815–00

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2. RS–232–C Performance Check

a. Set the RS–232–C Parameter switch to match the requirements of your controller.

b. Set the oscilloscope's front panel controls to obtain a baseline trace.

c. Set the oscilloscope's POWER button to OFF and then to ON.

d. CHECK The ADDR indicator is on when the power–up sequence is finished.

e. Connect the Controller via RS–232 cable to the RS232 DCE connector.

f. Enter the message "ID?;" from the controller to the RS–232.

g. CHECK The response to the controller from the RS–232 is "TEK/22,V81.1.VERS:XX", where "XX" is the ROM's firmware version number in the instrument.

h. CHECK The SRQ indicator is turned off.

i. Disconnect the test equipment from the instrument.

ADJUSTMENT PROCEDURE

There are no adjustment procedures for the GPIB and RS–232–C Options.

OPTION MAINTENANCE INFORMATION

Maintenance information contained in the Maintenance Section of the manual also applies to these options. Additional information for the Options is contained in this part of the manual.

Diagnostics

The diagnostics for Option 10 and Option 12 are added to the instrument. This discussion describes each diagnostic separately.

Com RB. The menu selected Com RB (communications readback) diagnostic checks the bit paths within the Option. The GPIB circuitry checked includes U1335B and U1323. The RS–232–C circuitry checked includes U1236 and U1223. Data is first written to the Option. Registers are then read and checked for the correct data. If the data read back is in error, the actual data read back is displayed on the crt:

COMM RB : rb(1) = x 2 x 1 & rb(0) = y 2 y 1

where:

rb is the data written to the Option (U1236 pin 7 or U1335 pin 10).

x 1 = y 1 = data read back from the Option (U1223 pin 3 or U1323 pin 3).

x 2 = y 2 = data read back from the Option (U1223 pin 2 or U1323 pin 2).

Comm LB. This test is menu selected and checks the GPIB controller U1321 and associated circuitry by commanding the controller to change its TR output and then checking the TR output. If an error is found it is displayed on the crt:

COMM_LB : FGET NOT SET
or
COMM_LB : FGET NOT CLEAR

Iports. Two additional parts are added to the menu selected Iports (input–ports) diagnostic. Option 10 adds U1322 and U1323. Option 12 adds U1222 and U1223. They are labeled on the crt display as comm_stat u1x23 and comm_param u1x22.

Out Ports. The Option Out–Ports diagnostic is selected at power–up. To start the diagnostic out–ports diagnostic, press and hold any one of the SETUP buttons at power up until the Cal Box appears on the screen. The out–ports diagnostic runs at the same time that the Cal Box is displayed. Option 10 adds U1335B. The pattern seen on U1335B pin 10 is about an eight second square wave. Option 12 adds U1236. The voltage pattern seen on U1236 is a continuous shifting between logic HI and LO levels. Output voltage levels of U1236 shifts first on pin 4 and last on pin 12.

Removal and Replacement Instructions

The exploded view drawings in the Replaceable Mechanical Parts list (Section 9) may be helpful during the removal and reinstallation of the GPIB and RS–232–C assembly and its circuit boards from the instrument. Circuit board and component locations are shown in the Diagrams section.

CABINET. To remove either the GPIB or the RS–232–C Assembly from the instrument, perform the Cabinet removal procedure in the Removal and Replacement Instructions of Section 6. In step 4 of the procedure, remove two screws and two post spacers

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and washers from the GPIB side panel or two screws and four post spacers and washers from the RS–232–C side panel.

GPIB AND RS–232–C ASSEMBLIES. The Option assembly can be removed and reinstalled as follows:

1. Disconnect the following connectors from the Option Assembly and the instrument.

   a. P4110, a two–wire connector located at the rear of the Option1 Assembly.

   b. P6423, a four–wire connector located at the rear of the Option Assembly.

   c. P9301, a five–wire connector located at the rear of the Option Assembly.

   d. P8100, a ribbon cable from the Storage circuit board.

2. Stand the instrument on its side (Option Assembly up) and remove two screws from the extreme edge of the bottom chassis frame underneath the delay line cable.

3. Lay the instrument down and remove the two screws from the top of the chassis frame (located inside the two cutouts on the Storage circuit board). Note the position of the ground clip when removing the screw from the chassis frame.

4. Remove the Option Assembly out from between the top and bottom chassis frames.

5. Slide the Option Assembly forward until the ribbon cable clears the Storage circuit board.

6. Remove the Option Assembly from the instrument by tilting the bottom of the assembly out first.

To reinstall the Option Assembly, perform the reverse of the preceding steps.

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REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

When ordering parts, include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the electrical parts list. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

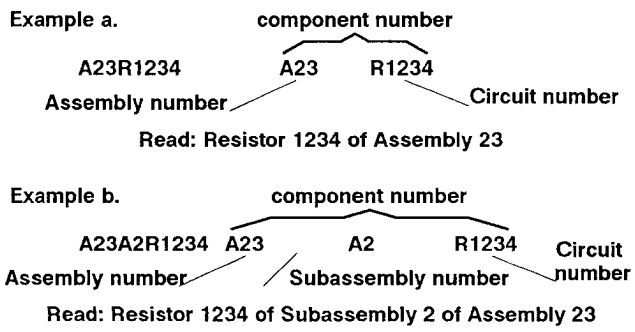
CROSS INDEX–MFR. CODE NUMBER TO MANUFACTURER

The Mfg. Code Number to Manufacturer Cross Index for the electrical parts list is located immediately after this page. The cross index provides codes, names, and addresses of manufacturers of components listed in the electrical parts list.

ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the parts list)



The circuit component's number appears on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the mechanical parts list. The component number is obtained by adding the assembly number prefix to the circuit number.

The electrical parts list is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the electrical parts list.

TEKTRONIX PART NO. (column two of the parts list)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL NO. (columns three and four of the parts list)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the parts list)

In the parts list, an item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. For further item name identification, the U.S. Federal Catalog handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the parts list)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NO. (column seven of the parts list)

Indicates actual manufacturer's part number.

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Mfr. Code	Manufacturer	Address	City, State, Zip Code
D5243	ROEDERSTEIN E SPEZIALFABRIK FUER KONDENSATOREN GMBN	LUDMILLASTRASSE 23-25	8300 LANDSHUT GERMANY
F3223	SGS ATES FRANCE SA	17 AV DE CHOISY	75643 PARIS CEDEX 13 FRANCE
S3774	OSHINO ELECTRIC LAMP WORKS LTD	5 2 MINAMI SHINAGAWA 2 CHORE SHINAGAWA KU	TOKYO JAPAN
TK0FL	UNIVERSAL SCIENTIFIC INDUSTRIAL	141 LANE 351 TAITING RD SEC 1 TSAD TUEN PO BOX 41	MAN TOU HSIEN TAIWAN ROC
TK0IH	SUNONWEALTH ELECTRIC MACHINE IND CO LTD #149, YI YUNG RD, LING TA DISTRICT,	KAOHSIUNG, TAIWAN, R.O.C. P O BOX 1436	KAOHSIUNG, TAIWAN, R.O.C.
TK0032	POWELL ELECTRONICS	411 FAIRCHILD DR	MT VIEW CA 94040
TK0161	WYLE LABORATORIES ELECTRONICS MARKETING GROUP LOS ANGELES DIV	124 MARYLAND ST	EL SEGUNDO CA 90245-4115
TK0196	ALMAC-STROUM ELECTRONICS (DIST)	1885 NW 169TH PLACE	BEAVERTON OR 97006
TK0213	TOPTRON CORP		TOKYO JAPAN
TK0515	EVOX-RIFA INC	100 TRI-STATE INTERNATIONAL SUITE 290	LINCOLNSHIRE IL 60015
TK0891	MICONICS	1 FAIRCHILD AVE	PLAINVIEW NY 11803
TK1326	NORTHWEST FOURSLIDE INC	18224 SW 100TH CT	TUALATIN OR 97062
TK1442	TAIYO-YUDEN (USA) INC	ARLINGTON CENTER 714 W ALGONQUIN RD	ARLINGTON HEIGHTS IL 60005
TK1492	COFER COMPONENT PROCESSING	3270 KELLER ST UNIT 11	SANTA CLARA CA 95050
TK1725	GREENPAR CONNECTORS LTD	PO BOX 15 HARLOW	ESSEX CM20 2ER ENGLAND
TK1727	PHILIPS NEDERLAND BV AFD ELONCO	POSTBUS 90050	5600 PB EINDHOVEN THE NETHERLANDS
TK1743	UNITRODE (UK) LTD	6 CRESSWELL PARK BLACKHEATH	LONDON SE 3 9RD ENGLAND
TK1863	RIVER ELETEC CORP	40-14, NISHI-SINJUKU-4 SHINJUKU-KU	TOKYO JAPAN 160
TK1864	INTERFET CORP	322 GOLD ST	GARLAND TX 75042
TK1899	MINNESOTA MINING AND MFG CO	5400 RT B PO BOX 1228	COLUMBIA MO 65205
TK1913	WIMA THE INTER-TECHNICAL GROUP IND	ONE BRIDGE ST PO BOX 23	IRVINGTON NY 10533
TK2015	PACIFIC HYBRID MICROELECTRONICS INC	10575 SW CASCADE BLVD	PORTLAND OR 97223
TK2073	TOCOS AMERICA INC	565 W GULF ROAD	ARLINGTON HEIGHTS IL 60005
TK2150	CALOGIC CORP	237 WHITNEY PLACE	FREMONT CA 94539
TK2319	COLLMER	14368 PROTON RD	DALLAS TX 75244
TK2411	TEKTRONIX INC, HONG KONG LIMITED	8\F MAPPIN HOUSE 98 TEXACO ROAD	TSUEN WAN, N T, HONG KONG

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Mfr. Code	Manufacturer	Address	City, State, Zip Code
0B0A9	DALLAS SEMICONDUCTOR CORP	4350 BELTWOOD PKWY SOUTH	DALLAS TX 75244
0DWW6	MICRO POWER ELECTRONICS	7973 SW CIRRUS DRIVE BLDG. #22	BEAVERTON OR 97005
0JR03	ZMAN MAGNETICS INC	7633 S 180th	KENT WA 98032
0JR04	TOSHIBA AMERICA INC ELECTRONICS COMPONENTS DIV BUSINESS SECTOR	2692 DOW AVE	TUSTIN CA 92680
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661-2999
0J7N9	MCX INC	30608 SAN ANTONIO ST	HAYWARD CA 94544
0J9R5	MARCON AMERICA CORP	3 PEARL COURT	ALLENDALE NJ 07401
00136	MCCOY ELECTRONICS CO	100 WATTS ST PO BOX B	MT HOLLY SPRINGS PA 17065-1821
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655012	DALLAS TX 75265
01961	VARIAN ASSOCIATES INC PULSE ENGINEERING SUBSIDIARY	7250 CONVOY CT P O BOX 12235	SAN DIEGO CA 92112
02113	COILCRAFT INC	1102 SILVER LAKE RD	CARY IL 60013-1658
02114	PHILIPS COMPONENTS DISCRETE PRODUCTS DIV FERRITE FACILITY	5083 KINGS HWY	SAUGERTIES NY 12477
02660	AMPHENOL CORP INDUSTRIAL TECHNOLOGY DIVISION (ITD)	720 SHERMAN AVENUE PO BOX 4340	HAMDEN CT 06514
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
07416	NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039-2410
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
09969	DALE ELECTRONICS INC	EAST HIGHWAY 50 P O BOX 180	YANKTON SD 57078
1ES66	MAXIM INTEGRATED PRODUCTS INC	120 SAN GABRIEL DRIVE	SUNNYVALE CA 94086
1W344	UNITED CHEMI-CON INC	9801 W HIGGINS SUITE 430	ROSEMONT IL 60018-4704
11236	CTS CORP BERNE DIV THICK FILM PRODUCTS GROUP	406 PARR ROAD	BERNE IN 46711-9506
12617	HAMLIN INC	612 EAST LAKE STREET	LAKE MILLS WI 53551
12697	CLAROSTAT MFG CO INC	LOWER WASHINGTON ST	DOVER NH 03820
12954	MICROSEMI CORP - SCOTTSDALE	8700 E THOMAS RD P O BOX 1390	SCOTTSDALE AZ 85252

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13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		LOS GATOS CA
13556	TRW CYLINDRICAL CONNECTOR DIV OF TRW INC	8821 SCIENCE CENTER DRIVE	MINNEAPOLIS MN 55428-3619
14552	MICROSEMI CORP	2830 S FAIRVIEW ST	SANTA ANA CA 92704-5948
14752	ELECTRO CUBE INC	1710 S DEL MAR AVE	SAN GABRIEL CA 91776-3825
14936	GENERAL INSTRUMENT CORP DISCRETE SEMI CONDUCTOR DIV	600 W JOHN ST	HICKSVILLE NY 11802
15454	KETEMA RODAN DIVISION	2900 BLUE STAR STREET	ANAHEIM CA 92806-2591
18324	SIGNETICS CORP MILITARY PRODUCTS DIV	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
18796	MURATA ERIE NORTH AMERICAN INC STATE COLLEGE OPERATIONS	1900 W COLLEGE AVE	STATE COLLEGE PA 16801-2723
19396	ILLINOIS TOOL WORKS INC PAKTRON DIV	1205 MCCONVILLE RD PO BOX 4539	LYNCHBURG VA 24502-4535
19613	MINNESOTA MINING AND MFG CO TEXTOOL PRODUCTS DEPT ELECTRONIC PRODUCT DIV	1410 E PIONEER DR	IRVING TX 75061-7847
19701	PHILIPS COMPONENTS DISCRETE PRODUCTS DIV RESISTIVE PRODUCTS FACILITY AIRPORT ROAD	PO BOX 760	MINERAL WELLS TX 76067-0760
20462	PREM MAGNETICS INC	3519 N CHAPEL HILL	MCHENRY IL 60050-2504
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT ELECTRONICS DEPT	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24165	SPRAGUE ELECTRIC CO	267 LOWELL ROAD	HUDSON NH 03051
24355	ANALOG DEVICES INC	RT 1 INDUSTRIAL PK PO BOX 9106	NORWOOD MA 02062
24546	BRADFORD ELECTRONICS	550 HIGH ST	BRADFORD PA 16701-3737
25403	PHILIPS COMPONENTS DISCRETE PRODUCTS DIV DISCRETE SEMICONDUCTOR GROUP	GEORGE WASHINGTON HWY	SMITHFIELD RI 02917
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
31433	KEMET ELECTRONICS CORP NATIONAL SALES HEADQUARTERS	PO BOX 5928	GREENVILLE SC 29606
31918	ITT SCHADOW INC	8081 WALLACE RD	EDEN PRAIRIE MN 55344-2224
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086-4518
34371	HARRIS CORP HARRIS SEMICONDUCTOR PRODUCTS GROUP	200 PALM BAY BLVD PO BOX 883	MELBOURNE FL 32919
34649	INTEL CORP SALES OFFICE /ST4-2/	3065 BOWERS AVE	SANTA CLARA CA 95051

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4T165	NEC ELECTRONICS USA INC ELECTRON DIV	401 ELLIS ST PO BOX 7241	MOUNTAIN VIEW CA 94039
50088	SGS-THOMSON MICROELECTRONICS INC	1310 ELECTRONICS DR	CARROLLTON TX 75006-6905
50157	MIDWEST COMPONENTS PRODUCT GROUP DIVISION OF THERM-O-DISC INC	1981 PORT CITY BLVD P O BOX 787	MUSKEGON MI 49443
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
51406	MURATA ERIE NORTH AMERICA INC HEADQUARTERS AND GEORGIA OPERATIONS	2200 LAKE PARK DR	SMYRNA GA 30080
52763	STETCO INC	3344 SCHIERHORN	FRANKLIN PARK IL 60131
52769	SPRAGUE-GOODMAN ELECTRONICS INC	134 FULTON AVE	GARDEN CITY PARK NY 11040-5352
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
54583	TDK ELECTRONICS CORP	12 HARBOR PARK DR	PORT WASHINGTON NY 11550
54937	DEYOUNG MANUFACTURING INC	12920 NE 125TH WAY	KIRKLAND WA 98034-7716
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195-4526
56845	DALE ELECTRONICS INC	2300 RIVERSIDE BLVD PO BOX 74	NORFOLK NE 68701-2242
57668	ROHM CORP	8 WHATNEY PO BOX 19515	IRVINE CA 92713
58361	QUALITY TECHNOLOGIES CORP	3400 HILLVIEW AVE	PALO ALTO CA 94304-1319
59610	SOURIAU INC	28309 N AVE CROCKER	VALENCIA CA 91355-1245
59640	SUPERTEX INC	1225 BORDER BY DESCER	SUNNYVALE CA 94086
59660	TUSONIX INC	7741 N BUSINESS PARK DR PO BOX 37144	TUCSON AZ 85740-7144
60386	SQUIRE ELECTRONICS INC	503 N 13TH AVE	CORNELIUS OR 97113-9303
61429	FOX ELECTRONICS FOX ENTERPRISES INC	PO BOX 1078	CAPE CORAL FL 33910-1078
61638	ADVANCED INTERCONNECTION CORP	5 DIVISION ST	WARWICK RI 02818-3842
61772	INTEGRATED DEVICE TECHNOLOGY	3236 SCOTT BLVD	SANTA CLARA CA 95051
61857	SAN-0 INDUSTRIAL CORP	85 ORVILLE DR PO BOX 511	BOHEMIA LONG ISLAND NY 11716-2501
64537	KDI ELECTRONICS INC SUBSIDIARY OF KDI CORP	31 FARINELLA DR	EAST HANOVER NJ 07936
65786	CYPRESS SEMICONDUCTOR CORP	3901 N 1ST ST	SAN JOSE CA 95134-1506
66302	VLSI TECHNOLOGY INC	1109 MCKAY DR	SAN JOSE CA 95131-1706
66891	BKC INTERNATIONAL ELECTRONIC INC	6 LAKE ST PO BOX 1436	LAWRENCE MA 01841-3011
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
71590	CRL COMPONENTS INC	HWY 20 W PO BOX 858	FORT DODGE IA 50501

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75498	MULTICOMP INC	3005 SW 154TH TERRACE #3	BEAVERTON OR 97006
76854	OAK/GRIGSBY AN OAK INDUSTRIES INC CO	88 N DUGAN ROAD PO BOX 890	SUGAR GROVE IL 60544-0890
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
81073	GRAYHILL INC	561 HILLGROVE AVE PO BOX 10373	LA GRANGE IL 60525-5914
81541	AIRPAX CORP CAMBRIDGE DIV A NORTH AMERICAN PHILIPS CO	WOODS RD PO BOX 520	CAMBRIDGE MD 21613
84411	AMERICAN SHIZUKI CORP OGALLALA OPERATIONS	301 WEST O ST	OGALLALA NE 69153-1844
91637	DALE ELECTRONICS INC	2064 12TH AVE PO BOX 609	COLUMBUS NE 68601-3632

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	671-0789-00	B010100	B011334	CIRCUIT BD ASSY:MAIN	80009	671078900
A1	671-0789-01	B011335	B014572	CIRCUIT BD ASSY:MAIN	80009	671078901
A1	671-0789-02	B014573		CIRCUIT BD ASSY:MAIN	80009	671078902
A1A7	671-1539-00	B011335		CIRCUIT BD ASSY:5 VOLT RECTIFIER	80009	671153900
A1A8	671-0849-00			CIRCUIT BD ASSY:BANDWIDTH LIMIT	80009	671084900
A1A9	671-0849-00			CIRCUIT BD ASSY:BANDWIDTH LIMIT	80009	671084900
A1A18	671-1235-00	B010100	B010345	CIRCUIT BD ASSY:THERMAL SHUTDOWN	80009	671123500
A1A18	671-1235-01	B010346		CIRCUIT BD ASSY:THERMAL SHUTDOWN	80009	671123501
A2	670-8699-01			CIRCUIT BD ASSY:ATTENUATOR	80009	670869901
A3	671-0787-00	B010100	B017836	CIRCUIT BD ASSY:FRONT PANEL	80009	671078700
A3	671-0787-01	B017837		CIRCUIT BD ASSY:FRONT PANEL	80009	671078701
A4	671-0790-00			CIRCUIT BD ASSY:TIMING	80009	671079000
A5	671-0791-00			CIRCUIT BD ASSY:ALT SWEEP	80009	671079100
A6	670-7615-01			CIRCUIT BD ASSY:EMI FILTER	80009	670761501
A10	671-0796-01	B010100	B010149	CIRCUIT BD ASSY:STORAGE	80009	671079601
A10	671-0796-02	B010150	B014634	CIRCUIT BD ASSY:STORAGE	80009	671079602
A10	671-0796-03	B014635		CIRCUIT BD ASSY:STORAGE	80009	671079603
A13	671-0792-00			CIRCUIT BD ASSY:SWEEP INTERFACE	80009	671079200
A14	670-8698-00			CIRCUIT BD ASSY:LOGIC CH1 & CH2	80009	670869800
A15	670-8698-00			CIRCUIT BD ASSY:LOGIC CH1 & CH2	80009	670869800
A16	671-0793-00			CIRCUIT BD ASSY:SWEEP REFERENCE	80009	671079300
A20	670-8898-02			CIRCUIT BD ASSY:XY PLOTTER	80009	670889802
A21	671-1227-00			CIRCUIT BD ASSY:RS232 (OPTION 12 ONLY)	80009	671122700
A22	671-0972-00			CIRCUIT BD ASSY:GPIB (OPTION 10 ONLY)	80009	671097200
A31	671-0795-00	B010100	B011334	CIRCUIT BD ASSY:SCALE ILLUM	80009	671079500
A31	671-1463-00	B011335		CIRCUIT BD ASSY:SCALE ILLUM	80009	671146300

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	671-0789-00	B010100	B011334	CIRCUIT BD ASSY:MAIN	80009	671078900
A1	671-0789-01	B011335	B014572	CIRCUIT BD ASSY:MAIN	80009	671078901
A1	671-0789-02	B014573		CIRCUIT BD ASSY:MAIN	80009	671078902
A1C100	283-0853-00			CAP,FXD,CER DI:2.2PF,200V	04222	SR212A2R2DAATR
A1C114	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100VMI	TK1743	CGB103KEX
A1C115	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100VMI	TK1743	CGB103KEX
A1C116	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C125	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	SA101C472KAA
A1C126	281-0820-00			CAP,FXD,CER DI:680 PF,10%,50V	04222	SA101C681KAA
A1C130	283-0159-00			CAP,FXD,CER DI:18PF,5%,50V	04222	SR155A180JAA
A1C133	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	TK1743	CGB101KEN
A1C150	283-0853-00			CAP,FXD,CER DI:2.2PF,200V	04222	SR212A2R2DAATR
A1C164	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C165	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C175	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	SA101C472KAA
A1C176	281-0820-00			CAP,FXD,CER DI:680 PF,10%,50V	04222	SA101C681KAA
A1C180	281-0140-00			CAP,VAR,CER DI:5-25PF,100V	59660	518-038A-5-25
A1C200	290-0136-00			CAP,FXD,ELCTLT:2.2UF,20%,20V	12954	D2R2EA20M1
A1C201	290-0136-00			CAP,FXD,ELCTLT:2.2UF,20%,20V	12954	D2R2EA20M1
A1C202	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	SA102A100KAA
A1C210	283-0853-00	B010100	B012646	CAP,FXD,CER DI:2.2PF,200V	04222	SR212A2R2DAATR
A1C210	281-0893-00	B012647		CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V,MI	04222	SA102A4R7DAA
A1C215	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C220	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C225	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V,MI	04222	SA101A100MAA
A1C226	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C228	281-0809-00			CAP,FXD,CER DI:200 PF,5%,100V	04222	SA101A201JAA
A1C229	281-0809-00			CAP,FXD,CER DI:200 PF,5%,100V	04222	SA101A201JAA
A1C237	281-0140-00			CAP,VAR,CER DI:5-25PF,100V	59660	518-038A-5-25
A1C239	281-0776-00			CAP,FXD,CER DI:120PF,5%,100V	04222	SA102A121JAA
A1C240	281-0511-00			CAP,FXD,CER DI:22PF,+/-2.2PF,500V	52763	2RDPZZ007 22POK
A1C241	281-0777-00			CAP,FXD,CER DI:51PF,5%,100V	04222	SA101A510JAA
A1C242	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	SA101C102KAA
A1C250	281-0768-00			CAP,FXD,CER DI:470PF,20%,100V	04222	SA101A471KAA
A1C251	281-0768-00			CAP,FXD,CER DI:470PF,20%,100V	04222	SA101A471KAA
A1C255	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C262	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C274	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C281	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C282	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	SA102C331MAA

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A1C292	290-0776-01			CAP,FXD,ELCTLT:22UF,20%,10WVDC	55680	UVX1A220MAA1TD
A1C312	281-0893-00			CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V,MI	04222	SA102A4R7DAA
A1C337	281-0893-00			CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V,MI	04222	SA102A4R7DAA
A1C350	281-0898-00			CAP,FXD,CER DI:7.5PF,+/-0.5PF,500V,MI	04222	MA107A7R5DAA
A1C351	281-0756-00			CAP,FXD,CER DI:2.2PF,+/-0.5PF,200V,MI	04222	SA102A2R2DAA
A1C369	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,MI	04222	SA101C102MAA
A1C381	283-0663-00			CAP,FXD,MICA DI:16.8PF,+/0.5PF,500V	TK0891	RDM15CD16R8D03
A1C389	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C390	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C392	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C396	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A1C397	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C400	283-0094-00			CAP,FXD,CER DI:27PF,10%,200V	59660	835-583-C0G0-27
A1C402	283-0051-00	B010100	B015627	CAP,FXD,CER DI:0.0033UF,5%,100V	04222	SR301A332JAA
A1C402	283-0100-00	B015628		CAP,FXD,CER DI:0.0047UF,10%,200V	04222	SR302A472KAA
A1C414	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C415	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C418	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C419	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	SA101A181JAA
A1C420	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100VMI	TK1743	CGB103KEX
A1C421	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C440	283-0665-00			CAP,FXD,MICA DI:190PF,1%,100V	TK0891	RDM15FD191F03
A1C453	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C454	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C455	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C459	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C460	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	TK1743	CGB222KEX
A1C467	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	TK1743	CGB222KEX
A1C469	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	TK1743	CGB222KEX
A1C473	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C480	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	SA101C472KAA
A1C487	281-0785-00			CAP,FXD,CER DI:68PF,10%,100V	04222	SA101A680KAA
A1C494	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100VMI	TK1743	CGB103KEX
A1C499	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C500	281-0903-00			CAP,FXD,CER DI:3.9PF,100V	04222	SA101A3R9DAA
A1C501	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C502	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C503	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C504	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C505	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	12954	AT513A105K035N

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A1C506	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	SA101C472KAA
A1C507	290-1086-00			CAP,FXD,ELCTLT:22UF,+/-20%,16V	55680	TVX1C220MAA1LS
A1C518	281-0852-00			CAP,FXD,CER DI:1800PF,10%,100VDC	04222	SA101C182KAA
A1C519	290-0814-00	B010100	B011028	CAP,FXD,ELCTLT:0.33MF,10%,20V	31433	T322A334K035AS
A1C519	285-1348-00	B011029		CAP,FXD,MTLZD:0.22UF,10%,63V	TK1913	MKS2 0.22 MFD 1
A1C520	290-0301-00	B010100	B012658	CAP,FXD,ELCTLT:10UF,10%,20V	12954	ST513B106K020N0
A1C520	290-0415-00	B012659		CAP,FXD,ELCTLT:5.6UF,10%,35V	12954	ST513B565K035
A1C521	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C525	281-0895-00			CAP,FXD,CER DI:6.8PF,100VDC	04222	SA101A6R8DAA
A1C527	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	SA101A220KAA
A1C528	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	SA101A220KAA
A1C531	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C537	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C538	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C539	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C540	290-0776-01			CAP,FXD,ELCTLT:22UF,20%,10WVDC	55680	UVX1A220MAA1TD
A1C544	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C545	285-1345-00			CAP,FXD,PLASTIC:2200PF,100V,5%	TK1913	2200 PF 5 PERCE
A1C547	281-0788-00			CAP,FXD,CER DI:470PF,10%,100V	04222	SA102C471KAA
A1C553	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C556	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C558	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C560	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C561	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C562	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C563	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C565	281-0768-00			CAP,FXD,CER DI:470PF,20%,100V	04222	SA101A471KAA
A1C566	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C590	290-0136-00			CAP,FXD,ELCTLT:2.2UF,20%,20V	12954	D2R2EA20M1
A1C603	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C635	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	TK1743	CGB222KEX
A1C646	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C647	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C648	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C649	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C764	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C770	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C775	281-0214-00			CAP,VAR,CER DI:0.6-3PF,400V	52763	313613-140
A1C777	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A1C779	285-1101-00			CAP,FXD,PLASTIC:0.022UF,10%,200V	19396	223K02PT485

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A1C780	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C782	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C785	281-0214-00			CAP,VAR,CER DI:0.6-3PF,400V	52763	313613-140
A1C787	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A1C789	285-1101-00			CAP,FXD,PLASTIC:0.022UF,10%,200V	19396	223K02PT485
A1C796	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C797	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C799	285-1341-01			CAP,FXD,MTLZD:0.1UF,20%,100VDC	TK1913	MKS 2 0.1UF 20%
A1C824	281-0785-00			CAP,FXD,CER DI:68PF,10%,100V	04222	SA101A680KAA
A1C825	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	SA102C331MAA
A1C828	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C832	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C835	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C845	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	SA106E222MAA
A1C847	285-1341-01			CAP,FXD,MTLZD:0.1UF,20%,100VDC	TK1913	MKS 2 0.1UF 20%
A1C849	285-1341-01			CAP,FXD,MTLZD:0.1UF,20%,100VDC	TK1913	MKS 2 0.1UF 20%
A1C851	285-1341-01			CAP,FXD,MTLZD:0.1UF,20%,100VDC	TK1913	MKS 2 0.1UF 20%
A1C853	281-0791-00			CAP,FXD,CER DI:270PF,10%,100V	04222	SA102C271KAA
A1C854	283-0279-00			CAP,FXD,CER DI:0.001UF,20%,3000V	18796	DHR12Y5S102M3KV
A1C855	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	84411	TEK266 .01 20 3
A1C871	285-1341-01			CAP,FXD,MTLZD:0.1UF,20%,100VDC	TK1913	MKS 2 0.1UF 20%
A1C873	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C875	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C877	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C882	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100VMI	TK1743	CGB103KEX
A1C893	283-0279-00			CAP,FXD,CER DI:0.001UF,20%,3000V	18796	DHR12Y5S102M3KV
A1C904	285-1222-00			CAP,FXD,PLASTIC:0.068UF,20%,250V	TK0515	PME 271 M 568
A1C906	290-1206-00			CAP,FXD,ELCTLT:270UF,20%,450V	1W344	SMG450VR271M35X
A1C907	285-1177-01			CAP,FXD,PLASTIC:1UF,10%,450V	84411	TEK326 1.0 10 4
A1C908	283-0481-00			CAP,FXD,CER DI:220PF,10%,250VAC	18796	DE7090B221KVA1-
A1C917	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	SA101C102KAA
A1C919	281-0852-00			CAP,FXD,CER DI:1800PF,10%,100VDC	04222	SA101C182KAA
A1C922	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C925	290-0973-00			CAP,FXD,ELCTLT:100UF,20%,25VDC	0J9R5	CEUSM1E101
A1C940	290-0922-00			CAP,FXD,ELCTLT:1000UF,20%,50V	1W344	SM50VB102Q16X31
A1C941	285-1341-01			CAP,FXD,MTLZD:0.1UF,20%,100VDC	TK1913	MKS 2 0.1UF 20%
A1C942	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-20%,100WVDC	0J9R5	CEBSM2D100M
A1C943	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-20%,100WVDC	0J9R5	CEBSM2D100M
A1C944	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	12954	AT513A105K035N
A1C945	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA

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A1C951	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,,TUBULAR,MI	TK1743	CGB103KEX
A1C952	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C954	290-0947-00			CAP,FXD,ELCTLT:33UF,+50-10%,160V W/SLEEVE ALUMINUM	0J9R5	CEUSM2C330-Q
A1C956	290-0946-00			CAP,FXD,ELCTLT:270UF,+100-10%,40V	0J9R5	CEUFM1G271
A1C958	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C959	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C960	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C961	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C962	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C963	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C964	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C965	290-0989-00			CAP,FXD,ELCTLT:4700UF,20%,10V	1W344	KMC10VB472M16X3
A1C968	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C970	290-1129-00			CAP,FXD,ELCTLT:1000UF,+100%-10%,12V	24165	672D108H012DS2A
A1C975	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	84411	TEK266 .01 20 3
A1C976	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	84411	TEK266 .01 20 3
A1C979	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	84411	TEK266 .01 20 3
A1C6121	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C6122	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C6123	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C6131	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V,MI	04222	SA101C102MAA
A1C7101	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C7201	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C7203	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C7204	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	SA102A100KAA
A1C7260	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C7320	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C7361	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1C7362	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	SA105E104MAA
A1C7431	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V,MI	TK1743	CGB103KEX
A1CR133	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR183	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR200	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR201	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR202	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR203	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR226	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR227	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR228	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427

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A1CR229	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR372	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR381	152-0245-00			SEMICOND DVC,DI:SW,SI,40V,D0-7	12954	MT7250
A1CR393	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR399	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR414	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR415	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR467	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR476	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR477	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR501	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR504	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR505	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR508	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR509	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR514	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR527	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR531	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR532	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR541	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR551	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR556	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR590	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR712	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR764	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR765	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR768	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR770	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR780	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR805	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR818	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR820	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR823	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR824	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR825	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR829	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR840	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR845	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR851	152-0400-00	B010100	B010195	DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR851	152-0413-00	B010196	B017174	DIODE,RECT:,;400V,1.0A,750NS	14936	RGP10G-022

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1CR851	152-0400-00	B017175		DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR853	152-0400-00	B010100	B010195	DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR853	152-0413-00	B010196	B017174	DIODE,RECT:,;400V,1.0A,750NS	14936	RGP10G-022
A1CR853	152-0400-00	B017175		DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR854	152-0400-00	B010100	B010195	DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR854	152-0413-00	B010196	B017174	DIODE,RECT:,;400V,1.0A,750NS	14936	RGP10G-022
A1CR854	152-0400-00	B017175		DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR855	152-0400-00	B010100	B010195	DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR855	152-0413-00	B010196	B017174	DIODE,RECT:,;400V,1.0A,750NS	14936	RGP10G-022
A1CR855	152-0400-00	B017175		DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR901	152-0750-00			DIODE,RECT:,FAST RCVRY;BRIDGE,600V,3A,IFSM = 125A,250NS	TK2319	RKBPC606
A1CR907	152-1165-00			DIODE,RECT:,ULTRA FAST;600V,4A,50NS	04713	MUR460RL
A1CR908	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR920	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR946	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR947	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR948	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR954	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR955	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR956	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR957	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR960	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR961	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR962	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR963	152-0400-00			DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR965	152-0400-00	B010100	B014572	DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR967	152-0400-00	B010100	B014572	DIODE,RECT:,FAST RCVRY;400V,1A,200NS	14552	MB2501
A1CR980	152-0582-00			DIODE,RECT:SCHTKY,;20V,3A,.475VF,80A IFSM	04713	1N5820
A1CR981	152-0582-00			DIODE,RECT:SCHTKY,;20V,3A,.475VF,80A IFSM	04713	1N5820
A1CR7201	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7202	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7203	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7301	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7302	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7303	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7304	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7305	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7306	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7307	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427
A1CR7308	152-0141-02			DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF	27014	FDH9427

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1CR7470	152-0075-00	B011029	B012730	SEMICOND DVC,DI:SW,GE,22V,80MW,DO-7	66891	G866
A1CR7470	152-1107-00	B012731		DIODE,SIG:SCHTKY,;40V,350MA,12PF	50088	BAT48
A1CR7471	152-0075-00	B011029	B012730	SEMICOND DVC,DI:SW,GE,22V,80MW,DO-7	66891	G866
A1CR7471	152-1107-00	B012731		DIODE,SIG:SCHTKY,;40V,350MA,12PF	50088	BAT48
A1DS856	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A1DS858	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A1DS870	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A1E200	276-0752-00			CORE,EM:FERRITE TELEQ	TK1442	BP53-BH3.5X10X4
A1E201	276-0752-00			CORE,EM:FERRITE TELEQ	TK1442	BP53-BH3.5X10X4
A1E272	276-0752-00			CORE,EM:FERRITE TELEQ	TK1442	BP53-BH3.5X10X4
A1E590	276-0752-00			CORE,EM:FERRITE TELEQ	TK1442	BP53-BH3.5X10X4
A1E907	276-0635-00			CORE,EM:TOROID,FERRITE	02114	768 T188/3E2A
A1E964	276-0752-00			CORE,EM:FERRITE TELEQ	TK1442	BP53-BH3.5X10X4
A1E966	276-0752-00			CORE,EM:FERRITE TELEQ	TK1442	BP53-BH3.5X10X4
A1J266	131-0787-00			TERMINAL,PIN:PCB/PRESSFIT,;MALE,STR,0.025 SQ,0.448 MLG X 0.137 TAIL,0.600 L,PHOS BRZ, 50 GOLD	22526	47359-000
A1J267	131-0787-00			TERMINAL,PIN:PCB/PRESSFIT,;MALE,STR,0.025 SQ,0.448 MLG X 0.137 TAIL,0.600 L,PHOS BRZ, 50 GOLD	22526	47359-000
A1J4210	131-0589-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE (QUANTITY OF 4)	22526	48283-029
A1J6113	131-0589-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE (QUANTITY OF 4)	22526	48283-029
A1J6121	131-0608-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.248 MLG X 0.137 TAIL,50 GOLD,PHZ BRZ,W/ FERRULE (QUANTITY OF 16)	22526	48283-036
A1J6123	131-4534-00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.318 MLG X 0.110 L 0.031 DIA TAIL,30 GOLD,BD RETENTION FOR 0.035 DIA HOLE	53387	2403-6232TB
A1J6411	131-0589-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE (QUANTITY OF 4)	22526	48283-029
A1J6412	131-4420-00			CONN,HDR:PCB,;MALE,STR,2 X 7,0.1 CTR,0.235 MLG X 0.110 TAIL,30 GOLD,BD RETENTION	53387	2414-6142TB
A1J9001	131-4421-00	B010100	B014572	CONN,HDR:PCB,;MALE,STR,2 X 10,0.1 CTR,0.235	53387	2420-6142TB
A1J9001	131-3360-01	B014573		CONN,HDR:PCB,;MALE,STR,2 X 10,0.1 CTR,0.365 D BD RETENTION	TK1899	2520-60K2UB
A1J9002	131-4421-00	B010100	B014572	CONN,HDR:PCB,;MALE,STR,2 X 10,0.1 CTR,0.235	53387	2420-6142TB

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A1J9002	131-3360-01	B014573		CONN,HDR:PCB,;MALE,STR,2 X 10,0.1 CTR,0.365 D BD RETENTION	TK1899	2520-60K2UB
A1J9003	131-4421-00	B010100	B014572	CONN,HDR:PCB,;MALE,STR,2 X 10,0.1 CTR,0.235	53387	2420-6142TB
A1J9003	131-5242-00	B014573		CONN,HDR:PCB,;MALE,STR,2 X 8,0.1 CTR,0.365H X 0.112 TAIL,SHRD/4 SIDES,CTR PLZ,BD RETENTION	53387	2516-60K2 W/BRD
A1J9010	131-4418-00	B010100	B016585	CONN,HDR PWR:PCB,;MALE,STR,1 X 8,0.156 CTR, 0.450 MLG X 0.125 TAIL	53387	CLY-1008-001A10
A1J9010	131-4418-01	B016586		CONN,HDR PWR:PCB,;MALE,STR,1 X 8,0.156 CTR, 0.450 MLG X 0.125 TAIL	19613	CLK-1008-L01A10
A1J9210	131-4419-00	B010100	B014572	CONN,HDR:PCB,;MALE,STR,2 X 5,0.1 CTR,0.235 MLG X 0.110 TAIL,30 GOLD,BD RETENTION	53387	2410-6142UB
A1J9210	131-3520-01	B014573		CONN,HDR:PCB,;MALE,STR,2 X 5,0.1 CTR,0.365H X 0.112 TAIL,SHRD/4 SIDES,CTR PLZ,30 GOLD, BD RETENTION	TK1899	2510-60K2UB
A1J9300	131-0608-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.248 MLG X 0.137 TAIL,50 GOLD,PHZ BRZ,W/ FERRULE (QUANTITY OF 5)	22526	48283-036
A1J9320	131-0589-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE (QUANTITY OF 4)	22526	48283-029
A1J9400	131-3177-00	B012647		CONN,BOX::PCB,;FEMALE,STR,1 X 9,0.15 CTR, 0.30 H X 0.125 TAIL,TIN,TOP ENTRY	00779	5-3809509
A1J9644	131-0608-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.248 MLG X 0.137 TAIL,50 GOLD,PHZ BRZ,W/ FERRULE (QUANTITY OF 3)	22526	48283-036
A1J9705	131-0589-00			TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE (QUANTITY OF 8)	22526	48283-029
A1J9870	131-0589-00	B014573		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE	22526	48283-029
A1J9882	131-0787-00			TERMINAL,PIN:PCB/PRESSFIT,;MALE,STR,0.025 SQ,0.448 MLG X 0.137 TAIL,0.600 L,PHOS BRZ,50 GOLD (QUANTITY OF 2)	22526	47359-000
A1J9965	131-0589-00	B011430		TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR,0.025 SQ,0.343 MLG X 0.122 TAIL,0.465 L,50 GOLD,W/ FERRULE (QUANTITY OF 2)	22526	48283-029
A1L142	108-0420-00			COIL,RF:FIXED,35NH,15%	0JR03	108-0420-00
A1L143	108-0420-00			COIL,RF:FIXED,35NH,15%	0JR03	108-0420-00
A1L192	108-0420-00			COIL,RF:FIXED,35NH,15%	0JR03	108-0420-00
A1L193	108-0420-00			COIL,RF:FIXED,35NH,15%	0JR03	108-0420-00
A1L266	108-1488-00	B012647		COIL,RF:FXD,1UH,10%	09969	IR-2

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A1L267	108-1488-00	B012647		COIL,RF:FXD,1UH,10%	09969	IR-2
A1L960	108-1319-00			INDUCTOR,FIXED:33UH,10%,1.8A	54583	TSL1110-330K 1R
A1L961	108-1319-00			INDUCTOR,FIXED:33UH,10%,1.8A	54583	TSL1110-330K 1R
A1L962	108-1319-00			INDUCTOR,FIXED:33UH,10%,1.8A	54583	TSL1110-330K 1R
A1L968	108-0554-00	B010100	B012093	COIL,RF:FIXED,5UH,+/-20%	0JR03	108-0554-00
A1L968	108-0554-01	B012094		COIL,RF:FIXED,5UH,+/-205,W/HEAT SHRINK	0JR03	108-0554-01 TEK
A1Q102	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q103	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q114	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q115	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q152	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q153	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q164	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q165	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q202	151-0212-00			TRANSISTOR,SIG:BIPOLAR,NPN;15V,50MA,1.0GHZ AMPLIFIER	04713	BFY90
A1Q203	151-0212-00			TRANSISTOR,SIG:BIPOLAR,NPN;15V,50MA,1.0GHZ AMPLIFIER	04713	BFY90
A1Q206	151-0369-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,30MA,2.0GHZ, AMPLIFIER	04713	MPSH69
A1Q207	151-0369-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,30MA,2.0GHZ, AMPLIFIER	04713	MPSH69
A1Q230	151-0271-00			TRANSISTOR,SIG:BIPOLAR,PNP;15V,30MA,2.0GHZ, AMPLIFIER	04713	MPSH69
A1Q231	151-0271-00			TRANSISTOR,SIG:BIPOLAR,PNP;15V,30MA,2.0GHZ, AMPLIFIER	04713	MPSH69
A1Q254	151-0752-01			TRANSISTOR,SIG:BIPOLAR,NPN;15V,75MA,4.0GHZ, AMPLIFIER,MOTOROLA ONLY	04713	SRF3188
A1Q255	151-0752-01			TRANSISTOR,SIG:BIPOLAR,NPN;15V,75MA,4.0GHZ, AMPLIFIER,MOTOROLA ONLY	04713	SRF3188
A1Q256	151-0752-00			TRANSISTOR,SIG:BIPOLAR,NPN;15V,75MA,4.0GHZ, AMPLIFIER,PHILIPS ONLY	25403	BFR96
A1Q257	151-0752-00			TRANSISTOR,SIG:BIPOLAR,NPN;15V,75MA,4.0GHZ, AMPLIFIER,PHILIPS ONLY	25403	BFR96
A1Q282	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q283	151-0736-00			TRANSISTOR:NPN,SI,TO-92	0JR04	2N4401

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1Q284	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q285	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q302	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q303	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q327	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q328	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q382	151-1042-00			TRANSISTOR,SIG:JFET,N-CH;6V,10-15MA,4.5MS, IDSS(1-2) < 0.5MA,AMPLIFIER (LOCATIONS A & B)	04713	SPF627M2
A1Q384	151-0711-00			TRANSISTOR,SIG:BIPOLAR,NPN;25V,50MA,650MHZ AMPLIFIER	04713	MPSH10
A1Q397	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q401	151-1103-00			TRANSISTOR,SIG:DMOS,N-CH;ENH,30V,50MA,45 OHM	TK2150	SD210DE
A1Q402	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q413	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q419	151-0711-00			TRANSISTOR,SIG:BIPOLAR,NPN;25V,50MA,650MHZ AMPLIFIER	04713	MPSH10
A1Q420	151-0711-00			TRANSISTOR,SIG:BIPOLAR,NPN;25V,50MA,650MHZ AMPLIFIER	04713	MPSH10
A1Q421	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q422	151-0199-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA, SWITCHING	04713	MPS3640
A1Q423	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q428	151-0711-00			TRANSISTOR,SIG:BIPOLAR,NPN;25V,50MA,650MHZ AMPLIFIER	04713	MPSH10
A1Q429	151-0712-00			TRANSISTOR,SIG:BIPOLAR,PNP;20V,50MA,600MHZ AMPLIFIER	04713	MPSH81
A1Q473	151-0276-01			TRANSISTOR,SIG:BIPOLAR,PNP;50V,50MA,40MHZ, AMPLIFIER	04713	2N5087RLRP
A1Q474	151-0276-01			TRANSISTOR,SIG:BIPOLAR,PNP;50V,50MA,40MHZ, AMPLIFIER	04713	2N5087RLRP
A1Q487	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q509	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q511	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q521	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1Q522	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q523	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q524	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q525	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q527	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q541	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q542	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q543	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q544	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q576	151-0199-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA, SWITCHING	04713	MPS3640
A1Q578	151-0199-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA, SWITCHING	04713	MPS3640
A1Q583	151-0198-00			TRANSISTOR,SIG:BIPOLAR,NPN;15V,50MA, 600MHZ,AMPLIFIER	04713	MPS918
A1Q586	151-0198-00			TRANSISTOR,SIG:BIPOLAR,NPN;15V,50MA, 600MHZ,AMPLIFIER	04713	MPS918
A1Q756	151-0432-00			TRANSISTOR:BIPOLAR,NPN;80V,500MA,150MHZ, AMPLIFIER	04713	MPS8099
A1Q770	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q775	151-0347-00			TRANSISTOR,SIG:BIPOLAR,NPN;160V,600MA, 100MHZ,AMPLIFIER	0JR04	2N5551
A1Q779	151-0350-00			TRANSISTOR,SIG:BIPOLAR,PNP;150V,600MA, 100MHZ,AMPLIFIER	0JR04	TO BE ASSIGNED
A1Q780	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q785	151-0347-00			TRANSISTOR,SIG:BIPOLAR,NPN;160V,600MA, 100MHZ,AMPLIFIER	0JR04	2N5551
A1Q789	151-0350-00			TRANSISTOR,SIG:BIPOLAR,PNP;150V,600MA, 100MHZ,AMPLIFIER	0JR04	TO BE ASSIGNED
A1Q804	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q814	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q825	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	MPS2369A
A1Q829	151-0199-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA, SWITCHING	04713	MPS3640

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1Q835	151-0199-00			TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA, SWITCHING	04713	MPS3640
A1Q840	151-0347-00			TRANSISTOR,SIG:BIPOLAR,NPN;160V,600MA, 100MHZ,AMPLIFIER	0JR04	2N5551
A1Q845	151-0350-00			TRANSISTOR,SIG:BIPOLAR,PNP;150V,600MA, 100MHZ,AMPLIFIER	0JR04	TO BE ASSIGNED
A1Q882	151-0405-00			TRANSISTOR:DARLINGTON,NPN,SI,TO-126MJE800 60V,4A,POWER	F3223	MJE800
A1Q908	151-0164-00			TRANSISTOR,SIG:BIPOLAR,PNP;60V,600MA, 200MHZ,AMPLIFIER	04713	MPS2907A
A1Q928	151-0432-00			TRANSISTOR:BIPOLAR,NPN;80V,500MA,150MHZ, AMPLIFIER	04713	MPS8099
A1Q930	151-0164-00			TRANSISTOR,SIG:BIPOLAR,PNP;60V,600MA, 200MHZ,AMPLIFIER	04713	MPS2907A
A1Q935	151-0565-00			THYRISTOR,SCR:8A,200V,SENS GATE,TO-220 W/LEADFORM	04713	SCR2117
A1Q938	151-0276-01			TRANSISTOR,SIG:BIPOLAR,PNP;50V,50MA,40MHZ, AMPLIFIER	04713	2N5087RLRP
A1Q939	151-0276-01			TRANSISTOR,SIG:BIPOLAR,PNP;50V,50MA,40MHZ, AMPLIFIER	04713	2N5087RLRP
A1Q944	151-0311-01			TRANSISTOR,PWR:BIPOLAR,NPN;300V,500MA, SWITCHING	04713	MJE340
A1Q7201	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q7202	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q7203	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q7204	151-0188-00			TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA, 250MHZ,AMPLIFIER	04713	2N3906
A1Q7362	151-0711-00			TRANSISTOR,SIG:BIPOLAR,NPN;25V,50MA,650MHZ AMPLIFIER	04713	MPSH10
A1Q7420	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q7440	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q7470	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q7471	151-0190-00			TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1Q7472	151-0190-00	B010100	B011029	TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA, 300MHZ,AMPLIFIER	04713	2N3904
A1R100	313-1430-00			RES,FXD,FILM:43 OHM,5%,0.2W	91637	CCF50-2-43R00J
A1R101	313-1430-00			RES,FXD,FILM:43 OHM,5%,0.2W	91637	CCF50-2-43R00J
A1R102	322-3155-00			RES,FXD,FILM:402 OHM,1%,0.2W,TC=T0MI	91637	CCF501G402ROF
A1R103	322-3155-00			RES,FXD,FILM:402 OHM,1%,0.2W,TC=T0MI	91637	CCF501G402ROF

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Component Number	Tektronix Part No.	Serial No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R104	322-3101-00			RES,FXD,FILM:110 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G110R0F
A1R105	322-3101-00			RES,FXD,FILM:110 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G110R0F
A1R106	322-3161-00			RES,FXD,FILM:464 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G464R0F
A1R108	322-3223-00			RES,FXD,FILM:2.05K OHM,1%,0.2W,TC=T0MI	91637	CCF501G20500F
A1R109	322-3221-00			RES,FXD,FILM:1.96K OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F19600F
A1R114	322-3225-00			RES,FXD,FILM:2.15K OHM,1%,0.2W,TC=T0	91637	CCF501G21500F
A1R115	322-3225-00			RES,FXD,FILM:2.15K OHM,1%,0.2W,TC=T0	91637	CCF501G21500F
A1R116	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R118	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R120	322-3123-00			RES,FXD,FILM:187 OHM,1%,0.2W,TC=T0MI	91637	CCF501G187R0F
A1R121	322-3123-00			RES,FXD,FILM:187 OHM,1%,0.2W,TC=T0MI	91637	CCF501G187R0F
A1R122	322-3085-00			RES,FXD,FILM:75 OHM,1%,0.2W,TC=T0	91637	CCF501G75R00F
A1R125	322-3177-00			RES,FXD,FILM:681 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G681R0F
A1R126	322-3177-00			RES,FXD,FILM:681 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G681R0F
A1R130	322-3068-00			RES,FXD,FILM:49.9 OHM,1%,0.2W,TC=T0MI	91637	CCF501G49R90F
A1R131	322-3068-00			RES,FXD,FILM:49.9 OHM,1%,0.2W,TC=T0MI	91637	CCF501G49R90F
A1R132	322-3165-00			RES,FXD,FILM:511 OHM,1%,0.2W,TC=T0MI	91637	CCF501G511R0F
A1R133	322-3101-00			RES,FXD,FILM:110 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G110R0F
A1R135	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R136	322-3126-00			RES,FXD,FILM:200 OHM,1%,0.2W,TC=T0MI	91637	CCF501G200ROF
A1R138	322-3218-00			RES,FXD,FILM:1.82K OHM,1%,0.2W,TC=T0MI	91637	CCF501G18200F
A1R139	322-3239-00			RES,FXD,FILM:3.01K OHM,1%,0.2W,TC=T0MI	91637	CCF501G30100F
A1R142	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R143	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R144	322-3162-00			RES,FXD,FILM:475 OHM,1%,0.2W,TC=T0MI	91637	CCF50G475R0F
A1R145	311-1238-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3386X-DY6-502
A1R150	313-1430-00			RES,FXD,FILM:43 OHM,5%,0.2W	91637	CCF50-2-43R00J
A1R151	313-1430-00			RES,FXD,FILM:43 OHM,5%,0.2W	91637	CCF50-2-43R00J
A1R152	322-3155-00			RES,FXD,FILM:402 OHM,1%,0.2W,TC=T0MI	91637	CCF501G402ROF
A1R153	322-3155-00			RES,FXD,FILM:402 OHM,1%,0.2W,TC=T0MI	91637	CCF501G402ROF
A1R154	322-3101-00			RES,FXD,FILM:110 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G110R0F
A1R155	322-3101-00			RES,FXD,FILM:110 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G110R0F
A1R156	322-3161-00			RES,FXD,FILM:464 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G464R0F
A1R158	322-3223-00			RES,FXD,FILM:2.05K OHM,1%,0.2W,TC=T0MI	91637	CCF501G20500F
A1R159	322-3221-00			RES,FXD,FILM:1.96K OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F19600F
A1R164	322-3225-00			RES,FXD,FILM:2.15K OHM,1%,0.2W,TC=T0	91637	CCF501G21500F
A1R165	322-3225-00			RES,FXD,FILM:2.15K OHM,1%,0.2W,TC=T0	91637	CCF501G21500F
A1R166	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R168	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R170	322-3123-00			RES,FXD,FILM:187 OHM,1%,0.2W,TC=T0MI	91637	CCF501G187R0F

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A1R171	322-3123-00			RES,FXD,FILM:187 OHM,1%,0.2W,TC=T0MI	91637	CCF501G187R0F
A1R172	322-3085-00			RES,FXD,FILM:75 OHM,1%,0.2W,TC=T0	91637	CCF501G75R00F
A1R175	322-3177-00			RES,FXD,FILM:681 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G681R0F
A1R176	322-3177-00			RES,FXD,FILM:681 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G681R0F
A1R180	322-3068-00			RES,FXD,FILM:49.9 OHM,1%,0.2W,TC=T0MI	91637	CCF501G49R90F
A1R181	322-3068-00			RES,FXD,FILM:49.9 OHM,1%,0.2W,TC=T0MI	91637	CCF501G49R90F
A1R182	322-3165-00			RES,FXD,FILM:511 OHM,1%,0.2W,TC=T0MI	91637	CCF501G511R0F
A1R183	322-3101-00			RES,FXD,FILM:110 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G110R0F
A1R185	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R186	322-3126-00			RES,FXD,FILM:200 OHM,1%,0.2W,TC=T0MI	91637	CCF501G200ROF
A1R188	322-3218-00			RES,FXD,FILM:1.82K OHM,1%,0.2W,TC=T0MI	91637	CCF501G18200F
A1R189	322-3239-00			RES,FXD,FILM:3.01K OHM,1%,0.2W,TC=T0MI	91637	CCF501G30100F
A1R192	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R193	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R194	322-3162-00			RES,FXD,FILM:475 OHM,1%,0.2W,TC=T0MI	91637	CCF50G475R0F
A1R195	311-1238-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3386X-DY6-502
A1R200	322-3147-00			RES,FXD,FILM:332 OHM,1%,0.2W,TC=T0MI	91637	CCF501G332R0F
A1R202	322-3178-00			RES,FXD,FILM:698 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G698ROF
A1R203	322-3178-00			RES,FXD,FILM:698 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G698ROF
A1R204	322-3089-00			RES,FXD,FILM:82.5 OHM,1%.0.2W,TC=T0MI	57668	CRB20 FXE 82E5
A1R206	322-3139-00			RES,FXD,FILM:274 OHM,1%,0.2W,TC=T0MI	91637	CCF501G274ROF
A1R207	322-3139-00			RES,FXD,FILM:274 OHM,1%,0.2W,TC=T0MI	91637	CCF501G274ROF
A1R210	322-3130-00	B010100	B012646	RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R210	322-3147-00	B012647		RES,FXD,FILM:332 OHM,1%,0.2W,TC=T0MI	91637	CCF501G332R0F
A1R212	322-3086-00			RES,FXD,FILM:76.8 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G76R80F
A1R213	322-3086-00			RES,FXD,FILM:76.8 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G76R80F
A1R215	322-3135-00			RES,FXD,FILM:249 OHM,1%,0.2W,TC=T0MI	91637	CCF501G249R0F
A1R216	322-3163-00			RES,FXD,FILM:487 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G487R0F
A1R217	322-3163-00			RES,FXD,FILM:487 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G487R0F
A1R218	322-3102-00			RES,FXD,FILM:113 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F113R0F
A1R219	322-3102-00			RES,FXD,FILM:113 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F113R0F
A1R220	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A1R222	322-3289-00			RES,FXD,FILM:10K OHM,1%,0.2W,TC=T0	91637	CCF50G10001F
A1R223	322-3289-00			RES,FXD,FILM:10K OHM,1%,0.2W,TC=T0	91637	CCF50G10001F
A1R225	322-3261-00			RES,FXD,FILM:5.11K OHM,1%,0.2W,TC=T0MI	91637	CCF50G5111FT
A1R226	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R227	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R230	322-3086-00			RES,FXD,FILM:76.8 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G76R80F
A1R231	322-3086-00			RES,FXD,FILM:76.8 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G76R80F
A1R233	322-3086-00			RES,FXD,FILM:76.8 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G76R80F

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R234	322-3054-00			RES,FXD,FILM:35.7 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F35R70F
A1R235	322-3054-00			RES,FXD,FILM:35.7 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F35R70F
A1R236	322-3185-00			RES,FXD,FILM:825 OHM,1%,0.2W,TC=T0MI	91637	CCF501G825ROF
A1R239	322-3228-00			RES,FXD,FILM:2.32K OHM,1%,0.2W,TC=T0MI	91637	CCF50-1G2320F
A1R240	311-1248-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3386X-1-501
A1R241	311-1237-00			RES,VAR,NONWW:1K OHM,10%,0.50W	32997	3386X-DY6-102
A1R242	313-1273-00			RES,FXD,FILM:27K OHM,5%,0.2W	91637	CCF50-2-27001J
A1R244	322-3172-00			RES,FXD,FILM:604 OHM,1%,0.2W,TC=T0MI	91637	CCF501G604ROF
A1R245	322-3172-00			RES,FXD,FILM:604 OHM,1%,0.2W,TC=T0MI	91637	CCF501G604ROF
A1R250	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R251	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R254	322-3110-00			RES,FXD,FILM:137 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G137R0F
A1R255	322-3110-00			RES,FXD,FILM:137 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G137R0F
A1R256	322-0175-00			RES,FXD,FILM:649 OHM,1%,0.25W,TC=T0	91637	CMF6042G649R0F
A1R257	322-0175-00			RES,FXD,FILM:649 OHM,1%,0.25W,TC=T0	91637	CMF6042G649R0F
A1R258	322-0180-00			RES,FXD,FILM:732 OHM,1%,0.25W,TC=T0	91637	CMF6042G732R0F
A1R259	322-0180-00			RES,FXD,FILM:732 OHM,1%,0.25W,TC=T0	91637	CMF6042G732R0F
A1R261	323-0058-00			RES,FXD,FILM:39.2 OHM,1%,0.5W,TC=T0	91637	CMF65 116G39R20
A1R262	322-3114-00			RES,FXD,FILM:150 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2-G1500F
A1R266	307-1502-01	B010100	B012646	NTWK,HYBRID CKT:VERTICAL OUTPUT	80009	307150201
A1R266	307-1502-02	B012647		NTWK,HYBRID CKT:VERTICAL OUTPUT	TK2015	FGA-0129-00
A1R278	322-3265-00			RES,FXD,FILM:5.62K OHM,1%,0.2W,TC=T0MI	91637	CCF501G56200F
A1R279	322-3322-00	B010100	B012129	RES,FXD,FILM:22.1K OHM,1%,0.2W,TC=T0MI	91637	CCF501G22101F
A1R279	322-3261-00	B012130		RES,FXD,FILM:5.11K OHM,1%,0.2W,TC=T0MI	91637	CCF50G5111FT
A1R281	322-3185-00			RES,FXD,FILM:825 OHM,1%,0.2W,TC=T0MI	91637	CCF501G825ROF
A1R282	322-3277-00			RES,FXD,FILM:7.5K OHM,1%,0.2W,TC=T0	91637	CCF501G75000F
A1R283	322-3162-00			RES,FXD,FILM:475 OHM,1%,0.2W,TC=T0MI	91637	CCF50G475R0F
A1R284	322-3173-00			RES,FXD,FILM:619 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F619R0F
A1R285	322-3169-00			RES,FXD,FILM:562 OHM,1%,0.2W,TC=T0MI	91637	CCF50-2F562R0F
A1R286	322-3068-00			RES,FXD,FILM:49.9 OHM,1%,0.2W,TC=T0MI	91637	CCF501G49R90F
A1R287	322-3068-00			RES,FXD,FILM:49.9 OHM,1%,0.2W,TC=T0MI	91637	CCF501G49R90F
A1R288	322-3158-00			RES,FXD,FILM:432 OHM,1%,0.2W,TC=T0MI	57668	CRB2D FXE 432
A1R289	322-3158-00			RES,FXD,FILM:432 OHM,1%,0.2W,TC=T0MI	57668	CRB2D FXE 432
A1R292	322-3179-00			RES,FXD,FILM:715 OHM,1%,0.2W,TC=T0MI	91637	CCF501G715R0F
A1R293	313-1620-00			RES,FXD,FILM:62 OHM,5%,0.2W	91637	CCF50-2-G62ROJ
A1R301	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R302	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R303	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R304	322-3210-00			RES,FXD,FILM:1.5K OHM,1%,0.2W,TC=T0	91637	CCF501G15000F
A1R305	322-3210-00			RES,FXD,FILM:1.5K OHM,1%,0.2W,TC=T0	91637	CCF501G15000F

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Component Number	Tektronix Part No.	Serial No. Effective	Serial No. Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R306	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R307	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R309	311-2230-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.50W LINEAR	TK2073	GF06UT2 501 M L
A1R310	322-3194-00			RES,FXD,FILM:1.02K OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G10200F
A1R311	322-3194-00			RES,FXD,FILM:1.02K OHM,1%,0.2W,TC=T0MI	91637	CCF50-2G10200F
A1R312	322-3098-00			RES,FXD,FILM:102 OHM,1%,0.2W,TC=T0MI	91637	CCF501G102ROF
A1R314	322-3170-00			RES,FXD,FILM:576 OHM,1%,0.2W,TC=T0	91637	CCF50G576R0F
A1R315	322-3170-00			RES,FXD,FILM:576 OHM,1%,0.2W,TC=T0	91637	CCF50G576R0F
A1R317	322-3218-00			RES,FXD,FILM:1.82K OHM,1%,0.2W,TC=T0MI	91637	CCF501G18200F
A1R318	322-3193-00			RES,FXD,FILM:1K OHM,1%,0.2W,TC=T0	91637	CCF501G10000F
A1R319	322-3212-00			RES,FXD,FILM:1.58K OHM,1%,0.2W,TC=T0MI	91637	CCF501G15800F
A1R321	322-3208-00			RES,FXD,FILM:1.43K OHM,1%,0.2W,TC=T0	91637	CCF501G14300F
A1R322	322-3238-00			RES,FXD,FILM:2.94K OHM,1%,0.2W,TC=T0	91637	CCF501G29400F
A1R324	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R326	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R327	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R328	322-3130-00			RES,FXD,FILM:221 OHM,1%,0.2W,TC=T0MI	57668	RB20FX221E
A1R329	322-3210-00			RES,FXD,FILM:1.5K OHM,1%,0.2W,TC=T0	91637	CCF501G15000F
A1R330	322-3210-00			RES,FXD,FILM:1.5K OHM,1%,0.2W,TC=T0	91637	CCF501G15000F
A1R331	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R332	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R335	322-3203-00			RES,FXD,FILM:1.27K OHM,1%,0.2W,TC=T0MI	91637	CCF501G12700F
A1R336	322-3203-00			RES,FXD,FILM:1.27K OHM,1%,0.2W,TC=T0MI	91637	CCF501G12700F
A1R337	322-3098-00			RES,FXD,FILM:102 OHM,1%,0.2W,TC=T0MI	91637	CCF501G102ROF
A1R339	322-3170-00			RES,FXD,FILM:576 OHM,1%,0.2W,TC=T0	91637	CCF50G576R0F
A1R340	322-3170-00			RES,FXD,FILM:576 OHM,1%,0.2W,TC=T0	91637	CCF50G576R0F
A1R342	322-3218-00			RES,FXD,FILM:1.82K OHM,1%,0.2W,TC=T0MI	91637	CCF501G18200F
A1R343	322-3193-00			RES,FXD,FILM:1K OHM,1%,0.2W,TC=T0	91637	CCF501G10000F
A1R344	322-3212-00			RES,FXD,FILM:1.58K OHM,1%,0.2W,TC=T0MI	91637	CCF501G15800F
A1R346	322-3208-00			RES,FXD,FILM:1.43K OHM,1%,0.2W,TC=T0	91637	CCF501G14300F
A1R347	322-3238-00			RES,FXD,FILM:2.94K OHM,1%,0.2W,TC=T0	91637	CCF501G29400F
A1R349	322-3097-00			RES,FXD,FILM:100 OHM,1%,0.2W,TC=T0MI	91637	CCF501G100R0F
A1R350	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R351	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R352	321-0274-00			RES,FXD,FILM:6.98K OHM,1%,0.125W,TC=T0MI	91637	CMF55116G69800F
A1R353	321-0274-00			RES,FXD,FILM:6.98K OHM,1%,0.125W,TC=T0MI	91637	CMF55116G69800F
A1R354	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R355	313-1470-00			RES,FXD,FILM:47 OHM,5%,0.2W	91637	CCF50-2-47R00J
A1R356	322-3269-00			RES,FXD,FILM:6.19K OHM,1%,0.2W,TC=T0MI	91637	CCF501G61900F
A1R357	322-3149-00			RES,FXD,FILM:348 OHM,1%,0.2W,TC=T0MI	91637	CCF501G348ROF

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