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User Manual

Tektronix

73A-270
Arbitrary Pulse/Pattern Generator Module

070-9148-03

This document supports firmware version 1.00 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

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EC Declaration of Conformity

We

Tektronix Holland N.V.
Marktweg 73A
8444 AB Heerenveen
The Netherlands

declare under sole responsibility that the

73A-270

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

To ensure compliance with EMC requirements this module must be installed in a mainframe which has backplane shields installed which comply with Rule B.7.45 of the VXIbus Specification. Only high quality shielded cables having a reliable, continuous outer shield (braid & foil) which has low impedance connections to shielded connector housings at both ends should be connected to this product.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Avoid Electric Overload

To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

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Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:



DANGER
High Voltage



Protective Ground
(Earth) Terminal



ATTENTION
Refer to Manual



Double
Insulated

Certifications and Compliances

Overvoltage Category

Overvoltage categories are defined as follows:

CAT III: Distribution level mains, fixed installation

CAT II: Local level mains, appliances, portable equipment

CAT I: Signal level, special equipment or parts of equipment, telecommunication, electronics

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73A-270 ARBITRARY PULSE/PATTERN GENERATOR

DESCRIPTION

INTRODUCTION

The 73A-270 Arbitrary Pulse/Pattern Generator (APPG) Module is a printed circuit board assembly for use in a card cage conforming to the VXIbus Specification, such as the 73A-021 used in the CDS 73A IAC System. The module provides two completely independent output channels with a common VXIbus backplane interface. Each channel can be individually programmed to generate an arbitrary string of active and inactive TTL or bipolar analog (±17.4V) pulse or pattern outputs.

Each channel contains a 1600-word by six-decimal digit high-speed memory. This memory is used to store up to 1600 6-digit output duration time values. Since the APPG allows programming of 1600 duration values (not just 1600 1's and 0's), very complex pulse trains may be programmed. After initial programming, these duration values may be updated "in-progress" (while the APPG is transmitting).

The APPG's ability to output short pulses repeatedly, or short pulses delayed by long intervals, make it ideal for triggering other VXIbus instruments, using either front panel connectors or the VXIbus backplane TTLTRG bus for signal routing. And in applications requiring synchronous operation between multiple VXIbus mainframes, multiple APPG modules may be driven by a single APPG, or all modules can be driven by a single external clock source.

The six-digit data loaded into each memory location represents the duration time of the output (the length of time the output will remain active or inactive) for that point in the data list. A separate two-digit decimal counter is provided for each channel to allow transmission of the data list from 1 to 63 times.

Each location in memory can be identified as an active or inactive output. Any location in the memory can be identified as the last address to provide a variable length data list. Any number of locations in the memory can be identified as breakpoints for pausing and then continuing transmission.

Like other CDS products, the APPG Module combines ease of use and flexibility of function in its programmable features. These features include:

- four output modes per channel - Retriggerable and Non-Retriggerable Modes, each with internal or external triggering.
- breakpoint capability - provided in all four modes at any location in the list.
- interrupts - can be programmed to generate an interrupt to the VXIbus backplane when transmission is complete or at breakpoints.
- four time resolutions (ranges) - 100 nsec, 1 µsec, 10 µsec, or 100 µsec.
- initial polarity of transmission - may be programmed so that a transition from the inactive state will occur either immediately on triggering or

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after one or more durations of output.

- repeat count - can be programmed to repeat from 1 to 63 times or indefinitely.

- capability to drive any of the eight VXIbus TTLTRG backplane lines.

- external triggering - external trigger source may be selected under program control to be any of the eight VXIbus TTLTRG lines.

- bipolar analog output - programmable over the full ±17.4V output range for both the active and inactive states.

The card is programmed with simple ASCII character strings consisting of numerical data combined with single letter commands. The 73A-270 supports the VXI fast handshake mode and handles all characters on a Direct Memory Access (DMA) basis. VXIbus handshake time is less than 500 nanoseconds per character.

Front panel BNC connectors are provided for TTL Pulse/Pattern Outputs, Analog Bipolar Pulse/Pattern Outputs, and External Trigger Inputs. A 25 pin DB25S connector on the front panel provides duplicates of the above BNC signals plus additional Input/Output signals for an external clock input, a buffered internal clock, and a transmission in progress signal. See Appendix B for a complete description of these signals.

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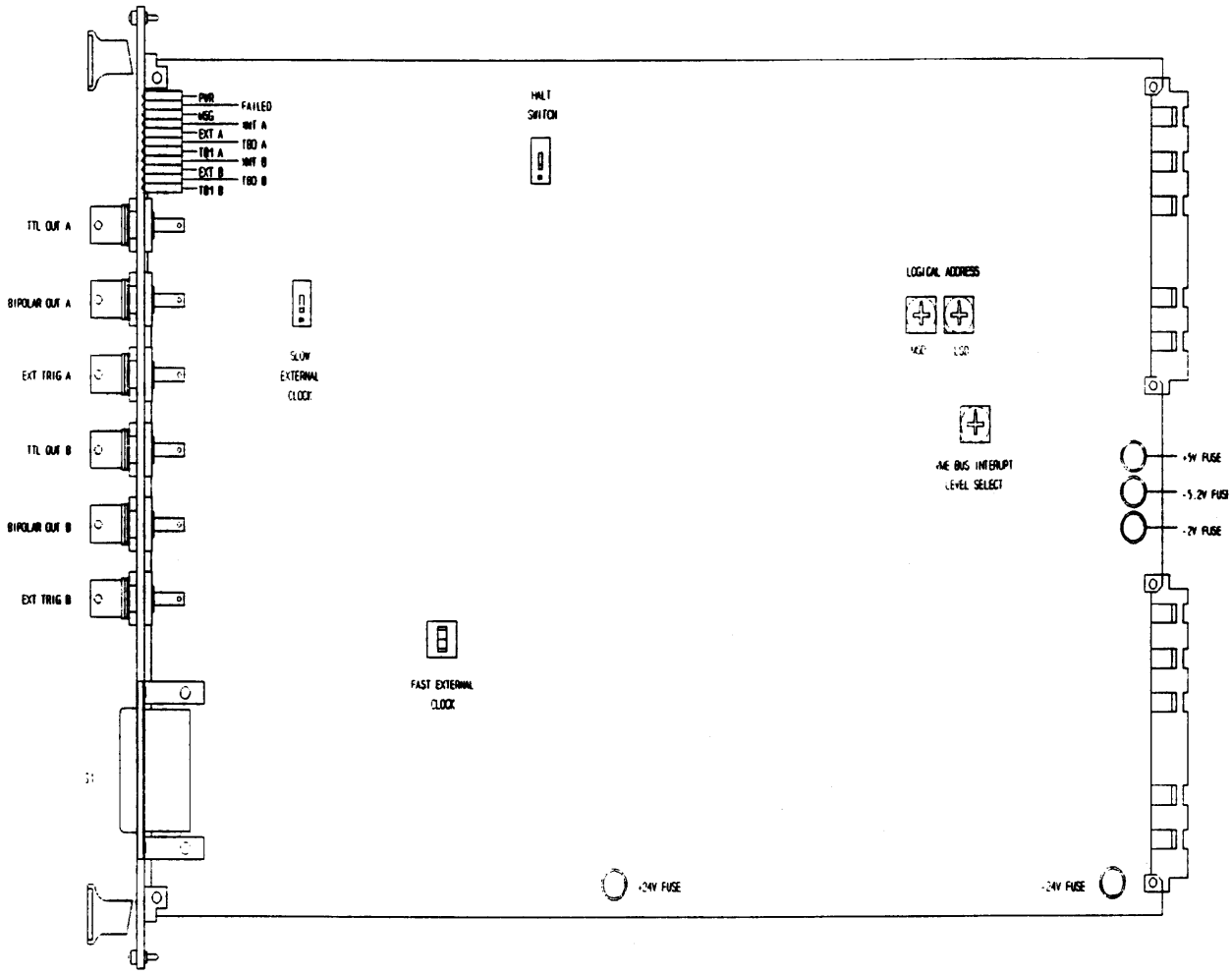


Figure 270-1: 73A-270 Controls and Indicators

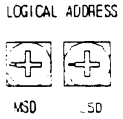
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CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 73A-270 Module's operating environment. See Figure 270-1 for their physical locations.

- **Switches**

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the 73A-270 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

The actual physical address of the 73A-270 Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the 73A-270 will be [(64d * XYh) + 49152d]. For example:

L.A.	M S D	L S D	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the 73A-270 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the 73A-270 is being used in a CDS IEEE-488 IAC system, consult the operating manual of the CDS 73A-151 RM/488 Interface Module.

If the 73A-270 is not being used in a CDS IAC System, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the logical address.

VMEbus Interrupt Level Select Switch



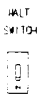
Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander (for example, the 73A-151 RM/IEEE-488 Interface Module in a CDS 73A-IBX System). The VMEbus interrupt level on which the 73A-270 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the 73A-270's interrupt handler, typically the module's commander. Setting the switch to an invalid interrupt level (0, 8, or 9) will disable the module's interrupts. When using the 73A-270 in a CDS 73A-IBX System, set the interrupt level to the same level chosen on the 73A-151.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

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Halt Switch



This two-position slide switch selects the response of the 73A-270 Module when the Reset bit in the module's VXIbus Control register is set.

If the Halt Switch is in the ON position, the 73A-270 Module is reset to its power-up state and all programmed module parameters are reset to their default values.

If the Halt Switch is in the OFF position, the module will ignore the Reset bit and no action will take place.

NOTE: The module is not in strict compliance with the VXIbus Specification when the Halt switch is OFF.

Control of the Reset bit depends on the capabilities of the 73A-270's commander. In a CDS 73A-IBX System, for example, the Reset bit is set if the 73A-151 RM/IEEE-488 Interface Module receives a STOP command via the IEEE-488 bus.

External Clock Switches

The 73A-270 has two External Clock switches. Depending on the clock source and/or frequency of the external clock, either the Fast External Clock or the Slow External Clock switch must be activated.

The Fast External Clock switch is a two-position rocker switch. Switch to position C2 if an external clock with a frequency of greater than 250 KHz (up to 10 MHz) is being supplied.

Switch to position C1 if the internal clock is to be used, or if an external clock with a frequency of less than 250 KHz is to be used.

NOTE: If a frequency of less than 10 MHz is supplied, VXIbus backplane handshake times for the 73A-270 will be lengthened to greater than 500 nanoseconds.

The Slow External Clock Switch is a two-position slide switch. The switch should be placed in the ON position if an external clock with a frequency of less than 250 KHz is to be used.

NOTE: For slow external clock operation, the external clock is internally synchronized to the internal 10 MHz clock. Phase jitter of up to ±50 nsec will be introduced. Slow external clock operation does not delay the 500 nanosecond VXIbus backplane handshake times.

The Fast External Clock switch instead of the Slow External Clock switch may be used for slow external clocks if throughput is not critical and elimination of phase jitter is required.

- **Fuses**

The 73A-270 Module has +5V, -5.2V, -2V, and ±24V removable fuses. The fuses protect the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

If any fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

If any fuse opens, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section of this manual.

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- **LEDs**

The following LEDs are visible at the top of the 73A-270 Module's front panel to indicate the status of the module's operation:

Power LED

This green LED is normally lit and is extinguished if the +5V, -5.2V, -2V, or ±24V buses or the internally regulated ±20.9V buses fail, or if the -2V, +5V, -5.2V, or ±24V fuses open.

Failed LED

This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failure consists of loss of a power voltage.

NOTE: If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's Power LED is extinguished.

MSG LED

This green LED is normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

Mode/Resolution LEDs

Four LEDs are provided for each of the two channels (Channel A and Channel B). The eight LEDs are arranged in the following order at the top front of the module. When lit, the LEDs indicate the following:

XMTA Channel A is transmitting.

EXTA Channel A external trigger is enabled.

TB0A Channel A resolution - least significant bit.

TB1A Channel A resolution - most significant bit.

XMTB Channel B is transmitting.

EXTB Channel B external trigger is enabled.

TB0B Channel B resolution - least significant bit.

TB1B Channel B resolution - most significant bit.

The TB0 and TB1 resolution LEDs are encoded as follows:

TB1 LED	TB0 LED	Resolution
OFF	OFF	100 nanosecond
OFF	ON	1 microsecond
ON	OFF	10 microsecond
ON	ON	100 microsecond

BITE (Built-In Test Equipment)

Four LEDs for each channel provide visual indication of the transmit status, resolution status, and external trigger mode. A readback mode provides the transmit status and data list command accept status of either channel. Finally, the serial pattern output connections to the VXIbus TTLTRG lines allow checking the programming and output intervals by any counter resource in the same VXIbus card cage.

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GLOSSARY

A glossary of VXIbus terms is provided in Appendix C. In addition, the following terms specific to the 73A-270 Module are defined:

Bipolar Outputs
: An output for each channel that provides the same pulse/pattern output as the basic pulse/pattern TTL output but at a programmable high and low level up to ±17.4V for both the active and inactive states.

Breakpoint
: A programmed breakpoint temporarily holds the output at the last programmed level until a trigger instructs the module to continue.

Non-Retriggerable Mode
: A programmed mode on the 73A-270 that ignores additional triggers while a channel is actually transmitting until transmission is completed or a breakpoint is executed.

Repeat Count
: A programmable count on the 73A-270 Module that allows the pulse/pattern output (up to 1600 locations) to be repeated a specified number of times up to 63 times, or continuously.

Retriggerable Mode
: A programmed mode on the 73A-270 that allows the pulse/pattern output to restart at the beginning of its transmission list if a trigger is received while the module is actively transmitting.

Pulse/Pattern Outputs
: A series of active and inactive levels of varying programmable time durations provided on a single wire output. Two independent outputs are provided on the 73A-270 Module.

Time Duration Value
: One of 1600 values programmable on each channel with a value of 1 to 999,999. This value is multiplied by the resolution programmed for the channel to determine the time a particular output level (active or inactive) programmed in any one of the 1600 locations is present on the pulse/ pattern output.

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SPECIFICATIONS

Number of Channels: Two.

Type Outputs: TTL active high and active low; VXIbus TTLTRG; bipolar analog (each channel).

Bipolar Outputs: Programmable level - ±17.4 volts (±8.7 into 50 ohms).
Transition time - <70 nsec, 10% to 90% points, typical

TTL Outputs: Drive capability, 3.2 mA source, 24 mA sink current.

Number of Sequential Output Durations: 1 to 1600 per channel.

Number of Repeat Times: 1 to 63, or continuous.

Time Period of Each Output Duration: Programmable, 1 to 999,999 times the resolution range selected for each channel:

Resolution Range	Time Period Duration
100 ns	100 nanoseconds to 99.9999 milliseconds.
1 µs	1 microsecond to 0.999999 seconds.
10 µs	10 microseconds to 9.99999 seconds.
100 µs	100 microseconds to 99.9999 seconds.

Programmable Resolution of Each Output Duration:

Internal 10 MHz Clock:
Four programmable resolution ranges:
100-nanosecond, 1 µsec, 10 µsec, and 100 µsec resolution.

External Clock:
1/f, 10/f, 100/f, 1000/f
f= external clock input frequency.

Significant Digits (Time Period Programming): 6 decimal digits (20 bit resolution).

Trigger Modes:

Non-retriggerable Mode: Single trigger for total number of output cycles without interruption.

Retriggerable Mode: Each trigger restarts output from first output duration.

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Trigger Capability:

Programmable:	Trigger under program control or trigger with external trigger input from multiple sources.
Sources (programmable):	Internal: Software initiated. External: Front panel connector. Any of 8 VXIbus TTLTRG lines. VXIbus TRIGGER command.
External Trigger Input:	Input (Front Panel or VXIbus TTLTRG): Trigger occurs on TTL transition from high to low. Front Panel Loading: 1 TTL load equivalent with 10K pullup.
VXIbus TTLTRG Selection:	Programmable, TTLTRG 0 through 7, synchronous trigger protocol.
Trigger Delay:	From receipt of trigger to start of output: 315 ns - 0 ns + 100 ns for all resolution ranges.
Breakpoint Capability:	1 to 1600 programmable breakpoints for each channel. Available in either Retriggerable or Non-Retriggerable modes.
Programmed By:	ASCII characters.
On-Card Memory:	3200 24 bit words (1600 words/channel).
Clock Source:	Internal: VXIbus slot 0 10 MHz ECL clock. External: front panel connector.

External Clock Input:

Type Input:	TTL.
Range:	1 kHz to 10 MHz.
Loading:	1.25 TTL load equivalents.

External Clock Outputs:

Type:	TTL, 15 mA source, 64 mA sink current.
Frequency:	10 MHz.

TTL Outputs:

Channel A and B Pulse/ Pattern Outputs:	TTL active high and TTL active low.
Channel A and B Transmission In Progress Outputs:	TTL active high and TTL active low.

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Drive Capability:	TTL, 5 mA source, 32 mA sink current.
Pulse/Pattern Output Sense:	BNC output, TTL high when active; VXIBus TTLTRG output, TTL low when active; DB25S TTL active high output, TTL high when active; DB25S TTL active low output, TTL low when active.
Transmission In Progress Output Sense:	TTL active high output, TTL high for transmission in progress; TTL active low output, TTL low for transmission in progress.
Bipolar Analog Outputs:	Levels (50 ohm load): Inactive level - ±8.7V dc. Active level - ±8.7V dc. Levels (high impedance load): Inactive level - ±17.4V dc. Active level - ±17.4V dc. Minimum load: 50 ohms. Resolution: 100 mV with 50 ohm load; 200 mV with high impedance. DC accuracy: 3% of full scale range. 10-90% rise/fall time: less than 60 nanoseconds.
Power-Up Conditions:	When power is applied, the module will go to the following known states: Channel A: Selected. Resolution: 100 nanosecond, both channels. Mode: Retriggerable, both channels. External Trigger: Disabled, both channels. External Trigger Source: Front panel, both channels. VXIbus TTLTRG Pulse/Pattern output: not programmed. Interrupt Capability: Disabled, both channels. Pulse/Pattern Memory Contents: Undefined. Channel A & B Repeat Count: Undefined. LEDs: Extinguished, except for Power LED. Pulse/Pattern Outputs: Inactive. Transmission In Progress Outputs: Transmission not in progress. Bipolar Outputs: 0V dc for both Active and Inactive levels.
VXIbus Data Rate:	Data/Commands, 1.8 Mbytes per second, fast handshake mode. Throughput will be affected by system controller and system controller/VXIbus interface.
Handshake Types:	Normal Mode Word Serial transfer or Fast Handshake Word Serial mode.
Logical Address:	Switch selectable, 1 through 254.

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VXIbus Compatibility:	Fully compatible with the VXIbus Specification for message-based instruments with the Halt Switch in the ON position.
VXI Device Type:	VXI message based instrument, VXIbus Revision 1.2.
VXI Protocol:	Word serial.
VXI Card Size:	C size, one slot wide.
Module-Specific Commands:	All module-specific commands and data are sent via the VXIbus Byte Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.
VMEbus Interface:	Data transfer bus (DTB) slave - A16, D16 only.
Interrupt Level:	Switch selectable, levels 1 (highest priority) through 7 (lowest).
Interrupt Acknowledge:	D16, lower 8 bits returned are the logical address of the module. Upper 8 bits contain the VXIbus protocol event code.
VXIbus Fast Handshake:	Active for internal clock and for recommended external clock switch settings for external clock.
VXIbus Commands Supported:	All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command Event: BYTE AVAILABLE (with or without END bit set) BYTE REQUEST BEGIN NORMAL OPERATION CLEAR IDENTIFY COMMANDER READ PROTOCOL TRIGGER
VXIbus Protocol Events Supported:	VXIbus events are returned via VME interrupts. The following events are supported and returned to the 73A-270 Module's commander: UNRECOGNIZED VXIbus COMMAND REQUEST TRUE (In IEEE-488 systems such as the 73A-IBX, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)
VXIbus Registers:	ID Device Type

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	Status Control Protocol Response Data Low See Appendix A for definition of register contents.
Power Requirements:	All required dc power is provided by the Power Supply in the VXIbus card cage.
Voltage:	+5 Volt Supply: 4.75V dc to 5.25V dc. +24 Volt Supply: +23.2V dc to +25.2V dc. -24 Volt Supply: -23.2V dc to -25.2V dc. -5.2 Volt Supply: -4.95V dc to -5.45V dc -2.0 Volt Supply: -1.9V dc to -2.1V dc
Current (Peak Module, I_{PM}):	+5 volt supply: 3.3 A +24 volt supply: 120 mA * -24 volt supply: 100 mA * -5.2 volt supply: 35 mA -2.0 volt supply: 26 mA
Current (Dynamic Module, I_{DM}):	+5 volt supply: 150 mA ptp @ 23 MHz +24 volt supply: 185 mA ptp @ 23 MHz * -24 volt supply: 245 mA ptp @ 17 MHz * -5.2 volt supply: 435 mA ptp @ 23 MHz -2.0 volt supply: 435 mA ptp @ 22 MHz * +24V dc tested with ±7V dc 1 MHz bipolar output into 50 Ohms on both channels.
Cooling:	Provided by the fan in the VXIbus card cage. Less than 10°C temperature rise with 1.76 liters/sec of air at a pressure drop of 0.099 mm of H_2O.
Fuses:	Replacement fuses: +5V: Littlefuse P/N 273004, -5.2V, -2V: Littlefuse P/N 273002, ±24V: Littlefuse P/N 273001,
Temperature:	-10°C to +65°C, operating (assumes ambient temperature of 55° and airflow to assure less than 10°C temperature rise). -40°C to +85°C, storage.
Humidity:	Less than 95% R.H., noncondensing.
VXIbus Radiated Emissions:	Complies with VXIbus Specification.
VXIbus Conducted Emissions:	Complies with VXIbus Specification.

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Dimensions, Shipping:	When ordered with a CDS card cage, this module will be installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, the module's shipping dimensions are: 406 mm x 305 mm x 102 mm. (16 in x 12 in x 4 in).
Weight:	1.4 kg. (3.1 lbs).
Weight, Shipping:	When ordered with a CDS card cage, this module will be installed and secured in one of the instrument module slots (slots 1-12). When ordered alone, the shipping weight is: 1.9 kg. (4.3 lbs).
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus card cage. (Refer to D size card cage manual for information on required adapters.)
Front Panel Signal Connectors:	Six BNC jacks: Pulse/pattern outputs, TTL; Pulse/pattern outputs, bipolar; External trigger inputs. One DB-25S connector: Pulse/pattern outputs, TTL active high and active low; Pulse/pattern outputs, bipolar; External trigger inputs; Transmission in progress outputs, TTL active high and active low; External clock input and output.
Recommended Cable:	(for DB-25S connector) 73A-734 Data Cable or 73A-782P Hooded Connector.
Equipment Supplied:	1 - 73A-270 Arbitrary Pulse/Pattern Generator Module.

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INSTALLATION

INSTALLATION REQUIREMENTS AND CAUTIONS

The 73A-270 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus card cage slot other than slot 0. If the module is being installed in a D size card cage, consult the operating manual for the card cage to determine how to install the module in that particular card cage. Setting the module's logical address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the 73A-270 Module's logical address.

CAUTION:

To avoid confusion, it is recommended that the slot number and the logical address be the same.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

CAUTION:

Note that there are two ejector handles on the module. To avoid installing the module incorrectly, make sure the ejector labeled "73A-270" is at the top.

CAUTION:

In order to maintain proper card cage cooling, unused card cage slots must be covered with blank front panels supplied by the card cage manufacturer. Based on the number of IAC Modules ordered with a CDS card cage, blank front panels are supplied to cover all unused slots.

CAUTION:

Verify that the card cage is able to provide adequate cooling and power for the 73A-270 Module. Refer to the card cage Operating Manual for instructions on determining cooling and power compatibility.

CAUTION:

If the 73A-270 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the 73A-270 Module to operate properly. Check the manual of the card cage being used for jumpering instructions.

If a CDS 73A-021 Card Cage is being used, the jumper points may be reached through the front of the card cage. There are five (5) jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

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INSTALLATION PROCEDURE

CAUTION:

The 73A-270 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the module's Revision Level, Serial Number (located on the CDS label on the top shield of the 73A-270), and switch settings on the Installation Checklist on the next page. Only qualified personnel should install the 73A-270 Module.

2) Verify that the Logical Address and Interrupt Level switches are switched to the correct value. The Halt switch should be in the ON position unless it is desired to not allow the resource manager to reset this module.

   Note that with either Halt Switch position, a "hard" reset will occur at power-on and when SYSRST* is set true on the VXIbus backplane. If the module's commander is a CDS 73A-151 RM/IEEE-488 Interface Module, SYSRST* will be set true whenever the Reset Switch on the front panel of the 73A-151 is depressed. Also note that when the Halt Switch is in the OFF position, the module is not in strict compliance with the VXIbus Specification.

3) The module can now be inserted into any slot of the chassis other than slot 0.

   NOTE: This module does not connect to the VXIbus local bus, so no front panel keying is required.

4) **Cable Installation -**
   If the DB25S connections are to be used, use either a 73A-734 Data Cable or 73A-782P Hooded Connector to interface between the DB25S output connector and the UUT. If the module is being installed in a CDS 73A Series card cage, route the cable from the front panel of the module down through the cable tray at the bottom of the card cage and out the rear of the card cage.

No calibration is required for this module.

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INSTALLATION CHECKLIST

Installation parameters may vary depending on the card cage being used. Be sure to consult the card cage Operating Manual before installing and operating the 73A-270 Module.

Revision Level: _____

Serial No.: _____

Card Cage Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Halt Switch: _____

Fast External Clock: _____

Slow External Clock: _____

Cable Installed: _____

Performed by: _____ Date: _____

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OPERATION

OVERVIEW

The 73A-270 Module is programmed by ASCII characters issued from the system controller to the 73A-270 Module via the module's VXIbus commander and the VXIbus card cage backplane. The module is a VXIbus Message Based Instrument and communicates using VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the 73A-270 Module's commander for details on the operation of that device.

If the Module is being used in a CDS 73A-IBX System card cage, the module's commander will be the 73A-151 Resource Manager/IEEE-488 Interface Module. Refer to the 73A-151 Operating Manual and the programming examples at the end of this section for information on how the system controller communicates with the 73A-151.

The module consists of two completely separate arbitrary pulse pattern generators with a common VXIbus backplane interface. Each channel contains a 1600-word by six- decimal digit high-speed memory. This memory is used to store up to 1600 six-digit output duration time values.

The six-digit data loaded into each memory location represents the length of time the output will remain active or inactive for that point in the data list. A separate two-digit decimal counter is provided for each channel to allow transmission of the data list from 1 to 63 times. Separate circuitry is provided for each channel to allow channel-specific selection of resolution, start of transmission, retriggering modes, or interrupt enabling.

Very complex wave trains may be programmed. For example, up to 800 100-nsec pulses may be programmed with the intervals between each pulse varying from 100 nsec to 100 msec. Or, by programming 1500 consecutive 100-millisecond active levels followed by a 100-nsec inactive level, a 100-nsec pulse may be accurately delayed 150 seconds. In the higher resolution range a 100 µsec pulse may be delayed up to 150,000 seconds (41 hours).

Each location in memory can be identified as an active or inactive output. Any location in the memory can be identified as the last address in order to provide a variable length data list. Any number of locations in the memory can be identified as breakpoints for independent triggering of segments of memory.

Four eight-channel multiplexers allow connection of the channel A and B pulse/pattern output and external trigger input to any of the eight VXIbus TTLTRG lines.

There are two bipolar analog output amplifiers for each channel, providing a programmable active and inactive level for each channel.

- **Programming Sequence**

The typical programming sequence is:

- One of two channels is selected with an S (Select) command. All channel-specific commands apply to that channel until another channel is selected.

- An R (Resolution) command is used to specify one of four clock resolutions for the selected channel.

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- A decimal address in the 1600-word memory is selected with an A (Address) command.

- Memory data values consisting of a time duration value and polarity, a last location identifier, and breakpoint location identifiers are loaded into that address with an L (List) command.

  The selected address automatically increments after each L (List) command, or it may be reprogrammed at any time with the A command.

- The selected channel is programmed for the number of times the entire data list in memory is to be transmitted with the C (Count) command.

- The selected channel may also be programmed with the M (Mode) command to select or deselect the retriggerable or non-retriggerable modes with or without external trigger enabled, or to enable or disable the VXIbus interrupt capability with the I (Interrupt) command.

- Transmission is then initiated with the B (Begin) command.

- **Programmable Features**

Modes

Four output modes are provided for each channel. The first two, the Non-Retriggerable Modes with internal or external triggering, each transmit the string of active and inactive level outputs the specified number of times, ignoring additional triggers during transmission. The second two, the Retriggerable Modes with internal or external triggering, reset the module to the beginning of the transmit string if an additional trigger is received during transmission.

Breakpoint Capability

A breakpoint capability is provided in all four modes at any location in the list. Transmission stops following any level programmed with a breakpoint, and resumes when an additional trigger is received. The external trigger modes may be triggered by a TTL signal on each channel, either through the VXIbus TTLTRG lines, through a front panel BNC or DB25S connector, or by the VXIbus TRIGGER command.

Interrupts

The APPG Module can be programmed to generate an interrupt to the VXIbus backplane when transmission is complete or at breakpoints, to indicate the need for a trigger to continue transmission.

Time Duration Ranges

The 6-digit output time duration values for each channel may be programmed using:

- 100-nanosecond increments up to 100 milliseconds,
- 1 µsec increments up to 1 second,
- 10 µsec increments up to 10 seconds, or
- 100 µsec increments up to 100 seconds.

Other resolutions may be obtained by using an external clock, available through the front panel DB25S connector. The module uses the VXIbus slot 0 10 MHz ECL clock for its internal time base. In applications requiring synchronous operation between multiple VXIbus mainframes, multiple APPG modules may be driven by a single APPG, or all modules can be driven by a single external clock source.

Initial Polarity

The initial polarity of transmission (active or inactive level) may be programmed so that a transition from the inactive state will occur either immediately on triggering or after one or more durations of output. Both polarities of the output are available at the module's DB25S front connector so that

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either polarity may be defined as the inactive state. BNC connectors are provided on the front panel for TTL output and the bipolar analog output levels for each of the two channels.

Repeat Count
The complete output pulse train for each channel can be programmed to repeat from 1 to 63 times or indefinitely. The individual output durations (active or inactive, including the level duration presently transmitting) may be updated 'in-progress' (while the module is transmitting).

TTLTRG Capability
Each channel's output may be programmed to drive any of the eight VXIbus TTLTRG backplane lines. The 73A-270's ability to output short pulses repeated or delayed by extremely long intervals makes it useful for triggering other VXIbus instruments.

External Triggering
The external triggers for each channel may also be driven under program control by any of the eight VXIbus TTLTRG lines. By selecting the same TTLTRG line, one channel's pulse/pattern output may be used to externally trigger the other channel or other APPG modules.

Bipolar Analog Outputs
The bipolar analog output for both the active and inactive states is programmable over the full ± voltage output range. The outputs for each channel are 50 ohm sources capable of driving a 50 ohm load to ±8.7V dc with a 100 mV resolution or a high impedance load to ±17.4V dc with a 200 mV resolution.

- **Front Panel BNC Connectors**

TTL Pulse/Pattern Outputs
The TTL OUT A and TTL OUT B BNC connections provide the programmed active and inactive output pulse trains for each channel. The TTL-compatible outputs for each channel are at a TTL high when an active level is programmed.

Analog Bipolar Pulse/Pattern Outputs
The BPLR OUT A and BPLR OUT B BNC connections provide analog output signals. The signal level when the module is not transmitting, or transmitting at an inactive level, will be the voltage level programmed by the N command. The signal level when the module is transmitting and at an active level will be the voltage level programmed by the P command.

External Trigger Inputs
The EXT TRG A and EXT TRG B BNC connections are used to input front panel external triggers. When Channel A or B is programmed for an external trigger and the front panel external trigger has been selected by the X command, transmission will start three to four clock cycles (400 ns maximum using the internal clock) following a high-to-low transition of the channel's external trigger input. Internal 10K pull-up resistors pull each input high when not connected.

DB25S Signals
Additional signals provided at the 25 pin DB25S front panel connector are:

- external clock input - allows several modules to be programmed for parallel operation.
- buffered internal clock - allows any module to be the common clock source for a parallel module output configuration.
- transmission in progress - indicates whether transmission is in progress for each channel.

See Appendix B for a complete description of these signals.

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POWER-UP

The 73A-270 Module will be ready for programming as soon as the VXIbus Resource Manager has initialized the VXIbus system. The 73A-270 Power LED will be on, and all other LEDs off. The MSG LED will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the card cage. The default condition of the module after power-up is described in the SYSFAIL, Self Test and Initialization subsection.

SYSTEM COMMANDS

Although these non-data commands are initiated by the 73A-270's commander (for example, the 73A-151 Module in a CDS 73A-IBX System) rather than the system controller, they have an effect on the 73A-270 Module. The following VXIbus instrument protocol commands will affect the 73A-270:

Command	Effect
CLEAR	The module clears its VXIbus interface. The 73A-270 Module has no input or output command buffers, so input and output data transfers are unaffected. Current module functional operation is also unaffected.
TRIGGER	The module triggers operation if the external trigger mode is programmed and the VXIbus TRIGGER command has been programmed as the source for the external trigger.
BEGIN NORMAL OPERATION	The module will begin operations.

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READ PROTOCOL

The module will return its protocol to its commander.

MODULE COMMANDS

A summary of the 73A-270's Module's commands is listed below. This is followed by detailed descriptions of each of the commands. A sample BASIC program using these commands is shown at the end of this section.

Command protocol and syntax for the 73A-270 Module are as follows:

1) The format for each command is specified in the detailed command description section of this manual.

2) Commands may be strung together indefinitely.

3) Carriage-return <CR>, line feed <LF>, or other separation characters (such as slashes, periods, commas, colons or semi-colons) are permitted but not required between commands. Leaving out <CR><LF> will usually significantly reduce a system controller's execution time. However, adding a <CR><LF> following commands improves readability.

• Summary

An overview of the commands, in the order they typically would be programmed, is as follows:

S Select - selects the channel (A or B) for which all following commands (except the T and X commands) will apply.

R Resolution - specifies one of four time resolution ranges for the selected channel.

A Address - specifies any of the 1,600 addresses in the selected channel for loading data into memory.

L List - specifies the time duration and polarity (active or inactive) of the output at the selected address for the selected channel. It can also specify the selected address as a breakpoint or last address. The programmed address will increment automatically at the end of each LIST command.

C Count - specifies the number of times the entire data list will be transmitted before stopping for the selected channel.

M Mode - specifies either the Triggerable or the Non-retriggerable Mode for the selected channel. It also enables or disables the external triggering for both modes.

T TTLTRG - specifies VXIbus TTLTRG0 through TTLTRG7 for connection to Channel A and B's pulse/pattern output, or specifies no connection.

X External Trigger - specifies the source for an external trigger for Channel A and B as: a) VXIbus TTLTRG0 through TTLTRG7, b) the VXIbus TRIGGER command, or

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c) the front panel BNC connector (or the equivalent DB25S connector pin).

N Inactive Analog - specifies the analog bipolar output voltage level for the selected channel corresponding to an inactive pulse/pattern signal output.

P Active Analog - specifies the analog bipolar output voltage level for the selected channel corresponding to an active pulse/pattern signal output.

Input Request

An Input Request to the 73A-270 returns status information for the selected channel. An input request is not a command output. It is generated by reading from the module.

I Interrupt - enables or disables interrupt capability for the selected channel.

B Begin - triggers data transmission for one or both channels. Transmission will begin immediately if external triggering is not active. If external triggering is active for a channel, the B command arms the external trigger input. Subsequently received external trigger inputs will then initiate transmission.

Q Quit - stops transmission in progress for one or both channels.

A detailed description of each command, in alphabetical order, is given on the following pages.

- **Command Descriptions**

Command: A (Address)

Syntax: zA

Purpose: The A command specifies a memory address in the selected channel's memory.

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Description: z is a 1- to 4-digit decimal integer from 0 to 1599 that specifies the current memory address for the selected channel. If z is omitted, the address will be set to address 0.

The A command strobes the address specified by z into the memory address register of the selected channel.

An A command can be sent while a transmission is in progress. The command will not affect the transmission nor will the transmission affect the contents of the address register. Two independent address registers, one for programming, the other for transmission, permit re-programming without affecting transmission.

Since the A command doesn't require reloading of the complete data list, any time duration value in memory can be changed by programming the appropriate address with the A command and updating the time duration value with the L command.

Example: If Channel B has been selected as the active channel (using the S command), then the command string "44A" programs Channel B memory address register to decimal value 44.

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Command: B (Begin)

Syntax: zB

Purpose: The B command either initiates or arms transmission for the selected channel or for both channels.

Description: z is a 1-digit decimal integer (0 or 1) that specifies the following:

z	Action
0	Begin or arm transmission for the channel last selected with an S command.
1	Begin or arm transmission for both channels simultaneously.

The type of triggering (selected by the M command) determines whether the B command starts or arms transmission. With internal triggering, the B command starts transmission. With external triggering, the B command is an ARM command for the external trigger.

Example: The command string "0S0M0B1S1M0B" initiates transmission in Channel A, then arms transmission in Channel B.

0S	select Channel A
0M	enable internal trigger and retriggerable mode
0B	begin transmission
1S	select Channel B
1M	enable external trigger and retriggerable mode
0B	arm transmission for an external trigger

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Command: C (Count)

Syntax: zC

Purpose: The C command specifies the number of times to transmit the entire data list in memory associated with the selected channel.

Description: z is a 1- or 2-digit decimal integer from 0 to 63 that specifies the number of times to transmit the data list. The value 0 specifies that the data list is to be transmitted continuously. The repeat count value can not be changed during operation.

The last programmed repeat count is reloaded automatically by the module at the completion of transmission. It does not need to be reprogrammed for each transmission. The repeat count is undefined after reset or at power-up. A C command is required for each channel for predictable operation following a reset or power-up.

Example: The command string "0S0C1S20C" specifies that Channel A is to repeat its data list continuously and Channel B is to repeat its data list 20 times.

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Input Request

Response
Syntax: z<CR><LF>

Purpose: An Input Request to the 73A-270 returns status information for the last selected channel. An input request is not a command output. It is generated by reading (inputting) from the module. The syntax shown is the syntax of the returned data.

Description: z is a 2-digit decimal number from 00 to 15, encoding four status bits. The four bits returned are:

1) Transmit In Progress A/B - Indicates the transmission status. A value of 1 indicates that the selected channel is transmitting. This bit will be zero during a breakpoint or following completion of transmission.

   This bit also reflects the state of the XMIT ACTIVE A or XMIT ACTIVE B output on the DB25S connector and the XMT A or XMT B LED on the front panel.

2) Transmit Complete Interrupt A/B - Indicates the status of the Transmit Complete Interrupt. A value of 1 indicates that a transmission is complete and an interrupt pending, if the interrupt has been enabled by the I command. This bit may be used to determine the source of an interrupt.

3) Memory Busy - A value of 1 indicates that the data list memory is busy. This bit is significant when trying to do in-progress data updates when the data being transmitted on the pulse/pattern output has several successive 100 nanosecond duration values. To update in-progress requires a free 100 nanosecond cycle when the memory is not being accessed by the transmitter (a duration value of 200 nanoseconds or more is transmitted). If an L command is issued while memory is busy, previous data sent by an L command will be overwritten.

4) Memory Overwrite Interrupt A/B - A value of 1 indicates that an interrupt has been generated in the selected channel as a result of issuing an L command while memory is busy. Proper operation of the 73A-270 Module requires checking the memory busy status if more than ten consecutive 100 nanosecond durations have been previously programmed and are being transmitted. Generation of this interrupt indicates improper use of the module and an error condition. The Memory Overwrite Interrupt can not be disabled by the I command.

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The state of the four bits indicated by return of the values 00 through 15 is as follows:

z	XMIT in Progress	XMIT Comp Interrupt	Memory Busy	Memory Busy Overwrite Interrupt
00	no	no	no	no
01	yes	no	no	no
02	no	yes	no	no
03	yes	yes	no	no
04	no	no	yes	no
05	yes	no	yes	no
06	no	yes	yes	no
07	yes	yes	yes	no
08	no	no	no	yes
09	yes	no	no	yes
10	no	yes	no	yes
11	yes	yes	no	yes
12	no	no	yes	yes
13	yes	no	yes	yes
14	no	yes	yes	yes
15	yes	yes	yes	yes

To check all possible causes of an interrupt, an input request must be performed for both channels A and B. Reading the data clears the above two interrupt bits (XMIT Complete and Memory Busy Overwrite Interrupt) for the selected channel.

Example: In response to an Input Request to the 73A-270 Module, the character string

02 <CR><LF>

might be returned. For the selected channel (A or B), this response indicates that transmission is not in progress, that an interrupt has been generated due to transmission completion or a breakpoint, that the memory is not busy, and that a Memory Busy Overwrite Interrupt has not been generated.

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Command: I (Interrupt)

Syntax: zI

Purpose: The I command enables or disables the XMIT Complete interrupt capability for the selected channel.

Description: z is a 1-digit decimal integer (0 or 1) that specifies:

z	Action
0	Disables the XMIT Complete interrupt capability for the selected channel.
1	Enables the XMIT Complete interrupt capability for the selected channel.

Interrupts indicate that a channel has completed transmission or that a breakpoint has occurred.

If an interrupt occurs, a VXIbus Request True event is generated, causing an interrupt at the VXIbus interrupt level selected by the Interrupt Level Select Switch on the 73A-270 Module. The VXIbus Interrupt Acknowledge clears the interrupt. Triggering the module to resume transmission arms the interrupt for the next transmission completion or breakpoint.

The 73A-270 generates two additional types of interrupts that cannot be disabled and are unaffected by the I command. They are the VXIbus Unrecognized Command interrupt and the Memory Busy Overwrite interrupt (see the L command).

The interrupt status may be read from the module at any time. The interrupt status is returned in response to an input request to the module (see Input Request) as a two-digit decimal integer followed by a carriage-return and line-feed <CR><LF>.

Example: The command string

0S1I1S0I

enables the XMIT Complete interrupt for Channel A and disables the XMIT Complete interrupt for Channel B. See the Input Request command description for an example of the response to an Input Request.

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Command: L (List)

Syntax: z_1z_2L

Purpose: For the selected channel, the L command specifies the time duration and polarity of the output level, breakpoint, and last address determination for the current memory address.

Description: z_1 is a 1- to 6-digit decimal integer from 1 to 999999 that specifies the duration of the output level as z_1 times 100 nanoseconds, 1 microsecond, 10 microseconds, or 100 microseconds, depending upon the resolution programmed for that channel. The z_1 parameter is not optional.

z_2 is a 1-digit decimal integer from 0 to 7 that specifies the output polarity (active or inactive), breakpoint, and last address bits for the current memory address, as shown:

z_2 Value	Last Address	Break-point	Polarity*	Command Format
0	No	No	Inactive	$z_1$0L
1	No	No	Active	$z_1$1L
2	No	Yes	Inactive	$z_1$2L
3	No	Yes	Active	$z_1$3L
4	Yes	No	Inactive	$z_1$4L
5	Yes	No	Active	$z_1$5L
6	Yes	Yes	Inactive	$z_1$6L
7	Yes	Yes	Active	$z_1$7L

* An active polarity output generates the following polarities:

TTL Out BNC connector - TTL high
Pulse/Pattern DB25S Output (active high) - TTL high
Pulse/Pattern DB25S Output (active low) - TTL low
VXIbus TTLTRG line - open collector low
Analog Bipolar Output - as programmed by P command

z_2 is not optional. It must be the last number to precede the L character, as shown under "Command Format" in the table above. A comma or carriage-return line-feed <CR><LF> may be used to separate z_1 and z_2, but is not required.

The L command strobes the time duration data and polarity, breakpoint and last address bits as specified by z_1 and z_2 into the present memory address. The memory address register is incremented automatically after the data is stored, allowing data to be stored in sequential addresses without sending an A (Address) command before each L command.

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A breakpoint causes the transmission to pause at the end of the time duration for which it is specified. The outputs will hold the polarity programmed for the last time duration prior to the pause.

An interrupt may be enabled (see I command) which generates an interrupt when the breakpoint occurs. The breakpoint is exited when the channel is triggered again.

The last address capability allows variable line length data lists of less than 1600 items to be transmitted or repeated.

In-Progress Updates

An L command can be sent while the module is transmitting, allowing in-progress updating of the data stream output. The new data can be specified at an address other than the address actively transmitting with minimal or no effect on the transmission. A minimal output time duration distortion occurs if the output is transitioning exactly when the new data is strobed into memory, in which case the transition is delayed two time increments (i.e. 200 nanoseconds). To avoid the time increment delay, in-progress commands should be timed to occur when the output data is not changing.

If in-progress data updates occur when the data to be up-dated is presently being transmitted, the new data will be effective immediately, allowing lengthening or shortening the duration, change of polarity, or change in breakpoint status or last address status of the data presently being transmitted. If the new data duration is less than the duration time already elapsed, the module will transition to the next data duration immediately.

NOTE: For the special case of having several successive duration outputs programmed to 100 nanoseconds, in-progress updating cannot always be done without error. If several in-progress updates are attempted in this situation, the data may be overwritten and lost.

A status capability which indicates whether the memory is busy is provided for these applications (see Input Request). An in-progress update should not be attempted when the memory is busy. The memory will not be accessible until the next time duration of 200 nanoseconds or more. A Memory Busy Overwrite interrupt will be generated if an in-progress data update occurs while memory is busy.

Example: The command string "0S1RA20L41L50L11L65L" programs the first output level of Channel A to a 2-µsec inactive output, followed by a 4-µsec active output, followed by a 5-µsec inactive output, followed by a 1-µsec and 6-µsec active output. The 6-µsec output is also specified as the last output in the list for Channel A. The "1R" characters preceding the L command specify a 1-µsec resolution for Channel A. The data is therefore in increments of 1 µsec. Figure 270-2 illustrates the output resulting from this command when programmed to repeat twice using the C (Count) command.

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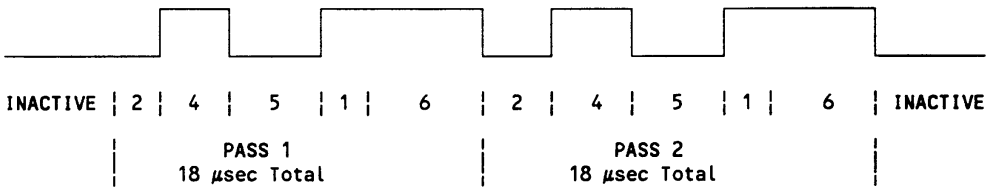


Figure 270-2: Sample Waveform TTL BNC Output

The above waveform would be output from Channel A as a result of the command 0S1RA20L41L50L11L65L2C0B.

0S Selects Channel A.
1R Selects 1 microsecond resolution.
A Selects memory address 0.
20L Sets first data duration for 2 µsec inactive.
41L Sets second data duration for 4 µsec active.
50L Sets third data duration for 5 µsec inactive.
11L Sets fourth data duration for 1 µsec active.
65L Sets fifth data duration for 6 µsec active and specifies it as last duration in the list.
2C Specifies repeat of the data output two times.
0B Starts transmission on the selected channel (Channel A).

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Command: M (Mode)

Syntax: zM

Purpose: The M command specifies either the Retriggerable or Non-Retriggerable modes for the selected channel. It also enables or disables external triggering.

Description: z is a 1-digit decimal integer that specifies the following:

z	Mode	Triggering
0	Retriggerable	Internal
1	Retriggerable	External
2	Non-Retriggerable	Internal
3	Non-Retriggerable	External

The difference between the Retriggerable modes and the Non-Retriggerable modes is that in the Non-Retriggerable modes, B (Begin) commands or external triggers during transmission are ignored. For the Retriggerable modes, B commands or external triggers during transmission will immediately restart transmission at the beginning of the list unless the channel is halted at a breakpoint.

If the module is stopped at a breakpoint in any mode, a trigger will cause the module to exit the breakpoint state and start transmission of the next segment of the data list. In this case, the trigger will not restart transmission at the beginning of the list. If the data list has breakpoints in it, but is not paused at one of those breakpoints when a retriggerable trigger occurs, transmission will restart at the beginning of the data list regardless of what segment of the list is transmitting.

If the module is retriggered to restart transmission at the beginning of the list, the repeat count will not be reset or decremented, but will remain at its present value.

The difference between internal and external triggering is that with internal triggering, transmission in a channel will begin immediately when a B command is issued. With external triggering, the B command becomes an arming command only. An external trigger at the front panel, on a VXIbus TTLTRG line or a VXIbus TRIGGER command as programmed by the X command, then starts transmission.

An external trigger at the front panel or on a VXIbus TTLTRG line initiates transmission three to four 100-nanosecond clock cycles (400 ns maximum using the internal clock) following a high to low transition on the trigger line, regardless of the resolution programmed for the channel.

Operation with Retriggerable mode - Internal Triggering:

The B (Begin) command starts transmission. Transmission will continue for the specified number of repeat times. If a B command is issued during transmission, transmission will immediately restart at the

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beginning of the data list. (The repeat count will not be changed.) Transmission will continue until the end of the data list has been sent the specified number of repeat times.

Operation with Retriggerable mode - External Triggering:

The B command arms the external trigger. When received, the external trigger starts transmission. Transmission will continue for the specified number of repeat times. An external trigger issued during transmission will immediately restart transmission at the beginning of the data list, unless the channel is halted at a breakpoint. (The repeat count will not be changed.) Transmission will continue until the end of the data list has been sent the specified number of repeat times. An additional B command is then required to rearm the external trigger. If breakpoints have been programmed, an external trigger is required to continue operation following each breakpoint occurrence.

Operation With Non-Retriggerable mode - Internal Triggering:

The B command is required to start transmission. An additional B command is required to continue transmission after each memory address identified as a breakpoint address. B commands issued while the module is transmitting will be ignored.

If no breakpoints are programmed, the module will transmit the data list the number of times specified by the C command, ignoring any triggers during transmission. A new trigger following completion of the transmission will repeat the transmission.

Operation With Non-Retriggerable mode - External Triggering:

A single B command to arm transmission, and an external trigger to start transmission are required. External trigger inputs are then used to continue transmission after each memory address identified as a breakpoint address.

External triggers issued while the module is transmitting will be ignored, unless the channel is halted at a breakpoint. When the list has been transmitted the specified number of times, an additional B command is required to arm the external trigger again.

Examples: The command string "81X0S0M1S3M1B" programs Channel A for the Retriggerable mode with internal triggering and Channel B for the Non-retriggerable mode with external trigger. "81X" programs VXIbus TTLTRG1 as the source of the external trigger on Channel B. "1B" sends a software trigger to Channel A, immediately starting transmission and arms Channel B for occurrence of an external trigger on TTLTRG1. A subsequent 0B command to Channel A during the transmission will restart Channel A transmission at the beginning of the data list. A subsequent B command or external trigger to Channel B while it is transmitting will be ignored unless breakpoints have been programmed into the data list for Channel B.

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Command: N (Inactive Analog Bipolar Level)

Syntax: zN

Purpose: The N command programs the inactive level of the analog bipolar output for the selected channel.

Description: z is a 2-digit signed decimal number from 00 to ±87 that specifies the inactive output level into a 50 ohm load as a multiple of 100 millivolts. Leading zeros are required; the + sign is optional. The inactive level is the level resulting from programming the polarity bit associated with a time duration to inactive (using the L command), and the level present on the output when the module is not transmitting.

The output into a high impedance load will be twice the programmed output level providing a maximum output level of ±17.4V. The output level for loads other than 50 ohms or open (high impedance) may be calculated as follows:

$$\text{Output Level} = \frac{2\,(\text{Programmed Voltage Value})\,(R_L)}{(R_L + 50)}$$

where R_L is the load.

On power-up or reset, the module is programmed for an inactive output level of 0 volts dc.

Examples:

1. -67N programs an inactive level of -6.7 into a 50 ohm load or -13.4 into an open load.

2. 09N programs an inactive level of 900 millivolts into a 50 ohm load or 1.800 volts into an open load.

3. To determine the programmed voltage value needed to achieve a +12 volt output into a 300 ohm load, use the above equation as follows:

$$\text{Programmed Voltage Value} = \frac{(\text{Output Level})\,(R_L + 50)}{2R_L}$$

$$\text{or: PVV} = \frac{12\,(300 + 50)}{2\,(300)} = 7 \text{ volts}$$

The command 70N will achieve the desired inactive level output of +12V for a 300 ohm load.

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Command: P (Active Analog Bipolar Level)

Syntax: zP

Purpose: The P command programs the active level of the analog bipolar output for the selected channel.

Description: z is a 2-digit signed decimal number from 00 to ±87 that specifies the active output level into a 50 ohm load as a multiple of 100 millivolts. Leading zeros are required; the + sign is optional. The active level is the level resulting from programming the polarity bit associated with a time duration to active (using the L command).

The output into a high impedance load will be twice the programmed output level providing a maximum output level of ±17.4V. The output level for loads other than 50 ohms or open (high impedance) may be calculated as follows:

$$\text{Output Level} = \frac{2\,(\text{Programmed Voltage Value})\,(R_L)}{(R_L + 50)}$$

where R_L is the load.

On power-up, the module is programmed to an active output level of 0 volts dc.

Examples:

1. -67P programs an active level of -6.7 into a 50 ohm load or -13.4 into an open load.

2. 09P programs an active level of 900 millivolts into a 50 ohm load or 1.800 volts into an open load.

3. To determine the programmed voltage value needed to achieve a +12 volt output into a 300 ohm load, use the above equation as follows:

$$\text{Programmed Voltage Value} = \frac{(\text{Output Level})\,(R_L + 50)}{2R_L}$$

$$\text{or: PVV} = \frac{12\,(300 + 50)}{2\,(300)} = 7 \text{ volts}$$

The command 70P will achieve the desired level output of +12V for a 300 ohm load.

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Command: Q (Quit)

Syntax: zQ

Purpose: The Q command stops transmission of one or both channels.

Description: z is a 1-digit decimal integer (0 or 1) that specifies the following:

z	Action
0	Stop transmission on the last selected channel.
1	Stop transmission in both channels simultaneously.

Examples: The command string "0S0Q" stops transmission on Channel A but not on Channel B.

The command string "1S0Q" stops transmission on Channel B but not on Channel A.

The command string "0S1Q" or "1S1Q" stops transmission on both channels within ±20 nanoseconds of each other.

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Command: R (Resolution)

Syntax: zR

Purpose: The R command specifies the time resolution range which will be used by the APPG Module for the selected channel.

Description: z is a 1-digit decimal integer (0, 1, 2, or 3) that specifies the following resolution ranges:

z	Internal 10 MHz Clock	External Clock *
0	100 nanosecond	1/f second
1	1 microsecond	10/f second
2	10 microsecond	100/f second
3	100 microsecond	1000/f second

* f = frequency of external clock

The R command programs the time increment multiplier for the selected channel. This multiplier is a time quantity equal to its associated resolution range. That is, for the 100 nanosecond resolution range, the channel programs in 100 nanosecond increments. For the 1 microsecond resolution range, the channel programs in 1 microsecond increments, and so on.

If an R command is sent to the module during transmission and the command is different from that presently programmed for the channel, the resolution multiplier for the channel will immediately change to correspond to the new programmed value.

Examples:

1. The command string "0S0R1S1R" programs Channel A for 100 nanosecond resolution and Channel B for 1 microsecond resolution. Programming a duration value of 6 with the L command will create a 600 nanosecond duration value on Channel A and a 6 microsecond duration value on Channel B.

2. If an external clock of 5 MHz is supplied and the command string "0S0R" is sent, the resolution for Channel A will be $1/(5 \cdot 10^6)$, or 200 nanoseconds.

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Command: S (Select)

Syntax: zS

Purpose: The S command selects Channel A or Channel B as the active channel for subsequent commands.

Description: z is the 1-digit decimal integer, 0 or 1, that selects the channel:

z	Channel Selected
0	Channel A
1	Channel B

An S command can be sent while a transmission is in progress without affecting transmission operations.

Examples: The command string "0S" selects Channel A as the active channel for subsequent commands that affect only the active channel.

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Command: T (TTLTRG)

Syntax: z_1z_2T

Purpose: The T command connects or disconnects the pulse/pattern output for channels A and B to or from any of the eight VXIbus backplane TTLTRG lines TTLTRG0* through TTLTRG7*.

Description: z_1 and z_2 are 1-digit decimal integers from 0 to 8 that specify the connections of Channel A (z_1) and Channel B (z_2) output to the VXIbus TTLTRG lines as follows:

z	Connects to TTLTRG Line
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	Disconnect from all TTLTRG lines

The T command has no effect on connections to the front panel BNC or DB25S 25 pin connector pulse/pattern outputs (they are always connected).

On power-up or reset, a value of 8 is programmed, disconnecting the pulse/pattern output from all TTLTRG lines.

Both channels may be connected to the same TTLTRG line. Since the VXIbus TTLTRG lines are "open collector", the line will be driven low if either channel is programmed for an active polarity level by the L command. The TTLTRG line is driven low when an active pulse/pattern output level is programmed to achieve this "wired-OR" capability made possible by the "open collector" signals.

The pulse/pattern output may also be connected to the same TTLTRG line as the external trigger (see the X command) of the opposite channel to use one channel to trigger another.

This command programs both Channel A and Channel B independent of the active channel programmed by the S (Select) command.

Example: The command string

28T82X0S3R2M0A3600000L15L1C1S0R3M0A11L94L0C1B

programs Channel A for connection to VXIbus TTLTRG2* and Channel B for no connection to the TTLTRG lines. It also programs a delayed 100 µsec

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pulse on Channel A that is used to trigger a continuous waveform on Channel B 36 seconds later.

28T	connects Channel A to TTLTRG2*
82X	connects Channel B external trigger to TTLTRG2*
0S	selects Channel A
3R	programs Channel A for 100 µsec resolution
2M	programs Channel A for non-retriggerable internal trigger mode
0A	reset Channel A data list address to address 0
3600000L	programs first data list as 360000 100-µsec durations, or 36 seconds at an inactive level
15L	programs second data list duration as a 100 µsec active duration (will drive TTLTRG2* active low), and as the last data list value
1C	programs Channel A for a repeat count of 1
1S	selects Channel B
0R	programs Channel B for 100 nanosecond resolution
3M	programs Channel B for non-retriggerable external trigger mode
0A	resets address counter
11L	programs first Channel B data list value as 100 nanosecond active level
94L	programs the second Channel B data list value as a 900 nanosecond inactive level, and as the last data list value.
0C	programs Channel B for continuous transmission
1B	triggers Channel A to start its delayed pulse program and arms Channel B for the external trigger to be generated by Channel A.

When this command is sent, the XMTA, TB0A, TB1A, and EXTB LEDs will light. Exactly 36 seconds later, the XMTA LED will go out and the XMTB will light continuously. At this time an oscilloscope on the TTL OUT B BNC may be used to observe a TTL signal with a one microsecond period and a high TTL pulse width of 100 nanoseconds.

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Command: X (External Trigger)

Syntax: z_1z_2X

Purpose: The X command connects or disconnects the External Trigger Input for both channels A and B, to or from any of the eight VXIbus backplane TTLTRG lines (TTLTRG0* through TTLTRG7*), or to the VXIbus TRIGGER command, or to the front panel BNC (or DB25S connector) External Trigger Input.

Description: z_1 and z_2 are 1-digit decimal integers from 0 to 9 that specify the channel A (z_1) and Channel B (z_2) external trigger source as follows:

z	Connect to
0	TTLTRG0*
1	TTLTRG1*
2	TTLTRG2*
3	TTLTRG3*
4	TTLTRG4*
5	TTLTRG5*
6	TTLTRG6*
7	TTLTRG7*
8	front panel BNC or DB25S connector
9	VXIbus TRIGGER command.

When connected to a TTLTRG line, a high to low transition generated by another VXIbus module or this module will trigger the connected channel.

On power-up or reset, a value of 8 is programmed, disconnecting the External Trigger Input from all TTLTRG lines and the VXIbus trigger command and connecting it to the front panel BNC and DB25S connector External Trigger Signal.

Both channels may be connected to the same TTLTRG line, allowing both channels to be triggered by the same signal.

Any external trigger input must be enabled by the M (Mode) command. And external trigger from any of the TTLTRG lines, the front panel, or the VXIbus TRIGGER command will have no effect if the channel has been programmed for internal triggering by the M command.

This command programs both Channel A and Channel B and is not dependent on which channel is programmed by the S command.

Example: The command string "93X" selects the VXIbus TRIGGER command from the VXIbus commander of the 73A-270 for Channel A, and VXIbus TTLTRG3* for Channel B, as the sources for any external trigger programmed for the two channels.

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SYSFAIL, SELF TEST, AND INITIALIZATION

The 73A-270 Module will reset to its default condition at power-up, or for a VXIbus hard or soft reset condition. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the 73A-270's commander, sets the Reset bit in the 73A-270's Control register and the Halt Switch is ON.

The 73A-270 Module continuously monitors the +5V dc, ±24V dc, -5.2V dc, -2V dc, and its own internal ±20.9V dc power supplies.

If all power supplies are valid, on power-up:

1) The SYSFAIL* (VME system-failure) line will never be set active, and the Failed LED will not be lit. If any of the supplies fails, either at power-up or during operation, the SYSFAIL line will be set active and the Failed LED will be lit and remain lit.

2) The module enters the VXIbus PASSED state (ready for normal operation) on power-up if all power supplies are valid.

The default condition of the 73A-270 Module after the completion of power-up is:

Channel A: Selected.
Resolution: 100 nanosecond, both channels.
Mode: Retriggerable, both channels.
External Trigger: Disabled, both channels.
External Trigger Source: Front panel, both channels.
VXIbus TTLTRG Pulse/Pattern Output: Not connected.
Interrupt Capability: Disabled, both channels.

Channel A and B Pulse/Pattern Memory Contents: Undefined.
Channel A and B Repeat Count: Undefined.
Power LED: Lit.
All Other LEDs: Extinguished.
Pulse/Pattern Outputs: Inactive.
Transmission In Progress Outputs: Inactive.

SYSFAIL* Operation

SYSFAIL* becomes active for any power supply failure, or if the module loses any of its power voltages. When the card cage Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the 73A-270 Module to deactivate SYSFAIL* in all cases except when +5 volt power is lost.

PROGRAMMING EXAMPLES

This section contains example programs which demonstrate how the various programmable features of the 73A-270 are used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller.

• Definition of BASIC Commands

The programming examples in this manual are written in Microsoft GW BASIC, using the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

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Command Result

CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)

The CALL ENTER statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the 73A-270.

CALL SEND (ADDRESS%, WRT$, STATUS%)

The CALL SEND statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.

END Terminates the program.

FOR/NEXT

Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.

GOSUB n

Runs the subroutine beginning with line n. EX: GOSUB 750 - runs the subroutine beginning on line 750. The end of the subroutine is delineated with a RETURN statement. When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.

GOTO n

Program branches to line n. EX: GOTO 320 - directs execution to continue at line 320.

IF/THEN

Sets up a conditional IF/THEN statement. Used with other commands, such as PRINT or GOTO, so that IF the stated condition is met, THEN the command following is effective. EX: IF I = 3, THEN GOTO 450 - will continue operation at line 450 when the value of variable I is 3.

REM All characters following the REM command are not executed. REM statements are used for documentation and user instructions. EX: REM **CLOSE ISOLATION RELAYS**

RETURN

Ends a subroutine and returns operation to the line after the last executed GOSUB command.

<CR> Carriage Return character, decimal 13.

<LF> Line Feed character, decimal 10.

- **Programming Examples In BASIC**

The following sample BASIC programs show how commands for the 73A-270 might be used. These examples assume that the 73A-270 has logical address 24 and is installed in a VXIbus card cage that is controlled through an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent using a Capital Equipment Corp. IEEE-488 interface. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 21 and to have converted the 73A-270 Module's logical address to an IEEE-488 primary address of decimal 24.

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Example 1:

The following program causes the 73A-270 to output a 2 µsec pulse 4 µsec after trigger, followed 10 µsec later by a ten millisecond (10,000 µsec) pulse. The signal is output on Channel A and is repeated continuously. The module is programmed for retriggerable operation with internal triggering.

Lines 10 through 40 initialize the PC's IEEE-488 interface card as a system controller with an IEEE-488 address of decimal 21. Line 50 assigns the decimal IEEE-488 address of the 73A-270 to the variable ADDR270%.

```
10   DEF SEG = &HC400
         Defines memory location of IBM PC IEEE-488 Interface Module.
20   SEND = 9 : INIT = 0 : ENTER = 21
         Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
30   PC.ADDRESS% = 21 : CONTROL% = 0
         Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a
         controller.
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADDR270% = 24
         Define 73A-270's IEEE-488 address.
60   WRT$ = "0S0C0A1R0M40L21L100L100005L0B"
         0S selects Channel A, 0C programs continuous output, 0A resets the data list address
         pointer, and 1R programs 1 µsec resolution. The following four L commands
         program a 4 µsec inactive level, a 2 µsec active level, a 10 µsec inactive level, and
         a 10 millisecond active level output. The "5" in the "100005L" identifies the 10
         millisecond duration as both active and the last item in the list. 0B starts
         transmission on Channel A.
70   CALL SEND (ADDR270%, WRT$, STATUS%)
380  END
```

Connecting an oscilloscope to the TTL OUT A BNC will display the described waveform. (An active level is a TTL high.)

Example 2:

This example programs the Channel B bipolar output to put out a steady state -2V signal as long as a TTL active low pulse occurs on the Channel A External Trigger BNC input at least every 250 milliseconds. If a pulse is missed, a series of eight 1 µsec pulses of -5.2V are output on the Channel B output with 19 µsec gaps between the pulses. The bipolar output is terminated with a 50 Ohm load.

Lines 10 through 40 initialize the PC's IEEE-488 interface card as a system controller with an IEEE-488 address of decimal 21. Line 50 assigns the decimal IEEE-488 address of the 73A-270 to the variable ADDR270%.

```
10   DEF SEG = &HC400
         Defines memory location of IBM PC IEEE-488 Interface Module.
20   SEND = 9 : INIT = 0 : ENTER = 21
         Initialize PROM offsets for IBM PC IEEE-488 Interface Module.
```


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```
30   PC.ADDRESS% = 21 : CONTROL% = 0
```
Define IEEE-488 Interface Module's IEEE-488 address, and define it to be a controller.

```
40   CALL INIT (PC.ADDRESS%, CONTROL%)
50   ADDR270% = 24
```
Define 73A-270's IEEE-488 address.

```
60   WRT$ = "78T87X0S1M0A3R25000L15L1C1S-20N-52P3M0A1R11L194L8C1B0S"
```
See the Note below.

```
70   CALL SEND (ADDR270%, WRT$, STATUS%)
80   RD$ = SPACES(4)
90   CALL ENTER (RD$, LENGTH%, ADDR270%, STATUS%)
```
Read the status of Channel A to see if transmission ever completed.

```
100  XMT = VAL(RD$)
110  IF XMT -2 * INT (XMT/2) > .5 THEN GOTO 80
```
Check to see if the status response is an odd number, indicating that transmission is still active.

```
120  PRINT "250 MILLISECOND UPDATE INPUT MISSED"
```
Print a message to the console if a 250 millisecond update was missed (Channel A completed transmission).

```
130  END
```

NOTE: Explanation of Line 60:

78T87X TTLTRG7 is used to trigger Channel B if Channel A puts out a pulse on TTLTRG7.

0S1M Channel A is selected and programmed for retriggerable operation with an external trigger.

0A The address counter is reset.

3R25000L15L
A 100 µsec pulse following a 250 millisecond delay is programmed for Channel A. If an external trigger occurs on the Channel A External Trigger BNC within 250 milliseconds, the retriggerable operation will start the 250 millisecond delay again without outputting the 100 µsec trigger pulse to Channel B.

1C Channel A is programmed for a repeat count of 1.

1S-20N-52P3M
Channel B is programmed for a -2.0V inactive bipolar output level and a -5.2V active bipolar output level, and is programmed for external trigger mode to activate the VXIbus TTLTRG7 trigger input.

0A The address counter is reset.

1R A 1 µsec resolution is programmed.

11L194L8C
Programs a 1 µsec pulse followed by a 19 µsec gap, for transmission eight times.

1B Arms both Channels A and B for an external trigger, Channel A from the front panel BNC and Channel B from VXIbus TTLTRG7. Operation will start as soon as the first pulse occurs on the Channel A BNC input.

0S Selects Channel A for the status response read in Line 90.

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APPENDIX A - VXIbus OPERATION

The 73A-270 Module is a C size single slot VXIbus Message Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The 73A-270 Module is neither a VXIbus commander nor VMEbus master, and therefore it does not have a VXIbus signal register. The 73A-270 is a VXIbus message based servant.

The module supports both the Normal Transfer mode and the Fast Handshake Mode of the VXIbus, using the Write Ready and Read Ready bits of the module's Response register.

A Normal Transfer mode Read of the 73A-270 Module proceeds as follows:

1. The commander reads the 73A-270's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready bit until it becomes true.

2. The commander writes the Byte Request command to the 73A-270's Data Low register (0DEFFh).

3. The commander reads the 73A-270's Response register and checks if the Read Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Read Ready bit until it becomes true.

4. The commander reads the 73A-270's Data Low register.

A Normal Transfer mode Write to the 73A-270 Module proceeds as follows:

1. The commander reads the 73A-270's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready bit until it becomes true.

2. The commander writes the Byte Available command to the 73A-270's Data Low register (0BCXX or 0BDXX depending on the End bit).

The module also supports the Fast Handshake mode during some commands. In this mode the module is guaranteed to return DTACK* within the 20 microsecond window defined by the VXIbus Specification. (If the internal 10 MHz clock is used, the 73A-270 will return DTACK* within 550 nanoseconds.) For non-normal use, where a slow external clock is used, with the Clock switches set for fast external clock, the 73A-270 Module asserts BERR* to switch from Fast Handshake mode to Normal Transfer mode. The 73A-270's Read Ready and Write Ready bits react properly during Fast Handshake.

A Fast Handshake Transfer Mode Read of the 73A-270 Module proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the 73A-270's Data Low register.

2. The commander reads the 73A-270's Data Low register.

A Fast Handshake Transfer Mode Write to the 73A-270 Module proceeds as follows:

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The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX depending on the state of the End bit) to the 73A-270's Data Low register.

The 73A-270 Module has no registers beyond those defined for VXIbus Message Based devices. All communications with the module are through the Data Low register, the Response register, or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the 73A-270's address space may cause incorrect operation of the module.

CAUTION:

If the user's card cage has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR* (as defined by the VXIbus Specification) may cause operating problems on these boards.

As with all VXIbus devices, the 73A-270 Module has registers located within a 64 byte block in the A16 address space.

The base address of the 73A-270 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set in the Logical Address switches.

73A-270 Configuration Registers.

Below is a list of the 73A-270 Configuration Registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address.

REGISTER DEFINITIONS

Register	Address	Type		Value (Bits 15-0)
ID Register	0000H	RO		1011 1111 1111 1100 (BFFCh)
Device Type	0002H	RO		See Device Type definition below
Status	0004H	R		1X11 1111 1111 1111 (BFFFh or FFFFh)
Control	0004H	W		0111 1111 1111 110X (7FFCh or 7FFDh)
Offset	0006H	WO		Not used
Protocol	0008H	RO		1111 0111 1111 1111 (F7FFh)
Response	000AH		RO	Defined by state of the interface
Data High	000CH			Not used
Data Low	000EH		W	See Data Low definition below
Data Low	000EH		R	See Data Low definition below

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BIT DEFINITIONS

Register	Bit Location	Bit Usage	73A-270 Value	73A-270 Usage
ID	15-14	Device Class	10	Message Based
	13-12	Address Space	11	A16 only
	11-0	Manufact. ID	1111 1111 1100	Colorado Data Systems
Device Type	15-0	Device Type	1111 1110 1111 0001	Ones comp. of 270
Status	15	A24/32 Active	1	Not used
	14	MODID*	1	MODID line not active
			0	MODID line active
	13-4	Device dependent	11 1111 1111	Not used
	3	Extended*	1	Not used
	2	Passed	1	Always passed
	1-0	Device dependent	11	Not used
Control	15	A24/32 Enable	1 or 0	No effect
	14-2	Device dependent	111 1111 1111 11	Not used
	1	SYSFAIL Inhibit	1	Disables module from driving Sysfail
			0	Enables module to drive Sysfail
	0	Reset	1	Reset
			0	Not reset
Protocol	15	CMDR*	1	Servant only
	14	Signal Reg.*	1	No Signal Reg.
	13	Master*	1	Slave only
	12	Interrupter	1	Interrupter
	11	FHS*	0	Fast Handshake capability
	10	Shared Memory*	1	No Shared Memory capability
	9-4	Reserved	11 1111	Not used
	3-0	Device dependent	1111	Not used
Response	15	Defined value of 0	0	Per VXI
	14	Reserved	1	Per VXI
	13	DOR	1	Not used
	12	DIR	1	Not used
	11	ERR*	1	Not used
	10	Read Ready	1 or 0	Indicates that the instrument portion of the module has data available to be read. Set by the instrument following a "Byte Request" command, and cleared on a read from the Data Low register or on reset.

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BIT DEFINITIONS (continued)

Register	Bit Location	Bit Usage	73A-270 Value	73A-270 Usage
Response (cont'd.)	9	Write Ready	1 or 0	Cleared upon receipt of a "Byte Available" command. Set when the instrument is ready to receive a data byte or on reset.
	8	FHS Active*	0	FHS active
			1	FHS inactive
	7	Locked*	1	Not used
	6-0	Device dependent	111 1111	Not used

Data High - not implemented.

Data Low (read/write)

Word Serial Commands

A write to the Data Low Register causes this module to execute some action based on the data written. This section describes the device specific Word Serial commands this module responds to and the results of these commands.

Read Protocol Command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

If the Data Low register is read after this command, the contents are as follows:

VXIbus Revision Level:
Bit 15
0 VXIbus Revision 1.2 Device

Device dependent (unused):
Bits 14 13 12 11
1 1 1 1

Reserved:
Bits 10 9 8 7 6 5
1 1 1 1 1 1

Triggered*: (supports trigger command)
Bit 4
0 This module supports the trigger command.

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I4*: (supports VXIbus 488.2 Instrument protocol)

Bit 3

1 This module does not support 488.2 protocol.

I*: (supports VXIbus Instrument protocol)

Bit 2

0 This module supports instrument protocol.

ELW*: (supports Extended Longword Serial protocol)

Bit 1

1 This module does not support ELW protocol.

LW*: (supports Longword Serial protocol)

Bit 0

1 This module does not support LW protocol.

73A-270 Interrupts

The 73A-270 will interrupt its commander with the following "events":

Unrecognized Command Event:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 1  1  1  0  1  1  1  1  <--Logical Address--->
```

This event is generated by this module in response to any command sent to the data low register other than the following:

Byte Available
Byte Request
Begin Normal Operation
Clear
Read Protocol
Trigger
Identify Commander

Request True:

```
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
 1  1  1  1  1  1 0 1 <--Logical Address--->
```

This event is generated as programmed by the I command or in response to a memory busy overwrite error.

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APPENDIX B - FRONT PANEL INPUT/OUTPUT CONNECTIONS

The signals listed below are available on a DB25S connector. When seen from the front, Pin 1 is on the bottom right, and Pin 14 is on the bottom left.

Six of the signals, Pulse/Pattern Out A and B, Bipolar Out A and B, and External Trigger A and B, are also available on the front panel BNC connections labeled TTL OUT A and B, BPLR OUT A and B, and EXT TRG A and B. A description of each of the signals follows the pinout listing.

DB25S Pin No.	Function
1	External Trigger A (TTL active low)
2	Transmission In Progress A (TTL active high)
3	Transmission In Progress A (TTL active low)
5	External Clock In *
7	Bipolar Out A
9	Bipolar Out B
11	Transmission In Progress B (TTL active low)
12	Transmission In Progress B (TTL active high)
13	External Trigger B (TTL active low)
14	Pulse/Pattern Out A (TTL active high)
15	Pulse/Pattern Out A (TTL active low)
17	External Clock Out *
24	Pulse/Pattern Out B (TTL active low)
25	Pulse/Pattern Out B (TTL active high)

4, 6, 10, 16, 18, 23 - Digital Ground
8, 19, 20, 21, 22 - Analog Ground

* Signal changes are clocked for a high-to-low transition of the External Clock In or Out signal.

Pulse/Pattern Outputs

Pulse/pattern outputs for Channel A and B are provided at the TTL OUT A and B front panel BNCs, and on the DB25S Pulse/Pattern Out A and B (TTL active high) and Pulse/Pattern Out A and B (TTL active low) connector pins. The front panel BNCs and the DB25S Pulse/Pattern Out (TTL active high) outputs are TTL high for an active pulse/pattern level. The DB25S Pulse/Pattern Out (TTL active low) outputs are TTL low for an active pulse/pattern level.

Analog Bipolar Pulse/Pattern Outputs

Analog bipolar pulse/pattern outputs for Channel A and B are provided at the BPLR OUT A and B front panel BNCs, and on the DB25S Bipolar Out A and B connector pins. The signal level for both the BNC and DB25S connections when the module is not transmitting or is transmitting at an inactive level will be as programmed by the N command. The signal level when the module is transmitting and an active level is programmed will be as programmed by the P command.

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External Trigger Inputs

The EXT TRG A and EXT TRG B BNC connections, or the DB25S External Trigger A and B (TTL active low) connector pins are used to input external TTL trigger signals. When Channel A or B is programmed for an external trigger and the front panel external trigger has been selected by the X command, transmission will start three to four clock cycles (400 ns maximum using the internal clock (400 ns maximum using the internal clock) following a high-to-low transition of the channel's external trigger input (on either the BNC or DB25S pin). Internal 10K pull-up resistors pull each input high when not connected.

S1 Connector Input/Output Signals

S1 is a 25 pin DB25S connector which provides several additional Input/Output signals.

Additional signals provided at the DB25S front connector are:

- an external clock input - so that several modules may be programmed for parallel operation.

- a buffered internal clock - brought to the front connector of the APPG Module, allowing any module to be the common clock source for a parallel module output configuration.

- each channel provides a TTL level output to the module's front connector indicating transmission is in progress. This signal (when indicating that transmission is not in progress) may be used to indicate the need for another trigger to continue transmission. Both TTL active high and TTL active low polarities of the signal are provided for both channels.

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APPENDIX C - VXIbus GLOSSARY

Certain terms used in this manual have very specific meanings in the context of a VXIbus System. A list of these terms is presented below.

Commander

A VXIbus device that has bus master capability and has VXIbus servants under it in the system hierarchy. A commander may be a servant as well.

Fast Handshake

Compared to the Normal Transfer Mode of the VXIbus, the Fast Handshake Transfer Mode reduces the number of VMEbus data transfer cycles by 50%. Upon receipt of a request for data, a fast handshake module is able to return data in less than 20 µs, so that the VXIbus fast handshake protocol can be used by the module's commander.. Using fast handshake protocol, data can be written and read without checking the Ready bits in the module's Response register.

Hard Reset

This is the state of the module when the SYSRESET* line is true. While in this state, the module is inactive and its Status and Control registers are cleared. The SYSFAIL* line is driven low, and the Failed LED is lit. In the case of a CDS 73A-IBX Card Cage, for example, a module hard reset occurs when the card cage is powered-up or the Reset switch on the front panel of the 73A-151 Resource Manager/IEEE-488 Interface Module is depressed.

Interrupt Handler

The module in the VXIbus system that generates the hardware interrupt acknowledge for a particular VME interrupt level. The software interrupt handler may or may not be on the same module as the hardware interrupt handler. In the case of CDS instrument modules, both the hardware and software interrupt handlers reside on the commander module of a given servant module.

Logical Address

A unique 8 bit number which identifies each VXIbus device in a system. It defines the device's A16 register addresses, and indicates the device's commander/servant relationship.

Reset Bit

Bit 0 in the Control register of the module. When set to a one (1) by the module's commander or resource manager, and the 73A-270 Halt switch is ON, the 73A-270 is forced into a reset state.

Resource Manager

A message based commander located at logical address 0, which provides configuration management services, including commander/servant mapping, address map configuration, self test, and diagnostic management. In CDS systems, the Resource Manager function is co-located with the VMEbus controller, the slot 0 timing functions, and the system controller interface.

Servant

A VXIbus device that may or may not have bus master capability, that is under control of a commander in the VXIbus system hierarchy. A servant may also be a commander.

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Soft Reset

This state is entered when the reset bit in the module's Control Register is set to one (1) by the module's commander. While in this state a device is inactive, interrupts which are pending are unasserted, all pending bus requests are unasserted, and any onboard processor is halted. The device's VMEbus slave interface is active in this state; however, the device is incapable of responding to any commands other than RESET and SYSFAIL INHIBIT. In the case of a CDS 73A-IBX Card Cage, for example, a module soft reset occurs when the card cage's 73A-151 Resource Manager/IEEE 488 Interface Module receives a STOP command over the IEEE-488 bus that is addressed to the 73A-270.

The 73A-270 does not reset for a Soft Reset unless the Halt switch is ON. When reset, the 73A-270 becomes inactive, clears all pending interrupts and resets its operation to the power-up state. The 73A-270 does not generate VMEbus bus requests and does not have an on-board processor.

SYSFAIL INHIBIT

Bit 1 in the Control register of the module. When set to a one (1) by the VXIbus Resource Manager, the device is disabled from driving the SYSFAIL* line. CDS modules are designed so that the Sysfail Inhibit bit will work under all conditions except when the +5V power is lost.

VXI Commands

These are commands passed from a commander to a servant within the VXIbus environment. A command may or may not be prompted by an external event. For example, an IEEE-488 GROUP EXECUTE TRIGGER will generate a trigger command to all addressed devices. However, a BEGIN NORMAL OPERATIONS command is generated by the VXIbus resource manager and has no external source.

VXI Events

Events are passed from a servant to a commander. They may be generated by the servant either in response to a command (for example, Unrecognized Command event) or due to a condition detected in the module (internal error).

VXI Message Based Instrument

An intelligent instrument that implements the defined VXIbus registers and, at a minimum, the Word Serial Protocol. All CDS VXIbus devices are message based.

VXI Word Serial Protocol

The simplest required communication protocol supported by Message Based devices in a VXIbus system. It utilizes the A16 communications registers to transfer data, using a simple polling handshake method. All CDS VXIbus devices implement the Word Serial protocol.

488-VXIbus Interface

An IEEE-488 to VXIbus Interface Device is a message based device which provides communication between the IEEE-488 bus and VXIbus instruments.

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Appendix D: Performance Verification

This procedure verifies the performance of the 73A-270 Arbitrary Pulse-Pattern Generator. It may be performed in your current VXIbus system if it meets the requirements described in Table A–2. Also, it is not necessary to complete the entire procedure if you are only interested in a specific performance area. Some tests depend on the correct operation of previously verified functions so it is best to perform the entire procedure in the order presented.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

Please familiarize yourself with the following conventions which apply throughout the procedure:

- Each verification sequence begins with a table, similar to the one below, which provides information and requirements specific to that section.

Equipment Requirements	Oscilloscope (item 1) Oscilloscope Probe (item 2)
Prerequisites	Prerequisites listed on page 56

The item number after each piece of equipment refers to an entry in Table A–1, *Required Test Equipment*.

- This procedure assumes that your VXIbus system is configured as indicated in Table A–3 and that you will be using the National Instruments PC-GPIB controller, and software (NI-488.2M). In the verification sequences you will be instructed to issue Interface Bus Interactive Control (ibic) commands to set up the 73A-270 system. Please refer to the NI-488.2M User Manual for additional information. If you are using a different controller, simply substitute the equivalent commands.

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Prerequisites

The test sequences in this procedure are a valid verification of the 73A-270 when the following requirements are met:

- The 73A-270 has been calibrated within the last 12 months
- The 73A-270 module covers are in place and the module is installed in an approved VXIbus mainframe according to the procedure in Section 2 of the Operating Manual
- The 73A-270 has passed its power-on self test
- The 73A-270 is operating in an ambient environment as specified in Section 1 of the Operating Manual and has been operating for a warm-up period of at least 10 minutes

Equipment Required

This procedure uses traceable signal sources and measurement instruments. Table A–1 lists the required equipment. You may use equipment other than the recommended examples if it meets the minimum requirements listed.

Table A–1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. Digitizing Oscilloscope	300 MHz bandwidth; 50 Ω input impedance; ≤ 1.5% DC vertical accuracy	Tektronix TDS 460	Checking pulse-pattern signal timing, amplitude, and phase
2. Oscilloscope Probe	250 MHz, 10X, 10 MΩ, 12.7 pF	Tektronix P6130	Checking pulse-pattern signal timing, amplitude, and phase
3. Counter/Timer	10 MHz frequency measurement	Tektronix 73A-541	Checking pulse/burst accuracy
4. External Clock Source	25 MHz	Tektronix VX4790A	Checking external clock
5. 50 Ω BNC Coaxial Cable (two required)	50 Ω impedance; BNC male connectors	Tektronix part number 012-0057-01	Interconnecting electrical signals
6. SMB to BNC Adapter Cable	50 Ω impedance; SMB male, BNC female, connectors	Tektronix VX1729	Interconnecting electrical signals
7. BNC Female to BNC Female (barrel)	50 Ω impedance; Female to BNC Female	Tektronix part number 103-0028-00	Interconnecting electrical signals
8. BNC Male to Dual Binding Post	50 Ω impedance; BNC male, Dual Binding Post connectors	Tektronix part number 103-0035-00	Interconnecting electrical signals
9. DB-25 front panel interconnect assembly	Male DB-25 Connector with 6-inch jumper wires (26 AWG) soldered to pins 4 & 5	DB-25, Tektronix part number 131-0570-00	Interconnecting electrical signals

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73A-270-Under-Test Configuration

In order to perform this verification procedure, the 73A-270-under-test must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table A–2.

Table A–2: Elements of a Minimum 73A-270 –Under-Test System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	Two available slots for 73A-270 and 73A-541 in addition to the Slot 0 controller	Tektronix VX1410 VX1400A	Provides power, cooling, and backplane for VXIbus modules
2. Slot 0 Controller	Resource Mgr., Slot 0 Device Functions, IEEE 488 GPIB Interface.	GPIB — VXI	Provides Slot 0 functions, Resource Mgr., and GPIB/VXIbus interface
3. VXIbus System Controller	VXIbus-Talker/Listener/Controller	IBM 486 with National Instruments GPIB PC2A card & NI-488.2M software and GPIB cable (Tektronix part number 012-0991-00)	Controlling the VXIbus System

Test System Configuration

Table A–3 describes the VXIbus system configuration which is assumed in this procedure. If your configuration is different, you do not need to change it, just note that you will observe your device names and addresses in the test sequence.

Table A–3: Test System Configuration

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address
GPIB0	GPIB0	(PC card)	NA
SLOT0	SLOT0	Slot 0	1
73A-270	VX270	Slot 1	2
73A-541	VX541	Slot 2	3
VX4790A	VX4790	Slot 3	4

Test Record

Photocopy the Test Record, and use it to record the performance verification results for your module.

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73A-270 Test Record

73A-270 Serial Number:		Temperature and Relative Humidity:		
Date of Last Calibration:		Verification Performed by:		
Certificate Number:		Date of Verification:		
VXIbus Interface Checks		**Logical Address, IEEE Address, Slot No., MFG., Model, etc.**		
Table Command Response	1st Response			
	2nd Response			
	3rd Response			
	4th Response			
	5th Response			
		Passed	**Failed**	
Program Command Response	1 MHz Pattern			
	Interrupt SRQ			
TTL OUT A Checks		**Minimum**	**Measured Value**	**Maximum**
Time Base Resolution	100 ns ± 10 ns	90 ns		110 ns
	1 µs ± 10 ns	99 ns		1.01 µs
	10 µs ± 10 ns	9.99 µs		10.01 µs
	100 µs ± 10 ns	99.99 µs		100.01 µs
Pulse Duration Multiplier	1000 × 100 ns	4,999.5 Hz		5,000.5 Hz
	100 × 1 µs	4,999.5 Hz		5,000.5 Hz
	10 × 10 µs	4,999.5 Hz		5,000.5 Hz
	1 × 100 µs	4,999.5 Hz		5,000.5 Hz
	2 × 100 µs	2,499.75 Hz		2,500.25 Hz
	85.8585 ms ±20 ns	85.85848 ms		85.85852 ms
	42.4242 ms ±20 ns	42.42418 ms		42.42422 ms
		Passed	**Failed**	
Burst Pattern	42 × 1100 µs			
	21 × 1100 µs			
TTL OUT B Checks		**Minimum**	**Measured Value**	**Maximum**
Time Base Resolution	100 ns ± 10 ns	90 ns		110 ns
	1 µs ± 10 ns	99 ns		1.01 µs
	10 µs ± 10 ns	9.99 µs		10.01 µs
	100 µs ± 10 ns	99.99 µs		100.01 µs

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73A-270 Test Record (Cont.)

TTL OUT B Checks		**Minimum**	**Measured Value**	**Maximum**
Pulse Duration Multiplier	1000 × 100 ns	4,999.5 Hz		5,000.5 Hz
	100 × 1 µs	4,999.5 Hz		5,000.5 Hz
	10 × 10 µs	4,999.5 Hz		5,000.5 Hz
	1 × 100 µs	4,999.5 Hz		5,000.5 Hz
	2 × 100 µs	2,499.75 Hz		2,500.25 Hz
	85.8585 ms ±20 ns	85.85848 ms		85.85852 ms
	42.4242 ms ±20 ns	42.42418 ms		42.42422 ms
		Passed	**Failed**	
Burst Pattern	42 × 1100 µs			
	21 × 1100 µs			

BPLR OUT A Checks		**Minimum**	**Measured Value (voltage & phase)**	**Maximum**
Voltage	± 2 V ± 260 mV	± 1.740 V		± 2.260 V
	± 5 V ± 260 mV	± 4.740 V		± 5.260 V
	± 8.7 V ± 260 mV	± 7.740 V		± 8.260 V
Opposite Phase with TTL OUT	± 8.7 V ± 260 mV	± 7.740 V		± 8.260 V
	± 0 V ± 260 mV	± 0.240 V		± 0.240 V

BPLR OUT B Checks		**Minimum**	**Measured Value (voltage & phase)**	**Maximum**
Voltage	± 2 V ± 260 mV	± 1.740 V		± 2.260 V
	± 5 V ± 260 mV	± 4.740 V		± 5.260 V
	± 8.7 V ± 260 mV	± 7.740 V		± 8.260 V
Opposite Phase with TTL OUT	± 8.7 V ± 260 mV	± 7.740 V		± 8.260 V
	± 0 V ± 260 mV	± 0.240 V		± 0.260 V

Triggering & Breakpoint for Channel A		**Passed**	**Failed**
Trigger Lines	TTLTRG0*		
	TTLTRG1*		
	TTLTRG2*		
	TTLTRG3*		
	TTLTRG4*		
	TTLTRG5*		
	TTLTRG6*		
	TTLTRG7*		
	EXT TRG A		
Breakpoint			

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73A-270 Test Record (Cont.)

Triggering & Breakpoint for Channel B		**Passed**	**Failed**
Trigger Lines	TTLTRG0*		
	TTLTRG1*		
	TTLTRG2*		
	TTLTRG3*		
	TTLTRG4*		
	TTLTRG5*		
	TTLTRG6*		
	TTLTRG7*		
	EXT TRG A		
Breakpoint			
External Clock & Transmission In Progress		**Passed**	**Failed**
External Clock	FAST EXT CLK		
	SLOW EXT CLK		
Transmission In Progress	Transmit in Progress A		
	Transmit in Progress B		

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Self Test

Following the VXIbus system startup sequence, the green PWR light on the 73A-270 front panel indicates that all power supplies are operational. If the +5 V, –5.2 V, –2 V, ± 24 V or the internally regulated ± 20.9 V buses fail, or if the –2 V, +5 V, –5.2 V, or ± 24 V fuses open, the PWR light will be off. Additionally, the FAILED light will be on and SYSFAIL* will be asserted indicating a module failure.

If any of the Mode or Resolution lights are on, it usually is an indication that the 73A-270 has not completed its initialization correctly. One typical reason for this condition is the FAST EXTERNAL CLOCK switch being in the external (C2) position.

NOTE. *If you experience any error indication from the Slot 0 Resource Manager, the 73A-270, or other VXIbus module, investigate and correct the problem before proceeding. Common items to check are logical address conflicts (primary and secondary; see Table A–3), breaks in the VXIbus daisy chain signals, improper seating of a module, loose GPIB cable.*

Performance Verification Tests

This procedure verifies the performance of the 73A-270. The test sequences contain setup instructions for the example equipment listed in Table A–1. You may use equipment other than the recommended examples if it meets the requirements listed. The order of the test sequences has been chosen to minimize system setup. Although not essential, it is recommended that you follow the order presented, as some tests rely on previously verified parameters. Before starting the the test sequence verify that the SLOW EXTERNAL CLOCK is in the OFF position and that the FAST EXTERNAL CLOCK is in the C1 position. Also, ensure that the INT LEVEL is set to the same level as the Slot 0 Commander module.

NOTE. All ASCII character string commands enclosed in quotes which are sent to the 73A-270 must be in UPPER CASE. *You may wish to leave your keyboard in the CAP LOCK mode.*

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VXIbus Interface

This sequence verifies that the 73A-270 configures correctly and communicates properly with your system controller.

Equipment Requirements	Oscilloscope (item 1) 50 Ω Coaxial Cable (item 5)
Prerequisites	All prerequisites listed on page 56

1. Send the appropriate commands to the Slot 0 device to get the primary/secondary GPIB address of the 73A-270, 73A-541, and VX4790A. Place these addresses into the IBCONF configurator for the VX270. VX541, amd VX4790A GPIB device.
2. Verify that the 73A-270 responds to setup commands with the following steps:
   a. Connect the 73A-270 TTL OUT A to Ch-1 of the oscilloscope (2 V/div, 250 ns/div, 1 MΩ input impedance).
   b. With the following commands, set the 73A-270 to the beginning of the address space, for the first List entry to have a duration of 500 ns (5×100 ns power-on default resolution) active high, for the second List entry to have an active low duration of 500 ns and to be designated as the Last Address, to transmit the list continuously, and finally to begin transmission of the last selected channel (in this case Ch A, the power-on default). Verify a 1 MHz 50% duty cycle pulse-pattern.

      `IBOC` (Start GPIB Talker/Listen/Controller program)

      ```
      IBFIND VX270
      ```

      ```
      IBRD 100
      ```
      (Observe 00 response)

      ```
      IBWRT "OA51L54LOCOB"
      ```
      (Observe 1 MHz square wave)

      ```
      IBWRT "Q"
      ```
      (Observe waveform stops)
3. To verify interrupt capability, set the 73A-270, to enable the transmit complete interrupt (XMIT), and to generate a burst of (63) pulses. Then read and verify a response of 02. This response means that there is no transmission in progress, that an interrupt has been generated due to transmission completion or breakpoint, that the memory is not busy, and that a Memory Busy Overwrite interrupt has not been generated. Following the read, the Slot 0 controller will be un-addressed and will acknowledge the interrupt as an SRQ pending.

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***NOTE**. Make sure the 73A-270 and the Slot 0 Resource Manager are set to the same INT LEVEL. Also, If an embedded controller is being used, follow the operating manual for displaying the state of the interrupt lines.*

```
IBWRT "1I63C0B"

IBRD 100
```
(Observe 02 response)

4. Check for VXIbus Request True event by performing a serial poll and verify that the response byte is

```
0x40 (decimal:64)
```
(i.e. DIO7 = 1)

```
IBRSP
```
(Observe 40 response)

TTL OUT A and B

This sequence verifies the time base resolution, the pulse duration multiplier, and the burst mode for the TTL OUT A and B signals. Complete all steps in this section for TTL OUT A and then repeat all steps for TTL OUT B.

Equipment Requirements	Oscilloscope (item 1) Counter/Timer (item 3) 50 Ω BNC Coaxial Cable (item 5)
Prerequisites	All prerequisites listed on page 56 All previous Performance Verification Tests

1. Connect the TTL OUT A (or TTL OUT B) output to Ch-1 of the oscilloscope (2 V/div, 1 ms/div, 1 MΩ input impedance).
2. Verify the time base resolution with the following steps:
   a. Select the channel to be tested:

```
IBWRT "0S" or IBWRT "1S"
```
(Select TTL OUT A or TTL OUT B)

   b. Set the 73A-270 for a 100 ns resolution and then to the beginning of the address space, for the first List entry to have a of 100 ns active high duration, for the second List entry to have a 100 ns active low duration and to be designated as the Last Address, to transmit the list continuously, and finally to begin transmission of the last channel selected. Verify a pulse duration of 100 ns ±10 ns.

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```
IBWRT "OROA11L14LOCOB"
```
(Observe 100 ns ±10 ns pulse width)

c. Verify the additional time base resolutions as directed in Table A–4

Table A–4: Time Base Resolution Verification

Command to Send	Pulse Width to Verify
`IBWRT "OROA11L14LOCOB"` (step 2b repeated for table continuity)	100 ns ±10 ns
`IBWRT "Q1ROB"`	1 µs ±10 ns
`IBWRT "Q2ROB"`	10 µs ±10 ns
`IBWRT "Q3ROB"`	100 µs ±10 ns
`IBWRT "Q"`	(Verify that the waveform stopped)

3. To verify the pulse duration multiplier, set the 73A–270 for a 100 ns resolution, to the beginning of the address space, for a first List entry of 100 µs active high, for a second List entry of 100 µs active low and designated as the Last Address, to transmit the list continuously, and finally to begin transmission of the last channel selected. Verify a 5 kHz ±0.5 Hz square wave.

```
IBWRT "OROA10001L10004LOCOB"
```
(Verify 5 kHz ±0.5 Hz)

4. Verify the additional pulse duration multipliers as directed in Table A–5

NOTE. *The last measurement in Table A–5 may require a Timer/Counter if you wish to verify the precise tolerances listed.*

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Table A–5: Pulse Duration Multiplier Verification

Command to Send	Multiplier / Resolution		Verify Period and Duty Cycle
IBWRT "0A0R10001L10004L0C0B" (step 3 repeated for table continuity)	1000	100 ns	5 kHz ±0.5 Hz, 50% ±0.1%
IBWRT "1R0A1001L1004L0C0B"	100	1 µs	5 kHz ±0.5 Hz, 50% ±0.1%
IBWRT "2R0A101L104L0C0B"	10	10 µs	5 kHz ±0.5 Hz, 50% ±0.1%
IBWRT "3R0A11L14L0C0B"	1	100 µs	5 kHz ±0.5 Hz, 50% ±0.1%
IBWRT "0A21L24L"	2	100 µs	2.5 kHz ±0.25 Hz, 50%
IBWRT "0R0A8585851L4242424L0C0B"	858585 high, 424242 low		85.8585 ms ±20 ns, 42.4242 ms ±20 ns

5. Verify the pulse-pattern burst count function with the following steps:

a. Connect the TTL OUT A or (TTL OUT B) to the counter/timer INPUT B input.

b. Set the 73A-270 for a 10 µs resolution, to first address location, to retriggerable mode, for a first List entry of 550 µs active high, and for a second list entry of 550 µs active low and designated as the Last Address.

```
IBWRT "Q"

IBWRT "2R0A0M551L554L"
```

c. Set the counter/timer for Basic Timer/Counter Measurement Mode, to Function Event Count B, for a Ch-B Trigger at 1 V, to Gate Indefinitely, and to return an Integer Format of maximum 2^{17}–1 value.

```
IBFIND VX541

IBWRT "ER"
(Query for any pending ERROR conditions)

IBRD 100
(Observe a 99 response; no ERRORs)

IBWRT "MM0;FN4;BT+100;BZ1;GI;IF17"

IBWRT "JM"
(Start the counter/timer measurement cycle)
```

d. Set the 73A-270 to generate the pulse-pattern List 42 times and to begin.

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```
SET VX270

IBWRT "42C0B"
```

e. Stop the counter/timer acquisition, read one response, and verify a return count of 42 events.

```
SET VX541

IBWRT "QM"

IBRD 100
```
(Observe return count of 42 events)

f. Repeat the burst test sending the data list 21 times.

```
IBWRT "JM"

SET VX270

IBWRT "21C0B"

SET VX541

IBWRT "QM"

IBRD 100
```
(Observe return count of 21 events)

6. This completes the TTL OUT signal test sequence. If you have not checked both channels of the 73A-270, repeat the sequence for the other channel.

BPLR OUT A and B

This sequence verifies the output voltage levels, polarity, and phase for the BPLR OUT A and BPLR OUT B signals. Complete all steps in this section for BPLR OUT A and then repeat all steps for BPLR OUT B.

Equipment Requirements	Oscilloscope (item 1) Counter/Timer (item 3) 50 Ω BNC Coaxial Cable, two required (item 5)
Prerequisites	All prerequisites listed on page 56 All previous Performance Verification Sequences

1. Connect the BPLR OUT A (or BPLR OUT B) to Ch-1 of the oscilloscope (50 Ω input impedance)

2. Connect the TTL OUT A (or TTL OUT B) of the 73A-270 under test to Ch-2 of the oscilloscope (1 MΩ input impedance)

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3. To verify the BPLR pulse-pattern phase and ±2 V accuracy, set the 73A-270 to generate a continuous pulse-pattern square wave from both the TTL and the BPLR outputs with a 10 µs period and a bipolar amplitude of ±2.0V. Check that the BPLR OUT signal is in phase with the TTL OUT signal and that the amplitude is ±2.0 V ±2 mV.

   ```
   SET VX270
   ```

   ```
   IBWRT "0S" or IBWRT "1S"
   ```
   (Select Ch-A or Ch-B)

   ```
   IBWRT "1R0A0C51L54L0B"
   ```

   ```
   IBWRT "20P-20N"
   ```
   (Verify ±2.0 V ±260 mV)

4. Reset 73A-270 for a BPLR OUT amplitudes of ±5.0 V and ±8.7 V and verify that the corresponding BPLR OUT signals are in phase with the TTL OUT signal and that the amplitude is within ±260 mV of the value set. Then change the polarity of the BPLR OUT signal and verify. Finally set the BPLR OUT signal to 0 V and verify.

   ```
   IBWRT "50P-50N"
   ```
   (Verify ±5.0 V ±260 mV)

   ```
   IBWRT "87P-87N"
   ```
   (Verify ±8.7 V ±260 mV)

   ```
   IBWRT "-87P87N"
   ```
   (Verify ±8.7 V ±260 mV and opposite polarity)

   ```
   IBWRT "00P00N"
   ```
   (Verify 0.0 V ± 260 mV)

   ```
   IBWRT "Q"
   ```
   (Verify that the pulse-pattern is stopped.)

5. The verification steps in this section should be performed for both BPLR OUT A and BPLR OUT B channels. If you have not tested both channels, repeat the steps in this section for the other channel.

Triggering, and Breakpoint Function

This sequence verifies the operation of the 73A-270 with the VXIbus TTL trigger lines (8), internal and external triggering and breakpoint recognition.

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Equipment Requirements	Oscilloscope (item 1) Counter/Timer (item 3) 50 Ω BNC Coaxial Cable, two required (item 5)
Prerequisites	All prerequisites listed on page 56 All previous Performance Verification Tests

1. Connect TTL OUT A to Ch-2 of the oscilloscope (1 MΩ input impedance).
2. To verify Ch-A operation with the VXIbus TTL trigger lines, Set the 73A-270 for Ch-A to generate a 500 kHz pulse-pattern triggered by an external trigger from TTLTRG0* and for Ch-B to provide the trigger pulse on TTLTRG0*. Verify a 500 kHz pulse-pattern and then stop the pattern.

   ```
   SET VX270

   IBWRT "O8X80T"

   IBWRT "1S3ROAOM51L54L1C"

   IBWRT "OS1ROA1M11L14LOC"

   IBWRT "1B"
   ```
   (Observe 500 kHz)

   ```
   IBWRT "Q"
   ```
   (Verify that the pulse-pattern stopped)
3. Check the remaining TTLTRG1* through TTLTRG7* lines by sending the commands in table A–6 and verifying a 500 kHz pulse-pattern.

Table A–6: VXIbus TTL Trigger Line Verification Ch. A triggered by Ch. B

TTLTRG Line	Change Setup, Restart Pattern, Verify 500 kHz Pulse-Pattern
TTLTRG1*	`IBWRT "18X81T"` `IBWRT "1B"` (Verify 500 kHz pulse-pattern.)
TTLTRG2*	`IBWRT "Q28X82T"` `IBWRT "1B"`
TTLTRG3*	`IBWRT "Q38X83T"` `IBWRT "1B"`
TTLTRG4*	`IBWRT "Q48X84T"` `IBWRT "1B"`
TTLTRG5*	`IBWRT "Q58X85T"` `IBWRT "1B"`

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Table A–6: (Cont.)VXIbus TTL Trigger Line Verification Ch. A triggered by Ch. B

TTLTRG Line	Change Setup, Restart Pattern, Verify 500 kHz Pulse-Pattern
TTLTRG6*	IBWRT "Q68X86T" IBWRT "1B"
TTLTRG7*	IBWRT "Q78X87T" IBWRT "1B"

4. Using the following commands, disable both channels from the TTLTRGX* lines and then resend the trigger pulse from channel B to restart the pulse-pattern from channel A. Check that channel A is not putting out a pulse pattern, and then stop the pulse-pattern:

```
IBWRT "Q88X88T"

IBWRT "1B"
```
(Verify no pulse-pattern from channel A)

```
IBWRT "Q"
```

5. Verify the EXT TRG A input with the following steps:

a. Connect TTL OUT B to EXT TRG A.

b. Restart both channels with the following command:

```
IBWRT "1B"
```

c. Verify a 500 kHz pulse pattern from channel A (triggered by channel B) and then stop the pattern.

```
IBWRT "Q"
```
(Verify that the pattern stopped)

d. Disconnect TTL OUT B from EXT TRG A.

6. Verify channel A breakpoint recognition with the following steps:

a. Set the 73A-270 to generate a continuous pulse pattern having a 10 ms active high level pulse with an active breakpoint followed by a 10 ms active low level pulse with an active breakpoint with the following commands:

```
IBWRT "OS3ROAOM1003L1006LOC"
```

b. Trigger the pulse-pattern and check that the TTL OUT A pulse-pattern is held at a TTL high level, confirming that the pattern stopped at the active high pulse breakpoint.

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```
IBWRT "0B"
```
(Verify a TTL high level)

c. Retrigger the pulse-pattern several times and check after each start that the TTL OUT A signal level alternates between a TTL low level and a TTL high level.

```
IBWRT "0B"
```
(Verify a TTL low level)

```
IBWRT "0B"
```
(Verify a TTL high level)

```
IBWRT "Q"
```
(Verify that the pulse-pattern stops)

7. Verify channel B operation with the VXIbus TTL Trigger Lines with the following steps:

a. Move the oscilloscope CH-2 coaxial cable from TTL OUT A to TTL OUT B.

b. Reset the 73A-270 for channel B to generate a 500 kHz pulse-pattern triggered by an external trigger from TTLTRG0* and for channel A to provide the trigger pulse on TTLTRG0*.

```
IBWRT "80X08T"

IBWRT "0S3R0A0M51L54L1C"

IBWRT "1S1R0A1M11L14L0C"

IBWRT "1B"
```

c. Verify a 500 kHz signal and then stop the pulse-patter:

```
IBWRT "Q"
```
(Verify that the pulse-pattern stopped)

d. Check the remaining TTLTRG1* through TTLTRG7* lines by sending the commands in table A–7 and verifying the 500 kHz pulse-pattern.

Table A–7: VXIbus TTL Trigger Line Verification Ch. B triggered by Ch. A

TTLTRG Line	Change Setup, & Restart Pattern
TTLTRG1*	`IBWRT "81X18T"` `IBWRT "1B"` (Verify a 500 kHz pulse–pattern.)
TTLTRG2*	`IBWRT "Q82X28T"` `IBWRT "1B"`

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Table A–7: (Cont.)VXIbus TTL Trigger Line Verification Ch. B triggered by Ch. A

TTLTRG Line	Change Setup, & Restart Pattern
TTLTRG3*	IBWRT "Q83X38T" IBWRT "1B"
TTLTRG4*	IBWRT "Q84X48T" IBWRT "1B"
TTLTRG5*	IBWRT "Q85X58T" IBWRT "1B"
TTLTRG6*	IBWRT "Q86X68T" IBWRT "1B"
TTLTRG7*	IBWRT "Q87X78T" IBWRT "1B"

e. With the following commands, disable both channels from the TTLTRGX* lines and restart the channel A pulse pattern. Verify that channel B is not putting out any pulse pattern, and then stop the pulse transmission:

```
IBWRT "Q88X88T"

IBWRT "1B"
```
(Verify that channel B is not putting out any pattern)

```
IBWRT "Q"
```

8. Verify the EXT TRG B input with the following steps:

a. Connect TTL OUT A to EXT TRG B. Restart both channels by sending:

```
IBWRT "1B"
```
(Verify a 500 kHz pulse-pattern)

b. Check that channel B is putting out a 500 kHz pulse pattern (triggered by channel A) and then stop the pattern by sending:

```
IBWRT "Q"
```
(Verify that the pattern stopped)

c. Disconnect TTL OUT A from EXT TRG B.

9. Verify channel B breakpoint recognition with the following steps:

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a. Program TTL OUT B to generate a continuous pulse pattern having a 10 ms active high level pulse with an active breakpoint followed by a 10 ms active low level pulse with an active breakpoint with the following steps:

```
IBWRT "1S3R0A0M1003L1006L0C"

IBWRT "0B"
```

b. Check that TTL OUT B is held at a TTL high level, which demonstrates that the pattern stopped at the active high pulse breakpoint.

c. Restart the pulse-pattern several times and check each time that the TTL OUT B signal level alternates between a TTL low level and a TTL high level as the breakpoints are being recognized.

```
IBWRT "0B"

IBWRT "0B"

IBWRT "Q"
```
(Verify that the pulse-pattern stopped)

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External Clock and Transmission In Progress

This sequence verifies the high and low speed external clock inputs and the Transmission In Progress signal inputs on the front panel DB-25 connector.

Equipment Requirements	Oscilloscope (item 1)
	Oscilloscope Probe (item 2)
	50 Ω BNC Coaxial Cable, two required (item 5)
	Arbitrary Waveform or Pattern Generator clock source (item 4)
	SMB to BNC Adapter Cable (item 6)
	BNC Female to BNC Female (item 7)
	BNC Male to Dual Binding Post Adapter (item 8)
	DB-25 connector with wires soldered to pins 4 & 5 (item 9)
Prerequisites	All prerequisites listed on page 56
	All previous Performance Verification Tests

1. Verify the Fast External Clock (250 kHz to 10 MHz) with the following steps:

a. Turn the mainframe power off and remove the 73A-270. Change the FAST EXTERNAL CLOCK switch from the C1 (internal) to the C2 (external) position. Return the 73A-270 to the mainframe and turn on the mainframe the power.

b. Connect TTL OUT A to Ch-1 of the oscilloscope (2 V/div, 100 µs, 1 MΩ input impedance).

c. Connect the Arbitrary Waveform Generator (AWG) ARB OUT to the 73A-270 Fast External Clock, pin 5 of S1 (front panel DB25, 5th pin up from bottom right) and pin 4 (4th pin up from bottom right, digital ground) using the SMB to BNC cable, the BNC barrel connector, the BNC dual binding post adapter, and two short pieces of 26 AWG jumper wire soldered to pins 4 and 5 of a male DB-25 connector.

d. Set the clock source (AWG) to generate a 1 MHz square wave.

```
IBFIND VX4790

IBWRT "SETSQUARE 0 2.5 1000000;10;T"
```

(The fourth parameter is numeric one followed by alphabetic O)

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e. Set the 73A-270 to divide the 1 MHz external clock source by 10 (10 µs resolution) and to set the pulse duration multiplier to 10 to generate a square wave with a 200 µs period (5 kHz) with the following steps:

```
SET VX270

IBWRT "OS1ROAOM101L104LOCOB"
```
(Verify 5 kHz waveform)

f. Momentarily disconnect the SMB connector from the VX4790A and check that the 5 kHz pulse pattern is no longer present on TTL OUT A.

2. Verify the Slow External Clock input with the following steps:

a. Turn the mainframe power off and remove the 73A-270. Return the FAST EXTERNAL CLOCK switch to the C1 position and change the SLOW EXTERNAL CLOCK switch to the ON (external) position. Replace the 73A-270 and turn the mainframe power on. Reconnect the coaxial cable to the TTL OUT A and the Arbitrary Waveform Generator (clock source) to pins 5 and 4 (GND) of S1.

b. Program the 73A-270 to select the 200 kHz external clock and to set its pulse duration multiplier to 20 to generate a 5 kHz square wave:

```
IBWRT "OSOROAOM201L204LOCOB"
```

c. Set the clock source to provide a 200 kHz square wave.

```
SET VX4790

IBWRT "SETSQUARE O 2.5 200000;10;T"
```
(Verify 5 kHz)

(The fourth parameter is numeric one followed by alphabetic O.)

d. Momentarily disconnect the SMB connector from the VX4790A and check that the 5 kHz pulse pattern is no longer present on TTL OUT A.

e. Using the oscilloscope probe, verify a 10 MHz clock signal on pin 17 of S1 (4th pin up from bottom left).

3. Verify the Transmission In Progress signal with the following steps:

a. Turn the mainframe power off and remove the 73A-270. Return the SLOW EXTERNAL CLOCK switch to OFF and verify that the FAST EXTERNAL switch is in the C1 position. Reinstall the 73A-270. and turn on the mainframe power. Reconnect the coaxial cable to TTL OUT A, and the external clock to S1 pins 5 and 4 (GND).

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b. Set the 73A-270 to generate a 500 Hz square wave and then stop the pulse pattern:

```
set VX270

IBWRT "OS3ROAOM101L104LOCOB"
```
(Verify a square wave)

```
IBWRT "Q"
```
(Verify no pattern)

c. Using the oscilloscope probe, check that S1 pin 2 (Transmission In Progress A, active high), is a TTL low level and that pin 3 (Transmission In Progress A, active low) is a TTL high level.

d. Restart the 500 Hz pulse pattern with the command below and check that pin 2 of S1 is now a TTL high level and pin 3 is a TTL low level.

```
IBWRT "OB"
```
(Check that pin 2 is high and pin 3 is low)

e. Move the coaxial cable to TTL OUT B. Program the 73A-270 to generate the 500 Hz pulse-pattern on TTL OUT B and then stop the pulse pattern:

```
IBWRT "1S3ROAOM101L104LOCOB"
```
(Verify a square wave)

f. Stop the pattern and again using the oscilloscope probe, check that Transmission In Progress B (active high), pin 12 of S1 (2nd down from top right,) is a TTL low level and that Transmission In Progress B (active low), pin 11 (3rd down from top right,) is a TTL high level.

```
IBWRT "Q"
```
(Verify no pattern and pin 12 is high and pin 11 is low)

g. Restart the 500 Hz pulse pattern and check that pin 12 of S1 is now a TTL high level and that pin 11 is a TTL low level.

```
IBWRT "1COB"
```
(Verify pin 12 is high and pin 11 is low)

This completes the 73A-270 verification procedure.

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Appendix E
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

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User-Replaceable Parts

Part Description	Part Number
User Manual	070-9148-XX
Label, Tek CDS	950-4523-00
Label, VXI	950-4522-00
Fuse, Micro 4 Amp 125 V Fast	159-0374-00
Fuse, Micro 1 Amp 125 V Fast	159-0116-00
Fuse, Micro 2 Amp 125 V Fast	159-0128-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-4174-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00

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