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User Manual

Tektronix

73A-451
Wire-Wrap Card with VXIbus Interface

070-9155-01



This document applies for firmware version 1.00
and above.

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Safety Summary

The general safety information in this summary is for both operating and servicing personnel. Additional specific warnings and cautions are found throughout the manual where they apply, and may not appear in this summary.

TERMS

In This Manual

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to the module or other property.

Marked on the Module

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the module itself.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.



This symbol indicates where special explanatory information is included in the manual. There is no caution or danger associated with the information.

Marked on the Module



DANGER — High Voltage.



Protective ground (earth) terminal.



ATTENTION — Refer to the manual.



Refer to manual before using.

Power Source

This module is intended to operate in a mainframe whose power source does not apply more than 250V rms between the supply conductors or between either supply conductor and ground. A protective ground connection through the grounding conductor in the power cord(s) is essential for safe operation.

Grounding the Module

This module is grounded through the grounding conductor of the mainframe power cord(s). To avoid electrical shock, plug the mainframe power cord(s) into a properly wired receptacle before connecting to the module connectors. A protective ground connection through the mainframe is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only fuses specified in the module parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications required for the fuse that it replaces.

Do Not Operate in Explosive Atmosphere

To avoid explosion, do not operate the module in an explosive atmosphere.

Do Not Remove Covers or Panels

To avoid personal injury, the module covers should be removed only by qualified service personnel. Do not operate the module without covers and panels properly installed.

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DESCRIPTION

INTRODUCTION

The 73A-451 Wire-Wrap Module is a printed circuit board assembly for use in a card cage conforming to the VXIbus Specification, such as the 73A-021 used in the CDS 73A IAC System. The 73A-451 includes standard VXIbus Message Based device interface circuitry which allows you to develop functions and/or interfaces unique to your own requirements without having to first design a VXIbus interface. Approximately 66 square inches of board space is available for user designed circuitry.

In addition to the power and EMI filtering required by the VXIbus standard, the circuitry provided includes two logical address switches, a VMEbus interrupt level select switch, a halt switch, and provisions for user-installed voltage regulators and VXIbus CLK10 receivers. The voltage regulators allow development of unique supply voltages (such as ±15V) not provided by the VXIbus standards.

The 73A-451 is fully compatible with the VXIbus specifications for message-based devices, and supports word serial protocol. As a VXIbus servant (slave) interface, it will handshake using Normal Transfer Mode. The Module supports the following VXIbus commands: BYTE AVAILABLE (with or without END bit set), BYTE REQUEST, BEGIN NORMAL OPERATION, READ PROTOCOL, IDENTIFY COMMANDER, CLEAR, and TRIGGER. It can also support the following VXIbus Protocol Events: UNRECOGNIZED VXIbus COMMAND, and REQUEST TRUE.

The CDS provided circuitry meets or exceeds all VXIbus power, cooling, emissions, and susceptibility specifications. Mounting holes are provided for user supplied shields, as required by application and/or VXIbus Standard.

Note that certain terms used in this manual have very specific meanings in the context of a VXIbus System. These terms are defined in the VXIbus Glossary (Appendix C).

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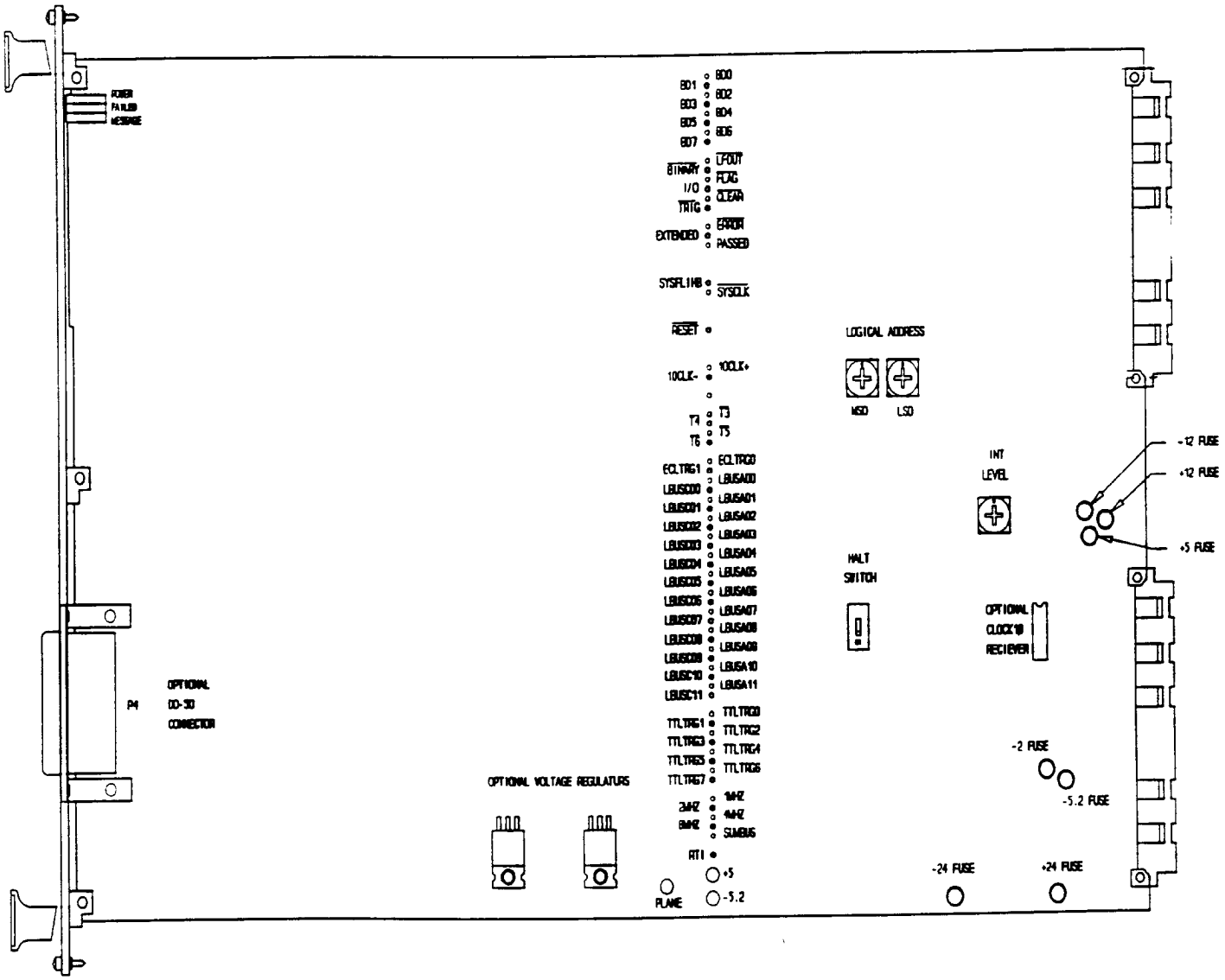


Figure 451-1: 73A-451 Controls and Indicators

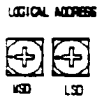
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CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 73A-451 Module's operating environment. See Figure 451-1 for their physical locations.

- **Switches**

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the 73A-451 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position to the white mark on the side of the switch.

The actual physical address of the 73A-451 module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the 73A-451 will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the 73A-451 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program the module. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the 73A-451 is being used in a CDS IEEE-488 IAC system, consult the operating manual of the CDS 73A-151 RM/488 Interface Module.

If the 73A-451 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC). This algorithm is described in detail in the 73A-151 Operating Manual.

If the 73A-451 is not being used in a CDS IAC System, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the module's logical address.

VMEbus Interrupt-Level-Select Switch



Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander (for example, the 73A-151 RM/IEEE-488 Interface module in a CDS 73A-IBX System). The VMEbus interrupt level on which the 73A-451 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position to the arrow on the module shield.

Valid interrupt-level-select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the 73A-451's interrupt handler, typically the module's commander. Setting the switch to an invalid

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commander. Setting the switch to an invalid interrupt level (0, 8, or 9) will disable the module's interrupts. When using the 73A-451 in a CDS 73A-IBX System, set the interrupt level to the same level chosen on the 73A-151.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

Halt Switch



This two-position slide switch selects the response of the 73A-451 Module when the RESET bit in the module's VXIbus CONTROL register is set.

If the Halt Switch is in the ON position, the 73A-451 Module is reset to its power-up state and all programmed module parameters are reset to their default values when the RESET bit is set in the module's control register.

If the Halt Switch is in the OFF position, the module will ignore the RESET bit and no action will take place.

NOTE: The module is not in strict compliance with the VXIbus specification when the HALT switch is OFF.

Control of the RESET bit depends on the capabilities of the 73A-451's commander. In a CDS 73A-IBX System, for example, the RESET bit is set if the 73A-151 RM/IEEE-488 Interface Module receives a STOP command via the IEEE-488 bus.

- **Fuses**

Each of the 73A-451's power buses is protected with an on-board fuse to protect other modules within the VXIbus chassis if an inappropriate voltage is applied to this module's front panel connector. The fuse also protects the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

If any of the fuses open, the SYSFAIL* (system failure) line on the VXIbus backplane will be asserted. If the +5V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on this module to disable SYSFAIL*.

The 73A-451 Module has fuses for +5V, -5.2V, -2V, +24V, -24V, +12V, and -12V.

If any of the fuses open, remove the fault before replacing the fuse. The fuses are in sockets, and are removed by pulling them straight away from the board.

- **LEDs**

The following LEDs are visible at the top of the 73A-451 Module's front panel to indicate the status of the module's operation:

Power LED

This green LED is normally on. It is extinguished if any of the monitored power voltages have failed due to an open fuse or a backplane power bus problem. The power voltages monitored are +5V, +12V, -12V, +24V, -24V, -5.2V and -2V. If the optional regulators for +15V and -15V have been installed, jumper M1 may be installed to monitor these voltages also.

Failed LED

This normally off red LED is lit if any of the monitored power voltages fails (see Power LED above) or if the user signal PASSED is false (low).

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NOTE: Either failed power or a false PASSED signal will cause the module to assert the VXI backplane signal SYSFAIL* until or unless the mainframe resource manager sets the SYSFAIL Inhibit bit in the 73A-451's control register. The Failed LED will remain lit independent of the state of the SYSFAIL Inhibit bit.

MSG LED

This green LED is normally off. When lit it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a 5 microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

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SPECIFICATIONS

Function:	Allows creation of special circuits for a VXIbus system.
Circuitry Provided:	VXIbus Message Based device interface to P1 Connector to support the Word Serial Protocol. EMI power bus filtering, power bus fuses (+5, -5.2 ±24, ±12, -2 Volt power supplies), buffered clocks.
User Interface:	
Signal Characteristics: Outputs:	HCT or LSTTL drivers for all outputs from the CDS provided circuitry.
Inputs:	No more than 2 LSTTL loads on any input to the CDS provided circuitry from the user's circuitry.
Termination:	8-bit data bus lines are pulled up with 3.3K ohms to +5V.
VXIbus Compatibility:	Provided VXIbus interface is fully compatible with the VXIbus Specification for Message Based instruments with the Halt Switch in the ON position.
VXIbus Interface:	
Device Type:	VXI Message Based Instrument, Word Serial protocol, VXI Servant (Slave) Interface.
Data Transfer Handshake:	Normal Transfer Mode.
Data Transfer Capability:	A16, D16 circuitry provided.
Interrupt Levels:	Circuitry provided for VXI Interrupter capability, switch selectable for levels 1 (highest priority) through 7 (lowest).
Interrupt Acknowledge:	D16, lower 8 bits returned are the logical address of the module, upper 8 bits are the VXIbus defined event codes.
Buffered Clocks Available:	16, 8, 4, 2, and 1 MHz phase coherent TTL clocks. Optional 10 MHz ECL clock with IC pads wired for MC10H116 Buffer.
MODID Line:	Terminated in 825 Ohms.
Other VXIbus Signals Available:	Local Bus A and C, TTL and ECL trigger lines and SUMBUS.
Module-Specific Commands:	All module-specific commands and data are sent via the VXIbus Byte-Available command.

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VXIbus Data Rate:

The CDS designed interface is capable of speeds in excess of 1 Mbyte per second. The interface requires 375 ns to return DTACK* on any VXIbus cycle.

VXIbus Commands Supported:

All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command Event:

BYTE AVAILABLE (with or without END bit set)
BYTE REQUEST
BEGIN NORMAL OPERATION
READ PROTOCOL
CLEAR
TRIGGER

VXIbus Protocol Events Supported:

VXIbus events are returned via VME interrupts. The following events are supported and returned to the 73A-451 module's commander:

UNRECOGNIZED VXIbus COMMAND
REQUEST TRUE (In IEEE-488 systems such as the 73A-IBX, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.

VXI EMI Shielding:

Mounting holes provided for user supplied shields as may be required by application and/or VXIbus Standard.

Power Requirements:

All required dc power is provided by the Power Supply in the VXIbus card cage.

Current (Peak Module, I_{PM}):

The total I_{PM} for the module is dependent on the circuitry added by the user. The I_{PM} of the provided CDS circuitry is 1.15 A. When circuit design is complete, make an estimate of module I_{PM} to assure compatibility with the card cage being used.

Current (Dynamic Module, I_{DM}):

The total I_{DM} for the module is dependent on the circuitry added by the user. The I_{DM} of the provided CDS circuitry is less than one milliamp. When circuit design is complete, make an estimate of module I_{DM} to assure compatibility with the card cage being used.

Power Available to User:

Voltage	Current*
+5 Volts	2.75 Amperes (fused for 4 Amps)
-5.2 Volts	0.8 Amperes (fused for 4 Amps)
-2 Volts	0.33 Amperes (fused for 2 Amps)
+24 Volts	0.5 Amperes (fused for 1 Amp)
-24 Volts	0.5 Amperes (fused for 1 Amp)
+12 Volts	0.8 Amperes (fused for 1 Amp)
-12 Volts	0.8 Amperes (fused for 1 Amp)

*Indicated currents are nominal, based on use of a CDS 73A-021 Card Cage and an even distribution of available card cage power

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	across all card slots. Individual currents may be exceeded on an application-specific basis, subject to total power availability of the card cage power supply.
User Power Busses:	Power busses run horizontally from front to rear of the card. Eight (8) power/ground bus pairs, jumper selectable for +5 Volts or -5.2 Volts; six (6) single power busses, jumper selectable for ±12 Volts, ±24 Volts, +5 Volts, -5.2 Volts, or 2 Volts. Refer to the Installation section for information on installing jumpers.
User Voltage Regulators:	Pads are provided for installation of voltage regulators from the 78XX and 79XX family of positive and negative regulators in TO-220 packages to develop user-specific supply voltages such as ±15V. The regulators are driven from the VXIbus ±24V supplies.
User Circuit Space:	Eight layer board with a total of sixty-six (66) square inches of user space, including 5.5 square inches for pin grid array style parts, consisting of a hole pattern on 0.1 inch grid spacing to allow installation of wire wrap sockets or other components.
Cooling:	When properly mounted in a 73A-021 card cage, up to 35 Watts of power may be dissipated on the card.
VXIbus Cooling Specification:	An airflow of 0.08 liters/sec/watt will provide an air temperature of ambient plus 10 °C. The CDS portion of the module will generate about 8 watts. Add in the heat generated by the user's circuitry to calculate whether the card cage being used will provide sufficient cooling. For a fully populated module with front and back shields installed, a typical pressure drop is 0.04 mm of H_2O.
Temperature:	-10 °C to +65 °C, operating (assumes ambient temperature of 55 ° and airflow to assure less than 10 °C temperature rise). -40 °C to +85 °C, storage.
Humidity:	Less than 95% R.H. non-condensing, -10 °C to +30 °C. Less than 75% R.H. non-condensing, +31 °C to +40 °C. Less than 45% R.H. non-condensing, +41 °C to +55 °C.
VXI Mainframe Slots:	One (1) slot if point to point wiring method is used. If wire wrap pins are used, two (2) slots, blank slot to left.
Front Face Plate:	Supplied with solid one wide or two wide (1.2" or 2.4") face plate with ejector handles. Two wide panel installed.
Card Size:	VXIbus C sized card, 9.187 inches x 13.3858 inches (233.35 mm. x 280 mm.).
Option 001:	One wide (1.2") front face plate with one uncommitted DD-50P connector installed. Requires mating 73A-780S Connector Assembly.

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Option 002:	Two wide (2.4") front face plate with one uncommitted DD-50P connector installed. Requires mating 73A-780S Connector Assembly.
Radiated Emissions:	CDS portion of the card complies with VXIbus Specification.
Conducted Emissions:	Complies with VXIbus Specification. All busses have filtering for currents up to the rating of their circuit breaker.
Module Envelope Dimensions:	VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in)
Dimensions, Shipping:	When ordered with a CDS card cage, this module will be installed and secured in two adjacent instrument module slots (slots 1 - 12). When ordered alone, the module's shipping dimensions are: 406 mm x 305 mm x 102 mm. (16 in x 12 in x 4 in).
Weight:	0.6 kg. (1.25 lb).
Weight, Shipping:	When ordered with a CDS card cage, this module will be installed and secured in two adjacent instrument module slots (slots 1-12). When ordered alone, the module's shipping weight is: 1 kg. (2.25 lb).
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus card cage. (Refer to D size card cage manual for information on required adapters.)
Front Panel Signal Connectors:	If Option 001 or 002 is ordered with the 73A-451, a 50 pin (DB 50P) connector is installed on the module.
Recommended Cable:	If Option 001 or 002 is ordered, the CDS 73A-742S Data Cable may be used with the 73A-451.
Equipment Supplied:	1 - 73A-451 Module.
Optional Equipment:	1 - 73A-780S Hooded Connector.

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EMC Compliance: This product, as provided, complies with the following standards:

EN 55011 Class A

EN 50081-1
EN 60555-2

EN 50082-1
IEC 801-2
IEC 801-3
IEC 801-4
IEC 801-5

Since this product is a prototyping module in which the end user may install their own circuitry, Tektronix, Inc. assumes no responsibility for compliance to these standards once modifications have been made. It is the responsibility of the purchaser of this product to assure compliance with any required EMC regulations.

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INSTALLATION

INSTALLATION REQUIREMENTS AND CAUTIONS

The 73A-451 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus card cage slot or pair of slots other than slot 0. The 73A-451 Module requires one or two slots, depending on whether the provided one-wide or two-wide front panel is installed. If the module is being installed in a D size card cage, consult the operating manual for the card cage for installation information. Setting the module's Logical Address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the 73A-451 Module's logical address.

CAUTION:

To avoid confusion, it is recommended that the slot number and the logical address be the same.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

CAUTION:

Note that there are two ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector labeled "73A-451" is at the top.

CAUTION:

In order to maintain proper card cage cooling, unused card cage slots must be covered with blank front panels supplied by the card cage manufacturer. Based on the number of IAC Modules ordered with a CDS card cage, blank front panels are supplied to cover all unused slots.

CAUTION:

Verify that the card cage is able to provide adequate cooling and power for the 73A-451 Module. Refer to the card cage Operating Manual for instructions on determining cooling and power compatibility.

INSTALLATION PROCEDURE

CAUTION:

The 73A-451 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the module's user assigned Revision Level, Serial Number, and switch settings on the Installation Checklist. Only qualified personnel should install the 73A-451 Module.

2) Verify that the Logical Address and Interrupt Level switch are switched to the correct value. The Halt switch should be in the ON position unless it is desired to not allow the resource manager to reset this module.

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Note that with either Halt Switch position, a "hard" reset will occur at power on and when SYSRESET* is set true on the VXIbus backplane. If the Module's commander is a CDS 73A-151 RM/488 Interface Module, SYSRESET* will be set true whenever the Reset Switch on the front panel of the 73A-151 is depressed. Also note that when the HALT switch is in the OFF position, the module is not in strict compliance with the VXIbus Specification.

3) The module can now be inserted into any slot or pair of slots of the chassis other than slot 0.

CAUTION:

If the 73A-451 module is inserted in a slot with any empty slots to the left of the module (as, for example, when the CDS-provided two-wide (2.4") front panel is used), the VME daisy-chain jumpers must be installed on the backplane of the VXIbus card cage in order for the 73A-451 Module to operate properly. This will be required, for example, in the slot to the left of the primary 73A-451 if installed with a two wide front panel (2.4"). Check the manual of the card cage being used for jumpering instructions.

If a CDS 73A-021 Card Cage is being used, the jumper points may be reached through the front of the Card Cage. There are five (5) jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

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INSTALLATION CHECKLIST

Installation parameters may vary depending on the card cage being used. Be sure to consult the card cage Operating Manual before installing and operating the 73A-451 Module.

Revision Level: _____

Serial No.: _____

Card Cage Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Halt Switch: _____

73A-742S Cable installed (if used): ___

73A-780S Hooded Connector installed (if used): ___

Performed by: _____ Date: _____

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OPERATION

OVERVIEW

The 73A-451 Module is programmed by 8-bit wide characters issued from the system controller to the 73A-451 module via the VXIbus card cage backplane. The module is a VXIbus Message Based instrument and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the 73A-451 Module's commander for details on the operation of that device.

If the Module is being used in a CDS 73A-IBX System card cage, the module's commander will be the 73A-151 Resource Manager/IEEE-488 Interface Module. Refer to the 73A-151 Operating Manual for information on how the system controller communicates with the 73A-151.

POWER-UP

The 73A-451 Module must set the PASSED bit in its Status register and be ready for programming within five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay to this power-up delay.

The CDS portion of the circuit does not have a self-test. The user's circuit may or may not implement a self-test. If the user's circuit will take longer than five seconds for self-test, the VXIbus extended self-test protocol must be implemented. A high true signal line is provided that must be driven to indicate the completion of self-test. (See the information on the Passed Signal in the Interface Operation section of this manual.)

SYSTEM COMMANDS

Although these non-data commands are initiated by the 73A-451's commander (for example, the 73A-151 Module in a CDS 73A-IBX System) rather than the system controller, they have an effect on the 73A-451 Module. Some of the commands will affect the CDS provided circuitry and some will be passed to the user's circuit. The following VXIbus Instrument Protocol Commands will affect the 73A-451:

Command	Effect
Clear	A signal to user's circuit to clear its VXIbus interface and any pending commands. Current module operations are unaffected.
Trigger	This signal may be used to trigger functions.
Begin Normal Operation	The CDS circuit will begin operations.
Read Protocol	The CDS circuit will return its protocol to its commander.

DATA COMMANDS

Command	Effect
Byte Available	The CDS circuit will pass the 8-bit data byte to the user's circuit. When the user's circuit indicates the data has been accepted, the CDS circuit will set Write Ready, permitting the 73A-451's commander to write another command to the 451.

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Byte Request

The CDS circuit will begin a read of the user's circuit. When it responds, the CDS circuit will set the Read Ready bit of the response register, permitting the 73A-451's commander to read the data.

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INTERFACE OPERATION

The CDS circuit on the 73A-451 Module provides a fully functional VXIbus Message Based device interface to support the Word Serial Protocol. With a proven interface to the VXIbus, you can concentrate design efforts on your particular instrumentation or functional needs. The CDS provided circuit has two interfaces: the VXIbus interface and the user interface. The VXIbus Local Busses A and C, as well as the Trigger lines (both ECL and TTL), are brought out to the wire-wrap area.

All VXIbus signals in this section are referred to by name rather than pin number. Appendix D lists the signal names with their pin numbers for both P1 and P2. The non-VXIbus signals that are provided are described in the User Interface subsection. All user signals are identified by name on both sides of the printed circuit board in a highly visible white silkscreen. All power and ground busses are also high-lighted and identified on the board.

VXIBUS INTERFACE

The CDS provided interface to the VXIbus complies with the VXIbus Specification. The VXIbus interface is a slave only, permitting design of a VXIbus servant. All switches needed to support selection of a logical address for the module and to select a VME interrupt level for the interface to send VXIbus events on are included in the VXIbus interface. The VXIbus interface also includes a HALT switch that permits the user to isolate the RESET bit in the control register, preventing a software reset to the module. If the 73A-451 Module is used in a CDS 73A-IBX configured system, the 73A-151 in that system supports a command to set the RESET bit on any module in the card cage.

The VXIbus interface will generate the Unrecognized Command, Internal Error and Request True VXIbus events. The Unrecognized Command event is generated automatically by the VXIbus interface if an unrecognized VXIbus Word Serial Protocol command is received. The Request True and Internal Error events are generated under command of the user's circuit through the user interface.

USER INTERFACE

The user interface of the 73A-451 Module is a set of signals brought out to the edge of the wire-wrap area. The signals are divided into three groups:

- signals the user interfaces to support the Word Serial protocol. These signals are similar to most data transfer busses, consisting of a bi-directional data bus and a control bus.

- signals that the user's circuit may or may not make use of. These include the Local Busses, the Trigger lines, the Sumbus, and decoded VXIbus commands such as Trigger.

- signals that make circuit design easier. These include the phase coherent clocks, line-feed detect and the T state signals.

The signals available at the user interface and their descriptions are as follows:

BD0, BD1, BD2, BD3, BD4, B45, BD6, BD7
These are buffered bi-directional data lines that correspond with D0 through D7 on the VXIbus backplane. BD0 is the least significant bit and BD7 the most significant bit. When data is written to

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the 73A-451 by its commander, the data on the buffered bus is guaranteed to be true 62 nsec. prior to the leading edge of T3*. When data is being read from the 73A-451 Module, the user's circuit must have the data true for 25 nsec. prior to the trailing edge of FLAG* and hold the data for 0 nsec after the trailing edge of FLAG*. The buffered data bus is true high.

LFOUT*

This is a low true signal that provides automatic decoding of linefeeds (0Ah) written to the user's circuit. LFOUT* is true at least 62 nsec prior to the leading edge of T3*. This signal is always false (high) if BINARYL* is true.

BINARYL*

This is a low true signal that the user's circuit must control to signal the VXIbus interface that linefeeds should not be decoded. This signal is used for sending or receiving non-ASCII 8 bit data to the 73A-451. This signal will also suppress the automatic generation of the END bit in a Byte Request response when a line-feed is returned by the 73A-451 in response to a Byte Request command. BINARYL* must be true prior to the bus cycle during which line-feeds or the END bit are to be suppressed. This means that you must anticipate the need to suppress the line-feed or the END bit.

FLAG*

This is a low true signal that the user's circuit must control. It signals the VXIbus interface that the user's circuit has completed a cycle with the interface. The user's circuit must assert FLAG* (drive it to a low) before T6*'s trailing edge. It is recommended that FLAG* be asserted by the occurrence of T3*.

The user's circuit should not release FLAG* (let it return to a high) until the circuit is ready to process another VXIbus cycle. On the trailing edge of FLAG*, the interface will set either its Write Ready or Read Ready bits in its response register, signifying to the 73A-451 Module's commander that the Module is ready to resume VXIbus activity.

If the cycle has been a read cycle, the CDS interface will latch the data from the user's circuit into the Datalow register of the VXIbus interface on the trailing edge of FLAG*. (Refer to the description of the buffered data bus for setup and hold times required of the data.) The user's circuit may hold FLAG* active for as long as is necessary. FLAG* being active prevents the VXIbus interface from accepting another Byte Request or Byte Available command. (Refer to Figures 451-2 for a timing diagram of a read and write transaction.) FLAG* must also be set true for at least 62 nsec. if the CLEAR* signal (described below) goes true (low).

I/O This signal indicates the direction of the current backplane cycle. I/O is true for 62 nsec. prior to the leading edge of T3* and remains true through the trailing edge of FLAG*. The state of I/O at other times is undefined. A low is data going to the module (VXIbus write to the 73A-451) and high is data coming from the module (VXIbus read of the 73A-451).

CLEAR*

This is a 125 nsec. low true pulse controlled by the CDS circuit. When the module receives a VXIbus Clear command, it must reset its VXIbus interface, clear any unexecuted commands in its input buffer and clear its output buffer. FLAG* must be set true for at least 62 nsec. in response to the CLEAR* signal.

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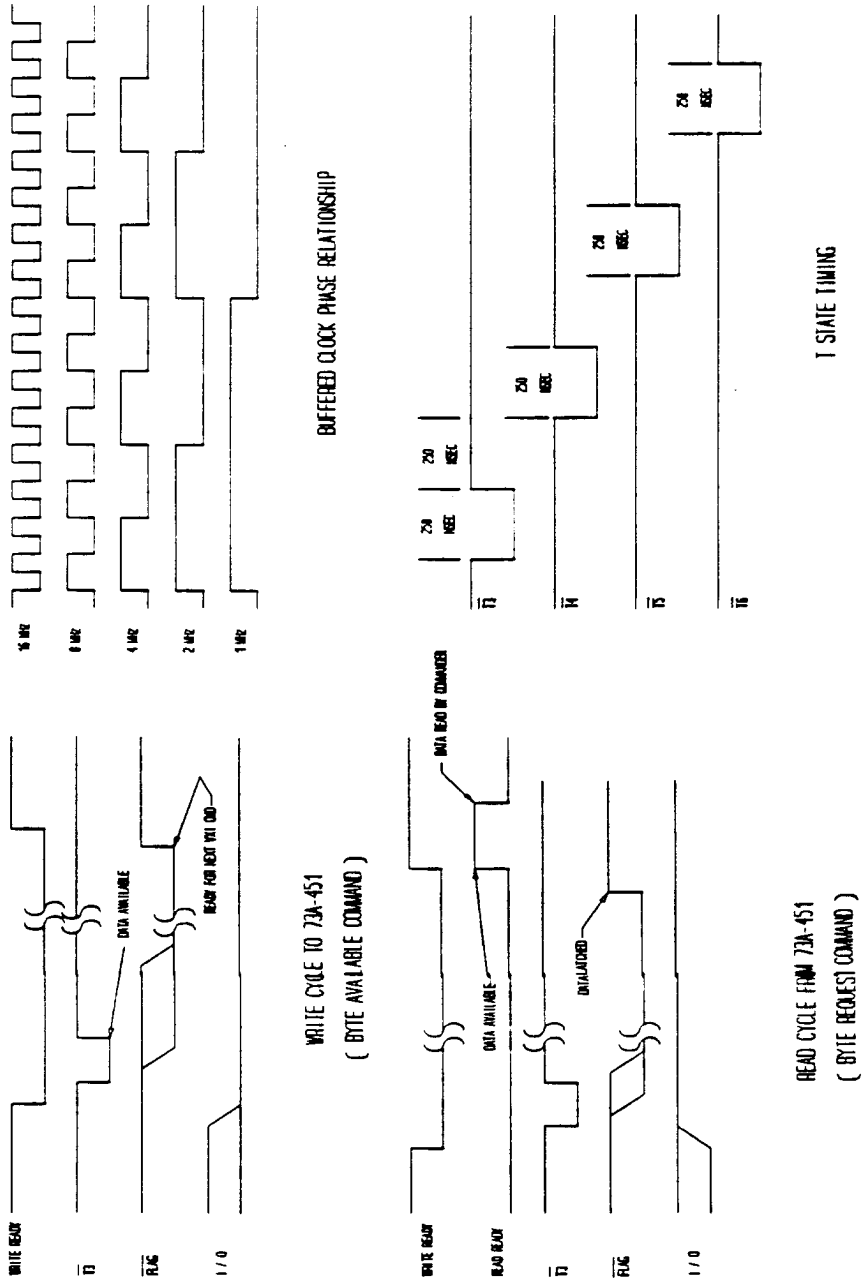


Figure 451-2: Timing Diagrams; Read and Write Transactions

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TRIG*

This is a 125 nsec. low true pulse that indicates to the user's circuit that a VXIbus Trigger command has been received by the interface.

ERROR*

This is a low true signal driven by the user's circuit to cause the VXIbus interface to generate an Internal Error event. ERROR* must be active for at least 62 nsec., then may be de-asserted.

EXTENDED

This is a high true signal driven by the user's circuit to inform the VXIbus Resource Manager that the Module is in Extended self-test. If the user's circuit implements a self-test that lasts longer than 5 seconds, this signal must be true before 5 seconds have elapsed. It is returned false when the user's circuitry completes extended self-test. If no self-test is implemented, this signal may be left open, and will be pulled high by the 73A-451's VXIbus interface.

PASSED

This is a high true signal that the user's circuit must drive when self-test is complete. When this signal is inactive, the signal will drive the backplane signal SYSFAIL* active unless Sysfail Inhibit is set by the card cage's resource manager (the 73A-151 in a CDS card cage). This signal must be driven true (high) during an extended self-test.

If no self-test is implemented, the signal should be left unconnected, since a CDS pull-up resistor is provided.

SYSFAIL INHIBIT

This is a high true signal to the user's circuit that indicates that the SYSFAIL* Inhibit bit in the control register has been set by the resource manager.

RESET*

This a low true signal used to reset the user's circuit. This signal will go active if the VXIbus signal SYSRST* or the RESET bit in the 73A-451's control register goes active. To defeat the RESET bit in the control register, the HALT switch should be OFF. The SYSRST* signal may not be defeated. If RESET* is asserted by the reset bit in the control register, it is guaranteed to be true for at least 100 microseconds. If it is asserted by the VXIbus signal SYSRST*, the time that it is true is undefined. It is recommended that the user's circuit be capable of resetting itself within 1 microsecond. Most microprocessors will reset properly in 1 microsecond or less.

10CLK+, 10CLK-

To use the 10 MHz differential ECL clock on the backplane, install U1091, a 10H116 IC, with its terminating resistors and decoupling capacitors. The differential output of the 10H116 will appear on 10CLK+ and 10CLK-. The user-installed components required to activate the 10CLK+ and 10CLK- circuitry are further described in the CLK10 paragraph of the Special Features section.

T3*,T4*, T5*, T6*

These are low true non-overlapping timing signals that the user's circuit may use for processing data cycles. The T3* signal along with the I/O signal indicates that the module has been addressed and a data input or output transfer started. For an output operation (BYTE AVAILABLE) command, T3* should be used to decode data (BD0-BD7) sent to the module. For an input operation (BYTE REQUEST command followed by a data low read) to the module, T3* is a request for data to be placed on the data lines (BD0-BD7).

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The additional T4*, T5* and T6* signals are particularly useful if the user's circuitry is a state machine. Each signal is a 250 ns low pulse with a 250 ns gap between each T signal. These signals will start at the beginning of a data cycle and occur once per cycle. If the user's circuit asserts and deasserts FLAG* prior to T6*, the interface will stop generating the T signals. (Refer to Figure 451-2 for a timing diagram of these signals.)

ECLTRGx

The two ECL triggers defined by the VXIbus Specification are brought out to the wire-wrap area of the module. The CDS interface has no signal conditioning on these two signals. If used, they must be properly terminated in the user's circuitry. Refer to the VXIbus Specification for various protocols that may be implemented.

LBUSAx

The twelve Local Bus A signals are brought to the wire-wrap area of the module. The CDS interface does not affect these signals. You should be aware of the optional VXIbus definition for keying on modules that access the local busses. If you decide not to add the mechanical keys to the module's front panel, it is recommended that another keying scheme be implemented, such as color coding. This will provide some protection from accidental damage to modules due to local bus incompatibility.

LBUSCx

The twelve Local Bus C signals are brought to the wire-wrap area of the module. The CDS interface does not affect these signals. Refer to the LBUSAx description about keying the module.

TTLTRGx

The eight TTL Trigger lines defined by the VXIbus Specification are brought to the wire-wrap area of the module. The CDS interface does not affect these signals. Refer to the VXIbus Specification for various protocols that may be implemented.

SYSCLK, 1MHZ, 2 MHZ, 4 MHZ, 8 MHZ

These buffered clocks are phase coherent. (Refer to Figure 451-2 for the phase relationship.) SYSCLK is the 16 MHz VMEbus signal and has wide variations on its duty cycle. This is due to backplane delays and reflections. All other clocks have a 50% duty cycle. Absolute accuracy of the frequency of these clocks is governed by the accuracy of the slot 0 device driving the SYSCLK signal. Refer to the operating manual of the slot 0 device. In a CDS 73A-IBX System, for example, this would be the 73A-151 Resource Manager/IEEE-488 Interface Module.

RFI*

This active low pulse is controlled by the user's circuit to generate a VXIbus Request True event. This event will result in the SRQ line being set active in an IEEE-488 system. The leading edge of RFI* will generate a Request True event. RFI* should be set true when the module requires service. The minimum pulse active time is 62 nsec.

SUMBUS

This is the VXIbus signal defined as an analog current driven bus. You must follow all VXIbus rules for use of the SUMBUS, including over-voltage protection and over-current protection. See the VXIbus Specification for specific SUMBUS design requirements.

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SYSFAIL, SELF TEST, AND INITIALIZATION

The CDS provided portion of the 73A-451 module does not execute a self test. If a self-test function is desired, the following discussion is a recommendation by CDS on how the self-test should be implemented in the VXIbus environment.

The module should execute a self-test at power-up, upon a VXIbus hard or soft reset condition, or upon a user-defined self-test command. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the 73A-451's commander, sets the RESET bit in the 73A-451's control register. Either of these conditions will cause the RESET* signal on the user interface to go active for as long as either condition exists. The duration of SYSRST* is indeterminate. The duration of the RESET bit being asserted is at least 100 microseconds long.

Reset Self-Test

During a power-up, or hard or soft reset, the following actions take place:

1) If the module executes a self-test, the user PASSED signal must be false (zero), setting the SYSFAIL* (VME system-failure) line active, indicating that the module is executing a self test. The board FAILED LED is lit.

2) If the self test completes successfully, the user's circuit asserts the user PASSED signal. The VXIbus interface will release the SYSFAIL* line and the interface becomes active. The communications registers will be active and ready for normal operation. SYSFAIL* must be released by the user PASSED signal within five seconds in normal operation. If the self-test lasts longer than five seconds, the PASSED and EXTENDED user signals must be asserted.

   If the self-test fails, the SYSFAIL* line must remain active (accomplished by leaving PASSED low), and the module should make an internal record of what failure(s) occurred. It then enters the VXIbus FAILED state, which allows an error message to be returned to the module's commander.

Commanded Self-Test

It should also be possible to invoke a self-test at any time during normal operation by using a device dependant command (TEST<CR><LF>, for example). SYSFAIL* must not be asserted during a commanded self-test. If SYSFAIL* is asserted, the 73A-451's commander will start system failure diagnostic activity in an attempt to determine which module is pulling SYSFAIL*. If the 73A-451's commander does not know that a self-test was commanded, system recovery may be attempted when none is desired. At the end of a commanded self-test, the module should be restored to its pre-test state.

SYSFAIL* Operation

SYSFAIL* becomes active during power-on, hard or soft reset, self-test, or if one of the module's power voltages is interrupted. SYSFAIL* may also be set by deasserting the PASSED signal. When the card cage Resource Manager detects SYSFAIL* set, it will attempt to set SYSFAIL* Inhibit in the 73A-451's control register. This will cause the 73A-451 module to deassert SYSFAIL* in all cases except for loss of +5V power.

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SPECIAL FEATURES

The special features described below give the 73A-451 Module added capability, increasing design possibilities and making the design process easier.

FREE AREA

An area is provided in the upper left corner of the board which has no power or ground busses in it. This area allows the use of at least two Pin Grid Array (PGA), Leadless Chip Carrier (LCC) or Plastic Leadless Chip Carrier (PLCC) integrated circuits, as long as the chip's pins or its socket's pins are on a 0.1 inch grid. Any square chip less than 1.3 inches per side will fit in this area.

POWER BUSSES

You must choose which voltage, +5V or -5.2V, is required on the power plane under the wire-wrap area. The voltage chosen will be available on the busses labeled PWR. The jumper selecting +5V or -5.2V is located on the lower middle edge of the board. Use at least 22 ga. wire for this jumper, since up to 4 amperes may be flowing through the jumper. Refer to Figure 451-3 and the 73A-451 schematic.

There are six individually configurable busses into the wire-wrap area that must be jumpered. All seven VXIbus voltages are available and marked at the right end of each bus. Select which voltage is required on a bus by bus basis and install the appropriate jumper. Refer to Figures 451-1, 451-4, and the 73A-451 schematic.

USER INSTALLED CIRCUITS

Since additional voltages may be required, other than those defined by the VXIbus Specification, two pads for voltage regulators are provided. The pads are set up for regulators of the 78XX and 79XX family of positive and negative regulators in TO-220 packages. Component locations for decoupling capacitors and dropping resistors are available. Input to the regulators is the 24V busses. The output of the regulators may be jumpered to any of the user definable busses. Use the four holes marked +15V and -15V to access the output of the regulators. Refer to Figure 451-5, the 73A-451 schematic, and the assembly drawing for component installation.

Recommended Components:

Ref. Desig.	Component Type	Mfg.	Mfg. Pt. No.
Q1461	78XX	Nat.	78XX
Q1462	79XX	Nat.	79XX
C1461	22µf tantalum	Sprague	199D226X9025CA1
C1462	0.1µf ceramic	Sprague	92C20Z5U104M050B
C1463	22µf tantalum	Sprague	199D226X9025CA1
C1464	0.1µf ceramic	Sprague	92C20Z5U104M050B
C1581	0.33µf ceramic	AVX	SR215E334MAA
C1582	0.33µf ceramic	AVX	SR215E334MAA
R1573, 4,5,6	10Ω, ½W carbon comp.	any	

If regulators for other than ±15V are installed and you want them to be automatically monitored the same as the 73A-451 monitors the VXI power, install jumper M1 and replace the following components with ¼ Watt 5% carbon composition or film resistors as shown:

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for ±12V: R1471 = 10 K Ω
R1378 = 2.7 K Ω
R1374 = 10 K Ω (standard value)

for ±5V: R1471 = 2.7 K Ω
R1378 = 3.9 K Ω
R1374 = 6.8 K Ω

Contact the factory for information on using other voltages, mixed voltages, or monitoring a single voltage.

CLK10

The VXIbus defined ECL 10 MHz clock is brought into a component location that is defined to hold a 10H116 ECL differential receiver chip. There are also locations for decoupling capacitors and 50 ohm terminating resistors. Refer to Figure 451-1, the 73A-451 schematic, and the assembly drawing for component installation.

Recommended Components:

Ref. Desig.	Component Type	Mfg.	Mfg. Pt. No.
U1091	10H116	Moto.	M10H116
C1292	0.1μf ceramic	Sprague	9C20Z5V104M050B
C1291	0.1μf ceramic	Sprague	9C20Z5V104M050B
R1292	50Ω ¼W carbon comp.	any	
R1293	50Ω ¼W carbon comp.	any	

DD-50 CONNECTOR

The 73A-451 Module has a component location for a single DD-50P at the lower front panel. The connector and a front panel with a cutout for the connector may be purchased from CDS. There are two front panels available. Option 001 is a one wide (1.2 inches) front panel with connector and Option 002 is a two wide (2.4 inches) front panel with connector. CDS also has a 73A-742S 48 conductor cable available for use with the DD-50P connector. Refer to Figure 451-1 for connector placement.

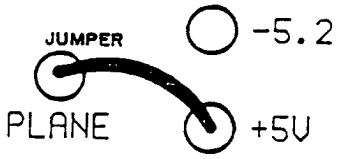


Figure 451-3: Example: Jumper of Power Plane to +5V

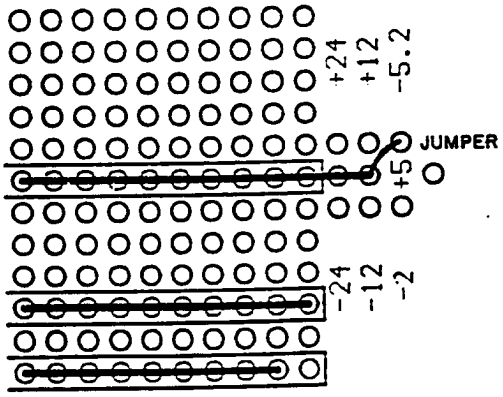


Figure 451-4: Example: Jumper to -5.2V

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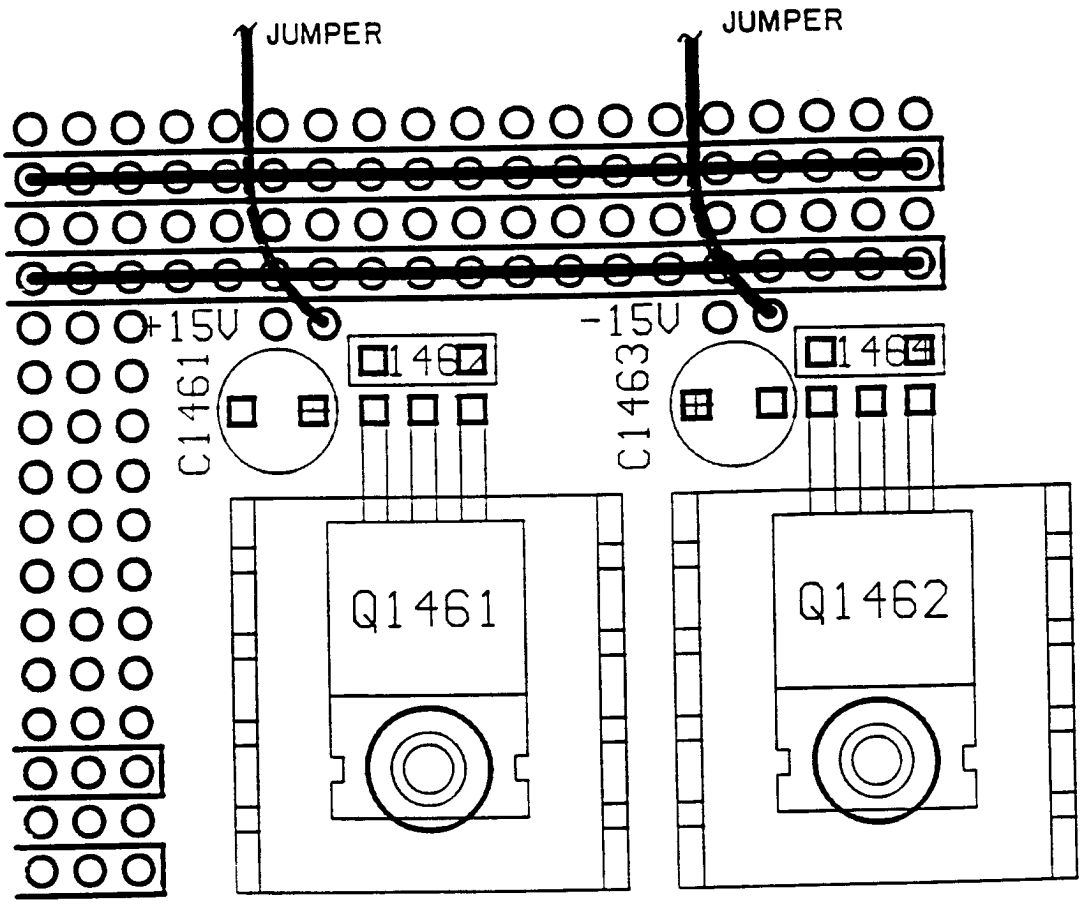


Figure 451-5: Jumpers (To Any User Definable Bus)

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APPENDIX A - VXIbus OPERATION

The 73A-451 Module is a C size single slot VXIbus Message-Based Word Serial device. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The 73A-451 Module is neither a VXIbus commander nor a VMEbus master, and therefore it does not have a VXIbus signal register. The 73A-451 is a VXIbus message based servant.

The module supports the Normal Transfer Mode of the VXIbus, using the Write Ready and Read Ready bits of the module's Response register.

A Normal Transfer Mode Read of the 73A-451 module proceeds as follows:

1. The commander reads the 73A-451's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready bit until it becomes true.

2. The commander writes the Byte Request command (0DEFFh) to the 73A-451's Data Low register.

3. The commander reads the 73A-451's Response register and checks if the Read Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Read Ready bit until it becomes true.

4. The commander reads the 73A-451's Data Low register.

A Normal Transfer Mode Write to the 73A-451 module proceeds as follows:

1. The commander reads the 73A-451's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready bit until it becomes true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX depending on the state of the End bit) to the 73A-451's Data Low register.

The 73A-451 module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the data low register, the response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the 73A-451's address space may cause incorrect operation of the module.

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APPENDIX B - POWER BUDGET WORKSHEET

The system designer must use the power budget worksheet to determine the operating parameters of the 73A-451 Module. The worksheet is preconfigured for using the 73A-451 Module in a CDS 73A-021 VXIbus card cage.

Voltage	Current Used	Current Available	Card Cage Budget	Power
+5 V	1.15*	4.0		
-5.2 V		4.0		
-2 V		2.0		
+24 V		1.0		
-24 V		1.0		
+12 V		1.0		
-12 V		1.0		
			Total Power for entire module**	

* +1.15 A represents the CDS circuitry only. Be sure to add in any additional current that the user's interface consumes.

** Must be less than 35 W.

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APPENDIX C - VXIbus GLOSSARY

Certain terms used in this manual have very specific meanings in the context of a VXIbus System. A list of these terms is presented below.

Commander

A VXIbus device that has bus master capability and has VXIbus servants under it in the system hierarchy. A commander may be a servant as well.

Fast Handshake

Compared to the Normal Transfer Mode of the VXIbus, the Fast Handshake Transfer Mode reduces the number of VMEbus data transfer cycles by 50%. Upon receipt of a request for data, a fast handshake module is able to return data in less than 20 µs, so that the VXIbus fast handshake word serial polling protocol can be used by the module's commander. Using fast handshake protocol, data can be written and read without checking the ready bits in the module's response register.

Hard Reset

This is the state of the module when the SYSRESET* line is true. While in this state, the module is inactive and its status and control registers are cleared. The SYSFAIL* line is driven low, and the failed LED is lit. In the case of a CDS 73A-IBX Card Cage, for example, a module hard reset occurs when the card cage is powered-up or the reset switch on the front panel of the 73A-151 Resource Manager/IEEE-488 Interface Module is depressed.

Interrupt Handler

The module in the VXIbus system that generates the hardware interrupt acknowledge for a particular VME interrupt level. The software interrupt handler may or may not be on the same module as the hardware interrupt handler. In the case of CDS instrument modules, both the hardware and software interrupt handlers reside on the commander module of a given servant module.

Logical Address

A unique 8 bit number which identifies each VXIbus device in a system. It defines the device's A16 register addresses, and indicates the device's commander/servant relationship.

Reset Bit

Bit 0 in the Control register of a module. When set to a one (1) by the module's commander or resource manager, the device is forced into a reset state.

Resource Manager

A message based commander located at logical address 0, which provides configuration management services, including address map configuration, commander/servant mapping, self test, and diagnostic management. In CDS systems, the Resource Manager function is co-located with the VMEbus controller, the slot 0 timing functions, and the system controller interface.

Servant

A VXIbus device that may or may not have bus master capability, that is under control of a commander in the VXIbus system hierarchy. A servant may also be a commander.

Soft Reset

This state is entered when the reset bit in the module's control register is set to one (1) by the module's commander. While in this state a device is inactive,

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interrupts which are pending are un-asserted, all pending bus requests are un-asserted, and the onboard processor is halted. While in this state the device's VMEbus slave interface is active; however, the device is incapable of responding to any commands other than reset and SYSFAIL INHIBIT. In the case of a CDS 73A-IBX Card cage, for example, a module soft reset occurs when the card cage's 73A-151 Resource Manager/IEEE-488 Interface Module receives a STOP command over the IEEE-488 bus that is addressed to the 73A-451.

SYSFAIL INHIBIT

Bit 1 in the Control register of a module. When set to a one (1) by the VXIbus Resource Manager, the device is disabled from driving the SYSFAIL* line. CDS modules are designed so that the SYSFAIL INHIBIT bit will work under all conditions except when the +5V power is lost.

VXI Commands

These are commands passed from a commander to a servant within the VXIbus environment. A command may or may not be stimulated by an external event. For example, an IEEE-488 Group Execute Trigger will generate a trigger command to all addressed devices. However, a Begin Normal Operations command is generated by the VXIbus resource manager and has no external source.

VXI Events

Events are passed from a servant to a commander. They may be generated by the servant either in response to a command (for example, unrecognized command event) or due to a condition detected in the module (internal error).

VXI Message Based Instrument

An intelligent instrument that implements the defined VXIbus registers and, at a minimum, the word serial protocol. All CDS instruments are message based.

VXI Word Serial Protocol

The simplest required communication protocol supported by Message Based devices in a VXIbus system. It utilizes the A16 communications registers to transfer data using a simple polling handshake method. All CDS instruments implement the word serial protocol.

488-VXIbus Interface

An IEEE-488 to VXIbus Interface Device is a message based device which provides communication between the IEEE-488 bus and VXIbus instruments.

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APPENDIX D - VXIbus CONNECTIONS

P1 CONNECTOR PINOUTS

Pin No.	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK*	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STBY	+12V
32	+5V	+5V	+5V

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P2 CONNECTOR PINOUTS

Pin No.	Row A	Row B	Row C
1	ECLTRG0	+5V	CLK10+
2	-2V	GND	CLK10-
3	ECLTRG1	RSV1	GND
4	GND	A24	-5.2V
5	LBUSA00	A25	LBUSC00
6	LBUSA01	A26	LBUSC01
7	-5.2V	A27	GND
8	LBUSA02	A28	LBUSC02
9	LBUSA03	A29	LBUSC03
10	GND	A30	GND
11	LBUSA04	A31	LBUSC04
12	LBUSA05	GND	LBUSC05
13	-5.2V	+5V	-2V
14	LBUSA06	D16	LBUSC06
15	LBUSA07	D17	LBUSC07
16	GND	D18	GND
17	LBUSA08	D19	LBUSC08
18	LBUSA09	D20	LBUSC09
19	-5.2V	D21	-5.2V
20	LBUSA10	D22	LBUSC10
21	LBUSA11	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID	D31	GND
31	GND	GND	+24V
32	SUMBUS	+5V	-24V

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Appendix E
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

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User-Replaceable Parts

Part Description	Part Number
User Manual	070-9155-XX
Label, Tek CDS	950-3749-00
Label, VXI	950-5062-00
Fuse, Micro 4 Amp 125 V Fast	159-0374-00
Fuse, Micro 2 Amp 125 V Fast	159-0128-00
Fuse, Micro 1 Amp 125 V Fast	159-0116-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00

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Appendix F
Options

Option 01

This option adds a front panel DD-50P connector to the 73A−451. A single wide front panel with a cut out for the connector replaces the standard front panel.

Option 02

Option 02 to a 73A−451 Module adds a front panel DD-50P connector. A double-wide front panel with a cut-out for the connector replaces the standard front panel.

Option 03

Option 03 to a 73A−451Wire Wrap Card substitutes a DB-25P connector for the optional P4 and includes a double wide (2.44 inch) face plate. The 25-pin male D-Connector is mounted at the P4 location on the printed circuit board. The wire wrap locations of P4 do not match the pin-out of the DB-25P. The table below shows the connections between the DB-25P connector and the printed circuit wire wrap locations.

P4 DB-25P	PC Card Wire Wrap Location	P4 DB-25P	PC Card Wire Wrap Location
1	20	14	37
2	21	15	38
3	22	16	39
4	23	17	40
5	24	18	41
6	25	19	42
7	26	20	43
8	27	21	44
9	28	22	45
10	29	23	46
11	30	24	47
12	31	25	48
13	32		

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Option 20

Option 20 to a 73A−451 VXIbus Prototyping Module adds RF shields to both sides of the module.

User-Replaceable Parts

Part Description	Part Number
Shield, Back	950-5697-00
Shield, Rear	950-7439-00
Screw, Phillips Metric 2.5 × 10 CSK Oval	950-1081-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00
Standoff Hex M2.5 × 19.5 MM	950-4051-00
Standoff Hex M2.5 thru × .538L	950-5688-00

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