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Data Timing Generator

▶ **DTG5078 • DTG5274 • DTG5334**



New serial data standards, expanding networks and ubiquitous computing continually redefine the cutting-edge of technology. The design engineer is challenged to economize without sacrificing performance.

The DTG5000 Series combines the power of a data generator with the capabilities of a pulse generator in a versatile, bench-top form factor, shortening the duration of complex test procedures and simplifying the generation of low-jitter, high-accuracy clock signals, parallel or serial data across multiple channels. Its modular platform allows you to easily configure the performance of the instrument to your existing and emerging needs to minimize equipment costs. Three mainframes and five plug-in output modules combine to cover a range of applications from legacy devices to the latest technologies. In addition, eight low-current, independently-controlled DC outputs can substitute for external power supplies. Each mainframe incorporates a full compliment of auxiliary input and output channels to easily integrate with other instruments, such as oscilloscopes and logic analyzers, to create a flexible and powerful lab.

▶ Features & Benefits

Versatile Platform Combines Features of Data Generator, Pulse Generator and DC Source

Up to 3.35 Gb/s Data Rate

From 1 to 96 Data Channels (Master/Slave)

Class-leading Delay Resolution of 0.2 ps (DTG5274/DTG5334), 1 ps (DTG5078), Up to 600 ns of Total Delay

Modular Architecture Helps to Protect Your Investment and Allows the Instrument to Expand with Your Growing Needs

Advanced Control Over Signal Parameters to Meet Most Current Testing Needs, Including Stressed Eye Generation
- External Jitter Injection (DTGM31, DTGM32 Modules)
- Level Control with 5 mV Resolution

Easy to Use and Learn Shortens Time to Test
- Easily Configure with Plug-in Modules
- Intuitive Windows User Interface
- Bench Top Form Factor
- Integrated PC Supports Network Integrationand Built-in CD-ROM, LAN, Floppy Drive, USB Ports

Up to 64 Mb Pattern Depth per Channel for Complex Data Patterns

▶ Applications

Semiconductor Device Functional Test and Characterization
- Support for Semiconductor Technologies from TTL to LVDS
- Initial Verification and Debugging, Comprehensive Characterization, Manufacturing and Quality Control

Compliance and Interoperability Testing to Emerging Standards
- PCI-Express Gen1:2.5 Gbps
- Serial ATA Gen1/2:1.5 Gbps/ 3 Gbps
- InfiniBand 2.5 Gbps
- XAUI: 3.125 Gbps
- HDMI: Version 1.3/DVI

Magnetic and Optical Storage Design
- Research, Development and Test of Next-generation Devices (HDD, DC/DVD, Blue-ray)

Data Conversion Device Design
- Characterization and Test of Next-generation D/A Convertors

Imaging Sensor Device Design
- Characterization and Functional Testing of Next-generation D/A Converters

Jitter Transfer and Jitter Tolerance Testing

Tektronix
Enabling Innovation

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▸ Characteristics

Mainframe Characteristics

Basic Features

Platform –
Benchtop mainframe with cold swappable plug-and-play plug-in output modules. Mainframes accept any combination of output modules.

Number of Slots for Output Modules –
DTG5078: 8 slots (A, B, C, D, E, F, G, H).
DTG5274: 4 slots (A, B, C, D).
DTG5334: 4 slots (A, B, C, D).

Master-Slave Capabilities –
DTG5078: Up to three DTG5078 mainframes can be connected in Master-Slave configuration.
DTG5274: Up to two DTG5274 mainframes can be connected in Master-Slave configuration.
DTG5334: Up to two DTG5334 mainframes can be connected in Master-Slave configuration.

Operating Modes –
Pulse Generator Mode (slots A to D only).
Data Generator Mode.

Output Patterns –
NRZ, RZ, R1, Pulse patterns (DTG5078/5274/5334: Slot A-D; DTG5078 Slot E-H, NRZ only).

Timing Parameters

Data Rate Range –
- DTG5078:
  - NRZ: 50 Kb/s to 750 Mb/s.
  - RZ, R1, Pulse Mode: 50 Kb/s to 375 Mb/s.
- DTG5274:
  - NRZ: 50 Kb/s to 2.7 Gb/s.
  - RZ, R1, Pulse Mode: 50 Kb/s to 1.35 Gb/s.
- DTG5334:
  - NRZ: 50 Kb/s to 3.35 Gb/s (settable to 3.4 Gb/s).
  - RZ, R1, Pulse Mode: 50 Kb/s to 1.675 Gb/s (settable to 1.7 Gb/s).

Data Rate (setting) Resolution –
Internal Clock : 8 digits.
External Clock : 4 digits.
External Phase Lock In : 4 digits.

Output Timing Controls

Delay Range –
PG Mode: 0 to 3 µs.
DG Mode:
- Long Delay Off: 0 to 5 ns (NRZ, RZ, R1).
- Long Delay On: NRZ:
  - Period ≥1.25 ns: 0 to 300 ns (Hardware sequence) or to 600 ns (Software sequence).
  - Period <1.25 ns: 0 to (240 ns x period) (Hardware sequence) or to (480 ns x period) (Software sequence).
- Long Delay On: RZ/R1:
  - Period ≥2.5 ns: 0 to 300 ns (Hardware sequence) or to 600 ns (Software sequence).
  - Period <2.5 ns: 0 to (120 ns x period) (Hardware sequence) or to (240 ns x period) (Software sequence).

Delay Resolution –
DTG5078: 1 ps.
DTG5274/DTG5334: 0.2 ps.

Phase Resolution – 0.1%.

Differential Timing Offset Feature (between pair of two adjacent channels (Odd and Even)) –
Range: –1 to 1 ns.
Resolution:
- DTG5078: 1 ps.
- DTG5274/DTG5334: 0.2 ps.

Semiautomatic Deskew Calibration –
Range: 500 ps.
Accuracy (after skew calibration):
- 100 ps, slots A to D.
- 200 ps, slots E to H (DTG5078 only).

Duty Cycle Adjustment Range –
0 to 100% (with 0 delay setting, RZ, R1, Pulse mode only).

Duty Cycle Adjustment Resolution – 0.1%.

Pulse Width Maximum Range –
290 ps to (period to 290 ps) (RZ, R1, Pulse mode only). (Range also depends on delay settings.)

Pulse Width Resolution – 5 ps.

Jitter Performance (output channels)

Clock Pattern ("1010..." clock pattern).

Random Jitter –
DTG5078: <4 ps_{RMS} (at 750 Mb/s with DTGM21, 0.8 V_{pk-pk}, delay: 0 ns).
DTG5274: <3 ps_{RMS} (at 2.7 Gb/s with DTGM30, 0.8 V_{pk-pk}, delay: 0 ns).
DTG5334: <3 ps_{RMS} (at 3.35 Gb/s with DTGM30, 0.8 V_{pk-pk}, delay: 0 ns).

Data Pattern (PRBS pattern 2^{15}-1)

Total Jitter –
DTG5078: at 750 Mb/s.
- <18 ps_{RMS}, <85 ps_{pk-pk} (typical) with DTGM21, 0.8 V_{pk-pk}, delay: 0 ns).

DTG5274: at 2.7 Gb/s.
- <16 ps_{RMS}, <60 ps_{pk-pk} (typical) with DTGM30, 0.8 V_{pk-pk}, delay: 0 ns).
- <14 ps_{RMS}, <60 ps_{pk-pk} (typical) with DTGM31, 0.8 V_{pk-pk}, delay: 0 ns).

DTG5334: at 3.35 Gb/s.
- <15 ps_{RMS}, 50 ps_{pk-pk} (typical) with DTGM30, 0.8 V_{pk-pk}, delay: 0 ns).
- <13 ps_{RMS}, 50 ps_{pk-pk} (typical) with DTGM31, 0.8 V_{pk-pk}, delay: 0 ns).
- <44 ps_{pk-pk} with DTGM30, Delay: 0 ns, Amplitude = 0.4 V_{pk-pk}, Offset = 0 V, Data Format = NRZ, Jitter Mode = Off, an ambient temperature of 20 to 30 °C.

Signal Control Features

Cross-point Adjustment (duty cycle distortion) –
Range: 30% to 70%.
Resolution: 1%.
(Slots A to D, and DTGM30/DTGM31/DTGM32 used in NRZ mode.)

Jitter Generation –
Jitter All or Partial Pattern.
Jitter Profile: Sine, Gaussian Noise, Square, Triangle.
Jitter Freq./Res.: 0.015 Hz to 1.56 MHz/1 MHz.
Jitter Amplitude: Up to 16.5 UI_{pk-pk} (depending on data rate and jitter frequency).
(Internal Jitter Generation available on Channel A1 only.)

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▸ Maximum Number of Output Channels

Number of Like Mainframes	DTG5078*1			DTG5274, DTG5334*1		
	DTGM21	DTGM30	DTGM31/DTGM32	DTGM21	DTGM30	DTGM31/DTGM32
1	32	16	3	8	8	4
2	64	32	6	16	16	8
3	96	48	9	—	—	—

*1 The DTG5078 has a limit to the number of modules that may be installed; the total must be less than 100. The coefficient for each module is shown below. DTGM30: 8, DTGM21: 10, DTGM31: 33, DTGM32: 32.

Pulse and Data Features

Pulse Generator (PG) Features (unique to PG mode) –
Continuous or Burst.
Burst Count: 1 to 65,536.
Pulse Rate: Off, 1/1, 1/2, 1/4, 1/8, 1/16.

Data Patterns

Pattern Length per Channel (Pattern Memory) –
Minimum:
- DTG5078: 1 bit (software mode) or 240 bits (hardware mode).
- DTG5274 / DTG5334: 1 bit (software mode) or 960 bits (hardware mode).

Maximum:
- DTG5078: 8,000,000 bits.
- DTG5274: 32,000,000 bits (in multiples of four).
- DTG5334: 64,000,000 bits (in multiples of four).

Built-in Data Patterns –
Binary Counter, Johnson Counter, Graycode Counter, Walking Ones, Walking Zeros, Checker Board, User-defined Patterns.

Pattern Import Capability –
Type/Tools:
- Tektronix TLA Data Exchange Format File (*.txt).
- Tektronix HFS Vector File (ASCII) (*.vca).
- Tektronix HFS Vector File (binary) (*.vcb).
- Tektronix AWG2000 Series (*.wfm).
- Tektronix AWG400s/500s/610/710/710B (*.pat).
- Tektronix DG2000 Series (*.dat).

Medium/Pass:
- Import data via GPIB, LAN, CD-ROM, floppy drive, USB memory devices.

Pattern Copy and Paste Capability –
Copy, paste and rotation between data listing/waveform editor and spreadsheet software (e.g., Excel) via clipboard.

PRBS/PRWS Data Patterns –
(Note: memory supports PRBS/PRWS patterns and user can create errored PRBS).
2^5–1, 2^6–1, 2^7–1, 2^8–1, 2^9–1, 2^{10}–1, 2^{11}–1, 2^{12}–1, 2^{13}–1, 2^{14}–1, 2^{15}–1, 2^{23}–1.

Sequencer Features

Sequence Length –
1 to 8,000 steps for main sequence.
1 to 256 steps for sub-sequence.
Max. Number of Blocks – 8,000.
Max. Number of Sub-sequences – 50.
Repeat Counter – 1 to 65,536 or infinite.
Channel Addition – AND or XOR (slots A to D only).
Note: DTG5078 slots E, F, G, and H do not support the following: RZ, R1, pulse generation modes which includes controls for trail delay/duty cycle/pulse width, channel addition and variable cross-points.

Auxiliary Channels

Clock Out

Connector –
Complementary output (common offset and ground).
- DTG5078/DTG5274: SMA rear panel.
- DTG5334: SMA front panel.

Frequency Range –
DTG5078: 50 kHz to 750 MHz.
DTG5274: 50 kHz to 2.7 GHz.
DTG5334: 50 kHz to 3.35 GHz, settable up to 3.4 GHz.

Frequency Resolution – 8-digit setting resolution.
Minimum: 1 mHz (e.g., with 50 kHz setting).
Internal Clock Accuracy – Within ±1 ppm.
Jitter –
DTG5078: <2 ps_{RMS} at 750 Mb/s, at 0.8 V_{pk-pk} (typical).
DTG5274: <2 ps_{RMS} at 2.7 Gb/s, at 0.8 V_{pk-pk} (typical).
DTG5334: <2 ps_{RMS} at 3.35 Gb/s, at 0.8 V_{pk-pk} (typical).
Amplitude/Resolution –
0.03 V_{pk-pk} to 1.25 V_{pk-pk}/10 mV (50 Ω).
0.06 V_{pk-pk} to 2.5 V_{pk-pk}/10 mV (1 MΩ).
Output Voltage Window –
–2 to 2.47 V (50 Ω).
–2 to 7 V (1 MΩ).
Max. Output Current – ±80 mA.
Transition Times (20% to 80%) –
DTG5078:
- <85 ps (Amplitude = 0.1 V_{pk-pk}, Offset = 0 V) (typical).
- <100 ps (Amplitude = 1 V_{pk-pk}, Offset = 0 V) (typical).

DTG5274:
- <70 ps (Amplitude = 0.1 V_{pk-pk}, Offset = 0 V) (typical).
- <80 ps (Amplitude = 1 V_{pk-pk}, Offset = 0 V) (typical).

DTG5334:
- <100 ps (Amplitude = 1 V_{pk-pk}, Offset = 0 V) (typical).

Overshoot –
<10%, at High = 1 V, Low = 0 V into (50 Ω) (typical).

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Other Output Channels
Auxiliary DC Outputs –
–3 to 5 V/10 mV, Max. current: ±30 mA, 8 independently controlled outputs, Connector: 2 x 8 pin header on front panel.
Sync Out –
CML (Current Mode Logic), VOH: 0 V , VOL: –0.4 V (50 Ω) (typical), SMA Connector, SE, Front panel, Rise/Fall Time (20 to 80%): 140 ps, Delay to Data Out: –4.5 ns (typical).
10 MHz Reference Out –
1.2 $V_{pk\text{-}pk}$ (50 Ω, AC coupled) (typical), 2.4 $V_{pk\text{-}pk}$ (1 MΩ, AC coupled) (typical), BNC Connector, Rear Panel.

Input Channels
External Clock In –
Input Ranges:
DTG5078: 1 MHz to 750 MHz. SMA Connector, Rear Panel.
DTG5274: 1 MHz to 2.7 GHz. SMA Connector, Rear Panel.
DTG5334: 1 MHz to 3.35 GHz. SMA Connector, Front Panel.
0.4 $V_{pk\text{-}pk}$ to 2 $V_{pk\text{-}pk}$ (50 Ω, AC Coupled), 50% ±5% duty cycle.
10 MHz Reference In –
Input Ranges:
10 MHz ±0.1 MHz, 0.2 $V_{pk\text{-}pk}$ to 3 $V_{pk\text{-}pk}$ (50 Ω, AC coupled), BNC Connector, Rear Panel.
Phase Lock In –
Input Ranges:
1 MHz to 200 MHz, 0.2 $V_{pk\text{-}pk}$ to 3 $V_{pk\text{-}pk}$ (50 Ω, AC coupled), BNC Connector, Rear Panel.
Skew Cal In –
Single-ended, ECL (into 50 Ω to –2 V), SMA Connector, Front Panel.
Trigger In –
Input Ranges:
–5 V to 5 V (50 Ω), 0.1 V resolution, –10 V to 10 V (1 kΩ), Min. 0.5 $V_{pk\text{-}pk}$ (50 Ω), 1 $V_{pk\text{-}pk}$ (1 kΩ), Min. 20 ns pulse width, Positive or Negative edge trigger, Delay timing: See manuals, BNC Connector, Front Panel.
Event In –
Input Ranges:
–5 V to 5 V (50 Ω), 0.1 V resolution, –10 V to 10 V (1 kΩ), 0.1 V resolution, Min. 0.5 $V_{pk\text{-}pk}$ (50 Ω), 1 $V_{pk\text{-}pk}$ (1 kΩ), Polarity: Normal or Invert, Delay timing: See manuals, BNC Connector, Front Panel.

Instrument Control/ Data Transfer Ports
GPIB –
GPIB for remote control and data transfer (conforms to IEEE 488.1, compatible with IEEE 488.2 and SCPI-1999.0).
LAN –
LAN for PC interface, remote control and data transfer (conforms to IEEE 802.3).

► Environmental

	Operating	Non-operating
Temperature	+10 ºC to +40 ºC	–20 ºC to +60 ºC
Humidity	20% to 80% relative humidity with a maximum wet bulb temperature of 29.4 ºC, non-condensing	(No diskette in floppy drive): 5% to 90% relative humidity with a maximum wet bulb temperature of 40 ºC, non-condensing
Altitude	3,000 m (10,000 ft.)	12,000 m (40,000 ft.)
Random Vibration	2.65 m/s^2 RMS (0.27 G_{RMS}), from 5 Hz to 500 Hz, 10 minutes	22.36 m/s^2 RMS (2.28 G_{RMS}) total from 5 Hz to 500 Hz, 10 minutes each axis 3-axes. 30 minutes total

Computer System and Peripherals
CompactPCI based PC, Celeron 566 MHz CPU, Microsoft Windows 2000 Professional, 128 MB SDRAM, 20 GB Hard Drive, 1.44 MB floppy drive on front panel, CD-ROM in rear panel, included USB compact keyboard and mouse.
PC I/O Ports
USB 1.1 compliant ports (3 total, 1 front, 2 rear), PS/2 mouse and keyboard connectors (rear panel), RJ-45 Ethernet connector (rear panel) supports 10Base-T and 100Base-Tx, VGA Out (rear panel), RS-232C.

Physical Characteristics

Display Characteristics –
LCD color display, 800 (H) x 600 (V) (SVGA).

Mainframe Dimensions	**mm**	**in.**
Height	266	10.5
Width	445	17.5
Length	462	19.7
Output Module Dimensions	**mm**	**in.**
Height	33	1.3
Width	84	3.3
Length	133	5.2
Weight (approx.)	**kg**	**lbs.**
DTG5078	17.5	38.6
DTG5274	17	37.5
DTG5334	17	37.5
DTGM21	0.26	0.57
DTGM30	0.27	0.6
DTGM31	0.27	0.6
DTGM32	0.27	0.6

Mechanical Cooling – Required Clearance.
Top and Bottom – 2 cm.
Side – 15 cm.
Rear – 7.5 cm.

Power Supply
Power Source – 100 to 240 VAC, 47 to 63 Hz.
Power Consumption – 560 W.
Safety –
UL61010B-1.
CAN/CSA-22.2 No. 1010.1.
EN61010-1/A2 1995.
Electromagnetic Compatibility (EMC) –
Europe:
EN61326 Class A.
EN61000-3-2, EN61000-3-3.
Australia/New Zealand:
AS/NZS 2064.

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▸ Output Module Characteristics

Basic Features	DTGM21	DTGM30	DTGM31	DTGM32
Output Channels and Connections	4 single-ended (installed in DTG5078) 2 single-ended (DTG5274/DTG5334) 4 SMA connectors	2 complementary channels 4 SMA connectors	1 complementary channel 2 SMA connectors	
Maximum Data Rate (Calculated by Transition Time)	1.1 Gb/s	3.35 Gb/s		350 Mb/s[*1]
Normal/Complement (Invert)	Selectable			
Source Impedance	50 Ω/23 Ω (selectable)	50 Ω		
Enable/Disable	Yes (software switch)			
Output Channel Timing				
Transition Times (20% to 80%) (50 Ω)	<340 ps (VOL = 0, VOH = 1) (typical) <1 ns (VOL = –1.65, VOH = 3.7) (typical)	<95 ps (VOL = 0, VOH = 0.1) (typical) <110 ps (VOL = 0, VOH = 1) (typical)		
Transition Time Control	No			
Slew Rate Control Range	—			
Setting Resolution	—			
Channel Output Levels				
Amplitude/Resolution	0.25 to 5.35 V_{pk-pk}/ 5 mV (from 23 Ω source impedance into 50 Ω) 0.25 to 3.9 V_{pk-pk}/ 5 mV (from 50 Ω source impedance into 50 Ω) 0.50 to 7.8 V_{pk-pk}/ 5 mV (from 50 Ω source impedance into 1 MΩ)	0.03 to 1.25 V_{pk-pk} /5 mV (into 50 Ω)[*2] 0.06 to 2.5 V_{pk-pk} /5 mV (into 1 MΩ)[*2]		
Output Voltage Window	–1.65 V to 3.70 V (from 23 Ω source impedance into 50 Ω) –1.2 V to 2.7 V (from 50 Ω source impedance into 50 Ω) –2.4 V to 5.4 V (from 50 Ω source impedance into 1 MΩ)	–2 V to 2.47 V (into 50 Ω) –2 V to 7 V (into 1 MΩ)		
DC Accuracy	(±3% of the set value) ±50 mV into 50 Ω to GND			
Limit setting	High and low level limits can be set			
Maximum Output Current	±80 mA			
Overshoot	<15% (typical) at High = 1 V, Low = 0 V	<10% (typical) at High = 1 V, Low = 0 V		
Typical Support Native Logic	TTL, CMOS, (P)ECL, LVPECL	LVDS, CMOS, (P)ECL, LVPECL, CML		
External Jitter Control	No		Yes	

[*1] minimum pulse width >2.86 ns.

[*2] maximum output amplitude is dependent on output voltage window (offset). (See Figure 1.)

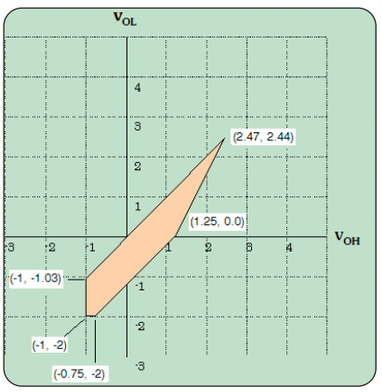
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▶ Output Module Characteristics, continued

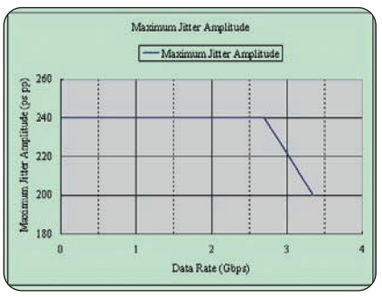
Channel Output Levels	DTGM21	DTGM30	DTGM31	DTGM32
External Jitter Control Input Channels and Connectors			1 single-ended channel 1 SMA connector	2 single-ended channels 2 SMA connectors
Input range			–0.5 V to +0.5 V (typical) Max input: –1 V to +1 V	–0.5 V to +0.5 V
Jitter Frequency			DC to 250 MHz[*3]	DC to 50 MHz
Jitter Amplitude			240 ps_{pk-pk} for 1 V_{pk-pk} input at Data rate ≤ 2.7 Gb/s[*4]	Range 1: Up to 1 ns at 1 V_{pk-pk} Range 2: Up to 2 ns at 1 V_{pk-pk}
External Tri-state (Hi Z) Control	Yes (SMB input connector)	No		
Tri-state Enable	Enable: Hi 3.3 V, disable Lo: 0 V	—		
Control Channels	By output module level	—		
Delay Time from Inhibit In to Data Output	Active to Inhibit: 13 ns, Inhibit to Active: 12 ns	—		

[*3] Up to 400 MHz by overdriving jitter input (max –1 V to +1 V_{pk-pk}). (See Figure 2.)

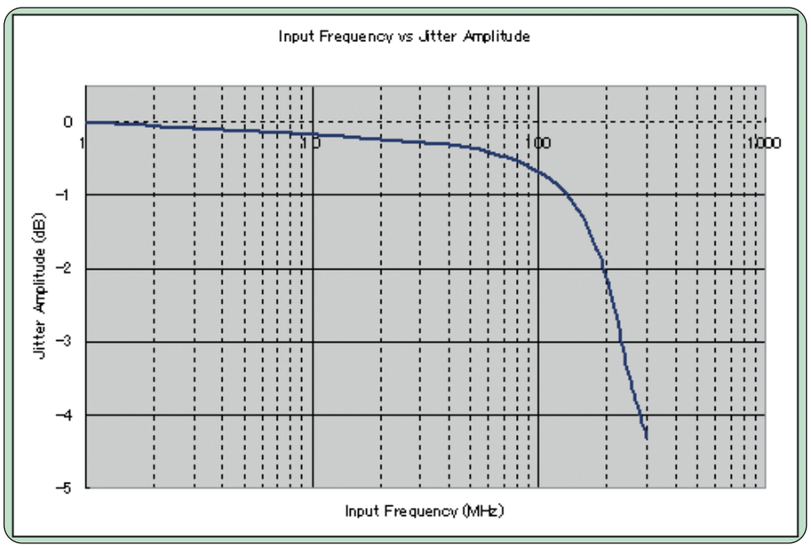
[*4] Jitter amplitude at data rates >2.7 Gb/s calculated as {240 – 61.5 x (data rate – 2.7)} ps_{pk-pk} for 1 V_{pk-pk} input (see Figure 3).



▶ Figure 1. DTGM30, M31, M32 Output Amplitude vs. Offset.



▶ Figure 3. DTGM31 Maximum Jitter Amplitude vs. Data Rate.



▶ Figure 2. DTGM31 Jitter Input Frequency Response.

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▸ Ordering Information

Mainframes

DTG5078

750 Mb/s, 8-slot mainframe.

DTG5274

2.7 Gb/s, 4-slot mainframe.

DTG5334

3.35 Gb/s, 4-slot mainframe.

Mainframes Include: Microsoft Windows 2000 Professional operating system recovery disk, DTG5000 Series application software install disk, user manual, technical reference, registration card, accessory pouch, front cover, compact USB keyboard, USB mouse, lead set for DC Output, 16-CON, twisted pair, 24 in. (60 cm), 50 Ω SMA terminator (male, DC to 18 GHz), SMA connector cap (10 each with DTG5078, 8 each with DTG5274/DTG5334), power cord, calibration certificate.

Please specify power cord and language option when ordering.

Mainframe Options

Opt. 1R – Rackmount.

International Power Plugs

Opt. A0 – North America power.

Opt. A1 – Universal Euro power.

Opt. A2 – United Kingdom power.

Opt. A3 – Australia power.

Opt. A5 – Switzerland power.

Opt. A6 – Japan power.

Opt. A10 – China power.

Opt. A99 – No power cord or AC adapter.

Language Options

Opt. L0– English.

Opt. L5– Japanese.

Output Modules

DTGM21

4 channels (DTG5078), 2 channels (DTG5274/DTG5334).

5.35 $V_{pk\text{-}pk}$ (from 23 Ω to 50 Ω).

3.9 $V_{pk\text{-}pk}$ (50 Ω), 7.8 $V_{pk\text{-}pk}$ (1 MΩ).

Tr/Tf (20% to 80%) <340 ps (1 $V_{pk\text{-}pk}$, into 50 Ω), fixed.

External Tri-state (Hi_Z) control function.

DTGM30

2 channels.

1.25 $V_{pk\text{-}pk}$ (50 Ω), 2.5 $V_{pk\text{-}pk}$ (1 MΩ).

Tr/Tf (20% to 80%) <110 ps (1 $V_{pk\text{-}pk}$, into 50 Ω), fixed.

▸ Cables

Type	Part Number
Lead Set for DC Output, 16-CON, Twisted Pair, 24 in. (60 cm)	012-A229-00
Pin Header Cable, 20 in. (51 cm)	012-1505-00
Pin Header SMB Cable, 20 in. (51 cm)	012-1503-00
GPIB Cable, Double-shielded, 79 in. (200 cm)	012-0991-00
Master-Slave Cable Set for Connecting Two Mainframes; Set of 4 SMA Cables, 51 cm, 50 Ω (174-1427-00), and Set of 2 BNC Cables, 46 cm (012-0076-00)	012-A230-00
Master-Slave Cable Set for Connecting Three Mainframes; Set of 6 SMA Cables, 51 cm, 50 Ω (174-1427-00) and Set of 3 BNC Cables, 46 cm (012-0076-00)	012-A231-00
BNC Cables 50 Ω	
18 in. (46 cm)	012-0076-00
24 in. (61 cm)	012-1342-00
42 in. (107 cm)	012-0057-01
With Shield, 98 in. (250 cm)	012-1256-00
SMA Cables 50 Ω	
12 in. (30 cm)	174-1364-00
20 in. (51 cm)	174-1427-00
39 in. (100 cm)	174-1341-00
60 in. (152 cm)	174-1428-00
Delay SMA Cables 50 Ω	
1 ns (male to female)	015-1019-00
2 ns	015-0560-00
2 ns (male to female)	015-1005-00
5 ns	015-0561-00
5 ns (male to female)	015-1006-00

▸ Adapters and Connectors

Type	Part Number
SMB to BNC adapter	015-0671-00
50 Ω SMA (male) to BNC (female) Adapter	015-0554-00
50 Ω SMA (female) to BNC (male) Adapter	015-0572-00
50 Ω N (male) to SMA (male) Adapter	015-0369-00
50 Ω SMA Adapter (male to female), DC to 18 GHz, VSWR: 1.2	015-0549-00
50 Ω SMA Adapter (slide on type female to male), DC to 18 GHz, VSWR: 1.05 + 0.002F (GHz)	015-0553-00
50 Ω SMA T-Connector (male to female/female)	015-1016-00
50 Ω SMA Divider (female/female/female), 6 dB, DC to 18 GHz, VSWR: 1.9	015-0565-00

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Data Timing Generator

► DTG5078 • DTG5274 • DTG5334

DTGM31

1 channel.

1.25 V_{pk-pk} (50 Ω), 2.5 V_{pk-pk} (1 MΩ).

Tr/Tf (20% to 80%) <110 ps (1 V_{pk-pk}, into 50 Ω), fixed.

External jitter control input.

Jitter frequency DC – 250 MHz.

Jitter amplitude up to 240 ps.

DTGM32

1 channel.

1.25 V_{pk-pk} (50 Ω), 2.5 V_{pk-pk} (1 MΩ).

Tr/Tf (20% to 80%) <110 ps (1 V_{pk-pk}, into 50 Ω), fixed.

2 ch. external jitter control input.

Jitter frequency DC – 50 MHz.

Jitter amplitude up to 1 ns/2 ns.

Output Modules include: Installation sheet (Japanese/English), SMA connector cap (set of 4 with DTGM21, set of 2 with DTGM30), 50 Ω SMA terminator (DC to 18 GHz) (set of 2 with DTGM30, set of 1 with DTGM31/32), registration card.

Service Options

Opt. C3 – Calibration Service 3 years.

Opt. C5 – Calibration Service 5 years.

Opt. D1 – Calibration Data Report (English).

Opt. D3 – Calibration Data Report 3 years (with Opt. C3).

Opt. D5 – Calibration Data Report 5 years (with Opt. C5).

Opt. R3 – Repair Service 3 years.

Opt. R5 – Repair Service 5 years.

Service Upgrade Kit

To determine if your DTG5334 or DTGM30 requires a service upgrade to meet these specifications, please contact your local Tektronix sales representative or technical support (1-800-833-9200, select Option 3, or e-mail: TechSupport@tektronix.com.

DTG53UP

Opt. 13 – Enable operation of up to 3.4 Gb/s and total jitter <44 ps_{pk-pk} up to 3.35 Gb/s, 800 mV_{pk-pk} differential output with DTGM30, requires the order of Option IFC.

Opt. IFC – Service installation and calibration, required with Option 13.

DTGM30UP

Opt. 13 – Enables total jitter <44 ps up to 3.35 Gb/s, 800 mV_{pk-pk} differential output with DTG5334, requires the order of Option IFC.

Opt. IFC – Service Installation and calibration, required with Option 13.

Recommended Accessories

Service Manual (English) – Order 071-1285-xx.

Test Adapters

HDMI TPA-R Test Adapter Set – HDMI TPA-R TDR (set of 2), HDMI TPA-R DI (differential), HDMI TPA-R SE (single-ended).

Order 013-A012-50.

HDMI TPA-P Test Adapter Set – HDMI TPA-P TDR, HDMI TPA-P DI (differential), HDMI TPA-P SE (single-ended).

Order 013-A013-50.

DVI TPA-R Test Adapter Set – DVI TPA-R TDR (set of 2), DVI TPA-R DI (differential), DVI TPA-R SE (single-ended).

Order 013-A014-50.

Note: These adapters do not include clock recovery circuits.

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www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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