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Tektronix Logic Analyzer Series
Product Specifications & Performance Verification

Technical Reference Manual

This document applies to TLA System Software Version 5.6 or above

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Tektronix

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Preface

This document lists characteristics and specifications of the following Tektronix Logic Analyzer Family products:

- TLA7000 series mainframes
- TLA7PC1 Controller
- TL708EX TekLink 8-Port Hub
- TLA700 series mainframes
- TLA600 series logic analyzers
- TLA7Axx/TLA7Nx series logic analyzer modules
- TLA7Lx/Mx/Nx/Px/Qx series logic analyzer modules
- TLA7PG2 pattern generation modules
- DSO digital storage oscilloscope modules

Other Tektronix Logic Analyzer modules, microprocessor-related products, and individual logic analyzer probes have their own documentation for characteristics and specifications.

This document also contains performance verification procedures for the TLA7000 Series mainframes.

To prevent personal injury or damage consider the following requirements before attempting service:

- Read the *General Safety Summary* and *Service Safety Summary* found in the *Tektronix Logic Analyzer Family Product Safety & Compliance Instructions* (Tektronix part number 071-2591-xx).

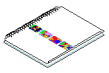
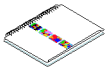
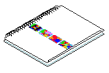
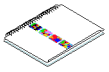
Related Documentation

Refer to the individual service manuals for the performance verification procedures and adjustment procedures for earlier TLA products.

The following table lists related documentation available for your logic analyzer. The documentation is available on the TLA Documentation CD and on the Tektronix Web site (www.tektronix.com/manuals).

You can also check the release notes on the instrument for additional information. To access the release notes, select Start > All Programs > Tektronix Logic Analyzer > TLA Release Notes.

Related Documentation

Item	Purpose	Location
TLA Quick Start User Manuals	High-level operational overview	 
Online Help	In-depth operation and UI help	
Installation Quick Reference Cards	High-level installation information	 
Installation Manuals	Detailed first-time installation information	 
XYZs of Logic Analyzers	Logic analyzer basics	 www.Tektronix.com
Declassification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products	 www.Tektronix.com
Application notes	Collection of logic analyzer application specific notes	
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures	
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET	
Field upgrade kits	Upgrade information for your logic analyzer	 
Optional Service Manuals	Self-service documentation for modules and mainframes	 

Specifications and Characteristics

This document lists the specifications for the Tektronix Logic Analyzer mainframes and other logic analyzer products. Additional specification documents are available on the TLA Documentation CD or on the Tektronix Web site. For the most current documentation, refer to the Tektronix Web site (http://www.Tektronix.com).

Characteristic Tables

All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) using performance verification procedures.

For mainframes and modules, the performance limits in this specification are valid with these conditions:

- The logic analyzer must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The logic analyzer must have had a warm-up period of at least 30 minutes.

For modules, the performance limits in this specification are valid with these conditions:

- The modules must be installed in a Logic Analyzer Mainframe.
- The module must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.
- The DSO module must have had its signal-path-compensation routine (self calibration or self cal) last executed after at least a 30 minute warm-up period.
- After the warm-up period, the DSO module must have had its signal-path-compensation routine last executed at an ambient temperature within ±5 °C of the current ambient temperature.

For optimum performance using an external oscilloscope, please consult the documentation for any external oscilloscopes used with your Tektronix Logic Analyzer to determine the warm-up period and signal-path compensation requirements.

Atmospheric Characteristics for the Tektronix Logic Analyzer Family

The following table lists the Atmospheric characteristics of components in the Tektronix Logic Analyzer family.

Table 1: Atmospheric characteristics

Characteristic	Description
Temperature	*Operating (no media in CD or DVD drive)*
	+5 °C to +50 °C, 15 °C/hr maximum gradient, noncondensing (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude) [1] [2]
	Nonoperating (no media in drive)
	-20 °C to +60 °C, 15 °C/hr maximum gradient, noncondensing
Relative Humidity	*Operating (no media in drive)*
	20% to 80% relative humidity, noncondensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C). [3] [4]
	Nonoperating (no media in drive)
	8% to 80% relative humidity, noncondensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C). [5]
Altitude	*Operating*
	To 3000 m (9843 ft), (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude.
	Nonoperating
	12,190 m (40,000 ft)

1 For TLA7012 instruments, the operating temperature is +5 °C to +45 °C, 11 °C/hr maximum gradient, noncondensing (derated 1 °C per 1000 ft above 5000 ft (1524 m) altitude)

2 TLA7Axx series module operating temperature is +40 °C maximum.

3 TLA7Axx series module operating humidity is 5% to 90% up to +30 °C, 75% from +30 to +40 °C, noncondensing. Maximum wet-bulb temperature is +29.4 °C.

4 TLA7NAx series module operating humidity is 5% to 90% up to +30 °C, 75% from +30 to +40 °C, 45 % from +40 to +50 °C, noncondensing. Maximum wet-bulb temperature is +29.4 °C.

5 TLA7Axx/TLA7NAx series module nonoperating humidity is 5% to 90% limited by a wet bulb temperature of +40 °C.

TLA7000 System Specifications

The following tables list the specifications common to the TLA7000 series logic analyzers.

Table 2: TLA7000 Backplane interface

Characteristic		Description
Number of Slots	Portable mainframe	4
	Benchtop mainframe	13
⩘ CLK10 Frequency		10 MHz ±100 ppm
Relative Time Correlation Error [1] [2] *(Typical)*	TLA7Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx "MagniVu" data	2 ns
	TLA7Axx/TLA7NAx to TLA7AxxTLA7NAx "MagniVu" data	2 ns
	TLA7Axx/TLA7NAx to TLA7Nx/Px/Qx "MagniVu" data	-3 ns
	TLA7Nx/Px/Qx to TLA7Nx/Px/Qx "normal" data using an internal clock	1 TLA7Nx/Px/Qx sample – 0.5 ns
	TLA7Axx/TLA7NAx to TLA7Axx "normal" data using an internal clock	1 TLA7Axx/TLA7NAx sample – 0.5 ns
	TLA7Axx/TLA7NAx to TLA7Nx/Px/Qx "normal" data using an internal clock	1 TLA7Nx/Px/Qx sample – 0.5 ns
	TLA7Nx/Px/Qx to TLA7Nx/Px/Qx "normal" data using an external clock	2 ns
	TLA7Axx/TLA7NAx to TLA7Axx/TLA7NAx "normal" data using an external clock	2 ns
	TLA7Axx/TLA7NAx to TLA7Nx/Px/Qx "normal" data using an external clock	4 ns

1 Includes typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a "typical" number for the measurement. Assumes standard accessory probes are utilized.

2 For time intervals longer than 1 ms between modules, add 0.01% of the difference between the absolute time measurements to the relative time correlation error to account for the inaccuracy of the CLK10 source.

Table 3: System trigger and external signal input latencies *(Typical)*

Logic analyzer source characteristic [1]	Same mainframe	To expansion frame
External system trigger input to LA probe tip [2]		
TLA7Nx/Px/Qx modules	–266 ns	–202 ns
TLA7AAx/TLA7NAx modules	–626 ns	–562 ns
TLA7BBx modules	–1202 ns	–1143 ns
TLA7Sxx modules	–958 ns ±30 ns	–1221 ns ±30 ns
External Signal In to LA probe tip via Signals 3, 4 (TTLTRG 0,1) [3]		
TLA7Nx/Px/Qx modules	–212 ns + Clk	–148 ns + Clk
TLA7AAx/TLA7NAx modules	–535 ns + Clk	–471 ns + Clk
TLA7BBx modules	–1190 ns + Clk	–1118 ns + Clk
TLA7Sxx modules	–950 ns ±30 ns	–1220 ns ±30 ns
External Signal In to LA probe tip via Signals 1, 2(ECLTRG 0,1) [3] [4]		
TLA7Nx/Px/Qx modules	–208 ns + Clk	–144 ns + Clk
TLA7AAx/TLA7NAx modules	–627 ns + Clk	–556 ns + Clk
TLA7BBx modules	–1186 ns + Clk	–1043 ns + Clk
TLA7Sxx modules	–950 ns ±30 ns	–1116 ns ±30 ns

1 All system trigger and signal input latencies were measured from a falling edge transition (active true low) with signals in the wired-OR configuration.

2 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

3 Clk represents the time to the next master clock at the destination logic analyzer module. With asynchronous clocking this represents the delta time to the next sample clock. With synchronous sampling this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied SUT clocks and qualification data.

4 Signals 1 and 2 (ECLTRG0, 1) are limited to a broadcast mode where only one source can drive the signal node at any one time. The signal source can be used to drive any combination of destinations.

Table 4: System trigger and external signal output latencies *(Typical)*

Logic analyzer source characteristic [1]	Same mainframe	To expansion frame
LA probe tip to external system trigger out (skid) [2]		
TLA7Nx/Px/Qx modules	376 ns + Smpl	437 ns + Smpl
TLA7AAx/TLA7NAx modules	794 ns + Smpl	854 ns + Smpl
TLA7BBx modules	1332 ns + Smpl	1392 ns + Smpl
TLA7Sxx modules	1170 ns ±30 ns	1230 ns ±30 ns
LA probe tip to External Signal Out via Signal 3, 4 (TTLTRG 0,1) [3]		
OR function		
TLA7Nx/Px/Qx modules	366 ns + Smpl	428 ns + Smpl
TLA7AAx/TLA7NAx modules	793 ns + Smpl	854 ns + Smpl
TLA7BBx modules	1328 ns + Smpl	1390 ns + Smpl
TLA7Sxx modules	950 ns ±30 ns	1011 ns ±30 ns
AND function		
TLA7Nx/Px/Qx modules	379 ns + Smpl	457 ns + Smpl
TLA7AAx/TLA7NAx modules	803 ns + Smpl	881 ns + Smpl
TLA7BBx modules	1340 ns + Smpl	1418 ns + Smpl
TLA7Sxx modules	950 ns ±30 ns	1028 ns ±30 ns
LA probe tip to External Signal Out via Signals 1, 2 (ECLTRG0,1) [3] [4]		
TLA7Nx/Px/Qx modules	374 ns + Smpl	444 ns + Smpl
TLA7AAx/TLA7NAx modules	793 ns + Smpl	863 ns + Smpl
TLA7BBx modules	1330 ns + Smpl	1399 ns + Smpl
TLA7Sxx modules	950 ns ±30 ns	1019 ns ±30 ns

1 SMPL represents the time from the event to the next valid data sample at the probe tip of the LA module. With asynchronous sampling, this represents the delta time to the next sample clock. With MagniVu asynchronous sampling, this represents 500 ps or less. With synchronous sampling, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

2 Skid is commonly referred to as the system level system trigger and signaling output latency. This is the absolute time from when the event first appears at the input probe tips of a module to when the corresponding event that it generates appears at the system trigger or external signal outputs.

3 All signal output latencies are validated to the rising edge of an active (true) high output.

4 Signals 1 and 2 (ECLTRG0, 1) are limited to a broadcast mode where only one source can drive the signal node at any one time. The signal source can be used to drive any combination of destinations.

Table 5: Intermodule latencies for LA source *(Typical)*

Logic analyzer source characteristic	Same mainframe	Frame to frame
LA to LA intermodule system trigger (TTLTRG7) [1] [2]		
LA2: Trigger All Modules, LA1: Do Nothing		
TLA7Nx/Px/Qx modules	66 ns + Smpl	128 ns + Smpl
TLA7AAx/TLA7ABx modules	108 ns + Smpl	118 ns + Smpl
TLA7BBx modules	82 ns + Smpl	145 ns + Smpl
TLA7Sxx modules	105 ns ±30 nsl	167 ns ±30 ns
LA to LA intermodule ARM (TTLTRG 2, 4 ,5, 6) [2] [3]		
TLA7Nx/Px/Qx modules	108 ns + Smpl + Clk	170 ns + Smpl +Clk
TLA7AAx/TLA7ABx modules	115 ns + Smpl + Clk	180 ns + Smpl + Clk
TLA7BBx modules	95 ns + Smpl + Clk	162 ns + Smpl +Clk
TLA7Sxx modules	85 ns ±30 ns	147 ns ±30 ns
LA to LA intermodule Signals 1, 2 (ECLTRG 0, 1) [2] [3] [4]		
(LA2: Trigger, Then Set Signal 2; LA1: If Signal 2 Is True, Then Trigger)		
TLA7Nx/Px/Qx modules	116 ns + Smpl + Clk	178 ns + Smpl + Clk
TLA7AAx/TLA7ABx modules	118 ns + Smpl + Clk	192 ns + Smpl + Clk
TLA7BBx modules	95 ns + Smpl + Clk	166 ns + Smpl + Clk
TLA7Sxx modules	130 ns ±30 ns	192 ns ±30 ns
LA to LA intermodule Signals 3, 4 (TTLTRG0,1) [2] [3]		
(LA2: Trigger, Then Set Signal 3; LA1: If Signal 3 Is True, Then Trigger)		
TLA7Nx/Px/Qx modules	116 ns + Smpl + Clk	128 ns + Smpl + Clk
TLA7AAx/TLA7ABx modules	120 ns + Smpl + Clk	184 ns + Smpl + Clk
TLA7BBx modules	91 ns + Smpl + Clk	158 ns + Smpl + Clk
TLA7Sxx modules	950 ns ±30 ns	1012 ns ±30 ns

1 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

2 SMPL represents the time from the event to the next valid data sample at the probe tip of the LA module. With asynchronous sampling, this represents the delta time to the next sample clock. With MagniVu asynchronous sampling, this represents 500 ps or less. With synchronous sampling, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

3 Clk represents the time to the next master clock at the destination logic analyzer module. With ascynchronous clocking this represents the delta time to the next sample clock. With synchronous sampling this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied SUT clocks and qualification data.

4 Signals 1 and 2 (ECLTRG0, 1) are limited to a broadcast mode where only one source can drive the signal node at any one time. The signal source can be used to drive any combination of destinations.

Table 6: TLA7000 External signal interface

Characteristic		Description	
System Trigger Input		TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Input levels	0 V to 3.0 V	
	Minimum input voltage swing	300 mV	
	Threshold range	0.5 V to 1.5 V	
	Threshold step size	50 mV	
	Input destination	System trigger	
	Input Mode	Falling edge sensitive, latched (active low)	
	Minimum Pulse Width	12 ns	
	Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods	
	Maximum Input Voltage	0 to+ 5 V peak	
External Signal Input		TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Input Destination	Signal 1, 2, 3, 4	
	Input levels	0 V to 3.0 V	
	Minimum input voltage swing	300 mV	
	Threshold range	0.5 V to 1.5 V	
	Threshold step size	50 mV	
	Input Mode	Active (true) low, level sensitive	
	Input Bandwidth [1]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Accepts signals during valid acquisition periods via real-time gating	
	Maximum Input Voltage	0 V to 5 V peak	
System Trigger Output		TTL compatible output via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Source selection	System trigger	
	Source Mode	Active (true) low, falling edge latched	
	Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions	
	Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output ≥4 V into open circuit, ≥2 V into 50 Ω to ground ≤ 0.7 V sinking 10 mA	
	Output Protection	Short-circuit protected (to ground)	

Table 6: TLA7000 External signal interface (cont.)

Characteristic		Description	
External Signal Output		TTL compatible outputs via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Source Selection	Signal 1, 2	
		Signal 3, 4	
		10 MHz clock	
	Output Modes	User definable	
	Level Sensitive	Active (true) low or active (true) high	
	Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL output	
		≥4 V into open circuit, ≥2 V into 50 Ω to ground	
		≤ 0.7 V sinking 10 mA	
	Output Bandwidth [2]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously	
	Output Protection	Short-circuit protected (to ground)	
Intermodule Signal Line Bandwidth		Minimum bandwidth up to which the intermodule signals are specified to operate correctly	
		Signal 1, 2	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum

[1] The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

[2] The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

TLA7012 Portable Mainframe Specifications

The following tables describe the specifications for the TLA7012 Portable Mainframe.

Table 7: TLA7012 Internal controller

Characteristic		Description
Operating system		Microsoft Windows XP Professional
Motherboard		The AB915GM motherboard is an ATX-family board that meets the FlexATX and microATX form-factor specifications. It is based around an Intel Mobil Celeron M or Pentium M processor and an Intel 915GM chipset, integrating video, system monitoring, and Ethernet controllers on a 9.0 X 7.5 inch board.
Microprocessor		Intel 2 GHz/533 Dothan microprocessor; 479-pin PGA socket for uFC-PGA processor package
Chip set		Intel 915GM GMCH with an Intel ICH6-M I/O hub. Supports dual channel memory for higher performance.
Main memory		Two 200 pin SO DIMM sockets for DDR2-400/533 (PC2-3200/4300) modules. Maximum 2 GB (two modules, Gbit technology), minimum 128 MB Installed Configuration 1 GB
Cache memory		2 MB Level 2 (L2) write-back cache
RTC, CMOS setup, & PNP NVRAM retention time *(Typical)*		> 5 years battery life, lithium battery
Bootable replaceable hard disk drive		Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface.
	Formatted capacity	80 GB Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
	Interface	SATA, native
	Average seek time	Read 9 ms Write 10 ms
DVD-RW drive		Standard PC compatible IDE (Integrated Device Electronics) DVD-RW drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment.

Table 8: TLA7012 Display system

Characteristic		Description		
Display selection		The TLA7012 Portable Mainframe motherboard can drive 3 video displays. Two DVI connectors connect to the external world. One of the connectors has both the DVI digital signals and the analog signals while the other connector has only DVI digital signals available. The third display connector is available only as an internal connection. This connection is via LVDS. This port drives the internal 15-inch display. One of the external connectors and the internal connection are connected to the same video information.		
External display drive		One VGA, SVGA, or XGA-compatible analog output port.		
	Primary video port with DVI digital only	*Resolution (Pixels)*	*Colors*	*Refresh Rates*
		640 x 480	256, 16-bit, 32-bit	60, 75, 85
		1024 x 768		60, 75, 85
		1280 x 1024		60, 75, 85
		1600 x 1200		
	Secondary video port with DVI digital and analog VGA signalling through an adapter	*Resolution (Pixels)*	*Colors*	*Refresh Rates*
		640 x 480	256, 16-bit, 32-bit	60, 75, 85
		1024 x 768		60, 75, 85
		1280 x 1024		60, 75, 80
		1600 x 1200		
		Maximum resolution on the analog VGA is 1600 x 1200 with 32-bit color at 75 Hz.		
Internal display	Classification	Color LCD (NEC TFT NL10276BC30-24D) Color LCD module NL10276BC30-24D is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight. This LCD display will be driven directly by the motherboard via LVDS signaling.		
	Resolution/Refresh rate and area	1024 pixels horizontal by 768 pixels vertical (1024X768) at 60 Hz refresh rate Area of 304 mm (11.7 in) by 228 mm (9 in) of viewing area.		
	Color scale	262, 144 colors (6-bit RGB) with a color gamut of 42% at center to NTSC		

Table 9: TLA7012 Front-panel interface

Characteristic		Description
Keypad		18 buttons allow user to perform the most common tasks required to operate theTLA
Special function knobs	Multi-function Knob	Various increment, decrement functions dependent on screen/window selected.
	Vertical position	Scrolling and positioning dependent on display type.
	Vertical scale	Scales waveform displays only.
	Horizontal position	Scrolling and positioning dependent on display type.
	Horizontal scale	Scales waveform displays only.
USB Port		Front panel (lower Right on Front Panel) 3 each USB 2.0 connectors.

Table 10: TLA7012 Rear-panel interface

Characteristic		Description
TekLink interface bus		Connector supports Reference Clock (10 MHz), Power On Signaling, Run event, System Trigger, General purpose events
	Input signal characteristics	LVDS compatible inputs via rear-panel 40-pin connector
	Output signal characteristics	LVDS compatible outputs via rear-panel 40-pin connector
	Reference clock characteristics	LVDS compatible inputs via rear-panel 40-pin connector
SVGA output ports		Two DVI connectors
External Trigger input		Trigger input routed to the system trigger line
External Signal input		Signal input routed to one of four internal signals
System Trigger output		Internal system trigger routed as TTL-compatible output
External Signal output		One of four internal signals routed to the signal output connector. The internal 10 MHz reference clock can be routed to this output.
USB 2.0 ports		Four USB 2.0 connections
GBit LAN port		RJ-45 connector 10/100/1000 Mbps

Table 11: TLA7012 AC power source

Characteristic	Description
Source voltage and frequency	100 V_{RMS} to 240 V_{RMS} ±10%, 50 Hz to 60 Hz 115 V_{RMS} ±10%, 400 Hz
Maximum power consumption	750 W
Steady-state input current	6 A_{RMS} maximum at 90 VAC_{RMS}, 60 Hz or 100 VAC_{RMS}, 400 Hz
Inrush surge current	70 A maximum
Power factor correction	Yes

Table 11: TLA7012 AC power source (cont.)

Characteristic	Description
On/Sleep indicator	Green/yellow front panel LED located left of the On/Standby switch provides visual feedback when the switch is actuated. When the LED is green, the instrument is powered and the processor is not sleeping. When the LED is yellow, the instrument is powered, but the processor is sleeping.
On/Standby switch and indicator	Front panel On/Standby switch allows users to turn the instrument on. A soft power down is implemented so that users can turn the instrument off without going through the Windows shutdown process; the instrument powers down normally. The power cord provides main power disconnect

Table 12: TLA7012 Portable mainframe transportation and storage

Characteristic	Description
Transportation Package Material	Transportation Package material meets recycling criteria as described in Environmental Guidelines for Package Design (Tektronix part number 063-1290-00) and Environmentally Responsible Packaging Handbook (Tektronix part number 063-1302-00).
Configuration for Transportation	The system can be shipped with or without modules installed. Only modules weighing less than 5lbs/slot which have been qualified to meet 60g shock (per Tektronix Standard part number 062-2858-00, Rev B, Class 5 subassembly requirement) can be shipped installed in this mainframe and its standard shipping package.

Table 13: TLA7012 Cooling

Characteristic	Description
Cooling system	Forced air circulation system with no removable filters using eight fans operating in parallel
Pressurization	Negative pressurization system in all chambers including modules
Slot activation	Installing a module activates cooling for the corresponding occupied slots by opening the airflow shutter mechanism. Optimizes cooling efficiency by only applying airflow to installed modules.
Air intake	Front sides and bottom
Air exhaust	Back rear
Cooling clearance	6 inches (152 mm) front, sides, top, and rear. Prevent blockage of airflow to bottom of instrument by placing on a solid, noncompressable surface; can be operated on rear feet.
Fan speed and operation	All fans operational at half their rated potential and speed (12 VDC)

Table 14: TLA7012 Mechanical

Characteristic		Description
Classification		The portable mainframe is intended for design and development bench and lab-based applications.
Overall dimensions		Dimensions are without front feet extended, front cover attached, pouch attached, nor power cord attached.
	Height (with feet)	11.6 in (294.64 mm)
	Width	17.75 in (450.85 mm)
	Depth	18.1 in (459.74 mm)
Weight		40 lbs 12 oz (18.45 kg) with no modules installed, two dual-wide slot covers, and empty pouch
		5 lbs (2.27 kg) maximum per module slot
Shipping configuration		58 lbs (26.30 kg) minimum configuration (no modules), with all standard accessories
		89 lbs 8 oz (41.6 kg) full configuration, with two TLA7P4 modules and standard accessories (including probes and clips)
Acoustic noise level *(Typical)*		43 dBA weighted (operator) 41 dBA weighted (bystander)
Construction materials		Chassis parts are constructed of aluminum alloy; front panel and trim peaces are constructed of plastic; circuit boards are constructed of glass.
Finish type		Tektronix blue body and Tektronix silver-gray trim and front with black pouch, FDD feet, handle, and miscellaneous trim pieces

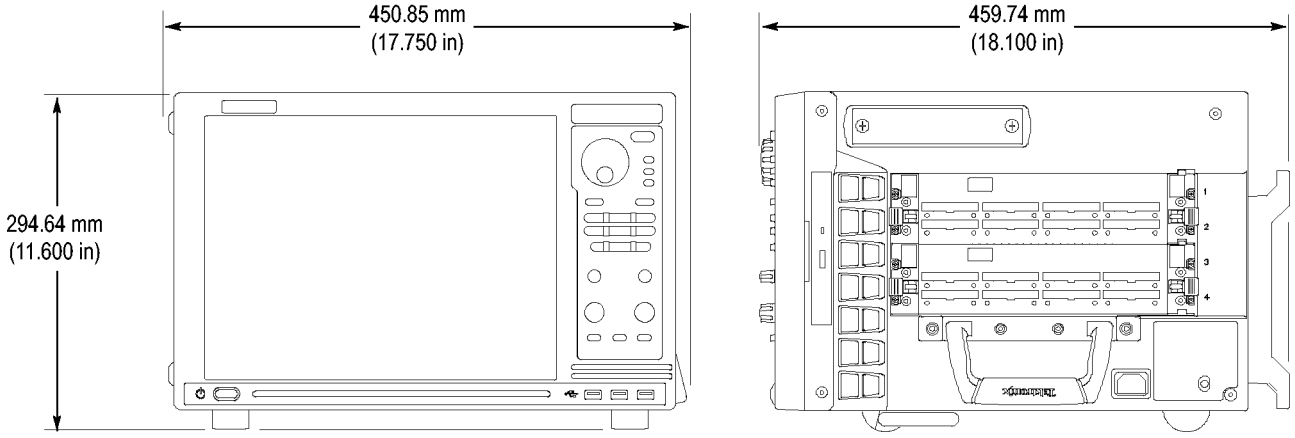


Figure 1: Dimensions of the TLA7012 Portable mainframe

TLA7016 Benchtop Mainframe Characteristics

The following tables list the specifications for the TLA7016 Benchtop Mainframe. The mainframe includes the interface module. The interface module provides the interface between an external controller and the mainframe. All communication between the controller and the mainframe is via GB LAN.

Table 15: TLA7016 Benchtop mainframe AC power source (Serial numbers B020000 and higher)

Characteristic	Description
Source voltage & Maximum power consumption	100 V_{RMS} to 120 V_{RMS}, 50 Hz to 60 Hz; 1450 W line power [1] 120 V_{RMS} to 240 V_{RMS}, 50 Hz to 60 Hz; 1900 W line power [1] 115 V_{RMS}, 440 Hz; 1450 W line power [1]
Inrush surge current	70 A maximum
Steady state input current	17.6 A_{RMS} maximum at 108 VAC_{RMS} 10 A_{RMS} maximum at 207 VAC_{RMS}
Power factor correction *(Typical)*	0.99 at 60 Hz operation and 0.95 at 400 Hz operation
ON/Standby switch and indicator	Front Panel On/Standby switch with integral power indicator. Switch allows users to turn the instrument on. A soft power down is implemented so that users can turn off the instrument without going through the Windows shutdown process; the instrument powers down normally.

[1] Maximum power consumed by a fully loaded six-module instrument.

Table 16: TLA7016 Benchtop mainframe AC power source (Serial numbers B01000 – B019999)

Characteristic		Description
Source voltage		100 V_{RMS} to 240 V_{RMS} ±10%, 45 Hz to 66 Hz 100 V_{RMS} to 120 V_{RMS}, 360 Hz to 440 Hz
Maximum power consumption		1450 W line power (the maximum power consumed by a fully loaded, 6-module instrument)
Fuse rating (Current and voltage ratings and type of fuse used to fuse the source line voltage)	90 V - 132 VAC_{RMS} Operation High-power/Low line (159-0379-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: Slow acting Rating: 20 A/250 V
	103 V - 250 VAC_{RMS} Operation (159-0256-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: No. 59/Fast acting Rating: 15 A/250 V
	207 V - 250 VAC_{RMS} Operation (159-0381-00)	Safety: IEC 127/Sheet 1 Size: 5 mm × 20 mm Style: Fast acting "F", high-breaking capacity Rating: 6.3 A/250 V

Table 16: TLA7016 Benchtop mainframe AC power source (Serial numbers B01000 – B019999) (cont.)

Characteristic	Description
Inrush surge current	70 A maximum
Steady state input current	16.5 A_{RMS} maximum at 90 VAC_{RMS} 6.3 A_{RMS} maximum at 207 VAC_{RMS}
Power factor correction *(Typical)*	0.99 at 60 Hz operation and 0.95 at 400 Hz operation
ON/Standby switch and indicator	Front Panel On/Standby switch with integral power indicator. Switch allows users to turn the instrument on. A soft power down is implemented so that users can turn off the instrument without going through the Windows shutdown process; the instrument powers down normally.

Table 17: TLA7016 Benchtop mainframe transportation and storage

Characteristic	Description
Transportation Package Material	Transportation Package material meets recycling criteria as described in Environmental Guidelines for Package Design (Tektronix part number 063-1290-00) and Environmentally Responsible Packaging Handbook (Tektronix part number 063-1302-01).
Configuration for Transportation	The system can be shipped with or without modules installed. Only modules weighing less than 5lbs/slot which have been qualified to meet 60g shock (per Tektronix Standard part number 062-2858-00, Rev B, Class 5 'subassembly' requirement) can be shipped installed in this mainframe and its standard shipping package.

Table 18: TLA7016 Benchtop mainframe cooling

Characteristic	Description
Cooling system	Forced air circulation system (positive pressurization) using a single low-noise centripetal (squirrel cage) fan configuration with no filters for the power supply and 13 module slots.
Fan speed control	Rear panel switch selects between full speed and variable speed. Slot exhaust temperature and ambient air temperature are monitored such that a constant delta temperature is maintained.
Slot activation	Installing a module activates the cooling for the corresponding occupied slots by opening the air flow shutter mechanism. Optimizes cooling efficiency by only applying airflow to modules that are installed.
Pressurization	Positive pressurization system, all chambers including modules
Slot airflow direction	P2 to P1, bottom of module to top of module
Mainframe air intake	Lower fan-pack rear face and bottom
Mainframe air exhaust	Top-sides and top-rear back. Top rear-back exhaust redirected to the sides by the fan pack housing to minimize reentry into the intake.
D Temperature readout sensitivity *(Typical)*	100 mV/ °C with 0 °C corresponding to 0 V output
Temperature sense range *(Typical)*	-10 °C to +90 °C, delta temperature ≤ 50 °C
Clearance	2 in (51 mm), rear, top, and sides

Table 18: TLA7016 Benchtop mainframe cooling (cont.)

Characteristic	Description
Fan speed readout	RPM = 20 (Tach frequency) or 10 ≥ (+Pulse Width) where (+Pulse Width) is the positive width of the TACH1 fan output signal measured in seconds
Fan speed range	650 to 2250 RPM

Table 19: Enhanced monitor

Characteristic		Description
Voltage readout		+24 V, -24 V, +12 V, -12 V, +5 V, -5.2 V, -2 V, +5 $V_{Standby}$ if present, and +5 $V_{External}$ via RS-232
Voltage readout accuracy *(Typical)*		±3% maximum
Current readout		Readout of the present current on the +24 V, -24 V, +12 V, -12 V, +5 V, -2 V, -5.2 V rails via RS-232
Current readout accuracy *(Typical)*		±5% of maximum power supply I_{mp}
RS-232 Connector		Provides access for RS-232 host to enhanced monitor
	Connector levels	±25 VDC maximum, 1 A maximum per pin
Passive monitor connector		25-pin connector provides access for monitoring the power supply, temperature, and fan speed.

Table 20: TLA7016 Benchtop mainframe Interface Module front panel characteristics

Characteristic		Description
TekLink interface bus		Connector supports Reference Clock (10 MHz), Power On Signaling, Run event, System Trigger, General purpose events
	Input signal characteristics	LVDS compatible inputs via rear-panel 40-pin connector
	Output signal characteristics	LVDS compatible outputs via rear-panel 40-pin connector
	Reference clock characteristics	LVDS compatible inputs via rear-panel 40-pin connector
External Trigger input		Trigger input routed to the system trigger line
External Signal input		Signal input routed to one of four internal signals
System Trigger output		Internal system trigger routed as TTL-compatible output
External Signal output		One of four internal signals routed to the signal output connector. The internal 10 MHz reference clock can be routed to this output.
GBit LAN port		RJ-45 connector 10/100/1000 Mbps

Table 21: TLA7016 Benchtop mainframe mechanical

Characteristic		Description
Classification		For lab benchtop or rackmount applications
Overall Dimensions	*Standard*	
	Height (with feet)	13.7 in (35 cm) including feet
	Width	16.7 in (42.4 cm)
	Depth	26.5 in (67 cm)
	Rackmount	
	Height	13.25 in (33.66 cm)
	Width	18.9 in (48 cm)
	Depth	28.9 in to 33.9 in (73.4 cm to 86.1 cm) in 0.5 in increments, user selectable
Interface module dimensions	Height	10.32 in (262.1 mm)
	Width	1.25 in (31.75 mm)
	Depth	14.75 in (373.4 mm)
Weight	Mainframe with interface module and slot fillers *(Typical)*	52 lbs 14 oz. (24 kg) minimum configuration with interface module and 6 dual-slot filler panels
	Maximum per slot	5 lbs (2.27 kg)
	Rackmount kit added	20 lbs (9.1 kg)
Shipping weight		60 lbs 11 oz (26.7 kg) minimum configuration with interface module (no other modules), with standard accessories
		187 lbs (85 kg) fully configured instrument with the addition of five logic analyzer modules and all module standard accessories including probes and clips
Size	Interface module	One slot wide
Acoustic noise level (*Typical*)	Variable fan speed (at 860 RPM)	43.2 dBA weighted (front)
		43.8 dBA weighted (back)
	Full speed fan (switched at rear)	66.2 dBA weighted (front)
		66.2 dBA weighted (back)
Construction materials		Chassis parts, aluminum alloy
		Front panel and trim pieces, plastic
		Circuit boards, glass laminate
Finish type		Mainframes are Tektronix silver gray with dark gray trim on fan pack and bottom feet support rails.

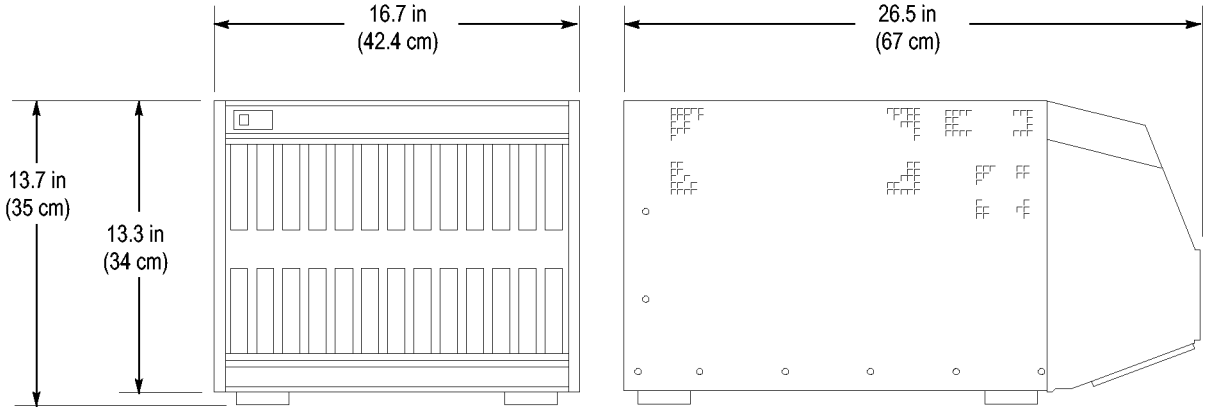


Figure 2: Dimensions of the TLA7016 Benchtop mainframe

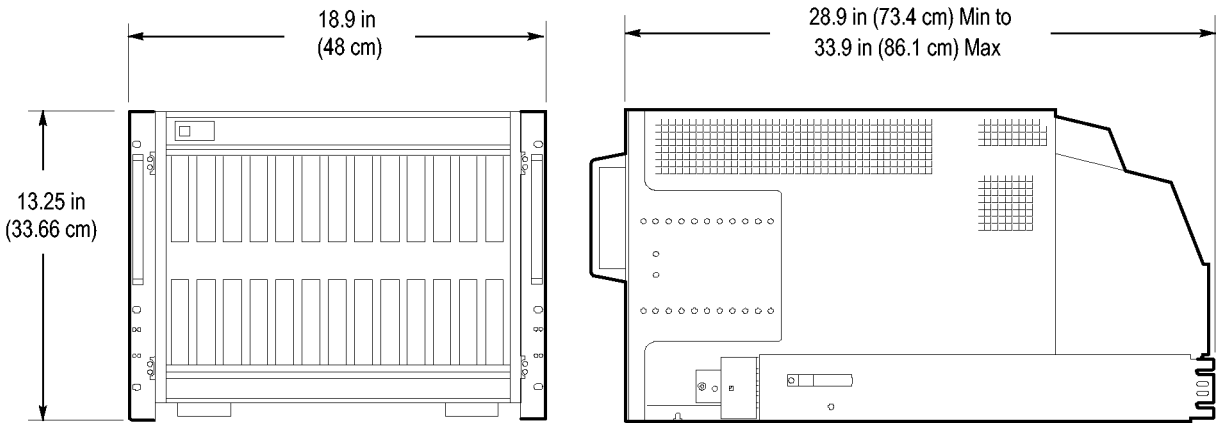


Figure 3: Dimensions of the TLA7016 Benchtop mainframe with rackmount option

TLA7PC1 Controller Specifications

Tektronix has released different motherboards for the TLA7PC1 controllers. The motherboards are indicated by the following serial number ranges.

- B010000 to B019999
- B020000 to B029999
- B030000 to B039999

The following tables list the specifications for the TLA7PC1 Controllers. The serial number ranges are designated by prefixes, such as: B01, B02, and B03.

NOTE. *To access the BIOS Setups for TLA7PC1 controllers with serial numbers B020000 and higher, restart the instrument and hold down the Delete key. For controllers with serial numbers B010000 to B019999, restart the instrument and hold down function key F2.*

Table 22: TLA7PC1 Internal specifications

Characteristic		Description
Operating system		Microsoft Windows XP Professional
Motherboard		ATX-family board, integrating video, system monitoring, IDE and Ethernet controllers on a single board.
	B01	AB915GM - Flex-ATX-family board, 9.0 X 8.0 in.
	B02	AIMB-760G2 - RoHS compliant, ATX-family board, 12.0 X 9.6 in.
	B03	AIMB-762G2 - RoHS compliant, ATX-family board, 12.0 X 9.6 in.
Microprocessor	B01	Intel 2 GHz/533 MHz FSB Pentium M, 479-pin PGA socket for uFC-PGA processor package
	B02, B03	Intel 3.4 GHz/800 MHz FSB Pentium 4, LGA775 socket
Chip set	B01, B02	Intel 915G GMCH with an Intel ICH6 PCI Express I/O hub
	B03	Intel 945G GMCH with an Intel ICH7R PCI Express I/O hub
Main memory		Maximum configuration: 4 GB (four 1 GB DIMMs) Installed configuration: 1 GB (two 512 MB DIMMs)
	B01	Two 200-pin SO-DIMM sockets for DDR2-400/533 MHz (PC2-3200/4300)
	B02	Two 240-pin DIMM sockets for DDR2-400/533 MHz (PC2-3200/4300) SDRAM
	B03	Two 240-pin DIMM sockets for DDR2-533/667 MHz (PC2-4300/5400) SDRAM
Cache memory		Level 2 (L2) write-back cache 1 MB
RTC, CMOS setup, & PNP NVRAM retention time *(Typical)*	B01	>5 years battery life, lithium battery
	B02, B03	>3 years battery life, lithium battery

Table 22: TLA7PC1 Internal specifications (cont.)

Characteristic		Description
Hard disk drive		Standard PC compatible IDE hard disk drive residing on an EIDE interface.
	Size	80 GB, continually subject to change due to the fast-moving PC component environment.
	Interface	SATA, native
	Average seek time	Read 9 ms Write 10 ms
DVD-ROM/CD-RW drive		Standard PC compatible IDE DVD/CD-RW drive residing on an EIDE interface. The initial drive was a Teac DV-W28E793 with +R/RW and –R/RW. Continually subject to change due to the fast-moving PC component environment.
External display drive	B01	Can drive two external video displays via DVI connectors. One DVI port with DVI digital only, other port with DVI digital and analog VGA signaling via an adapter. DVI has maximum resolution of 1600 x 1200 pixels; with 256, 16-bit, or 32-bit colors; and refresh rates of 60 Hz, 75 Hz, or 85 Hz. Analog VGA has maximum resolution of 1600 x 1200 with 32-bit colors at 75 Hz refresh rate.
	B02, B03	One VGA, SVGA, or XGA-compatible analog output port, with maximum resolution of 2048 x 1536 pixels at 85 Hz refresh rate
Source voltage and frequency		100 V_{RMS} to 240 V_{RMS} ±10%, 50 Hz to 60 Hz
Fuse		Internal
Maximum power consumption		400 W
Steady-state input current		8 A_{RMS} maximum at 100 $VAC_{RMS,}$ 5 A_{RMS} maximum at 240 VAC_{RMS}

Table 23: External controls and connectors

Characteristic		Description
USB ports		Four USB 2.0 ports
PS2 ports	B01	None
	B02	Keyboard and mouse connectors in rear; one common PS2 connector in front
On/Standby switch		Switch used to power on the instrument
I/O Indicators		LEDs for power on/off, HDD activity, and fan alarm
CPU reset switch		Hardware reset for the PC
Alarm reset switch		Reset switch for the system fan and over temperature monitor circuitry
Video Ports	B01	One DVI-I connector and one DVI-D connector
	B02, B03	One analog SVGA connector
LAN Ports		Two RJ45 with integrated green and yellow/amber LEDs located above the USB connectors
Audio Ports		Two vertical 3.5 mm audio-jack stack. Line Output (top, lime) capable of driving headphones, Microphone Input (bottom, pink)

Table 24: TLA7PC1 mechanical

Characteristic		Description
Dimensions	Height	3.5 in (88.9 mm)
	Width	17.1 in (434.3 mm)
	Depth	24 in (609.6 mm)
Weight		24 lbs 12 oz (11.25 kg)
Shipping configuration		35 lbs (15.9 kg)
Construction materials		Chassis parts are constructed of steel alloy and trim peaces are constructed of plastic; circuit boards are constructed of glass laminate.
Finish type		Tektronix silver-gray

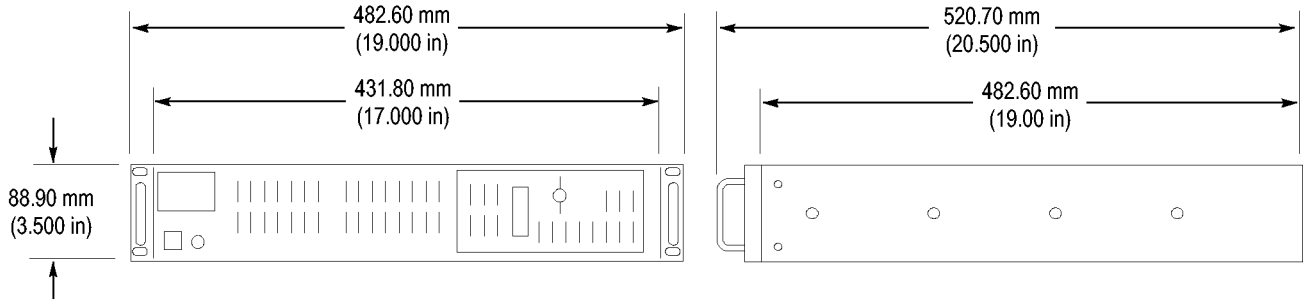


Figure 4: Dimensions of the TLA7PC1 Benchtop PC Controller

TL708EX TekLink 8-Port Hub Characteristics

Table 25: TL708 EX TekLink 8-Port Hub signal switching characteristics

Characteristic		Description
TekLink cable assembly delay characteristics *(Typical)*	Shielded twisted pairs (EVT0, EVT1, EVT2)	9.5 ns
	Non-shielded twisted pairs (EVT3, EVT4, EVT5, EVT6)	10.5 ns
TekLink Port In to Port Out delays *(Typical)*	REF_CLK (EVT0) delay	5 ns
	Typical system trigger (EVT1) delay	15 ns
TekLink REF_CLK out to Run out delay *(Typical)*		REF_CLK out leads Run out by 5 ns
TekLink input signal characteristics *(Typical)*		LVDS compatible inputs through the front-panel 40-pin connector
	Input destination	EVT0_IN_POS/NEG to EVT6_IN_POS/NEG
	Input levels	LVDS compatible input
TekLink output signal characteristics *(Typical)*		LVDS compatible outputs through the front-panel 40-pin connector
	Output destination	EVT0_OUT_POS/NEG to EVT6_OUT_POS/NEG
	Output levels	LVDS compatible output
	Vod (voltage out differential)	247 mV minimum 454 mV maximum
	Vos	1.125 V minimum 1.375 V maximum
TekLink AUX_PWR *(Typical)*		4.3 V power bi-directional diode isolated 1.3 A maximum output available
TekLink real-time interface bus		Connector supports Reference Clock (10 MHz), Local 10/100 LAN connection, Power On Signaling, Run event, System Trigger, General purpose events

Table 26: TL708EX TekLink 8-Port Hub AC power source characteristics

Characteristic	Description
Source voltage and frequency	100 V_{RMS} to 240 V_{RMS} ±10%, 47 Hz to 63 Hz
Maximum power consumption	110 W
Steady state input current	0.9 A_{RMS} maximum at 120 VAC_{RMS} at 80 W
Inrush surge current	At 120 VAC, 18 A maximum At 230 VAC, 35 A maximum
Power factor correction	Yes

Table 27: TL708EX TekLink 8-Port Hub atmospherics

Characteristic		Description
Temperature	Operating	0 °C to +50 °C, 11 °C/hr maximum gradient, non-condensing (derated 1 °C per 305m (1000 ft) above 1524 m (5000 ft) altitude)
	Non-operating	-40 °C to +71 °C, 15 °C/hr maximum gradient, non-condensing
Humidity	Operating & Non-operating	5% to 95% relative humidity, non-condensing 75% above 30 °C 45% above 40 °C
Altitude	Operating	To 3000 m (9843 ft)
	Non-operating	To 12,000 m (40,000 ft)

Table 28: TL708EX TekLink 8-Port Hub miscellaneous

Characteristic	Description
Cooling system	Forced-air circulation system with no removable filters using two fans operating in parallel
Transportation Package Material	Transportation Package material meets recycling criteria as described in Environmental Guidelines for Package Design (Tektronix part number 063-1290-00) and Environmentally Responsible Packaging Handbook (Tektronix part number 063-1302-00).
Cooling clearance	153 mm (6 in) on back for adequate cooling

Table 29: TL708EX TekLink 8-Port Hub mechanical

Characteristics		Description	
Classification		Portable instrument intended for design and development bench and lab based applications	
Dimensions		*Benchtop Configuration*	*Rackmount Configuration*
	Height	50.8 mm (2.0 in)	44.5 mm (1.75 in)
	Width	444.5 mm (17.5 in)	482.6 mm (19 in)
	Depth	317.5 mm (12.5 in)	298.5 mm (11.75 in)
Weight		2.7 kg (5 lbs 14 oz) minimum configuration with power cord and accessories	
Shipping weight		4.66 kg (10 lbs 4 oz) minimum configuration	
Construction material		Chassis parts are constructed of aluminum alloy; circuit boards constructed of glass laminate.	
Finish type		Tektronix silver-gray	

TLA700 System Specifications

The following tables list the specifications common to the TLA715 and TLA721 logic analyzers. Refer to the individual logic analyzers section for detailed specifications.

Table 30: TLA700 Backplane interface

Characteristic		Description
Slots	Portable mainframe	4
	Benchtop mainframe	10 (three slots taken up by the controller module)
	Expansion mainframe	13
✓ CLK10 Frequency		10 MHz ±100 ppm
Relative Time Correlation Error [1] [2] *(Typical)*	TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx "MagniVu" data	2 ns
	TLA7Axx/TLA7NAx to TLA7AxxTLA7NAx "MagniVu" data	2 ns
	TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx "MagniVu" data	-3 ns
	TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx "normal" data using asynchronous sampling	1 TLA7Lx/Mx/Nx/Px/Qx sample – 0.5 ns
	TLA7Axx/TLA7NAx to TLA7Axx "normal" data using asynchronous sampling	1 TLA7Axx/TLA7NAx sample – 0.5 ns
	TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx "normal" data using asynchronous sampling	1 TLA7Lx/Mx/Nx/Px/Qx sample – 0.5 ns
	TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx "normal" data using an external clock	2 ns
	TLA7Axx/TLA7NAx to TLA7Axx/TLA7NAx "normal" data using an external clock	2 ns
	TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx "normal" data using an external clock	4 ns
	TLA7Lx/Mx/Nx/Px/Qx "MagniVu" to DSO data	3 ns
	TLA7Axx/TLA7NAx "MagniVu" to DSO data	2 ns
	TLA7Lx/Mx/Nx/Px/Qx to DSO "normal" data using asynchronous sampling [3]	1 TLA7Lx/Mx/Nx/Px/Qx sample + 2 ns
	TLA7Axx/TLA7NAx to DSO "normal" data using asynchronous sampling [3]	1 TLA7Axx/TLA7NAx sample + 2 ns
	TLA7Lx/Mx/Nx/Px/Qx to DSO "normal" data using an external clock [3]	3 ns
	TLA7Axx/TLA7NAx to DSO "normal" data using an external clock [3]	2 ns
	DSO to DSO [3]	3 ns

[1] Includes typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a "typical" number for the measurement. Assumes standard accessory probes are utilized.

2 For time intervals longer than 1 µs between modules, add 0.01% of the difference between the absolute time measurements to the relative time correlation error to account for the inaccuracy of the CLK10 source.

3 The DSO module time correlation is measured at the maximum sample rate on one channel only.

Table 31: TLA700 Backplane latencies

Characteristic		Description	
System trigger and external signal input latencies [2] *(Typical)*			
		Portable mainframe and benchtop mainframe	*Expansion*
External system trigger input to TLA7Lx/Mx/Nx/Px/Qx probe tip [4]		-266 ns	-230 ns
External system trigger input to TLA7Axx probe tip [4]		-653 ns	-617 ns
External signal input to TLA7Lx/Mx/Nx/Px/Qx probe tip via Signal 3, 4 [5]		-212 ns + Clk	-176 ns + Clk
External signal input to TLA7Axx/TLA7NAx probe tip via Signal 3, 4 [5]		-212 ns + Clk	-176 ns + Clk
External signal input to TLA7Lx/Mx/Nx/Px/Qx probe tip via Signal 1, 2 [5 6]		-634 ns + Clk	-596 ns + Clk
External signal input to TLA7Axx/TLA7NAx probe tip via Signal 1, 2 [5 6]		-636 ns + Clk	-615 ns + Clk
External system trigger input to DSO probe tip [4]		-25 ns	11 ns
System trigger and external signal output latencies [1] *(Typical)*			
TLA7Lx/Mx/Nx/Px/Qx probe tip to external system trigger out		376 ns + SMPL	412 ns + SMPL
TLA7Axx/TLA7NAx probe tip to external system trigger out		794 ns + SMPL	830 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx probe tip to external signal out via Signal 3, 4 [3]	OR function	366 ns + SMPL	402 ns + SMPL
	AND function	379 ns + SMPL	415 ns + SMPL
TLA7Axx/TLA7NAx probe tip to external signal out via Signal 3, 4 [3]	OR function	792 ns + SMPL	828 ns + SMPL
	AND function	800 ns + SMPL	836 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx probe tip to external signal out via Signal 1, 2 [3 6]	normal function	364 ns + SMPL	385 ns + SMPL
	inverted logic on backplane	364 ns + SMPL	385 ns + SMPL
TLA7Axx/TLA7NAx probe tip to external signal out via Signal 1, 2 [3 6]	normal function	796 ns + SMPL	817 ns + SMPL
	inverted logic on backplane	796 ns + SMPL	817 ns + SMPL
DSO probe tip to external system trigger out		68 ns	104 ns
DSO Probe tip to external signal out via Signal 3, 4 [3]	OR function	65 ns	101 ns
	AND function	75 ns	111 ns
DSO probe tip to external signal out via Signal 1, 2 [3 6]	normal function	68 ns	89 ns
	inverted logic on backplane	71 ns	92 ns
Inter-module latencies *(Typical)*			
TLA7Lx/Mx/Nx/Px/Qx to DSO inter-module system trigger [1 4]		358 ns + SMPL	394 ns + SMPL
TLA7Axx/TLA7NAx to DSO inter-module system trigger [1 4]		772 ns + SMPL	808 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module system trigger [1 4]		66 ns + SMPL	102 ns + SMPL
TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx inter-module system trigger [1 4]		479 ns + SMPL	515 ns + SMPL
TLA7Axx/TLA7NAx to TLA7Axx/TLA7NAx inter-module system trigger [1 4]		116 ns + SMPL	152 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to DSO inter-module ARM [1]		360 ns + SMPL	396 ns + SMPL

Table 31: TLA700 Backplane latencies (cont.)

Characteristic	Description	
TLA7Axx/TLA7NAx to DSO inter-module ARM [1]	779 ns + SMPL	815 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM [1 5]	108 ns + SMPL + Clk	144 ns + SMPL + Clk
TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM [1 5]	479 ns + SMPL + Clk	533 ns + SMPL + Clk
TLA7Axx/TLA7NAx to TLA7Axx inter-module ARM [1 5]	111 ns + SMPL + Clk	147 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2 [1 5 6]	116 ns + SMPL + Clk	137 ns + SMPL + Clk
TLA7Axx/TLA7NAx to TLA7Axx inter-module via Signal 1, 2 [1 5 6]	113 ns + SMPL + Clk	134 ns + SMPL + Clk
TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2 [1 5 6]	534 ns + SMPL + Clk	555 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Q to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4 [1 5]	116 ns + SMPL + Clk	152 ns + SMPL + Clk
TLA7AxxTLA7NAx to TLA7Axx inter-module via Signal 3, 4 [1 5]	124 ns + SMPL + Clk	160 ns + SMPL + Clk
TLA7Axx/TLA7NAx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4 [1 5]	545 ns + SMPL + Clk	581 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx/TLA7NAx inter-module System Trigger [1 4]	-287 ns + SMPL	-251 ns + SMPL
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module System Trigger [4]	-240 ns	-204 ns
DSO to TLA7Axx/TLA7NAx inter-module System Trigger [4]	-598 ns	-562 ns
DSO to DSO inter-module System Trigger [4]	50 ns	86 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx/TLA7NAx inter-module ARM [1 5]	-300 ns + SMPL + Clk	-264 ns + SMPL + Clk
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM [5]	-192 ns + Clk	-156 ns + Clk
DSO to TLA7Axx/TLA7NAx inter-module ARM [5]	-600 ns + Clk	-564 ns + Clk
DSO to DSO inter-module ARM	59 ns	95 ns
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2 [5 6]	-179 ns + Clk	-158 ns + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx/TLA7NAx inter-module via Signal 1, 2 [1 5 6]	-294 ns + SMPL + Clk	-273 ns + SMPL + Clk
DSO to TLA7Axx/TLA7NAx inter-module via Signal 1, 2 [5 6]	-598ns + Clk	-577 ns + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx/TLA7NAx inter-module via Signal 3, 4 [1 5]	-294 ns + SMPL + Clk	-258 ns + SMPL + Clk
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4 [5]	-184 ns + Clk	-148 ns + Clk
DSO to TLA7Axx/TLA7NAx inter-module via Signal 3, 4 [5]	-598 ns + Clk	-562 ns + Clk

1 SMPL represents the time from the event at the probe tip inputs to the next valid data sample of the LA module. With Normal asynchronous sampling, this represents the delta time to the next sample clock. With MagniVu asynchronous sampling, this represents 500 ps or less. With synchronous sampling, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

2 All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.

3 All signal output latencies are validated to the rising edge of an active (true) high output.

4 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

5 "Clk" represents the time to the next master clock at the destination logic analyzer. With asynchronous sampling, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. With the synchronous sampling, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.

6 Signals 1 and 2 are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.

Table 32: TLA700 External signal interface

Characteristic		Description	
System Trigger Input		TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Input Levels	TTL compatible input	
	V_{IH}	≥ 2.0 V	
	V_{IL}	≤ 0.8 V	
	Input destination	System trigger	
	Input Mode	Falling edge sensitive, latched (active low)	
	Minimum Pulse Width	12 ns	
	Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods	
	Maximum Input Voltage	0 to +5 V peak	
External Signal Input		TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Input Destination	Signal 1, 2	
		Signal 3, 4	
	Input Levels	TTL compatible input	
	V_{IH}	≥ 2.0 V	
	V_{IL}	≤ 0.8 V	
	Input Mode	Active (true) low, level sensitive	
	Input Bandwidth [1]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Accepts signals during valid acquisition periods via real-time gating	
	Maximum Input Voltage	0 to +5 V peak	
System Trigger Output		TTL compatible output via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Source selection	System trigger	
	Source Mode	Active (true) low, falling edge latched	
	Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions	
	Output Levels	50 Ω back terminated TTL-compatible output	
	V_{OH}	≥4 V into open circuit	
		≥2 V into 50 Ω to ground	
	V_{OL}	≤ 0.7 V sinking 10 mA	
	Output Protection	Short-circuit protected (to ground)	

Table 32: TLA700 External signal interface (cont.)

Characteristic		Description	
External Signal Output		TTL compatible outputs via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)	
	Source Selection	Signal 1, 2	
		Signal 3, 4	
		10 MHz clock	
	Output Modes Level Sensitive	User definable	
		Active (true) low or active (true) high	
	Output Levels	50 Ω back terminated TTL output	
	V_{OH}	≥ 4 V into open circuit	
		≥2 V into 50 Ω to ground	
	V_{OL}	≤ 0.7 V sinking 10 mA	
	Output Bandwidth [2]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions	
		Outputs 10 MHz clock continuously	
	Output Protection	Short-circuit protected (to ground)	
Intermodule Signal Line Bandwidth		Minimum bandwidth up to which the intermodule signals are specified to operate correctly	
		Signal 1, 2	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum

1 The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

2 The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

TLA715 Dual Monitor Portable Mainframe Specifications

The following tables describe the specifications for the TLA715 Dual Monitor Portable Mainframe.

Table 33: TLA715 Internal controller

Characteristic		Description
Operating system		Microsoft Windows 2000
Microprocessor		Intel Pentium PC-AT configuration with an Intel 815E chip-set and a 733 MHz Pentium III processor
Main memory		SDRAM
	Style	144 pin SO DIMM, 2 sockets, gold plated, 1.25-inch (3.175 cm) maximum height
	Speed	133 MHz
	Available configurations	32, 64, 128, 256 MB per SO DIMM
	Installed configurations	512 MB with both sockets loaded
Cache memory		256 KByte Level 2 (L2) write-back cache
Flash BIOS		256 KByte
Real-time clock and CMOS setups NVRAM		Real-time clock/calendar, standard and advanced PC CMOS setups; see BIOS specification
RTC, CMOS setup, & PNP NVRAM retention time *(Typical)*		> 10 years battery life, lithium battery
Floppy disk drive		Standard 3.5 inch 1.44 MB PC compatible high-density, double-sided floppy disk drive, 500 Kb/sec transfer rate
Bootable replaceable hard disk drive		Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface.
	Size	40 GB Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
	Interface	ATA -5/enhanced IDE (EIDE)
	Average seek time	Read, 12 ms
	Average latency	7/14 ms
	I/O data transfer rate	33.3 Mbps maximum (U-DMA mode 2)
	Cache buffer	2 MB (30 GB) /512 KB (10 GB)
CD-RW drive		Standard PC compatible IDE (Integrated device Electronics) 8x-8x-24x CD-RW drive residing on an IDE interface. Continually subject to change due to the fast-moving PC component environment.

Table 34: TLA715 display system

Characteristic		Description		
Classification		Standard PC graphics-accelerator technology capable of supporting both internal color LCD display and two external color VGA, SVGA, or XGA monitors		
Display memory		4 MB SDRAM clocked up to 100 MHz, no external video memory		
Display selection		Hardware sense of external SVGA monitor during BIOS boot sequence; defaults to internal color LCD display (indicated by two beeps); automatically switches to external SVGA monitor, if attached (indicated by one beep). Dual (simultaneous) display of external SVGA monitor and internal color LCD is possible via special CMOS "simulscan" setup, as long as internal and external displays operate at same resolution (limited to 800x600 on current LCD) and display rates (simulscan mode indicated by three beeps). Four beeps during the BIOS boot indicates a monochrome LCD was found (not supported). Five beeps indicates no recognizable LCD or external monitor was found. Dynamic Display Configuration 1 (DDC1) support for external SVGA monitor is provided.		
External display drive		Two VGA, SVGA, or XGA-compatible analog output ports. Display size is selected via Win2000 display applet.		
	Display Size (Primary video port with Silicon motion chip)	*Resolution (Pixels)*	*Colors*	*Refresh Rates*
		640 x 480	256, 64 K, 16.8 M	60, 75, 85
		800 x 600	265, 64 K, 16.8 M	60, 75, 85
		1024 x 768	256, 64 K, 16.8 M	60, 75, 85
		1280 x 1024	256, 64 K, 16.8 M	60
		1600 x 600	256, 64 K	60
		1600 x 1200	256, 64 K	60
	(Secondary video port with 815E chip set)	*Resolution (Pixels)*	*Colors*	*Refresh Rates*
		640 x 480	256, 64 K, 16.8 M	60, 75, 85
		800 x 600	256, 64 K, 16.8 M	60, 75, 85
		1024 x 768	256, 64 K, 16.8 M	60, 75, 85
		1280 x 1024	256, 64 K, 16.8 M	60, 75, 80
		1600 x 1200	256	60, 75
Internal display	Classification	TFT (Thin Film Transistor) 26 cm active-matrix color LCD display, CCFL backlight, intensity controllable via software		
	Resolution	800 X 600, 262, 144 colors with 211.2 mm (8.3 in) by 158.4 mm (6.2 in) of viewing area		
	Color scale	262, 144 colors (6-bit RGB) with a color gamut of 42% at center to NTSC		

Table 35: TLA715 front-panel interface

Characteristic		Description
QWERTY Keypad		31-key ASCII to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
HEX Keypad		25-key HEX supporting standard DSO and LA entry functions
Special function knobs	Multi-function knob	Various increment/decrement functions dependent on screen or window type
	Vertical position	Scrolling and positioning dependent on display type
	Vertical scale	Scales waveform displays only
	Horizontal position	Scrolling and positioning dependent on display type
	Horizontal scale	Scales waveform displays only
Integrated pointing device		Vertically mounted Trackball with two control buttons (SELECT and MENU)
USB port		Front panel (lower left-hand side) dual USB connector
Mouse Port		PS/2 compatible pointing device port
Keyboard Port		PS/2 compatible keyboard port

Table 36: TLA715 rear-panel interface

Characteristic	Description
Parallel interface port	36-pin high-density connector supports Output only, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP) Complies with IEEE P1284-C/D2 for bi-directional Parallel Peripheral Interface for Personal Computers (draft) style 1284-C
Serial interface port	9-pin male sub-D connector to support RS-232 serial port
SVGA output Port 1 and Port 2	Two 15-pin sub-D SVGA connectors
PC CardBus32 port	Standard Type I, II, III PC-compatible, PC card slot Complies with PCMCIA 2.1 and JEIDA 4.1

Table 37: TLA715 AC power source

Characteristic		Description
Source voltage and frequency		100 V_{RMS} to 240 V_{RMS} ±10%, 45 Hz to 66 Hz 100 V_{RMS} to 120 V_{RMS}, 360 Hz to 440 Hz
Fuse rating	90 V to 250 V operation (159-0046-00)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
	90 V to 250 V operation (159-0381-00)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum power consumption		600 W
Steady-state input current		6 A_{RMS} maximum at 90 VAC_{RMS}, 60 Hz or 100 VAC_{RMS}, 400 Hz
Inrush surge current		70 A maximum
Power factor correction		Yes

Table 37: TLA715 AC power source (cont.)

Characteristic	Description
On/Sleep indicator	Green/yellow front panel LED located next to On/Standby switch provides visual feedback when the On/Off switch is actuated. When the LED is green, the instrument is powered and the processor is not sleeping. When the LED is yellow, the instrument is powered, but the processor is sleeping.
On/Standby switch and indicator	Front panel On/Standby switch. Users can push the switch to power down the instrument without going through the Windows shutdown process; the instrument normally powers down. The power cord provides main power disconnect.

Table 38: TLA715 cooling

Characteristic	Description
Cooling system	Forced air circulation system with no removable filters using six fans operating in parallel
Pressurization	Negative pressurization system in all chambers including modules
Slot activation	Installing a module activates the cooling for the corresponding occupied slots by opening the airflow shutter mechanism. Optimizes cooling efficiency by only applying airflow to installed modules.
Air intake	Front sides and bottom
Air exhaust	Back rear
Cooling clearance	2 inches (51 mm) front, sides, top, and rear. Prevent blockage of airflow to bottom of instrument by placing on a solid, noncompressable surface; can be operated on rear feet.
Fan speed and operation	All fans operational at half their rated potential and speed (12 VDC)

Table 39: TLA715 mechanical

Characteristic		Description
Overall dimensions		Dimensions are without front feet extended, front cover attached, pouch attached, nor power cord attached.
	Height (with feet)	9.25 in (23.5 cm)
	Width	17 in (43.18 cm)
	Depth	17.5 in (44.45 cm)
Weight		30 lbs 12 oz (13.9 kg) with no modules installed, two dual-wide slot covers, and empty pouch
Shipping configuration		60 lbs 13 oz (27.58 kg) minimum configuration (no modules), with all standard accessories 86 lbs 9 oz (39.26 kg) full configuration, with two TLA 7P4 modules and standard accessories (including probes and clips)
Acoustic noise level *(Typical)*		42.7 dBA weighted (operator) 37.0 dBA weighted (bystander)

Table 39: TLA715 mechanical (cont.)

Characteristic	Description
Construction materials	Chassis parts are constructed of aluminum alloy; front panel and trim peaces are constructed of plastic; circuit boards are constructed of glass.
Finish type	Tektronix blue body and Tektronix silver-gray trim and front with black pouch, FDD feet, handle, and miscellaneous trim pieces

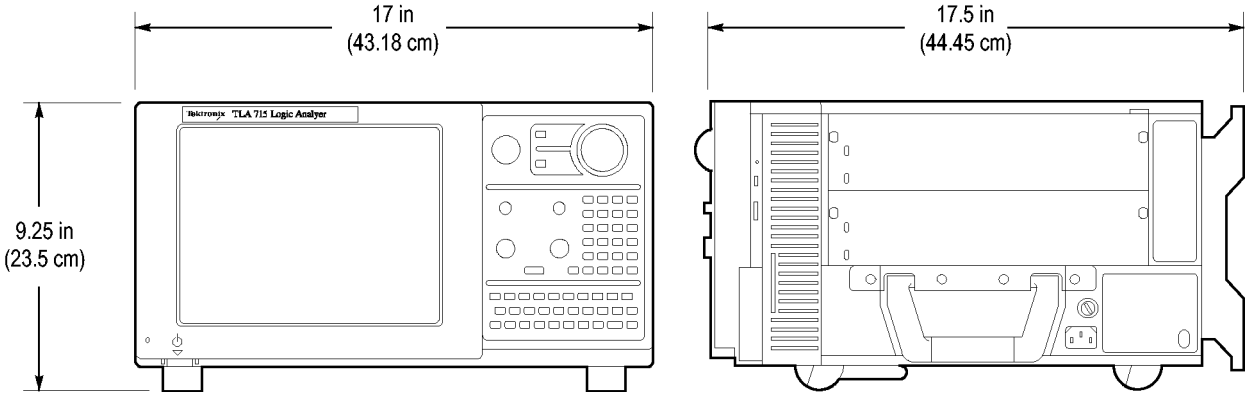


Figure 5: Dimensions of TLA715 Portable mainframe

Benchtop and Expansion Mainframe Specifications

The following tables list the specifications for the TLA721 Benchtop mainframe and the TLA7XM expansion mainframe.

Table 40: Benchtop and expansion mainframe AC power source

Characteristic		Description
Source Voltage		100 V_{RMS} to 240 V_{RMS} ±10%, 45 Hz to 66 Hz 100 V_{RMS} to 120 V_{RMS}, 360 Hz to 440 Hz
Maximum Power Consumption		1450 W line power (the maximum power consumed by a fully loaded 13-slot instrument)
Fuse Rating (Current and voltage ratings and type of fuse used to fuse the source line voltage)	90 V - 132 VAC_{RMS} Operation High-power/Low Line (159-0379-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: Slow acting Rating: 20 A/250 V
	103 V - 250 VAC_{RMS} Operation (159-0256-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: No. 59/Fast acting Rating: 15 A/250 V
	207 V - 250 VAC_{RMS} Operation (159-0381-00)	Safety: IEC 127/Sheet 1 Size: 5 mm × 20 mm Style: Fast acting "F", high-breaking capacity Rating: 6.3 A/250 V
Inrush Surge Current		70 A maximum
Steady State Input Current		16.5 A_{RMS} maximum at 90 VAC_{RMS} 6.3 A_{RMS} maximum at 207 VAC_{RMS}
Power Factor Correction *(Typical)*		0.99 at 60 Hz operation and 0.95 at 400 Hz operation
ON/Standby Switch and Indicator		Front Panel On/Standby switch with integral power indicator

Table 41: Benchtop and expansion mainframe cooling

Characteristic	Description
Cooling system	Forced air circulation system (positive pressurization) using a single low-noise centripetal (squirrel cage) fan configuration with no filters for the power supply and 13 module slots.
Fan speed control	Rear panel switch selects between full speed and variable speed. Slot exhaust temperature and ambient air temperature are monitored such that a constant delta temperature is maintained.
Slot activation	Installing a module activates the cooling for the corresponding occupied slots by opening the air flow shutter mechanism. Optimizes cooling efficiency by only applying airflow to modules that are installed.
Pressurization	Positive pressurization system, all chambers including modules

Table 41: Benchtop and expansion mainframe cooling (cont.)

Characteristic	Description
Slot airflow direction	P2 to P1, bottom of module to top of module
Mainframe air intake	Lower fan-pack rear face and bottom
Mainframe air exhaust	Top-sides and top-rear back. Top rear-back exhaust redirected to the sides by the fan pack housing to minimize reentry into the intake.
Δ Temperature readout sensitivity	100 mV/ °C with 0 °C corresponding to 0 V output
Temperature sense range	-10 °C to +90 °C, delta temperature ≤ 50 °C
Clearance	2 in (51 mm), rear, top, and sides
Fan speed readout	RPM = 20 (Tach frequency) or 10 ≥ (+Pulse Width) where (+Pulse Width) is the positive width of the TACH1 fan output signal measured in seconds
Fan speed range	650 to 2250 RPM

Table 42: Enhanced monitor

Characteristic	Description
Voltage readout	+24 V, -24 V, +12 V, -12 V, +5 V, -5.2 V, -2 V, +5 $V_{Standby}$ if present, and +5 $V_{External}$ via RS232
Voltage readout accuracy *(Typical)*	±3% maximum
Current readout	Readout of the present current on the +24 V, -24 V, +12 V, -12 V, +5 V, -2 V, -5.2 V rails via RS232
Current readout accuracy *(Typical)*	±5% of maximum power supply I_{mp}
Rear panel connector levels	±25 VDC maximum, 1 A maximum per pin (Provides access for RS-232 host to enhanced monitor)

Table 43: Benchtop and expansion mainframe mechanical

Characteristic			Description
Overall Dimensions	Standard	Height	13.7 in (346.7 mm) including feet
		Width	16.7 in (424.2 mm)
		Depth	26.5 in (673.1 mm)
	Rackmount	Height	13.25 in (336.6 mm)
		Width	18.9 in (480.1 mm)
		Depth	28.9 in to 33.9 in (734.1 mm to 861.1 mm) in 0.5 in increments, user selectable
Benchtop controller dimensions		Height	10.32 in (262.1 mm)
		Width	2.39 in (60.7 mm)
		Depth	14.75 in (373.4 mm)
Expansion module dimensions		Height	10.32 in (262.1 mm)
		Width	1.25 in (31.75 mm)
		Depth	14.75 in (373.4 mm)

Table 43: Benchtop and expansion mainframe mechanical (cont.)

Characteristic		Description
Weight	Mainframe with benchtop controller and slot fillers *(Typical)*	58 lbs 11 oz. (26.7 kg)
	Shipping configuration *(Typical)*	60 lbs 11 oz. (26.7 kg) minimum configuration with controller (only) and all standard accessories (two manuals, five dual-wide and one single-wide slot filler panels, power cord, empty pouch, front cover, keyboard, software, and cables) 187 lbs (85 kg) fully configured, same as above with the addition of five LA modules (four TLA7P4 modules, one TLA7N4 module) and all module standard accessories (probes and clips)
	Benchtop controller	6 lbs 10 oz. (3.0 kg)
	Expansion module	3 lbs (1.4 kg)
	Maximum per slot	5 lbs (2.27 kg)
	Rackmount kit adder	20 lbs (9.1 kg)
Size	Benchtop controller	Three slots wide
	Expansion module	Single slot wide
Acoustic noise level (*Typical*)	Variable fan speed (at 860 RPM)	43.2 dBA weighted (front) 43.8 dBA weighted (back)
	Full speed fan (switched at rear)	66.2 dBA weighted (front) 66.2 dBA weighted (back)
Construction materials		Chassis parts, aluminum alloy Front panel and trim pieces, plastic Circuit boards, glass laminate
Finish type		Mainframes are Tektronix silver gray with dark gray trim on fan pack and bottom feet support rails. Benchtop controllers are Tektronix silver gray on front lexan and injector/ejector assemblies with a black FDD and PC card ejector buttons.

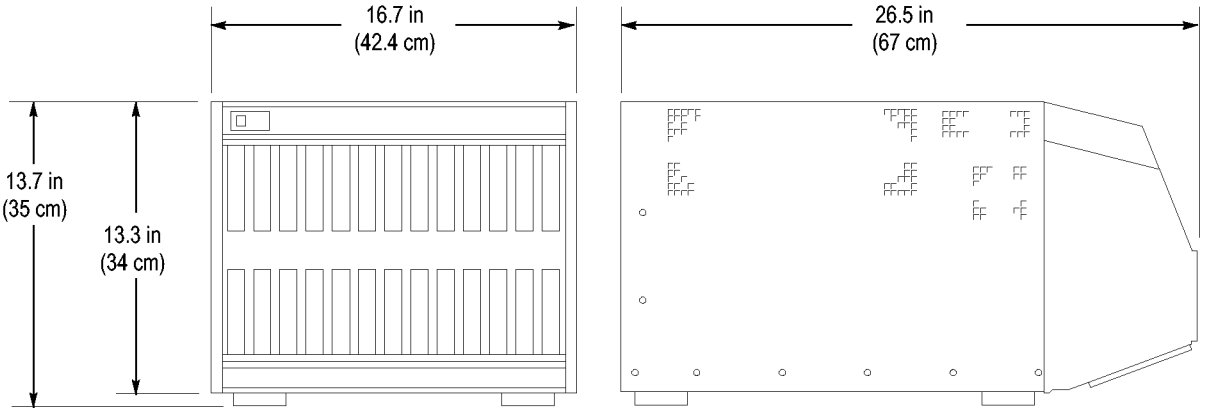


Figure 6: Dimensions of the benchtop and expansion mainframe

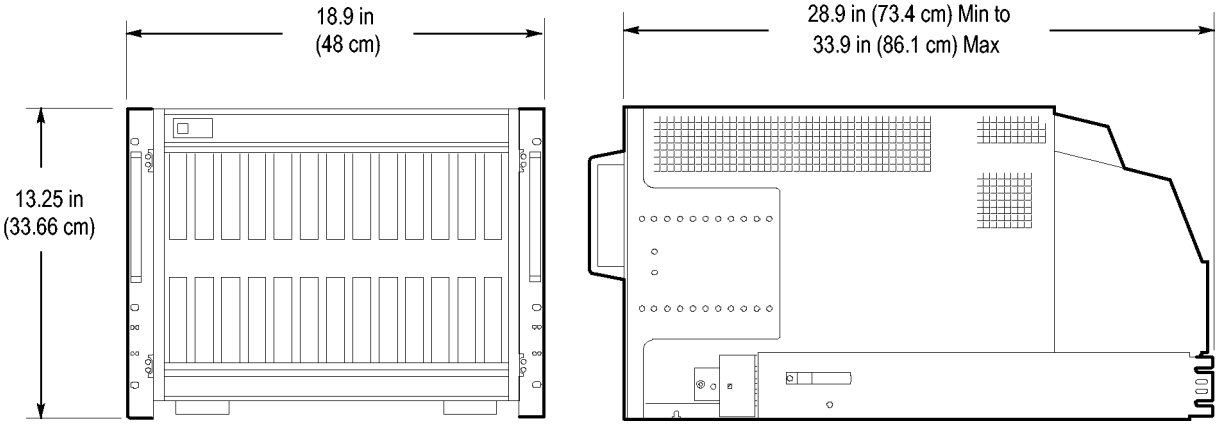


Figure 7: Dimensions of the benchtop and expansion mainframe with rackmount option

TLA721 Dual Monitor Benchtop Controller Specifications

The following tables list the specifications for the TLA721 Dual Monitor Benchtop Controller.

Table 44: TLA721 benchtop controller characteristics

Characteristic		Description
Operating system		Microsoft Windows 2000
Microprocessor		Intel 733 MHz Pentium III configuration with an Intel 815E chip-set
Main memory		Two 144 pin SODIMM sockets support one or two SDRAM modules.
	Available configurations	16, 32, 64, 256 MB per SODIMM
	Installed configuration	512 MB maximum configuration
	Speed	133 MHz
	CAS latency	2, 3
	RAS to CAS delay	2, 3
	RAS precharge	2, 3
	DRAM cycle time	5/7 or 7/9
Cache memory		512 KB, level 2 (L2) write-back cache
Flash BIOS		512 KB Provides PC plug-and-play services with and without Microsoft Windows operating system. Flash based BIOS field upgradable via a floppy disk Forced recovery jumper is provided
Real-time clock and CMOS setups NVRAM		Real-time clock/calendar. Standard and advanced PC CMOS setups: see BIOS specifications
RTC, CMOS setup, & PnP NVRAM retention time *(Typical)*		Battery life is typically > 7 years
Floppy disk drive		Standard 3.5 inch, 1.44 MB, high-density, double-sided, PC-compatible high-density floppy disk drive
	Transfer rate	500 Kb per second
	Access time (ave.)	194 ms

Table 44: TLA721 benchtop controller characteristics (cont.)

Characteristic		Description
Bootable replaceable hard disk drive		Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface
	Size	40 GB Continually subject to change due to the fast-moving PC component environment. This storage capacity valid at product introduction.
	Interface	ATA-5/Enhanced IDE (EIDE)
	Average seek time	Read 12 ms
	I/O data-transfer rate	33.3 MB/s maximum (U-DMA mode 2)
	Average latency	7/14 ms
	Cache buffer	512 KB
CD-RW Drive		Standard PC compatible IDE (Integrated device Electronics) 8x-8x-24x CD-RW drive residing on an IDE interface. Continually subject to change due to the fast-moving PC component environment.
	Applicable formats	CD-DA; CE-ROM Mode 1, Mode 2; CD-ROM XA Mode 2 (Form 1, Form 2); Photo CD (single/multi session); Enhanced CD
	Interface	IDE (ATAPI)
	Average access time	130 ms
	Data-transfer rate (burst sustained)	16.7 MB per second maximum, 1290-3000 KB per second
Display classification		Standard PC graphics accelerator technology (bitBLT based) residing on the Peripheral Component Interconnect (PCI) bus capable of supporting external color VGA, SVGA, or XGA monitors.

Table 44: TLA721 benchtop controller characteristics (cont.)

Characteristic		Description		
Display configuration		Hardware automatically senses a missing flat panel LCD in the benchtop mainframe and defaults to the external SVGA monitor output during the BIOS boot sequence (no internal TFT LCD display exists). This is indicated by a single beep during the boot sequence. Dynamic Display Configuration 1 (DDC1) support for the external monitor is provided.		
Display memory		4 MB SDRAM is on board the video controller; no external video memory		
Display drive		Two VGA, SVGA, or XGA compatible analog output ports		
Display size		User selected via Microsoft Windows Plug and Play support for DDC1 and DDC2 A and B		
	(Primary video port with Silicon Motion Chip)	*Resolution (Pixels)*	*Colors*	*Refresh Rates*
		640 x 480	256, 64 K, 16.8 M	60, 75, 85
		800 x 600	256, 64 K, 16.8 M	60, 75, 85
		1024 x768	256, 64 K, 16.8 M	60, 75, 85
		1280 x 1024	256, 64 K, 16.8 M	60
		1600 x 600	256, 64 K	60
		1600 x 1200	256, 64 K	60
	(Secondary video port with 815E Chip set)	*Resolution (Pixels)*	*Colors*	*Refresh Rates*
		640 x 480	256, 64 K, 16.8 M	60, 75, 85
		800 x 600	256, 64 K, 16.8 M	60, 75, 85
		1024 x768	256, 64 K, 16.8 M	60, 75, 85
		1280 x 1024	256, 64 K, 16.8 M	60, 75, 85
		1600 x 1200	256	60, 75

Table 45: Front panel characteristics

Characteristic	Description
SVGA output port (SVGA)	Two 15-pin sub-D SVGA connectors
Dual USB ports	Two USB (Universal Serial Bus) compliant ports
Mouse port	Front panel mounted PS2 compatible mouse port utilizing a mini DIN connector
Keyboard port	Front panel mounted PS2 compatible keyboard port utilizing a mini DIN connector
Parallel interface port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial interface port (COM)	9-pin male sub-D connector to support an RS232 serial port
PC CardBus32 port	Standard Type I and II PC compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC compatible PC card slot

TLA600 Series Specifications

The following tables list the specifications for the TLA600 series logic analyzer.

Table 46: TLA600 input parameters with probes

Characteristic	Description	
✓ Threshold Accuracy	±100 mV	
Threshold range and step size	Settable from +5 V to -2 V in 50 mV steps	
Threshold channel selection	16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).	
✓ Channel-to-channel skew	≤ 1.6 ns maximum	
Channel-to-channel skew *(Typical)*	≤ 1.0 ns	
Sample uncertainty	*Asynchronous*	*Synchronous*
	Sample period	500 ps
Probe input resistance *(Typical)*	20 kΩ	
Probe input capacitance: P6417, P6434 *(Typical)*	2 pF	
Probe input capacitance: P6418 (Typical)	1.4 pF data channels 2 pF CLK/Qual channels	
Minimum slew rate *(Typical)*	0.2 V/ns	
Maximum operating signal	6.5 V_{p-p} -3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum	
Probe overdrive: P6417, P6418 P6434	±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±300 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±4 V maximum beyond threshold	
Maximum nondestructive input signal to probe	±15 V	
Minimum input pulse width signal (single channel) *(Typical)*	2 ns	
Delay time from probe tip to input probe connector *(Typical)*	7.33 ns	

Table 47: TLA600 timing latencies

Characteristic		Description
System Trigger and External Signal Input Latencies [1] *(Typical)*	External System Trigger Input to LA Probe Tip [2]	-266 ns
	External Signal Input to LA Probe Tip via Signal 3, 4 [3]	-212 ns + Clk
	External Signal Input to LA Probe Tip via Signal 1, 2 [3 4]	-208 ns + Clk

Table 47: TLA600 timing latencies (cont.)

Characteristic		Description	
System Trigger and External Signal Output Latencies *(Typical)*	LA Probe Tip to External System Trigger Out [5]	376 ns + SMPL	
	LA Probe Tip to External Signal Out via Signal 3, 4 [5]	OR function	366 ns + SMPL
		AND function	379 ns + SMPL
	LA Probe Tip to External Signal Out via Signal 1, 2 [4 5]		
	normal function	364 ns + SMPL	
	inverted logic on backplane	364 ns + SMPL	

1 All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.

2 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

3 "Clk" represents the time to the next master clock at the destination logic analyzer. In the asynchronous (or internal) clock mode, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. In the synchronous (or external) clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.

4 Signals 1 and 2 (ECLTRG0, 1) are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.

5 SMPL represents the time from the event at the probe tip inputs to the next valid data sample. With asynchronous sampling, this represents the delta time to the next sample clock. With MagniVu asynchronous sampling, this represents 500 ps or less. With synchronous sampling, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

Table 48: TLA600 external signal interface

Characteristic		Description	
System Trigger Input		TTL compatible input via rear panel mounted BNC connectors	
	Input Levels	TTL compatible input	
	V_{IH}	≥2.0 V	
	V_{IL}	≤ 0.8 V	
	Input Mode	Falling edge sensitive, latched (active low)	
	Minimum Pulse Width	12 ns	
	Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods	
	Maximum Input Voltage	0 to +5 V peak	
External Signal Input		TTL compatible input via rear panel mounted BNC connectors	
	Input Destination	Signal 1, 2, 3, 4	
	Input Levels	TTL compatible input	
	V_{IH}	≥2.0 V	
	V_{IL}	≤ 0.8 V	
	Input Mode	Active (true) low, level sensitive	
	Input Bandwidth [1]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Accepts signals during valid acquisition periods via real-time gating	
	Maximum Input Voltage	0 to +5 V peak	

Table 48: TLA600 external signal interface (cont.)

Characteristic		Description	
System Trigger Output		TTL compatible output via rear panel mounted BNC connectors	
	Source Mode	Active (true) low, falling edge latched	
	Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions	
	Output Levels	50 Ω back terminated TTL-compatible output	
	V_{OH}	≥4 V into open circuit	
		≥2 V into 50 Ω to ground	
	V_{OL}	≤ 0.7 V sinking 10 mA	
	Output Protection	Short-circuit protected (to ground)	
External Signal Output		TTL compatible outputs via rear panel mounted BNC connectors	
	Source Selection	Signal 1, 2, 3, 4, or 10 MHz clock	
	Output Modes Level Sensitive	User definable	
		Active (true) low or active (true) high	
	Output Levels	50 Ohm back terminated TTL output	
	V_{OH}	≥ 4 V into open circuit	
		≥2 V into 50 Ω to ground	
	V_{OL}	≤ 0.7 V sinking 10 mA	
	Output Bandwidth [2]	*Signal 1, 2*	*Signal 3, 4*
		50 MHz square wave minimum	10 MHz square wave minimum
	Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions	
		Outputs 10 MHz clock continuously	
	Output Protection	Short-circuit protected (to ground)	

[1] The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

[2] The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

Table 49: TLA600 channel width and depth

Characteristic	Description	
Number of channels	*Product*	*Channels*
	TLA601, TLA611, TLA621	32 data and 2 clock
	TLA602, TLA612, TLA622	64 data and 4 clock
	TLA603, TLA613, TLA623	96 data, 4 clock, and 2 qualifier
	TLA604, TLA614, TLA624	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	*Product*	*Memory depth*
	TLA601, TLA602, TLA603, TLA604	64 K or 256 K samples [1]
	TLA611, TLA612, TLA613, TLA614	64 K or 256 K samples [1]
	TLA621, TLA622, TLA623, TLA624	1 M samples

[1] PowerFlex options

Table 50: TLA600 clocking

Characteristic	Description	
Asynchronous sampling		
Sampling period [1]	4 ns to 50 ms in a 1-2-5 sequence	
Minimum recognizable word [2] (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417, P6418, or P6434 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
synchronous sampling		
Number of clock channels [3]	*Product*	*Clock Channels*
	TLA601, TLA611, TLA621	2
	TLA602, TLA612, TLA622	4
	TLA603, TLA613, TLA623	4
	TLA604, TLA614, TLA624	4
Number of qualifier channels [5]	*Product*	*Qualifier Channels*
	TLA601, TLA611, TLA621	0
	TLA602, TLA612, TLA622	0
	TLA603, TLA613, TLA623	2
	TLA604, TLA614, TLA624	4
Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.8 ns Maximum hold time = User interface hold time + 0.2 ns	
	Examples: for a P6417 or a P6418 probe and user interface setup and hold of 2.0/0.0 typical: Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns	
Setup and hold window size (data and qualifiers) *(Typical)*	Channel-to-channel skew (*typical*) + (2 x sample uncertainty) Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns	
Setup and hold window range	For each channel, the setup and hold window can be moved from +8.5 ns (Ts) to -7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.	
Maximum synchronous clock rate [4]	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz (10 ns minimum between active clock edges)	
Demux clocking		

Table 50: TLA600 clocking (cont.)

Characteristic	Description	
TLA603, TLA613, TLA623	Channels multiplex as follows:	
TLA604, TLA614, TLA624	A3(7:0) to	D3(7:0)
	A2(7:0) to	D2(7:0)
	A1(7:0) to	D1(7:0)
	A0(7:0) to	D0(7:0)
TLA601, TLA611, TLA621	Channels multiplex as follows:	
TLA602, TLA612, TLA622	A3(7:0) to	C3(7:0)
	A2(7:0) to	C2(7:0)
	A1(7:0) to	D1(7:0) TLA602, TLA612, TLA622
	A0(7:0) to	D0(7:0) TLA602, TLA612, TLA622
Time between DeMux clock edges [4] *(Typical)*	5 ns minimum between Demux clock edges in full-speed mode 10 ns minimum between Demux clock edges in half-speed mode	
Time between DeMux store clock edges [4] *(Typical)*	10 ns minimum between Demux master clock edges in full-speed mode 20 ns minimum between Demux master clock edges in half-speed mode	
Data Rate [4] *(Typical)*	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.	
Clocking state machine		
Pipeline delays	Each channel can be programmed with a pipeline delay of 0 through 3 active clock edges.	

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous sampling only. Setup and hold window specification applies to synchronous sampling only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.

4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.

5 All qualifier channels are stored. For custom clocking there are an additional 4 qualifier channels on C2 3:0 regardless of channel width.

Table 51: TLA600 trigger system

Characteristic	Description	
Triggering Resources		
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available:	
	16 word recognizers	0 range recognizers
	13 word recognizers	1 range recognizer
	10 word recognizers	2 range recognizers
	7 word recognizers	3 range recognizers
	4 word recognizers	4 range recognizers

Table 51: TLA600 trigger system (cont.)

Characteristic	Description
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted.
Glitch detector [1] [2]	Each channel group can be enabled to detect a glitch.
Minimum detectable glitch pulse width *(Typical)*	2.0 ns (single channel with P6417, P6418, or a P6434 probe)
Setup and hold violation detector [1] [3]	Each channel can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector [1]	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample. This mode can be used to create transitional storage selections where all channels are enabled.
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51}. Maximum time is 9.007×10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
External Signal In [1]	A backplane input signal
External Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as External Signal In, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
MagniVu™ acquisition trigger	Triggering of MagniV memory is controlled by the main acquisition trigger
MagniVu™ trigger position	The MagniV trigger position is programmable within 4 ns boundaries and separate from the main acquisition memory trigger position.
Increment counter	Either of the two counter/timers used as counters can be increased.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues from the started or stopped state that it was in prior to the reset.

Table 51: TLA600 trigger system (cont.)

Characteristic	Description
Signal out	A signal sent to the backplane to be used by other instruments
Trigger out	A trigger out signal sent to the backplane to trigger other instruments
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Not allowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous sampling is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous sampling rate is reduced to 10 ns.
Setup and hold violation storage	The acquisition memory can be enabled to store setup and hold violation information with each data sample when synchronous sampling is used. The probe data storage size is reduced by one half (the other half holds the violation information). The maximum clock rate is reduced by half.

1 Each use of External Signal In, glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.

2 Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.

3 Any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns.

Table 52: TLA600 MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory. There are no clocking options.

Table 53: TLA600 Data handling

Characteristic	Description
Nonvolatile memory retention time *(Typical)*	Battery is integral to the NVRAM. Battery life is > 10 years.

Table 54: TLA600 internal controller

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Celeron, 566 MHz

Table 54: TLA600 internal controller (cont.)

Characteristic		Description
Main Memory		SDRAM
	Style	168 pin DIMM, 2 Sockets
	Speed	100 MHz
	Installed Configurations	Minimum 256 MB loaded in one socket
		Maximum 512 MB with both sockets loaded
Real-Time Clock and CMOS Setups, Plug & Play NVRAM Retention Time		Battery life is typically > 3 years when the logic analyzer is not connected to line voltage. When connected to line voltage the life of the battery is extended. Lithium battery, CR3032
Hard Disk Drive		Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface.
	Size	Minimum 10 GB
		Maximum 30 GB
		Continually subject to change due to the fast-moving PC component environment.
		These storage capacities valid at product introduction.
CD-RW Drive		Standard PC compatible IDE (Integrated Device Electronics) 24x-10x-40x CD-RW drive residing on an EIDE interface.
		Continually subject to change due to the fast-moving PC component environment.
Floppy Disk Drive		Standard 3.5 inch 1.44 MB PC compatible high-density, double-sided floppy disk drive.

Table 55: TLA600 display system

Characteristic		Description	
Classification		Standard PC graphics accelerator technology (bitBLT-based); capable of supporting both internal color LCD display and external color SVGA/XGA monitor	
Display Memory		DRAM-based frame-buffer memory	
	Size	2 MB	
Display Selection		Both front panel and external displays can be used simultaneously, each with independent resolutions. Supports Windows dual-monitor capability.	
External Display Drive		One SVGA/XGA-compatible analog output port	
	Display Size	Selected via Windows	
		Plug and Play support for DDC1 and DDC2 A and B	
		Resolution (Pixels)	*Colors*
		640 x 480	256, 64 K, 16.8 M
		800 x 600	256, 64 K, 16.8 M
		1024 x 768	256, 64 K, 8 M
		1280 x 1024	256, 64 K, 8 M

Table 55: TLA600 display system (cont.)

Characteristic		Description
Internal Display	Classification	Thin Film Transistor (TFT) 10.4 inch active-matrix color LCD display; CCFL backlight; intensity controllable via software
	Resolution	800 x 600 pixels
	Color Scale	262,144 colors (6-bit RGB)

Table 56: TLA600 front-panel interface

Characteristic	Description
QWERTY	ASCII to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
Special Function Knobs	Various functions

Table 57: TLA600 rear-panel interface

Characteristic	Description
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM 1)	9-pin male sub-D connector to support RS-232 serial port
Single USB Ports	One USB (Universal Serial Bus) compliant port
SVGA Output Port (SVGA OUT)	15-pin sub-D SVGA connector
Mouse Port	PS/2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	PS/2 compatible keyboard port utilizing a mini DIN connector
Type I and II PC Card Port	Standard Type I and II PC-compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC-compatible PC card slot

Table 58: TLA600 AC power source

Characteristic		Description
Source Voltage and Frequency		90-250 $V_{RMS,}$ 45-66 Hz, continuous range CAT II 100-132 $V_{RMS,}$ 360-440 Hz, continuous range CAT II
Fuse Rating	90 V - 132 V Operation (2 required)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
	90 V - 250 V Operation (2 required)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum Power Consumption		600 Watts line power maximum
Steady-State Input Current		6 A_{RMS} maximum
Inrush Surge Current		70 A maximum
Power Factor Correction		Yes
On/Standby Switch and Indicator		Front Panel On/Standby switch, with indicator. The power cord provides main power disconnect.

Table 59: TLA600 cooling

Characteristic	Description
Cooling System	Forced air circulation (negative pressurization) utilizing six fans operating in parallel
Cooling Clearance	2 in (51 mm), sides and rear; unit should be operated on a flat, unobstructed surface

Table 60: TLA600 mechanical characteristics

Characteristic		Description
Weight		Includes empty accessory pouch and front cover
	TLA614, TLA624, TLA613, and TLA623	18.1 Kg (40 lbs)
	TLA612, TLA622, TLA611, and TLA621	18 Kg (39.75 lbs)
	TLA604 and TLA603	17.6 Kg (38.75 lbs)
	TLA602 and TLA601	17.5 Kg (38.5 lbs)

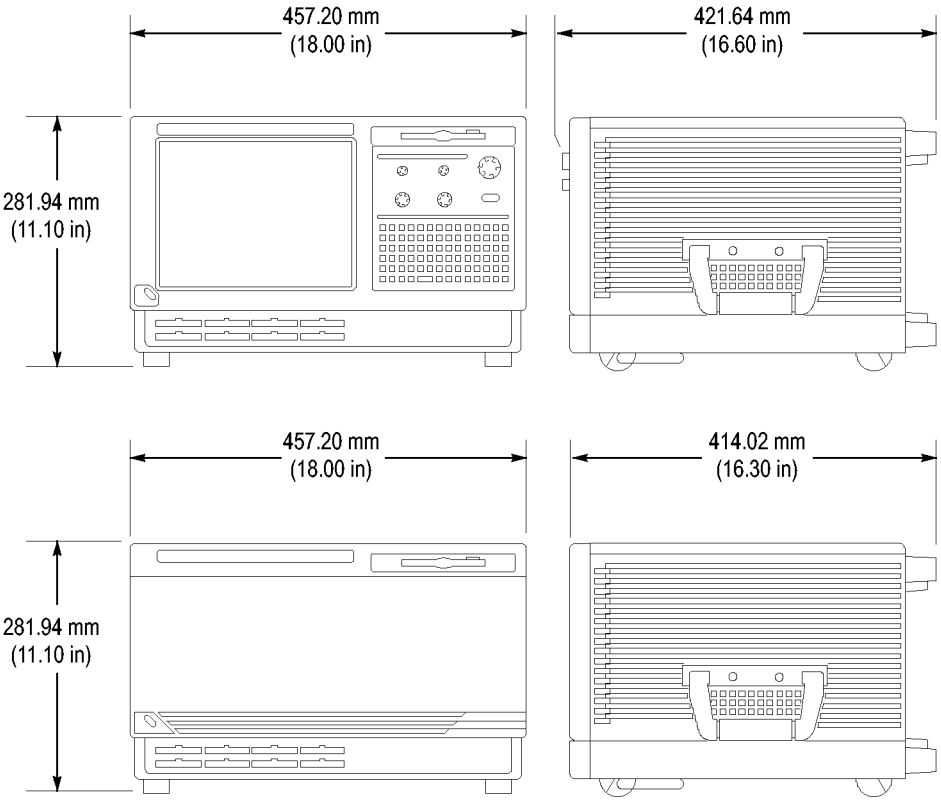


Figure 8: Dimensions of the TLA600 series logic analyzer

TLA7Axx/TLANAx Series Logic Analyzer Module Specifications

The following tables list the specifications of the TLA7Axx/TLA7NAx Series Logic Analyzer modules.

Table 61: TLA7Axx/TLA7NAx input parameters (with probes)

Characteristic		Description	
✓ Threshold accuracy (Certifiable parameter)		± (35 mV + 1% of the threshold voltage setting)	
Threshold range and step size		Settable from +4.5 V to -2.0 V in 5 mV steps	
Threshold channel selection		16 threshold groups assigned to channels. Each probe has four threshold settings, one for each of the clock/qualifier channels and one per group of 16 data channels.	
✓ Channel to channel skew		≤ 400 ps maximum When merged, add the following for slave modules: 0.0 ns when data is acquired on the slave modules through local clocks 125 ps when data is acquired on the slave modules using the master module's clock and merge deskew has been performed. 375 ps when data is acquired on the slave modules using the master module's clock and merge deskew has *NOT* been performed.	
Channel to channel skew *(Typical)*		≤ 300 ps When merged, add the following for slave modules: 0.0 ns when data is acquired on the slave modules through local clocks 125 ps when data is acquired on the slave modules via the master modules' clock and merge deskew has been performed. 375 ps when data is acquired on the slave modules via the master module's clock and merge deskew has *NOT* been performed.	
Sample uncertainty		*Asynchronous*	*Synchronous*
		Sample period	125 ps
Minimum slew rate *(Typical)*		0.2 V/ns	
Input voltage range		-2.5 V to +5 V	
Maximum operating voltage swing		6.0 V peak-to-peak	
Probe overdrive	Single ended probes	± 150 mV or ± 25% of signal swing minimum required beyond threshold, whichever one is greater	
	Differential probes	V_{pos}-V_{neg} is ≥ 150 mV_{p-p}	
Maximum nondestructive input signal to probe		± 15V	
Minimum input pulse width (single channel) *(Typical)*		P6860, P6880, P6960, and P6980 probes	500 ps
		P6810 probes	750 ps

Table 61: TLA7Axx/TLA7NAx input parameters (with probes) (cont.)

Characteristic	Description	
Delay time from probe tip to input probe connector *(Typical)*	P6860, P6960, and P6980 probes	7.7 ns ± 60ps
	P6810 and P6880 probes	7.7 ns ± 80ps

Table 62: TLA7Axx analog output

Characteristic	Description
Number of outputs	Four analog outputs regardless of the module channel width. Any four of the module's channels can be mapped to the four analog outputs.
Attenuation	10X mode for normal operation 5X mode for small signals (-1.5 V to +2.5 V)
Bandwidth *(Typical)*	2 GHz
Accuracy (gain and offset) *(Typical)*	± (50 mV + 2% of signal amplitude)

Table 63: Channel width and depth

Characteristic		Description
Number of channels	TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4	128 data, 8 clock/qualifier
	TLA7AA3, TLA7AC3, TLA7NA3	96 data, 6 clock/qualifier
	TLA7AA2, TLA7AB2, TLA7AC2, TLA7NA2	64 data, 4 clock/qualifier
	TLA7AA1, TLA7NA1	32 data, 2 clock/qualifier
Acquisition memory depth	TLA7AAx, TLA7NAx series	32 M per channel, maximum
	TLA7ABx series	64 M per channel, maximum
	TLA7ACx series	128 M per channel, maximum

Table 64: Clocking

Characteristic	Description
Asynchronous sampling	
✓ Sampling period	500 ps to 50 ms in a 1-2-5 sequence. Storage control can be used to only store data when it has changed (transitional storage) 2 ns minimum for all channels 1 ns minimum for half channels (using 2:1 Demultiplex mode) 0.5 ns minimum for quarter channels (using 4:1 Demultiplex mode)
✓ Minimum recognizable word [1] (across all channels)	Channel-to-channel skew + sample uncertainty Example for a P6860 high-density probe and a 2 ns sample period: 400 ps + 2 ns = 2.4 ns

Table 64: Clocking (cont.)

Characteristic	Description	
synchronous sampling		
Master clock channels [2]	*Product*	*Clock channels*
	32+2 module	2
	64+4 module	4
	96+6 module	4
	128+8 module	4
Merged slave clock channels [2]	*Product*	*Clock channels*
(64+4 channel modules and 32+2 channel modules cannot be merged.)	96+6 module	4
	128+8 module	4
Qualifier channels	*Product*	*Qualifier channels*
Note: Qualifier channels are stored.	32+2 module	0
	64+4 module	0
	96+6 module	2
	128+8 module	4
Single channel setup and hold window size *(Typical)*	500 ps	
✓ Single module setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 100 ps	
	Maximum setup time = User interface setup time + 75 ps	
	Maximum hold time = User interface hold time + 50 ps	
	Example using a P6800 series probe and user interface setup and hold of 625/0 typical:	
	Maximum window size = 400 ps + 250 ps + 100 ps = 750 ps	
	Maximum setup time = 625 ps + 75 ps = 700 ps	
	Maximum hold time = 0.0 ps + 50 ps = 50 ps	
Single module setup and hold window size (data and qualifiers) *(Typical)*	Typical window size = Typical channel-to-channel skew + (2 x sample uncertainty) + 75 ps	
	Example using P6860 probe: 300 ps + 250 ps + 75 ps = 625 ps	
Setup and hold window range	For each channel, the setup and hold window can be moved from +8.0 ns (T_s typical) to -8.0 ns (T_s typical) in 0.125 ns steps (setup time).	
	The setup and hold window can be shifted toward the setup region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same setup and hold window. Setup times are specified as typical figures. Hold time follows the setup time by the setup and hold window size.	

Table 64: Clocking (cont.)

Characteristic	Description	
✓ Maximum synchronous clock rate TLA7Axx series	450 MHz in full-speed mode (2.2 ns minimum between active clock edges) 235 MHz in half-speed mode (4.25 ns minimum between active clock edges) 120 MHz in quarter-speed mode (8.3 ns minimum between active clock edges) 800 MHz on half channels [3] Software controls the selection between full-speed and half-speed modes.	
✓ Maximum synchronous clock rate TLA7NAx series	450 MHz in full-speed mode (2.2 ns minimum between active clock edges) 235 MHz in full-speed mode (4.25 ns minimum between active clock edges) 120 MHz in quarter-speed mode (8.3 ns minimum between active clock edges) Software controls the selection between full-speed and half-speed modes.	
Demultiplex clocking		
Demultiplex channels (2:1) TLA7AA3, TLA7AA4, TLA7AB4, TLA7AC3, TLA7AC4, TLA7NA3, TLA7NA4 modules	Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows:	
	A3(7:0) to/from	D3(7:0)
	A2(7:0) to/from	D2(7:0)
	A1(7:0) to/from	D1(7:0)
	A0(7:0) to/from	D0(7:0)
	E3(7:0) to/from	E1(7:0) TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4 modules only
	E2(7:0) to/from	E0(7:0) TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4 modules only
	CK3 to/from	Q2 TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4 modules only
	CK2 to/from	Q3 TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4 modules only
	CK1 to/from	Q0
	CK0 to/from	Q1
TLA7AA1, TLA7AA2, TLA7AB2, TLA7AC2, TLA7NA1, TLA7NA2 modules	Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows:	
	A3(7:0) to/from	C3(7:0)
	A2(7:0) to/from	C2(7:0)
	A1(7:0) to/from	D1(7:0) TLA7AA2, TLA7AB2, TLA7AC2, TLA7NA2 modules only
	A0(7:0) to/from	D0(7:0) TLA7AA2, TLA7AB2, TLA7AC2, TLA7NA2 modules only

Table 64: Clocking (cont.)

Demultiplex clocking		
Demultiplex channels (4:1) TLA7AA3, TLA7AA4, TLA7AB4, TLA7AC3, TLA7AC4, TLA7NA3, TLA7NA4 modules	Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others.	
	E3(7:0) to	E2(7:0), E1(7:0), E0(7:0) TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4 modules only
	A3(7:0) to	A2(7:0), D3(7:0), D2(7:0)
	A1(7:0) to	A0(7:0), D1(7:0), D0(7:0)
	C3(7:0) to	C2(7:0), C1(7:0), C0(7:0)
	CK3 to	CK2, Q3, Q2 TLA7AA4, TLA7AB4, TLA7AC4, TLA7NA4 modules only
	CK1 to	CK0, Q1, Q0
TLA7AA1, TLA7AA2, TLA7AB2, TLA7AC2, TLA7NA2, TLA7NA1 modules	Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others.	
	A1(7:0) to	A0(7:0), D1(7:0), D0(7:0) TLA7AA2, TLA7AB2, TLA7AC2 TLA7NA2 modules only
	C3(7:0) to	C2(7:0), A3(7:0), A2(7:0)
Time between Demultiplex clock edges *(Typical)*	Same limitations as normal synchronous acquisition	
Source synchronous sampling (TLA7Axx)		
Clocks per module	Four	
Clocks with merged modules	When merged, the slave modules have two clocks available from the master module. Including the local clocks, the total is six clocks.	
Clock groups	Four for a single module and for a merged system	
Size of clock group valid FIFO	Four stages when operated at 235 MHz or below (three stages when operated above 235 MHz); this allows four (source synchronous or other) clocks to occur before the clock that completes the Clock Group Valid signal for that group.	
Source synchronous clock alignment window	Channel-to-channel skew only	

Table 64: Clocking (cont.)

Demultiplex clocking	
Source synchronous clock reset	The Clock Group Valid FIFO can be reset in one of the two ways: **1.** By the overflow of a presettable (0-255) 8-bit counter that counts one of the following clocks: 2ns Clock or the master heartbeat clock (synchronous or asynchronous). An active edge places the reset count to its preset value. An active clock edge will clear the Clock Group Valid reset before the clock gets to the FIFO so that no data is lost. **2.** By enabling an external reset. In this mode, one of the clock channels must be traded on the master module to act as a level-sensitive reset input. Any one of the clocks can be selected. A polarity selection is available. This mode affects all Clock Group Complete circuits. Neither one of the above modes can be intermixed; one or the other must be selected.
Clocking state machine	
Pipeline delays	Channel groups can be programmed with a pipeline delay of 0 through 7 active clock changes.

1 Specification only applies with asynchronous clocking. With synchronous sampling, the setup and hold window size applies.

2 Any clock channel can be enabled. For enabled clock channels, either the rising, falling, or both edges can be selected as active clock edges; clock channels are stored.

3 This is a special mode and has some limitations such as the clocking state machine and trigger state machine only running at 500 MHz.

Table 65: TLA7Axx/TLA7NAx module trigger system

Characteristic	Description	
Trigger resources		
Word recognizers and range recognizers	16, word recognizers can be combined to form full width, double bounded range recognizers. The following selections are available:	
	16 word recognizers	0 range recognizers
	13 word recognizers	1 range recognizer
	10 word recognizers	2 range recognizers
	7 word recognizers	3 range recognizers
	4 word recognizers	4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across the modules. The master module contains the most-significant groups.	
Glitch detector (normal asynchronous clock mode)	Channel groups can be enabled to detect glitches. Glitches are subject to pulse width variations of up to ± 125ps	
Minimum detectable glitch pulse width *(Typical)*	Minimum input pulse width (single channel)	
	P6860, P6960 high density probe:	500 ps
	P6880, P6980 differential probe:	500 ps
	P6810 general purpose probe:	750 ps
Setup and hold violation detector (normal synchronous clock mode)	Any channel can be enabled to detect a setup or hold violation. The range is from 8.0 ns before the clock edge to 8.0 ns after the clock edge in 0.125 ns steps. The channel setup and hold violation size can be individually programmed. The range can be shifted towards the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same as the setup and hold window. Any setup value is subject to variation of up to the channel skew specification. Any hold value is subject to variation of up to the channel skew specification.	
Transition detector	16 transition detectors. Any channel group can be enabled or disabled to detect a rising transition, a falling transition, or both rising and falling transitions between the current valid data sample and the previous valid data sample.	
Counter/timers	2 counter/timers, 51 bits wide, can be clocked up to 500 MHz Maximum count is 2^50-1 (excluding sign bit) Maximum time is 4.5 X 10^6 seconds or 52 days Counters can be used as Settable, resettable, and testable flags. Counters can be reset, do nothing, increased, or decreased. Timers can be reset, started, stopped, or not changed. Counters and timers have zero reset latency and one clock terminal count latency.	
Signal In 1	A backplane input signal.	

Table 65: TLA7Axx/TLA7NAx module trigger system (cont.)

Characteristic	Description
Signal In 2	A backplane input signal.
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered.
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-for-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger states	16
✓ Trigger state sequence rate	Same rate as valid data samples received. 500 MHz maximum.
Trigger machine actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Programmable to any data sample (2 ns boundaries)
MagniVu trigger	Main acquisition machine controls the triggering of the MagniVu memory
MagniVu trigger position	Programmable within 2 ns boundaries and separate from the main acquisition memory trigger position
Increment/decrement counter	Counter/timers used as counters can be increased or decreased.
Start/stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer used as a timer is reset, the timer continues in the started or stopped state that it was prior to the reset.
Reloadable word recognizer (snapshot)	Loads the current acquired data sample into the reference value of the word recognizer via a trigger machine action. All data channels are loaded into their respective word recognizer reference register on a one-to-one manner.
Reloadable word recognizer latency	378 ns
Signal Out	A signal sent to the backplane to be used by other modules
Trigger Out	A signal sent to the backplane to trigger other modules
Storage control	
Storage	Storage is allowed only if a specific condition is met. The condition can use any of the trigger resources except for counter/timers. Storage commands defined in the current trigger state will override the global storage control. Storage can be used to start the acquisition with storage initially turned on (default setting) or off.
By event	Storage can be turned on or off; only the current sample can be stored. Event storage control overrides any global storage commands.
Block storage (store stretch)	When enabled, 31 samples are stored before and after the valid sample. This allows the storage of a group of samples around a valid data sample when storage control is being used. This only has meaning when storage control is used. Block storage is disallowed when glitch storage or setup and hold violation storage is enabled.

Table 65: TLA7Axx/TLA7NAx module trigger system (cont.)

Characteristic	Description
Glitch violation storage	Glitch violation information can be stored to acquisition memory with each data sample when asynchronous sampling is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The fastest asynchronous clock rate is reduced to 4 ns.
Setup and hold violation storage	Setup and hold violation information can be stored to acquisition memory with each data sample when synchronous sampling is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The maximum synchronous clock rate in this mode is 235 MHz.

Table 66: MagniVu acquisition

Characteristic	Description
MagniVu sampling period	Data is asynchronously sampled and stored every 125 ps in a separate MagniVu (high-resolution) memory. The storage speed can be changed by software to 250 ps, 500 ps, or 1000 ps with no loss in memory depth so that the high resolution memory covers more time at a lower resolution.
MagniVu memory depth	Approximately 16 K per channel. The MagniVu memory is separate from the main acquisition memory.

Table 67: Merged modules

Characteristic	Description
Number of merged modules	2, 3, 4, or 5 adjacent modules can be merged. Only 102-channel modules or 136-channel modules can be merged. Merged modules can have unequal channel widths and channel depths.
Number of channels after merging	The sum of all channels available on each of the merged modules including clocks and qualifiers. No channels are lost when modules are merged.
Merged system acquisition depth	Channel depth is equal to that of the shallowest module.
Number of clock and qualifier channels after merging	The qualifier channels on the slave modules can only be used as data channels. They cannot influence the actual clocking function of the logic analyzer (for example, log strobe generation). The clock channels on the slave TLA7Axx modules can capture data on those modules for source-synchronous applications. Each slave module contributes four additional clock channels to the merged set. All clock and qualifier channels are stored to acquisition memory.
Merged system trigger resources	The same as a single module except for word recognizer width, setup and hold violation detector width, glitch detector width, and transition detector width has increased to equal that of the merged channel width. Range recognizers will increase to the merged channel width up to three modules; range recognition is not supported on the two outside slave modules.
Merged range significance	Most significant Master, Slave 1, Slave 2

Table 68: Data placement

Characteristic	Description
Timestamp counter resolution and duration	125 ps resolution 3.25 days duration

Table 69: NVRAM

Characteristic	Description
Nonvolatile memory retention time (*Typical*)	The battery life is integral to the NVRAM; battery life is > 10 years.

Table 70: Mechanical

Characteristic		Description
Material		Chassis parts are constructed of aluminum alloy. The front panel is constructed of plastic laminated to steel front panel. Circuit boards are constructed of glass laminate.
Weight	136-channel module	5 lb 6 oz. (2.438 kg)
	102-channel module	5 lb 4 oz. (2.381 kg)
	68-channel module	5 lb 0.5 oz. (2.282 kg)
	34-channel module	4 lb 15.5 oz. (2.254 kg)
Shipping weight		7 lb 12 oz. (3.515 kg) for 136-channel module when packaged for domestic shipment
Overall dimensions	Height	10.32 in (262 mm)
	Width	2.39 in (61 mm) with merge connector recessed, 0.41 in (10.41 mm) with merge connector extended
	Length	14.7 in (373 mm)
Mainframe interlock		1.4 ECL keying is implemented

TLA7Lx/Mx/Nx/Px/Qx Module Specifications

The following tables list the specifications of the TLALx/Mx/Nx/Px/Qx logic analyzer modules.

Table 71: LA module channel width and depth

Characteristic	Description	
Number of channels	*Product*	*Channels*
	TLA7N1, TLA7L1, TLA7M1	32 data and 2 clock
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	64 data and 4 clock
	TLA7N3, TLA7L3, TLA7M3	96 data, 4 clock, and 2 qualifier
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	*Product*	*Memory depth*
	TLA7L1, TLA7L2, TLA7L3, TLA7L4	32 K or 128 K samples [1]
	TLA7M1, TLA7M2, TLA7M3, TLA7M4	512 K samples
	TLA7N1, TLA7N2, TLA7N3, TLA7N4	64 K or 256 K or 1 M or 4 M samples [1]
	TLA7P2, TLA7P4	16 M samples
	TLA7Q2, TLAQP4	64 M samples

[1] PowerFlex options

Table 72: LA module clocking

Characteristic	Description	
Asynchronous sampling		
Sampling period [1]	2 ns to 50 ms in a 1-2-5 sequence	
Minimum recognizable word [2] (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417 or a P6418 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
synchronous sampling		
Number of clock channels [3]	*Product*	*Clock channels*
	TLA7N1, TLA7L1, TLA7M1	2
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	4
	TLA7N3, TLA7L3, TLA7M3	4
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	4
Number of qualifier channels	*Product*	*Qualifier channels*
	TLA7N1, TLA7L1, TLA7M1	0
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	0
	TLA7N3, TLA7L3, TLA7M3	2
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	4

Table 72: LA module clocking (cont.)

Characteristic	Description
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.8 ns Maximum hold time = User interface hold time + 0.2 ns Maximum setup time for slave module of merged pair = User Interface setup time + 0.8 ns Maximum hold time for slave module of merged pair = User Interface hold time + 0.7 ns Examples: for a P6417, P6418, or P6434 probe and user interface setup and hold of 2.0/0.0 typical: Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns
Setup and hold window size (data and qualifiers) *(Typical)*	Channel-to-channel skew (*typical*) + (2 x sample uncertainty) Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns
Setup and hold window range	For the TLA7Nx/Px/Qx logic analyzer modules, each channel of the setup and hold window can be moved from +8.5 ns (Ts) to -7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size. For the TLA7Lx and TLAMx logic analyzer modules, the user interface restricts the setup and hold window range to groups rather than individual channels.
✓ Maximum synchronous clock rate [4]	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz in half speed mode (10 ns minimum between active clock edges)
Demux clocking	
Demux Channels TLA7N3, TLA7N4, TLA7P4, TLA7Q4, TLA7L3, TLA7L4, TLA7M3, TLA7M4	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)
TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA7L1, TLA7L2, TLA7M1, TLA7M2	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2 only A0(7:0) to D0(7:0) TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2 only
Time between DeMux clock edges [4] *(Typical)*	5 ns minimum between DeMux clock edges in full-speed mode 10 ns minimum between DeMux clock edges in half-speed mode
Time between DeMux store clock edges [4] *(Typical)*	10 ns minimum between DeMux master clock edges in full-speed mode 20 ns minimum between DeMux master clock edges in half-speed mode
Data Rate *(Typical)* TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA7N3, TLA7N4, TLA7P4, TLA7Q4,	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.

Table 72: LA module clocking (cont.)

Demux clocking	
Clocking state machine	
Pipeline delays	For the TLA7Nx/Px/Qx logic analyzer modules, each channel can be programmed with a pipeline delay of 0 through 3 active clock edges. For the TLA7Lx and TLAMx logic analyzer modules, the user interface restricts the programming to groups rather than individual channels.

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous sampling only. Setup and hold window specification applies to synchronous sampling only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, the rising edge, falling edge, or both edges can be selected as the active clock edges. The clock channels are stored.

4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.

Table 73: LA module trigger system

Characteristic	Description
Triggering Resources	
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: 16 word recognizers — 0 range recognizers 13 word recognizers — 1 range recognizer 10 word recognizers — 2 range recognizers 7 word recognizers — 3 range recognizers 4 word recognizers — 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across all the modules; the master module contains the most-significant groups. The master module is to the left (lower-numbered slot) of a merged pair. The master module is in the center when three modules are merged. Slave module 1 is located to the right of the master module, and slave module 2 is located to the left of the master module.
Glitch detector [1 2]	Each channel group can be enabled to detect a glitch
Minimum detectable glitch pulse width *(Typical)*	2.0 ns (single channel with a P6417, P6418, or P6434 probe)
Setup and hold violation detector [1 3]	Each channel can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. For the TLA7Lx and TLAMx logic analyzer modules, the user interface restricts the setup and hold violation detector to groups rather than individual channels. The setup and hold violation of each window can be individually programmed.
Transition detector [1 4]	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample.

Table 73: LA module trigger system (cont.)

Characteristic	Description
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51}. Maximum time is 9.007 X 10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
Signal In 1	A backplane input signal
Signal In 2	A backplane input signal
Trigger In	A backplane input signal that causes the main acquisition and the **MagniVu** acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
⩘ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
Increment counter	Either of the two counter/timers used as counters can be increased.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues in the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other modules
Trigger out	A trigger out signal sent to the backplane to trigger other modules
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Block storage is disallowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous sampling is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous sampling rate is reduced to 10 ns.

1 Each use of a glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.

2 Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.

3 For TLA7N1, TLA7N2, TLA7N3, TLA7N4, TLA7P2, TLA7P4, TLA7Q2, and TLA7Q4 Logic Analyzer modules, any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns. For TLA7L1, TLA7L2, TLA7L3, TLA7L4, TLA7M1, TLA7M2, TLA7M3, and TLA7M4 Logic Analyzer modules, any setup value is subject to variation of up to 1.6 ns; any hold value is subject to variation of up to 1.4 ns.

4 This mode can be used to create transitional storage selections where all channels are enabled.

Table 74: LA module MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory.

Table 75: LA module data handling

Characteristic	Description
Nonvolatile memory retention time *(Typical)*	Battery is integral to the NVRAM. Battery life is > 10 years.

Table 76: LA module input parameters with probes

Characteristic		Description	
✓ Threshold Accuracy		±100 mV	
Threshold range and step size		Settable from +5 V to -2 V in 50 mV steps	
Threshold channel selection		16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).	
✓ Channel-to-channel skew		≤ 1.6 ns maximum (When merged, add 0.5 ns for the slave module.)	
Channel-to-channel skew *(Typical)*		≤ 1.0 ns typical (When merged, add 0.3 ns for the slave module.)	
Sample uncertainty		*Asynchronous*	*Synchronous*
		Sample period	500 ps
Probe input resistance *(Typical)*		20 kΩ	
Probe input capacitance: P6417, P6434 *(Typical)*		2 pF	
Probe input capacitance: P6418 *(Typical)*		1.4 pF data channels 2 pF CLK/Qual channels	
Minimum slew rate *(Typical)*		0.2 V/ns	
Maximum operating signal		6.5 V_{p-p} -3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum	
Probe overdrive	P6417, P6418	±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater	
	P6434	±300 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±4 V maximum beyond threshold	
Maximum nondestructive input signal to probe		±15 V	

Table 76: LA module input parameters with probes (cont.)

Characteristic	Description
Minimum input pulse width signal (single channel) *(Typical)*	2 ns
Delay time from probe tip to input probe connector *(Typical)*	7.33 ns

Table 77: LA module mechanical

Characteristic		Description
Slot width		Requires 2 mainframe slots
Weight *(Typical)*		5 lbs 10 oz. (2.55 kg) for TLA7N4 and TLA7P4
		8 lbs (3.63 kg) for TLA7N4 and TLA7P4 packaged for domestic shipping
Overall dimensions	Height	262 mm (10.32 in)
	Width	61 mm (2.39 in)
	Depth	373 mm (14.7 in)
Probe cables	P6417 length	1.8 m (6 ft)
	P6418 length	1.93 m (6 ft 4 in)
	P6434 length	1.6 m (5 ft 2 in)
Mainframe interlock		1.4 ECL keying is implemented

TLA7PG2 Module Specifications

The following tables list the specifications for the pattern generator module. For information on the individual pattern generator probes, refer to *TLA7PG2 Pattern Generator Probe Instruction Manual*.

Table 78: PG module electrical specification, operational mode

Characteristic	Description
Operational mode	
Normal	Pattern data output is synchronized by the internal/external clock input
Step	Pattern data output is synchronized by the software command
Output pattern	
✓ Maximum Data Output Rate Output level: 5 V Load: 1 MΩ + 1 pF Series termination resistor: 75 W	134 MB/s in Full Channel Mode 268 MB/s in Half Channel Mode
Maximum Clock Output Frequency Output level: 5 V Load: 1 MΩ + 1 pF Series termination resistor: 75 Ω	134 MHz in Full Channel Mode 134 MHz in Half Channel Mode
Maximum Operating Frequency	The maximum operating frequency of the module is a function of the output level, output pattern and the load condition, including the series termination resistor in the probe. Operating conditions exceeding this frequency may result in damage to the probe.
Pattern length	40 to 262,140 (2^{18} - 4) in Full Channel Mode (standard) 80 to 524,280 (2^{19} - 8) in Half Channel Mode (standard) 40 to 1,048,572 (2^{20} - 4) in Full Channel Mode (option 1M or PowerFlex upgrade) 80 to 2,097,144 (2^{21} - 8) in Half Channel Mode (option1M or PowerFlex upgrade)

Table 78: PG module electrical specification, operational mode (cont.)

Characteristic	Description	
Number of channels	64 channels in Full Channel Mode	
	32 channels in Half Channel Mode	
	The pattern memory for the following data channel will be shared with strobe control/internal inhibit control	
	Probe D data output channel	*Control*
	D0:0	STRB0
	D0:1	STRB1
	D0:2	STRB2
	D0:3	STRB3
	D0:4	Inhibit probe A
	D0:5	Inhibit probe B
	D0:6	Inhibit probe C
	D0:7	Inhibit probe D
Sequences	Maximum 4,000	
Number of blocks	Maximum 4,000	
Number of subsequences	Maximum 50	
Subsequences	Maximum 256 steps	
Repeat count	1 to 65,536 or infinite	

Table 79: PG module clocking

Characteristic		Description
Internal clock		
Clock Period		2.0000000 s to 7.462865 ns in Full Channel Mode
		1.0000000 s to 3.7313432 ns in Half Channel Mode
Period Resolution		8 digits
Frequency Accuracy		± 100 ppm
External clock input		
Clock Rate		DC to 134 MHz in Full Channel Mode
		DC to 267 MHz in Half Channel Mode
Polarity		Normal or Invert
Threshold	Range	-2.56 V to +2.54 V
	Resolution	20 mV
Input Impedance		1 kΩ terminated to GND
Sensitivity		500 mV_{p-p}

Table 80: PG module event processing

Characteristic		Description
Event Action		Advance, Jump and Inhibit
Number of Event Inputs		8 External Event Inputs (2 per each probe)
Number of Event Definitions		8 (A maximum of 256 event input patterns can be OR'd to define an event)
Event Mode	for Advance	Edge or Level
	for Jump	Edge or Level
Event Filter		None or 50 ns

Table 81: PG module inter-module interactions

Characteristic	Description
Signal Input	Input from backplane Selectable from Signal 1, 2, 3, and 4 Used to define the Event
Signal Output	Output to backplane Selectable from Signal 1, 2, 3, and 4 Specified as High or Low in each Sequence line

Table 82: PG module merged PG modules

Characteristic	Description
Number of modules that can be merged together	Five
External Event Input for merged module	For Jump and Advance, only the External Event Input of the leftmost module is used. For Inhibit, each module uses its own External Event Input as a source

Table 83: PG module mechanical

Characteristic		Description
Slot width		Requires two mainframe slots
Weight*(Typical)*		2.5 kg (5 lbs. 4 oz.)
Overall dimensions (excluding connectors)	Height	10.32 in (262 mm)
	Width	2.39 in (61 mm)
	Depth	14.7 in (373 mm)
Mainframe interlock		1.4 ECI keying is implemented

DSO Module Specifications

The following tables list the specifications for the DSO Module.

Table 84: DSO module signal acquisition system

Characteristic	Description		
✓ Accuracy, DC gain	±1.5% for full scale ranges from 20 mV to 100 V ±2.0% for full scale ranges <19.9 mV		
✓ Accuracy, internal offset [1]	*Full scale range setting*	*Offset accuracy*	
	10 mV - 1 V	±[(0.2% x offset) + 1.5 mV + (6% x full scale range)]	
	1.01 V - 10 V	±[(0.25% x offset) + 15 mV + (6% x full scale range)]	
	10.1 V - 100 V	±[(0.25% x offset) + 150 mV + (6% x full scale range)]	
✓ Analog bandwidth, DC-50 Ω coupled	*Full scale range setting*	*Bandwidth* [2]	
	10.1 V - 100 V	DC - 500 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	100 mV - 10 V	DC - 1 GHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	50 mV - 99.5 mV	DC - 750 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	20 mV - 49.8 mV	DC - 600 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	10 mV - 19.9 mV	DC - 500 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
Bandwidth, analog, selections	20 MHz, 250 MHz, and FULL on each channel		
Calculated rise time *(Typical)* [3] Typical full-bandwidth rise times are shown in the chart to the right	*Full scale range setting*	*TLA7E1 and TLA7E2*	*TLA7D1 and TLA7D2*
	10.1 V - 100 V	900 ps	900 ps
	100 mV - 10 V	450 ps	900 ps
	50 mV - 99.5 mV	600 ps	900 ps
	20 mV - 49.8 mV	750 ps	900 ps
	10 mV - 19.9 mV	900 ps	900 ps
Crosstalk (channel isolation)	≥300:1 at 100 MHz and ≥100:1 at the rated bandwidth for the channel's sensitivity (Full Scale Range) setting, for any two channels having equal sensitivity settings		
Digitized bits	8		

Table 84: DSO module signal acquisition system (cont.)

Characteristic	Description		
Effective bits, real time sampling *(Typical)*	*Input frequency*	*TLA7E1 and TLA7E2 5 GS/s (each channel)*	*TLA7D1 and TLA7D2 2.5 GS/s (each channel)*
	10.2 MHz	6.2 bits	6.2 bits
	98 MHz	6.1 bits	6.1 bits
	245 MHz	6.0 bits	6.0 bits
	490 MHz	5.7 bits	5.7 bits
	990 MHz	5.2 bits	N/A
Frequency limit, upper, 20 MHz bandwidth limited *(Typical)*	20 MHz		
Frequency limit, upper, 250 MHz bandwidth limited *(Typical)*	250 MHz		
Input channels	*Product*	*Channels*	
	TLA7E2	4	
	TLA7D2	4	
	TLA7E1	2	
	TLA7D1	2	
Input coupling	DC, AC, or GND [4]		
Input impedance, DC-1 MΩ coupled	1 MΩ ±0.5% in parallel with 10 pF ±3 pF		
Input impedance selections	1 MΩ or 50 Ω		
Input resistance, DC-50 Ω coupled	50 Ω ±1%		
Input VSWR, DC-50 W coupled	≤1.3:1 from DC - 500 MHz, ≤1.5:1 from 500 MHz - 1 GHz		
Input voltage, maximum, DC-1 MΩ , AC-1 MΩ, or GND coupled	300 V_{RMS} but no greater than ±420 V peak, Installation category II, derated at 20 dB/decade above 1 MHz		
Input voltage, maximum, DC-50 Ω or AC-50 Ω Coupled	5 V_{RMS}, with peaks ≤ ±25 V		
Lower frequency limit, AC coupled *(Typical)*	≤10 Hz when AC-1 MΩ Coupled; ≤200 kHz when AC-50 Ω Coupled [5]		
✓ Random noise	*Bandwidth selection*	*RMS noise*	
	Full	≤(350 µV + 0.5% of the full scale Setting)	
	250 MHz	≤(165 µV + 0.5% of the full scale Setting)	
	20 MHz	≤(75 µV + 0.5% of the full scale Setting)	
Range, internal offset	*Full scale range setting*	Offset range	
	10 mV - 1 V	±1 V	
	1.01 V - 10 V	±10 V	
	10.1 V - 100 V	±100 V	
Range, sensitivity (full scale range), all channels	10 mV to 100 V [6]		

Table 84: DSO module signal acquisition system (cont.)

Characteristic	Description				
Step response settling errors *(Typical)* [7] [8]	*Full scale range setting*	*± Step response*	*Maximum setting error (%) at*		
			20 ns	*100 ns*	*20 ms*
	10 mV - 1 V	≤2 V	0.5%	0.2%	0.1%
	1.01 V - 10 V	≤20 V	1.0%	0.5%	0.2%
	10.1 V - 100 V	≤200 V	1.0%	0.5%	0.2%

1 Net offset is the nominal voltage level at the digitizing oscilloscope input that corresponds to the center of the A/D Converter dynamic range. Offset accuracy is the accuracy of this voltage level.

2 The limits given are for the ambient temperature range of 0 °C to +30 °C. Reduce the upper bandwidth frequencies by 5 MHz for each °C above +30 °C. The bandwidth must be set to FULL.

3 Rise time (rounded to the nearest 50 ps) is calculated from the bandwidth when Full Bandwidth is selected. It is defined by the following formula:
Rise Time (ns) = 450 BW (MHz)

4 GND input coupling disconnects the input connector from the attenuator and connects a ground reference to the input of the attenuator.

5 The AC Coupled Lower Frequency Limits are reduced by a factor of 10 when 10X passive probes are used.

6 The sensitivity ranges from 10 mV to 100 V full scale in a 1-2-5 sequence of coarse settings. Between coarse settings, you can adjust the sensitivity with a resolution equal to 1% of the more sensitive coarse setting. For example, between the 500 mV and 1 V ranges, the sensitivity can be set with 5 mV resolution.

7 The Full Bandwidth settling errors are typically less than the percentages from the table.

8 The maximum absolute difference between the value at the end of a specified time interval after the mid-level crossing of the step, and the value one second after the mid-level crossing of the step, expressed as a percentage of the step amplitude. See IEEE std. 1057, Section 4.8.1, Settling Time Parameters.

Table 85: DSO module timebase system

Characteristic	Description	
Range, Extended Real-time Sampling Rate	5 S/s to 10 MS/s in a 1-2.5-5 sequence	
Range, Real-time Sampling Rate	*Products*	*Limits*
	TLA7E1 and TLA7E2	25 MS/s to 5 GS/s on all channels simultaneously in a 1-2.5-5 sequence
	TLA7D1 and TLA7D2	25 MS/s to 2.5 GS/s on all channels simultaneously in a 1-2.5-5 sequence
Record Length	512, 1024, 2048, 4096, 8192, and 15000	
✓ Long Term Sample Rate	±100 ppm over any ≥ 1 ms interval	

Table 86: DSO module trigger system

Characteristic	Description	
✓ Accuracy (Time) for Pulse Glitch or Pulse Width Triggering	*Time Range*	Accuracy
	2 ns to 500 ns	± (20% of setting + 0.5 ns)
	520 ns to 1 s	± (104.5 ns + 0.01% of setting)
✓ Accuracy (DC) for Edge Trigger Level, DC Coupled	±((2% × | Setting) |) + 0.03 of Full Scale Range + Offset Accuracy) for signals having rise and fall times ≥20 ns	
Range (Time) for Pulse Glitch and Pulse Width Triggering	2 ns to 1 s	
Range, Trigger Level	*Source*	*Range*
	Any Channel	±100% of full scale range

Table 86: DSO module trigger system (cont.)

Characteristic	Description		
Range, Trigger Point Position	Minimum: 0% Maximum: 100%		
Resolution, Trigger Level	0.2% of full scale for any Channel source		
Resolution, Trigger Position	One Sample Interval at any Sample Rate		
Sensitivities, Pulse-Type Runt Trigger *(Typical)*	10% of full scale, from DC to 500 MHz, for vertical settings >100 mV full scale and ≤10 V full scale at the BNC input		
Sensitivities, Pulse-Type Trigger Width and Glitch *(Typical)*	10% of full scale for vertical settings >100 mV full scale and ≤10 V full scale at the BNC input		
✓ Sensitivity, Edge-Type Trigger, DC Coupled	The minimum signal levels required for stable edge triggering of an acquisition when the trigger source is DC-coupled		
	Products	*Trigger Source*	*Sensitivity*
	TLA7E1 and TLA7E2	Any Channel	2.5% of Full Scale Range from DC to 50 MHz increasing to 10% of Full Scale Range at 1 GHz
	TLA7D1 and TLA7D2	Any Channel	2.5% of Full Scale Range from DC to 50 MHz increasing to 10% of Full Scale Range at 500 MHz
Sensitivity, Edge-Type Trigger, Not DC Coupled *(Typical)*	*Trigger Coupling*	*Typical Signal Level for Stable Triggering*	
	AC	Same as the DC-coupled limits for frequencies above 60 Hz; attenuates signals below 60 Hz	
	High Frequency Reject	One and one-half times the DC-coupled limits from DC to 30 kHz; attenuates signals above 30 kHz	
	Low Frequency Reject	One and one-half times the DC-coupled limits for frequencies above 80 kHz; attenuates signals below 80 kHz	
	Noise Reject	Three times the DC-coupled limits	
Time, Minimum Pulse or Rearm, and Minimum Transition Time, for Pulse-Type Triggering *(Typical)*	For vertical settings >100 mV and £10 V at the BNC input		
	Pulse Class	*Minimum Pulse Width*	Minimum Rearm Width
	Glitch	1 ns	2 ns + 5% of Glitch Width Setting
	Width	1 ns	2 ns + 5% of Width Upper Limit Setting
Trigger Position Error, Edge Triggering *(Typical)*	*Acquisition Mode*	*Trigger Position Error* [1]	
	Sample	±(1 Sample Interval + 1 ns)	

[1] The trigger position errors are typically less than the values given here. These values are for triggering signals having a slew rate at the trigger point of ³5% of full scale/ns.

Table 87: DSO module front-panel connectors

Characteristic	Description
⌿ Probe Compensator, Output Voltage The Probe Compensator output voltage in peak-to-peak Volts	0.5 V (base-top) ± 1% into a ≥ 50 Ω load

Table 88: DSO module mechanical

Characteristic	Description	
Slot width	Requires 2 mainframe slots	
Weight *(Typical)*	*Products*	*Weight*
	TLA7D1 and TLA7E1	2.44 kg (5.38 lbs)
	TLA7D2 and TLA7E2	2.55 kg (5.63 lbs)
Shipping Weight *(Typical)*	*Products*	*Weight*
	TLA7D1 and TLA7E1	6.35 kg (14 lbs)
	TLA7D2 and TLA7E2	7.71 kg (17 lbs)
Overall Dimensions	Height: 262.05 mm (10.32 in)	
	Width: 60.66 mm (2.39 in)	
	Depth: 373.38 mm (14.70 in)	

External Oscilloscope (iView) Characteristics

The following table lists the characteristics for iView (Integrated View) and for the Tektronix logic analyzer mainframe when connected to an external oscilloscope. For detailed information on the individual specifications of the external oscilloscope, refer to the documentation that accompanies the oscilloscope.

Table 89: External oscilloscope (Integrated View or iView) characteristics

Characteristic	Description
Supported Tektronix logic analyzer instruments	TLA5000 and TLA5000B series TLA715, TLA721 TLA7012, TLA7016
TLA application software version	V5.6 or greater
Minimum recommended TLA controller RAM [1]	512 MB
Supported external oscilloscopes as of May, 2008 *(For the latest list of supported external oscilloscopes, visit our Web site at www.tektronix.com/la.)*	TDS1000 and TDS2000 Series [2] [3] TDS1000B and TDS2000B Series [3] [4] TDS3000, TDS3000B, and TDS3000C Series (TDS3GM or TDS3GV GPIB/RS-232 communication module required) DPO3000 Series [4] DPO4000 and MSO4000 Series [4] [5] TDS5000 and TDS5000B Series TDS6000, TDS6000B, and TDS6000C Series DPO7000 and DPO7000B Series DPO70000 and DSA70000 Series TDS7000 and TDS7000B Series CSA7000 and CSA7000B Series TDS654C, TDS684C, TDS694C TDS754C, TDS784C, TDS724D, TDS754D, TDS784D, TDS794D
Maximum number of external oscilloscopes	One per Tektronix logic analyzer mainframe
iView cable length [6]	6.56 ft (2 m)

Table 89: External oscilloscope (Integrated View or iView) characteristics (cont.)

Characteristic	Description	
Time correlation uncertainty[7] (*Typical at system trigger)*	3 ns	Logic analyzer triggers external oscilloscope (2 ns + logic analyzer sample period + external oscilloscope sample period)
	5 ns	External oscilloscope triggers logic analyzer (4 ns + logic analyzer sample period + external oscilloscope sample period)

1 If RAM is less than 256 MB, the record length of the external oscilloscope may be limited to 1 M.

2 A GPIB extender is needed to connect the iView cable to the oscilloscope. One end of a standard GPIB cable can be used.

3 If you encounter possible alignment problems with the logic analyzer and oscilloscope waveform edges, refer to Aligning Logic Analyzer and Oscilloscope Waveform Edges. (See page 77, *Aligning Logic Analyzer and Oscilloscope Waveform Edges*.)

4 A GPIB to USB adapter (TEK-USB-488) is required to connect the iView cable to the oscilloscope.

5 There is a known timing offset between triggers when a TLA logic analyzer is triggered by the oscilloscope. Tektronix is correcting this problem.

6 When used with a TLA7016 mainframe and an external PC (such as TLA7PC1), the instruments must be physically located close together so that the iView cable can span both instruments. Removing the sleeving from the iView cable assembly increases the spacing distance available between the external PC and the TLA7016 mainframe.

7 Includes sampling uncertainty, typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a typical number for the measurement.

Aligning Logic Analyzer and Oscilloscope Waveform Edges

The first time that you take an acquisition after changing the horizontal scale setting on TDS1000B, TDS2000B, TDS1000 or TDS2000 series oscilloscopes, the logic analyzer and oscilloscope waveform edges may not be aligned within the listed specification. You can realign the waveform positions in the waveform window that contains the oscilloscope data (Menu bar > Data > Time Alignment). Make sure that the external oscilloscope is the data source and then adjust the time offset to align the waveforms. Use the following approximate offsets for various horizontal scale settings. (See Table 90.)

Table 90: TDS1000B, TDS2000B, TDS1000, and TDS2000 Series oscilloscope waveform edge alignment

Horizontal scale	Time offset
100 ns	–5 ns
250 ns	–11 ns
500 ns	–18 ns
1 µs	–12 ns
2.5 µs	–50 ns
5 µs	–120 ns
10 µs	–250 ns
25 µs	–650 ns

Performance Verification Procedures

This chapter contains procedures for functional verification, certification, and performance verification procedures for the TLA7000 series logic analyzer mainframes. Refer to the individual service manuals for performance verification procedures for other Tektronix Logic Analyzer products. Generally, you should perform these procedures once per year or following repairs that affect certification.

Summary Verification

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on diagnostics, extended diagnostics, and manual check procedures. These procedures can be used for incoming inspection purposes.

Certification procedures certify the accuracy of an instrument and provide a traceability path to national standards. Certification data is recorded on calibration data reports provided with this manual. The calibration data reports are intended to be copied and used for calibration/certification procedures.

After completing the performance verification procedures or the certification procedures, you can fill out a calibration data report to keep on file with your instrument.

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Specifications* chapter of this manual.

Test Equipment

These procedures use external, traceable signal sources to directly test characteristics that are designated as checked ✓ in the *Specifications* chapter of this manual. Always warm up the equipment for 30 minutes before beginning the procedures.

Table 91: Test equipment

Item number and description	Minimum requirements	Example
1. Benchtop Mainframe	TLA7016 Benchtop Mainframe with a logic analyzer module installed and an external computer with TLA application software installed.	-
2. Portable Mainframe	TLA7012 Portable Mainframe with a logic analyzer module installed	-

Table 91: Test equipment (cont.)

Item number and description	Minimum requirements	Example
3. Frequency counter	Frequency accuracy: <0.0025% Frequency range: 1 kHz to 100 MHz	Hewlett Packard 5314A
4. Cable, precision 50 Ω coaxial	50 Ω , 36 in, male-to-male BNC connectors	Tektronix part number 012-0482-XX

Functional Verification

The following table lists functional verification procedures for the benchtop and portable mainframes. If necessary, refer to the *TLA7000 Series Logic Analyzer Installation Manual* for installation instructions.

Table 92: Functional verification procedures

Instrument	Procedure
Benchtop and portable mainframe	Power-on and fan operation
	Power-up diagnostics
	Extended diagnostics
	TLA Mainframe diagnostics
	CheckIt Utilities diagnostics

Power-on and Fan Operation

Complete the following steps to check the power-on and fan operation of the logic analyzer:

You will need a mainframe with an LA module installed in each mainframe.

1. Power on the instrument and observe that the On/Standby switch illuminates.
2. Check that the fans spin without undue noise.
3. If everything is properly connected and operational, you should see the modules in the System window of the logic analyzer application.
4. If there are no failures indicated in the System window, the power-on diagnostics pass when you power on the mainframe(s).

Extended Diagnostics

Do the following steps to run the extended diagnostics:

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

You will need a mainframe with an LA module installed in each mainframe.

Prerequisites	Warm-up time: 30 minutes

Perform the following tests to complete the functional verification procedure:

NOTE. *Installing a module in the mainframe provides a means of verifying connectivity and communication between the module and the mainframe. Try using a different module and repeat the tests to isolate the problem to the mainframe or to the module.*

1. If you have not already done so, power on the instrument and start the logic analyzer application if it did not start by itself.
2. Go to the System menu and select Calibration and Diagnostics.
3. Verify that all power-on diagnostics pass.
4. Click the Extended Diagnostics tab.
5. Select All Modules, All Tests, and then click the Run button on the property sheet.

   All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.
6. Scroll through the tests and verify that all tests pass.

TLA Mainframe Diagnostics

The TLA Mainframe Diagnostics are a comprehensive software test that checks the functionality of the mainframes. To run these diagnostics, do the following steps:

1. Quit the logic analyzer application.
2. Click the Windows Start button.
3. Select All Programs → Tektronix Logic Analyzer → TLA Mainframe Diagnostics.
4. Select your instrument from the Connection dialog box (in most cases this will be the **[Local]** selection).
5. Run the mainframe diagnostics.

CheckIt Utilities

CheckIt Utilities is a comprehensive software application used to check and verify the operation of the PC hardware in the portable mainframe. To run the software, you must have either a keyboard, mouse, or other pointing device.

NOTE. *To check the DVD drive, you must have a test CD installed before starting the CheckIt Utilities. The test CD needs to contain a file with a size between 5 MB and 15 MB.*

To run CheckIt Utilities, follow these instructions:

1. Quit the logic analyzer application.
2. Click the Windows Start button.
3. Select All Programs → CheckIt Utilities.
4. Run the tests. If necessary, refer to the CheckIt Utilities online help for information on running the software and the individual tests.

Certification

The system clock of the controller is checked for accuracy. The instrument is certifiable if this parameter meets specifications. Complete the performance verification procedures and record the certifiable parameters in a copy of the Calibration Data Report at the end of this chapter.

Performance Verification Procedures

This section contains procedures to verify that the TLA7012 Portable Mainframe and the TLA7016 Benchtop Mainframe perform as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question.

Tests Performed

Do the following tests to verify the performance of the TLA7012 Portable Mainframe and the TLA7016 Benchtop Mainframe. (See Table 93.) You will need test equipment to complete the performance verification procedures. (See Table 91.) If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Table 93: Performance verification procedures

Parameter	Procedure
System clock (CLK 10) [1]	10 MHz system clock test

[1] Certifiable parameter

Checking the 10 MHz System Clock (CLK10)

The following procedure checks the accuracy of the 10 MHz system clock:

Equipment required	Frequency counter (item 3) Precision BNC cable (item 4)
Prerequisites	Warm-up time: 30 minutes

1. Verify that all of the prerequisites above are met for the procedure.
2. Connect the frequency counter to the External Signal Out BNC connector on the instrument.
3. Go to the System window and select System Configuration from the System menu.
4. In the System Configuration dialog box, select 10 MHz Clock from the list of routable signals in the External Signal Out selection box and click OK.
5. Verify that the output frequency at the External Signal Out connector is 10 MHz ±1 kHz. Record the measurement on a copy of the calibration data report and disconnect the frequency counter.
6. In the System Configuration dialog box, reset the External Signal Out signal to None.

Calibration Data Report

Photocopy this table and use it to record the performance test results for your instrument.

TLA7012 and TLA7016 Test Record

Instrument model number:
Serial number:
Certificate number:
Verification performed by:
Verification date:

System Clock Test Data

Characteristic	Specification	Tolerance	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)		

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