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Tektronix Logic Analyzers

TLA7NAx Logic Analyzer Modules Data Sheet



The TLA Series logic analyzer modules offer the highest performance for today's demanding applications.

Features & Benefits

- 34/68/102/136 Channel Logic Analyzers with up to 128 Mb Record Length to Capture Long Periods of Time
- 500 ps (2 GHz)/32 Mb Timing Analysis to Track Down Elusive Timing Problems Faster
- 125 ps (8 GHz) MagniVu™ Acquisition simultaneous with Timing or State Acquisition to Find Difficult Problems Quickly
- Up to 450 MHz State Acquisition Analysis of Synchronous Digital Circuits
- Glitch and Setup/Hold Violation Triggering and Display Finds and Displays Elusive Hardware Problems
- Transitional Storage Extends the Signal Analysis Capture Time
- Connectorless Probing System With 0.5 pF Capacitive Loading Eliminates Need For Onboard Connectors, Minimizes Intrusion on Circuits and is Ideal for Differential Signal Applications
- Broad Processor and Bus Support

Applications

- Hardware Debug and Verification
- Processor/Bus Debug and Verification Including Source Synchronous Clocking
- Embedded Software Integration, Debug and Verification

Breakthrough Solutions for Real-time Digital Systems Analysis

The TLA7NAx Logic Analyzer Module speeds debug and verification of fast buses and complex embedded systems with an industry-leading combination of acquisition, triggering and analysis capabilities. Quickly debug fast buses like DDR memory and PCI-X, using long record length to capture intermittent events over a wide time window and MagniVu high-speed timing to simultaneously capture glitches as small as 125 ps. The TLA7NAx module's advanced triggering capabilities allow you to trigger on microprocessor operation failures, which speeds troubleshooting of embedded systems incorporating microprocessors such as the PowerQUICCIII. Additional tools like source code and protocol analysis and listing view make monitoring and debugging processor operation faster and easier.

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Characteristics

General

Number of Channels (all channels are acquired including clocks) – TLA7NA1: 34 channels (2 are clock channels).
TLA7NA2: 68 channels (4 are clock channels).
TLA7NA3: 102 channels (4 are clock and 2 are qualifier channels).
TLA7NA4: 136 channels (4 are clock and 4 are qualifier channels).
Channel Grouping: No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).

Module "Merging" – Up to five 102 channel or 136 channel modules can be "merged" to make up to a 680 channel module. Merged modules exhibit the same depth and state speed as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three module merge. Only one set of clock connections is required.

Time Stamp – 51 bits at 125 ps resolution (3.25 days duration).

Clocking/Acquisition Modes – Internal, internal 2X, internal 4X, external, external 450 (with option 45 only). 8 GHz MagniVu high-speed timing is available simultaneous with all modes.

Number of Mainframe Slots Required per TLA Series Module – 2.

Input Characteristics (with P68xx or P69xx probes)

Capacitive Loading – 0.5 pF (P69xx), <0.7 pF (P68xx) clock/data.

Input Voltage Range – Operating: -2.5 V to 5.0 V.
Nondestructive: ± 15 V.

Threshold Selection Range – From -2.0 V to +4.5 V in 5 mV increments. Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (-1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined.

Threshold Selection Channel Granularity – Separate selection for each of the clock/qualifier channels and one per group of 16 data channels for each 34 channel probe.

Threshold Accuracy (including probe) – ±(35 mV + 1%).

Minimum Input Signal Swing – 300 mV (single ended).
V_{MAX} - V_{MIN} > 150 mV (differential).

Input Signal Minimum Slew Rate – 200 mV/ns typical.

State Acquisition Characteristics

State Acquisition

Full Channel	Half Channel
235 MHz Standard	N/A
450 MHz Optional	450 MHz / 450 Mbps or 235 MHz / 470 Mbps (DDR)

State Record Length with Time Stamps

Full Channel	Half Channel*[1]
512 Kb Standard	1 Mb
2 Mb Optional	4 Mb
8 Mb Optional	16 Mb
32 Mb Optional	64 Mb

*[1] Half-channel record length available with option 45 only.

Setup-and-Hold Time Selection Range – 16 ns range that may be shifted towards the setup region by 0 ns [+8, -8] ns, 4 ns [+12, -4] ns, or 8 ns [+16, 0] ns.

Setup-and-Hold Window – All Channels: 625 ps typical.
Single Channel: 500 ps typical.

Minimum Clock Pulse Width – 500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 750 ps (P6810).

Active Clock Edge Separation – 400 ps.

Demux Channel Selection – Channels can be demultiplexed (by two) to other channels through user interface with 8 channel granularity. Available with option 45 only.

Timing Acquisition Characteristics

MagniVu™ Timing Sample Rate – 125 ps max, adjustments to 250 ps, 500 ps, 1 ns, and 2 ns.

MagniVu Timing Record Length – 16 Kb per channel, with adjustable trigger position.

Timing Resolution (quarter/half/full channels) – 500 ps/1 ns/2 ns to 50 ms.

Timing Resolution with Glitch Storage Enabled (full channels) – 4 ns to 50 ms.

Timing Record Length (with or without transitional storage)

Full Channel	Half Channel	Quarter Channel
512 Kb Standard	1 Mb	2 Mb
2 Mb Optional	4 Mb	8 Mb
8 Mb Optional	16 Mb	32 Mb
32 Mb Optional	64 Mb	128 Mb

Timing Record Length with Glitch Storage Enabled – Half of default main record length.

Channel-to-Channel Skew – 300 ps typical.

Minimum Recognizable Pulse/Glitch Width (single channel) – 500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 750 ps (P6810).

Minimum Detectable Setup/Hold Violation – 250 ps.

Minimum Recognizable Multichannel Trigger Event – Sample period + channel-to-channel skew.

Trigger Characteristics

Independent Trigger States – 16.

Maximum Independent If/then Clauses per State – 16.

Maximum Number of Events per If/then Clause – 8.

Maximum Number of Actions per If/then Clause – 8.

Maximum Number of Trigger Events – 18 (2 counter/timers plus any 16 other resources).

Number of Word Recognizers – 16.

Number of Transition Recognizers – 16.

Number of Range Recognizers – 4.

Number of Counters/Timers – 2.

Trigger Event Types – Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot.

Trigger Action Types – Trigger module, trigger all, modules, trigger main, trigger MagniVu, store, don't store, start store, stop store, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing.

Maximum Triggerable Data Rate – 500 MHz.

Trigger Sequence Rate – DC to 500 MHz (2 ns).

Counter/Timer Range – 51 bits each (>50 days at 2 ns).

Counter Rate – DC to 500 MHz (2 ns).

Timer Clock Rate – 500 MHz (2 ns).

Counter/Timer Latency – 2 ns.

Range Recognizers – Double bounded (can be as wide as any group (408 channel max), must be grouped according to specified order of significance).

Setup-and-Hold Violation Recognizer Setup Time Range – From 8 ns before to 7 ns after clock edge in 125 ps increments.

Setup-and-Hold Violation Recognizer Hold Time Range – From 7 ns before to 8 ns after clock edge in 125 ps increments.

Trigger Position – Any data sample.

MagniVu Trigger Position – MagniVu position can be set from 0% to 60% centered around the MagniVu trigger.

Storage Control (data qualification) – Global (conditional), by state (start/stop), block, by trigger action, or transitional. Force main prefill selection is available to fill memory before the trigger position prior to triggering the analyzer.

Physical

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

Ordering Information

TLA7NAx Logic Analyzer Modules

Includes: Certificate of calibration, installation manual, TLA Documentation CD, one-year warranty (return to Tektronix).
Probes must be ordered separately.

TLA7NA1 – 34-channel Logic Analyzer module, 125 ps MagniVu™ Acquisition simultaneous with 500 ps Timing and 235 MHz State, 512 Kb Record Length Logic Analyzer Module.
Options for up to 32 Mb record length and/or up to 450 MHz State.

TLA7NA2 – 68-channel Logic Analyzer module, 125 ps MagniVu™ Acquisition simultaneous with 500 ps Timing and 235 MHz State, 512 Kb Record Length Logic Analyzer Module.
Options for up to 32 Mb record length and/or up to 450 MHz State.

TLA7NA3 – 102-channel Logic Analyzer module, 125 ps MagniVu™ Acquisition simultaneous with 500 ps Timing and 235 MHz State, 512 Kb Record Length Logic Analyzer Module.
Options for up to 32 Mb record length and/or up to 450 MHz State.

TLA7NA4 – 136-channel Logic Analyzer module, 125 ps MagniVu™ Acquisition simultaneous with 500 ps Timing and 235 MHz State, 512 Kb Record Length Logic Analyzer Module.
Options for up to 32 Mb record length and/or up to 450 MHz State.

Logic Analyzer TLA7NAx Module Options

(Base configuration is 512 Kb record length at 235 MHz state.)

Opt 7S – Increase to 2 Mb Record Length.

Opt 8S – Increase to 8 Mb Record Length.

Opt 9S – Increase to 32 Mb Record Length.

Opt 45 – Increase state speed to 450 MHz.

Logic Analyzer Probe Selection Guidelines

There is a flexible choice of logic analyzer probes available for use with TLA7NAx modules. Please see logic analyzer probe data sheets for more information.

TLA7NAx Service Options

Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. D1 – Calibration Data Report

Opt. D3 – Calibration Data Report 3 Years (with Option C3).

Opt. D5 – Calibration Data Report 5 Years (with Option C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

Opt. IN – Product Installation Service.

CE

ISO 9001

Product(s) are manufactured in ISO registered facilities.

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