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Service Manual

Tektronix

TLA 510 & 520
Logic Analyzer

070-8976-04

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

CE

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

Injury Precautions

Use Proper Power Cord

To avoid fire hazard, use only the power cord specified for this product.

Avoid Electric Overload

To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Ground the Product

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Explosive Atmospheres

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Use Proper Power Source

Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

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Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:



WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*



CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols in This Manual

This symbol may appear in the manual:



This symbol indicates where specific cautions and warnings are found.

Symbols on the Product

These symbols may appear on the product:



DANGER
High Voltage



Protective ground
(earth) terminal



ATTENTION
Refer to
manual



Double
Insulated

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Certifications

CSA Certified Power Cords

CSA Certification includes the products and power cords appropriate for use in the North America power network. All other power cords supplied are approved for the country of use.

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Service Safety Summary

Only qualified personnel should perform service procedures. Read this Service Safety Summary and the General Safety Summary before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Caution When Servicing the CRT

To avoid electric shock or injury, use extreme caution when handling the CRT. Only qualified personnel familiar with CRT servicing procedures and precautions should remove or install the CRT.

CRTs retain hazardous voltages for long periods of time after power is turned off. Before attempting any servicing, discharge the CRT by shorting the anode to chassis ground. When discharging the CRT, connect the discharge path to ground and then the anode. Rough handling may cause the CRT to implode. Do not nick or scratch the glass or subject it to undue pressure when removing or installing it. When handling the CRT, wear safety goggles and heavy gloves for protection.

Use Care When Servicing With Power On

To avoid electric shock, do not touch exposed connections.

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

X-Radiation

To avoid x-radiation exposure, do not modify or otherwise alter the high-voltage circuitry or the CRT enclosure. X-ray emissions generated within this product have been sufficiently shielded.

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Preface

This manual contains service information for the TLA 510 & 520 Logic Analyzer. The basis of the logic analyzer is a system unit (mainframe) that contains a single-host controller board and up to two slots for either two acquisition modules or one acquisition module and one pattern generator. Also, the logic analyzer contains a floppy drive, a hard drive, a keyboard, and a color monitor.

The information in this manual explains how to verify, service, troubleshoot, and repair the system unit to the module or board level.

This manual contains the following service information:

- *Specifications* describes functional characteristics and performance requirements for the TLA 510 & 520 system unit and its associated modules.
- *Operating Information* provides instruction on installation and tells you how to operate the TLA.
- *Theory of Operation* provides descriptions of system unit modules. For those modules not repaired at the user site, general descriptions are provided, sufficient to guide the technician to a faulty module.
- *Performance Verification* describes how to verify the functional performance of the system unit.
- *Adjustment Procedures* describes how to perform adjustments on the system unit and modules.
- *Maintenance* describes the following:
  - How to remove and replace modules and system unit components
  - General troubleshooting procedures for system unit and modules
  - How to perform maintenance on the system unit and modules
- *Options* lists the options to the logic analyzer.
- *Replaceable Electrical Parts* lists all the electrical parts associated with the system unit. Parts for modules supported with separate service manuals are not included.
- *Diagrams* contains circuit board parts locator illustrations
- *Replaceable Mechanical Parts* lists the mechanical parts for the system unit.

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Related Manuals

The logic analyzer documentation consists of the standard accessory user manual and this optional accessory service manual. The service manual assumes that the reader is familiar with the logic analyzer and its user manual.

Manual Conventions

The following terms and conventions are used throughout this manual:

- The term *system unit* refers to the mechanical chassis of the logic analyzer.
- The term *mainframe* when used in the menus refers to the system unit.
- The term *module* refers to either to the acquisition or pattern generation circuit card. The term also appears in the menus displayed on the terminal.
- The term *92C96* refers to the 92C96 Data Acquisition Module. The 92C96 is the configurable 92A96 Data Acquisition Module.
- The term *92A96* refers to the 92A96 Data Acquisition Module. The 92A96 functions identically to the 92C96 Data Acquisition Module.
- The terms *92A96* and *92C96* are used interchangably throughout this manual. Both terms refer to either version of the logic analyzer module unless stated otherwise.
- The tilde symbol (~) represents active low signals.

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Introduction

Service Strategy

This manual contains all the information needed for periodic maintenance of the TLA 510 & 520 Logic Analyzers. (Examples of such information are procedures for checking performance and for readjustment.) Further, it contains all information for repair to the board or module level. This means that the procedures, diagrams, and other troubleshooting aids help isolate failures to a specific module, rather than to components of that module. Once a failure is isolated, replace the module with a replacement or exchange module obtained from Tektronix.

All modules are listed in the *Electrical and Mechanical Parts List*. To isolate a failure to a board or module, use the fault isolation procedures found in the *Maintenance* section. To remove and replace any failed board or module, follow the instructions in *Removal and Replacement Procedures*, also found in *Maintenance*.

Service Offerings

Tektronix provides service to cover repair under warranty. Other services are available that may provide a cost-effective answer to your service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians, trained on Tektronix products, are best equipped to service your TLA 510 & 520 Logic Analyzers. Tektronix technicians are apprised of the latest information on improvements to the product as well as the latest product options.

Warranty Repair Service

Tektronix warrants this product for one year from the date of purchase. (The warranty appears after the title page and copyright page in this manual.) Tektronix technicians provide warranty service at most Tektronix service locations worldwide. Your Tektronix product catalog lists all service locations worldwide.

Repair Service

The following services may be purchased to tailor repair of your TLA 510 & 520 Logic Analyzers to fit your requirements.

Depot Service. Tektronix offers single per-incident repair and annual maintenance agreements that provide repair of the logic analyzer.

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Of these services, the annual maintenance agreement offers a particularly cost-effective approach to service for many owners of the TLA 510 & 520 Logic Analyzers. Such agreements can be purchased to span several years.

On-Site Service. The standard annual maintenance agreement includes on-site service, with repair done at your facility. This service reduces the time your logic analyzer is out of service when repair is required.

Self Service

Tektronix supports repair to the module level by offering a *Module Exchange* program.

Module Exchange. This service reduces down time for repair by allowing you to exchange most modules for remanufactured ones. Tektronix ships you an updated and tested exchange module from the Beaverton, Oregon service center. Each module comes with a 90-day service warranty.

For More Information. Contact your local Tektronix service center or sales engineer for more information on any of the repair or adjustment services previously described.

Before You Begin

This manual is for servicing the TLA 510 & 520 Logic Analyzers. To prevent injury to yourself or damage to the logic analyzer, do the following tasks before you attempt service:

- Be sure you are a qualified service person
- Read the Safety Summary found at the beginning of this manual
- Read *Service Strategy* in this section

When using this manual to service your logic analyzer, be sure to heed all warnings, cautions, and notes.

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Specifications

This chapter provides a description and a list of specifications for the TLA 500 series logic analyzer.

Product Description

The Tektronix TLA 510 and 520 Logic Analyzers consist of a system unit, color X Terminal, application software packages, and probes for acquiring data.

The logic analyzer is available in one of two products: the 100-channel TLA 510 and the 200-channel TLA 520. Each come with a standard 8 Kbytes of acquisition memory. Both logic analyzers are available with several options including deeper memory depths. A Pattern Generator (92S16) is available for the TLA 510 only.

Hardware

The system unit provides computing power, input/output features, and mass storage for the internal acquisition and pattern generation modules.

The standard display device is a color X Terminal with a keyboard and a mouse. Interactive menus define the contents of the system.

The system unit consists of the following major internal components:

- 100 channels of data acquisition (200 channels for the TLA 520)
- 40 MHz 68ECO30 CPU
- Hard and floppy disk drives
- RS-232 ports
- Local Area Network (LAN) interface
- External input and output connections

The mass-storage device in the system unit is a SCSI hard disk drive. The operating system software is installed on the hard disk.

A 3.5-inch floppy disk drive is standard in the system unit. The floppy disk drive is used for loading application software from floppy disk, copying user files for use on other TLA 510 & 520 mainframes, and making or restoring backup user files.

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The system unit supports three 9-pin RS-232 communication ports accessible on the rear panel:

- The Terminal port connects the system unit to a console terminal (X Terminal serial window or other serial display devise).
- The Host port connects the system unit to a host computer system.
- The Auxiliary port connects the system unit to other RS-232-compatible devices (for example, a printer).

The local area network connects the system unit to the X Terminal. The LAN software also provides a means to transfer files between the logic analyzer and a host computer through ftp (file transfer protocol) and other protocols. An optional 92LANP application software product allows you to remotely control the logic analyzer through the LAN interface.

A 37-pin female D-connector allows you to monitor or drive external devices with the optional 92PORT application software. The connector provides eight discrete inputs, eight discrete outputs, and corresponding strobe read and write signals.

Configurations

The TLA 510 logic analyzer comes with 100 channels of acquisition and is available with acquisition memory depths of 8 Kbits, upgradable to 32 Kbits, 128 Kbits, 512 Kbits, or 2 Mbits. The TLA 510 logic analyzer can be upgraded with up to 200 channels of acquisition or 16 channels of pattern generation at 50 MHz.

The TLA 520 logic analyzer comes with 200 channels of acquisition and is available with acquisition memory depths of 8 Kbits, upgradable to 32 Kbits, 128 Kbits, 512 Kbits, or 2 Mbits.

To upgrade either logic analyzer, you must return the instrument to an authorized service center and have Tektronix perform the upgrade. For information regarding available upgrades, contact your local Tektronix sales representative.

Both logic analyzers come standard with a 14-inch X Terminal, 101-key keyboard, and mouse.

System Software

The logic analyzer is controlled by system software stored on the hard disk drive.

To determine the version number of the current system software, check the Version menu. The Version menu displays the version numbers of the internal components, system and application software in the system unit; both menus are in the Utility menu group.

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System software loads into memory (RAM) at power-on, and performs the following tasks:

- Manages system resources (that is, memory, CPU, storage devices, common control functions, files and file access, and data communication I/O devices)
- Provides system service subroutines so that internal acquisition and pattern generation hardware and applications programs have a common set of subroutines
- Provides common system control functions such as start/stop control and allocation of system hardware resources
- Controls communication between standard subroutines, modules, application software, and I/O devices (standard, optional, and mass storage)

As a backup, the instrument can also load system software from a set of floppy disks.

Application Software

Tektronix offers application software packages; each package includes a user manual. Refer to the appropriate manual for more detailed information. A list of application software currently installed is shown in the Version Menu. To load application software from a floppy disk, refer the *TLA 510 & 520 User Manual*.

The Microprocessor Support packages provide both hardware and software mnemonic disassembly formats. Each support package includes a microprocessor-specific probe adapter which provides the hardware necessary to properly acquire data from the microprocessor. Some of the microprocessor support packages include reference memories that you can use with the manual to become more familiar with the package.

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Acquisition and Pattern Generation Modules

Data acquisition and pattern generation modules, consisting of one or two printed-circuit boards, are the building blocks of the TLA 510 and 520 system. These boards are installed in the system unit bus slots according to configuration guidelines in the user manual for each module. Refer to Table 1–1 for a list of available modules. Brief descriptions of these modules are included in *Theory of Operation*. For detailed information on individual modules, including specifications and menu and field descriptions, refer to the appropriate user manual.

Table 1–1: TLA 510 and 520 Acquisition and Pattern Generation Modules

Module	Purpose	Channels	Depth	Speed
92C96[1]	acquisition	96	8K[2]	100 MHz
92C96D	acquisition	96	32K	100 MHz
92C96XD	acquisition	96	128K	100 MHz
92C96SD	acquisition	96	512K	100 MHz
92A96UD	acquisition	96	2M	100 MHz
92S16	pattern generation	16	1K	50 MHz

1 **All 92C96 and 92A96 modules offer High-Speed timing asynchronous support of 48 channels at 200 MHz and 24 channels at 400 MHz.**

2 **8 K is standard in the TLA 510 and 520.**

Characteristics Tables

This section describes the electrical, mechanical, and environmental and safety characteristics of the following:

- TLA 510 and 520 system unit with the 92LANSE Module
- 92C96 and 92A96 Acquisition Module and Probes
- 92S16 Pattern Generation Module
- P6463A Pattern Generation Probe
- P6460 External Control Probe

The Performance Requirements column items are product specifications that can be verified using the Performance Check procedures provided in this manual (refer to a qualified service technician). The Supplemental Information column provides pertinent characteristic operating details that are not guaranteed.

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TLA System Unit

The following tables list the specifications for the TLA 510 and 520 system unit:

- Table 1–2 Environmental and Safety
- Table 1–3 Mechanical
- Table 1–6 Electrical
- Table 1–7 Standard Electrical Interfaces
- Table 1–8 Discrete I/O Signals
- Table 1–9 Recorded Data Interface

Table 1–2: TLA 510 and 520 Environmental and Safety

Characteristic	Supplemental Information
Atmospherics	
Temperature	As per Tektronix Standard 062-2847-00
Operating	+10° C to +40° C (+50° F to +104° F)
	±20° C/hr (±36° F/hr) maximum gradient
Nonoperating	–40° C to +60° C (–40° F to +140° F)
	±30° C/hr (±54° F/hr) maximum gradient
Relative Humidity	As per Tektronix Standard 062-2847-00 (noncondensing) Some discoloration of internal mechanical parts may occur.
Operating	20% – 80%, 30° C (86° F) maximum wet bulb
Nonoperating	10% – 90%, 40° C (104° F) maximum wet bulb
Altitude	As per Tektronix Standard 062-2847-00
Operating	3 km (10,000 ft) maximum, limited by hard disk drive
Nonoperating	12 km (40,000 ft) maximum, limited by hard disk drive
Dynamics	
Vibration	As per Tektronix Standard 062-2858-00, Rev. B
Operating	Limited by hard and floppy disk drives
Random Vibration	0.24 G_{RMS}, 5 – 500 Hz
5 – 350 Hz	0.000125 G^2/Hz APSD
350 – 500 Hz	–3 dB/octave slope
500 Hz	0.0000876 G^2/Hz APSD
Nonoperating	Limited by hard and floppy disk drives
Random Vibration	1.43 G_{RMS}, 10 – 300 Hz
	Limited by power supply
10 – 50 Hz	0.029 G^2/Hz APSD
50 – 300 Hz	–8 dB/octave slope

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Table 1–2: TLA 510 and 520 Environmental and Safety (Cont.)

Characteristic	Supplemental Information
Shock	As per Tektronix Standard 062-2858-00, Rev. B
Operating	10 G, 11 ms, 1/2 sine; limited by hard disk drive[1]
Nonoperating	20 G, 11 ms, 1/2 sine; limited by power supply
Bench Handling	As per Tektronix Standard 062-2858-00, Rev. B
Operating/Nonoperating	2 inches on bottom, along all four edges, limited by hard disk, and floppy disk drive
Packaged Product	As per Tektronix Standard 062-2858-00, Rev. B
Manual Handling	Assurance Level 1
Warehouse Stacking	Assurance Level 2
Electromagnetic Compatibility (EMC)	As per EC Council Directive 89/336/EEC (EC92), and EN 50081-1 (emissions), EN50082-1 (immunity)
Emissions	Emissions shall be within the following limits:
Radiated	Class A limits, EN 55011
Conducted	Class A limits, EN 55011
Power Line Harmonics	EN 60555-2
FCC	Emissions are below FCC CFR Title 47, Part 15, Subpart B, Class A specification limits for radiated and conducted emissions, with test cables removed.
Immunity	
Electrostatic Discharge (ESD) IEC 801-2	The system unit shall withstand discharge through a 330 Ω series resistor of a 150 pF capacitor charged with up to 8 kV, with no component failure or corruption of the system software.[2]
Radio Frequency Electromagnetic Field IEC 801-3	The system unit shall withstand 3 volts/meter electromagnetic field over the frequency range of 27 MHz to 500 MHz, with no component failure or corruption of the system software.[2]
Fast Transients, Common Mode IEC 801-4	The system unit shall withstand fast transients on AC power lines of 1 kV, 5/50 ns, at 5 kHz, and on signal and control lines of 0.5 kV, 5/50 ns, at 5 kHz, with no component failure or corruption of the system software.[2]
Safety	The system unit complies with the requirements of UL 3111-1, IEC 1010-1, EN61010-1, and CSA C22.2 No. 1010.1-92. The terminal is listed by a nationally recognized testing laboratory (NRTL) and is CSA certified.
Safety Certification Compliance	Safety Class 1 Installation Category II Pollution Degree 2

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Table 1–2: TLA 510 and 520 Environmental and Safety (Cont.)

Characteristic	Supplemental Information
Installation Requirements (System Unit)	
Power Consumption	700 Watts maximum (@ 75% efficiency)
Heat Dissipation	2400 BTU/Hour maximum
Surge Current	40 A maximum at 127 VAC, 0.5 cycle
	75 A maximum at 250 VAC, 0.5 cycle
Cooling Clearance	8 inches on all sides
Fan Noise	50 dB (A) maximum

1 **During floppy disk drive read and write operations, shock is limited to 5 G, 11 ms, 1/2 sine.**

2 **Degradation of performance may occur momentarily during the electrostatic discharge, fast transient, power line surge, or electromagnetic field, in the way of incorrectly acquired data; which in turn may cause false triggers or other momentary erratic operation of the instrument. Corruption of system software includes any other non-temporal result which prevents the instrument from returning to its normal operating mode.**

Table 1–3: TLA 510 and 520 Mechanical

Characteristic	Description
Weight	38 lbs (17 kg) with no instrument modules 44 lbs (20 kg) fully loaded
Physical Dimensions	
Height	6.25 in (15.87 cm)
Width	19.13 in (48.58 cm)
Depth	23.50 in (59.69 cm)
Finish	
Top	Smoke Tan
Base	Slate Gray

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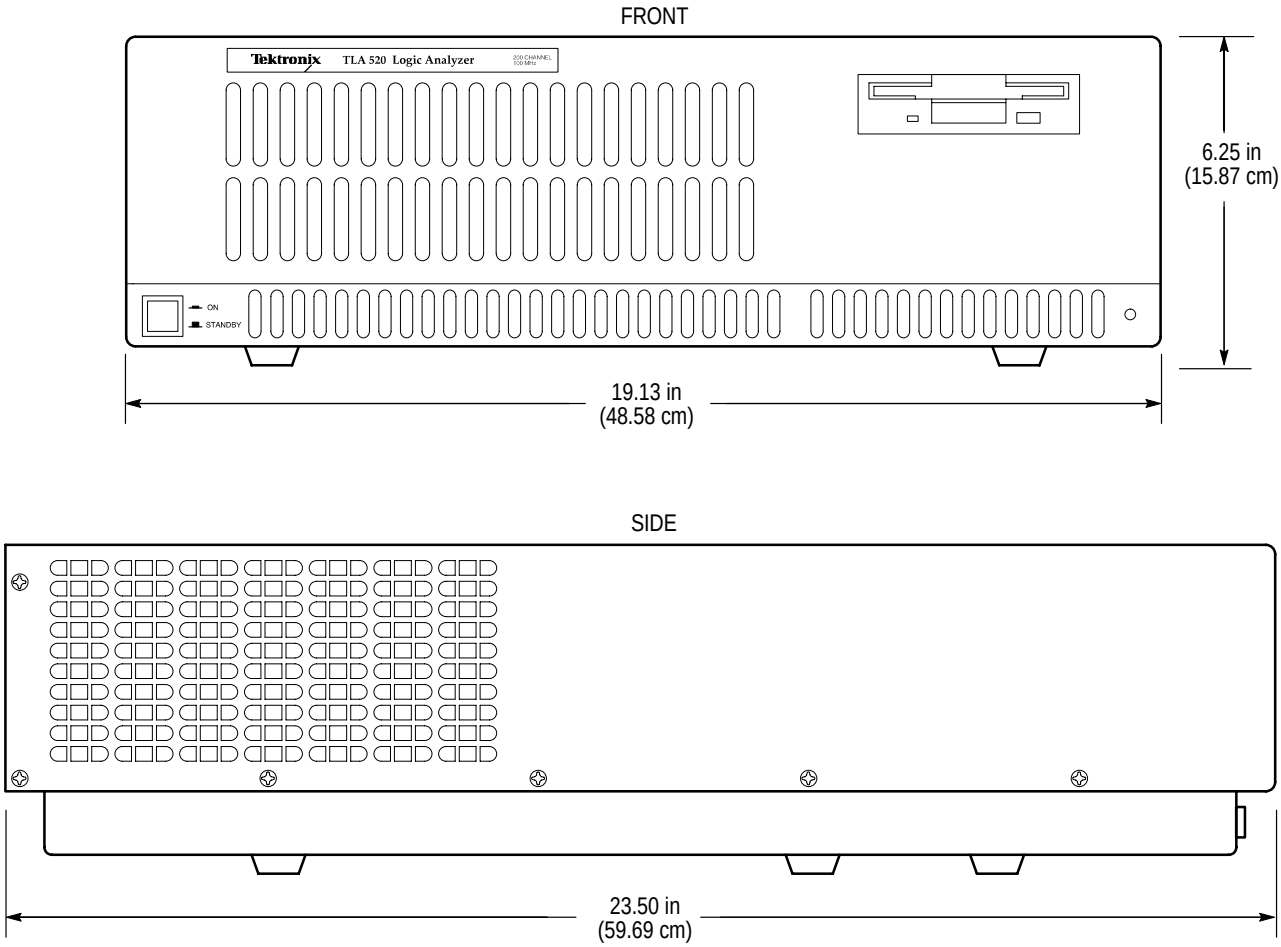


Figure 1–1: System Unit Dimensions

Table 1–4: Terminal Physical Dimensions

Terminal	Weight	Height	Width	Depth
9203/05XT				
Logic Unit	9 lbs (4.05 kg)	2.5 in (6.4 cm)	14.3 in (36.3 cm)	13.5 in (34.3 cm)
Monitor	42.2 lbs (19.2 kg)	16.3 in (41.5 cm)	16.3 in (41.5 cm)	17.4 in (44.2 cm)
9206XT				
Logic Unit	4 lbs (1.8 kg)	2.17 in (5.53 cm)	11.0 in (27.9 cm)	12.25 in (31.12 cm)
15-inch Monitor	28. 6 lbs (13.0 kg)	15.0 in (38.0 cm)	14.6 in (37.2 cm)	16.2 in (41.2 cm)
17-inch Monitor	38.9 lb (17.7 kg)	16.6 in (42.2 cm)	16.1 in (41.0 cm)	17.2 in (43.8 cm)

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Table 1–5: Terminal Keyboard Physical Dimensions

Characteristic	Specification
Weight	2.6 lbs (1.1 kg)
Height	Flat 1.7 in (4.3 cm); to Key 1.0 in (2.54 cm); Tilted 2.4 in (6.07 cm)
Width	18.5 in (46.9 cm)
Length	7.3 in (18.5 cm)

Table 1–6: TLA 510 and 520 Electrical

Characteristic	Performance Requirement	Supplemental Information
Serial Communication Interface		
Operational Modes		Full Duplex, Half Duplex, Data Only
Baud Rates		
Terminal Port		38400 (default), 19200, 9600, 4800, 2400, 1200, 600, 300, 110 (± 0.05%)
Host Port		38400, 19200, 9600 (default), 4800, 2400, 1200, 600, 300, 110 (± 0.05%)
Auxiliary Port		38400, 19200, 9600 (default), 4800, 2400, 1200, 600, 300, 110 (± 0.05%)
Ethernet LAN Interface		
Supports TCP/IP with IEEE 802.3 10Base5 and 10Base2 (Supports largest Ethernet packets of 1500 data bytes.)	Transfer a file from a host to the TLA 510 and 520 Logic Analyzer and back using FTP with either 10Base5 or 10Base2	For 10Base2 specification, capacitive loading is 5 pF, (plus 9-inch coaxial cable, equivalent capacitive loading is 12 pF)
Supports Internet Control Message Protocol (ICMP)		Type 0: echo reply message Type 8: echo message
Supports Address Resolution Protocol (ARP)		
Supports File Transfer Protocol (FTP)		Server only
Supports Trivial File Transfer Protocol (TFTP)		Server only
System Unit Power		
Primary Power Input		The system unit, with appropriate power cord, can operate over either voltage range, requires a fuse change (external access).
With Standard Power Cord 115 VAC, single phase	90 VAC – 127 VAC, < 8 A	8 Amp. Slow-blow fuse (3AG)
With Option A1 – A5 230 VAC,single phase	180 VAC – 250 VAC, < 4 A	5 Amp. Slow-blow fuse (5 × 20 mm)

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Table 1–6: TLA 510 and 520 Electrical (Cont.)

Characteristic	Performance Requirement	Supplemental Information
Primary Line Frequency		47 Hz – 63 Hz Operation over 63 Hz may exceed protective ground conductor leakage current limit of 3.5 mA.
Primary Ground Resistance		Routine test to check ground continuity between chassis and protective earth ground. Power plug ground to chassis is $< 0.1\ \Omega$
Primary Circuit Dielectric Withstand Voltage		1500 V_{RMS}, 50 Hz – 60 Hz for 10 seconds without breakdown
Ride Through (cycle drop out)		Under full load and low line voltage, all DC voltages remain in regulation when AC power is removed for 20 ms or less. Otherwise, the system unit shuts down
Switching Frequency		140 kHz, typical
Over Temperature Shutdown		75° C, ±5° C

Table 1–7: Standard Electrical Interfaces

Characteristic	Description
RS-232 Interface	The interface is defined as a Data Communications Equipment (DCE) pinpoint.
Operational Modes	Full Duplex, Half Duplex, Flagging
Data Type	Asynchronous
Control Lines	DCD, CTS, DSR
Bits per Character	7-bit ASCII, 8-bit Binary
Parity	None, Odd, Even
Stop Bits	1
Protocols	Kermit, Xmodem (PCL)
Flow Control	XON/XOFF, DTR/CTS (receive & transmit)
Baud Rates	
Terminal	38400 (default), 19200, 9600, 4800, 2400, 1200, 600, 300, 110
Host	38400, 19200, 9600 (default), 4800, 2400, 1200, 600, 300, 110
Auxiliary	38400, 19200, 9600 (default), 4800, 2400, 1200, 600, 300, 110
Ethernet LAN Interface	The interface conforms to the ANSI/IEEE 802.3, 3rd Edition, 1992; also known as ISO/IEC 8802-3, 1992 except that “Control Out” functionality is not supported. Refer to the standard for details about this interface.

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Table 1–8: Discrete I/O Signals

Characteristic	Description
Output Signals SO–1:8	Outputs can be momentary or latching (Signal pins 2 – 9 with respective ground pins 21 – 28)
Drive (typical)	Driven from standard 74ALS996 with 10 Ω series resistors and protection diodes
Negative-going pulse width (typical)	2 ms, or greater, under momentary operation
Recommended maximum load	1 standard STTL load with up to 250 pF capacitance for edge integrity
Read Strobe (pin 10) Write Strobe (pin 1)	With respective ground pin 29 With respective ground pin 20
Drive (typical)	Driven from standard 74F14
Negative-going pulse width (typical)	With active positive edge
Read Strobe	225 ns
Write Strobe	150 ns
Recommended maximum load	1 standard STTL load with up to 60 pF capacitance for edge integrity
+5 V (pin 19)	Fused at 0.75 A
Ground (pins 20 – 37)	Fused at 1.5 A
Input Signals SI–1:8	Inputs are level only (Signal pins 11 – 18 with respective ground pins 30 – 37)
Load (typical)	1 standard FTTL load with 4.7 kΩ pull-up resistor and approximately 60 pF capacitive load, also includes 10 Ω series resistors and protection diodes

Table 1–9: Recorded Data Interface

Characteristic	Supplemental Information
Floppy Disk Format	Standard floppy disk drive is 3.5-inch, high density, 135 TPI-1.44 Mbyte (low-level PC format compatible), type 2HD.
Low-Level PC Disk Format	Low-Level format for personal computers is supported, but the DOS operating system file structure is not supported. Use the DASdisk utility to read or write user files on a PC.
SunOS Operation	Sun workstations, running SunOS, can directly read and write user files using the tar command. A special utility program is not needed.
Bad Sector Mapping	Bad sector mapping is not supported. Floppy disks are unusable if an error (bad sector) is found.

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Acquisition Module and Probes

The following tables list the specifications for the 92C96 Acquisition Module and probes:

- Table 1–10 Environmental (probe only)
- Table 1–11 92C96 Physical
- Table 1–12 92C96 Electrical

NOTE. *The Safety and Environmental specifications for the 92C96 modules are the same as the TLA 510 and 520.*

Table 1–10: 92C96 Probe Environmental

Characteristic	Description
Temperature	
Operating	–15° C to +55° C
Non-Operating	–62° C to +85° C
Humidity	
Altitude	10–90% relative humidity (non operating)
Operating	15,000 ft (4.5 km) maximum
Non-Operating	50,000 ft (15 km) maximum

Table 1–11: 92C96 Physical

Characteristic	Description
Overall Dimensions	
Width	Approx. 10 in (24.5 cm)
Length	Approx. 15.5 in (39.37 cm)
Probe Length-ribbon or coaxial cable (including podlets)	Approx. 72 in (183 cm)
90-Channel Interface (optional)	
Width	Approx. 7.5 in (19 cm)
Length	Approx. 5.1 in (13 cm)
Height	Approx. 1.14 in (3 cm)

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Table 1–12: 92C96 Electrical

Characteristic	Performance Requirements	Supplemental Information
Input (at probe, all chan.)		
Input R		100 kΩ nominal
Input C		9.4 pF nominal, 10 pF max.
Bandwidth (min. probe)		140 MHz
Absolute max. voltage limits		±15 V (p-p)
Min. TTL signal input (ribbon cables)		1.2 V (p-p) nominal (centered on threshold)
Min. ECL signal input (coaxial cables)		600 mV (p-p) nominal (centered on threshold)
Threshold levels		–4.0 V to +8.75 V; 50 mV steps
DC threshold accuracy		±75 mV
Max. operating input amplitude		10 V (p-p); for signals above 5.5 V (p-p) threshold must be set to $\left(\frac{V_{iH} + V_{iL}}{2}\right) \pm .1V$
Synchronous		
Min. Setup time	5.5 ns ECL (ribbon cables) 5.0 ns TTL[1, 2]	5.0 ns ECL (coaxial cables)
Min. Hold time	0 ns [1, 2]	
Min. time between clock edges	10 ns	With multiple clock edges
Max. external clock rate	100 MHz	Using single-edge clock
Min. clock pulse width	4.9 ns ECL	4.3 ns TTL, high or low, measure at threshold [2]
Setup and Hold time — Clock Qualifiers (external clock and 'before' edge mode):		
Clock as Qualifier (Clock 0, 1, 2, 3)		
setup time	5 ns [2]	
hold time	0 ns [2]	
Qualifier (C2: 0, 1, 2, 3)		
setup time	6.5 ns [2]	
hold time	0 ns [2]	
Max. transaction rate	100 MHz (10 ns)	
Asynchronous		
Channel to channel skew	2.5 ns	Timing accuracy; 2X the sample period +3.5 ns
Pulse width guaranteed to be sampled (multichannel)	Sample period + 2.5 ns [1]	

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Table 1–12: 92C96 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Pulse width guaranteed to be triggered (multichannel)		General Purpose: sample period + 3.5 ns High Speed (5 ns or slower): 2X sample period + 3.5 ns High Speed (2.5 ns): 4X sample period + 3.5 ns
Glitch pulse width guaranteed to be sampled		3.5 ns, 1st order (two edges in sample interval)
Max. asynchronous clock rate		
96 Channels	100 MHz (10 ns)	
48 Channels	200 MHz (5 ns)	
24 Channels	400 MHz (2.5 ns)	
Timebase accuracy		
100 MHz or greater		±300 ps ±0.05%
50 MHz or less		± 0.05%, 400 ps p-p jitter
Counters/Timers		
Counter accuracy	± 0 counts, +1 state clock for event generation	
Timer accuracy (event generation)	+1/–0 state clock, +1/–1 timer clock, ±0.05%	
Timebase accuracy (internal)		± 0.05%, 400 ps p-p jitter
Sync Out		
Delay (from probe tip)	75 ns max.	68 ns typical
Min. pulse width		8.5 ns; External clock ±1.5 ns
Voltage range with 1 MΩ load	0 V ±0.5 V 5 V ±0.5 V	
Output source impedance		50 Ω nominal
Timestamp		
Timebase accuracy		
Short term	±3 ns	
Long term	±1 count (MCLK) ±0.05%	
Timestamp resolution	10 ns	
Timestamp width	44 bits	
Timestamp range	2 days	
Module-to-module relative accuracy		25 ns; skew between multiple 92C96s in a single instrument

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Table 1–12: 92C96 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Power Requirements		150[3] watts max.
Power available to probe adapter		
–15 V Supply		0.5 A max.
+5 V Supply		0.1 A max.

1 **Min. slew rate: .8 V/ns to guarantee Setup and Hold times (degrades S/H below this value)**

2 **Measured with 1.6 V (p-p) input signal**

3 **92C96 Acquisition Module power requirements reduced to 140 W effective as of DAS serial number B061162**

92S16 Pattern Generator Module

The following tables list the specifications for the 92S16 Pattern Generator module:

- Table 1–13 Physical
- Table 1–14 Electrical

NOTE. *The Safety and Environmental specifications for the 92S16 module are the same as the TLA 510 and TLA 520.*

Table 1–13: 92S16 Physical

Characteristic	Description
Overall Dimensions	
Height	Approx. 10 in (25.4 cm)
Length	Approx. 15.5 in (39.37 cm)

Table 1–14: 92S16 Electrical

Characteristic	Performance Requirements	Supplemental Information
Pattern Processor		
Sequence Number		0 to 1023, 1024 lines More than one microinstruction can be assigned to the same sequence line. The maximum number depends on the card types installed and the features you have enabled.

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Internal Registers:		2 16-bit registers named A & B
Instructions		LOAD (load value), INCR (increment value by one), DECR (decrement value by one), and "Hold" (hold is the default operation; no instruction is entered).
Micro instructions for algorithmic pattern generation		Seq Flow: Advance to next sequence line (default instruction-Instruction field blank) Halt Jump <to label>[1] Call <to label>[1] Return (ends subroutines) Repeat N (N between 1 and 256) IF A=0 Jump <to label>[1] IF A<>0 Jump <to label>[1] IF B=0 Jump <to label>[1] IF B<>0 Jump <to label>[1] IF Key Jump <to label>[1] (Monitor menu Trace mode feature only) IF IRQ Jump <to label>[1] IF Ext Jump <to label>[1]

1 **A label can be any unique string up to six characters long. Leading and trailing blanks are discarded.**

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Micro instructions for algorithmic pattern generation (Cont.)		Register Operation: Hold A (default instruction – Instruction field blank) Hold B (default instruction – Instruction field blank) Incr A (increment value in A by one) Incr B (increment value in B) Decr A (decrement value in A by one) Decr B (decrement value in B) Output: Output Pattern from group data columns (default operation) Load A Load B Out A (Output value in register A instead of value in 92S16 Group columns) Out B (Output value in register B instead of value in 92S16 Group columns) Hold Out Control: Mask IRQ (mask interrupt request) Unmask IRQ (unmask interrupt request) Trigger (Issue trigger signal to event bus and SMB connector on back of 92S16 card) Incr Page (Increment 92S32 memory page by one) Hold S32 (hold 92S32s at current sequence line) Advance S32 (advance 92S32s to next sequence line)

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
92S16 Electrical Outputs		
Maximum Number of Pattern Data		1024
Pattern Data Width		16 + 2 parallel channels
Data channel maximum skew between channels in the same probe	1 ns at probe connector	Any data channel within a pod will be valid at the probe connector within 1 ns of every other channel from the same probe.
Data channel maximum relative error between data channels from the same probe	2 ns at P6464 Connector (edge positioned)	Any data channel within a pod will be valid at the probe connector within 2 ns relative to any other data channel from the same pod.
Clock Delay		5 ns steps
Tri-State		Any data channel can be inhibited (tri-stated) according to programmed commands entered into the pattern generator. 92S16s can be programmed to inhibit data channels both in response to an internally programmed inhibit bit, or in response to an externally acquired inhibit signal (from P6460 probe), or in response to a Boolean combination of internal and external inhibits.
Vector Source for 92S16		
Pod A		Data pattern from the 8 LSBs of 92S16 data groups, the 8 LSBs of 92S16 register A, the 8 LSBs of 92S16 register B, or a repeat of the 8 LSBs output for the previous clock cycle, regardless of the source.
Pod B		Data pattern from the 8 MSBs of 92S16 data groups, the 8 MSBs of 92S16 register A, the 8 MSBs of 92S16 register B, or a repeat of the 8 MSBs output for the previous clock cycle, regardless of the source.

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Clock Outputs		
Pod Clock Output		1 clock line per probe can be used as a Pod clock.
Number of Pod Clocks		2 Pod clocks
Pod Clock Polarity		Rising or Falling Edge, menu-selectable
Pod Clock Pulse Width		Measured at pod connector
Internal Clock		≥8 ns
External Clock		Input pulse width ±6 ns A TTl-level external clock pulse can be supplied to the P6460 External Control Probe
Pod Clock Delay from External Clock Input		108 ns typical
Pod Clock Maximum Skew between Pods		Add 3 ns for Maximum Skew at pat gen probe tip if adjusted without probe.
Within 92S16	2 ns at pod connector	Edges of any two pod clocks from a single card will occur within 2 ns of each other (measured at pod connector)
Pod clock maximum relative error between pods		Add 3 ns for maximum relative error measured at pat gen probe tip if card was adjusted without a probe.
Within 92S16	4 ns at probe connector	Edges of any two pod clocks within a 92S16 will occur at the pod connector within 4 ns
Pod Clock Edge Positioning		
92S16	±5 ns in 5 ns steps programmable	Pod Clock can be positioned in –5 ns to +5 ns range in 5 ns steps.
Tri-State		Pod Clock may be programmed to be tri-stated (inhibited) by the module. Inhibit control to probe comes either from microcode, or from P6460 External Control Probe, or a Boolean combination
Operating Rate Run Mode 92S16		Up to 50 MHz (20 ns cycle time) determined by the clock selection
Clock Source		Internal or external selectable
Internal		From the time base of the mainframe
External		Signal supplied to P6460 External Control Probe

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Polarity	Rising or falling edge selectable:	
–Period	20 ns min	
–Pulse High	9 ns min	
–Pulse Low	9 ns min	
92S16 External Control Signals		
Using P6460 Probe		External control signals for 92S16 are obtained by a P6460 acquisition probe called the External Control Probe. Some of these signals can also be supplied by the event bus.
Input Threshold:		
Threshold Range	–6.40 V to +6.35 V in 50 mV steps	
Threshold Accuracy	65 mV ±1% of the threshold	
Logic Swing	–40 V to the threshold + 10 V max 500 mV_{p-p} min centered on the threshold	
External Clock Input		1 external clock input edge selectable 9 ns min pulse width
IRQ Input		1 interrupt input from P6460 probe, or backplane general-purpose event lines 3–10, or high-speed event lines 5–8. Two methods of handling interrupts are provided: 1. IRQ Call method calls an interrupt service subroutine whenever the interrupt is detected. 2. IF IRQ Jump instructions test an IRQ flag and cause a branch if the flag has been set. The test only occurs when an If IRQ Jump instruction is executed.
Interrupt Latency		1 cycle for IRQ Call 2 cycles for IRQ Jump If a second interrupt arrives while the first interrupt is being processed, there is no delay in processing the second interrupt after the first action has been completed (no interrupt latency). If an interrupt arrives during execution of a sequence line containing a Repeat instruction, the interrupt will only be serviced after the repeat action has been completed.

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Interrupt Mask		Mask/Unmask instructions enable/disable recognition of an incoming interrupt request for the sequence line containing the instruction. From 11 ns typical after the rising/falling edge selected for 1 clock cycle of the external clock.
IRQ Call		1 level One-level stack is available to save a return address either for an interrupt service call or for a subroutine call.
RQ Call		1 cycle
Processing Cycle Delay		When a valid interrupt request is logged in, the first interrupt vector appears at pat gen probe tip in the cycle next to the cycle in which the interrupt has been sampled.
IRQ Call minimum pulse width		15 ns
IRQ Call input timing window prior to external clock input		10 ns typical To be recognized in a certain cycle, assert the interrupt request in a range of 10 ns prior to the selected edge of the external clock, otherwise recognized in the next cycle.
IRQ Call input timing window prior to pod clock output		110 ns typical to be recognized in a certain cycle, assert the interrupt request in a range of 110 ns typical prior to Pod clock selected edge output, otherwise recognized in a next cycle.
IRQ Jump		Causes Pattern Processor branch if the IRQ flag has been set before tested by “IF IRQ” instruction.
IRQ Jump minimum pulse width		15 ns
IRQ Jump setup time relative to external clock input		15 ns min 15 ns prior to the selected edge of the external clock.
IRQ Jump hold time relative to external input		0 ns max. Assert the IRQ request 0 ns after the selected edge of the external clock.
IRQ Jump set up time relative to pod clock output		108 ns +1 Clock Cycle typical. Assert the IRQ request 108 ns +1 Clock Cycle prior to Pod Clock selected edge output.

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Qualifier Input		1 qualifier input from P6460 Level-selectable Qualifies an interrupt An interrupt is recognized if selected edge is detected on the interrupt input only when the qualifier input stays high- or low-level specified.
Qualifier Input Minimum Pulse Width		15 ns
Qualifier Input		15 ns min
Setup Time Relative to Interrupt Selected Edge		Maintain qualifier input high- or low-level specified for 15 ns prior to the selected edge of the interrupt.
Qualifier Input		0 ns max
Hold Time Relative to Interrupt Selected Edge		Maintain qualifier input high- or low-level specified for 0 ns after the selected edge of the interrupt.
External Jump Input		1 external jump input from P6460 Ext line, general-purpose event lines 3–10, or high-speed event lines 5–8. Level-selectable. Causes Pattern Processor branch if this input is activated only when tested by "If Ext Jump" instruction.
External jump minimum pulse width		15 ns
External jump input setup time relative to external clock input		15 ns min. 10 ns typical. Assert the external jump request 15 ns prior to the selected edge of the external clock.
External jump input hold time relative to external input		0 ns max. Assert the external jump request 0 ns after the selected edge of the external clock.
External jump input setup time relative to pod clock output		115 ns +1 Clock Cycle typical. Assert the external jump request 105 ns +1 Clock Cycle prior to Pod Clock selected edge output.
External inhibit input		1 external inhibit input from P6460. Level-selectable. External inhibit can be ANDed/ORed with the internal inhibit bit-by-pod basis.
External inhibit minimum pulse width		15 ns
External inhibit delay		47 ns typical. When external inhibit is asserted, the data outputs will be inhibited (tri-stated) of 47 ns if the external inhibit only is selected. (Refer to Figure A–3.)

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Table 1–14: 92S16 Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Pause Input		1 pause input from P6460. Level-selectable. Freezes the current data outputs while the pause input remains true.
Pause input minimum pulse width		15 ns
Pause input setup time relative to external clock input		15 ns min. 10 ns typical. Assert the pause request 15 ns prior to the selected edge of the external clock.
Pause input hold time relative to external clock input		0 ns max. Assert the pause request 0 ns after the selected edge of the external clock.
Pause input setup time relative to pod clock output		121 ns typical. Assert the pause request 121 ns prior to Pod Clock selected edge output.
92S16 External Start Input and Trigger Output		
External start input		1 external start input from P6460 and/or event lines 1–4. Edge-selectable. The pattern generator automatically starts when the external start signal is asserted after the module has been armed by pressing the START key.
External start input minimum pulse width		15 ns
Trigger Output		1 trigger output available for both SMB connector and one of the general-purpose event lines 3–10, or high-speed event lines 5–8. SMB connector: TTL-level output 5 STD TTL Fan-out TTL high level occurs on the trigger output connector (SMB connector) on the card for 1 clock cycle when the pattern generator executes the trigger instruction.
Trigger Output Timing		
Relative to pod clock output		–55 ns Trigger signal occurs 55 ns prior to the selected rising/falling edge of the pod clock output when no delay is programmed.
Relative to External Clock Input		55 ns Trigger signal occurs 55 ns after the rising/falling edge selected of the external clock.

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P6463A Pattern Generation Probe

The following tables list the specifications for the P6463A Pattern Generator module:

- Table 1–15 P6463A Environmental
- Table 1–16 P6463A Mechanical
- Table 1–17 P6463A Electrical

Table 1–15: P6463A Environmental

Characteristic	Description
Temperature	
Operating	0° C to +50° C
Storage	–55° C to +75° C
Humidity	10% to 95% relative humidity (maximum)
Altitude	
Operating	4.5 km (15,000 ft.) maximum
Storage	15 km (50,000 ft.) maximum

Table 1–16: P6463A Mechanical

Characteristic	Description
Probe Housing Dimensions	Length = 15 cm, (6.0 in) Width = 10 cm, (3.9 in) Height = 3.8 cm, (1.5 in)
Cable Dimensions	2 meters (80 inches)

Table 1–17: P6463A Electrical

Characteristic	Performance Requirements	Supplemental Information
Clock		
Clock (Maximum Frequency)	50 MHz (20 ns)	
User Power		240 mA @ 5.0 V (28 mA @ 25 MHz & V_{cc} =7 V for 74HCT126)

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Table 1–17: P6463A Electrical (Cont.)

Characteristic	Performance Requirements	Supplemental Information
Output Signals		V_{cc} = 4.75 V R_{term} = 0 Ω
V_H	2.7 V minimum (using 74F126)	6.5 V @ V_{cc} = 7 V using 74HCT126 drivers
V_L	0.5 V maximum (using 74F126)	0.5 V @ V_{cc} = 7 V using 74HCT126 drivers
Clock Period Minimum Period		20 ns (50 MHz) in 9-channel mode or 40 ns (25 MHz) in 16-channel mode.
Data Minimum Period		40 ns (25 MHz) in 9-channel mode or 80 ns (12.5 MHz) in 16-channel mode.
Data and clock drive capability	48 mA sink, 12 mA source (at 10 MHz using 74F126)	24 mA sink/source for 74HCT126 @ 25 MHz Maximum capacitive load: 50 pF
Transition time (resistive load)		3.5 ns maximum (20% to 80%) (6 ns with 74HCT126)
Internal inhibit delay (inhibit in to signal out)		30.0 ns ±6.5 ns (enable/disable) (35 ns ±9 ns for 74HCT126)
External inhibit delay (TP250 in to signal out)		14.0 ns ±4.0 ns (enable/disable) (19 ns ±7 ns for 74HCT126)

P6460 External Control Probe

Table 1–18 list the electrical specification for the P6460 External Control Probe.

Table 1–18: P6460 Electrical

Characteristic	Description
User's Ground Sense	< 100 Ω to user's ground
Input Impedance	1 MΩ ± 1%, 5 pF nominal; leadset adds approx. 5 pF
Max. Non-Destructive Input Voltage Range	± 40 V (DC + peak AC)
Max. Voltage Between Any Two Inputs	±60 V (DC + peak AC)
Operating Input Voltage Range	From –40 V to input threshold's voltage + 10 V
Threshold Offset and Accuracy	±0.25% of threshold ±50 mV
Minimum Input Swing	0.5 V peak-to-peak, centered on the threshold
Minimum Pulse Width (with input 250 mV over the threshold from +0.5 V and –0.5 V)	4 ns at threshold

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Operating Information

This chapter tells you how to install and operate the TLA 510 and 520 logic analyzer. You should review the installation section after performing maintenance.

Installation

This section provides information on installing the system unit, terminal, and software. The basic steps to installing your logic analyzer consist of the following:

- Determine the best locations for the system unit and the terminal (refer to *Site Considerations*)
- Connect the power cords to the system unit and terminal; connect the power cords to the appropriate power source
- Connect the terminal to the system unit (refer to *System Unit Connections*)
- Connect the probes to the rear of the system unit
- Connect the probes to the system-under-test

The rest of this section provides more detailed information on installing your TLA 510 and 520 logic analyzer.

Site Considerations

Information provided here describes the environment in which the logic analyzer should be operated; the intended site must meet the stated conditions.

The system unit is intended for use in a normal environment. The system unit will operate in a temperature environment between +10° C and +40° C (+50° F and +104° F). The system unit's maximum heat dissipation is 2400 BTUs per hour. The terminal's maximum heat dissipation is 613 BTUs per hour.

When the logic analyzer is to be operated on a bench or cart, it should be placed in a normal, upright position. For proper cooling, allow at least eight inches (20.4 cm) of clearance on all sides of the system unit. The terminal may be placed on top of the system unit.

If you place the system unit on its side, place it on its side with the media drives down. Support the system unit so it will not tip over. Use a commercially available PC-cradle (saddle) to support the system unit.

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CAUTION. *To prevent damage from overheating, do not place the system unit on its side with the media drives towards the top.*

System Unit Connections

After determining where to install the logic analyzer, you are ready to connect the system unit to the power source, to the terminal, or optionally to a host computer network.

The acquisition and pattern generation probes attach to the logic analyzer through openings in the back panel. For detailed information using and connecting the acquisition probes, refer to the *92A96 & 92C96 Module User Manual*. For information on connecting the pattern generation probes refer to either the *92S16/32 Module User Manual* or to the *P6463A Pattern Generation Probe Instruction Manual*.

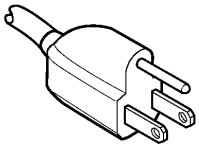
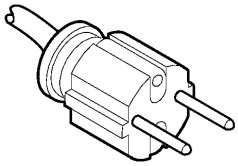
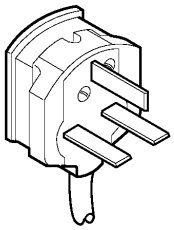
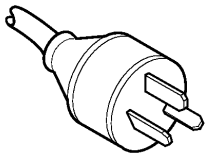
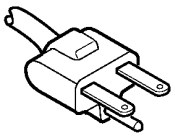
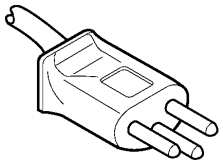
The power cord attaches to the system unit through a power-cord connector on the rear panel. The standard power cord for the system unit is rated for 115 V operation. Optional power cords are rated for 230 V operation. Refer to Table 2–1 for more information on power cords.

A different fuse is required for 230 V operation than for 115 V operation. Before connecting the power cord, ensure that the correct fuse is installed. Refer to *Selecting the Line Voltage and Replacing the Line Fuse* on page 6–5 for information on replacing the fuse.

Connect the proper power cord to the system unit and terminal. The two power cords are interchangeable. Connect both power cords to an appropriate power source. Table 2–1 shows the standard power cord and optional power cords that are available for the TLA 510 and 520. Use the cord that is proper for your site.

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Table 2–1: Power Cord Identification

Plug Configuration	Normal Usage	Option Number
	North America 115 V	Standard
	Europe 230 V	A1
	United Kingdom 230 V	A2
	Australia 230 V	A3
	North America 230 V	A4
	Switzerland 230 V	A5

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Terminal Connections

The terminal connects to the system unit with an RS-232 serial cable (provided as a standard accessory) and a Thinnet Ethernet cable. Figure 2–1 shows the connections for the 9204XT terminal (an earlier version of the 14-inch terminal). Figure 2–2 shows the connections for the 17-inch 9205XT terminal. The 9204XT and 9205XT terminals have been replaced by the 9206XT terminals.

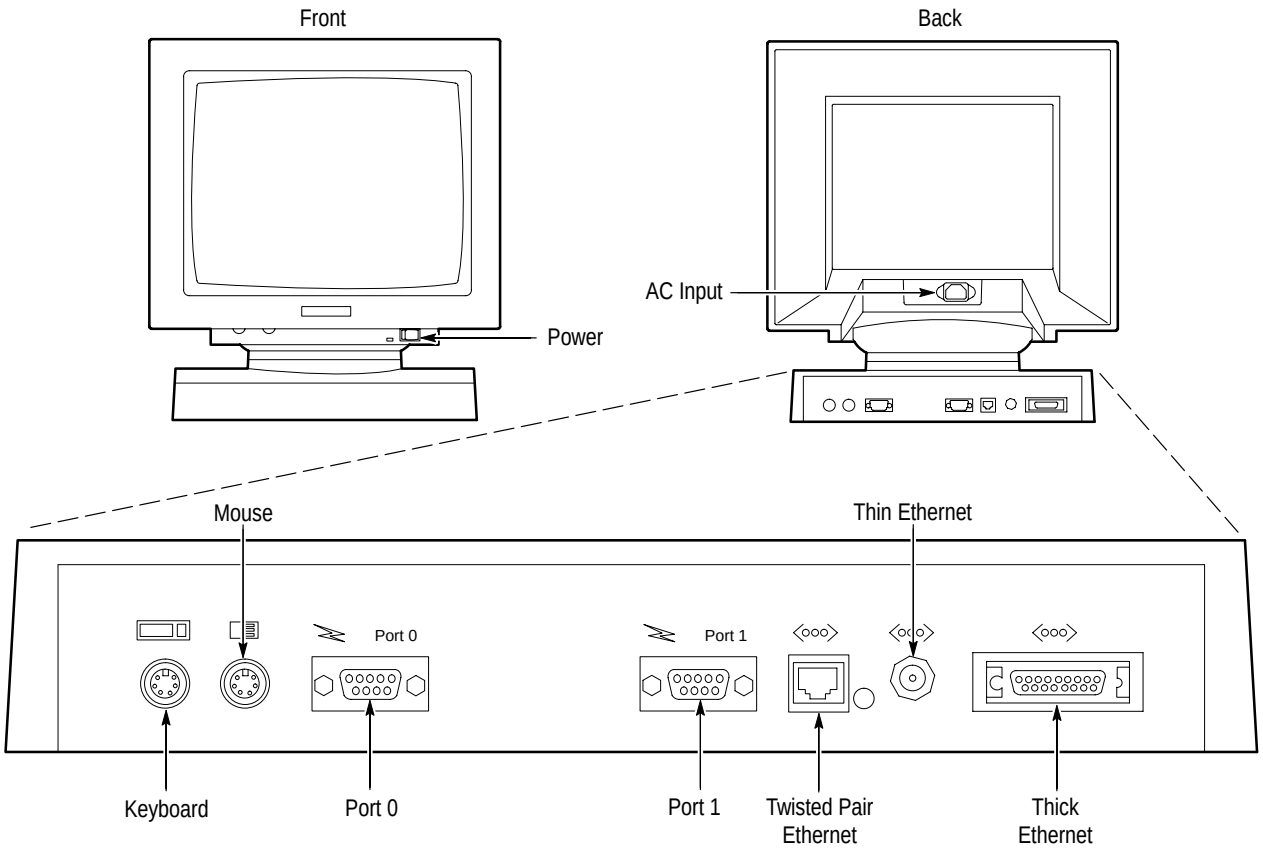


Figure 2–1: 9204XT Terminal Connections

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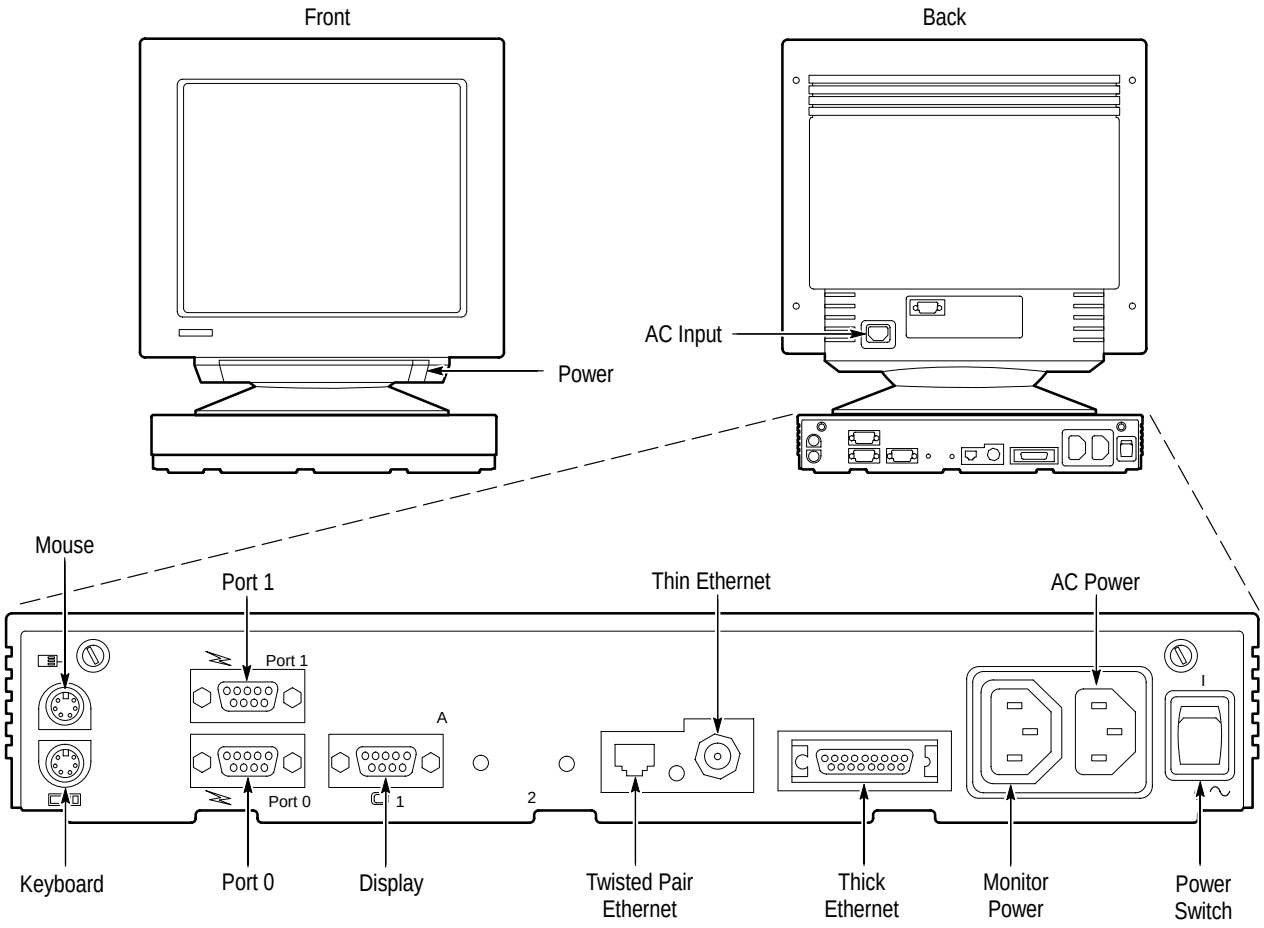


Figure 2–2: 9205XT Terminal Connections

Figure 2–3 shows the connections to the rear of the logic module of the 9206XT terminals. The 9206XT comes standard with a 15-inch monitor and can be ordered with an optional 17-inch monitor. The logic unit is powered by an external power supply. The connection scheme is similar for both versions of 9206XT terminals.

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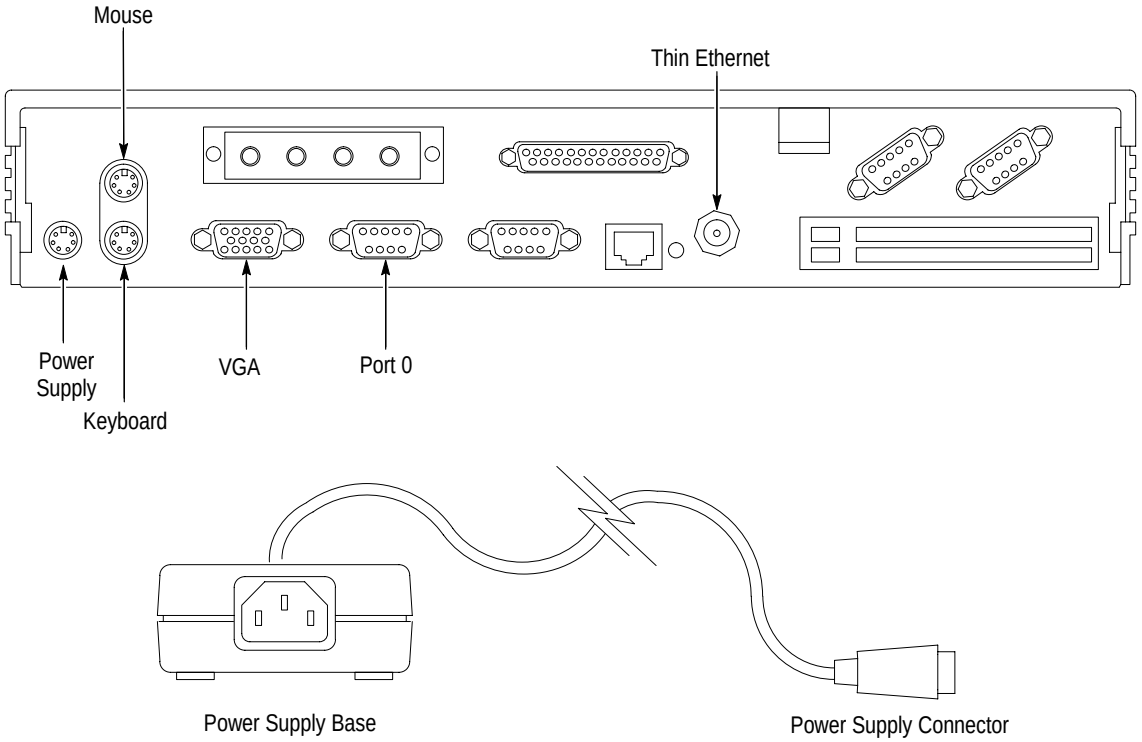


Figure 2–3: 9206XT Logic Module Connections and Power Supply

The connection procedures for the all the terminals are similar. Refer to either the terminal installation manual that came with the terminal or to the previous connection illustrations while performing the following procedures:

1. Connect the RS-232 serial cable from the Terminal Port 0 to the Terminal port on the system unit.
2. Connect a BNC-T connector to the Thin Ethernet BNC connector on the logic module (or on the terminal). Connect a second BNC-T connector to the BNC connector on the back of the system unit.
3. Connect a 50 Ω terminator to one side of the BNC-T connector on the logic module (or terminal) and connect another terminator to the BNC-T connector on the system unit.
4. Connect the 50 Ω BNC cable from the unused side of the BNC-T connector on the logic module (terminal) to the unused side of the BNC-T connector on the system unit.
5. Connect the keyboard and the mouse to the logic module.
6. Connect the monitor cable from the monitor to the logic module.
7. Connect the power cord (or power supply) to the logic module.

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8. Connect the power cord to the monitor.

9. Power on the monitor and the logic module. Wait for the serial window to appear and then power on the system unit.

The terminal should be set for the correct settings to communicate with the system unit when it is shipped from the factory. After powering on the terminal and the system unit, the terminal will display its Boot Monitor. Table 2–2 lists the terminal's default boot parameters. If the terminal does not boot properly, you should check the boot parameters against those in the table.

Table 2–2: Terminal Default Boot Parameters

Parameter	Default Value	Parameter	Default Value
IADDR	10.0.0.2	DNODE	0.0
IHOST	10.0.0.1	BMETHOD	ROM
IMASK	255.0.0.0	BDISPLAY	DISABLED
IGATE	0.0.0.0	BAFROM	NVRAM
BPATH*	/XP300/os		

*** On initial power on, the default value is /XP300/os and then changes to os.**

The terminal should display a series of messages in the Boot Monitor. When the boot process is complete, the serial window will be displayed with the word "Connected." The serial window should then display the file system check messages as the system completes its boot process. After a few moments, the logic analyzer display appears.

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Host Computer or Serial Printer Connections

You can connect the logic analyzer to a host computer or to a serial printer with a serial cable. Connect the serial cable to either the Host or Auxiliary 9-pin DCE ports on the rear of the system unit. If the host computer has a 9-pin DTE male connector, connect straight through using a 9-wire cable with a 9-pin female connector on one end and a 9-pin male connector on the other end. If your host computer or serial printer has a 25-pin male connector, use an 9-wire cable with connectors wired as shown in Table 2–3. Table 2–3 also describes the wiring of the optional 9204XT terminal's serial port cable.

Table 2–3: 9-pin DCE-to-25-Pin DTE Cable Connections

Port Signal Name	9-Pin Male Connector (System Unit End)	Terminal Connector
Protective Ground (Shield)	(Shield)	(Shield)
Carrier Detect	Pin 1	Pin 1
Receive Data	Pin 2	Pin 2
Transmit Data	Pin 3	Pin 3
Data Terminal Ready	Pin 4	Pin 4
Signal Ground	Pin 5	Pin 5
Data Set Ready	Pin 6*	No Connection
Request To Send	Pin 7	Pin 7
Clear To Send	Pin 8	Pin 8

* **Pin 6 is pulled up to +5 V**

If your host computer or printer has a 25-pin DCE female connector, you must provide a cable wired as listed in Table 2–4.

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Table 2–4: 9-pin DCE-to-25-Pin DCE Cable Connections

Port Signal Name	9-Pin Male Connector (System Unit End)	25-Pin Male Connector
Protective Ground (Shield)	(Shield)	Pin 1
Carrier Detect	Pin 1	Pin 4
Receive Data	Pin 2	Pin 2
Transmit Data	Pin 3	Pin 3
Data Terminal Ready	Pin 4	Pin 5
Signal Ground	Pin 5	Pin 7
Data Set Ready	Pin 6*	Pin 6
Request To Send	Pin 7	Pin 8
Clear To Send	Pin 8	Pin 20

*** Pin 6 is pulled up to +5 V**

The serial printer connects to the logic analyzer's Auxiliary port; the port connector is accessible on the rear panel. When printing to a serial printer the Auxiliary Port output data format consists of 8–bits/character, No parity and one stop bit. For specific information on using a printer with specific modules, refer to the appropriate module user manual.

The baud rate and flow control are selectable in the Communications menu. For information on how to set the Baud rate DIP switches, refer to *Terminal, Host, and Auxiliary Port Baud Rate Selections*.

When printing to a serial printer, ensure that your printer's communication settings match those of the Auxiliary port. For specific instructions on the use and care of your printer, refer to its supporting documentation.

Output data is transmitted on pin 2 of the Auxiliary port connector and is received on pin 3. For recommended cable connections to either DTE or DCE type serial printer ports, refer to Tables 2–3 and 2–4 of this chapter.

Terminal, Host, and Auxiliary Port Baud Rate Selections

There are two different ways that you can select the baud rates for the Terminal, Host, and Auxiliary Ports on the logic analyzer. The easiest way is to set the baud rates in the Communications menu .

Communications Menu. You can set the baud rates for the Terminal port, Auxiliary port, and the Host port through the Communications Menu as shown in Figure 2–4. The default baud rate for the Terminal port is 38400; the default baud rate for the other ports is 9600. The last selected rate is always stored in

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nonvolatile RAM and can also be selected by using the DIP switches on the Controller board (accessible through slot 1 on the rear panel).

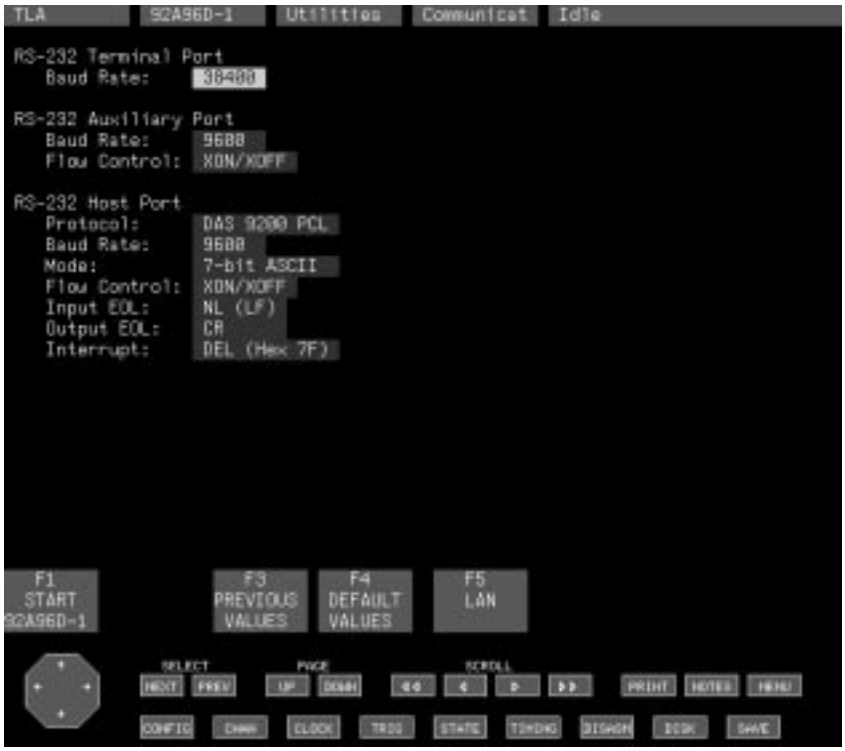


Figure 2–4: Communications Menu

DIP Switches. You can also override the selections in the Communications menu using the DIP switches mounted on the Controller board. You can access these switches through an opening on the system unit's rear panel shown in Figure 2–5.

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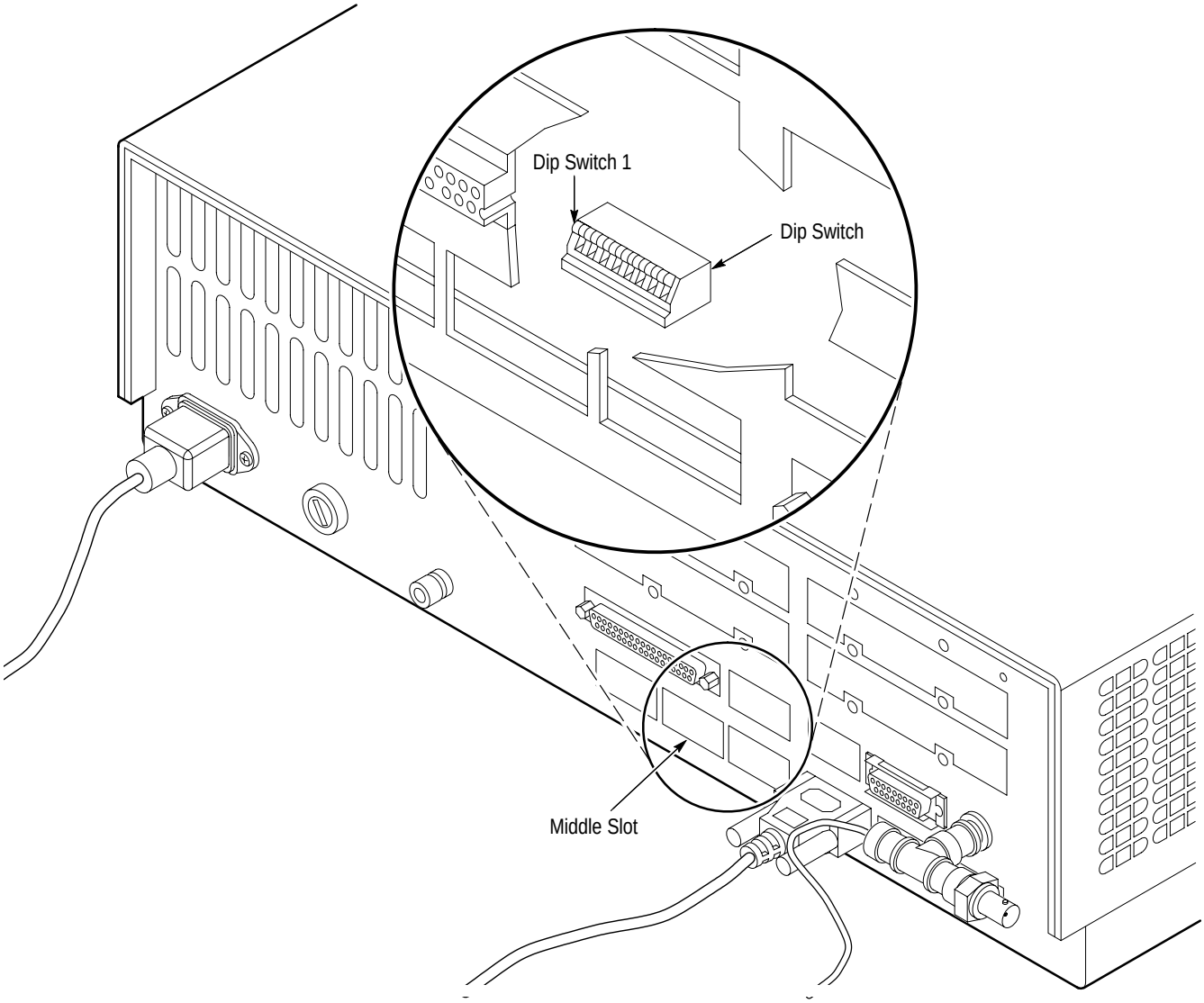


Figure 2–5: DIP Switch Location

DIP switch pairs 3 and 4, 5 and 6, and 7 and 8 select the baud rates for the RS-232 ports as listed in Table 2–5. DIP switch 1 is the left-most switch as you face the rear of the system unit. The operation of DIP switches 1 and 2 is described later in this manual.

For example, if you set DIP switches 7 and 8 both in the up position, the baud rate for the Auxiliary Port (serial printer port) will always power-on to a default baud rate of 9600. You can use the other switch settings to provide alternative baud rate settings. The restore parameters settings shown in Table 2–5 cause the three ports to power-on with the baud rates specified in the Communications menu.

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It is recommended that you operate your logic analyzer with all DIP switches in the up (or open) position.

Table 2–5: Baud Rate DIP Switches

Switch Use	Setting (Up=Open, Down=Closed)	Result of Setting
Boot Control (Switches 1 & 2)	Up / Up	Normal system boot
	Down / Up	BOOT?> prompt
	Up / Down	Not used
	Down / Down	Loop on level 0 diagnostics
Terminal Port (Switches 3 & 4)	Up / Up	38400 baud (default)
	Up / Down	2400 baud
	Down / Up	1200 baud
	Down / Down	Restore Parameters
Host Port (Switches 5 & 6)	Up / Up	9600 baud (default)
	Up / Down	2400 baud
	Down / Up	1200 baud
	Down / Down	Restore Parameters
Auxiliary Port (Switches 7 & 8)	Up / Up	9600 baud (default)
	Up / Down	2400 baud
	Down / Up	1200 baud
	Down / Down	Restore Parameters

Software Installation

The logic analyzer comes with the system software already installed and ready to use. If you order your logic analyzer with any application software products (such as one of the microprocessor disassembler products), you must install the software on the hard disk before using it. Refer to the application's user manual for information on installing the application software.

A copy of the back-up system software is available on floppy disks. For information on installing or reinstalling the system software, *Loading System Software* on page 6–67.

There may be occasions when you must set some of the software configuration requirements to communicate with the terminal. Details on setting the communication requirements are also provided in *Maintenance.*

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Operating Information

The logic analyzer uses a common system unit for the TLA 510 and TLA 520 logic analyzer; the main difference is that the TLA 510 logic analyzer comes standard with 100 channels of acquisition while the TLA 520 logic analyzer comes with 200 channels of acquisition.

The logic analyzer uses the 92C96 Data Acquisition Module to acquire data. The TLA 510 logic analyzer can also be ordered with the 92S16 Pattern Generation Module that provides 16 channels of pattern generation. The term Module refers to either the acquisition or pattern generation unit in the logic analyzer and is used throughout this document.

Figure 2–6 shows a front view of the system unit. The ON/STANDBY switch and the floppy disk drive are located at the front of the instrument as shown. An LED located in the lower right corner on the front of the system unit illuminates when the hard disk is being accessed.

The ON/STANDBY switch illuminates when the system is powered on. The switch is located in the lower-left corner on the front of the instrument. When in the STANDBY position, the DC voltages are removed from the circuitry; however, AC voltages still exist inside the instrument. The switch is illuminated when the system unit is powered on. To remove AC voltages from the system unit, you must remove the power cord.

The ON/STANDBY switch, not the power cord, should be used for powering the system unit on and off. Since the power-off sequence is logic-controlled, you will notice a slight delay before DC power is removed from the system unit. During a normal power-off sequence, the instrument saves information on the type of shutdown occurring and saves the current state of the file system.

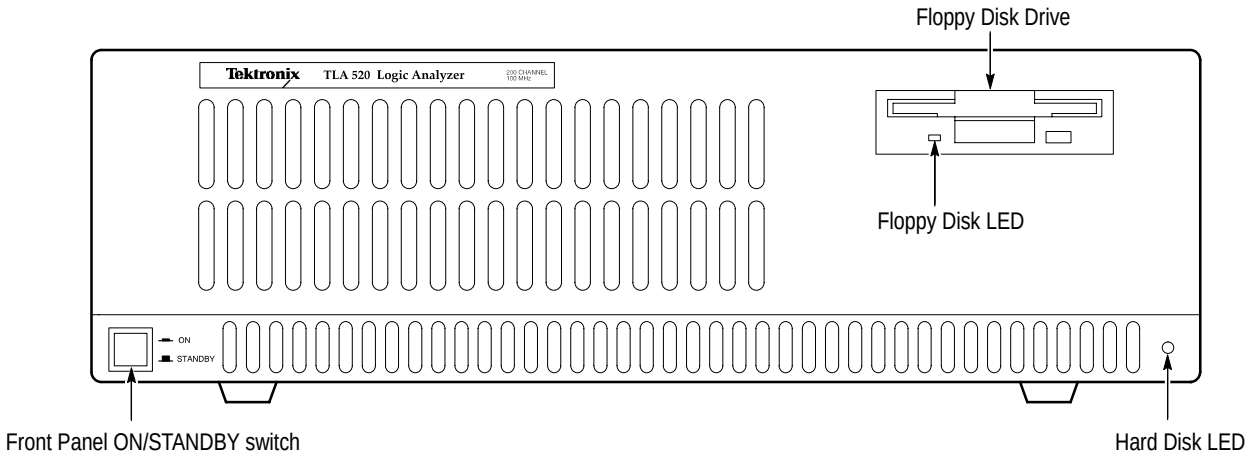


Figure 2–6: Front View of the System Unit in the Normal Upright Position

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Figure 2–7 shows a rear view of the system unit with probes connected to the acquisition module. The acquisition module provides connections for up to four probe assemblies. A probe power connection provides power for certain microprocessor probe assemblies that need power. A Sync-out connector lets you connect a triggering signal from the module to an external device, such as an oscilloscope or back to the system under test.

Figure 2–8 shows the rear view of the system unit with its external connectors. Three 9-pin RS-232 ports provide connections to a terminal, auxiliary (printer) and host computer. The 37-pin female D-connector allows you to monitor or drive external devices with the optional 92PORT application software.

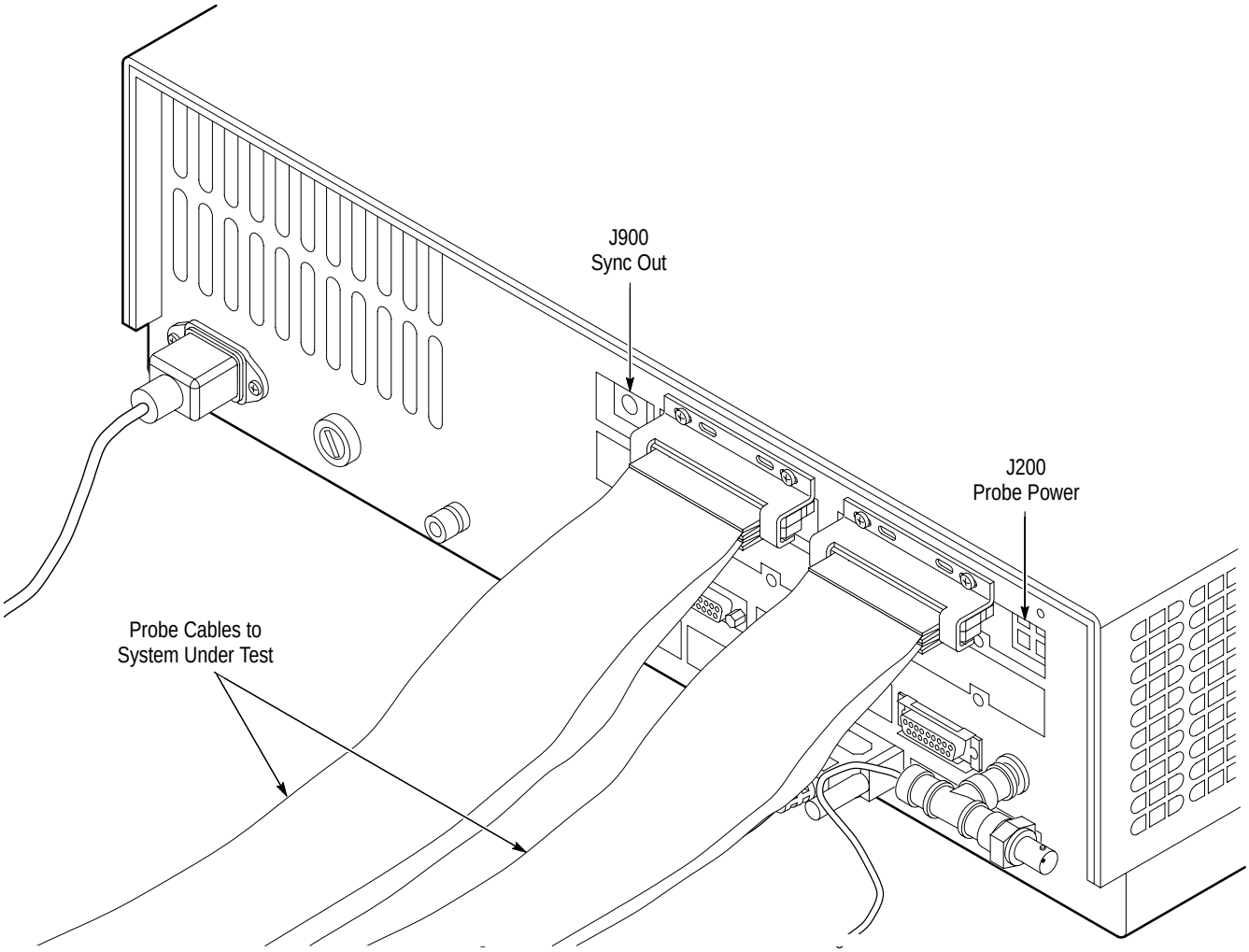


Figure 2–7: Rear View of the System Unit with Probes Attached

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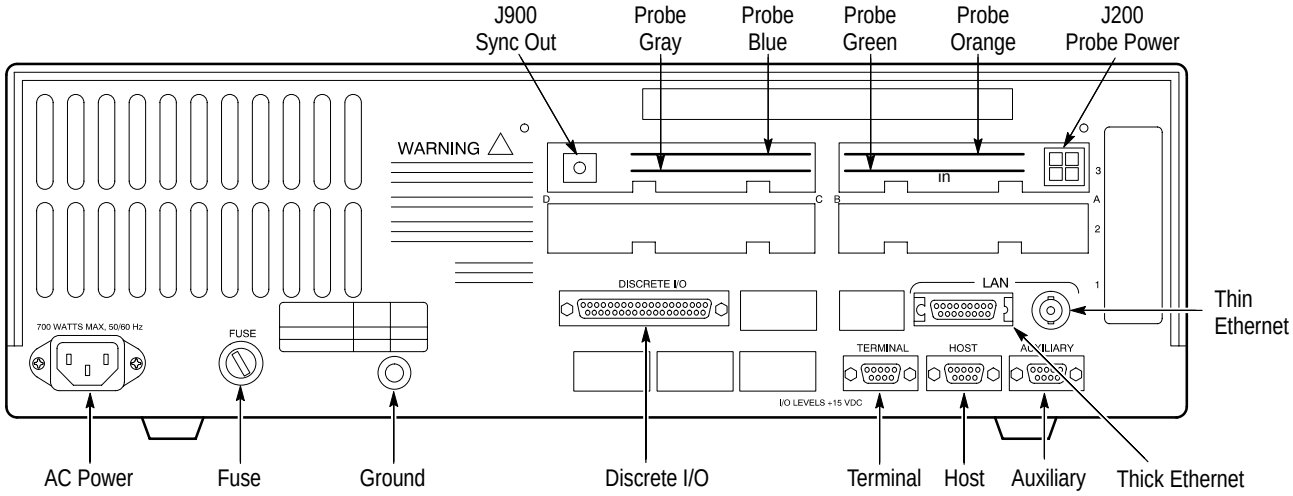


Figure 2–8: Rear View of the System Unit with External Connectors

Powering On and Powering Off

To normally power on the logic analyzer, power on the terminal and wait for it to complete its power on sequence, indicated by the word “connected”. Then, power on the system unit. The terminal goes through its power-on tests before the logic analyzer performs its checks. When all power-on checks have been completed, the Menu Selection Overlay displays. Figure 2–9 shows an example of the Menu Selection overlay.

To power off the logic analyzer, simply push the ON/STANDBY switch on the system unit to STANDBY and then power off the terminal.

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Figure 2–9: Menu Selection Overlay

Diagnostics, File System Checks, and the Boot Option Overlay

If your logic analyzer has System Software Release 3, Version 1.60 and higher, you can bypass the power-on diagnostics and file system checks by changing the settings in the Boot Option overlay to the Diagnostics menu. The default settings are to execute diagnostics and the file system check each time you power on the logic analyzer. However, you can set up the logic analyzer to bypass the diagnostics and file system checks for up to 14 days or up to five power-on cycles, which ever occurs first. You can also set the logic analyzer to only run the file system check after an abnormal power down.

There are certain conditions that require the diagnostics or file system checks to be run. If these conditions occur, they override the selections made in the Boot Option overlay. The conditions required for running diagnostics include the following:

- A module failed at the last power on.
- The module configuration of the logic analzer has changed (you either removed or added a module to the logic analyzer).

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If an abnormal power down occurs, the logic analyzer will always run the file system check, regardless of the settings in the Boot Option overlay.

Information under the BOOT ACTIVITY area in the Boot Option overlay summarizes the most recent diagnostics and file system check activity. It lists the last time that the diagnostics were checked and the last time the files system was checked.

***NOTE**. If you run the File System Check procedure from the floppy disks, the logic analyzer will ignore the settings in the Boot Option overlay.*

These features let the user power on the logic analyzer quickly without having to wait for the power-on diagnostics or file system checks. Refer to the discussion of the Boot Option overlay in the user manual for more information on setting the boot options.

Menu Overview

The logic analyzer is controlled by interactive menus that display on the terminal. A menu is a screen display that offers selectable or scrollable choices. Some menus associated with overlays (submenus) that provide additional menu selections or information.

The menu set can be divided into four separate groups:

- Setup menus
- Display menus
- Utility menus
- Application menus

Setup Menus

Setup menus define the conditions under which modules will operate and communicate with other modules.

There are two classes of Setup menus: those that control system-wide operating parameters and those that pertain specifically to one module type.

System Setup Menus. These menus will always appear on the Menu Selection overlay (the Cluster Setup can only be entered after you define a cluster using the System Config menu). The System Configuration, Cluster Setup, and System Monitor menus are described in more detail in the Reference section of this manual.

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The following System Setup menus are available:

- System Configuration Menu. This menu lists the modules installed in the logic analyzer. At initial power-on, the default groupings of modules are displayed; you can select different module formations (groups of modules of the same type). A typical example of when you might want to change a module formation is when your application requires more channels in a module than currently defined.

  The System Configuration menu also displays the current collection of modules in a cluster; you can change the clusters with the Cluster Definition overlay.

- System Monitor Menu. This menu displays the status of the modules as well as the clusters. This menu lets you see at a glance which modules and clusters are running, which are waiting for their trigger condition, which have acquired data and stopped, and how the autorunning has restarted. If you acquire data for the selected module or cluster using Autorun, the number of times that module or cluster has been started is shown in the upper-right corner of the status line.

  The System Monitor menu is especially valuable when you have defined more than one cluster and have them running simultaneously.

- Cluster Setup Menu. This menu is only selectable after you create a cluster using the System Configuration menu. This menu lets you define how modules assigned to the same cluster interact. Specifically, it allows you to define signals passed between modules, time-correlate data acquired by two different modules, and specify Autorun conditions where a module acquires data, compares it to a reference memory file, and based upon the comparison, stops or automatically repeats the acquisition.

Module Setup Menus. Module Setup menus that appear below the System Setup menus correspond specifically to the module currently selected. For example, if 92C96-1 is the active module, the Config, Channel, Clock, Trigger, and Monitor menus pertain only to this one module; other Setup menus will appear when you select a different module (for example, 92S16-1). Refer to the *510 & 520 User Manual* and the module user manual for complete details on all the menus, overlays, and fields of the Module Setup menus.

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Figure 2–10 shows the Setup menus for each module.

MODULE	SETUP
92C96	System Configuration Cluster Setup* System Monitor Configuration Clock Channel Trigger Monitor
92S16	System Configuration Cluster Setup* System Monitor Configuration Channel Program Monitor

* All modules in a cluster share a Cluster Setup menu.
Modules not in a cluster have no Cluster Setup menu.

Figure 2–10: Setup Menus

The following Setup menus are available for the acquisition module:

- Configuration (Config) Menu. This menu allows you to select the software support mode, default memory size, and whether or not you want to capture signal glitches. This menu shows you the name and type of module, including the number of acquisition channels, and indicates the number of intermodule signals you have defined.
- Channel Menu. This menu allows you to create channel groups and define their names, radix, and order. You can also assign the individual channel names and define their polarities and threshold voltages.
- Clock Menu. This menu lets you select the sample clock source and the internal clock period or the external clock equations and qualifiers. You can choose microprocessor-specific options if you have a microprocessor support package installed on the hard disk and selected in the Configuration menu.
- Trigger Menu. This menu lets you define the trigger position, trigger specification program-including states, events, and actions. You can also define the type of storage qualification you want. You can use trigger libraries that contain templates for trigger specification programs or create your own trigger libraries.

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- Monitor Menu. This menu monitors the progress of the acquisition. The menu displays if an acquisition is not completed within a few seconds. You can use the Monitor menu to debug trigger specification programs by monitoring the status of the acquisition, counter or timer values, and the amount of acquisition memory being used.

The following Setup menus are available for the pattern generation module:

- Configuration Menu. This menu shows the current hardware configuration and software mode for the pattern generation module.
- Channel Menu. This menu lets you collect channels into logical groups for data entry and display purposes. You can change the names, radix, and display order of each group.
- Program Menu. This menu allows you to enter data and instructions to stimulate the circuit or system under test. You can also send a signal to the acquisition module.
- Monitor Menu. This menu lets you debug pattern generation programs by watching pattern-generator/circuit under test interactions at a reduced clock rate. You can set breakpoints in the pattern generation programs and single-step through problem areas.

Display Menus

Display menus control the display format and viewing characteristics of acquired data. Display menus are module-dependent (see Figure 2–11). Module display menus are described in detail in the module user manuals.

MODULE	Display
92C96	State Timing Graph Disassembly
92S16	(no Display menus)

Figure 2–11: Module Display Menus

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The following Display menus are available for the acquisition module (there are no display menus for the pattern generation module):

- State Menu. This menu displays acquired data as a table of logical states of the input channels. Channels are organized as defined in the Channel menu and data is displayed in the radix you select.
- Timing Menu. This menu provides a graphic display with each input channel represented as a digital (two-state) waveform. It also shows the bus value of all channel groups defined in the channel menu.
- Graph Menu. This menu displays a graph of data from any two of the selected channel groups plotted against their locations in the acquisition memory.
- Disassembly Menu. This menu is a table display that translates the logic input for specific channel groups into microprocessor-specific mnemonics..

Utility Menus

Utility menus provide system-level tools. They allow you to control data transfers to and from the hard and floppy disks, and allow you to define the parameters that control the communication ports.

The following Utility menus are available:

- Save/Restore Menu. This menu allows you to save setups and acquisition memory data, restore setups from previously saved files, and delete setup and reference memory files from the hard disk.
- Disk Services Menu. This set of menus provides the tools necessary to duplicate floppy disks, format and verify floppy disks, backup and restore user files with floppy disks, and copy or delete specific files. A directory of all user file names on floppy or hard disks is provided; accompanying information specifies the size of the file, creation or revision date of the file.
- Symbol Editor Menu. This menu allows you to create and edit symbol tables that you can use to specify trigger word patterns and evaluate acquired data. You can create and edit either range or pattern type symbol tables.
- Communications Menu. This menu specifies RS-232 port settings and view LAN network settings. You can specify baud rates and flow control for each RS-232 port.
- Diagnostics Menu. This menu provides a list of major system components, a diagnostic report indicating operational status at power-on, a summary and brief description of the modules installed in the logic analyzer, the system software version, date and time, and some general user instructions.
- Version Menu. This menu displays the version numbers of all installed modules, the system software, and all installed application software.

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Application Menus

Application menus control the operation of application software packages. Most software supporting the application packages resides on floppy disks and must be loaded onto the system hard disk before being used. All nonresident application software and corresponding menus are described in separate manuals supporting each application software package.

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Theory of Operation

This section describes the general functions of the circuitry on major components. System components include the system units, acquisition and pattern generation modules, probes, and terminal. This manual does not discuss the circuit functions of the terminal. (The terminal service manuals are not part of the documentation package; contact your local Tektronix representative for ordering information.)

System Unit

The mechanical chassis houses all system unit components and options. A card cage within this chassis holds modules. The probes connect to the modules in the rear of the chassis. The major system unit components consist of the following:

- Backplane board
- Controller board
- 92LANSE board
- Hard and Floppy Disk Drives
- Power Supply

These components communicate with each other and with any installed modules by way of the backplane and system unit cables. Refer to Figure 3–1 for a cable diagram of the TLA 510 and TLA 520.

Backplane Board

This board provides the mechanical and electrical connection between the Controller board, and slots that accept logic analyzer modules. The backplane provides the bus structures for inter-system unit communications. The modules access the buses within a system unit by way of two 540-pin connector slots mounted on the backplane. The four basic bus structures on the backplane are:

- Control bus
- Instrument bus
- Application bus
- Power-supply bus

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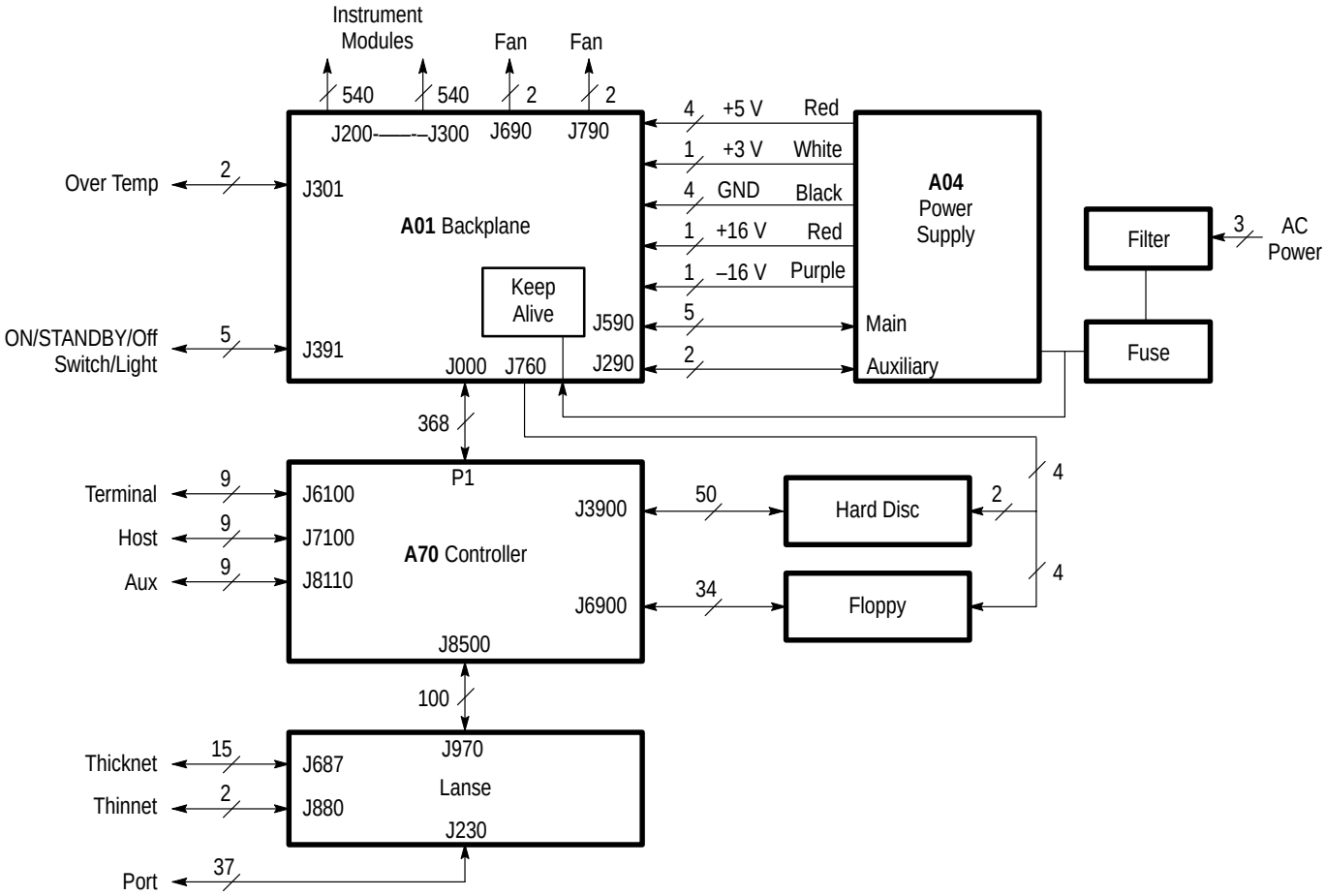


Figure 3–1: System Unit Cable Diagram

Control Bus. The Control bus provides buffered address, data, and control lines for the Logic Analyzer. These lines support the transfer of data, setup, and status information between the Controller board and other system unit components. This information is not used during real-time interactions with the device-under-test. The primary functions of the Control bus are as follows:

- Provide setup information to the modules
- Provide test vectors to pattern generation modules
- Retrieve data from acquisition modules
- Retrieve status information from modules

The Control bus is asynchronous, allowing a wide range of module responses.

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Instrument Bus. The Instrument bus consists of three buses: the Event bus, Time Base bus, and Correlation bus.

The Event bus allows modules to pass real-time, low-speed events (≥40 ns) between each other at TTL levels. Sixteen general-purpose event lines allow Boolean combinations of events between modules, including sequential arms, trigger, qualification, and start/stop functions. A differential ECL signal (TSYNC) is a synchronizing clock used to clock events on and off the Instrument bus. TSYNC runs at periods of 40 ns.

The Time Base bus provides four programmable time bases for asynchronous acquisition and timestamp (for time correlation). The four time bases are programmable by the Controller from 1 ms to 20 ns, plus 40 ns, in increments of 1, 2, and 5.

The Correlation bus passes signals needed for time alignment of data from acquisition modules. The data may have been acquired at different rates. There are eight correlation signal lines available on the backplane. The maximum clock rate is 25 MHz; all correlation signals are open-collector TTL. For a complete description of correlation, refer to the user manual for the specific module.

Application Bus. The Application bus consists of differential pairs of ECL signal lines. It provides fast communication (250 MHz or 800 picosecond edge speeds) between modules in adjacent slots. For a complete description of the Application Buss, refer to the user manual for the specific module.

Power-Supply Bus. The Power-supply bus distributes voltages to all instrument slots on the backplane; other system unit components receive power through cabling (see Figure 3–1). This bus also carries power-control signals between the Controller board and the power supply.

Controller Board

The Controller board consists of several interrelated circuits that provide the logic analyzer with computing resources and the means for setting up hardware for the system unit and its modules.

Controller. Figure 3–2 contains circuit blocks with alphabetical indexes to the following descriptions for the Controller board.

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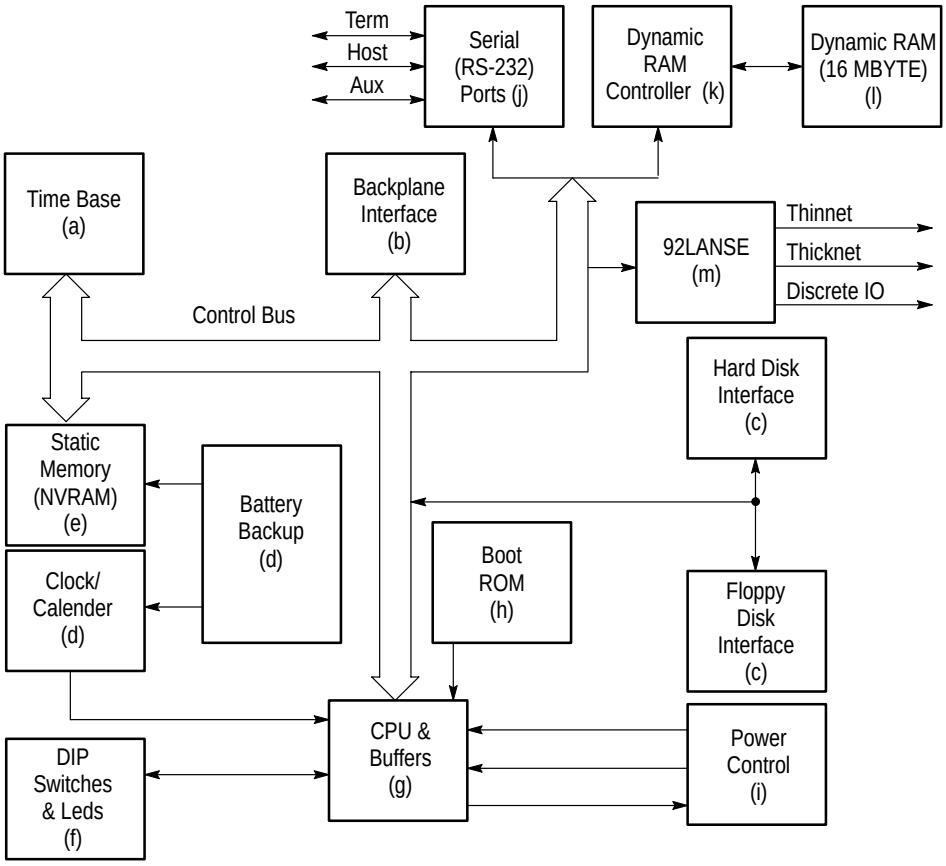


Figure 3–2: Controller Board Block Diagram

(a) Four asynchronous ECL TIME BASES reside on (and are programmed by) the Controller board. Asynchronous acquisitions and timestamp operations use these time bases. For more information on the time bases, refer to *Instrument Bus* in this chapter.

(b) The BACKPLANE INTERFACE provides the connection for address, data, and control lines between the controller's CPU and the module slots.

(c) The SCSI HARD DISK INTERFACE and the FLOPPY DISK INTERFACE link the control lines from the CPU to the hard and floppy disk drives. The floppy disk interface uses a CACHE MEMORY; this is a high-speed intermediate buffer that talks directly to the CPU using the Control bus. The SCSI interface uses DMA to access memory directly.

(d) The Controller board contains a single part that contains BATTERY BACKUP, CLOCK/CALENDAR, and STATIC MEMORY (NVRAM). The battery powers the other features when the system unit loses power (such as when you power off the system unit or disconnect the power cord).

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(e) The STATIC MEMORY contains approximately 32 Kbytes of nonvolatile RAM for storing interrupt routine addresses, previous shutdown conditions, and pointers to other processes.

(f) LEDs monitor the state of the power supplies and activity of the CPU during level 0 power-on diagnostics. DIP SWITCHES override the baud rates (set in the Communications menu) for the RS-232 ports. Refer to *Troubleshooting* on page 6–27 for more information on the LEDs and DIP switches.

(g) The CPU is a 68EC030 microprocessor operating at 40 MHz; it uses an asynchronous bus structure and decoding circuitry to transfer 32 address bits and 32 data bits. The BUFFERS link the address, data, and control lines from the CPU to outside circuitry. These buffers can be tri-stated when other controllers (for example, a DMA controller) use these lines.

(h) The BOOT ROM contains 64 Kbytes of ROM space used to store power-on sequences and level 0 diagnostic.

(i) POWER CONTROL issues the TURNOFF request signal to the CPU for a normal power-off sequence (power switch OFF). The CPU performs file-management procedures and sends a SHUTDOWN signal to the power supply, causing the power supply to shut down.

If an unexpected power loss occurs (for example, power cord pulled), the power supply issues the POWER FAIL signal to the CPU. The CPU does not access the disk drives to store data. STATIC MEMORY stores the data. The next time you ON/STANDBY the system unit, the Previous Shutdown field in the ON/STANDBY menu contains the message “Power Failure” instead of “Normal”. Refer to *Troubleshooting* on page 6–27 for more information on the messages in the Previous Shutdown field.

(j) The SERIAL (RS-232) PORTS provide support for Terminal, Host, and Auxiliary communications.

(k) The DYNAMIC RAM CONTROLLER consists of RAM read/write accessing and refresh circuitry for the DYNAMIC RAM.

(l) The DYNAMIC RAM contains 16 Mbytes of storage. Most of the DYNAMIC RAM stores system software and post-processes acquired data. The upper quarter of DYNAMIC RAM temporarily stores configuration and data files to improve the system response time.

(m) The 92LANSE Module is an I/O adapter that connects directly to the Controller board. The module provides an Ethernet communication medium for host and terminal interfacing. The 92LANSE module also provides limited remote control and monitoring capabilities of the system under test.

You can ON/STANDBY or down the TLA 510 and TLA 520 using two pins on the Controller board (J5000 labeled REMOTE). The pins are at the rear of the

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Controller board and are accessible through the card cage. Shorting the pins together causes the system unit to ON/STANDBY. To power off, remove the short.

Also, you can press ON/STANDBY and power off your system unit and terminal using the terminal power button. To use this option, install a jumper wire between J6110-1 (labeled REM) and J8101-3 (labeled RTS) on the Controller board. When you turn on the terminal (with the system unit power switch in the STANDBY position), power applies to the system unit after the terminal power-on diagnostics complete. The jumper is not installed when the system unit is shipped.

***NOTE**. If the terminal fails its power-on diagnostics with the jumper wire installed, the terminal may not display information from the system unit.*

92LANSE Module

The 92LANSE Module consists of a circuit board with connections for Thicknet/ Thinnet cables, and software support for Transport Control Protocol and Internet Protocol (TCP/IP) with FTP (File Transfer Protocol). The module is compatible with networks complying with the IEEE 802.3 10BASE5 (Thicknet) and 10BASE2 (Thinnet) interface standards. The network type is selected with a 92LANSE board jumper block and cable availability.

TCP/IP networking protocols allow the 92LANSE Module to communicate with operating systems such as UNIX, DEC Ultrix-32, DEC VMS, and DOS. To transfer files to and from a Logic Analyzer, the host computer must have TCP/IP capability.

The 92LANSE FTP is a listening-only device, allowing the logic analyzer to respond only to commands issued from your host. You cannot issue commands from a logic analyzer to your host.

The 92LANSE Module's control/status register maintains independent control and status of the module's chip set. The chip set consists of an AM7990 Ethernet Controller, an AM7992B Serial Interface Adapter (SIA), and a Thinnet transceiver. The Ethernet controller uses an external memory buffer that also provides access to the Contoller's CPU to transfer data to and from the network.

Because the 92LANSE Module connects directly to the Controller board, the 92LANSE diagnostics run at the same time as the diagnostics for the Controller board. Diagnostic errors are reported as errors to Slot 0 in the Diagnostic menu. The Version menu reports the hardware version of the 92LANSE Module and the Controller board on the same line for Slot 0.

Jumper J790 (Heart Beat Enable jumper) enables the Heart Beat feature used during a Signal Quality Error (SQE) test as described by the IEEE 802.3 definition. The Heart Beat Enable is only effective when J685 (THICK/THIN) is in the "THIN" (2-3) position. The Heart Beat Enable jumper is shipped in the 1-2 position (enabled).

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The software supports FTP server functions as well as remote shell (rsh), remote copy (rcp), and the echo/echo-reply BSD UNIX ping functions of the ICMP (Internet Control Message Protocol).

92Port. The 92LANSE board provides the circuitry for the 92port software product. The Discrete I/O connector on the back panel of the system unit provides an interface with a device under test. For more information on 92port refer to *92port Instructions* manual.

Hard and Floppy Disk Drives

A media bracket assembly inside the system unit houses the hard disk and floppy disk drives. These drives interface with the Controller board by way of ribbon cables. Cables from the backplane board provide power to the drives. Refer to the Diagnostics Menu to see what size the hard disk is.

When you power off the system unit by pressing the ON/STANDBY switch, a power-off sequence completes file-management procedures and locks the head in the hard disk drive into a safe position.

Use the floppy disk drives for the following purposes:

- Loading application software from floppy disk
- Copying files for use on other system units
- Making and restoring backup files
- Storing instrument setups, reference data, and acquisition data from the modules

A light on the front of the 1.44 Mbyte floppy-disk drive indicates when the system unit is accessing a floppy disk. A light on the lower-right front of the system unit indicates the system unit is accessing the hard disk drive.

Power Supply

The power supply is located in a separate housing within the system unit. A series of wires attached to the backplane transfers power from the power supply to the modules and Controller Board. The system controller controls the power supply through a ribbon cable which attaches to the backplane. The media power cable supplies power from the backplane board to the hard and floppy disk drives. Power is supplied to the fan by way of a two-wire cable. The power supply provides:

- +3 V, +5 V and ±16 V supplies for the system unit (refer to Figure 3–1), and +12 V and +5 V for the hard and floppy disk drives.
- Power to the instrument modules plugged into each slot of the backplane. Each module has different power requirements.

A back panel fuse is used for current surge protection. The 115 V operation uses a 8 A slow blow fuse; 230 V operation uses a 5 A slow blow fuse.

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Keep Alive Power Supply

The keep-alive power supply is located on the backplane board. This power supply is used by the power-controlled circuitry, which is also on the backplane board.

Power Sequencing

The power control circuitry provides methods for sequencing power when various conditions occur. This section describes each method.

ON. When you press the ON/STANDY switch to ON, the system unit powers on. The hardware removes the system reset 200 ms after the power supply is in regulation. At that time the CPU will fetch its Reset Exception Vector and begin execution of the specified address.

***NOTE**. All references to the ON/STANDBY switch also apply to the remote on option discussed on page 3–6 if enabled.*

STANDBY. As soon as the ON/STANDBY switch is in the STANDBY position, the software performs house keeping chores such as completing file-management procedures and locking the head in the hard disk drive to a safe position. Once the system has powered off it remains off until you press the switch to ON.

Software Over Current. After powering on and reading each module's ID-ROM, the system software determines if there is too much power required for the power supply and power cord combination. If there is too much power, the system unit powers off even if the ON/STANDBY switch is in the ON position. The system stays down until you cycle the ON/STANDBY switch from ON to STANDBY, then back to ON.

External to Power Supply Over Current. After the system unit powers on, if an External Over Current condition occurs on the +5 V line to any card slot, the system powers off. The system powers off without warning the software even if the ON/STANDBY switch is ON. The system stays off until you cycle the ON/STANDBY switch from ON to OFF, then back to ON.

***NOTE**. There is not an Over Current warning on either the Media +5 V or Media +12 V. The Media +5 V has a fuse and the Media +12 V is current limited. The +16 V and –16 V also have fuses. The +3 V supply does not have a fuse.*

Internal to Power Supply Over Current. After the system unit powers on, if an Internal Over Current condition occurs on the +5 V supply, the supply goes into current limit. This will hold the CPU in a reset condition without warning the

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software. Once the system is in reset it will remain there until the Internal Over Current condition no longer exists, or either one of the following occurs.

- The ON/STANDBY switch is release
- A Card Cage Over Temp condition occurs

Either of these items causes the system to power off after 10 seconds.

Internal to Power Supply Over Voltage. After the system powers up, if an Internal Over Voltage occurs on any of the +5 V, +3 V, +16 V, or –16 V supplies, the system powers off. The system powers off without warning the software even if the ON/STANDBY switch is ON. Once the system has powered off, it will remain off until you unplug the AC power cord then plug it in again. You must also cycle the ON/STANDBY switch from ON to STANDBY then back to ON.

Card Cage Over Temp. If a Card Cage Over Temp condition occurs, the software sets the Shut Down bit to the CPU. This bit causes the system to power off. The system stays down until you cycle the ON/STANDBY switch from ON to OFF then back to ON. The system powers up again if the card cage has cooled down and the Card Cage Over Temp condition no longer exists.

Power Supply Over Temp. If a Power Supply Over Temp condition occurs, the system powers off. The software cannot tell the difference between this over temperature condition and an AC Power Fail. Once the power supply cools and the over temp condition no longer exists, the system attempts to power on. The ON/STANDBY switch must be in the ON position.

AC Power Fail. If an AC Power Fail (loss of AC Power) condition occurs the system powers off. The system stays off until AC power is restored and you cycle the ON/STANDBY switch from ON to OFF then back to ON.

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92C96 Data Acquisition Module

The 92C96 Module is a 100 MHz, 96-channel data acquisition module for general-purpose, medium-speed hardware analysis, 32-bit microprocessor support, and up to 400 mega samples per second of high-speed time analysis. You can acquire 96 channels at speeds up to 100 MHz (synchronous), 48 channels up to 200 MHz, or 24 channels up to 400 MHz (asynchronous). The module comes with twelve 8-channel probes and four single-channel clock probes, or with an optional 90-channel microprocessor interface.

The 92C96 module is available in the following versions:

- 92C96 module with an 8K acquisition depth memory (standard)
- 92C96D module with a 32K acquisition depth memory
- 92C96XD with a 128K acquisition depth memory
- 92C96SD with a 512K acquisition depth memory
- 92A96UD with a 2M acquisition depth memory

In addition to stand-alone operation, you can time-correlate the 92C96 Module with other 92C96 Modules to provide multiple time bases. For more information on using the 92C96 Module, refer to the *92A96 &* 92C96 *User Manual*.

The circuit blocks of the 92C96 include the following (refer to Figure 3–3):

- The Processor Interface Subsystem enables the system controller to set up each of the other subsystems using the backplane.
- The Signal Conditioning Subsystem prepares the system-under-test (SUT) data by improving its signal-to-noise ratio before it is sampled. It also selects the synchronous clock source for the Timing Subsystem.
- The Timing Subsystem provides the pipeline timing clocks for the Acquisition and Qualification Subsystems. This circuitry clocks the data from acquisition through storage.
- The Acquisition Subsystem samples the desired SUT data and presents it for qualification and possible storage in memory.
- The Qualification Subsystem examines the sampled data to determine which part of it to store in memory.
- The Memory Subsystem stores the qualified data.
- The Timestamp Subsystem provides a time reference stored with each sample.

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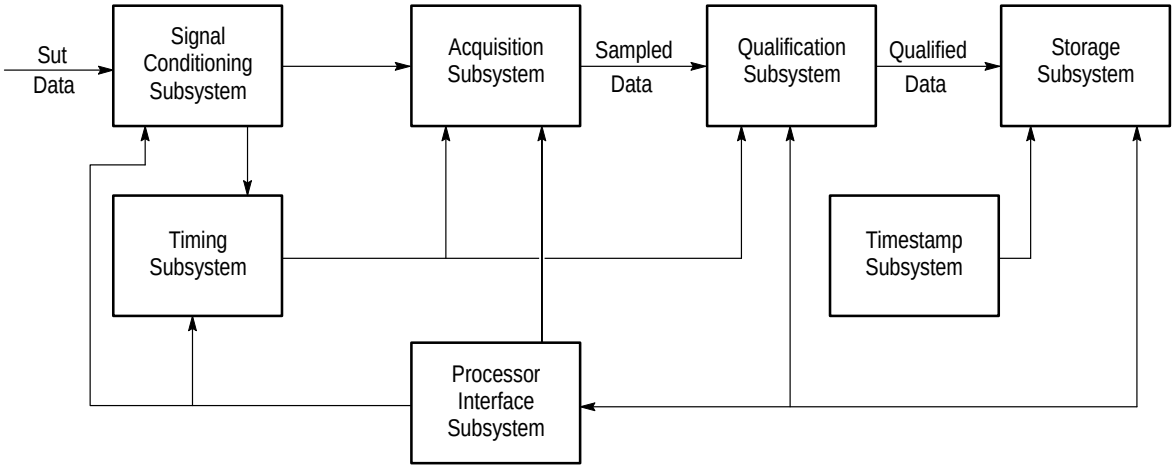


Figure 3–3: 92C96 Module Functional Block Diagram

92S16 Pattern Generation Module

The 92S16 algorithmic pattern generator provides up to 18 channels of output pattern vectors and two clock channels. An SMB connector, located on the back of the module, supplies a TTL-level output trigger signal. The 92S16 uses the P6463A Pattern Generator Probe. The circuit blocks of the 92S16 provide:

- A memory depth of 1 Kbyte of RAM.
- Clock outputs (up to a maximum rate of 50 MHz) for the pattern generation probes. You can select various pattern-generator clock rates to use either internal or external clock signals.
- A controller interface and ROMs that allow communication with the Controller board. These ROMs store the module identification.
- A probe interface establishing a serial communication link for the probes and the status-readback circuitry. This allows the Controller board to read the vector being delivered by the pattern-generator probe and identifies the probe attached to each connector (pod).
- Status readback circuits that take data from the microcode memory, program counter, and first latch, and perform logic operations. The information is divided into 8-bit words for transfer to the controller.
- Probe receivers that convert differential ECL outputs from acquisition and pattern-generator probes to TTL levels.

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- Vector and microcode memories. The vector memory is a 1K × 16 bit RAM and contains the output pattern. The microcode memory (micro-instruction memory) is a 1K × 28-bit RAM. The output of the microcode memory controls the pattern generation.
- A program counter control multiplexer. This multiplexer interprets codes from the program counter to determine the next address for the vector memory output and the microcode memory.
- A program counter that takes the output of the instruction multiplexer and applies the address to the vector memory and the microcode memory.
- An interrupt logic circuit that accepts the external interrupt signal from the optional P6460 or an Event. The signal is clocked through a register that causes the interrupt address to be put onto the bus and the return address to be pushed on the stack.
- A pattern selector that determines the next output pattern. It selects the output pattern from any of three sources: the vector memory, the internal register, or the first latch before the clock (repeat previous vector).
- A pod clock that may be delayed in 5 ns steps, over a range of –5 to +5 ns, referenced to the master clock.
- An inhibit control circuitry that selects either the programmed internal inhibit signal stored in the microcode memory or the external inhibit signal received from the optional P6460 probe. It can also perform appropriate logic operations between the internal inhibit and the external inhibit signals.
- A PROM to supply identification information to the Controller board.

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Performance Verification Procedures

This section is divided into the following three sections:

- *Quick Verification* provides a procedure to verify that the components that make up the system unit are operating and communicating properly.
- *Functional Verification* checks that the individual modules that make up the logic analyzer function properly. These tests may be performed as an incoming inspection and to determine if adjustment, further testing, or repair is necessary.
- *Performance Verification* verifies that the logic analyzer meets the performance requirement specifications. These specifications are listed under the Performance Requirements column in the chapter *Specifications.*

Procedures are provided to verify the following items:

- System unit
- All types of the 92C96 Data Acquisition Modules
- 92S16 Pattern Generation Module

NOTE. *References to 92C96 apply to all types of that module: the 8k standard memory, 92C96D, 92C96XD, 92C96SD, and to the 92A96UD module*

Verification of the probes is included with the appropriate modules.



WARNING. *Dangerous electric shock hazards exist inside the system unit. Only qualified service personnel should perform these procedures.*

This manual does not provide verification for the X Terminal. Refer to the *X Terminal Diagnostics* on page 6–27 for more information on terminal diagnostics and other terminal tests.

Some of the following procedures require you to remove the system unit top cover. You may also be required to add or remove modules from the system unit to perform the verification procedures. Refer to *Removal and Replacement Procedures* on page 6–7 for these details.

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NOTE. *Some of the test procedures involve complex menu setups. If you will be using these procedures again at a later time or date, it is recommended that you save the menu setups on the system unit's hard or floppy disks. Refer to the* TLA 510 & 520 User Manual *for more information on saving the menu setups.*

Verification Interval

To ensure correct instrument operation, verification checks should be checked every 1.5 years. Before performing any verification procedures, complete any relevant maintenance procedures outlined in the *Maintenance* section of this manual.

Equipment Required

The equipment necessary to complete all of the verification procedures is listed in Table 4–1. A partial list of equipment needed for each product is given at the beginning of each procedure.

The specifications given in Table 4–1 are the minimum necessary to produce accurate results. Related equipment must meet or exceed the listed specifications. Detailed instructions for operating test equipment are not included with this manual. Refer to the manual for the specific test equipment if more information is needed.

Table 4–1: Master Equipment List for Verification Procedures

Equipment	Specifications	Equivalent Tektronix Instrument
TLA 510 or 520 system unit	No substitute allowed	
9204XT, 9205XT, or 9206XT Terminal		
92C96 or 92A96UD Data Acquisition Module	No substitute allowed	
92S16 Pattern Generation Module	No substitute allowed	
P6460 External Control Probe	No substitute allowed	
Two P6463A Pattern Generator Probes	No substitute allowed	
P6041 Passive Probe	No substitute allowed	
Two-channel Oscilloscope	400 MHz	
One FET Probe	2.5 to 3.0 pF	
Two Oscilloscope Probes	250 MHz, 10 MΩ	
Two Dual Lead Adapters		015-0325-XX
DC Power Supply	Variable 0–10 V, 2A min	

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Table 4–1: Master Equipment List for Verification Procedures (Cont.)

Equipment	Specifications	Equivalent Tektronix Instrument
Valhalla Scientific Model 2100 Wattmeter or equivalent		
Digital Multimeter	3.5 digits, 0.1% VDC	
Time Base Universal Counter	125 MHz	
Two Pulse Generators	250 MHz	
Sinewave Generator	Adjustable to 250 Mhz	
Subminiature to miniature adapter		013-0202-XX
Three 10-inch coaxial cables	50 Ω	012-0208-XX
One 24-inch coaxial cable	50 Ω	012-1342-XX
One 72-inch coaxial cable	50 Ω	012-0204-XX
Two BNC Connectors	Male-to-Male	103-0029-XX
Two BNC Connectors	Female to Female	
Two Female BNC to Dual Banana Plug Connectors		
BNC T Connector		103-0030-XX
BNC Terminator	50 Ω	011-0049-XX
82 Ω resistor	5%, .25 W	315-0820-XX
68 Ω resistor	5%, .25 W	315-0680-XX
Test Fixtures	Refer to page 5–27	
3.5 in, High Density Floppy Diskette		
RS-232 Line Printer 100 CPS, XON/XOFF, DTR/CTS		
RS-232 Terminal		
Braided Ground Strap		196-3353-XX

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Quick Verification

This section provides a procedure to verify that the components that make up the system unit are operating and communicating properly.

TLA 510 & 520 System Unit

Most of the system unit is tested by power-up diagnostics which are described in the *Maintenance* chapter of this manual. The areas not checked by diagnostics are covered in the following functional check procedures.

Equipment Required

To perform the system unit tests, you will need the following equipment:

- TLA 510 or 520 system unit
- X Terminal
- 92C96 Data Acquisition Module
- RS-232 terminal (with RS-232 cable)
- A 3.5-inch, high density (type 2HD) floppy disk (formatted under Disk Services menu)
- RS-232 Line Printer (100 Characters per Second with XON/XOFF and DTR/CTS flow control)

Equipment Setup

Use the following steps to set up the system unit for the functional checks.

***NOTE**. Although the logic analyzer can be operated remotely without an X Terminal, full testing requires that a local X terminal be attached.*

1. Connect the system unit and X terminal to the appropriate power source. Ensure that the system unit is properly connected to the X Terminal.
2. Power up the X Terminal.
3. Power up the system unit. After a few moments the logo will appear.
4. After the logo, check that the Menu Selection Overlay appears on the screen.

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System Unit Functional Checks

Use the following steps to functionally check all slots, the system unit controller board, backplane, power supply, and hard and floppy disk drives.

1. Move the cursor to the Utilities column and select the Diagnostic menu. Check that the Diagnostic menu appears. If no failures occur, the following areas have been functionally checked:
   - System Microprocessor and Microprocessor Control Bus
   - Dynamic RAM
   - Memory Management System
   - Boot ROM
   - Hard-Disk Drive and Interface
   - X Terminal RS-232 Serial Port
   - LAN Port
2. Select the 92C96 module and select the Trigger menu.
3. Press **F1: START** to begin an acquisition. After a few moments, the State Table menu will appear. Insert a floppy disk into the floppy disk drive. Save the system setup on a floppy disk by using the following steps:
   - **a.** Select the Save/Restore menu from the Menu Selection Overlay.
   - **b.** Move the cursor to the Operation field and select **Save System Setup**.
   - **c.** Move the cursor to the File field and type in a temporary file name.

NOTE. *You must choose a unique file name. If you use an existing file name on the hard disk, the contents of that file will be overwritten.*

   - **d.** Press **F8: EXECUTE OPERATION** to save the system setup on the hard disk.
   - **e.** Select the Disk Services menu from the Menu Selection Overlay.

NOTE. *If you have an unformatted floppy disk, select Format Floppy, and then press F8: EXECUTE OPERATION and follow the on screen prompts.*

   - **f.** Move the cursor to the Operation field and select **Copy File**.
   - **g.** Move the cursor to the Source Disk field and select **Hard Disk**.
   - **h.** Move the cursor to the Source File Type field and select **Setup**.

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i. Move the cursor to the Source File Name field and either select or type in the file name you used in step c above.

j. Move the cursor to the Destination Disk field and select **Floppy**.

k. Move the cursor to the Destination File field and either select or type in a temporary file name.

l. Press **F8: EXECUTE OPERATION** to copy the system setup on the floppy disk. Very that the file is successfully saved to the floppy disk.

This completes the functional checks of the Start Event Line and the floppy and hard-disk drive interfaces.

4. Connect the line printer to the Auxiliary RS-232 port connector on the system unit.

5. Select the Communication menu from the Menu Selection Overlay.

6. Move the cursor to the RS-232 Auxiliary Port Baud Rate field and select the fastest baud rate that your printer will support. Move the cursor to the Flow Control field and select **DTR/CTS**.

7. Select the State menu from the Menu Selection Overlay.

8. Select the on-screen Print button to select the State Table Print menu.

9. Move the cursor to the Send Output To field and select **RS-232 Auxiliary Port**.

10. Set the Characters per Line, Lines per Page, New Line Characters, and New Page Characters as appropriate for your printer. The Output Format field should be set to ASCII.

***NOTE**. Refer to your printer's documentation for setting the RS-232 parameters.*

---

11. Move the cursor to the Print Sequence Number field and enter **0** for the beginning sequence number. Set the ending sequence number to print 10 pages. (To print 10 pages; multiply the Lines per Page number by 10 and enter that value in the ending sequence number field.)

12. Press **F5: START PRINT** followed by **Return** (to confirm your choice), to begin the print operation. Ensure that there are no missing characters or lines on the printout. This checks the DTR/CTS Flow Control.

13. Press **F8: EXIT & SAVE**. Select the Communications menu from the Menu Selection Overlay.

14. Change the RS-232 Auxiliary Port Flow Control field to **XON/XOFF**.

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15. Repeat steps 7 through 12 to check the XON/XOFF Flow Control.

This completes the functional checks of the Auxiliary RS-232 port connector and related circuitry.

16. Connect a remote RS-232 terminal to the Host RS-232 port connector of the system unit using an appropriate RS-232 cable. Refer to *Host Computer or Serial Printer Connections* in the *Getting Started* chapter of the *TLA 510 & 520 User Manual* for further information on the RS-232 requirements. Ensure that the terminal baud rate and RS-232 communication parameters match the TLA 510 or 520 communication menu parameters.

    Be sure that DAS 9200 PCL is the selected protocol for the TLA RS-232 Host Port.

NOTE. *Refer to the documentation for your terminal to set the RS-232 parameters. Refer to the the* TLA 510 & 520 User Manual *for instructions on how to set the Host RS-232 port parameters to match the remote terminal.*

---

17. Issue an Identification query by typing ID? followed by Enter or Return, on the remote terminal keyboard. Note that the TLA 510 or 520 does not support remote echo. Therefore, the typed characters will not appear on the terminal display. Verify that the TLA 510 or 520 returns an ID response. This checks the Host RS-232 port.

18. Select the Diagnostic menu from the Menu Selection Overlay and press **F5: SET TIME**. The Set Date/Time Overlay will appear on the screen. Now, set the system date and time. Press **F8: EXIT & SAVE** to save the new values.

19. Power down the system unit. Wait approximately five minutes and power it up again. Check that the date and time are correctly set and that the Diagnostic menu indicates a **Normal** previous shutdown. This checks the NVRAM and Clock Calendar circuitry on the Controller Board.

LAN Functional Verification

For stand-alone TLA 510 and 520 operation with an X Terminal, the LAN functionality is verified by being able to display TLA 510 and 520 menus on the terminal. The following procedure is intended for logic analyzers operating on a network. Before you can verify the LAN operation, the following must have occurred:

- The logic analyzer must contain the correct version of system software (Release 3, Version 1.40 or higher).
- The local area network cable (Thicknet or Thinnet) must be properly connected to the rear of the system unit.

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- The Thicknet/Thinnet jumper block (J686) must be in the correct position (Thick for Thicknet or Thin for Thinnet). The default is Thinnet.
- The Internet address, Getaway address, and Subnet mask must be set and installed. Refer to *Configuration Utility* on page 6–86 for details.
- The host setup has been updated to recognizes the logic analyzer at the specified Internet address.

Perform the following steps to verify proper LAN operations.

1. Make a connection between the host and the logic analyzer using FTP.
2. After the connection is made, transfer any large ASCII text file (called doc in the example) into the Print_Output directory of the logic analyzer using the FTP put command. Refer to the *Put Example*.

NOTE. *The Print_Output directory accepts ASCII text files. Text files are easier to read and therefore easier to compare.*

3. Transfer the file back from the logic analyzer by using the FTP get command and change the file's name to doc.copy. Refer to the *Get Example*.
4. Use a host system utility such as Unix diff command to compare the returned file (doc.copy) against the original (doc) for completeness. If the returned file is identical to the original, the functional check has passed and the LAN is ready to operate.

Put Example

The following example of the put command shows how the connections are made with FTP in steps 1 and 2 above.

```
ftp> cd Print_Output
250 CWD command successful.
ftp> put doc
200 PORT command successful, port = 36,1,0,0,11,231.
150 STOR: Opening data connection for doc (36.1.0.0,3047).
226 STOR: Transfer complete.
local: doc remote: doc
379220 bytes sent in 18 seconds (21 Kbytes/s)
ftp>
```


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Get Example

The following example of the get command shows how a file is read back from the host via the network.

```
ftp> get doc doc.copy
200 PORT command successful, port = 36,1,0,0,11,234.
150 RETR: Opening data connection for doc
(36.1.0.0,3050) (374864 bytes).
226 RETR: Transfer complete.
local: doc.copy remote: doc
379220 bytes received in 17 seconds (22 K-bytes/s)
```

This completes the Quick Verification of the TLA 510 or 520 system unit.

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Functional Verification

This section checks that the individual modules that make up the logic analyzer and the Discrete I/0 function properly. These tests may be performed as an incoming inspection to determine if adjustment, further testing, or repair is necessary.

Discrete I/0

The 92PORT software must be properly installed before the test can be performed. Refer to the *92PORT Instructions* for more information.

1. Power on the X Terminal and then the TLA 5010 or 520 system unit. Verify that diagnostics pass.
2. Verify that both the TLA 510 or 520 window and the 92PORT window appear on the X Terminal. If the 92PORT window does not appear you should confirm that the 92PORT software is properly installed. Refer to the *92PORT Instructions* for more information.
3. Install the Discrete I/O Loopback fixture onto the Discrete I/O port backpanel connector. Refer to page 5–36 for instructions on building the fixture.
4. Test the Discrete I/O outputs and inputs by clicking the mouse on each button (output) in the 92PORT window. Verify that each indicator (input) responds by changing color. Notice that some of the outputs are toggle functions while others are momentary.
5. Connect a voltmeter between a ground square pin and the +5 V output pin on the loopback fixture. Verify that the meter reading is approximately +5 V.
6. Connect a oscilloscope channel 1 ground to a ground square pin. Connect the channel 1 input to the Write output square pin of the loopback fixture. Adjust the oscilloscope for 1 V/div, 1 µs/div, negative trigger slope, and a trigger level of approximately +1.5 V.
7. Test the Write Output strobe by clicking the mouse on one of the output buttons in the 92PORT window. Check for the presence of the pulse by verifying that the oscilloscope trigger indicator flashes when the mouse button is clicked.
8. Connect the scope input to the Read Output strobe square pin. Click the mouse on one of the Output buttons in the 92PORT window. Verify that a negative going pulse appears on the oscilloscope display. You might need to increase the intensity to see this pulse.

This completes the functional verification of the Discrete I/O interface.

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92C96 Acquisition Module

These test procedures check the 92C96 Module for basic operation functionality. They exercise and check the main internal features and attached probes and cables that are not covered by the power-up diagnostics.

These test procedures include:

- Module Sync Out
- Input Channel Threshold
- Internal Clocking: General Purpose Support
- Internal Clocking: High-Speed Timing Support
- External Clocking

Complete the tests for each 92C96 Module one at a time. The External Clocking test requires a 92S16 Pattern Generation Module. Refer to the *Removal and Replacement Procedures* on page 6–7 for instructions on removing and installing modules in the system unit.

NOTE. *All of the hardware and system setups build upon the previous tests. The individual tests only include the changes from the previous setup. For these reasons, the tests should be performed consecutively from start to finish.*

Equipment Required

The following list of equipment is necessary to complete the functional checks.

- TLA 510 or 520 system unit
- X Terminal
- 92C96 Data Acquisition Module (with standard accessories)
- 92S16 Pattern Generation Module
- Two P6463A Pattern Generation Probes with leadsets
- P6041 Passive Probe (Sync Out Cable)
- Two-channel, 400-MHz Oscilloscope (Tektronix 2465B with standard probes)
- 5 VDC Power Supply (1 A per P6463A probe) (Tektronix PS 282)
- One 24-inch, 50 Ω BNC Coaxial Cable (Tektronix part number 012-1342-00)
- 50 Ω Feed-through Termination (Tektronix part number 011-0049-01)

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- 92C96 Acquisition Fixture[1]
- General Purpose Acquisition Fixture[2]
- Decoupling Fixture[2]

Module Sync Out Test

This test checks the 92C96 Module Sync Out signal to see that it exists, transitions between approximately 0 V and +5 V, and has a 50 Ω source impedance.

Equipment Setup. Use the following hardware setups as shown in Figure 4–1 for this test.

1. Connect the Sync Out cable (P6041) to J900 on the 92C96 Module.
2. Connect the other end of the Sync Out cable to the vertical input channel of an oscilloscope.
3. Adjust the oscilloscope input attenuation for 1 V/div, input termination for 1 MΩ and horizontal timebase for 20 ns/div.

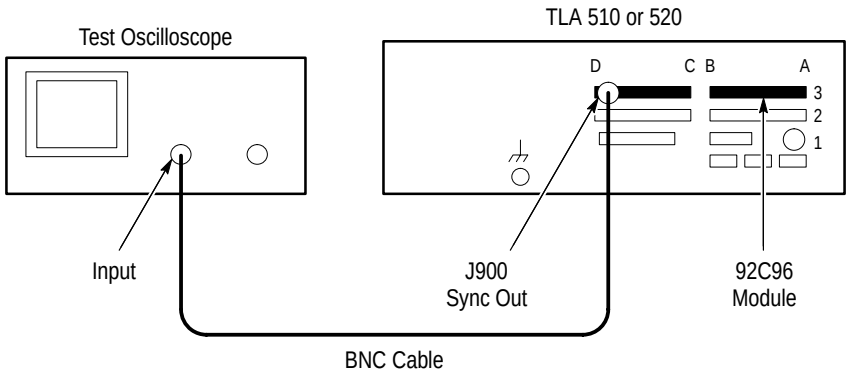


Figure 4–1: 92C96 Channel Connections

1 **You must build a 92C96 Acquisition Fixture as described under Test Fixtures on page 5–27 to connect the Sync Out signal to the inputs of the acquisition probes.**

2 **You must build a General Purpose Acquisition Fixture and a Decoupling Fixture as described under Test Fixtures on page 5–27 to connect the outputs of the pattern generation probes to the inputs of the acquisition probe and to provide power to the pattern generation probes.**

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Test Operation. Use the following steps to check operation of the Sync Out signal.

1. Power on the logic analyzer and select the 92C96 Trigger menu and program the menu as shown.

```
Trigger Pos: T--------
Store: All Cycles
Prompt Visibility: On
------------------------------------------------------------------

State   One
  If      Anything
  Then    Assert Signal         Module Sync Out
          Go To State           Two

End of State One

State   Two
  If      Anything
  Then    Unassert Signal       Module Sync Out
  Go To State                   One

End of State Two
```

This Trigger program generates a Sync Out signal period that is twice the selected sampling period (the power-up default period is 10 ns asynchronous).

2. Press **F1: START** to enable the Sync Out signal.
3. Check the oscilloscope display for a square-wave trace transitioning from approximately 0 V to +5 V with a 20 ns period.
4. Select 50 Ω input termination (or use external 50 Ω terminator) for the oscilloscope vertical input. Verify the amplitude is now 0 V to 2.5 V.
5. Press **F1: STOP**.

Input Threshold Test

This test checks continuity for all input data channels and checks that their threshold levels are functional.

Equipment Setup. Use the following hardware setups as show in Figure 4–2 for this test. The Sync Out signal from the 92C96 Module is used as a test signal for this test procedure.

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1. Move the end of the Sync Out cable from the oscilloscope to the 92C96 Acquisition Fixture. Disconnect the 50 Ω termination from the Sync Out cable, if present, for the acquisition fixture provides its own termination.
2. Connect sections A0 and A1 (channel podlet groups) of the orange 92C96 Probe to the 92C96 Acquisition Fixture. Pay attention to proper ground and signal orientation

***NOTE**. The 92C96 Acquisition Fixture only allows testing of 16 channels at a time.*

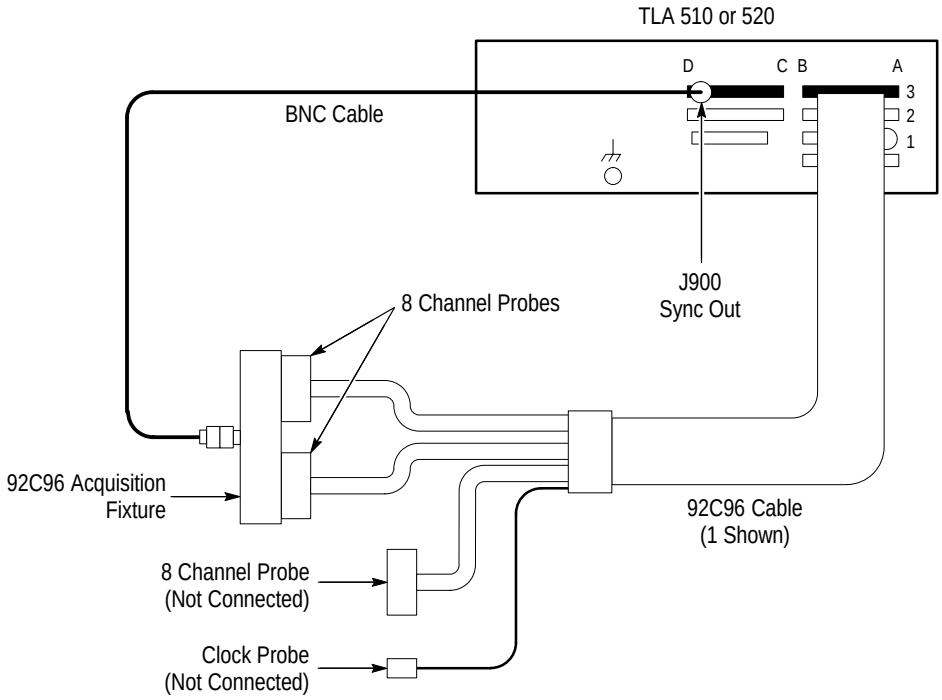


Figure 4–2: 92C96 Channel Connections for the Input Threshold Check

Test Operation. Use the following procedure to check all input channels of the 92C96 Module for operation and to check that the variable threshold works.

1. Select the 92C96 Clock menu.
2. Select Internal clocking and a 100 ns clock period.

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***NOTE**. Clocks faster than 100 ns show some delay before the test pattern begins. This is due to the latency of the Sync Out signal and is considered normal behavior.*

3. Select the 92C96 Trigger menu.
4. Move the cursor to the "Go To State" action in State One and press **F8: ADD**. Select **Add Action** to add a trigger action to State One.
5. Select the 92C96 Channel menu.
6. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.
7. Set Data Thresholds to TTL (+1.5 V) and press **F8: EXIT & SAVE**.
8. Press **F1: START**.
9. Check the 92C96 State display for a pattern of all zeros and all ones (00... and FF...) on alternating sequences for all channels of the sections being tested. (All other channels will be solid all ones.)
10. Select the 92C96 Channel menu.
11. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.
12. Set Data Thresholds to VAR (variable), +3.0 V and press **F8: EXIT & SAVE**.
13. Press **F1: START**.
14. Check the 92C96 State display for a pattern of all zeros for all channels of the sections being tested.
15. Select the 92C96 Channel menu.
16. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.
17. Set Data Thresholds to VAR (variable), –0.50 V and press **F8: EXIT & SAVE**.
18. Press **F1: START**.
19. Check the 92C96 State display for a pattern of all ones for all channels of the sections being tested.
20. Now repeat steps 5 through 19 for sections A2 and A3, D0 and D1, D2 and D3, C0 and C1, and C2 and C3.

***NOTE**. You must remove the previously connected sections from the 92C96 Acquisition Fixture and replace them with the next sections to test until you've checked all 96 channels of the 92C96 Module.*

21. Select the 92C96 Channel menu.

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22. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.

23. Set Data Thresholds to TTL (+1.5 V) and press **F8: EXIT & SAVE**.

Internal Clocking: General Purpose Support Test

This test checks that data can be properly acquired at various clock rates from 10 ns to 1 ms.

Equipment Setup. Use the previous hardware setups with the following changes:

1. Move the end of the Sync Out cable from the 92C96 Acquisition Fixture to the oscilloscope vertical input.
2. Adjust the oscilloscope horizontal timebase for 1 ms/div.

Test Operation. Use the following steps to check the internal clocking for General Purpose Support of the 92C96 Module.

1. Select the 92C96 Trigger menu.
2. Move the cursor to the Trigger action in State One.
3. Press **F7: DELETE**, select **Delete Action** to delete the Trigger action from State One (disables triggering).
4. Select the 92C96 Clock menu and set Clock to Internal 1 ms.
5. Press **F1: START**.
6. Check for the following after the 92C96 Monitor menu appears:
   - The orange bar in the upper left corner of the display should be actively switching between states One and Two.
   - All counters should be displayed as Unused.
   - The flag should be displayed as Cleared.
   - The Memory Status indicator should be orange to the left of the T and gray to the right.
   - The Memory Locations Unfilled field will vary depending on the Trigger Position selected in the Trigger menu and on the module memory size.
7. Check the oscilloscope display for a Sync Out signal with a 2 ms period (twice the clock period).
8. Press **F1: STOP**.
9. Select the 92C96 Clock menu and change the internal clock to 500 µs.
10. Press **F1: START**.

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11. Check the oscilloscope display for a Sync Out signal that is twice the clock period.

12. Repeat steps 8 through 11 for each of the following clock period values to be used in step 9: 200 µs, 100 µs, 50 µs, 20 µs, 10 µs, 5 µs, 2 µs, 1 µs, 500 ns, 200 ns, 100 ns, 50 ns, 20 ns, and 10 ns. Change the oscilloscope time per division setting as required to view the Sync Out signal.

NOTE. *Internal clock rates at or above 5 µs cause the display of the orange bar indicating changing states to become erratic and, at times, to disappear from the screen.*

---

13. Press **F1: STOP**.

Internal Clocking: High-Speed Timing Support Test

This test checks that data can be properly acquired at various clock rates from 5 ns to 1 ms.

Equipment Setup. Use the previous hardware setups for this test.

Test Operation. Use the following steps to check the high-speed internal clocking of the 92C96 Module.

1. Select the 92C96 Config menu.
2. Select High-Speed Timing in the Software Support field.
3. Select the 92C96 Clock menu and change the internal clock to 1 ms.
4. Select the 92C96 Trigger menu. Setup the menu as shown in Figure 4–3 (same as the Module Sync Out check).

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```
Trigger Pos: T--------
Store: All Cycles
Prompt Visibility: On
------------------------------------------------------------------------
State   One
  If      Anything
  Then    Assert Signal         Module Sync Out
  Go To State                   Two

End of State One

State   Two
  If      Anything
  Then    Unassert Signal       Module Sync Out
  Go To State                   One

End of State Two
```

Figure 4–3: Internal Clocking High-Speed Timing Test Trigger Menu

5. Press **F1: START**.
6. Check the oscilloscope display for a Sync Out signal that is four times the selected clock period.
7. Repeat steps 3 through 6 for each of the following clock period values to be used in step 3: 500 µs, 200 µs, 100 µs, 50 µs, 20 µs, 10 µs, 5 µs, 2 µs, 1 µs, 500 ns, 200 ns, 100 ns, 50 ns, 20 ns, 10 ns, and 5 ns. Change the oscilloscope time per division setting as required to view the Sync Out signal. Also note that the Sync Out signal period will still be 20 ns if tested at the 2.5 ns (or 5 ns) clock period.
8. Press **F1: STOP**.

External Clocking Test

This test checks each of the four clock lines and the four qualifier lines for proper edge and level operation.

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NOTE. *This check requires that a TLA 510 that does not already have a 92S16, must have one installed in slot #2 in order to perform the External Clocking check.*

A TLA 520 must have the 92C96 in slot #2 removed and replaced with a 92S16. After the External Clocking check has been performed on the 92C96 in slot #3, it can be swapped with the 92C96 that was previously removed.

Equipment Setup. Disconnect the equipment from the previous test. Table 4–2 shows the necessary connections between the P6463A Pattern Generation Probes, the General Purpose Acquisition Fixture pins, and the 92C96 Module probe channel podlets for the remaining functional check tests.

Table 4–2: Functional Check Connections

92C96 Channel	Acq Fix Pin #	P6463A	92S16
–	39	CLK	POD B
C1_0	37	8	POD B
A3_0	35	7	POD B
A2_0	33	6	POD B
A1_0	31	5	POD B
A0_0	29	4	POD B
D3_0	27	3	POD B
D2_0	25	2	POD B
D1_0	23	1	POD B
D0_0	21	0	POD B
–	19	CLK	POD A
C0_0	17	8	POD A
Clock_3	15	7	POD A
Clock_2	13	6	POD A
Clock_1	11	5	POD A
Clock_0	9	4	POD A
C2_0	7	3	POD A
C2_3	5	2	POD A
C2_2	3	1	POD A
C2_1	1	0	POD A

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Use the following steps to connect the two P6463A probes and the 92C96 probe assembly podlets to the General Purpose Acquisition Fixture, and to connect the Decoupling Fixture to the two P6463A probes.

NOTE. *Prior to connecting the P6463A probes, verify that they are configured in the 9-bit mode. Refer to the P6463A manual for details.*

1. Position the acquisition fixture such that the ground square pins are to the bottom and the pattern generation probes to the right side. Place the 92C96 probes on the left side of the acquisition fixture.

   The General Purpose Acquisition Fixture connects between the 92C96 probes and the P6463A Pattern Generation Probes.

2. Refer to Table 4–2 to connect the 92C96 probe to the acquisition fixture. The square pin closest to the 18-inch black lead is designated as pin 1. Be sure to connect the ground side of the podlets to the ground square pins of the acquisition fixture. Tie the unused leads of the lead sets with a rubber band.

3. Connect the P6463A Pattern Generation Probes to the acquisition fixture as indicated by Table 4–2. Be sure to connect the ground side of the podlets to the ground square pins of the fixture. Tie back the unused leads of the lead set with a rubber band.

4. Carefully connect the positive side of the Decoupling Fixture to the positive side of the power supply, and connect the negative side of the fixture to the negative side of the power supply. Note the polarity of the tantalum capacitor.



CAUTION. *Incorrectly connecting the power to the Decoupling Fixture can cause the tantalum capacitor to burn or explode.*

5. Connect the 18-inch black lead of the acquisition fixture to the common or ground output of the power supply.

6. Connect the black (VL) leads of both pattern generator probes to the common or ground output of the Decoupling Fixture.

7. Connect the red (VH) leads of both pattern generator probes to the positive side of the Decoupling Fixture.

8. If you suspect any problems with your connections, double check your wiring. Also be certain that you have turned ON the +5 V power supply.

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92S16 Pattern Generation Setups. The following steps list the initial 92S16 Pattern Generation setups that are used in the remaining procedures.

NOTE*. All of the following pattern generation menus are created from power-up default conditions. If you restore any previous menu setups, the default conditions will be overwritten and the menu setups may not be correct.*

1. Select the 92S16 Module and select the 92S16 Config menu.
2. Change the Clock field to Internal 20 ns.
3. Select the 92S16 Channel menu.
4. Move the cursor to the top Group Name field and change the name to Add/Data.
5. Move the cursor to the right upper pod field and select **2A_7-0**.
6. Press **F7: DELETE** and select **Delete Pod from Group**.
7. Use **F8: ADD** to add another group. Change the new Group Name field to Control. Move the cursor to the right and select **2B_8**. The Channel field should show Ch 8. Use **F8: ADD** to add another pod and select **2A_8**. The Channel field should show Ch 8.
8. Use **F8: ADD** to add another group. Change the Group Name field to Clk/Qual. Move the cursor to the right and select **2A_7-0**. The Channels field should show Ch 76543210.
9. The 92S16 Channel menu should look like Figure 4–4.

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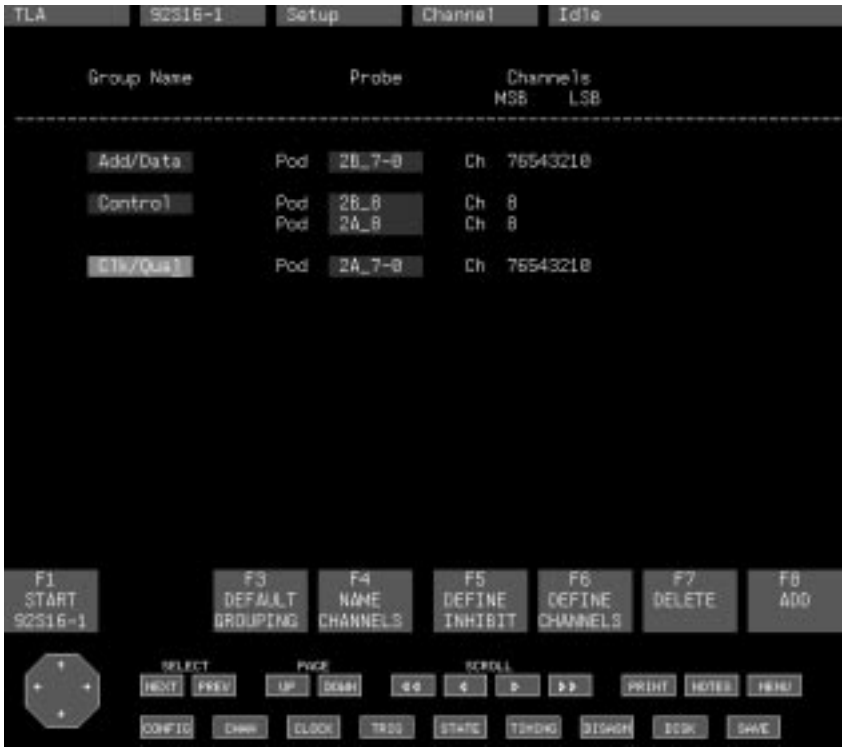


Figure 4–4: 92S16 Channel Menu

This example shows the 92S16 Channel menu used for the 92C96 functional tests.

10. Select the 92S16 Program menu.

11. Press **F5: DISPLAY FORMAT**.

Set the radix of Add/Data to Hex and Order to 0. Set the radix of Control to Bin and Order to 1. Set the radix of Clk/Qual to Bin and Order to 2. Press **F8: EXIT & SAVE**.

12. Press **F3: RUN CONTROL**.

Set the 92S16 Start Location field to Seq 0. Press **F8: EXIT & SAVE**.

13. Program the 92S16 as shown in Figure 4–5 and Figure 4–6.

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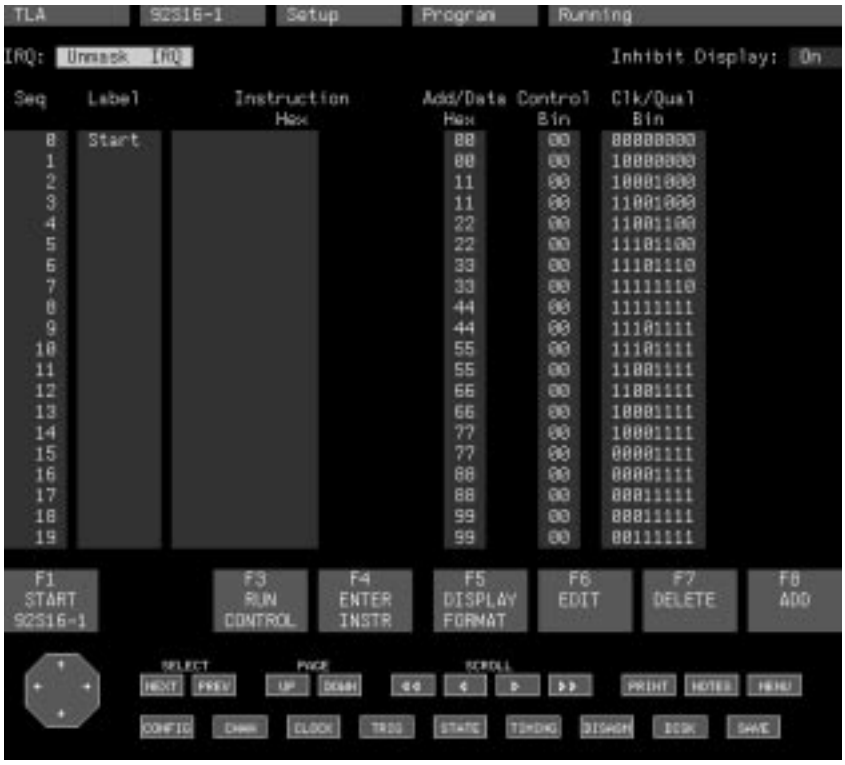


Figure 4–5: 92S16 Program Menu for the External Clocking Tests (Sequences 0 – 19)

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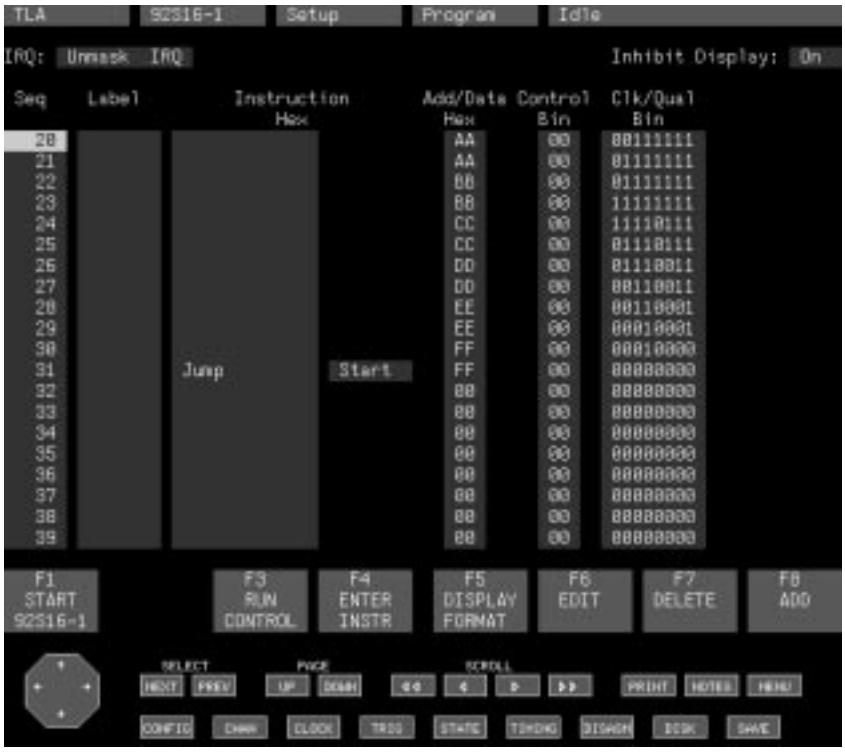


Figure 4–6: 92S16 Program Menu for the External Clocking Tests (Sequences 20 – 31)

14. Select the 92S16 Monitor menu.

15. Check that the Trace field is Off.

92C96 Data Acquisition Setups. Use the following steps to set up the 92C96 Module for the External Clock Tests.

1. Select the 92C96 Module.

2. Select the 92C96 Config menu. Select **General Purpose** in the Software Support field, select OFF in the Latch Mode field.

3. Select the 92C96 Channel menu. Program the channel menu to match Figure 4–7. Use **F7: DELETE** and **F8: ADD** to get the required display.

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Figure 4–7: 92C96 Channel Menu for the External Clocking Tests

4. Use the default values for the Channel Definition overlay and use the default values for the Threshold Definition overlay (TTL).
5. Select the 92C96 Trigger menu. Press **F4: DEFAULT TRIGGER** to select the default trigger menu.
6. Select the 92C96 Clock menu. Move the cursor to the Module Clock field and select **External**. You will initially start with the default clock, rising edge (⁄) of Clock _3.

Test Operation

Use the following steps to check the operation of the external clocks and qualifiers.

1. Select the 92S16 Module and select the Monitor menu.
2. Press **F1: START** to start the 92S16 Module.
3. Select the 92C96 Module and select the Clock menu.
4. Refer to Table 4–3 and select the rising edge (⁄) of Clock_3.

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5. Press **F1: START** to start the 92C96 Module. After the acquisition has completed, compare the acquired data with the expected data (in hexadecimal radix) under the Add/Data column in Table 4–3. Check the screen for a repeating series of the data listed in the table.

6. Repeat the above steps for each test listed in Table 4–3 using the external clock and qualifiers shown in the table. The Add/Data are the expected results of each test.

7. Select the 92S16 Module and then select the Monitor menu.

8. Press **F1: STOP** to stop the 92S16.

Table 4–3: 92C96 External Clocking Test

Test	External Clocks and Qualifiers	Add/Data
1	⎍ Clock_3	00 BB
2	⎎ Clock_3	77 CC
3	⎍ Clock_3 AND /Clock_1 or ⎎ Clock_3 AND /Clock_1	00 77
4	⎍ Clock_3 AND Clock_1 or ⎎ Clock_3 AND Clock_1	BB CC
5	⎍ Clock_3 AND /C2_0 or ⎎ Clock_3 AND /C2_0	00 CC
6	⎍ Clock_3 AND /C2_0 or ⎎ Clock_3 AND /C2_0	77 BB
7	⎍ Clock_2	11 AA
8	⎎ Clock_2	66 DD
9	⎍ Clock_2 AND /Clock_0 or ⎎ Clock_2 AND /Clock_0	11 66
10	⎍ Clock_2 AND Clock_0 or ⎎ Clock_2 AND Clock_0	AA DD
11	⎍ Clock_2 AND /C2_3 or ⎎ Clock_2 AND /C2_3	11 DD

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Table 4–3: 92C96 External Clocking Test (Cont.)

Test	External Clocks and Qualifiers	Add/Data
12	⎍ Clock_2 AND C2_3 or ⎲ Clock_2 AND C2_3	66 AA
13	⎍ Clock_1	22 99
14	⎲ Clock_1	55 EE
15	⎍ Clock_1 AND /Clock_3 or ⎲ Clock_1 AND /Clock_3	99 EE
16	⎍ Clock_1 AND Clock_3 or ⎲ Clock_1 AND Clock_3	22 55
17	⎍ Clock_1 AND /C2_2 or ⎲ Clock_1 AND /C2_2	22 EE
18	⎍ Clock_1 AND /C2_2 or ⎲ Clock_1 AND /C2_2	55 99
19	⎍ Clock_0	33 88
20	⎲ Clock_0	44 FF
21	⎍ Clock_0 AND /Clock_2 or ⎲ Clock_0 AND /Clock_2	88 FF
22	⎍ Clock_0 AND Clock_2 or ⎲ Clock_0 AND Clock_2	33 44
23	⎍ Clock_0 AND /C2_1 or ⎲ Clock_0 AND /C2_1	33 FF
24	⎍ Clock_0 AND /C2_1 or ⎲ Clock_0 AND /C2_1	44 88

This completes the 92C96 Module functional tests.

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92S16 Pattern Generation Module

This procedure functionally checks the 92S16 Pattern Generation Module. The procedure includes the following tests: External Inhibit, External Jump, External IRQ and Qualifier, External Pause, External Start, and Trigger Out. The power-up diagnostics check most of the internal electronic circuitry except the probes and functions that can only be checked with the probes connected.

Equipment Required

You will need the following equipment to perform the 92S16 functional checks. You will need to build one General Purpose Acquisition Fixture, one BNC-to Test Point Adapter, and one Decoupling Fixture as described on page 5–27.

- TLA 510 or 520 system unit
- X Terminal
- 92C96 Data Acquisition Module
- 92S16 Pattern Generation Module
- Two P6463A Pattern Generation Probes (with lead sets)
- P6460 External Control Probe (with lead set)
- P6041 Passive Probe (Sync Out Cable)
- Adjustable 250 MHz Sinewave Generator
- 250 MHz Pulse Generator
- 400 MHz Oscilloscope (Tektronix 2465B)
- Two P6137 Oscilloscope Probes
- +5 V Power Supply (2 A minimum) (Tektronix PS 282)
- 24-inch 50 Ω coaxial cable (Tektronix part number 012-1342-00)
- BNC-to-Test Point Adapter (Refer to Test Fixtures beginning on page 5–27)
- General Purpose Acquisition Fixture (Refer to Test Fixtures beginning on page 5–27)
- Decoupling Fixture (Refer to Test Fixtures beginning on page 5–27)

Equipment Setup

Use the following steps to set up the TLA 510 or 520 system unit and test equipment for the 92S16 functional checks. This procedure uses the same equipment setups for all the tests.

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1. Position the General Purpose Acquisition Fixture such that the ground square pins are to the bottom. Place the P6463A probes on the right side of the fixture and the 92C96 probes on the left.

2. Refer to Table 4–4 to connect the leadsets of each probe to the acquisition fixture. The square pin closest to the 18-inch black lead is designated as pin 1. Connect the probes to their respective pod connectors on the 92S16 and 92C96 Modules as indicated in the table. It may be necessary to remove the backpanel probe retainer clips to connect the probes.

Table 4–4: Acquisition Fixture Connections

92C96 Channel	Acq Fix Pin #	P6463A	92S16
Clock_2	39	CLK	POD B
C2_1_Brn	37	8	POD B
D1_7_Vlt	35	7	POD B
D1_6_Blu	33	6	POD B
D1_5_Grn	31	5	POD B
D1_4_Ylw	29	4	POD B
D1_3_Org	27	3	POD B
D1_2_Red	25	2	POD B
D1_1_Brn	23	1	POD B
D1_0_Blk	21	0	POD B
–	19	CLK	POD A
C2_0_Blk	17	8	POD A
D0_7_Vlt	15	7	POD A
D0_6_Blu	13	6	POD A
D0_5_Grn	11	5	POD A
D0_4_Ylw	9	4	POD A
D0_3_Org	7	3	POD A
D0_2_Red	5	2	POD A
D0_1_Brn	3	1	POD A
D0_0_Blk	1	0	POD A

NOTE. *Prior to connecting the P6463A probes, verify that they are configured in the 9-bit mode. Refer to the P6463A manual for details.*

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3. Carefully connect the positive side of the decoupling fixture to the positive side of the power supply, and connect the negative side of the fixture to the negative side of the power supply. Note the polarity of the tantalum capacitor.



WARNING. *Incorrectly connecting the power to the decoupling fixture can cause the tantalum capacitor to burn or explode.*

4. Connect the black (VL) leads of both pattern generator probes to the common or ground output of the decoupling fixture. Connect the 18-inch black lead of the acquisition fixture to the ground or common output of the power supply.
5. Connect the red (VH) leads of both pattern generator probes to the positive side of the decoupling fixture.
6. Connect a 50 Ω coaxial cable from the output of the sinewave generator to the input of the pulse generator.
7. Power up the test equipment.
8. Set the sinewave generator to an output frequency of 10 MHz and an output amplitude of 4 V peak-to-peak.
9. Connect the channel 1 scope probe to the output of the pulse generator. Set the pulse generator to trigger on the external input and set the pulse duration to 20 ns. Use the following steps to adjust the pulse generator output:
   a. Change the scope Volts/Div to 1 V.
   b. Ground the channel 1 input of the scope.
   c. Use the Vertical Position control to place the scope's trace 1.4 divisions below the center graticule.
   d. Remove the ground from the channel 1 input.
   e. Set the level controls of the pulse generator to center a 2 V peak to-peak signal on the center graticule of the scope.
   f. Adjust the output for a pulse width of 20 ns.
   g. The pulse generator output is now centered at the 1.4 V threshold. Any signals appearing above the center graticule of the scope is considered a TTL high; any signals below the center graticule is considered a TTL low.
10. Ensure that the TLA 510 or 520 system unit is properly connected to the terminal. Power up the terminal and the system unit.
11. Check that the system unit passes all of the power-up diagnostics.

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NOTE. *The power-up diagnostics must be successfully completed before you continue this procedure.*

Cluster Setup

Use the following steps to set up the cluster t for the remainder of this procedure.

1. Select the Sys Config menu from the Menu Selection Overlay.
2. Press **F6: DEFINE CLUSTER** followed by **F2: CLUSTER ALL**.
3. Press **F8: EXIT & SAVE**.

External Inhibit Test

This test checks the external inhibit circuitry of the 92S16.

92S16 Pattern Generator Setups. Use the following steps to set up the 92S16 Module for the External Inhibit test. These setups are the initial setups used for the remainder of this procedure.

1. Select the 92S16 Module and select the 92S16 Config menu.
2. Move the cursor to the Clock field and select **Internal 100 ns**.
3. Move the cursor to the P6460 Threshold Level field and select **TTL**.
4. Select the 92S16 Channel menu.
5. Refer to Figure 4–8 and do the following steps to program the channel menu:
   a. Change the 92S16 group name to **S16_Data**.
   b. Press **F8: ADD** and select **Add Group.** Change the new group name to **S16_Qual**. Press **F8: ADD** and select **Add Pod to Group**.

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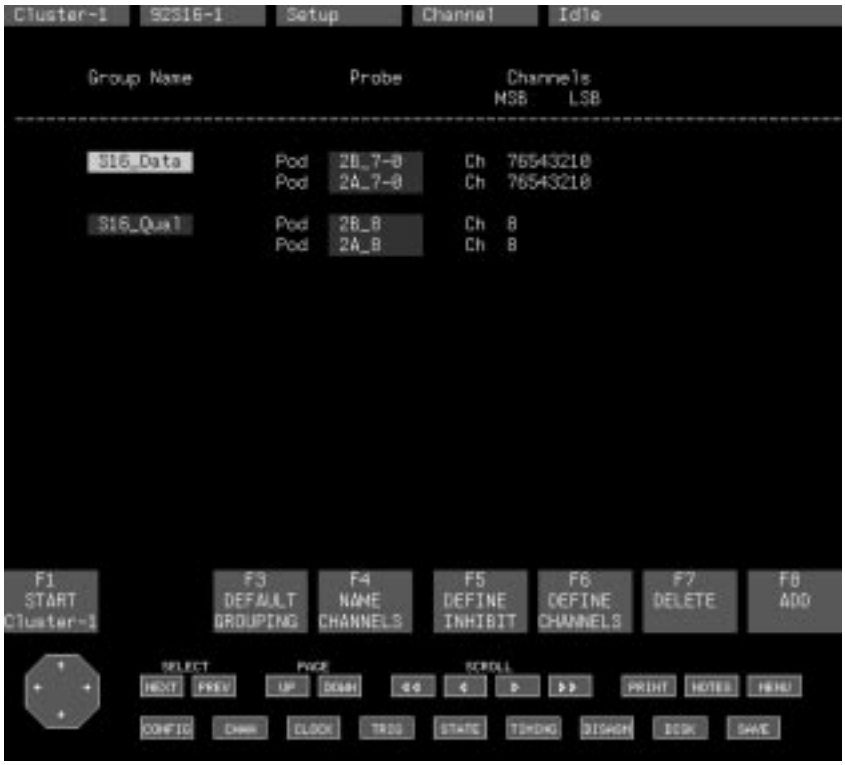


Figure 4–8: 92S16 Channel Menu

6. Press **F5: DEFINE INHIBIT**, press **F3: DEFAULT MASK** followed by **Return** to confirm.
7. Change the Inhibit field for both of A and B pods to **External = 0 Only**.
8. Change the Mask field of the clock channel (C) for both of the A and B pods to **Unmasked**. Press **F8: EXIT & SAVE**.
9. Press **F6: DEFINE CHANNELS** and press **F3: DEFAULT CHANNELS** followed by a **Return** to confirm.
10. Do the following for both of the A and B pods:
    a. Check that the Output Level field is **TTL**; change it if not.
    b. Check that the Clock Polarity field is the rising edge (⁄); change it if not.
    c. Check that the Clock Delay field is **0 ns**; change it if not.
11. Press **F8: EXIT & SAVE**.
12. Select the 92S16 Program menu.
13. Change the program menu to match Figure 4–9.

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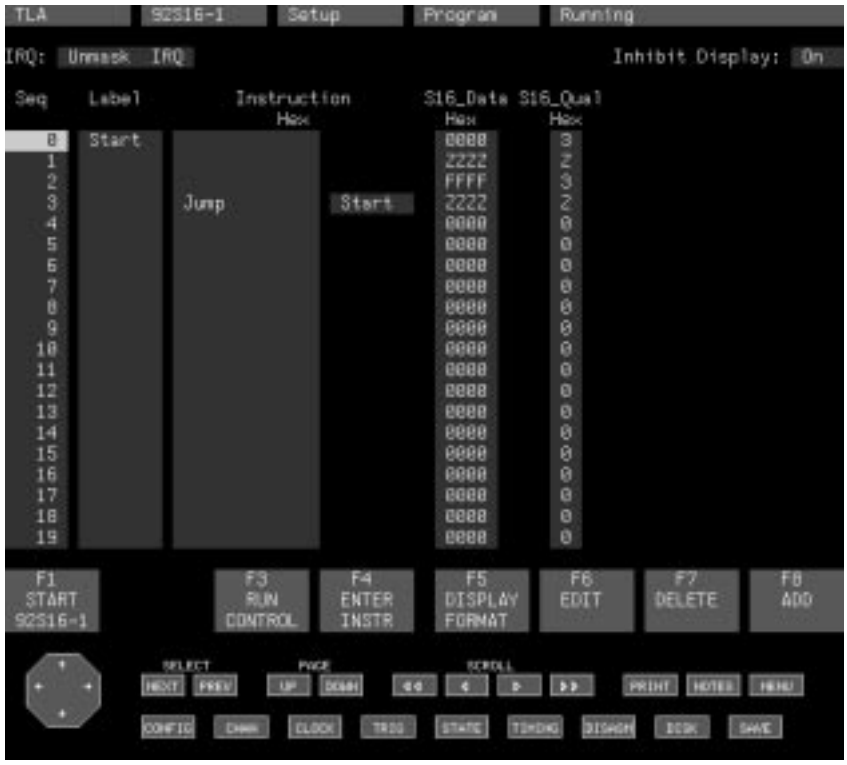


Figure 4–9: 92S16 Program Menu

92C96 Data Acquisition Setups. Use the following steps to set up the 92C96 Module. These setups are the initial setups used for the remainder of this procedure.

1. Select the 92C96 Module and select the Config menu.
2. Check that Software Support is General Purpose and Latch Mode is Off.
3. Select the 92C96 Channel menu.
4. Delete the Address and Control groups. Delete the D3 and D2 sections in the Data group.
5. Change the Radix field for the remaining Data group to **Hex**.
6. Press **F5: DEFINE THRESHOLD**. Check that the Threshold field for both Clock and Data are **TTL**. Press **F8: EXIT & SAVE**.
7. Press **F6: DEFINE CHANNELS**, then press **F5: DEFAULT ALL NAMES**. Check that the Polarity Field for all channels of all Sections are positive (+). Press **F8: EXIT & SAVE**.
8. Select the 92C96 Clock menu..

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9. Select **External** 92C96 Clock. Move the cursor to the External Clocks field and select the falling edge (\) of Clock_2. Move the cursor to the External Qualifiers field and select **C2_1_Brn**.

10. Select the 92C96 Trigger menu.

11. Change word recognizer value for the data channel group to **FFFF**.

Test Operation. Use the following steps to test the External Inhibit circuitry of the 92S16.

1. Disconnect the 50 Ω coaxial cable from the input of the pulse generator.

2. Connect a BNC-to-test point adapter to the output of the pulse generator. Connect the channel 1 scope probe to the test adapter. Check that the channel 1 V/div control is set at 1 V; adjust the output level of the pulse generator for a DC value 1 major division above the center graticule of the scope.

3. Connect the P6460 External Control Probe to pod D of the 92S16. Connect the ground leads of the P6460 to a ground on the pulse generator.

4. Attach the red (EXT INHIB) lead of the P6460 lead set to the test point adapter.

5. Press **F1: START**. The 92C96 should trigger and display an alternating pattern of 00s and FFs.

6. Using the channel 1 scope probe, adjust the output level of the pulse generator for a DC value 1 major division below the center graticule of the scope.

7. Press **F1: START**. Check that the 92C96 does not trigger and displays SLOW CLOCK. Check that the Status field displays Waiting for Enable. Press **F1: STOP**.

8. Select the 92S16 Module and select the Channel menu

9. Press **F5: DEFINE INHIBIT**. Change the Inhibit field for both of the A and B pods to **External = 1 Only**. Press **F8: EXIT & SAVE**.

10. Select the 92C96 Module and the State menu.

11. Press **F1: START**. The 92C96 should trigger and display an alternating pattern of 00s and FFs.

12. Using the channel 1 scope probe, adjust the output level of the pulse generator for a DC value one major division above the center graticule of the scope.

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13. Press **F1: START**. Check that the 92C96 does not trigger and displays SLOW CLOCK. Check that the Status field displays Waiting for Enable. Press **F1: STOP**.

14. Remove the P6460 red lead from the test point adapter.

External Jump Test

This test checks the 92S16's external jump circuitry.

92S16 Pattern Generation Setups. Use the following steps to set up the 92S16 Module for the External Jump Test.

1. Select the 92S16 Module and select the Config menu.

2. Press **F8: EXTERNAL CONTROL**. Move the cursor to the EXT Jump field and select **On**. Move the cursor down to the next field and select **P6460 Ext Jump = 1**. Press **F8: EXIT & SAVE**.

3. Select the 92S16 Channel menu.

4. Press **F5: DEFINE INHIBIT**. Change the Inhibit field for both of the A and B pods to Internal Only. Press **F8: EXIT & SAVE**.

5. Select the 92S16 Program menu.

6. Change the program menu to match Figure 4–10.

92C96 Data Acquisition Setups. Use the following steps to set up the 92C96 for the External Jump Test.

1. Select the 92C96 Module and select the Clock menu.

2. Check that the External Clocks are set for the falling edge (\) of Clock_2; change them if not. Move the cursor to the External Qualifiers field and turn the qualifiers off (the qualifier fields should be blank).

3. Select the 92C96 Trigger menu.

4. Change the word recognizer to 3333.

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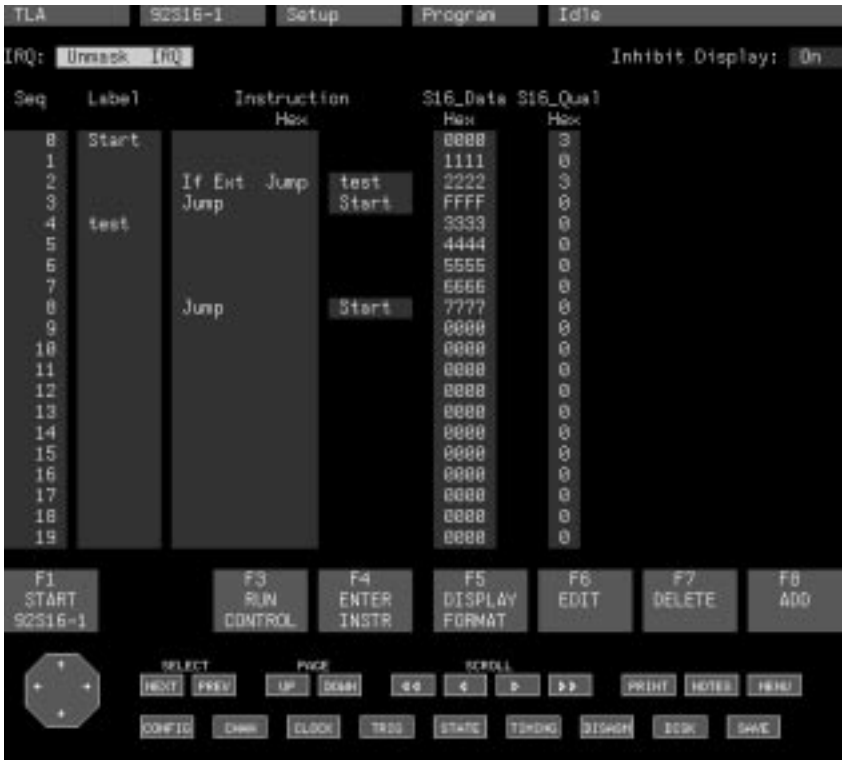


Figure 4–10: 92S16 Program Menu for the External Jump Test

Test Operation. Use the following steps to test the External Jump circuitry of the 92S16.

1. Adjust the output level of the pulse generator for a DC value 1 major division below the center graticule of the scope.
2. Attach the orange (EXT JUMP) lead of the P6460 lead set to the test point adapter.
3. Press **F1: START**. Check that the 92C96 does not trigger and the Status field displays Waiting for Trigger. Press **F1: STOP**.
4. Adjust the output level of the pulse generator for a DC value 1 major division above the center graticule of the scope.

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5. Press **F1: START**. Check that the 92C96 triggers and that the data is a repetitive sequence of the following:

   0000
   1111
   2222
   3333
   4444
   5555
   6666
   7777

6. Remove the P6460 orange lead from the test point adapter.

External IRQ And Qualifier Test

This test checks that the 92S16 will respond to an external interrupt and qualifier from the P6460 probe input.

92S16 Pattern Generation Setups. Use the following steps to set up the 92S16 Module for the External IRQ and Qualifier Test.

1. Select the 92S16 Module and select the Config menu.
2. Press **F8: EXTERNAL CONTROL**. Move the cursor to the EXT Jump field and select **Off**.
3. Move the cursor to the IRQ field and select **On**. The next fields should be set to: IRQ Jump is enabled when P6460 IRQ = ⨍ and P6460 Qualifier = X. Press **F8: EXIT & SAVE**.
4. Select the 92S16 Program menu.
5. Change the Sequence 2 instruction from If Ext Jump to If IRQ Jump.

92C96 Data Acquisition Setups. The 92C96 setups do not change from the previous test.

Test Operation. Use the following steps to test the External IRQ and Qualifier circuitry of the 92S16.

1. Reconnect the 50 Ω coaxial cable to the pulse generator input.
2. Adjust the sinewave generator and pulse generator output levels for a 2 V peak-to-peak, 10 MHz signal centered around the 1.4 V threshold level.
3. Attach yellow (IRQ) and green (IRQ QUAL) leads of the P6460 lead set to the test point adapter.
4. Select the 92C96 Module and select the State menu.

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5. Press **F1: START**. Check that the 92C96 triggers and the data is a repetitive sequence of the following:

   0000
   1111
   2222
   3333
   4444
   5555
   6666
   7777

6. Select the 92S16 Module and select the Config menu.

7. Press **F8: EXTERNAL CONTROL**. Move the cursor to the last field in the IRQ group and select **P6460 Qualifier = 0**. Press **F8: EXIT & SAVE**.

8. Select the 92C96 Module and select the State menu.

9. Press **F1: START**. Check that the 92C96 triggers and the data is a repetitive sequence of the following:

   0000
   1111
   2222
   3333
   4444
   5555
   6666
   7777

10. Select the 92S16 Module and select the Config menu.

11. Press **F8: EXTERNAL CONTROL**. Move the cursor to the second field in the IRQ group and select the falling edge (\) of the P6460 IRQ signal. Move the cursor to the last field in the IRQ group and select **P6460 Qualifier = 1**. Press **F8: EXIT & SAVE**.

12. Select the 92C96 Module and select the 92C96 State menu.

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13. Press **F1: START**. Check that the 92C96 triggers and the data is a repetitive sequence of the following:

    0000
    1111
    2222
    3333
    4444
    5555
    6666
    7777

14. Remove the P6460 yellow and green leads from the test point adapter.

External Pause Test

This test checks the External Pause circuitry of the 92S16.

92S16 Pattern Generation Setups. Use the following steps to set up the 92S16 Module for the External Pause Test.

1. Select the 92S16 Module and select the Config menu.
2. Change the Clock field to Internal 1 ms.
3. Press **F8: EXTERNAL CONTROL**. Move the cursor to the IRQ field and select **Off**.
4. Move the cursor to the Pause field and select **On**. Move the cursor down to the next field and select **P6460 Pause = 1**. Press **F8: EXIT & SAVE**.
5. Select the 92S16 Program menu.
6. Change the program menu to match Figure 4–11.

92C96 Data Acquisition Setups. The 92C96 setups do not change from the previous test.

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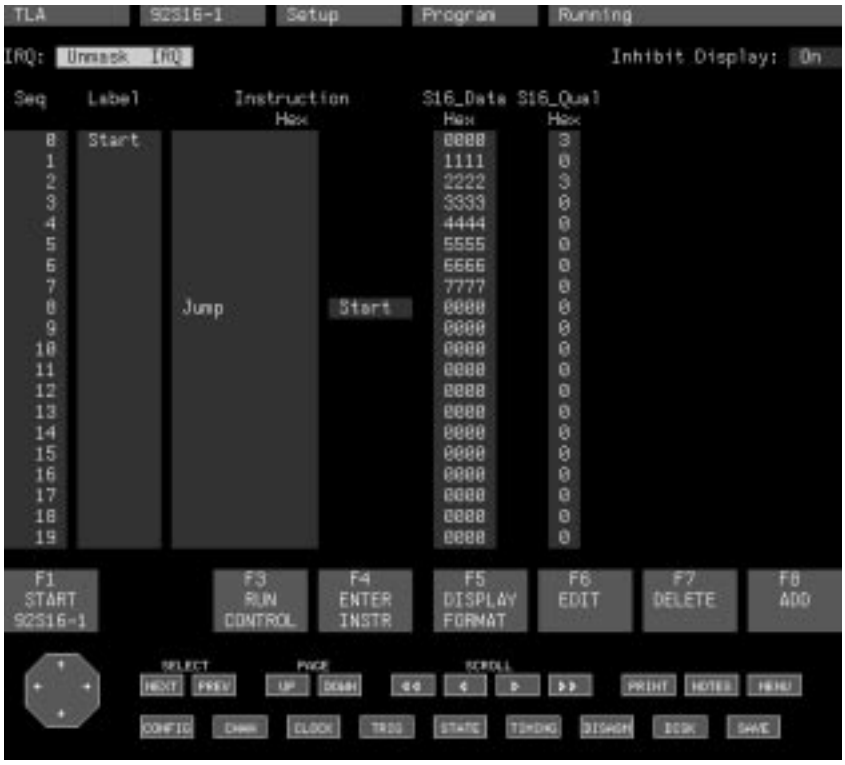


Figure 4–11: 92S16 Program Menu for the External Pause Test

Test Operation. Use the following steps to test the External Pause circuitry of the 92S16.

1. Disconnect the 50 Ω coaxial cable from the pulse generator.
2. Adjust the output level of the pulse generator for a DC value one major division above the center graticule of the scope.
3. Attach the brown (PAUSE) lead of the P6460 lead set to the test point adapter.
4. Press **F1: START**. Check that the 92C96 does not trigger and displays SLOW CLOCK. Check that the Status field displays Waiting for Trigger.
5. Press **F1: STOP**.
6. Adjust the output level of the pulse generator for a DC value one major division below the center graticule of the scope.

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7. Press **F1: START**. Check that the 92C96 triggers and the data is a repetitive sequence of the following values:

   0000
   1111
   2222
   3333
   4444
   5555
   6666
   7777

   It may take time for the acquisition memory to fill and the state table to appear.

8. Remove the P6460 brown lead from the test point adapter.

External Start Test

This test checks the External Start circuitry of the 92S16.

92S16 Pattern Generation Setups. Use the following steps to set up the 92S16 Module for the External Start Test.

1. Select the 92S16 Module and select the Config menu.
2. Change the Clock field to Internal 10 µs.
3. Press **F8: EXTERNAL CONTROL**. Move the cursor to the Pause field and select **Off**.
4. Move the cursor to the Ext Start field and select **On**. The next field should be set for: Starts when P6460 EXT START = ⟋. Press **F8: EXIT & SAVE**.
5. Select the 92S16 Program menu.
6. Change the S16_Qual fields by replacing the 0 value with a 3 in sequences 4 and 6.

92C96 Data Acquisition Setups. The 92C96 setups do not change from the previous test.

Test Operation. Use the following steps to test the External Start circuitry of the 92S16.

1. Reconnect the 50 Ω coaxial cable to the pulse generator input.
2. Adjust the sinewave generator and the pulse generator output for a 2 V peak-to-peak, 35 MHz signal centered around the 1.4 V threshold level (15 ns positive pulse width).

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3. Press **F1: START**. Check that the 92C96 does not trigger.
4. Attach the black (EXT START) lead of the P6460 lead set to the test point adapter.
5. Check that the 92C96 triggers and the data is a repetitive sequence of the following values:

   0000
   1111
   2222
   3333
   4444
   5555
   6666
   7777

6. Remove the P6460 black lead from the test point adapter.

Trigger Out Test

This test checks that the 92S16 can generate a Trigger Out signal.

92S16 Pattern Generation Setups. Use the following steps to set up the 92S16 Module for the Trigger Out Test.

1. Select the 92S16 Module and select the Config menu.
2. Change the Clock field to Internal 100 ns.
3. Press **F8: EXTERNAL CONTROL**. Move the cursor to the Ext Jump field and select **Off**. Press **F8: EXIT & SAVE**.
4. Select the 92S16 Program menu.
5. Change the program menu to match Figure 4–12.
6. Select the 92S16 Monitor menu.
7. Turn the Trace On.

92C96 Data Acquisition Setups. The 92C96 setups do not change from the previous test.

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Figure 4–12: 92S16 Program Menu for the Trigger Out Test

Test Operation. Use the following steps to test the Trigger Out circuitry of the 92S16.

1. Connect a P6041 (Sync Out Cable) to the SMB connector of the 92S16 (J260). Connect the other end of the P6041 probe directly to the channel 1 input BNC of the scope.
2. Press **F1: START**. The 92S16 Status field will change from Start in Progress to Running.

NOTE. *The scope should be set for 1 V/div and 20 ms/div to display the trigger out signal.*

---

3. Press **F2: CONTINUE TRACE**. Check that the 92S16 displays the pattern traces on the screen and a Trigger Out signal is displayed on the scope.
4. Press **F1: STOP**.
5. Turn the Trace Off.

This completes the 92S16 functional checks.

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P6463A Probe

The functional checks are a limited number of tests that allow you to check the probe's operational status. The functional checks test major portions of the probe, such as circuitry supporting probe ID readout, output clock, inhibit channels, and 9- & 16-channel modes.

Equipment Required

To perform the functional checks, you will need the following equipment:

- TLA 510 or 520 system unit and X Terminal
- 92C96 Data Acquisition Module
- 92S16 Pattern Generation Module
- P6463A probe with lead set
- Tektronix 2465B Oscilloscope (or equivalent) and two P6137 probes
- Digital Multimeter
- PS282A Power Supply (or equivalent)
- General Purpose Acquisition Fixture (refer to *Test Fixtures* on page 5–27)
- Decoupling Fixture (refer to *Test Fixtures* on page 5–27)

Equipment Setup

Before performing any procedures, there are some initial steps you must follow to prepare for the functional checks. It is recommended that you start at the beginning of these functional checks and work through them all in order.

Probe Connection

The steps listed here allow you to connect the acquisition and pattern generation probes together and set the P6463A probe for 16-channel mode.

1. Connect the positive side of the decoupling fixture to the positive side of the power supply. Connect the negative side of the fixture to the negative side of the power supply. Note the polarity of the tantalum capacitor.



WARNING. *Incorrectly connecting the power to the decoupling fixture can cause the tantalum capacitor to burn or explode.*

2. Connect the black (VL) leads of the pattern generator probe to the common or ground output of the decoupling fixture. Connect the 18-inch black lead of the acquisition fixture to the ground or common output of the power supply.
3. Connect the red (VH) leads of the pattern generator probe to the positive side of the decoupling fixture.

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4. Connect the 92C96 podlets to the P6463A leads through the General Purpose Acquisition Fixture according to Table 4–5. Ensure that the ground side of the 92C96 podlets are connected to the common (ground) side of the Acquisition Fixture. In the same respect, ensure that the signal side of the 92C96 podlets are connected to the signal side of the P6463A probe connectors.

5. Set the P6463A probe for 16-channel operation (jumpers J115 and J570 shorting pins 1 and 2).

Table 4–5: Acquisition Fixture Connections

92C96 Channel	Acq Fix Pin #	P6463A	92S16
Clock_2	39	CLK	POD A
	37		
D1_7_Vlt	35	15	POD A
D1_6_Blu	33	14	POD A
D1_5_Grn	31	13	POD A
D1_4_Ylw	29	12	POD A
D1_3_Org	27	11	POD A
D1_2_Red	25	10	POD A
D1_1_Brn	23	9	POD A
D1_0_Blk	21	8	POD A
	19		
	17		
D0_7_Vlt	15	7	POD A
D0_6_Blu	13	6	POD A
D0_5_Grn	11	5	POD A
D0_4_Ylw	9	4	POD A
D0_3_Org	7	3	POD A
D0_2_Red	5	2	POD A
D0_1_Brn	3	1	POD A
D0_0_Blk	1	0	POD A

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Functional Checks

These checks provide a method for functionally testing the following areas of the P6463A probe:

- Probe ID circuitry
- Bit independence and functionality of inhibit signals
- 9- and 16-channel modes of operation
- User remote inhibit

Probe ID Circuitry Check

Perform the following steps the check the P6463A ID circuitry.

1. Connect the P6463A probe to Pod A on the 92S16; the lead set should be connected to the Acquisition Fixture as described earlier.
2. Select the 92S16 Config menu. As you connect the probe to (and disconnect from) the module, check the upper left of the display for the following responses:

```
Module: 92S16 Pod: 2A Probe Connected
Module: 92S16 Pod: 2A Probe Disconnected
```

3. With the probe connected, press and release the probe's ID button while checking for the following responses on the terminal:

```
Module: 92S16 Pod: 2A Pod ID Pressed
Module: 92S16 Pod: 2A Pod ID Released
```

This completes the functional check of the probe ID circuitry.

Bit Independence and Inhibit Signal 0 – 7 Check

Perform the following steps to check the bit independence and inhibit signals 0 through 7.

1. Select the Sys Config menu from the Menu Selection Overlay.
2. Press **F6: DEFINE CLUSTER**, then press **F2: CLUSTER ALL**. Press **F8: EXIT & SAVE**.
3. Select the Cluster Setup menu from the Menu Selection Overlay. Set the Start Mode field to ATE.

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4. Select the 92C96 Channel menu. Program the menu with the information shown in Figure 4–13. Use **F8: ADD** and **F7: DELETE** to obtain this setup.

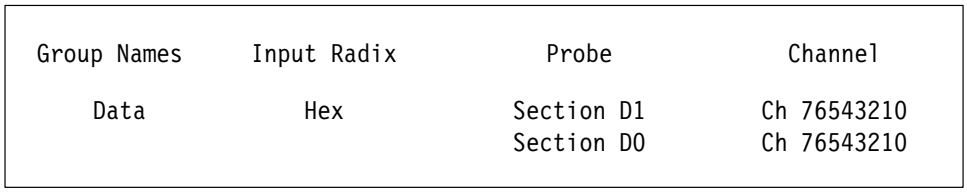


Figure 4–13: 92C96 Channel Menu for the Bit Independence and Inhibit Signal 0 through 7 Check

5. Select the 92C96 Clock menu. Program the menu with the following information:

   ```
   Module Clock: External

   External Clocks: \ Clock_2
   ```

6. Select the 92C96 Trigger menu. Program the menu with the following information:

   ```
                    Data

   If Word #1 =     OOFF
   Then Trigger and Store
   ```

7. Select the 92S16 Config menu. Program the menu with the following information. Setting the clock rate to a slow value allows the P6463A channels to stabilize (after being tri-stated) to ensure that the acquired data is valid.

   ```
   Clock: Internal 1 ms
   ```

8. Select the 92S16 Channel menu. Program the menu as shown in Figure 4–14. Use **F8: ADD** and **F7: DELETE** to obtain this setup.

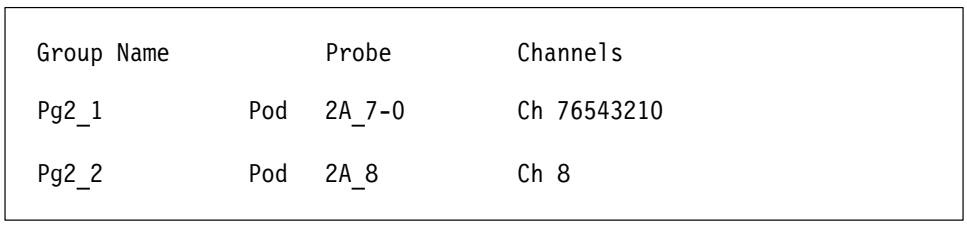


Figure 4–14: 92S16 Channel Menu

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9. Press **F5: DEFINE INHIBIT** and program the menu as shown in Figure 4–15 for pod 2A. (These tests assume the P6463A is attached to pod A).

C	Pod_2A_C	Masked
8	Pod_2A_8	Masked
7	Pod_2A_7	Unmasked
6	Pod_2A_6	Unmasked
5	Pod_2A_5	Unmasked
4	Pod_2A_4	Unmasked
3	Pod_2A_3	Unmasked
2	Pod_2A_2	Unmasked
1	Pod_2A_1	Unmasked
0	Pod_2A_0	Unmasked

Figure 4–15: Defining Inhibit Signals

10. Press **F8: EXIT & SAVE**; Select the 92S16 Program menu.

11. Press **F5: DISPLAY FORMAT** and program the following information:

Order	Group Name	Radix
0	Pg2_1	Hex
1	Pg2_2	Bin

12. Press **F8: EXIT & SAVE**; enter the pattern shown in Figure 4–16 for the 92S16 program:

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Figure 4–16: 92S16 Program Menu

13. Press **F3: RUN CONTROL** and set the 92S16 Start Location as Seq 0. Press **F8: EXIT & SAVE**.

14. After entering the pattern shown in Figure 4–16, move the cursor back to sequence 11 and type all Zs in Pg2_1 and Pg2–2. Repeat this for sequences 12 and 13. These sequences will then be displayed as:

11	ZZ	0
12	ZZ	1
13	ZZ	0

15. Select the 92C96 Monitor menu. Press **F1: START**. Wait until the state display appears and then check the resulting display for the data pattern shown in Figure 4–17.

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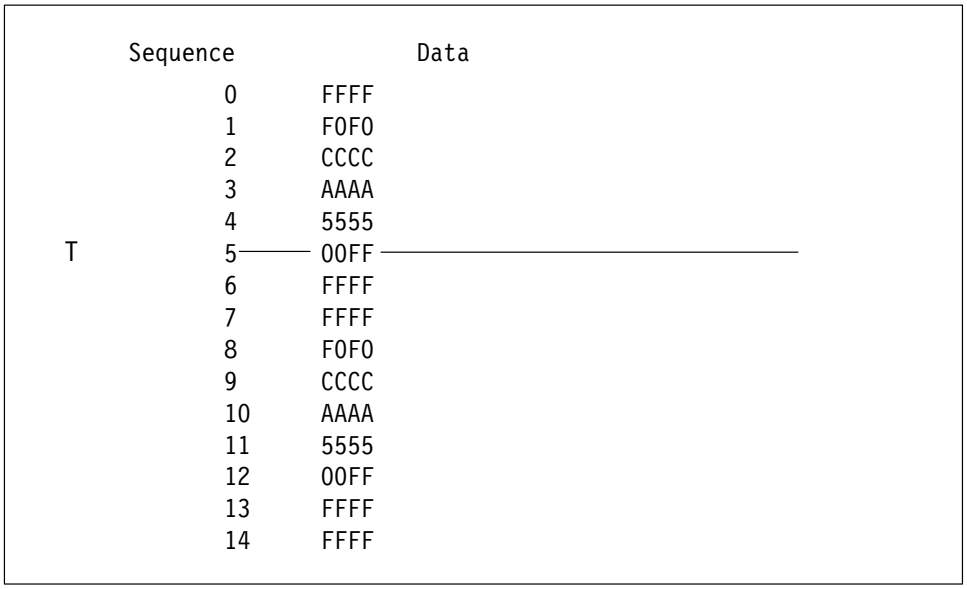


Figure 4–17: Results Of Checking Bit Independence and Inhibit Signals 0 – 7

This completes the test for bit independence; it also tests the functionality of the inhibit signals for probe channels 0, 1, 2, 3, 4, 5, 6, and 7.

Bit Independence and Inhibit Signal 8 – 15 Check

Perform the following steps to check the bit independence and inhibit signals 8 through 15.

1. Select the 92C96 Trigger menu.
2. Program the trigger menu with the information shown in Figure 4–18.

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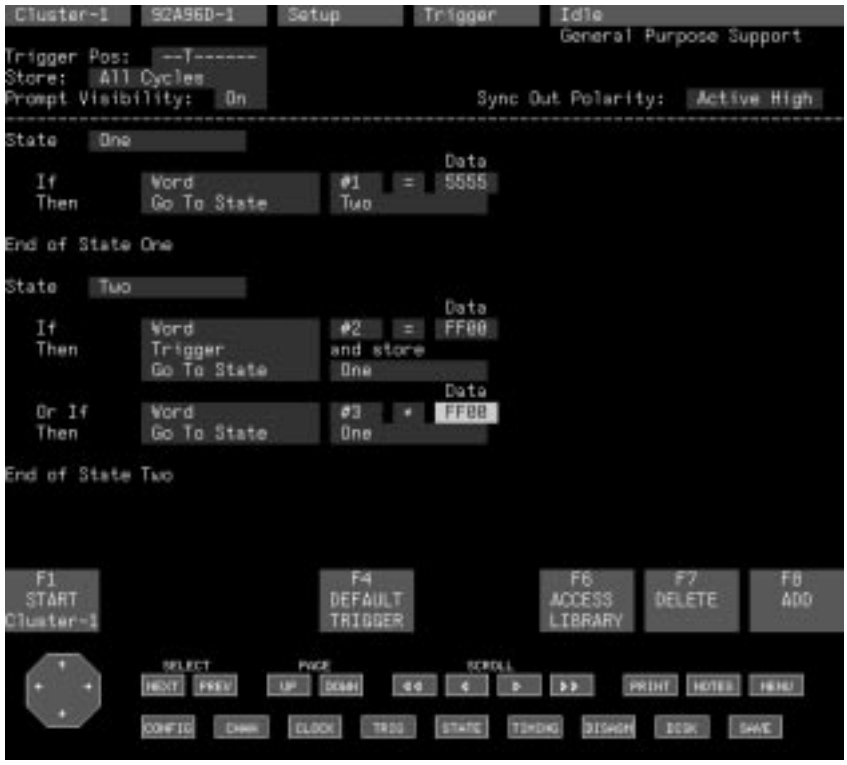


Figure 4–18: 92C96 Trigger Menu

3. Select the 92S16 Channel menu. Press **F5: DEFINE INHIBIT** and program the menu as shown in Figure 4–19 for pod 2A.

Channel	Mask	
C	Pod_2A_C	Masked
8	Pod_2A_8	Unmasked
7	Pod_2A_7	Masked
6	Pod_2A_6	Masked
5	Pod_2A_5	Masked
4	Pod_2A_4	Masked
3	Pod_2A_3	Masked
2	Pod_2A_2	Masked
1	Pod_2A_1	Masked
0	Pod_2A_0	Masked

Figure 4–19: Defining Inhibit Signals for Signals 8 – 15 Check

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4. Press **F8: EXIT & SAVE**; press **F6: DEFINE CHANNELS** to display the Channel Definition overlay. Program the overlay with the following:

   ```
   Pod: 2A
   Output Level: TTL
   Clock Polarity: ⎍
   Clock Delay: 0 ns
   ```

5. Press **F8: EXIT & SAVE** to exit the overlay.

6. Select the 92C96 Monitor menu. Press **F1: START**. When the 92C96 triggers wait for the state display to appear. Check the resulting display for the data pattern shown in Figure 4–20.

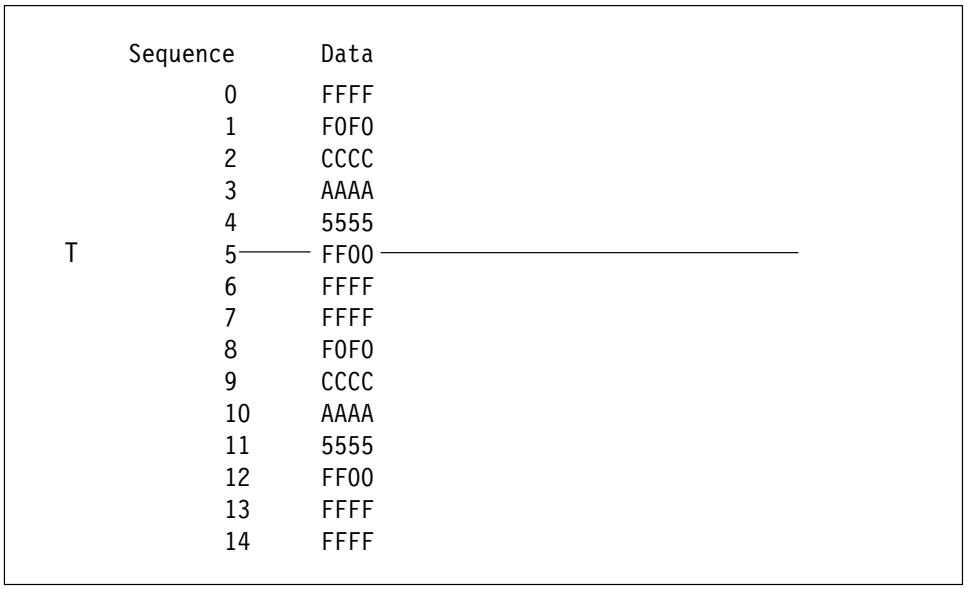


Figure 4–20: Results of Checking Inhibit Signals 8 – 15

This completes testing of the inhibit signals for probe channels 8, 9, 10, 11, 12, 13, 14, and 15.

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User Remote Inhibit Check

Perform the following steps to check the user remote inhibit function.

1. Select the 92S16 Program menu. Remove the tri-state mask from sequences 11 through 13 by typing over these sequences with the following:

```
BEFORE:                    AFTER:

11    00    Z              11    00    0
12    FF    Z              12    FF    1
13    FF    Z              13    FF    0
```

2. Select the 92C96 Trigger menu. Program the menu with the following changes.

```
State One

                      Data
If Word #1 =          FF55
Then Go To State Two

End of State One
```

***NOTE**. State Two remains unchanged.*

3. Select the 92C96 Monitor menu. Press **F1: START**. The 92C96 monitor menu should display the following message at the upper right:

```
Waiting For Trigger
```

4. Refer to Figure 4–21. Using a jumper lead, short pins 1 and 2 of TP250 for a few seconds. TP250 is located on the probe's ID/Logic Board. The 92C96 should trigger and cause the data pattern shown in Figure 4–22 to be displayed. Verify that the pattern at and after the trigger match the data shown in Figure 4–22. The samples displayed prior to the trigger point may be different than that shown in Figure 4–22.

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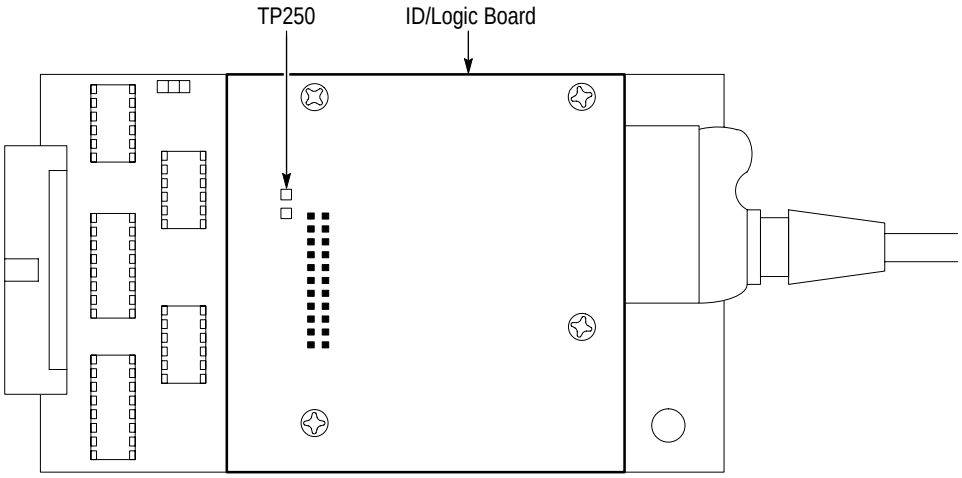


Figure 4–21: Location of Test Point 250

	Sequence	Data
	1012	FFFF
	1013	F0F0
	1014	CCCC
	1015	AAAA
	1016	5555
	1017	0000
	1018	FFFF
	1019	FFFF
	1020	F0F0
	1021	CCCC
	1022	AAAA
	1023	5555
T	1024	FF00
	1025	FFFF
	1026	FFFF
	1027	FFF0
	1028	FFCC
	1029	FFAA
	1030	FF55
	1031	FF00

Figure 4–22: Results of Checking the User Remote Inhibit Using TP250

This completes the check of the user remote inhibit function.

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Nine Channel Mode Check

Perform the following steps to check the 9-channel mode function.

1. Remove the probe's upper case half and move jumpers J115 and J570 to select the 9-channel mode (pins 2 & 3 shorted).
2. Select the 92S16 Program menu. Change the Inhibit Display field to Off and press **F7: DELETE** to delete sequences to obtain the pattern shown in Figure 4–23.



Figure 4–23: Reprogramming the 92S16 Program Menu for 9-Channel Checks

3. Select the 92C96 Channel menu. Program the menu with the information shown in Figure 4–24.

Group Names	Input Radix	Probe	Channel
Data	Hex	Section D1	Ch 0
		Section D0	Ch 76543210

Figure 4–24: Reprogramming the 92C96 Channel Menu for 9-channel Checks

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4. Select the 92C96 Trigger menu. Program the menu with the information shown in Figure 4–25.

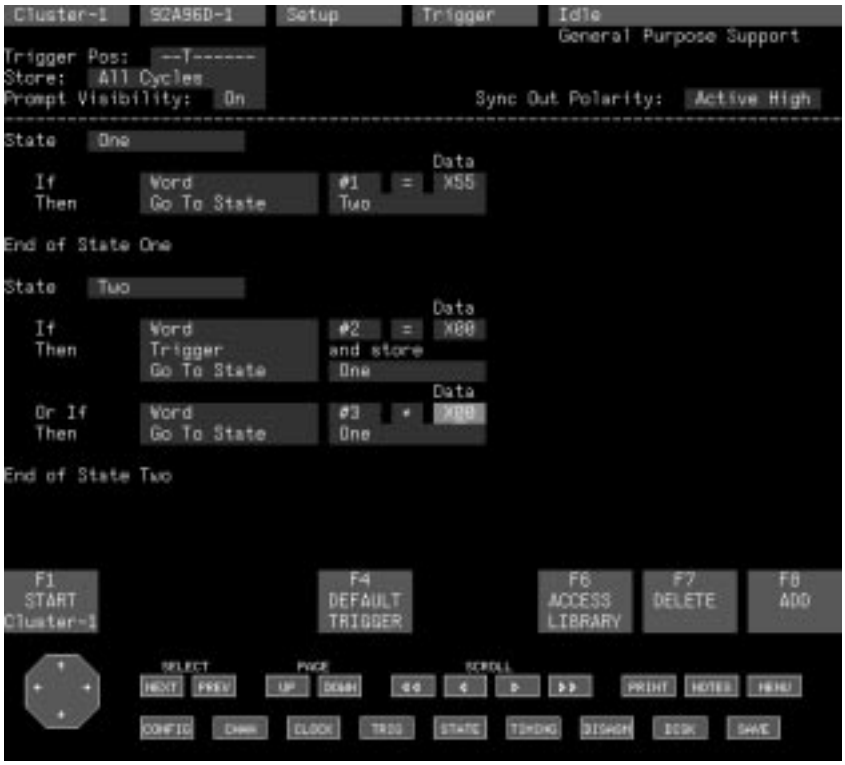


Figure 4–25: Reprogramming the Trigger Menu For 9-channel Checks

5. Select the 92C96 Monitor menu. Press **F1: START**. When the 92C96 triggers, check the resulting display for the data pattern shown in Figure 4–26.

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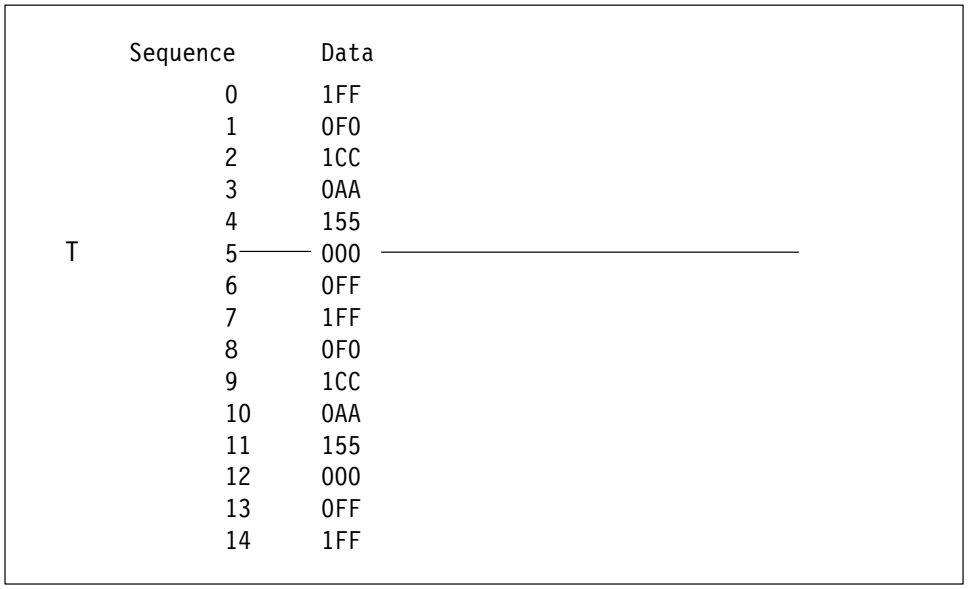


Figure 4–26: Results of Checking the 9-channel Mode of Operation

This completes the check of the 9- and 16-channel modes of operation.

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Performance Verification

This section verifies that the logic analyzer meets the performance requirement specifications. These specifications are listed under the Performance Requirements column in the chapter *Specifications* of this manual.

TLA 510 & 520 System Unit

This procedure verifies the following TLA 510 or 520 system unit power requirements:

Primary Power Input

115 VAC, Single Phase:	90-127 VAC @ < 8 A
230 VAC, Single Phase with System Unit Option A1-A5:	180-250 VAC @ < 4 A

Equipment Required

You will need the following equipment to perform this procedure:

- TLA 510 or 520 system unit
- X Terminal
- 92C96 Data Acquisition Module
- Valhalla Scientific Model 2100 Wattmeter or equivalent

Test Procedure

The power requirements for the TLA 510 or 520 system unit depend upon the module configuration and the power cord used.

1. Determine the type of power cord for your system unit.
2. According to the type of power cord used, check that the AC line fuse is appropriate 8 A slow-blow for 115 VAC or 5 A slow-blow for 230 VAC.
3. Connect the wattmeter in series with the power cord to the TLA 510 or 520 system unit.
4. Power up the terminal and the system unit.

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5. Select the 92C96 Trigger menu and change the trigger action to **Do Nothing**, and press **F1:START**.

6. Check that the AC line current indicated by the wattmeter meets the specification above, for the appropriate range of voltage.

This completes the TLA 510 or 520 system unit performance checks.

92C96 Acquisition Module

These procedures verify that the 92C96 Module meets the performance requirement specifications. These specifications are listed under the Performance Requirements column in the *Specifications* chapter.

The following performance checks are included in this section:

- Data Threshold Accuracy
- Clock Threshold Accuracy
- Minimum Pulse Width Capture
- Minimum Glitch Width/Minimum Data Amplitude
- Setup and Hold Time
- Counter and Timer Accuracy
- Maximum Synchronous Transaction Rate/Maximum External Clock Rate/Minimum Time Between Clock Edges
- Module Sync Out
- Module Sync Out Delay

All of the hardware and system setups build upon the previous procedures. The individual procedures only include the changes from the previous setup. For these reasons, the procedures should be performed consecutively from start to finish.

Some of the test procedures involve complex menu setups. If you will be using these procedures again at a later time or date, it is recommended that you save the menu setups on the system unit's hard or floppy disks. Refer to the *TLA 510 & 520 User Manual* for instructions on saving menu setups.

Allow a 15 minute warm-up period for the TLA 510 or 520 and all test equipment before performing any of these procedures.

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Equipment Required

The following list of equipment is necessary to complete the performance checks.

- TLA 510 or 520 system unit
- X Terminal
- 92C96 Data Acquisition Module (with standard accessories)
- P6041 Passive Probe (Sync Out Cable)
- Two-channel, 400 MHz Oscilloscope (Tektronix 2465B with standard probes)
- One FET Oscilloscope Probe (with short ground pin) (Tektronix P6201)
- Two 10 MΩ Oscilloscope Probes (Tektronix P6137)
- 5 V, 1.6 Amp DC Power Supply (Tektronix PS282)
- 4½ digit, ±0.05% VDC Digital Voltmeter
- Two Pulse Generators, 250 MHz, with Back Termination
- 125 MHz, High Stability Time Base Universal Counter
- Ground Strap (included with the 92C96 Module)
- Two 10-inch, 50 Ω BNC Coaxial Cables (Tektronix part number 012-0208-XX)
- One 24-inch, 50 Ω BNC Coaxial Cable (Tektronix part number 012-1342-XX)
- One 72-inch, 50 Ω BNC Coaxial Cable (Tektronix part number 012-0204-XX)
- Two Male-Male BNC Connectors (Tektronix part number 103-0029-XX)
- Two Female-Female BNC Connectors (Tektronix part number 103-0028-XX)
- BNC T Connector (Tektronix part number 103-0030-XX)
- Two Female BNC to Dual Banana Plug Connectors (Tektronix part number 103-0090-XX)
- 50 Ω Feed-through Termination (Tektronix part number 011-0049-XX)
- Two Dual-Lead Adapters (Tektronix part number 015-0325-XX)
- 92C96 Acquisition Fixture[1]
- BNC-to-Test Point Adapter[2]

1 **You must build a 92C96 Acquisition Fixture as described under Test Fixtures on page 5–27.**

2 **You must build a BNC-to-Test Point Adapter as described under Text Fixtures on page 5–27 to connect the output of the pulse generator to the Clock probes.**

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Data Threshold Accuracy

This procedure verifies the data channel input threshold levels; including TTL, CMOS, ECL, and all VAR (variable) threshold levels.

***NOTE**. The data and clock threshold accuracy tests rely on random noise. Perform these tests in a TLA 510 or 520 containing only a single 92C96 Module. Other modules in the system unit degrade the test accuracy.*

Equipment Setup

Use the following hardware and system setups for these procedures. Refer to Figure 4–27 for details of the setup while reading these setup instructions.

1. Connect a ground strap between the chassis of the TLA 510 or 520 system unit and the test equipment (test equipment must be earth-grounded to the TLA 510 or 520 system unit).
2. Connect the positive output of a variable DC voltage source to the signal side of the 92C96 Acquisition Fixture.
3. Connect two 92C96 8-channel probes to the 92C96 Acquisition Fixture. Begin with sections A0 and A1 of the orange 92C96 probe.

***NOTE**. To avoid damaging the acquisition probes, do not let them hang by the podlets or leadsets. Place them on a flat surface.*

4. Connect the 92C96 Module Sync Out signal (from J900) to the input of a digital voltmeter (or digital multimeter). Adjust the voltmeter DC voltage range for greatest accuracy.

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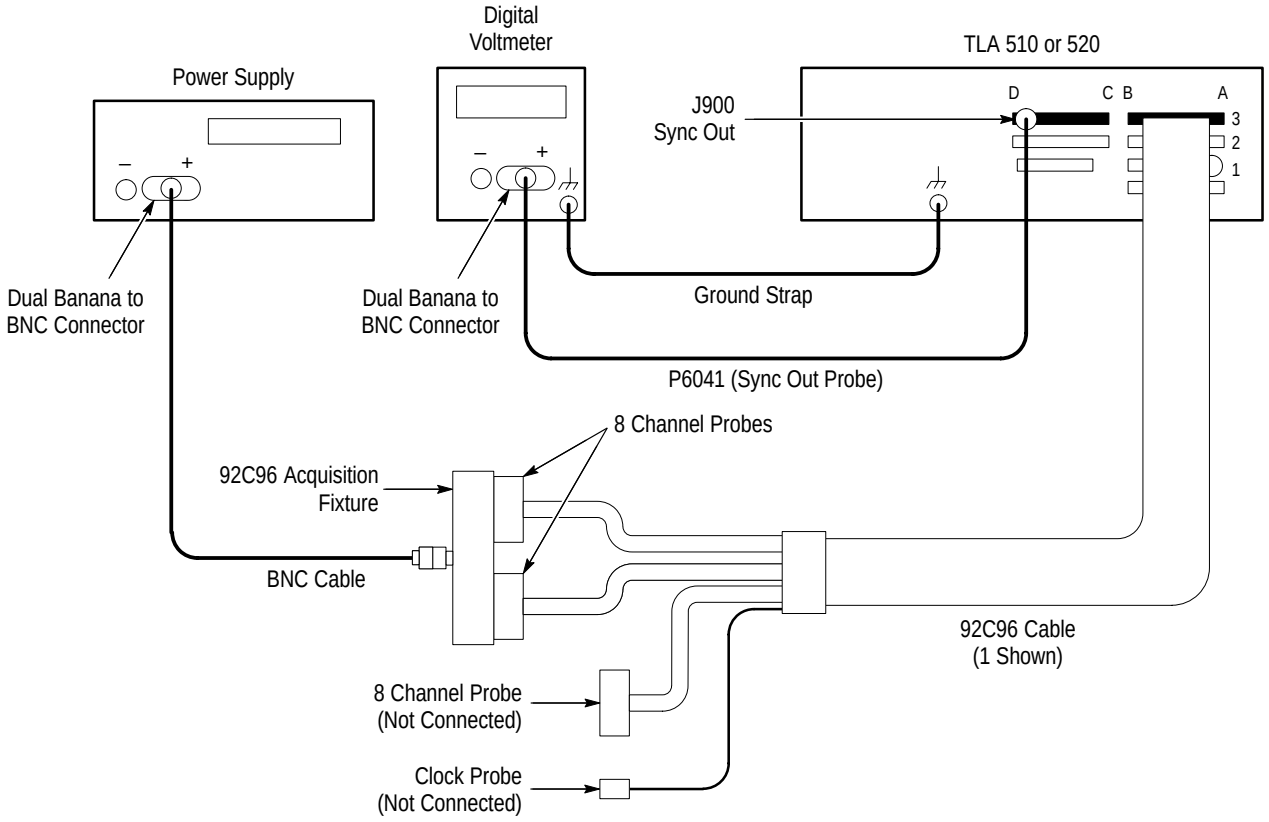


Figure 4–27: Data Threshold Accuracy Equipment Setup

Test Procedure

Use the following steps to verify the threshold level accuracy performance for each data channel.

1. Select the 92C96 Channel menu.
2. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.
3. Set Data Thresholds to your desired type and level, for example TTL +1.5 V, and press **F8: EXIT & SAVE**.
4. Select the 92C96 Trigger menu. Program the trigger menu as shown next.

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```
Trigger Pos: T--------
Store: All Cycles
Prompt Visibility: On
------------------------------------------------------------------
State   One

  If      Channel              XX            is Asserted
  Then    Pulse Signal         Module Sync Out

End of State One
```

Channel XX is defined as the desired test channel (section_channel); for example, A0_0. This Trigger program generates a Sync Out signal that reflects the status of the input channel (A0_0 in this example).

5. Press **F1: START** to enable the Sync Out signal.
6. Adjust the variable DC voltage source (near the 92C96 threshold setting) until the Sync Out signal displayed on the DVM measures approximately +2.5 V. It will be difficult to achieve a stable reading.
7. Disconnect the variable DC voltage source and digital voltmeter from their respective connections.
8. Connect the variable DC voltage source to the digital voltmeter.
9. Verify that the DC voltage source level is the threshold voltage ±0.075 V; for example, +1.5 V ±0.075 V for TTL.
10. Reconnect the variable DC voltage source to the 92C96 Acquisition Fixture and the digital voltmeter to the 92C96 Module Sync Out signal (J900).
11. Press **F1: STOP**.
12. Repeat steps 4 through 11 for each remaining channel of sections A0 and A1. Then repeat again for each data channel of sections A2, A3, D0, D1, D2, D3, C0, C1, C2, and C3 (replace tested sections connected to the 92C96 Acquisition Fixture with sections to be tested, up to two sections at a time). Then repeat steps 1 through 11 for each desired threshold type and level selection.

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Clock Threshold Accuracy

This procedure verifies the clock channel input threshold levels; including TTL, CMOS, ECL, and all VAR (variable) threshold levels.

Equipment Setup

Use the following hardware and system setups for these procedures. Refer to Figure 4–28 for details of the setup while reading these setup instructions.

1. Connect the positive output of a variable DC voltage source to a digital voltmeter.
2. Set the digital voltmeter range for greatest accuracy.
3. Connect Clock_3 of the gray 92C96 probe to the middle of the 92C96 Acquisition Fixture. Then connect two of the 8-channel probes from the gray probe to the 92C96 Acquisition Fixture, one on each side of the clock podlet (these acquisition groups merely provide more ground connections).

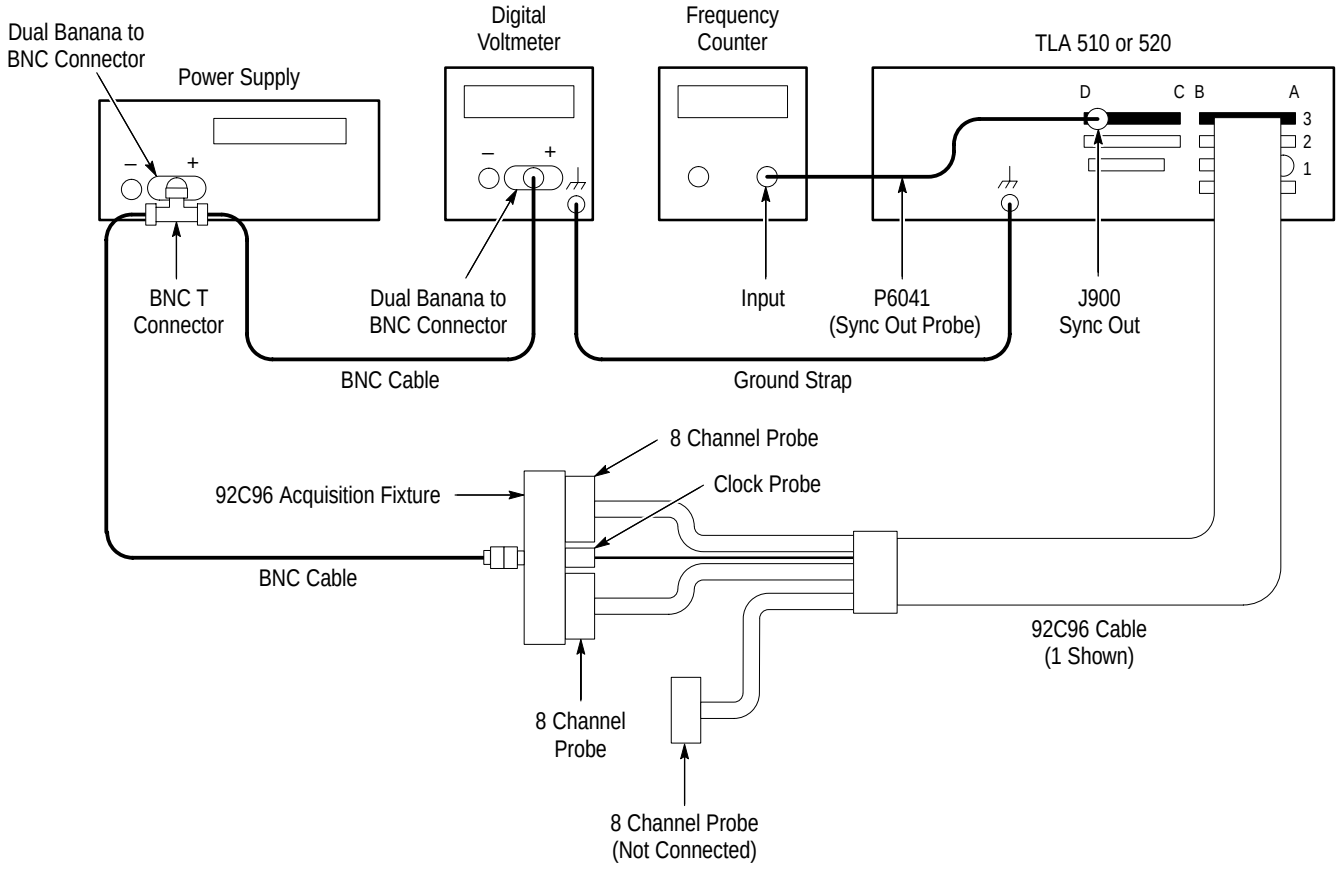


Figure 4–28: Clock Threshold Accuracy Equipment Setup

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4. Connect both the voltage source and the voltmeter to the 92C96 Acquisition Fixture.

5. Connect a counter to the 92C96 Module Sync Out signal (J900) using the P6041 Probe. Adjust the counter frequency range to measure an approximately 10 MHz signal.

Test Procedure

Use the following steps to verify the threshold level accuracy performance for each clock channel.

1. Select the 92C96 Trigger menu. Program the Trigger menu as shown next.

```
Trigger Pos: T--------
Store: All Cycles
Prompt Visibility: On
------------------------------------------------------------------

State   One

  If      Anything
  Then    Pulse Signal          Module Sync Out
          Go To State           Two

End of State One

State   Two

  If      Anything
  Then    Go To State           One

End of State Two
```

This trigger program inhibits a trigger from occurring and causes the Module Sync Out signal to pulse.

2. Select the 92C96 Channel menu.

3. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.

4. Set Clock Threshold to your desired type and level, for example TTL +1.5 V, and press **F8: EXIT & SAVE**.

5. Select the 92C96 Clock menu.

6. Select External clocking and the clock channel under test, for example Clock_3, as the single Sample Clock source (no qualifiers) in the clock equation.

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7. Press **F1: START** to start the 92C96 Module.
8. Adjust the variable DC voltage source until the frequency counter reads a maximum frequency indicating a voltage around the selected threshold.
9. Verify that the voltmeter reading is within ±75 mV of the selected threshold level; for example, +1.5 V ±0.075 V for TTL.
10. Press **F1: STOP**.
11. Repeat steps 5 through 10 for each remaining clock channel (disconnect existing connections and reconnect the appropriate clock and 8-channel probes to test).
12. Repeat steps 2 through 11 for other clock threshold levels you want to check.

Minimum Pulse Width Capture

This procedure verifies that the 92C96 Module can capture a minimum pulse width of the sample period plus 2.5 ns.

Equipment Setup

Use the following steps to set up the test equipment and the TLA 510 or 520 system unit for these procedures. Refer to Figure 4–29 for details of the setup while reading these setup instructions.

1. Connect a pulse generator output to the 92C96 Acquisition Fixture.
2. Connect sections A0 and A1 to the 92C96 Acquisition Fixture. You can only verify two sections at a time due to capacitive loading effect on the probes.

NOTE. *To avoid damaging the acquisition probes do not let them hang by the podlets or leadsets. Place them on a flat surface.*

3. Make sure a ground strap is connected between the ground post at the rear of the TLA 510 or 520 and the ground post of the pulse generator.
4. Set the pulse generator for Back Termination and Normal (+) output.
5. Connect a FET probe (with a short ground lead) to one of the vertical inputs of the oscilloscope.

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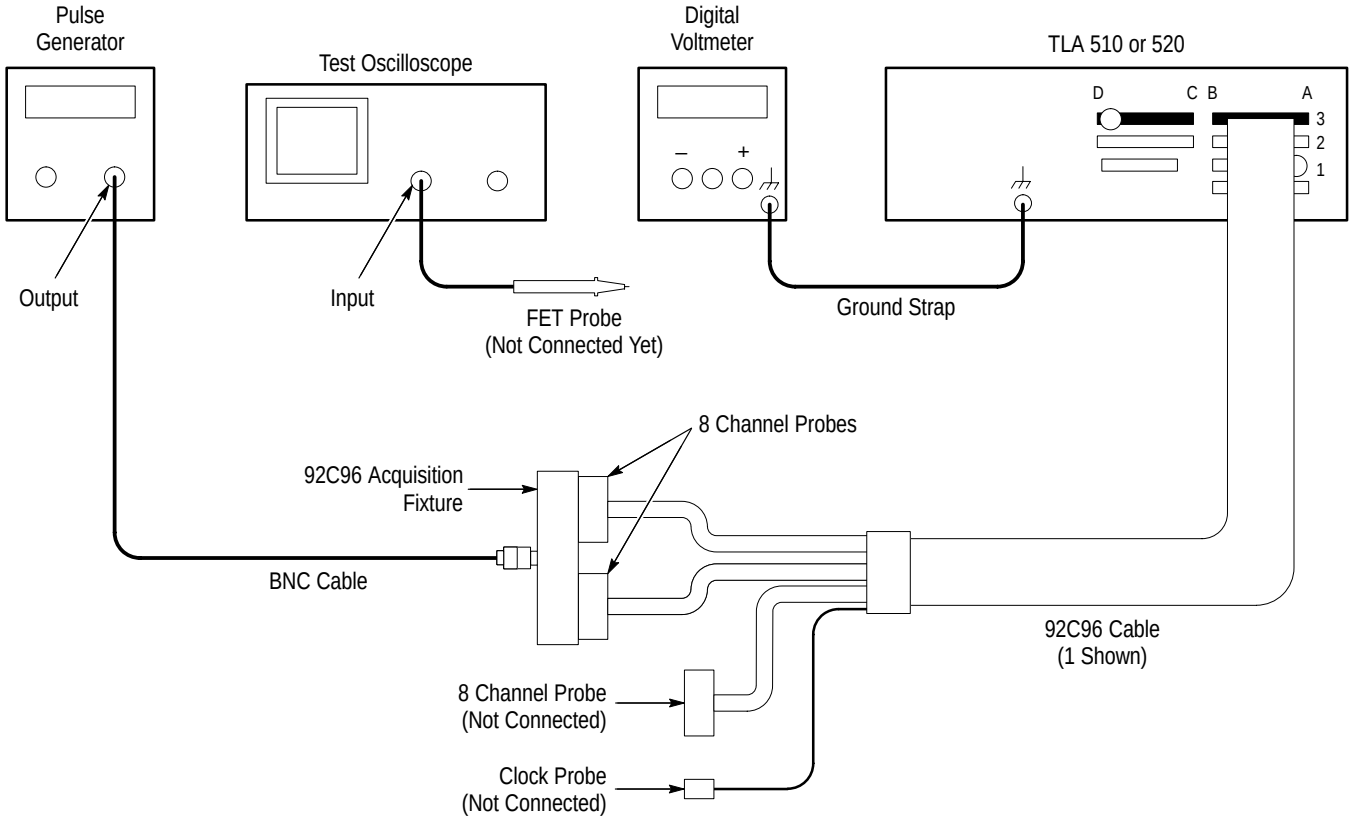


Figure 4–29: Minimum Pulse Width Capture Equipment Setup

Test Procedure

Use the following steps to verify a minimum pulse width capture of the sample period plus 2.5 ns.

1. Select the 92C96 Module and select the Channel menu.
2. Press **F5: DEFINE THRESHOLD**. Change the Threshold field for all the acquisition probes to VAR 0.00V. Press **F8: EXIT & SAVE**.
3. Select the 92C96 Trigger menu.
4. Change the Trigger Position to Defined with the maximum number of cycles before the end of memory (you accomplish this by entering a very large number and letting the instrument default to its largest possible value). Your setting depends on the maximum memory depth of your 92C96 Module.
5. Press **F4: DEFAULT TRIGGER** (if it isn't already).
6. Select the 92C96 Clock menu.
7. Change the Clock field to Internal 10 ns.

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8. Using the FET scope probe, adjust the pulse generator output for a period four times the selected clock period and a pulse width equal to the selected clock period plus 2.5 ns. In this case, a signal with a period of 40 ns and a pulse width of 12.5 ns (10 ns + 2.5 ns), as viewed on the oscilloscope. Adjust the output amplitude for a 1.6 V peak-to-peak pulse centered around ground.

***NOTE**. If you will be acquiring 800 mV signals, you must use the optional coaxial type cables. With 800 mV signals when testing at the 200 megasample clock rate, you must add 3.0 ns to the sample period, instead of 2.5 ns. Also, you should set the pulse generator output amplitude for 800 mV, instead of 1.6 V.*

9. Press **F1: START**. The 92C96 Module should trigger and display the State menu.

10. Select the 92C96 Timing menu.

11. Press **F5: Define Format**. Use the edit traces function to display channels Address 15 through Address 00.

12. Select a magnification appropriate to display the data.

***NOTE**. Magnification required will depend on the memory available in your 92C96 Module. With minimum memory (8K) an appropriate magnification is 200.*

13. Verify that the displayed data for the sections under test resembles a picket fence across the screen with no missing pulses. Figure 4–30 shows an example of a valid timing display for sections A0 and A1 acquired data.

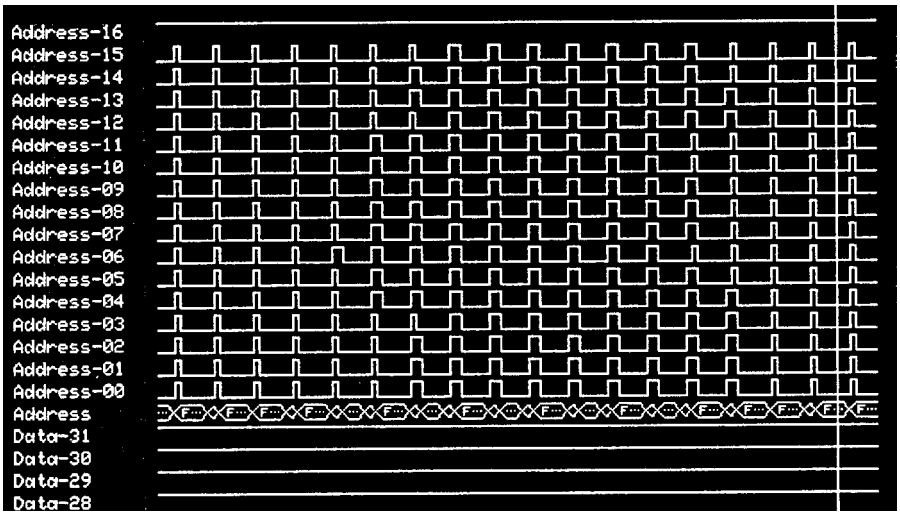


Figure 4–30: Minimum Detectable Multichannel Event

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14. Scroll through the entire acquired data and verify that no channels are missing data pulses.
15. Disconnect the now tested sections from the 92C96 Acquisition Fixture.
16. Connect remaining sections to be tested (up to two at a time) to the 92C96 Acquisition Fixture.
17. Repeat steps 9 through 16 for any remaining sections.
18. Select the 92C96 Config menu.
19. Change the Software Support field to High Speed Timing.
20. Select the 92C96 Clock menu.
21. For each of the two High Speed Timing clock selections (5 ns and 2.5 ns) perform steps 8 through 17. For each of these clock selections you must readjust the pulse generator as described in step 8.

Minimum Glitch Width & Data Amplitude

This procedure verifies that the 92C96 can capture a glitch pulse width of at least 3.5 ns at 100 MHz (10 ns Internal Clock). It also verifies the Minimum Data Amplitude (1.6 V_{p-p} for ribbon-type probe cables or 800 mV_{p-p} for coaxial-type probe cables; either, centered at threshold) and indirectly verifies the probe bandwidth.

Equipment Setup

Use the test equipment and the TLA 510 or 520 system unit setups from the previous procedure for these procedures.

Test Procedure

Use the following steps to verify a minimum glitch pulse width capture of 3.5 ns.

1. Select the 92C96 Config menu.
2. Select General Purpose Software support — if it isn't already.
3. Change the Latch Mode field to On.
4. Select the 92C96 Clock menu. Change the Clock field to Internal 10 ns.
5. Using the FET scope probe, adjust the pulse generator output for a ≥40 ns period and a 3.5 ns wide positive pulse measured at ground as viewed on the oscilloscope. Adjust the output amplitude for a 1.6 V (or 800 mV) peak-to-peak pulse centered around ground.
6. Press **F1: START**. The 92C96 should trigger and display the Timing menu.
7. Select a magnification appropriate to display the data.

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***NOTE**. Magnification required will depend on the memory available in your 92C96 Module. With minimum memory (8k) an appropriate magnification is 200.*

8. Verify that all samples in the Timing menu indicate that latched pulses were stored for all section channels under test throughout the entire memory depth. A failure occurs if any pulses are not detected. Figure 4–31 shows a sample timing display for sections A0 and A1 data.

9. Scroll through the entire acquired data and verify that there are no channels missing any pulses.

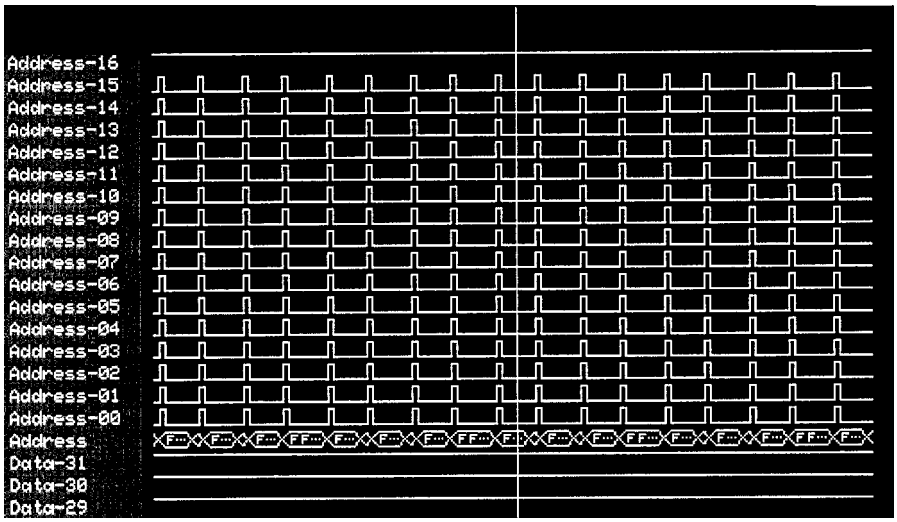


Figure 4–31: Minimum Detectable Glitch Pulse Width

10. Repeat the preceding steps 6 through 9 for the remaining 92C96 probe sections (up to two at a time).

Setup and Hold

This procedure verifies a 92C96 Setup time of 5 ns and a Hold time of 0 ns. This procedure also verifies the clock qualifier channels' setup and hold times when you test data channels C2_0 through C2_3 in this procedure.

Equipment Setup

Use the test equipment and the TLA 510 or 520 system unit setups from the previous procedure for these procedures, with the following additions.

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1. Connect the Clock_3 podlet to the 92C96 Acquisition Fixture centered on the fixture, between the two 8-channel sections.
2. Using the FET scope probe, adjust the pulse generator output for a 5.0 ns wide positive pulse measured at ground.

Test Procedure

Use the following steps to verify Setup and Hold times.

1. Select the 92C96 Clock menu.
2. Select **External** in the Module Clock field.
3. Select the falling edge (\) of Clock_3 as the Sample Clock source.
4. Press **F1: START**. The 92C96 should trigger and display the Timing menu.
5. Select the State menu.
6. Check that the data in the State display are all ones. Scroll through the entire acquired data and verify that the data are all ones for the sections under test. You can use the 92C96 State display search functions to verify that the acquired data are correct for all memory locations.
7. Disconnect the now tested sections from the 92C96 Acquisition Fixture.
8. Connect remaining sections to be tested (up to two at a time) to the 92C96 Acquisition Fixture.
9. Repeat steps 4 through 8 for any remaining sections.
10. Repeat steps 1 through 9 for each remaining external clock channel (disconnect the tested clock and connect one remaining untested clock). Note that in step 3 you must select the falling edge (\) of the currently connected clock channel.
11. Depress the Complement button on the pulse generator IN. Readjust the pulse generator for a 5.0 ns wide negative pulse measured at ground.
12. Select the 92C96 Clock menu.
13. Change the Sample Clock External Clock source to a rising edge (/).
14. Repeat steps 1 through 10 for all sections and external clocks, except now in step 6, verify that the data in the State display are all zeros. Note that in step 3 you must select the rising edge (/) of the currently connected clock channel.

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Counter and Timer Accuracy

This procedure verifies the Counter accuracy of ± 0 counts and the Timer accuracy of ±1 Timer clock, +1/–0 State clock.

***NOTE**. Before performing this procedure you must successfully verified the 92C96 Long Term Timestamp Verification on page 4–84.*

Equipment Setup

Use the test equipment and the TLA 510 or 520 system unit setups from the previous procedure for these procedures.

Test Procedure

Use the following steps to verify counter and timer accuracys.

1. Select the 92C96 Clock menu.
2. Set the Module Clock field to Internal 50 ns.
3. Select the 92C96 Trigger menu.
4. Press **F4: DEFAULT TRIGGER** to return the Trigger menu to its default setups.
5. Program the Trigger menu as shown next.

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```
Trigger Pos: ----T----
Store: All Cycles
Prompt Visibility: On
------------------------------------------------------------------

State   One

  If      Anything
  Then    Incr Counter          #1
          Resume Timer          #2
          Go To State           Two

End of State One

State   Two

  If      Anything
  Then    Incr Counter          #1
  Or If   Counter               #1 ≥ 1,000,000
  Then    Go To State           Three

End of State Two

State   Three

  If      Anything
  Then    Stop Timer            #2
          Trigger

End of State Three
```

This trigger program sets up the counters and timers for testing their accuracy.

6. Press **F1: START**. The 92C96 should trigger and display the State menu.
7. Select the 92C96 Monitor menu.
8. Verify that the Counter #1 value is 1,000,000 ±0 counts.
9. Verify that the Timer #2 value is 50,000.050 µs ± 60 ns (49,999.99 µs — 50,000.110 µs).
10. Repeat steps 3 through 9, substituting Counter #2 for Counter #1 and Timer #1 for Timer #2. The Trigger menu program should resemble the previous program except for changes to the counter and timer numbers.

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Maximum Synchronous Transaction Rate

This procedure verifies that the 92C96 operates at speeds up to and including 100 MHz. This procedure also verifies a maximum external clock rate of 100 MHz, and it verifies that the minimum time between clock edges is 10 ns.

Equipment Setup

Use the following test equipment and the TLA 510 or 520 system unit setups for these procedures. Refer to Figure 4–32 for details of the setup while reading these setup instructions.

1. Connect the trigger output of the master pulse generator to the trigger input of the slave pulse generator with a 20-inch long BNC coaxial cable.
2. Connect the output of the master pulse generator to the BNC end of the BNC-to-Test Point Adapter with a 72-inch long BNC coaxial cable and a female-female BNC connector.
3. Connect the output of the slave pulse generator directly to the BNC end of the 92C96 Acquisition Fixture with a male-male BNC connector.
4. Connect section A0 (color-coded orange) to the 92C96 Acquisition Fixture.
5. Connect Clock_0 (color-coded orange) to the BNC-to-Test Point Adapter.
6. Set the oscilloscope as described below.

Timebase	5 ns/div.
Display Mode	Ch. 1 and Ch. 2
Trigger Mode	Auto
Trigger Source	Ch. 2
Trigger Coupling	DC
Trigger Level	0.00 V
Ch.1 and Ch.2	
Volts/Div.	1 V
Input Coupling	DC

7. Connect Channel 1 of the oscilloscope to the signal side of the BNC-to-Test Point Adapter. Connect the scope ground to the ground side of the fixture.
8. Connect Channel 2 of the oscilloscope to the signal side of the 92C96 Acquisition Fixture. Connect the scope ground to the ground side of the fixture. Make sure the probes in steps 7 and 8 are of the same type and length (that is, match their delay).

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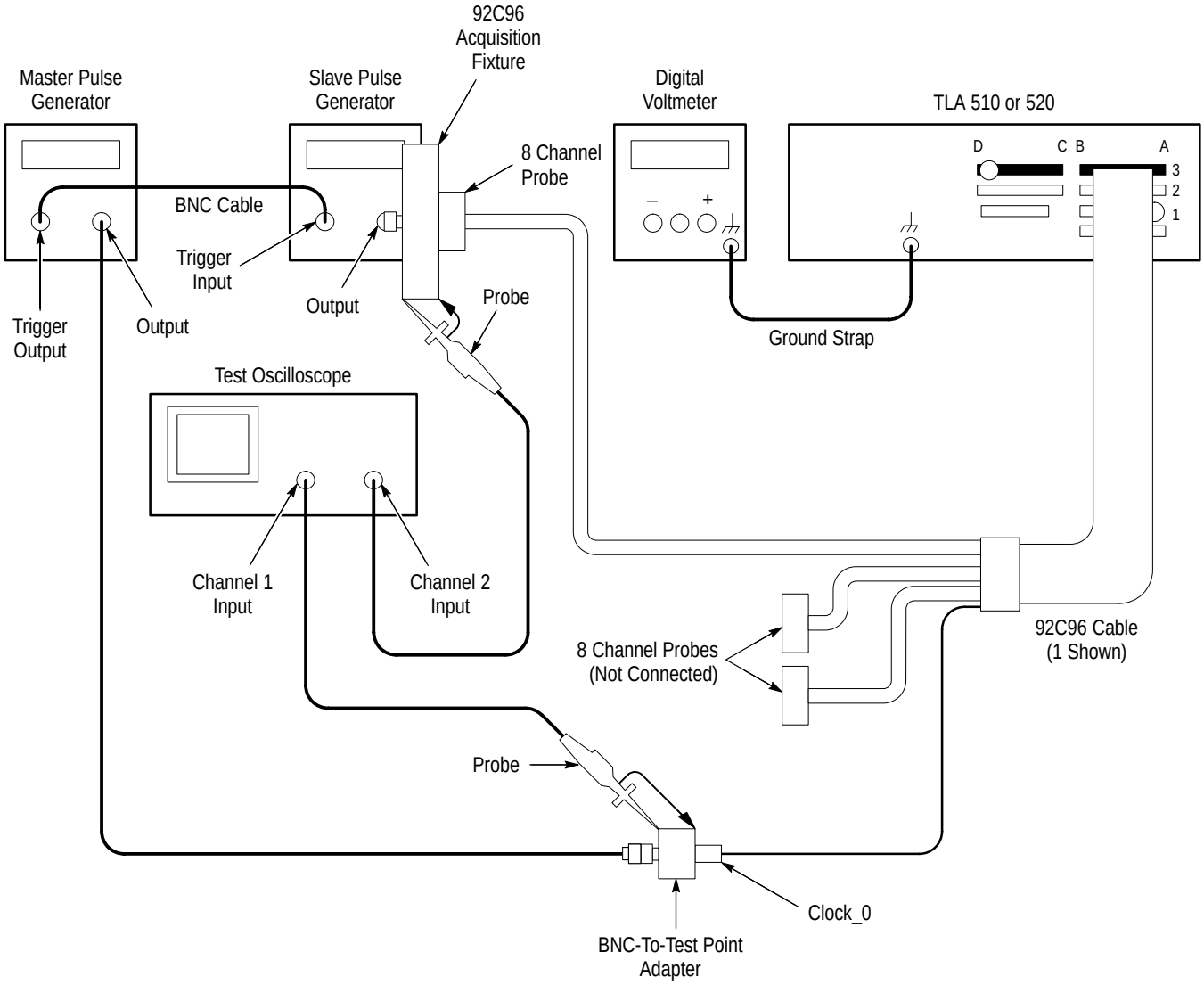


Figure 4–32: Maximum Synchronous Transaction Rate Equipment Setup

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9. Set up the master pulse generator as described below.

Backterm	OUT
Complement	OUT
Period	10 ns
Duration	5 ns

10. Adjust the master pulse generator for a square wave (50% duty cycle) with a 10 ns period. This pulse serves as the clock. It will be necessary to temporally change the oscilloscope trigger source to channel 1.

11. Adjust the master pulse generator amplitude for a 2.5 V_{p-p} pulse centered around 0 V.

12. Set up the slave pulse generator as described next.

Backterm	OUT
Complement	IN
Period	Ext. Trigger
Duration	5 ns

Adjust the amplitude for a 2.5 V_{p-p} pulse centered around 0 V

13. Adjust the slave pulse generator duration control so that four master generator clock cycles occur per slave generator output cycle. Be sure the positive-going data pulse is about 7 ns wide. This pulse serves as the data.

An example of the timing relationship of the master and slave pulse generator signals is shown in Figure 4–33. The 20-inch BNC cable connected in step 1 sets the delay between the two signals. The delay from the rising edge of the clock signal (Ch. 1) to the falling edge of the data (Ch. 2) should be between 1 to 2 ns. If this is not the case, change the length of the BNC cable used in step 1 until this delay is achieved. After setting the amplitude and timing, disconnect the scope probes before running the test to decrease the loading on the pulse generators.

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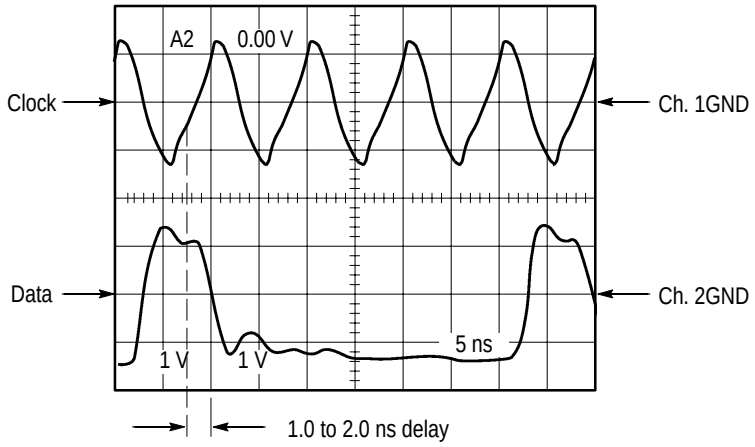


Figure 4–33: Clock To Data Pulse Setup and Hold Relationship

Test Procedure

Use the following steps to verify synchronous operations.

1. Select the 92C96 Clock menu.
2. Select External clocking and the rising edge (⁄) of Clock_0 as the single Sample Clock source in the clock equation (no qualifiers).
3. Select the 92C96 Channel menu.
4. Press **F5: DEFINE THRESHOLD** to call the Threshold Definition overlay.
5. Set Data Threshold and Clock Threshold to VAR 0.00 V and press **F8: EXIT & SAVE**.
6. Select the 92C96 Trigger menu.
7. Press **F4: DEFAULT TRIGGER**.
8. Set Trigger Pos for the middle of the acquisition memory and choose Store Event in the Store field.
9. Program the rest of the Trigger menu as shown next. Note that If-Then clauses must be in the order given in this trigger program.

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```
Trigger Pos: ----T----
Store: Store Event
Prompt Visibility: On
------------------------------------------------------------------

Store   Event
  If      Consec Cycles Sections           are Not Equal
End of Store Event

State   One
                                                 Address          Data       Control
  If      Word                 #1 =              XXXXXXFF       XXXXXXXX      XXXXXXXX
  Then    Go To State          Two
          Incr Counter         #1

End of State One

State   Two
  If      Consec Cycles Sections              are Equal
  Then    Trigger              and store
          Go To State          Seven
                                                 Address          Data       Control
  Or If   Word                 #2 =              XXXXXX00       XXXXXXXX      XXXXXXXX
  Then    Inc Counter          #2
          Go To State          Three
                                                 Address          Data       Control
  Or If   Word                 #2 ≠              XXXXXX00       XXXXXXXX      XXXXXXXX
  Then    Trigger              and store
          Go To State          Seven

End of State Two

State   Three
  If      Consec Cycles Sections           are Not Equal
  Then    Trigger              and store
          Go To State          Seven
                                                 Address          Data       Control
  Or If   Word                 #2 =              XXXXXX00       XXXXXXXX      XXXXXXXX
  Then    Inc Counter          #2
          Go To State          Four
                                                 Address          Data       Control
  Or If   Word                 #2 ≠              XXXXXX00       XXXXXXXX      XXXXXXXX
  Then    Trigger              and store
          Go To State          Seven

End of State Three
```


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```
State   Four
  If      Consec Cycles Sections            are Not Equal
  Then    Trigger              and store
          Go To State          Seven
                                              Address          Data       Control
  Or If   Word                 #2 =           XXXXXX00      XXXXXXXX      XXXXXXXX
  Then    Inc Counter          #2
          Go To State          Five
                                              Address          Data       Control
  Or If   Word                 #2 ≠           XXXXXX00      XXXXXXXX      XXXXXXXX
  Then    Trigger              and store
          Go To State          Seven

End of State Four

State   Five
  If      Consec Cycles Sections               are Equal
  Then    Trigger              and store
          Go To State          Seven

  Or If   Counter              #1 ≥ 1,000,000
  Then    Trigger              and store
          Go To State          Six
                                              Address          Data       Control
  Or If   Word                 #1 =           XXXXXXFF      XXXXXXXX      XXXXXXXX
  Then    Inc Counter          #1
          Go To State          Two
                                              Address          Data       Control
  Or If   Word                 #1 ≠           XXXXXXFF      XXXXXXXX      XXXXXXXX
  Then    Trigger              and store
          Go To State          Seven

End of State Five

State   Six
  If      Anything
  Then    Do Nothing

End of State Six

State   Seven
  If      Anything
  Then    Do Nothing
End of State Seven
```


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This trigger program causes acquisition memory to store a 00-FF-00-FF alternating data acquisition pattern for the A0 data channels. Trigger and gaps occur on FF cycles. State Seven stops trigger program execution if an error occurs.

10. Press **F1: START**. The 92C96 Module triggers, stops, and displays the State menu. Figure 4–34 shows what the State menu should look like. Note that the sequence numbers will vary, depending on the memory depth of the 92C96 Module. Gray highlight should appear behind every FF sequence indicating a gap occurred in the data.

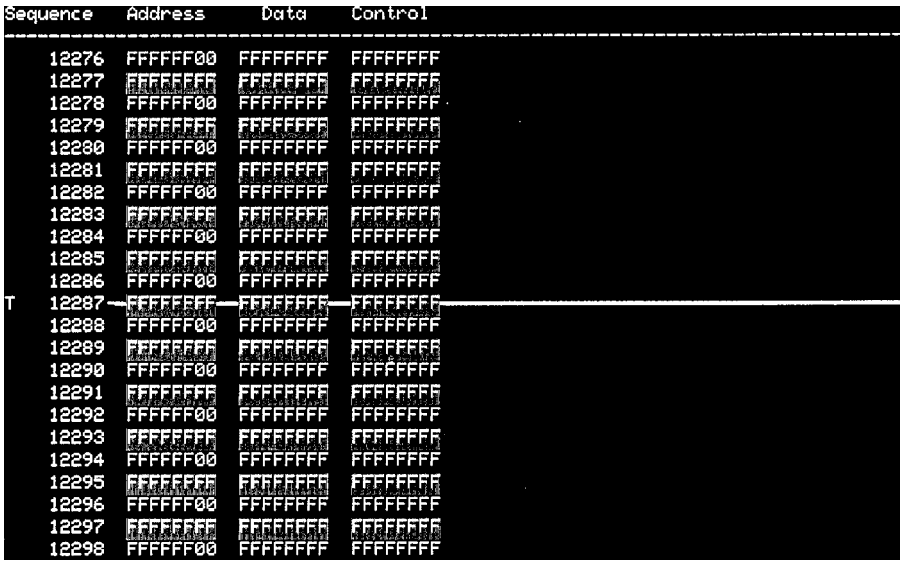


Figure 4–34: Data Pattern Displayed For Maximum Synchronous Transaction Rate Test

11. Select the 92C96 Monitor menu.

12. Verify the following information in the Monitor menu.

Counter #1	1, 000,000
Counter #2	3, 000,000
Final State	Six

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Module Sync Out Delay

This procedure verifies that the 92C96 Module Sync Out signal has a delay of ≤75 ns as measured from the probe tip to the Sync Out connector. To check Module Sync Out drive levels, perform the Module Sync Out test next in this section.

Equipment Setup

Use the test equipment and the TLA 510 or 520 system unit setups from the final conditions in the previous procedure for these procedures, with the following changes:

1. Connect the P6041 Sync Out cable to the 92C96 Module Sync Out connector (J900).
2. Disconnect the 92C96 Acquisition Fixture from the slave pulse generator's BNC connector and connect the fixture to the P6041 cable.
3. Disconnect the 92C96 data channel group A0 from the 92C96 Acquisition Fixture.
4. Select **Ch. 1** as the oscilloscope trigger source.
5. While viewing the oscilloscope display of the signal from the channel 1 probe connected to the BNC-to-Test Point Adapter, adjust the master pulse generator for a ≥1.0 µs period square wave and an amplitude of 1.6 V_{p-p} centered around 0 V.

Test Procedure

Use the following steps to verify Sync Out delay.

1. Select the 92C96 Trigger menu.
2. Press **F4: DEFAULT TRIGGER**.
3. Change the Store field to All Cycles. Then program the Trigger menu as shown next.

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```
Trigger Pos: ----T----

Store: All Cycles
Prompt Visibility: On
------------------------------------------------------------

State   One
  If      Anything
  Then    Pulse Signal          Module Sync Out
          Go To State           Two

End of State One

State   Two
  If      Anything
  Then    Go To State           One

End of State Two
```

This trigger program inhibits a trigger from occurring and causes the Module Sync Out signal to pulse.

4. Press **F1: START**.

5. On the oscilloscope display, measure the time between the rising edge of the clock from the BNC-to-Test Point Adapter (oscilloscope channel 2) and the transition (plus and minus slope crossing) of the Sync Out signal (oscilloscope channel 1). The measurement must be ≤75 ns at the connector. However, if you are measuring at the end of the sync out cable, add 6 ns to the measurement to compensate for the cable length (i.e., ≤81 ns).

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Timestamp Time Base Accuracy Long Term

This procedure verifies the 92C96 Timestamp Time Base accuracy signals for the Long Term specification.

Equipment Setup

Use the following hardware setups as shown in Figure 4–35 for this test.

1. Connect the Sync Out cable (P6041) to J900 on the 92C96 Module.
2. Connect the other end of the Sync Out cable to the input of the counter timer.
3. Adjust the counter for a waveform period measurement.

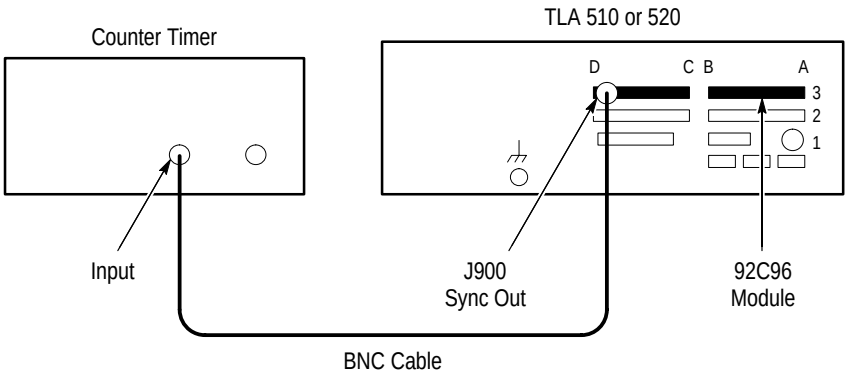


Figure 4–35: 92C96 Channel Connections

Test Operation

Use the following steps to verify the Sync Out signal.

1. Power on the logic analyzer and select the 92C96 Trigger menu and program the menu as shown in Figure 4–36.

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```
Trigger Pos: T--------
Store: All Cycles
Prompt Visibility: On
-----------------------------------------------------------------
State   One
  If      Anything
  Then    Assert Signal         Module Sync Out
          Go To State           Two

End of State One

State   Two
  If      Anything
  Then    Unassert Signal       Module Sync Out
  Go To State                   One

End of State Two
```

Figure 4–36: 92C96 Trigger Menu For Long Term Timestamp Verification

This Trigger program generates a Sync Out signal period that is twice the selected sampling period (the power-up default period is 10 ns asynchronous).

2. Press **F1: START** to enable the Sync Out signal.
3. Check the counter display for a 20 ns period.
4. Press **F1: STOP**.

This completes the 92C96 Module performance checks.

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92S16 Pattern Generation Modules

The following procedures verify the performance requirements of the 92S16 Pattern Generation Module.

Equipment Required

In addition to the TLA 510 or 520 system unit you will need the following equipment to perform the 92S16 Performance Check Procedures. Refer to Table 4–1 for more information on the test equipment specifications.

- 92S16 Pattern Generation Module
- 92C96 Data Acquisition Module
- Digital Multimeter
- 400 MHz Oscilloscope (Tektronix 2465B)
- Two 10 MΩ Oscilloscope Probes (Tektronix P6137)
- 100 MHz Pulse Generator
- Two Dual-Lead Adapters (Tektronix part number 015-0325-XX)
- +5 V Power Supply (2 A minimum) (1 A for each P6463A probe) (Tektronix PS282)
- Two P6463A Pattern Generation Probes
- P6460 External Control Probe
- P6041 Passive Probe (Sync Out Cable)
- BNC T Connector (Tektronix part number 103-0030-XX)
- 50 Ω BNC Terminator (Tektronix part number 011-0049-XX)
- BNC-to-Test Point Adapter (refer to *Test Fixtures* on page 5–27)
- General Purpose Acquisition Fixtures (refer to *Test Fixtures* on page 5–27)
- Two Clock Skew Fixtures (refer to *Test Fixtures* on page 5–27)
- Decoupling Fixtures (refer to *Test Fixtures* on page 5–27)
- Dual (1 × 2) square-pin connector (Tektronix part number 131-1614-XX)

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Test Configurations

Use the following steps to set up the TLA 510 or 520 system unit for the 92S16 Performance Check Procedures.



CAUTION. *Before installing or removing any cards, be sure to power down the system unit. Damage to circuitry may occur if cards are installed or removed while the system unit is receiving power. Before you unplug the power cord, power down the system unit (using the front-panel ON/STANDBY switch) and wait at least 30 seconds to allow sufficient time for the hard-disk drive head to park and lock in a safe position.*

1. Ensure that the TLA 510 or 520 system unit is powered down and that the power cord is removed.



CAUTION. *Observe anti-static precautions before handling any TLA 510 or 520 card; otherwise, damage may occur. To avoid static damage, store any unused modules in anti static packaging.*

2. Connect the P6463A Pattern Generation Probes to the pod A and B connectors of the 92S16 Module. It may be necessary to temporarily remove the backpanel probe retainer clips to connect the probes.

NOTE*. If you adjusted the 92S16 Module to the P6463A probes using the adjustment procedures in Chapter 5 of this manual, you should label the probes with the pod number where they were connected so that you can reconnect them to their proper locations.*



WARNING. *Incorrectly connecting the power to the decoupling fixture can cause the tantalum capacitor to burn or explode.*

3. Carefully connect the positive side of the decoupling fixture to the positive side of the power supply, and connect the negative side of the fixture to the negative side of the power supply. Note the polarity of the tantalum capacitor.
4. Connect the black (VL) leads of both pattern generator probes to the common or ground output of the decoupling fixture.
5. Connect the red (VH) leads of both pattern generator probes to the positive side of the decoupling fixture.

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NOTE. *Prior to connecting the P6463A probes, verify that they are configured in the 9-bit mode (J115 and J570 both jumpered on pins 2 and 3. Refer to the P6463A manual for more information.*

6. Double-check all of the above connections.

92S16 Performance Verification

Perform the following procedure to verify the performance of the 92S16.

Clock And Data Skew Checks. This procedure verifies the following specifications:

Maximum Skew At Probe Tip Between Different Output Clocks:	4 ns within the same card
Maximum Data Channel Skew:	1 ns within the same probe

Menu Setups. Use the following steps to set up the 92S16 menus for the Clock And Data Skew Checks.

1. Connect the power cord to the power receptacle and power up the terminal, the TLA 510 or 520 system unit, and the power supply in that order.
2. Verify that the TLA 510 or 520 passes the power-up diagnostics before continuing with this procedure.
3. Select the 92S16 Module and select the Config menu.
4. Select **Internal 100 ns** in the Clock field.
5. Select the 92S16 Channel menu.
6. Press **F8: ADD**, select **Add Group**. The TLA 510 or 520 will add a new group for the 92S16 strobe lines.
7. Press **F8: ADD**, select **Add Pod to Group**. The TLA 510 or 520 will add the other strobe line to the group you just created.
8. Select the 92S16 Program menu.
9. Move to the sequence 0 label field and enter Start.
10. Move to the sequence 1 instruction field and select **Jump**. Move to the right and enter Start.
11. Move to the sequence 1 data column and enter all highs (Fs). The default sequence 0 data should be all 0s. Note that the strobe data column allows a maximum value of 3 instead of F.
12. Press **F1: START**.

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Clock Skew Verification. Use the following steps to verify the clock skew between the clock podlets.

1. Power up the oscilloscope.
2. Set the scope timebase to 1 ns/div and the channel 1 and channel 2 inputs to 500 mV/div. Trigger off the rising edge of channel 1.
3. Connect the Dual-Lead Adapters to the scope probe tips. Temporarily connect the dual square-pin connector to the black lead and the white lead of the dual-lead adapter connected to the channel 2 scope probe.
4. Connect one of the Clock Skew Fixtures to the 92S16 pod A clock output.
5. Connect the channel 1 scope probe to the Clock Skew Fixture connected to the pod A clock output.
6. Temporarily touch the dual square-pin connector to the pod A clock output. Record the amount of delay between the channel 1 and channel 2 traces. Subtract this delay value from all following scope measurements.
7. Remove the dual square-pin connector from the channel 2 scope probe.
8. Connect another Clock Skew Fixture to the pod B clock output. Connect the channel 2 scope probe leads to the Clock Skew Fixture.
9. Record the skew between the rising edges of the two clock signals. Change the scope to trigger on the falling edge of channel 1 and record the skew between the falling edges of the two clock signals.
10. Verify that the difference between the maximum and minimum values of the clock skew is within 4.0 ns. Remember to subtract the delay recorded earlier.
11. Press **F1: STOP**. Select the 92S16 Channel menu.
12. Press **F6: DEFINE CHANNELS**. Select pod B and change the Clock Delay field to –5 ns. Leave pod A clock delay at 0 ns. Press **F8: EXIT & SAVE**.
13. Press **F1: START**.
14. Record the skew between the falling edges of the two clock signals. Change the scope to trigger on the rising edge of channel 1 and record the skew between the rising edges of the two clock signals.
15. Verify that the difference between the maximum and minimum values of the clock skew is within 9 ns. Remember to subtract the delay recorded earlier.
16. Press **F1: STOP**. Select the the 92S16 Channel menu.
17. Press **F6: DEFINE CHANNELS**. Select pod B and change the Clock Delay field to +5 ns. Leave pod A clock delay at 0 ns. Press **F8: EXIT & SAVE**.

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18. Press **F1: START**.

19. Record the skew between the rising edges of the two clock signals. Change the scope to trigger on the falling edge of channel 1 and record the skew between the falling edges of the two clock signals.

20. Verify that the difference between the maximum and minimum values of the clock skew is within 9 ns. Remember to subtract the delay recorded earlier.

21. Press **F1: STOP**.

Data Skew Verification. Use the following steps to verify the data channel maximum skew between channels in the same probe. This procedure uses the same 92S16 setups as the previous check.

1. Select the 92S16 Channel menu.

2. Press **F6: DEFINE CHANNELS**. Select pod B and change the Clock Delay field to 0 ns. Leave pod A clock delay at 0 ns. Press **F8: EXIT & SAVE**.

3. Press **F1: START**.

4. Move the Clock Skew Fixture from the pod A clock podlet to the pod A channel 0 podlet. Connect the channel 1 scope probe to the fixture.

5. Move the Clock Skew Fixture from the pod B clock podlet to the pod A channel 1 podlet. Connect the channel 2 scope probe to the fixture.

6. Record the skew between the falling edges of the two signals. Change the scope to trigger on the rising edge of channel 1 and record the skew between the rising edges of the two signals.

7. Move the Clock Skew Fixture from pod A channel 1 to channel 2 and record the skew between the rising edge of the two signals. Change the scope to trigger on the falling edge of channel 1 and record the skew between the falling edges of the two signals.

8. Repeat steps 1-7 for data channels 0 through 7 of the pod A probe.

***NOTE**. The verification of the channel 8 (strobe) output is only valid when the P6463A probe is in the 9-bit mode. The verification of channels 8 through 15 outputs, when the P6463A probe is in the 16-bit mode, will be performed separately (later).*

---

9. Move the Clock Skew Fixture from pod A channel 7 to channel 8 (strobe output) and record the skew between the two signals. Remember to look at both the rising and falling edges.

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10. Verify that the difference between the maximum and minimum values of the recorded skew values are within 1 ns. Remember to subtract the delay recorded earlier.
11. Repeat the above steps for the 92S16 pod B probe.
12. Press **F1: STOP**.

92S16 External Clock Verification. Use the following steps to set up the TLA 510 or 520 system unit for the 92S16 External Clock Verification checks. If you have not already built the General Purpose Acquisition Fixture, refer to *Test Fixtures* on page 5–27 for the instructions you will need to build the fixture.

1. Position the acquisition fixture such that the ground square pins are to the bottom. Place the P6463A probe on the right side of the fixture and the 92C96 probes on the left.
2. Refer to Table 4–6 to connect the podlets of each probe to the acquisition fixture. The square pin closest to the 18-inch black lead is designated as pin 1. Connect the probes to their respective pod connectors on the 92S16 and 92C96 Modules as indicated in the table.
3. Connect the 18-inch black lead of the acquisition fixture to the ground connection of the power supply.

Table 4–6: Acquisition Fixture Connections

92C96 Channel	Acq Fix Pin #	P6463A	92S16
Clock_2	39	CLK	POD B
C2_1_Brn	37	8	POD B
D1_7_Vlt	35	7	POD B
D1_6_Blu	33	6	POD B
D1_5_Grn	31	5	POD B
D1_4_Ylw	29	4	POD B
D1_3_Org	27	3	POD B
D1_2_Red	25	2	POD B
D1_1_Brn	23	1	POD B
D1_0_Blk	21	0	POD B
–	19	CLK	POD A
C2_0_Blk	17	8	POD A
D0_7_Vlt	15	7	POD A
D0_6_Blu	13	6	POD A
D0_5_Grn	11	5	POD A

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Table 4–6: Acquisition Fixture Connections (Cont.)

92C96 Channel	Acq Fix Pin #	P6463A	92S16
D0_4_Ylw	9	4	POD A
D0_3_Org	7	3	POD A
D0_2_Red	5	2	POD A
D0_1_Brn	3	1	POD A
D0_0_Blk	1	0	POD A

4. Power on the pulse generator and the power supply.
5. Connect the BNC-to-Test Point Adapter to the output of the pulse generator. Pull out the BACK TERM on the pulse generator. Also make sure the Complement button is out (Normal output). Use the oscilloscope to set the pulse generator for a 20 ns period with a 9 ns-wide positive pulse. Set output amplitude from 0 V to +2.5 V.
6. Connect the P6460 External Control Probe to the pod D connector on the 92S16 Module.
7. Attach the white lead (EXT CK) of the P6460 lead set to the signal side of the BNC-to-Test Point Adapter. Connect the ground sense line of the P6460 probe to the ground side of the test point adapter.
8. Power up the Terminal and TLA 510 or 520 system unit and verify that all the diagnostics pass before continuing with this procedure.

92S16 9 ns High External Clock Verification. This procedure verifies the following specifications:

External Clock Inputs:

Period:	20 ns minimum
High Pulse:	9 ns minimum
Polarity:	Rising Edge Selectable

Use the following steps to form the cluster for the 92S16 performance verifications.

1. Select the Sys Config menu from the Menu Selection Overlay.
2. Press **F6: DEFINE CLUSTER** followed by **F2: CLUSTER ALL**.
3. Press **F8: EXIT & SAVE**

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92S16 Pattern Generation Setups. Use the following steps to set up 92S16 for the 92S16 9 ns High External Clock Verification.

1. Select the 92S16 Module and select the Config menu.
2. Select **EXTERNAL** ⁄ in the Clock field.
3. Select the 92S16 Channel menu.
4. Press **F6: DEFINE CHANNELS**. Check that the Output Level is TTL, Check Polarity is ⁄, and Clock Delay is 0 ns for both pods. Press **F8: EXIT & SAVE**.
5. Select the 92S16 Program menu.
6. Change the Program menu to match Figure 4–37.

IRQ: Unmask IRQ — Inhibit Display: On

Seq	Label	Instruction	Pg2_1 Hex	Pg2_2 Hex
0	Start		0000	0
1			0101	0
2			0202	0
3			0404	0
4			0808	0
5			1010	0
6			2020	0
7			4040	0
8			8080	0
9		Jump Start	FFFF	0

Figure 4–37: Walking Bit Pattern for 92S16 Verification Procedures

92C96 Data Acquisition Setups. Use the following steps to set up the 92C96 for the 92S16 9 ns High External Clock Verification.

1. Select the 92C96 Module and select the Clock menu.
2. Change the 92C96 Clock field to External. Change the Sample Clock Field to \ Clock_2.
3. Select the 92C96 Trigger menu. Press **F4: Default Trigger**.

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Test Operation. Use the following steps to perform the 92S16 9 ns High External Clock Verification.

1. Press **F1: START**. Ensure that the 92C96 triggers and displays the State menu.
2. Select the 92C96 Timing menu. Press **F5: Define Format**. Use the edit traces function to display channels Data 15 through Data 00.
3. Change the magnification as necessary to display a ramp (walking bit) pattern with no dropped bits or unevenness in the pattern. Scan the entire acquired data for the ramp pattern and verify that there are no gaps or unevenness. Figure 4–38 shows an example of the ramp pattern.

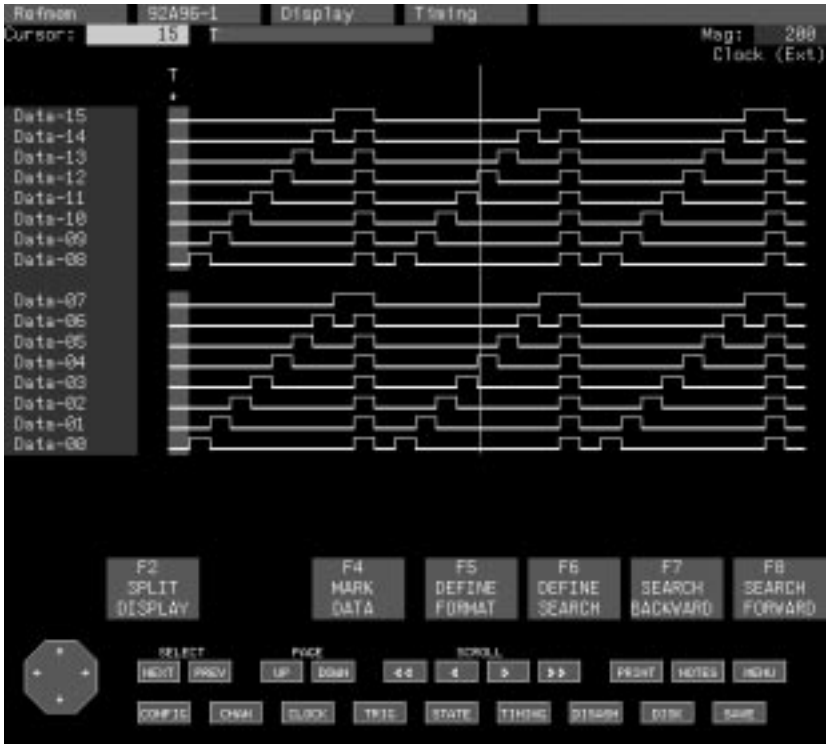


Figure 4–38: Sample Ramp Pattern for the 92S16 External Clock Verification

92S16 9 ns Low External Clock Verification. This procedure verifies the following specification:

External Clock Inputs:

Period:	20 ns minimum
Low Pulse:	9 ns minimum
Polarity:	Falling Edge Selectable

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Press the Complement button on the pulse generator and readjust the output for a 20 ns period with a 9 ns wide negative pulse and an amplitude from 0 to +2.5 V.

The following steps set up the TLA 510 or 520 menus for this test. This test uses the same setups as the previous test except for the change in the 92S16 Config menu.

1. Select the 92S16 Module and select the Config menu.
2. Select **EXTERNAL** \.
3. Select the 92C96 Module. Press **F5: MOVE TO DISPLAY** followed by **F1: START**.
4. Verify that the 92C96 triggers and that the displayed Timing menu is the same as the previous test. Scan the entire acquired data for the ramp pattern and verify that there are no gaps or unevenness.

This completes the 92S16 Module performance check.

P6463A Probe

The following procedures provide a method of verifying the probe's advertised specifications. It is recommended that you start at the beginning of these verification procedures and progressively work through all the procedures. To perform the verification procedures, you will need the following equipment:

- TLA 510 or 520 system unit and terminal
- 92S16 Pattern Generation Module
- Tektronix PS 282 Power Supply (or equivalent)
- Tektronix 2465B Oscilloscope (or equivalent)
- Two Tektronix P6137 Probes (or equivalent)
- 92S16 Clock Skew Fixture
- Two dual lead adapters (Tektronix part number 015-0325-XX)
- 82 Ω resistor (Tektronix part number 315-0820-XX)
- 68 Ω resistor (Tektronix part number 315-0680-XX)

Maximum Frequency (Clock & Data)

This procedure verifies the following specifications:

Clock Maximum Frequency: 50 MHz (20 ns)

Data Maximum Frequency: 25 MHz (40 ns)

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1. Connect the P6463A probe to the pod A connector of the 92S16 at the rear of the system unit.



WARNING. *Incorrectly connecting the power to the decoupling fixture can cause the tantalum capacitor to burn or explode.*

2. Carefully connect the positive side of the decoupling fixture to the positive side of the power supply, and connect the negative side of the fixture to the negative side of the power supply. Note the polarity of the tantalum capacitor.
3. Connect the black (VL) leads of the pattern generator probe to the common or ground output of the decoupling fixture.
4. Connect the red (VH) leads of the pattern generator probe to the positive side of the decoupling fixture.
5. Remove the top case half on the P6463A and set it aside. Position both jumpers J115 and J570 to short pins 2 and 3. This puts the probe in the 9-channel mode.
6. Power on the X Terminal, TLA 510 or 520 system unit, and power supply in that order.
7. Select the 92S16 Config menu and set the clock rate for Internal 20 ns.
8. Select the 92S16 Channel menu. Program the following information as shown in Figure 4–39.

Group Name	Probe	Channels
Pg2_1	Pod 2A_7-0	Ch 76543210
Pg2_2	Pod 2A_8	Ch 8

Figure 4–39: 92S16 Channel Menu for Maximum Frequency Verification

9. Select the 92S16 Program menu. Program sequences 0 and 1 as shown in Figure 4–40.

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Figure 4–40: 92S16 Program Menu for Maximum Frequency Verification

10. Set the Oscilloscope as follows:

- Vertical Input: 1 V/div
- Timebase: 5 ns/div
- Trigger Source: Channel 1

11. Use the 92S16 Clock Skew Fixture to connect the P6463A clock lead to the scope probe attached to Channel 1 of the oscilloscope.

12. Press **F1: START** and verify that the clock period is 20 ns as displayed on the oscilloscope. This verifies the maximum frequency for the 9-channel mode.

13. Press **F1: STOP**.

14. Position both jumpers J115 and J570 to short pins 1 and 2. This puts the probe in the 16-channel mode.

15. Press **F1: START** and verify that the oscilloscope shows the clock period is 40 ns. This verifies the maximum frequency for the 16-channel mode.

16. Press **F1: STOP**.

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Clock/Data Output Levels and Drive Capability

This procedure verifies the following specifications:

TTL Output Levels: V_{HI} = 2.7 V min., V_{LO} = 0.5 V max.

TTL Drive Capability: 48 mA sink (at 10 MHz), 12 mA source

This test uses the same 92S16 Channel menu setup as the previous test.

***NOTE**. This test should be performed with the standard TTL Line drivers installed, and with the 0 Ω termination resistors installed; refer to the P6463A manual for more information on line drivers and termination resistors.*

1. Select the 92S16 Config menu and change the clock to Internal 100 ns.
2. Select the 92S16 Program menu and program the information shown in Figure 4–41.

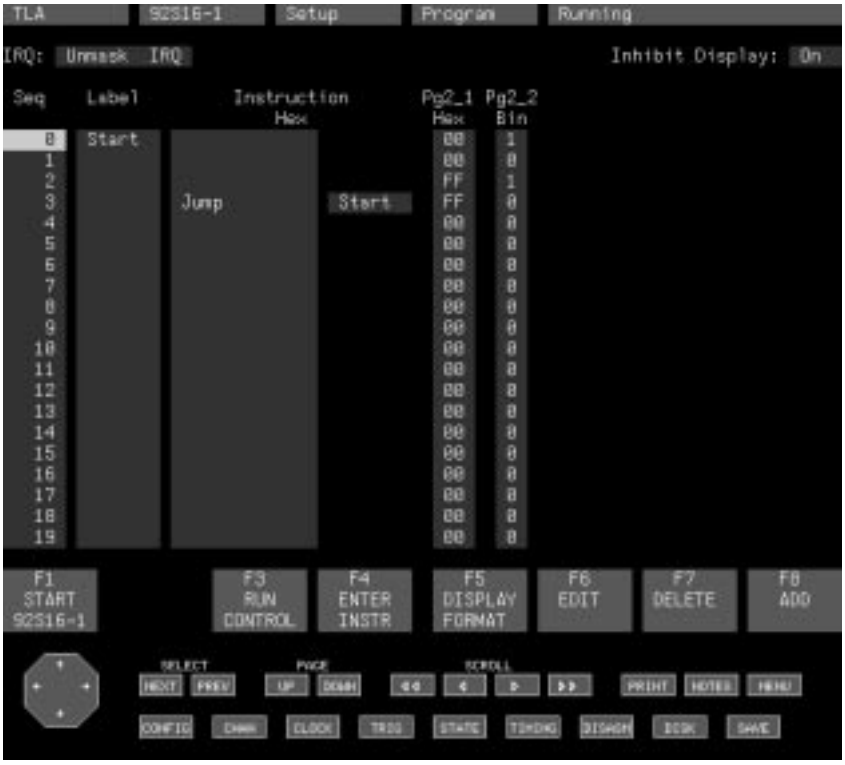


Figure 4–41: 92S16 Program Menu for P6463A Verification Procedures

3. Press **F1: START**.
4. Connect one end of an 82 Ω resistor to one end of an 68 Ω resistor. Connect the unused end of the 82 Ω resistor to the +5 V output of the external power

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supply. Connect the unused end of the 68 Ω resistor to the power supply's common or ground.

5. Connect an oscilloscope probe to the junction of the two resistors. To verify that the P6463A clock and 16 data channels can drive a signal to the proper level, individually connect each channel to the junction of the two resistors.
6. Verify a minimum of +2.7 V for a logic high and a maximum of +0.5 V for a logic low on each channel being verified.
7. Press **F1: STOP**.

Clock Minimum Pulse Width

This procedure verifies the following specification:

Clock Pulse Width: 7 ns minimum

1. Select the 92S16 Config menu and change the clock to Internal 20 ns.
2. Using the equipment setup from the previous procedure, connect the Clock channel to the junction of the two resistors.
3. Press **F1:START**. Using the oscilloscope in the same manner, check that the clock pulse width is a minimum of 7 ns duration measured at a 1.4 V threshold.
4. Press **F1:STOP**.
5. Select the 92S16 Channel menu. Press **F6: DEFINE CHANNELS** to call the Channel Definition overlay, and change the Clock Polarity to \. Press **F8: EXIT & SAVE** to exit the overlay.
6. Press **F1: START**. Using the oscilloscope in the same manner, check that the clock pulse width is a minimum of 7 ns duration measured at a 1.4 V threshold.
7. Press **F1: STOP**.

This completes the verification of the P6463A probe.

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Adjustment Procedures

This section contains procedures for performing the TLA 510 or 520 adjustments so that the instrument meets or exceeds performance specifications. Not all TLA 510 or 520 components require adjustments. Some components contain factory set adjustments which can only be altered with special test fixtures and equipment not available outside of Tektronix. This section contains only the adjustments that can be made without using these special test fixtures or equipment. If the TLA 510 or 520 logic analyzer does not meet or exceed specifications as outlined by these procedures, repair is necessary; if this is the case, contact your Tektronix Service Center.

Purpose

The adjustment procedures listed in this section of this manual provide instructions for performing adjustments. They are not intended as troubleshooting tools or verification procedures. This chapter is divided into sections that describe the adjustments for each TLA 510 or 520 module.

Adjustment Interval

To ensure correct instrument operation, adjustments should be checked every 1.5 years. Before performing the adjustment procedures, complete any relevant maintenance procedures outlined in the *Maintenance* section of this manual.

Limits and Tolerances

The limits and tolerances given in this section are adjustment guidelines only. They should not be interpreted as instrument specifications unless they are listed as specifications in Chapter 1 of this manual. Tolerances are given for the component under test and do not include test equipment errors.

Equipment Required

The equipment necessary to complete all the adjustment procedures are listed in Table 5–1. A partial list of equipment needed for each component is given at the beginning of each procedure.

The specifications given in Table 5–1 are the minimum necessary to produce accurate results. Related equipment must meet or exceed the listed specifications. Detailed instructions for operating test equipment are not included with this document. Refer to the manual for the specific test equipment if more information is needed.

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The chapter *Diagrams* contains the Component Location Diagrams. Use the diagrams to locate the components, test points, and adjustments mentioned in these procedures unless otherwise indicated.

Alternative Equipment

If equipment other than the recommended test equipment is used, the control settings or adjustments of the test equipment may need to be changed. If the exact equipment listed in Table 5–1 is not available, check the Minimum Specification column carefully to see if any other equipment will be sufficient.



WARNING. *Dangerous electric-shock hazards exist inside the system unit. To prevent electric-shock, remove all jewelry (e.g., watch and rings) before beginning any of the adjustment procedures.*

Table 5–1: Equipment Needed for Adjustment Procedures

Equipment	Specifications	Equivalent Tektronix Instrument
TLA 510 or 520 System Unit	No substitute allowed	
9204XT, 9205XT, or 9206XT Terminal	No substitute allowed	
92C96 or 92A96 Data Acquisition Module	No substitute allowed	
92S16 Pattern Generation Module	No substitute allowed	
Two P6463A Pattern Generation Probes	No substitute allowed	
P6460 External Control Probe	No substitute allowed	
Two-channel Oscilloscope with Probes	350 MHz	
Two FET Probes	2.5 to 3.0 pF	
Two Oscilloscope Probes	50 Ω	
Subminiature to miniature adapter	Oscilloscope Probe Accessory	013-0202-XX
Two Dual Lead Adapters	Oscilloscope Probe Accessory	015-0325-XX
Digital Voltmeter	5.5 digit	
Dual Variable DC Power Supply	300 mA from both outputs	
Variable DC Power Supply	1 A output per P6463A probe	
Frequency Counter	200 MHz	
Digital Multimeter	3.5 digits 0.1% VDC	
Sinewave Generator	Variable frequency up to 200 MHz with variable output	
Delay Line Adjustment Tool	No substitute allowed	003-1134-XX
Two non-conductive adjustment tools	Eight and three inches long	
Bayonet-type probe tip		013-0085-XX

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Power Supply Adjustment

Power supply adjustments are only necessary if the measurements in the *Troubleshooting* section of the *Maintenance* chapter are out of tolerance. To determine if the voltage supplies are within tolerance, perform the Power Supply Check on page 6–41.

Equipment Setup

Use the following test equipment and TLA 510 or 520 setups for these procedures.

1. Set the digital voltmeter (DVM) or digital multimeter to the 20 VDC range.



CAUTION. *When powering off the system unit, wait at least 30 seconds before disconnecting the power cord. This allows the system unit to complete file-management procedures and move the hard-disk drive head to a safe position.*

2. Power off the logic analyzer and remove the power cord from the system unit.
3. Remove the top cover from the system unit.
4. Refer to *Removing The Fan Frame* on page 6–21 and remove the fan frame. Do not remove the power connections.
5. Place the fan so that air flows through the card cage.



CAUTION. *If the system unit has two modules installed, the power should not be on longer than five minutes. This avoids excessive heat build up that could damage the modules.*

6. Power on the system unit.



WARNING. *High voltage is present on the Backplane board. To avoid electric shock do not touch conductive parts.*

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Voltage Adjustments

Refer to Figures 5–1 and 5–2 while performing the following adjustments:

1. Using a digital multimeter set at 20 VDC range, measure the voltage from ground (J390 pin 2) to the +15 V test pad. Adjust the ±15 V ADJ for +16 V.
2. Set the digital multimeter to the 10 VDC range. Measure the voltage from ground (J390 pin 2) to the +5 V test pad. Adjust the 5 V ADJ for 5.15 V.
3. Connect the negative lead to the 3 V sense at J290 pin 2. Place the positive lead on the 5 V test pad. Adjust the 2 V ADJ for 2.1 V.

This concludes the power supply adjustments

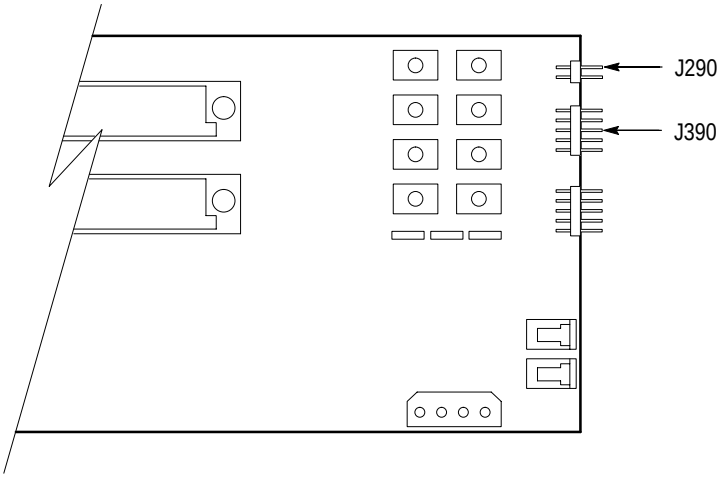


Figure 5–1: Location of J290 and J390 on the Backplane Board

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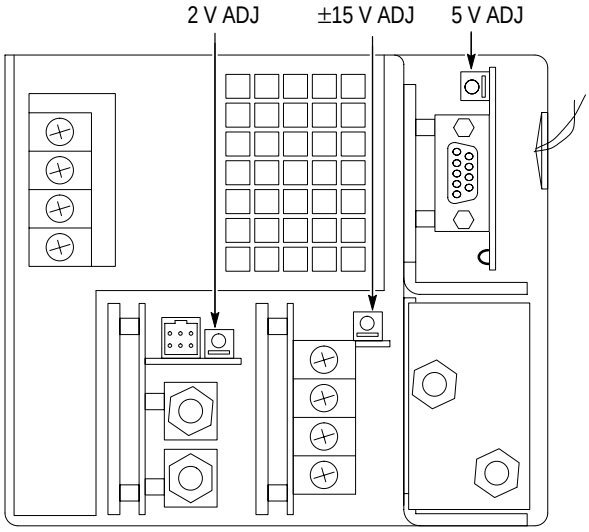


Figure 5–2: Power Supply Adjustment Locations

4. Power off the system unit and reinstall the fan frame. When replacing the fan make sure the media ribbon cables are out from under the lip of the fan frame and not in front of the fans. This ensures that the cables are not pinched and that airflow to the card cage is not obstructed.

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92C96 Adjustments

Few adjustments are necessary for the 92C96 Module. The Data and Clock Threshold voltages are set (± 75 mV) at the factory and should not require further adjustment.

Use the procedure in this section to adjust the Data and Clock Threshold gain and reference. This procedure also allows you to check the variable range (–4.00 to +8.75) and accuracy as well as the fixed settings: ECL, TTL, and CMOS. The procedure outlines seven adjustments: PRREF, CREF-zero, DREF-zero, CREF-gain, DREF-gain, CTHRESH and DTHRESH. Refer to Figure 5–3 as you perform this procedure.

NOTE. *Install the module to be adjusted into slot 3. Remove any module from slot 2.*

Equipment Setup

Use the following test equipment and TLA 510 or 520 setups for these procedures.

1. Set the digital voltmeter (DVM) or digital multimeter to the 20 VDC range.



CAUTION. *When powering off the system unit, wait at least 30 seconds before disconnecting the power cord. This allows the system unit to complete file-management procedures and move the hard-disk drive head to a safe position.*

2. Power off the logic analyzer and remove the power cord from the system unit.
3. Remove the system unit top cover and card cage door.
4. Place the system unit on its right side (disk drive and power supply down) to reach the test points and adjustments.
5. Power on the logic analyzer.

Threshold Adjustment

Use the following steps to adjust the Data and Clock threshold gain and reference. Refer to Figure 5–3 to locate the adjustments and test points.

1. Select the 92C96 Channel menu.
2. Press **F5: DEFINE THRESHOLD**, and set both the Clock and Data Thresholds to VAR –4.00V.
3. Press **F8: EXIT & SAVE**.
4. Select the 92C96 Clock menu.
5. Select **External** for the Module Clock selection.

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6. Refer to Figure 5–3 and connect the DVM's Low and High Input leads as follows:

   Low Input lead to +5 V (C342 +lead)

   High Input lead to PRREF (TP324)

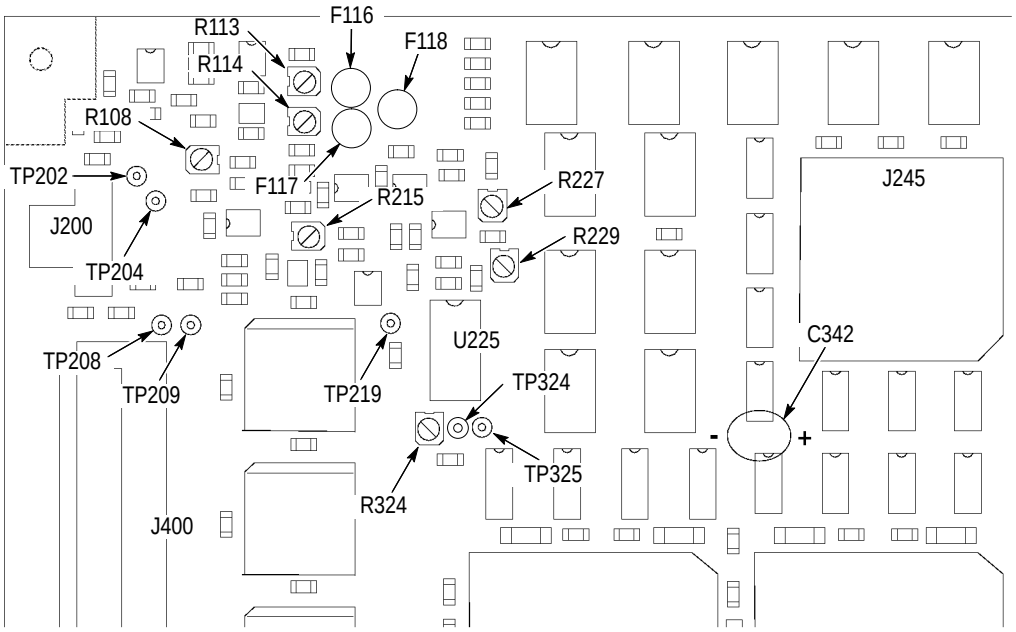


Figure 5–3: Data and Clock Threshold Test Points and Adjustments Locations

7. Adjust R324 for –1.680 V (±90 mV).
8. Move the DVM's Low Input lead to TP325 (ground).
9. Press **F1: START,** wait for the Slow Clock message to appear, and press **F1: STOP** before setting the thresholds.
10. Move the DVM's High Input lead to CREF (TP202).
11. Adjust R227 for –4.000 V (±25 mV).
12. Move the DVM's High Input lead to DREF (TP204).
13. Adjust R108 for –4.000 V (±25 mV).
14. Select the 92C96 Channel menu.
15. Press **F5: DEFINE THRESHOLD**, and set both the Clock and Data Thresholds to VAR +8.75 V.

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16. Press **F8: EXIT & SAVE**.

17. Press **F1: START**, wait for the Slow Clock message to appear, and press **F1: STOP** before setting the thresholds.

18. Adjust R215 for +8.750 V (±25 mV) at DREF (TP204).

19. Move the DVM's High Input lead to CREF (TP202).

20. Adjust R229 for +8.750 V (±25 mV).

The following steps are for adjusting the Divide-by-7 threshold amplifiers.

21. Connect the DVM's Low and High Input Leads as follows and note the measured value:

    Low Input lead to PREF (TP219)

    High Input lead to DREF (TP204)

22. In Table 5–2, locate the PREF-DREF voltage that is closest to the voltage measured in step 21 and note its Divide-by-7 value. If the PREF-DREF voltage measured is out of the range of this table, then divide the value by seven. Note that the Divide-by-7 voltages are negative numbers.

Table 5–2: Threshold Adjustment Voltages

PREF-DREF	Divide-by-7	PREF-DREF	Divide-by-7
5.553	0.7933	5.563	0.7947
5.554	0.7934	5.564	0.7949
5.555	0.7936	5.565	0.7950
5.556	0.7937	5.566	0.7951
5.557	0.7938	5.567	0.7953
5.558	0.7940	5.568	0.7954
5.559	0.7941	5.569	0.7956
5.560	0.7943	5.570	0.7957
5.561	0.7944	5.571	0.7959
5.562	0.7946	5.572	0.7960

23. Move only the DVM High Input lead to DTHRESH (TP209).

24. Adjust R114 for a DVM reading equal to the Divide-by-7 value determined in step 22 (±25 mV).

25. Move only the DVM High Input lead to CREF (TP202).

26. Again, locate the voltage and its Divide-by-7 value using Table 5–2.

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27. Move only the DVM High Input lead to CTHRESH (TP208).
28. Adjust R113 for a DVM reading equal to the Divide-by-7 value determined in step 26 (±25 mV).

Threshold Verification

The following steps check the fixed and variable threshold settings.

1. Connect the DVM Low and High Input leads as follows:

   Low Input lead to GND (TP325)

   High Input lead to CREF (TP202)

2. Select the 92C96 Channel menu.
3. Press **F5: DEFINE THRESHOLD**, and set both the Clock and Data Thresholds to VAR –1.80 V.
4. Press **F8: EXIT & SAVE**.
5. Press **F1: START**, wait for the Slow Clock message to appear, and press **F1: STOP** before setting the thresholds.
6. Check for –1.800 V (±25 mV).
7. Move the DVM High Input lead to DREF (TP204)
8. Check for –1.800 V (±25 mV).
9. For each of the threshold voltages in the table below, perform the following:
   a. Set the Clock and Data thresholds.
   b. Start and stop the 92C96 Module.
   c. Check both the CREF and DREF test point voltages in Table 5–3. If any settings are not within tolerance, recheck their adjustments. If they are still out of tolerance, the module may be in need of repair.

Table 5–3: CREF and DREF Threshold

Thresholds	CREF T.P.	DREF T.P.
TTL	+1.5 V (±75 mV)	+1.5 V (±75 mV)
ECL	–1.3 V (±75 mV)	–1.3 V (±75 mV)
CMOS	+2.5 V (±75 mV)	+2.5 V (±75 mV)
–4.00	–4.00 V (±75 mV)	–4.00 V (±75 mV)
+8.75	+8.75 V (±75 mV)	+8.75 V (±75 mV)

10. Remove the DVM leads.

This concludes the 92C96 Module adjustments.

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92S16 Coarse Adjustment Procedure

The following procedure provides instructions for the 92S16 Pattern Generator Module's coarse adjustments. These adjustments are performed at the factory and need normally be done only after extensive repair.

This 92S16 Pattern Generation Module adjustment procedure presented here contains four delay adjustments and a DAC adjustment for the P6460 External Control probe. The 92S16 contains six delay lines in three different circuits. The register timing circuitry requires one adjustment, the pod clock positioning circuitry requires three, and the deskew circuitry between the pod clocks requires two.

The 92S16 Adjustment Procedure consists of five separate procedures that must be performed in the order given, unless otherwise specified.

1. DAC Threshold Accuracy Adjustment
2. First Latch Clock Delay Adjustment
3. Probe Clock Delay Adjustment
4. Pod Clock Positioning Delay Adjustment
5. Last Latch Clock Delay Adjustment

Equipment List

You will need the following equipment to perform the adjustments in this procedure. Tektronix part numbers are in parenthesis.

- TLA 510 or 520 system unit and X Terminal
- 92S16 Pattern Generation card with a P6460 External Control Probe and two P6463A Probes.
- 350 MHz Oscilloscope (Tektronix 2465B)
- Two P6137 Oscilloscope Probes
- Subminiature to miniature adapter (Tektronix part number 013-0202-XX)
- Two Dual-lead Adapters (Tektronix part number 015-0325-XX)
- Digital Multimeter (3.5 digits, 0.1% VDC)
- 200 MHz Digital Counter
- 200 MHz Signal Generator with variable output
- Delay line Alignment Tool (Tektronix part number 003-1134-XX)
- BNC-T Connector (Tektronix part number 103-0030-XX)
- BNC-to-Oscilloscope Probe Adapter (Tektronix part number 013-0084-02)

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- BNC-to-Test Point Adapter (refer to *Test Fixtures* on page 5–27)
- 92S16 Threshold Fixture (refer to *Test Fixtures* on page 5–27)

92S16 Test Points Explained

Throughout this procedure you will be asked to attach an oscilloscope probe to a test point. Each test point consists of two pins — a signal pin and a ground pin. The signal pin on the 92S16 Pattern Generator module is identified by a round pad around the pin without any identifying markings. The test point's ground pin (pin 1) on the 92S16 card is identified by a square pad around the pin.

Test points in this text are usually identified as TPn, where n is the test point's number. Therefore, an instruction might say "connect oscilloscope probe channel 1 to test point TP54". This means connect the oscilloscope channel 1 probe input to the signal pin of test point TP54 and connect the oscilloscope probe's ground lead to the ground pin of test point TP54. This is true throughout this procedure, unless the procedure specifies otherwise.

NOTE. *Ground the oscilloscope probe at the same test point as you pick up the signal. Refer to the* Diagrams *chapter for component and test point location diagrams.*

Equipment Setup

Use the following steps to set up the TLA 510 or 520 system unit for the 92S16 adjustments.

1. Ensure that the TLA 510 or 520 system unit is powered down and that the power cord is disconnected.



CAUTION. *When powering off the system unit, wait at least 30 seconds before disconnecting the power cord. This allows the system unit to complete file-management procedures and move the hard-disk drive head to a safe position.*

2. Remove the system unit top cover and card-cage door.



CAUTION. *Observe anti-static precautions before handling any TLA 510 or 520 system unit card; otherwise, damage may occur.*

3. To be able to reach all the test points and delay line adjustments, place the system unit on its right side (disk drives and power supply down).

NOTE. *Make sure there is adequate clearance for the power supply air intake.*

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4. Check the location of the 92S16 module. If necessary, move it to slot #3. This step is necessary to access all the adjustment points on the module.
5. Ensure that the square-pin jumper is installed at J500 on the 92S16. This jumper is located near the front edge of the board. The TLA 510 or 520 system unit controller cannot communicate with the 92S16 without this jumper.
6. Ensure the system unit is properly connected to the terminal. Connect both the terminal and system unit to the power receptacle. Power on the terminal and then the system unit. Check that the TLA 510 or 520 system unit passes all the power on diagnostics, including the 92S16.
7. Locate the oscilloscope so that you can make a connection to the card under test and adjust the oscilloscope simultaneously.

You can now proceed to the DAC Threshold Accuracy Adjustment procedure.

DAC Threshold Accuracy Adjustment

Use the following procedure to adjust the 92S16's Digital Analog Converter (DAC) threshold accuracy for use with any P6460 External Control Probe (92S16 pod D). This adjustment requires a 92S16 Threshold Fixture. Refer to *Test Fixtures* on page 5–27.

Refer to *Diagrams* for the component locations.

***NOTE**. If you are performing only timing alignments, skip this procedure and proceed to the next one.*

---

1. Connect the 92S16 Threshold Fixture directly to the 92S16 card's pod D connector (J240) so that the fixture's pin 1 connects to pin 1 of J240.
2. Select the 92S16 Module and select the Config menu.
3. Move the cursor to the P6460 Threshold Level field and select VAR. Move the cursor to the right and select or enter 0.00V.
4. Connect the positive DMM lead to pin 13 of the threshold fixture and the negative lead to the ground point (the junction of the three wires).
5. Press **F1: START**. Adjust R320 for a DMM reading of 0.00 V ±2 mV).
6. Select the 92S16 Config menu.
7. Move the cursor to the P6460 Threshold Level field.
8. Change the VAR value to +6.35 V (maximum value).
9. Press **F1: START**. Adjust R322 for a DMM reading of –1.587 V ±12 mV).

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10. Select the 92S16 Config menu.
11. Move the cursor to the P6460 Threshold Level field.
12. Change the VAR value to –6.40 V (minimum value).
13. Press **F1: START**. Check that the DMM reads +1.600 V ±12 mV. If necessary, readjust R320 to equalize the difference between the maximum and minimum values. The two voltages should be within 6 mV of each other.
14. Disconnect the DMM leads and remove the threshold fixture.

Clock Control Adjustments

The following procedures are used to adjust these four circuits for their proper delay. Perform the adjustments in the order shown.

- First Latch clock
- Probe clock
- Pod clock Positioning
- Last Latch clock

Adjustment Setup. Use these steps to set up the TLA 510 or 520 system unit for the delay line adjustments. The same 92S16 program menu is used for all following adjustments.

1. Power off the TLA 510 or 520 and remove all delay line covers from the 92S16 board.



CAUTION. *Before attaching any probe, power off the system unit to prevent damage to the pattern generator board circuits.*

2. Connect the P6463A pattern generator probes to pod A and B of the 92S16.
3. Power on the TLA 510 or 520 system unit. Check that all diagnostics pass.
4. Select the 92S16 Module and select the Config menu.
5. With the cursor in the Clock field, select the External clock with a rising edge (⁄).
6. Move the cursor to the P6460 Threshold Level field, select VAR and set the threshold level to 0.00 volts.
7. Select the 92S16 Program menu. Move the cursor to the Sequence 0 Label field and type in **Start**.

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8. Move the cursor two columns to the right and type in **FFFF** for the Sequence 0 data field.

9. Move the cursor to the Sequence 1 Instruction field and select **Jump**. Move the cursor to the right and type in **Start** for the destination. Move the cursor to the right again, and type 0000 in the Sequence 1 data field.

10. Connect the P6460 External Control Probe to the 92S16 Pod D connector. Connect the Clock input (white lead) and user GND of the P6460 probe to the BNC-to-Test Point Adapter. Connect the Test Point Adapter to one side of a BNC-T, and connect a BNC oscilloscope probe adapter to the other side of the BNC-T. Connect the BNC-T to the signal generator's output.

11. Connect the channel 2 oscilloscope probe to the BNC oscilloscope probe adapter.

First Latch Clock Adjustment. Use the following steps to adjust the First Latch Clock delay line. Perform the measurements at the VBB point (VBB=VCC–1.3V).

***NOTE**. While performing the following adjustments the Pattern Generator module may unexpectedly stop. This is due to noise induced by probing internal clock test points. If this occurs, simply restart the Pattern Generator module and continue with the procedure.*

The following oscilloscope setup needs to be done only once during the 92S16 adjustments.



***CAUTION.** Do not allow the oscilloscope probe ground to encounter any point on the board other that the specified GND test point. Doing otherwise may result in damage to the board's circuits.*

1. Use the following steps to set up both channels of the oscilloscope:

   a. Set both of the vertical input controls to 0.5 V/div. Set the horizontal timebase to 1 ns/div and signal coupling to DC. Set the trigger to the rising edge of channel 2.

   b. Attach a dual-lead adapter to the channel 1 oscilloscope probe.

   c. Connect the black lead (ground) of this dual-lead adapter to the ground pin (pin 1) of TP132.

   d. Briefly connect the white lead of the same dual-lead adapter to U624-16 (+5 V)

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e. Position the +5 VDC level at 1.3 V above the center horizontal graticule line of the oscilloscope. The graticule center line is now set at VBB.

2. Set up the signal generator and counter as follows:

a. Disconnect the P6460 External Control Probe and the BNC-to-Test Point Adapter from the BNC-T at the signal generator's output.

b. Connect a coaxial cable between the signal generator output and the digital counter input. Adjust the signal generator frequency output for a period of 26.50 ns (26.47 ns – 26.53 ns) Adjust the oscilloscope trigger level for a stable trigger condition, then use channel 2 of the oscilloscope to set the output amplitude to 2 V peak to peak.

c. Reconnect the BNC-to-Test Point Adapter and P6460 External Control Probe to the signal generator's output.

d. Reset the oscilloscope to display only Channel 1.

3. Start the 92S16 Module by pressing **F1: START**.

NOTE. *Try to keep all oscilloscope measurements within the center six divisions of the horizontal graticule area. This will ensure the greatest accuracy.*

Following references in this procedure to "Graticule Center" refer to the junction point of the center horizontal and center vertical graticule lines.

---

4. Connect the channel 1 oscilloscope probe (white lead of the dual lead adapter) to pin 2 of test point TP108. Connect channel 1 GND (black lead of dual lead adapter) to pin 1 of test point TP108. Use the horizontal position to adjust the rising edge of the waveform to the graticule center.

5. Move the channel 1 oscilloscope probe to pin 2 of test point TP132. Connect channel 1 GND to pin 1 of test point TP132. Adjust DL200 so that the rising edge of the resulting waveform is located at the graticule center (±200 ps). Replace the delay line cover.

6. Press **F1: STOP**.

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Probe Clock Adjustment. Use the following steps to adjust the delay lines in the probe clock circuitry.

1. Press **F1: START**.
2. Move the channel 1 oscilloscope probe to pin 2 of TP158 (This test point is located near the probe connections at the rear edge of the board.) Connect the channel 1 ground to pin 1 of test point TP158. Adjust the oscilloscope so that the rising edge of the displayed waveform is located at the graticule center.
3. Move the channel 1 oscilloscope probe to pin 2 of test point TP154, and ground the oscilloscope probe at pin 1 of the same test point.
4. Adjust DL240 so that the rising edge of the displayed signal is 0.8 ns (±200 ps) to the right of the graticule center. Replace the delay line cover.
5. Move the channel 1 oscilloscope probe to pin 2 of TP156. Adjust DL250 so that the rising edge of the displayed signal is also located 0.8 ns (±200 ps) to the right of the graticule center. Replace the delay line cover.
6. Press **F1: STOP**.

Pod Clock Positioning Adjustment. Use the following steps to adjust the Pod Clock Positioning delay lines.

1. Select the 92S16 Channel menu. Press **F6: DEFINE CHANNEL**.
2. Move the cursor to the Pod field and select 3B. Move the cursor to the Clock Delay field and select –5 ns.
3. Move the cursor back to the Pod field and select 3A. Move the cursor to the Clock Delay field and verify that it is set to 0 ns.
4. Press **F8: EXIT & SAVE**. Press **F1: START**.
5. The channel 1 oscilloscope probe should still be connected to pin 2 of test point TP156. If it is not, connect it to the test point. Connect channel 1 ground to pin 1 of the same test point. Move the trace horizontally so that the rising edge of the signal is two major divisions (2 ns) to the left of the graticule center.
6. Move the channel 1 oscilloscope probe to pin 2 of test point TP154 and ground the oscilloscope probe to pin 1 of the same test point.
7. Adjust DL220 so that the rising edge of the channel 1 signal is three major divisions (3 ns) to the right of the graticule center. This results in a 5 ns (±200 ps) total delay from test point TP156 to TP154. Then replace the delay line cover.

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8. Press **F1: STOP**. Select the 92S16 Channel menu. Press **F6: DEFINE CHANNEL**.

9. Move the cursor to the Pod field and select 3B. Move the cursor to the Clock Delay field and select +5 ns. Leave pod 3A Clock Delay set to 0 ns.

10. Press **F8: EXIT & SAVE**. Press **F1: START**.

11. The channel 1 oscilloscope probe should still be connected to test point TP154. Adjust the horizontal position so that the rising edge of the signal is two major divisions (2 ns) to the left of the graticule center.

12. Move the channel 1 oscilloscope probe to pin 2 of test point TP156 and ground the oscilloscope probe to pin 1 of the same test point.

13. Adjust DL230 so that the rising edge of the channel 1 signal is three major divisions (3 ns) to the right of the graticule center (see Figure 5–4). This results in a 5 ns (±200 ps) total delay from TP154 to TP156. Replace the delay line cover.

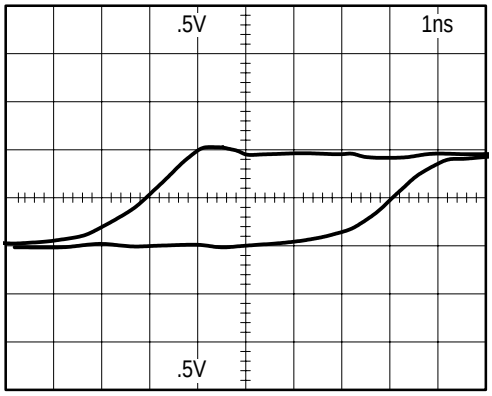


Figure 5–4: Clock Positioning Delay Line Adjustment

14. Press **F1:Stop**.

Last Latch Clock Adjustment. Use the following steps to adjust the Last Latch Clock delay line. Perform these measurements at the Vbb point (Vbb=Vcc–1.3V).

1. Set up the signal generator as follows:

   a. Disconnect the P6460 External Control Probe and the BNC-to-Test Point Adapter from the signal generator's output.

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b. Connect a coaxial cable between the signal generator output and counter channel A input. Adjust the signal generator output for a period of 46.00 ns (45.97 ns – 46.03 ns).

c. Reconnect the P6460 External Control Probe and the BNC-to-Test Point Adapter to the signal generator's output. Adjust the oscilloscope trigger level for a stable trigger condition, then use channel 2 to set the output amplitude to 2 V peak to peak.

d. Reset the oscilloscope to display only Channel 1.

2. Start the 92S16 Module by pressing **F1: START**.
3. Connect the oscilloscope probe channel 1 to pin 2 of test point TP108. Connect the oscilloscope probe ground to pin 1 of test point TP108. Then position the resulting rising edge of the waveform to the graticule center.
4. Move the oscilloscope probe channel 1 to pin 2 of test point TP154. Connect the oscilloscope probe ground to pin 1 of test point TP154. Then adjust DL210 so that the rising edge of the resulting waveform is located at the graticule center.(±200 ps) Then replace the delay line cover.
5. Press **F1: STOP**.

This completes the coarse adjustments for the 92S16.

92S16 Probe Tip Adjustment Procedure

This procedure is used to deskew the 92S16 Pattern Generator module's clock outputs to the specifications stated in the *Specifications* chapter.

***NOTE**. This procedure assumes that a coarse adjustment of the Pattern Generator module was previously performed.*

Equipment List

You will need the following equipment to perform these probe tip adjustments. Tektronix part numbers are given in parenthesis.

- TLA 510 or 520 system unit
- X Terminal
- 92S16 Pattern Generation card with a P6460 External Control Probe and two P6463A probes.
- 350 MHz Oscilloscope (Tektronix 2465B)
- Two P6137 Oscilloscope Probes
- Two Dual-Lead adapters (Tektronix part number 015-0325-XX)

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- Digital Multimeter
- 200 MHz Signal Generator
- Variable Power Supply (+5 V, 2 A min. PS282)
- Delay line alignment Tool (003-1134-XX)
- Decoupling Fixture (see *Test Fixtures* on page 5–27)
- Two 92S16 Clock Skew Fixtures (see *Test Fixtures* on page 5–27)
- BNC-to-Test Point Adapter (see *Test Fixtures* on page 5–27)
- BNC-T connector (Tektronix part number 103-0030-XX)
- BNC-to-Probe adapter (Tektronix part number 013-0084-XX)



CAUTION. *When adjusting the delay lines in this procedure, use only the alignment tool described in the equipment list. Any other tool may damage the circuit components.*

Equipment Setup

Use the following steps to set up the TLA 510 or 520 for the probe tip adjustments.

1. Ensure that the TLA 510 or 520 is powered down and that the power cord is disconnected.



CAUTION. *Before installing or removing any card, power off the system unit and disconnect the power cord. Damage to circuitry may occur if cards are installed or removed while the system unit is receiving power. Before you unplug the power cord, power off the system unit (using the front-panel DC power switch) and wait at least 30 seconds to allow sufficient time for the hard-disk drive head to park and lock in a safe position.*

2. Remove the system unit top cover and card-cage.



CAUTION. *Observe anti static precautions before handling any TLA 510 or 520 card; otherwise, damage may occur. To avoid static damage, store any unused modules in antistatic packaging.*

3. To be able to reach all the test points and delay line adjustments, place the system unit on its right side (disk drives and power supply down).

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***NOTE**. Make sure there is adequate clearance for the power supply air intake.*

4. Ensure that the square-pin jumper is installed at J500 on the 92S16 card. This jumper is located near the front edge of the board.
5. Remove the 92S16 pattern generator card delay line cover from DL250 only.
6. Install the 92S16 card into slot #3.
7. Ensure that the system unit is properly connected to the terminal. Connect both the terminal and system unit to the power receptacle.
8. Place the oscilloscope close enough to the system unit so that you can reach both the oscilloscope controls and the system unit at the same time.
9. Attach the P6463A Probes to the 92S16 pods A and B.
10. Connect the P6460 External Control probe to pod D of the 92S16 to provide an external clock signal.
11. Connect the pattern generator probes to the power supply by way of the Decoupling Fixture and connect the probe's red leads to +5 V. Connect the black leads to the power supply ground.
12. Power on the terminal first and then the system unit. Check that the TLA 510 or 520 passes all the power on diagnostics.

Programming the 92S16 For Deskew Adjustment

Before you can deskew 92S16 pattern generator clocks, you must first program the 92S16 for that particular purpose. Follow these steps to program the Pattern Generator module.

1. Select the 92S16 Module and select the Config menu.
2. Move the cursor to the Clock field and select the External clock with a rising edge (⟋).
3. Move the cursor to the P6460 Threshold Level field and select VAR. Then move to the Voltage field and select 0 V.
4. Select the 92S16 Program menu. Move the cursor to the Sequence 0 label field and type in **Start**.
5. Move the cursor to the Sequence 1 instruction field and select Jump.
6. Move the cursor to the right and type in **Start** for the destination.
7. Move the cursor to the right again and type **0000** into the Sequence 0 data field and **FFFF** into the Sequence 1 data field, if the fields contain other data.
8. Press **F8: Exit & Save**.

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Making Test Connections

1. Use these steps for a preliminary oscilloscope setup:
   a. Set both vertical input controls to 0.5 V/div. Set the horizontal timebase to 100 ns/div and signal coupling to DC.
   b. Set oscilloscope channel 2 as the oscilloscope trigger source.
2. Follow these steps to set up the signal generator:
   a. Connect the P6460 clock input to the BNC-to-Test Point Adapter. Connect the test point adapter to a BNC-T adapter and connect a oscilloscope probe-to-BNC adapter to the other side of the BNC-T. Then connect the BNC-T to the signal generator.
   b. Set the Signal Generator to an output frequency that is one-half of the desired pattern generator output frequency.
   c. Connect oscilloscope probe channel 2 to the signal generator output by way of the BNC-T probe adapter.
   d. View oscilloscope channel 2 momentarily and adjust the signal generator output to a 3 V peak-to-peak signal.
   e. Then set the oscilloscope's horizontal time base to 1 ns/div and display channel 1 only.
3. Press **F1:Start**.

Adjusting the Probe Tip Clock

You are now ready to make the probe tip clock adjustments.

1. Connect the pod A clock output to the Clock Skew fixture with the ground pin connected to the fixture's ground or common side.
2. Connect the pod B clock output to the other Clock Skew fixture.
3. Connect oscilloscope probe channel 1 to the pod A clock output on the Clock Skew fixture. Connect the oscilloscope probe channel 1 ground to the common side of the Clock Skew fixture.
   a. For TTL operation the reference is 1.4 V to 1.5 V above the ground reference. Thus set the ground reference three major divisions below the horizontal graticule center.
   b. Adjust the horizontal positioning so the rising edge of the displayed clock waveform is located at graticule center.

      The remaining skew adjustments are compared to and adjusted to match this probe tip adjustment.

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4. Connect oscilloscope probe channel 1 to the clock output of pod B. Then adjust DL250 to position the rising edge of the displayed waveform at the graticule center ±200 ps.

You now have deskewed both clocks at the probe tip. This completes the 92S16 pattern generator probe tip adjustments.

92S16 Clock and Data Characterizing Procedure

To achieve greater accuracy at the probe tip, you can characterize each individual probe's data channel against the clock channel. You can perform this procedure anytime extreme probe tip accuracy is required.

Equipment List

You will need the following equipment to perform this procedure. Tektronix part numbers are in parenthesis.

- TLA 510 or 520 system unit
- X Terminal
- 92S16 Pattern Generation card with a P6460 External Control Probe and two P6463A Probes.
- 350 MHz Oscilloscope (Tektronix 2465B)
- Two P6137 Oscilloscope Probes
- Two Dual-Lead Adapters (Tektronix part number 015-0325-XX)
- Digital Multimeter
- 200 MHz Sinewave Generator
- Variable power supply (+5 V, 2 A minimum, PS282)
- Decoupling Fixtures (See *Test Fixtures* on page 5–27)
- Two 92S16 Clock Skew Fixtures (See *Test Fixtures* on page 5–27)
- BNC-to-Test Point Adapter (See *Test Fixtures* on page 5–27)
- BNC-T connector (Tektronix part number 103-0030-XX)
- BNC-to-oscilloscope probe adapter (Tektronix part number 013-0084-02)

Equipment Setup

Use the following steps to set up the TLA 510 or 520 for the adjustments.

1. Ensure that the system unit is properly connected to the terminal. Connect both the terminal and system unit to the power receptacle.

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2. Attach the P6463A probes to the 92S16 pod A and B. Connect the P6460 External Control probe to pod D of the 92S16.
3. Place the oscilloscope close enough to the system unit so that you can reach both of them at the same time.
4. Set the variable power supply to +5 V. Connect the pattern generator probes to the power supply by way of the decoupling fixture and connect the probe's red leads to +5 V and black leads to the power supply ground.
5. Power on the terminal first and then the system unit. Check that the TLA 510 or 520 passes all the power on diagnostics.

Programming 92S16 For Characterization

Follow these steps to program the 92S16 Pattern Generator module for the clock/data characterization:

1. Select the 92S16 Module and select the Config Menu.
2. Move the cursor to the Clock field and select the External clock with a rising edge (⁄).
3. Move the cursor to the P6460 Threshold Level field and select VAR. Then move to the voltage field and select 0 V.
4. Select the 92S16 Program menu. Move the cursor to the Sequence 0 label field and type in **Start**.
5. Move the cursor to the Sequence 1 instruction field and select **Jump**.
6. Move the cursor to the right and type in **Start** for the destination.
7. Move the cursor to the right again and type **0000** into the Sequence 0 data field and **FFFF** into the Sequence 1 data field, if the fields contain other data.
8. Press **F8: Exit & Save**.

Making Test Connections

1. Set up the oscilloscope as follows:

   The channel 2 oscilloscope probe should contain the dual-lead adapter.

   a. Set both vertical input controls to 0.5 V/div. Set the horizontal timebase to 10 ns/div and signal coupling to DC.

   b. Set channel 2 as the oscilloscope trigger source.

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2. Follow these steps to setup the signal generator:

   a. Connect the P6460 clock input (white lead) to the BNC-to-Test Point Adapter. Connect the test point adapter to a BNC-T adapter and connect a oscilloscope probe-to-BNC adapter to the other side of the BNC-T. Then connect the BNC-T to the signal generator.

   b. Set the Signal Generator to an output frequency that is one-half of the desired pattern generator output frequency.

   c. Briefly connect the oscilloscope probe channel 2 to the signal generator by way of the BNC-T probe adapter.

   d. View the oscilloscope channel 2 and adjust the signal generator output for a 3 V peak-to-peak signal.

   e. Then set the oscilloscope's horizontal timebase to 1 ns/div and look at channel 1 only.

3. Select the pattern generator probe to be characterized and connect its probe's clock and one data channel to the two Clock Skew fixtures. Note that the ground side of the podlet connects to the fixture's common side.

4. Connect the oscilloscope probe channel 2 to the clock pin of the pattern generator probe to be characterized.

5. Press **F1: Start**.

6. Connect oscilloscope probe channel 1 to the clock pin on the Clock Skew fixture. Connect the oscilloscope probe channel 1 ground to the common side of the Clock Skew fixture.

   For TTL operation, the reference is 1.4 V to 1.5 V above the ground reference. Thus, set the ground reference three major divisions below the horizontal graticule center.

Characterizing the Probes

Perform the following steps to characterize the probes:

1. Use the oscilloscope's horizontal position control to locate the rising edge of the clock waveform at the graticule center. This is where all skew measurements are compared.

2. Connect the oscilloscope probe channel 1 to the first data channel to be characterized. Record the skew value of the probe's data channels for the rising and falling edges with respect to the graticule center. You can easily see both edges simultaneously by adjusting the oscilloscope 's trigger holdoff control.

   The skew is the time difference between the active edge of the probe clock and the data channel. This difference should not be greater than 1.5 ns.

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***NOTE**. All measurements are taken with respect to the probe clock, located in step 1 above.*

3. Repeat step 2 for all data channels on this probe and record the skew value of each data channel for the rising and falling edges of that data channel.
4. After you have recorded all data values, you can return to the Define Channel overlay and change the clock polarity:\.
5. Repeat steps 1 through 3, except locate the falling edge of the clock waveform at the center graticule in step 1.
6. Repeat the procedure for any additional probes to be characterized.
7. Press **F1: STOP**.

This completes the clock and data characterization procedure.

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Test Fixtures

Most functional check procedures, performance verification procedures, and some adjustment procedures require the use of a test fixture. Table 5–4 lists the fixtures and briefly describes their use.

Table 5–4: Test Fixtures

Fixture Name	Use of Fixture
92C96 Acquisition Fixture	Use with 92C96 module to connect the Probe Lead Set to a signal source (BNC). (See Figure 5–5.)
92S16 Threshold Fixture	Use with 92S16 module to adjust threshold settings of the P6460 probe. (See Figure NO TAG.)
General Purpose Acquisition Fixture	Use with 92S16 module to connect pattern generator probe outputs to acquisition probe inputs. (See Figure 5–7.)
92S16 Decoupling Fixture	Use with Pattern Generation Probes to decouple probe power leads from the output of the external power supply. (See Figure 5–8.)
92S16 Clock Skew Fixture	Use with 92S16 modules to connect an oscilloscope probe to the pattern generator probe outputs. (See Figure 5–9.)
BNC-to-Test Point Adapter	Use with 92S16 Module to connect the P6460 External Control Probe to a signal source (BNC) See Figure 5–10
Discrete I/O Fixture	Use with 92PORT software and Discrete I/O output on the system unit rear panel.

92C96 Acquisition Fixture

This procedure lists the steps needed to build the 92C96 Acquisition Fixture. This fixture is designed to interconnect the 92C96 Module Sync Out signal to two 92C96 8-Channel Probes. The ground side pins are ganged together. The signal side pins are also ganged together and are terminated to ground through two parallel 100 Ω resistors.

Material Required

The following material is required to build the fixture.

- 2 × 40 wide square-pin strip
- Two 4-inch long, 22 gauge bare wires
- Two 100 Ω resistors, 5%, ¼ watt (Tektronix part number 315-0101-XX)
- BNC RF connector (Tektronix part number 131-0768-XX)
- Solder and soldering iron

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Build Procedure

Refer to Figure 5–5 and use the following steps to build the acquisition fixture.

1. Use diagonal cutters to cut a block of 20 pairs of square pins from the 2 × 40 square-pin connector strip.
2. Solder one 4-inch bare wire to all the square pins on the side with the longer pins, keeping the bare wire as far from the insulator as possible.
3. Turn the strip over and solder the other 4-inch bare wire to all the square pins on the other side of the pin strip. Cut off any excess length.
4. Check all solder connections, making sure that each pin on the fixture is soldered to the bare wire. Check that none of the pins on the top of the pin strip are soldered to the pins on the bottom.
5. Solder one 100 Ω resistor between the top and bottom rows of pins at one end of the fixture. Then solder the other 100 Ω resistor between the top and bottom rows of pins at the other end of the fixture.

***NOTE**. Make a 270° loop at each end of the resistors for easier soldering.*

6. Locate the BNC RF connector and clip off two adjacent mounting posts from one side of the outer ground ring of the connector.
7. Solder the center conductor of the BNC RF connector to the center of the bare wire on one side of the fixture. This side will be called the signal side of the fixture.
8. Solder the remaining two mounting posts to the other side of the fixture. This side will be called the ground side of the fixture.

This completes the construction of the 92C96 Acquisition Fixture.

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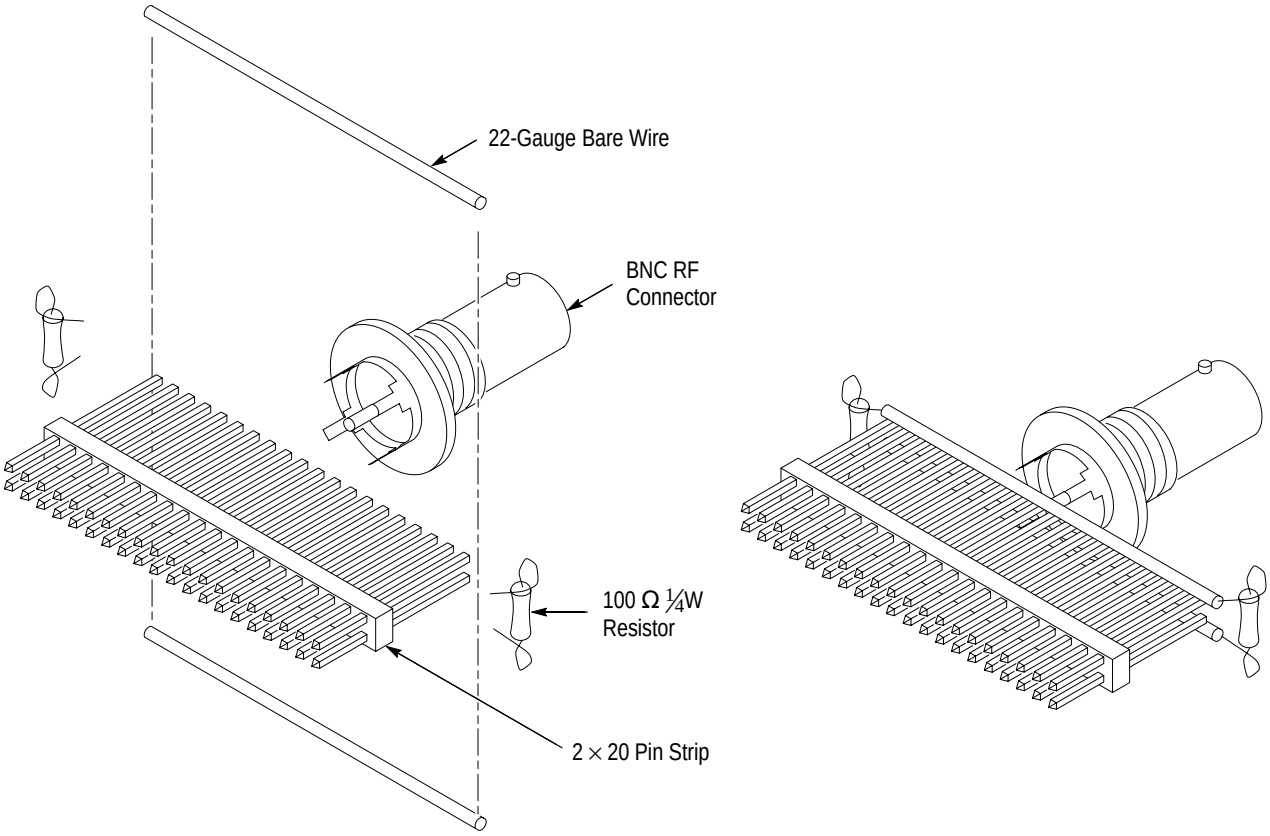


Figure 5–5: 92C96 Acquisition Fixture Construction

92S16 Threshold Fixture

The threshold fixture shown in Figure 5–6 is used for checking and adjusting the threshold setting on the 92S16 Pattern Generation Module with P6460 probe.

Equipment Required

You will need the following material to build the threshold fixture:

- Terminal connector holder, 2 holes × 8 holes, Tektronix part number 352-0484-00
- Five mini-PV female connectors, Tektronix part number 131-0707-00
- 10.5 kΩ resistor, 0.1%, Tektronix part number 321-0291-00
- 22-gauge wire
- Solder and soldering iron

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Build Procedure

Refer to Figure 5–6 and use the following steps to build the acquisition fixture.

1. Cut three lengths of wire, each approximately one inch long.
2. Connect three of the mini-PV connectors to the three lengths of wire.
3. Connect the remaining two mini-PV connectors to the resistor, one at each end.
4. Insert the mini-PV connectors (attached to the wires) into holes 1, 4, and 7 of the terminal connector holder. See Figure 5–6.
5. Solder the three free ends of the wires together. This is the signal ground.
6. Insert the two mini-PV connectors (attached to the resistor) into holes 13 and 16 of the terminal connector holder. Pin 13 is the test point for all measurements.



CAUTION. *When connecting this fixture to an acquisition board or pattern generator board probe connector, be sure to mate pin 1 of the fixture to pin 1 of the probe connector.*

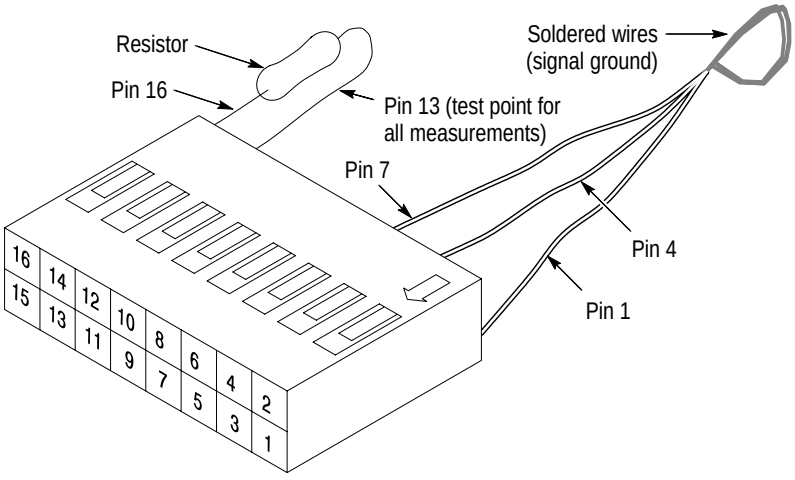


Figure 5–6: 92S16 Threshold Fixture

This completes the construction of the threshold fixture.

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General Purpose Acquisition Fixture

This procedure lists the steps needed to build a General Purpose Acquisition Fixture. The fixture shown in Figure 5–7 is used to connect the outputs of the pattern generation probes to the input of the data acquisition probes. This fixture is used with several of the functional check and performance verification procedures.

Equipment Required

Use the following material to build the General Purpose Acquisition Fixture.

- 2 × 40 wide pin strip (Tektronix part number 131-2171-00)
- 4-inch-long 22-gauge bare wire
- 18-inch insulated black wire with male banana jack ends
- Solder and a soldering iron

Build Procedure

Refer to Figure 5–7 and use the following steps to build the General Purpose Acquisition Fixture.

1. Place the 4-inch bare wire across one side of the 2 × 40 wide pin strip and solder it to all the pins on one side. Keep the bare wire as close to the insulator as possible. This will be used as the ground for the probe podlets.
2. Clip off one of the banana jacks of the 18-inch insulated black wire. Strip off ½ inch of the insulation and solder the end to the 4-inch bare wire on the pin strip. Make sure that the other end of the insulated black wire has a male banana jack on it.
3. Check all the solder connections, making sure that each pin in the pin strip (on one side of the fixture) is soldered to the 4-inch bare wire. Turn the fixture so that the bare wire is to the bottom. Check that none of the pins on the top of the pin strip are soldered.

This completes the construction of the General Purpose Acquisition Fixture.

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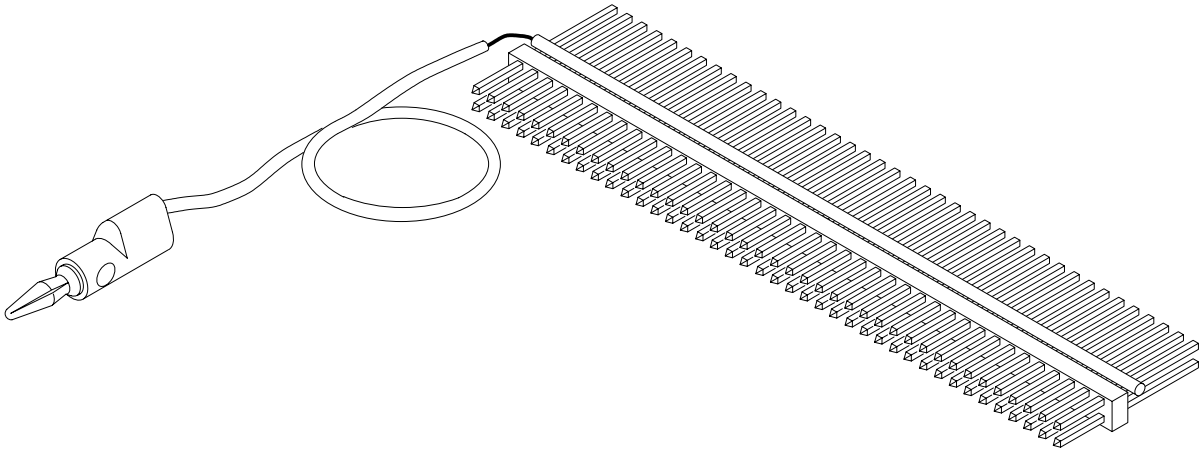


Figure 5–7: General Purpose Acquisition Fixture

92S16 Decoupling Fixture

This procedure lists the steps needed to build a decoupling fixture. The decoupling fixture shown in Figure 5–8 is used to decouple the power supply outputs connected to the pattern generation probes.

Equipment Required

You will need the following material to build the decoupling fixture.

- Square-pin connector (Tektronix part number 131-1634-XX)
- 3-inch-long 18-gauge bare wire
- 0.01 μF ceramic capacitor 20%, 50 V (Tektronix part number 283-0204-XX)
- 33 μF tantalum capacitor 20%, 10 V (Tektronix part number 290-0535-XX)
- Solder and a soldering iron

Build Procedure

Refer to Figure 5–8 and use the following steps to build the decoupling fixture.

1. Use diagonal cutters to cut a block of at least 12 square-pins from the square pin connector strip.
2. Clip the sixth and seventh square pins from both sides of the strip.
3. Place the 3-inch bare wire across one side of the square pin connector and solder it to all the pins. Keep the bare wire as close to the insulator as possible. Clip off any excess lead length of the bare wire.
4. Use the diagonal cutters to cut away the bare wire over the gap left by the sixth and seventh pins you cut off in step 2 above.

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5. Check all the solder connections, making sure that each pin of the pin strip is soldered to the bare wire. Turn the fixture so that the bare wire is to the bottom.
6. Connect a 33 μF tantalum capacitor across the gap on the fixture, taking note of where the positive side the capacitor is connected.
7. Connect a 0.01 μF capacitor in parallel with the 33 μF capacitor.
8. Mark the positive side of the fixture.

This completes the construction of the decoupling fixture.

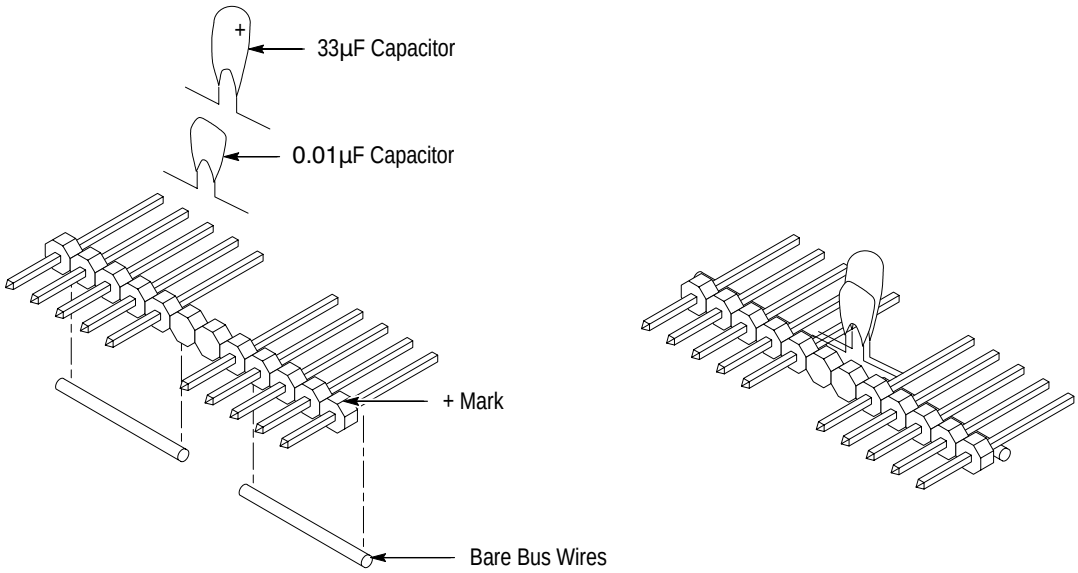


Figure 5–8: 92S16 Decoupling Fixture

92S16 Clock Skew Fixture

The Clock Skew Fixture consists of a 510 Ω resistor connected across a dual square pin connector. Its purpose is to provide a convenient method for connecting a oscilloscope probe to the P6463A probe podlets. The 510 Ω resistor provides the necessary termination. You will need to build at least two fixtures to be used for the 92S16 Performance Check Procedures.

Equipment Required

You will need the following material to build each Clock Skew Fixture:

- 2 × 10 square-pin connector (Tektronix part number 131-1614-XX)
- 510 Ω Resistor, ¼ watt (Tektronix part number 315-0511-XX)
- Solder and a soldering iron

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Build Procedure

Refer to Figure 5–9 and use the following steps to build the Clock Skew Fixture.

1. Use diagonal cutters to cut a pair of square-pins from the 2 × 10 square-pin connector strip.
2. Solder the 510 Ω resistor across the longer side of the two square pins.
3. Check that there is no solder bridge between the two square pins and clip off any excess resistor lead length.

This completes the construction of the Clock Skew Fixture.

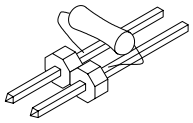


Figure 5–9: 92S16 Clock Skew Fixture

BNC-to-Test Point Adapter

The BNC-to-Test Point Adapter consists of a BNC-to-square pin adapter with 50 Ω termination. Its purpose is to connect the acquisition probe to a single pulse generator output without causing excessive capacitive and inductive loading. It also provides a convenient method for connecting the test oscilloscope's probe used to monitor the pulse or signal generator's output.

NOTE. *The lead distance from the ground pins to the BNC connector body is critical; keep this distance as short as possible. Any excessive lead length in the fixture will distort high-speed signals.*

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Equipment Required

You will need the following material to build the BNC-to-Test Point Adapter:

- BNC male Connector (Tektronix part number 131-0602-XX)
- Plain hex nut (Tektronix part number 210-0413-XX)
- 2 × 10 square-pin connector (Tektronix part number 131-3074-XX)
- Two Terminal lugs 0.391 inch inner diameter (Tektronix part number 210-0255-XX)
- 51 Ω Resistor, 1 watt (Tektronix part number 303-0510-XX)
- Bare wire, 18 gauge
- Solder and a soldering iron

Build Procedure

Refer to Figure 5–10 and use the following steps to build the BNC-to-Test Point Adapter.

1. Use diagonal cutters to cut a block of four pairs of square pins from the 21 × 10 square pin connector strip. Each cut will produce a block of 2 × 4 pins.
2. Cut two 1-inch lengths of bare wire. Solder one of these wires so that all four short pins on one side of the block of pins are shorted together. Clip off any excess wire. Use the other 1-inch piece of wire and repeat the same steps with the other side of the block of square pins. You should now have a 2 × 4 pin strip with each side (four pins) of the strip shorted together (but not to the other side of the square-pin strip).
3. Place the two terminal lugs on the BNC connector so that they stick out opposite one another. Add the hex nut and tighten so the lugs stay in position.
4. Bend both of the lugs out (away from the BNC connector) at a 90 degree angle to the body of the BNC connector.
5. Solder one of the shorted sides of the 2 × 4 square-pin strip directly to one of the terminal lugs. This will be the ground or reference side.
6. Carefully bend the signal conductor of the BNC connector down and solder it to the other shorted side of the 2 × 4 square-pin strip. This will be the signal conductor side. Clip this conductor as short as possible to avoid any high-speed signal loss.
7. Solder one end of the 51 Ω resistor to the unused terminal lug. Clip the leads of the resistor as short as possible to avoid any high-speed signal loss.
8. Bend the other end of the resistor and solder it to the signal conductor of the BNC connector. Clip off any excess lead length.

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This completes the construction of the BNC-to-Test Point Adapter.

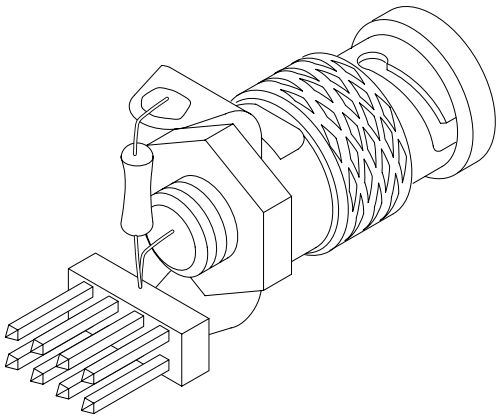


Figure 5–10: BNC-to-Test Point Adapter

Discrete I/O Loopback Fixture

Equipment Required

You will need the following material to build the Discrete I/O Loopback Fixture.

- A 37-pin D connector (Tektronix part number 131-0422-XX)
- One foot of 22 AWG insulated strapping wire
- 2 × 10 square pin strip (Tektronix part number 131-3074-XX)

Build Procedure

Perform the following steps to build the Discrete I/O Loopback Fixture.

1. Solder wire straps to the solder tails on the back of the D connector to short the following pairs of pins:

   2 and 11
   3 and 12
   4 and 13
   5 and 14
   6 and 15
   7 and 16
   8 and 17
   9 and 18

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2. Cut three pairs of square pins from the square pin strip. One pin of the pair will be soldered to the signal location of the D connector and the other to an adjacent ground location. Solder pin pairs to the locations list in Table 5–5.

Table 5–5: Solder Locations

Signal Name	Signal Location	Ground Location
Write Output	Pin 1	Pin 20
Read Output	Pin 10	Pin 28
+5 Volts	Pin 19	Pin 37

This completes the construction of the Discrete Loopback Fixture.

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Maintenance

This section explains how to keep your TLA 510 or 520 system unit, associated modules, and terminal in good working condition. It also contains procedures for removing and replacing major components of the system unit (such as power supply, media, etc).



WARNING. *Dangerous electric-shock hazards exist inside the system unit. Be sure the front-panel ON/STANDBY switch is in the STANDBY position and the power cord is disconnected before removing the cabinet. Only qualified service personnel should disassemble the system unit.*



CAUTION. *When powering off the system unit, wait 60 seconds before disconnecting the power cord. This allows the system unit to complete file-management procedures and move the hard disk head to a safe position.*

Inspection and Cleaning

Preventive maintenance consists of periodic cleaning. If dust accumulates on components, it acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown. Periodic cleaning reduces instrument breakdown and increases reliability.

You should clean the TLA 510 or 520 system unit and terminal as needed, based on the operating environment.

Static Precautions

Many components within the system unit are extremely susceptible to static-discharge damage. Follow the quidelines in this section to prevent static damage.



CAUTION. *Static can seriously damage the internal electrical components of the system unit. Service the system unit only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the instrument. Always wear a grounded wrist strap, or equivalent, while servicing the system unit.*

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Observe the following precautions to avoid damage:

- Do not handle static-sensitive components on the boards.
- Transport and store static-sensitive boards in their original containers or on conductive foam. Label any package that contains static-sensitive assemblies.
- Wear a wrist strap attached to the system unit while handling the boards to discharge the static voltage from your body.
- Do not slide a board over any surface. If you need to temporarily set a board down, place it on the card cage to protect it from damage by static voltage.
- Do not allow anything capable of generating or holding a static charge on the work surface.
- Avoid handling boards in areas that have a floor or work-surface covering capable of generating a static charge.
- When not in use, store boards in a static-free (conductive) package.

Cleaning Guidelines

Use the following guidelines when cleaning the system unit and modules:



CAUTION. *Spray-wash dirty parts with a cleaning solution (as described in Interior Cleaning, later in this section), THOROUGHLY RINSE with de-ionized water, and IMMEDIATELY DRY with low air pressure.*

When cleaning near unsealed electromechanical components, do as little washing as possible. This prevents removing the lubricant from the components and getting excess cleaning agents into the contact areas of the switches. RESIDUE WILL CAUSE CORROSION, which can degrade instrument performance.

DO NOT use a freon-based cleaner on the circuit boards. Freon will damage aluminum capacitors.

DO NOT wash the front ON/STANDBY switch. Cover the ON/STANDBY switch during washing procedures.

DO NOT use fluorocarbon-based spray cleaners or silicon spray lubricants on switches or switch contacts. These sprays may damage the circuit-board material or plastic parts, and leave a dust-collecting residue. Use Tektronix Contact Lubricant and Cleaner (part number 006-7753-XX) as a lubricant.

To prevent damage from electrical arcing, completely dry all circuit boards, switches, and board interface connectors. Do this by heating the board or switch in an oven at 65° C (150° F) for 15 minutes before applying power.

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TLA 510 and 520 System Unit

The following paragraphs describe maintenance procedures for TLA 510 and 520 system units.

Exterior Cleaning. Dust the exterior surfaces of the system unit with a dry, lint-free cloth or a soft-bristle brush. If dirt remains, use a cloth or swab dampened with warm-water. A swab is also useful for cleaning in narrow spaces around the controls. Do not use abrasive compounds on any part of the instrument.



CAUTION. *To prevent damage from getting water inside the instrument during external cleaning, use only enough water to dampen the cloth or swab.*

DO NOT use chemical cleaning agents; they may damage the plastics in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Interior Cleaning. Clean the interior every six months to keep dust from contaminating the disk drives. To access the system unit's interior, refer to the *Removal and Replacement Procedures* on page 6–7.

Use a dry, low-velocity stream of air to clean the interior of the system unit. A soft-bristle brush is useful for cleaning around components. If a liquid must be used for minor internal cleaning, use isopropyl alcohol, denatured ethyl alcohol, or de-ionized water.

If the interior of the instrument needs a thorough cleaning, follow the *Cleaning Guidelines* previously discussed.

Floppy Disk Drive. The floppy disk drive requires routine maintenance to operate at maximum efficiency. The diskette may be permanently damaged if dirt and dust accumulate on the recording surfaces. To prevent damage, the diskette should be stored in the envelope and box provided, where they will not be exposed to dust or dirt. In addition, the floppy disk drive head should be cleaned periodically.

You will need the following materials for routine maintenance:

- Vacuum cleaner
- 3.5-inch floppy disk head-cleaning kit

The routine maintenance and cleaning schedules for the floppy disk drive is as follows:

- Clean the exterior (face) of the floppy disk drive monthly with a damp cloth and a mild detergent.

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CAUTION. *Do not allow liquid cleaning adgents to enter the disk drive. Liquid agents may damage internal components when power is applied.*

- Clean the head monthly. Use the instructions that came with the head-cleaning kit.
- Clean the interior every six months with a soft-bristle brush and a vacuum cleaner.

If the disk drive is heavily used, or is used in a dirty environment, you should clean the drive more frequently.

Hard Disk Drive. The hard disk drive requires no periodic maintenance.

Terminal and Keyboard

The following describe maintenance procedures for the terminal and keyboard.

Exterior Cleaning. Dust the exterior surfaces of the terminal and keyboard with a dry, lint-free cloth or a soft-bristle brush. If dirt remains, use a cloth or swab dampened with warm-water. A swab is also useful for cleaning in narrow spaces around the controls. Do not use abrasive compounds on any part of these instruments.

CAUTION. *To prevent getting water inside the instrument during external cleaning, use only enough water to dampen the cloth or swab.*

DO NOT use chemical cleaning agents; they may damage the plastics in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Terminal Screen. Clean the face of the display screen using a soft cloth dampened with a solution of mild detergent and water.

Keyboard. Use a soft artist's brush to remove any dust or foreign matter between the keypads.

Interior Cleaning. For procedures on disassembly and interior cleaning of the X terminal, refer to the *TekXpress Family of X Terminals* service manual. (This manual is not part of the TLA 510 and 520 documentation package; to obtain a manual, contact your local Tektronix representative.)

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TLA 510 and 520 Modules

To clean the surface of a module, use a dry, low-velocity stream of air. A soft natural-bristle brush is useful for cleaning around components. To prevent static damage to parts, use only a natural-bristle brush (a synthetic brush can generate static electricity).



CAUTION. *Do not use liquid cleaning agents when cleaning the modules. Residue will cause corrosion, which can degrade instrument performance.*

Corrective Maintenance

Corrective maintenance consists of inspecting the instrument for damage and obtaining replacement parts. Periodic inspection reduces instrument breakdown. This section also discusses procedures for changing the line-voltage selection.

Inspection

Inspect the instrument for broken connections, frayed wires, poorly seated components, leaking capacitors, damaged hardware, and heat-damaged components. Heat-damaged parts usually indicate other circuit problems. If you notice any of these problems, inform your Tektronix field representative.

Obtaining Replacements

Obtain replaceable parts for your instrument from your local Tektronix Field Office or representative.

Mechanical. Most of the mechanical parts in this instrument are manufactured by Tektronix. Some parts are selected by Tektronix to satisfy particular requirements, or are manufactured to certain specifications for Tektronix. To determine the Tektronix part number of a mechanical part, refer to *Replaceable Mechanical Parts*.

Electrical. Individual electrical components are not replaceable parts, except fuses. Instead, whole assemblies are replaced. The part numbers for the assemblies can be found in *Replaceable Electrical Parts*. The power supply is replaceable as a unit only. The part number can also be found in *Replaceable Electrical Parts*.

Selecting the Line Voltage and Replacing the Line Fuse

There is no line-voltage selection for the system unit. The system unit automatically adjusts to line voltages in the range of 90 to 250 VAC. Only use a power cable that is in good condition and complies with the local certification standards.

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***NOTE**. 230 V operation requires one of the power-cord Options A1-A5.*

Line Fuse Replacement. The following procedure describes how to change the line fuse for the system unit. The system unit, with the appropriate power cord, can operate over the 115 VAC range and the 230 VAC range. The 115 VAC operation requires a 8 Amp, slow-blow fuse; the 230 VAC operation requires a 5 Amp, slow-blow fuse. The 230 VAC operation has a different fuse cap than the 115 VAC operation.

To change either fuse, perform the following steps:

1. Power off the system unit.
2. Wait 60 seconds and disconnect the power cord from the system unit. This allows time for the power-off sequence to complete.
3. Remove the line fuse and replace it with the appropriate fuse. Table 6–1 lists the fuses and the Tektronix part number.

Table 6–1: System Unit Fuse Replacement

Line Operation	Fuse	Tektronix Part Number
115 VAC	8 Amp, slow blow (3AG)	159-0046-XX
230 VAC	5 Amp, slow blow (5 × 20 mm)	159-0353-XX

X Terminal. There is no line-voltage selection for the X Terminal. The terminal automatically adjusts to line voltages in the range of 90 to 260 VAC with the frequency between 48 and 66 Hz. Only use a power cable that is in good condition and complies with the local certification standards.

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Removal and Replacement Procedures

This section describes how to remove and replace the major hardware components of the TLA 510 and 520 system units.

In the following procedures, directional terms (top, bottom, left, right, front, and back) assume that your system unit is in an upright position (with the bottom down), and that you are facing the front of the system unit. Replacement procedures are the reverse of the removal procedures, unless otherwise noted.

Figure 6–1 shows the system unit; use this figure to locate the major components.

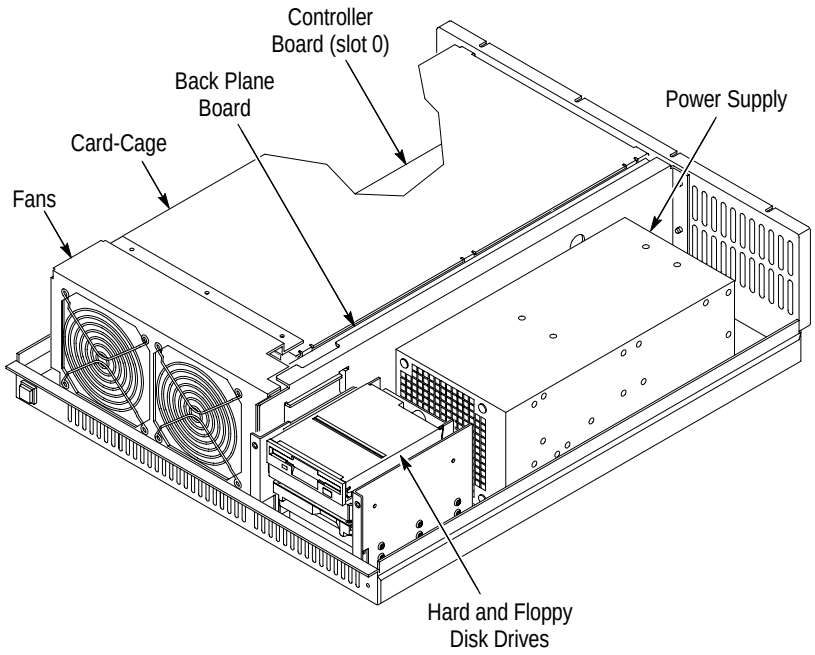


Figure 6–1: TLA 510 and 520 System Unit Internal Components

In addition to the illustrations in this section, refer to *Replaceable Mechanical Parts* for a detailed exploded view and parts list for the system unit.

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General Precautions

Observe the following precautions when performing any removal and replacement procedures.

- DO NOT attempt any disassembly procedure with the power cord connected.
- DO NOT attempt system unit replace and removal procedures with probes installed, RS-232, or LAN connections in place.

Tools Required

The following list identifies the tools necessary for disassembly of the TLA 510 or 520 system unit, and probes. This is a complete list of tools; you will need only the tools for your specific disassembly needs.

- 5/16 inch flexible shaft nutdriver
- 11 inch (shaft length) #2 POZIDRIV screwdriver (magnetic tip)
- #1 POZIDRIV screwdriver
- #1 Phillips screwdriver
- Torque screwdriver with a #1 Phillips tip
- #0 Phillips screwdriver
- Small diagonal cutters
- Two board ejector tools (Tektronix part number 105-0985-XX)

System Unit Removal and Replacement

The following procedures describe how to remove and replace the major components of the TLA 510 and 520 system unit. Unless stated otherwise, the replacement procedures are the reverse of the removal procedures.

Procedure #1: Removing Probes

Before attempting the removal and replacement procedure, you must first remove probes, RS-232, and LAN connections. To remove RS-232 and LAN connections, release any retaining mechanisms and pull the connection from its connector. To remove probes perform the following steps.

1. Power off the system unit.

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CAUTION. *After powering off the system unit with the ON/STANDBY switch, wait 30 seconds before disconnecting the power cord. This allows the system unit to lock the head in the hard disk drive to a safe position and complete file-management procedures.*

2. Remove the power cord.

3. Remove the probes and EMI brackets from the system unit by removing the screws from the probe retainer brackets. Figure 6–2 shows probe connections for the 92C96 modules. Figure 6–3 show EMI brackets for the TLA 510 or 520 and the TLA 510 with option 30 (92S16) installed.

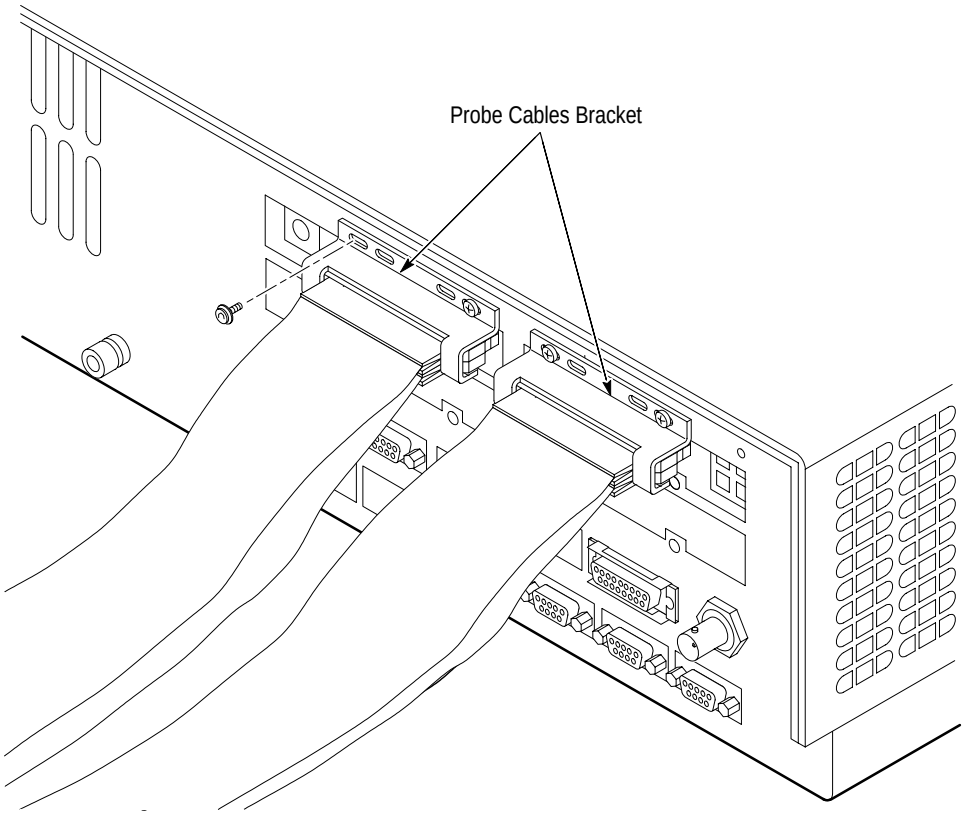


Figure 6–2: Probe Cable Connections

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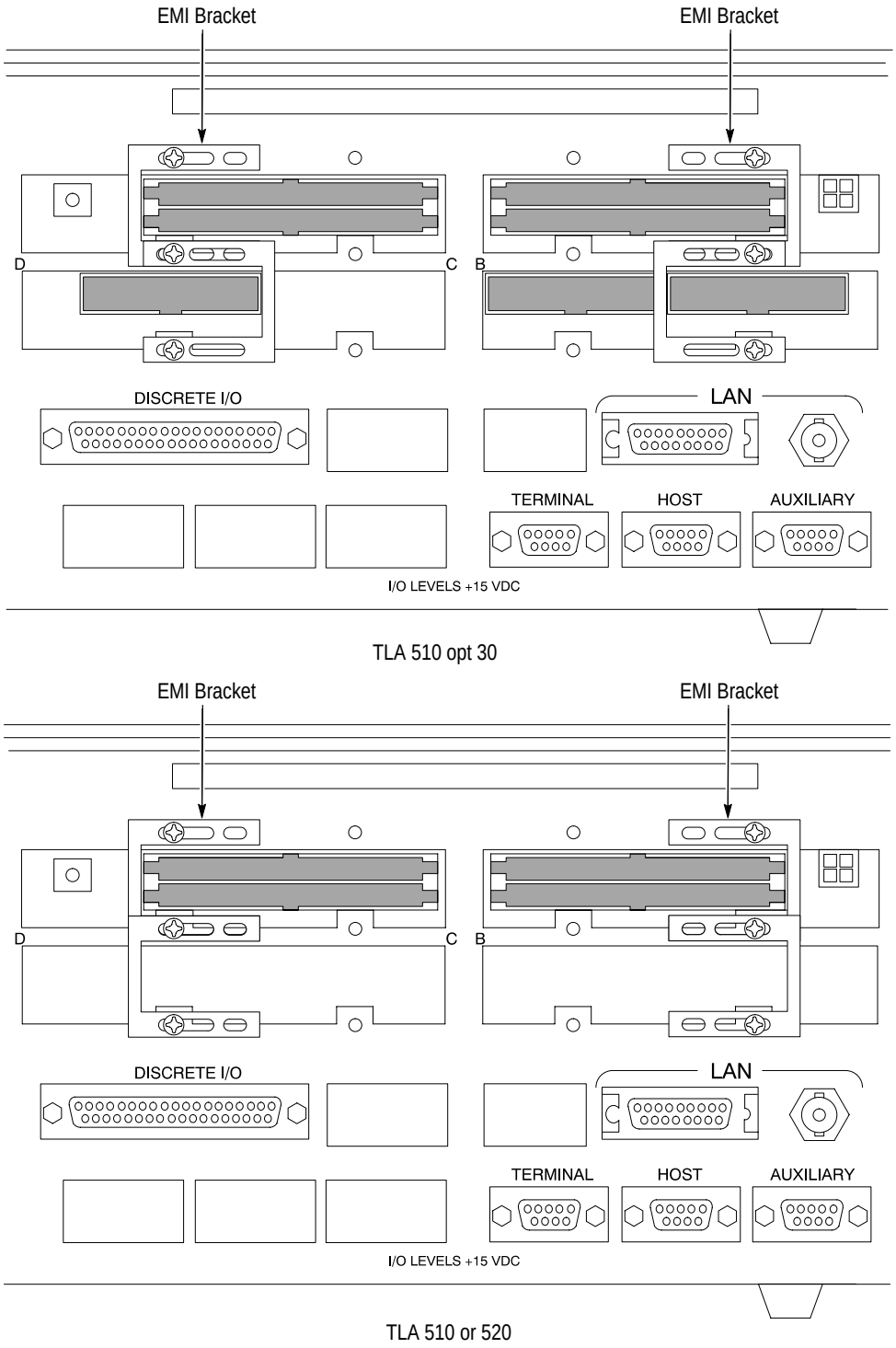


Figure 6–3: EMI Brackets

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Installation Hint. When reconnecting probes, connect the probe retainer bracket first then the EMI bracket.

Procedure #2: Removing the System Unit Top Cover

To install or remove a module, you must first remove the system unit's top cover and retainer bracket. Use the following steps to remove the top cover.

1. Perform Procedure #1.

CAUTION. *Only qualified service personnel should perform disassembly procedures. Dangerous electric-shock hazards may be exposed when you remove the system unit cover. Power off the system unit using the front-panel ON/STANDBY switch. Wait 60 seconds before disconnecting the power cord, so the power off sequence completes.*

2. Refer Figure 6–4 and remove all screws holding the top cover to the chassis using the POZIDRIV screwdriver.

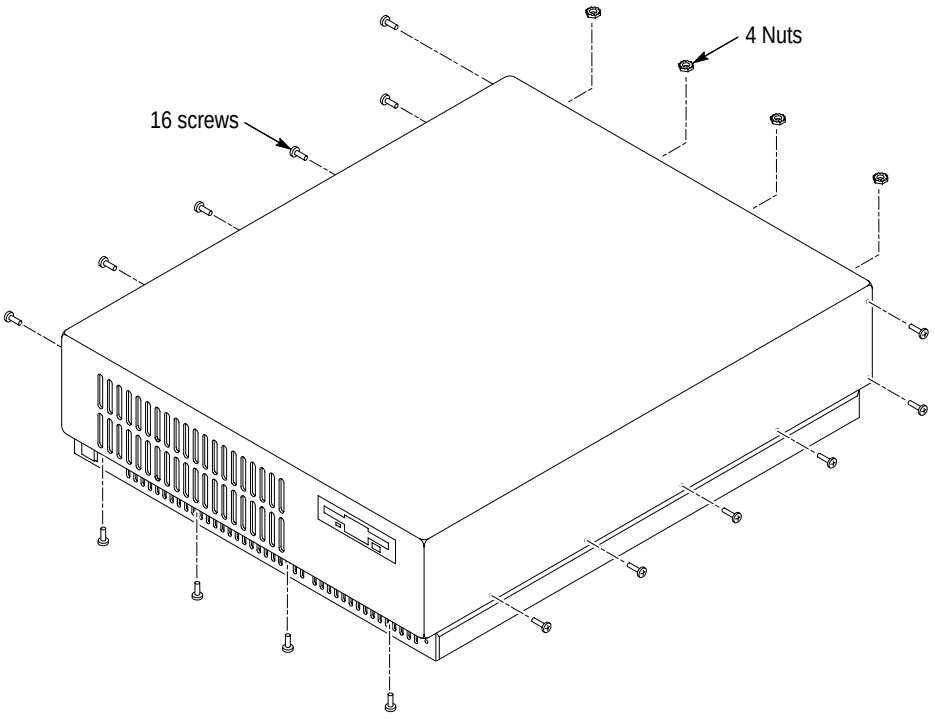


Figure 6–4: Screw Location for Top Cover

3. Refer to Figure 6–4 and use the $\frac{5}{16}$ inch nutdriver to remove the four hex nuts from the back of the top cover.

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4. Refer to Figure 6–5 and lift the cover from the back and slide it forward.

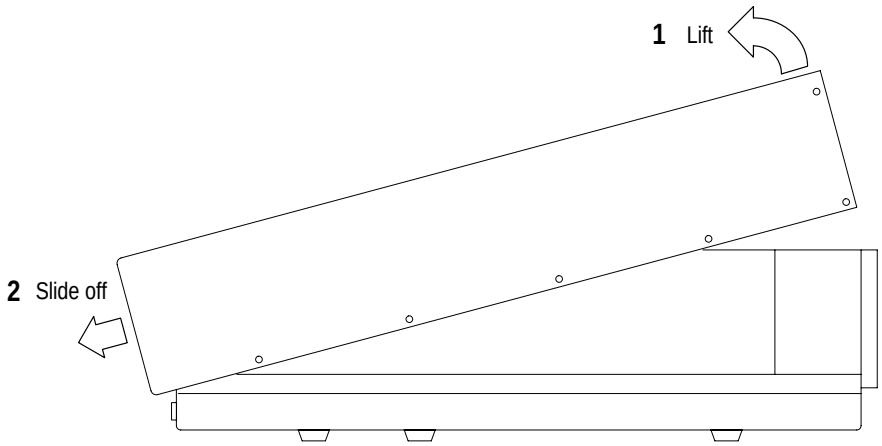


Figure 6–5: Removing the Cover

Installation Hint. When replacing the top cover, the screws must be torqued to 8-inch pounds.

Procedure #3: Removing Modules from the Card Cage

1. Perform procedure #1 and #2.



CAUTION. *Many components within the system unit are susceptible to static-discharge damage. Follow the standard handling precautions for static-sensitive devices in the* Maintenance *section when servicing this instrument.*

2. Refer to Figure 6–6 and remove the two screws that hold the card retainer bracket to the card cage.

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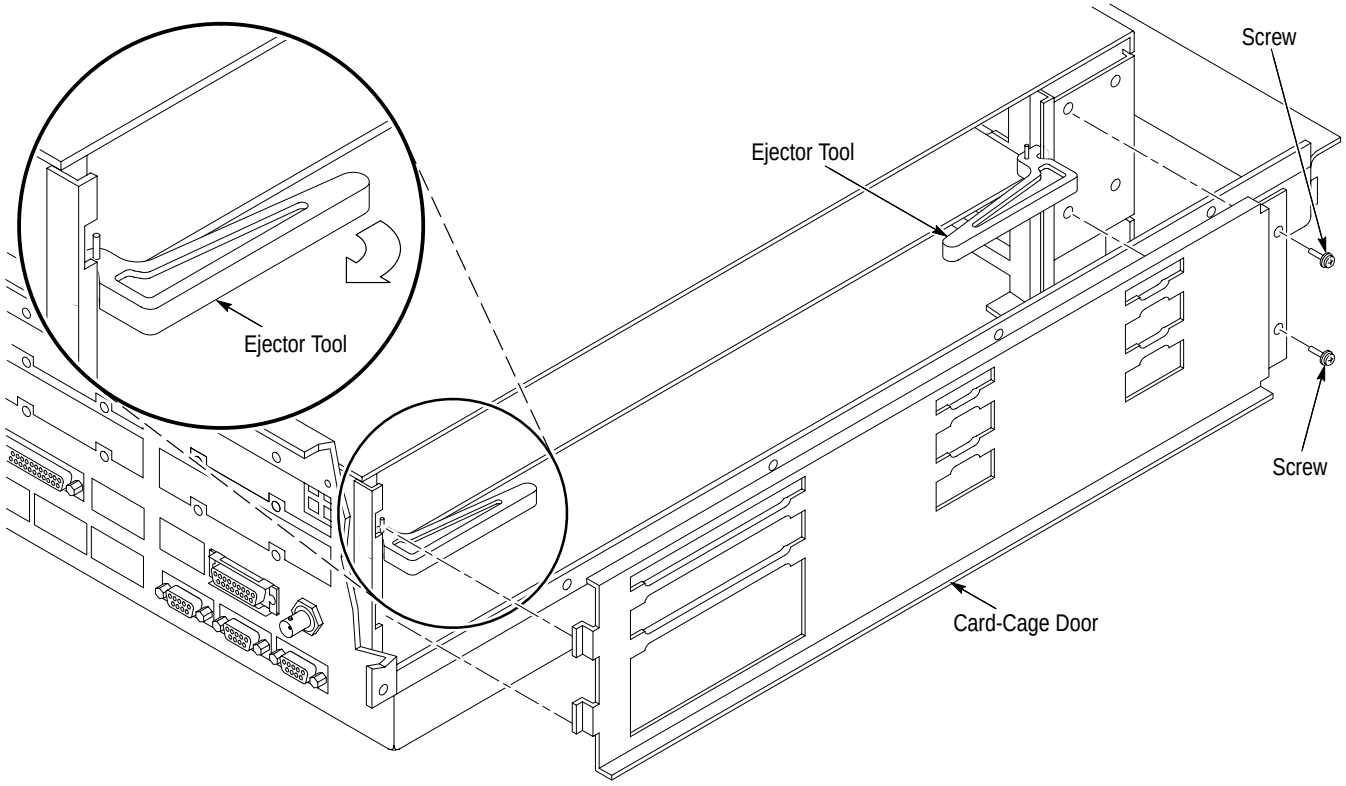


Figure 6–6: Card Retainer Bracket

3. Remove the bracket and set it aside.
4. Disconnect the probes, LAN cables, and RS-232 connections from the back of the system unit.
5. Insert the two board-ejector tools into the board you are removing, as shown in Figure 6–6.
6. Pry the board from the backplane board and remove it from the system unit.

CAUTION. *Pry with even force on both sides of the board to prevent bending the backplane-alignment pins.*

Installation Hints. When you install a module, align the connection between the backplane and the module before applying pressure; this prevents damage.

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Procedure #4: Removing the 92LANSE Module

1. Perform procedures #1, #2 and #3 to remove all modules from the system unit.
2. Refer to Figure 6–7 and unscrew the five screws holding the 92LANSE module to the Controller board.

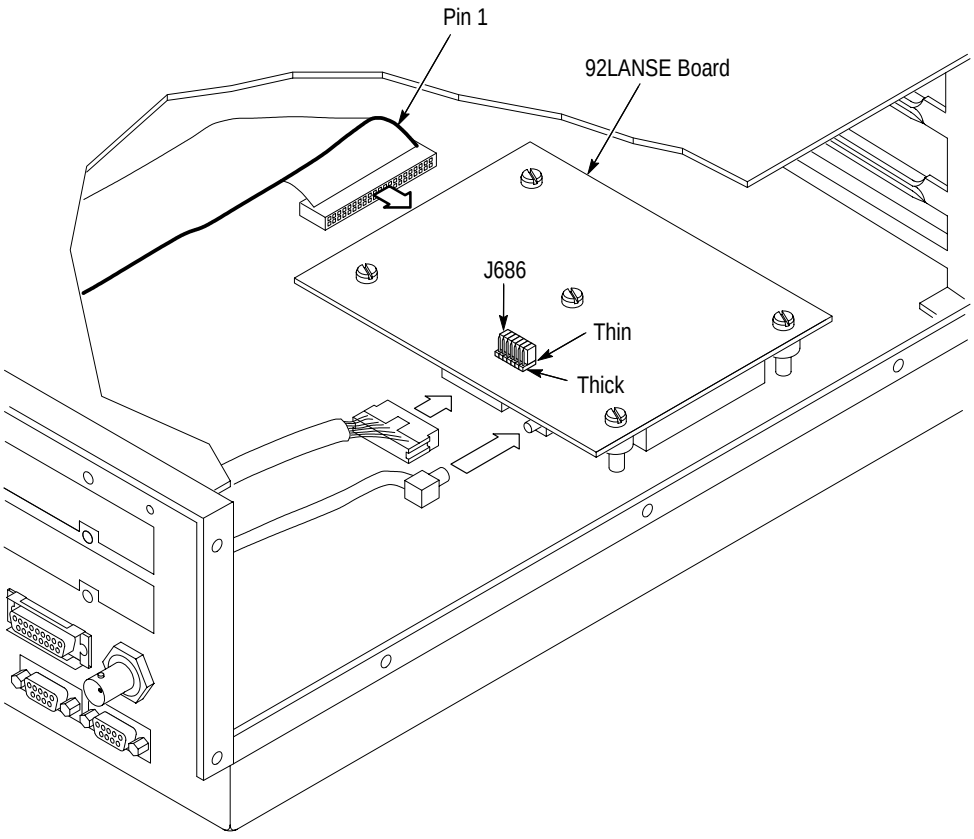


Figure 6–7: 92LANSE Screw and Cable Locations

3. Lift the 92LANSE up from the Controller board and remove the cables connected to the 92LANSE as shown in Figure 6–7.

Procedure #5: Removing the Floppy Disk Drive From the Media Frame

This procedure describes how to remove the floppy disk drive from your media frame. You do not need to remove the media frame from the chassis to remove the floppy disk drive.

1. Perform procedures # 1 and #2.
2. Refer to the top of Figure 6–8 and remove the five screws that hold the floppy frame to the media frame.

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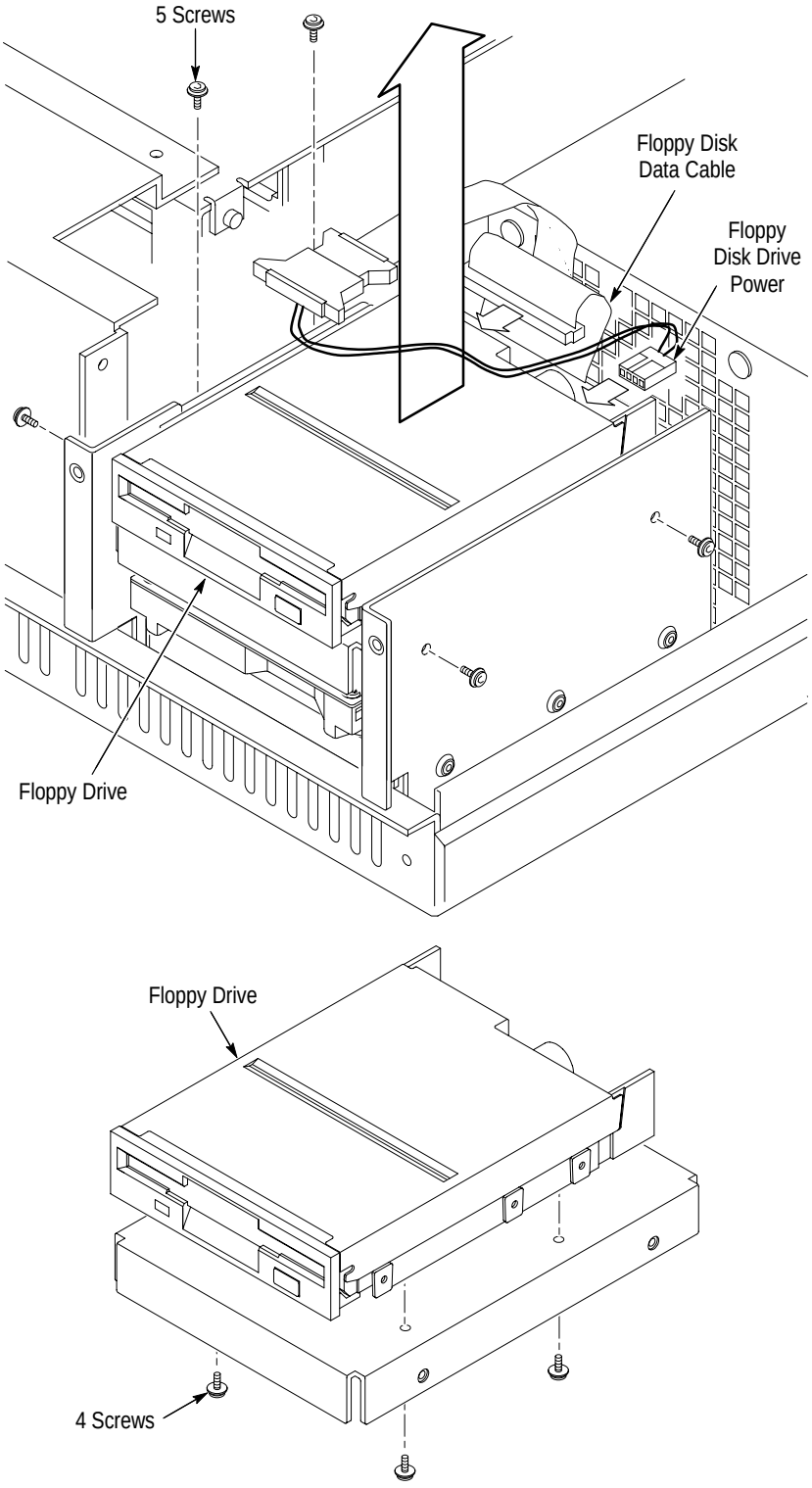


Figure 6–8: Floppy Disk Drive Removal

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3. Refer to the top of Figure 6–8 and remove the power cable and data cable from the back of the floppy disk drive.
4. Lift the floppy disk drive frame from the media frame.
5. Remove the four bottom screws that hold the drive to the frame and remove the drive as shown in the bottom of Figure 6–8.

Procedure #6: Removing the Media Frame

To replace the hard disk drive, you must first remove the media frame from the chassis.

1. Perform procedures #1 and #2.
2. Refer to Figure 6–9 and remove the six screws that hold the media frame to the chassis. Partially lift the media frame from the chassis.

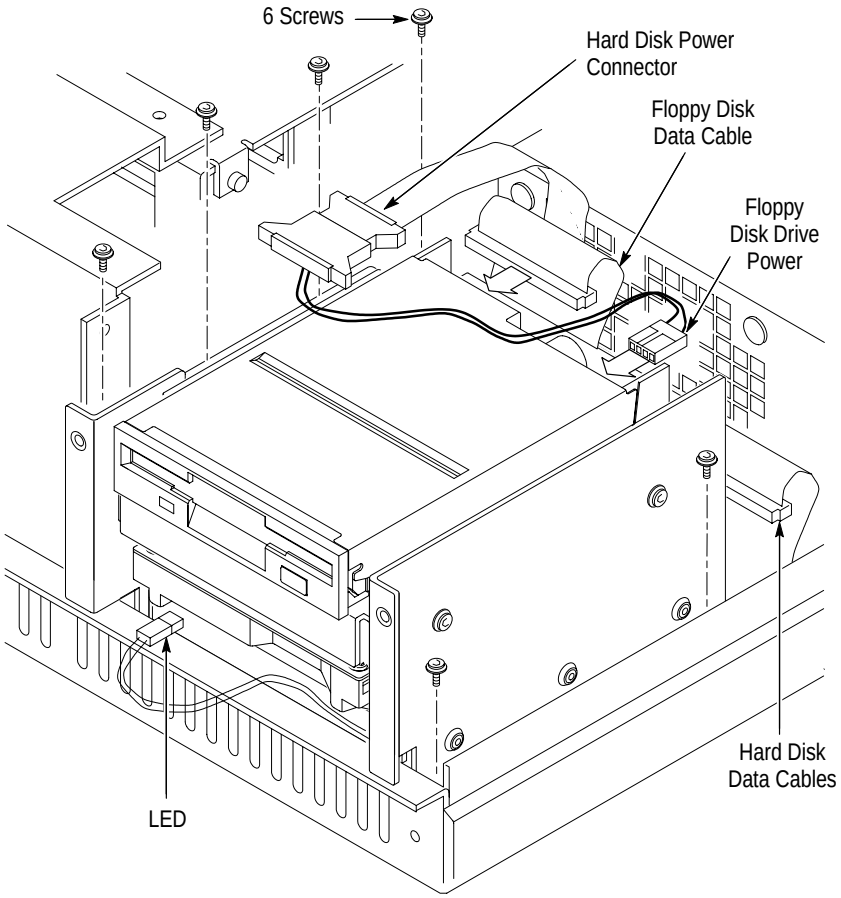


Figure 6–9: Media Frame Screw Locations

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3. Disconnect the Ribbon and power cables from the rear of the disk drives as shown in Figure 6–9 and Figure 6–10.
4. Remove the connection to the hard disk drive activity light.

Installation Hint. Figure 6–10 shows where each power and data cable connection is located. Refer to this figure when reinstalling the media frame into the chassis.

When reconnecting the hard disk drive activity light, the black wire on the LED connector needs to be positioned toward the outside edge of the drive.

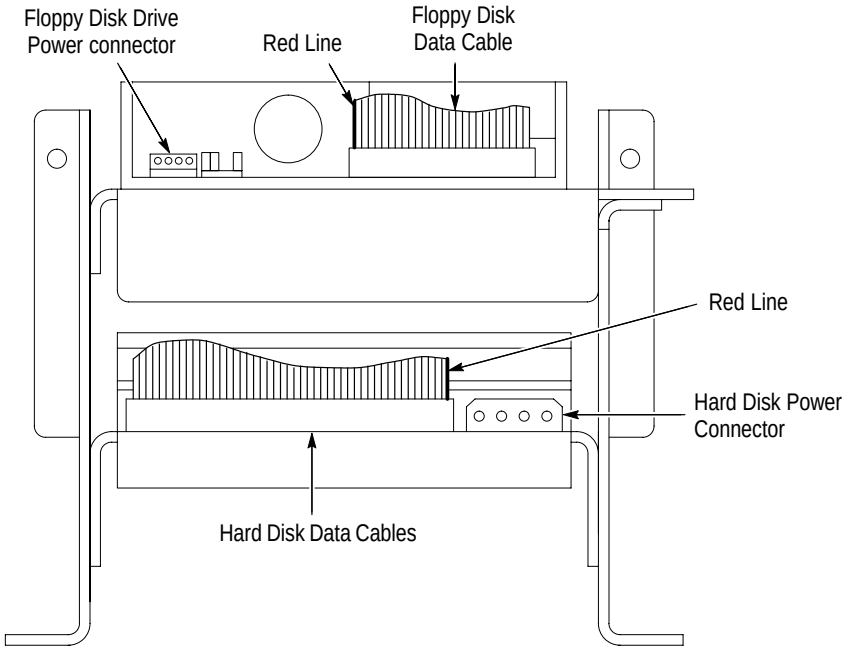


Figure 6–10: Hard and Floppy Disk Drives Connections

Installation Hint. The screws that hold the media frame to the chassis, go through slotted holes instead of round ones. This allows you to adjust the media frame so that its front face is flush with the front of the top cover. Only tighten the screws part way and then place the cover on the system unit to see if the media frame is flush. Once you are sure it is flush, tighten the screws firmly.

Procedure #7: Removing the Hard Disk Drive

1. Perform procedures #1, #2 and #6
2. Refer to Figure 6–11 and remove the screws that hold the hard disk drive to the media frame.
3. Slide the drive from the media frame.

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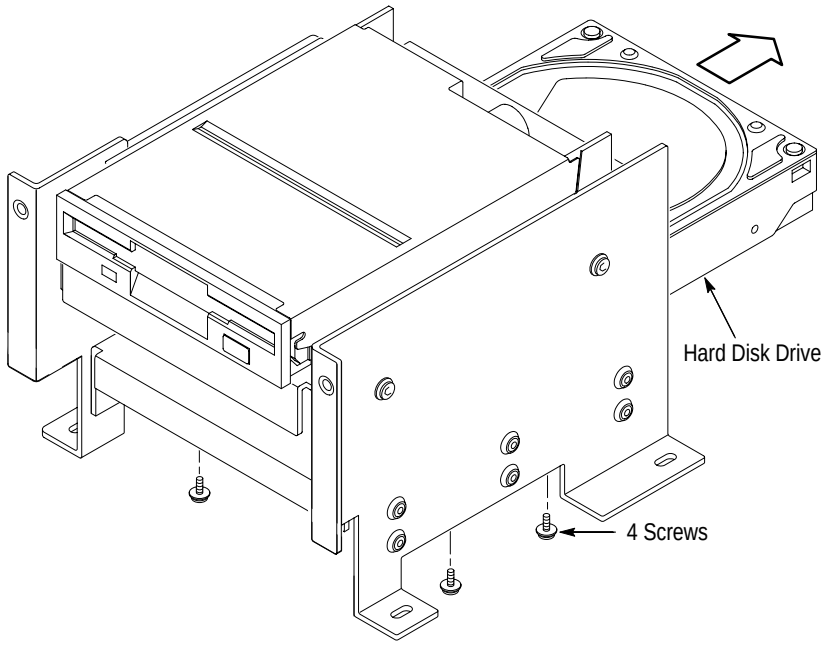


Figure 6–11: Hard Disk Drive Screw Locations

Installation Hint. Refer to Figure 6–10 to reconnect cables.

Procedure #8: Removing the Power Supply

1. Perform procedures #1 and #2.



WARNING. *Dangerous electric-shock hazards exist inside the system unit. Be sure the front-panel ON/STANDBY switch is in the STANDBY position and the power cord is disconnected before removing the cabinet. Only qualified service personnel should disassemble the system unit.*

2. Refer to Figure 6–12 and remove the line voltage connections, black, white (neutral), and one green/yellow (GND) wires from the top left side of the back of the power supply. An easy way to reach the screws that attach the wires to the supply is through the ventilation opening in the rear of the chassis.
3. Remove the power supply fan connection from the backplane board (J120) as shown in Figure 6–13.
4. Turn the chassis on its side with power supply on the bottom.
5. Refer to Figure 6–13 and remove the four screws that hold power supply to chassis.

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6. Place the chassis in the normal position and slide the power supply forward enough to lift the supply out of the chassis.

7. Remove the remaining wires from the supply. Pay attention to the wire colors and locations. Refer to Figure 6–12 for later reinstallation.

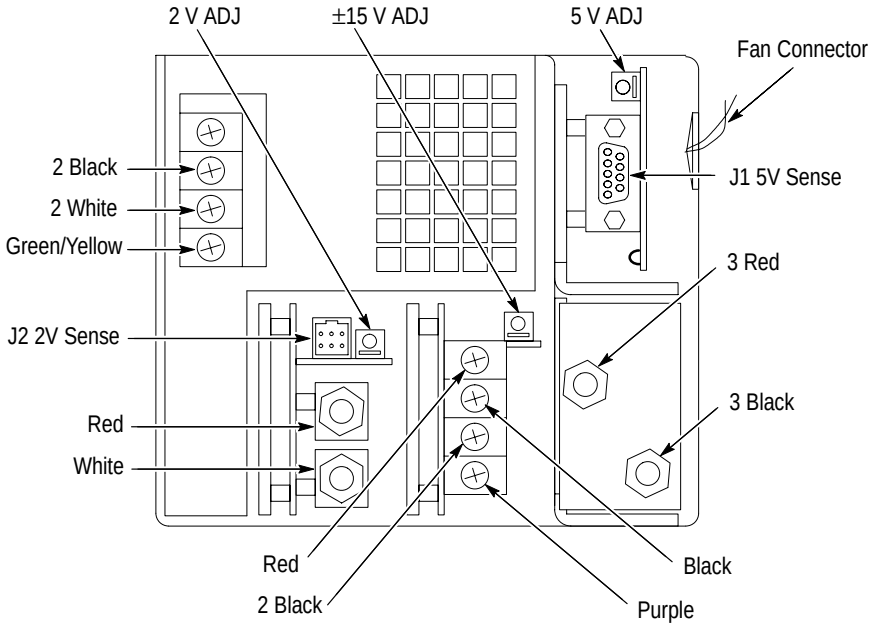


Figure 6–12: Back Panel of Power Supply

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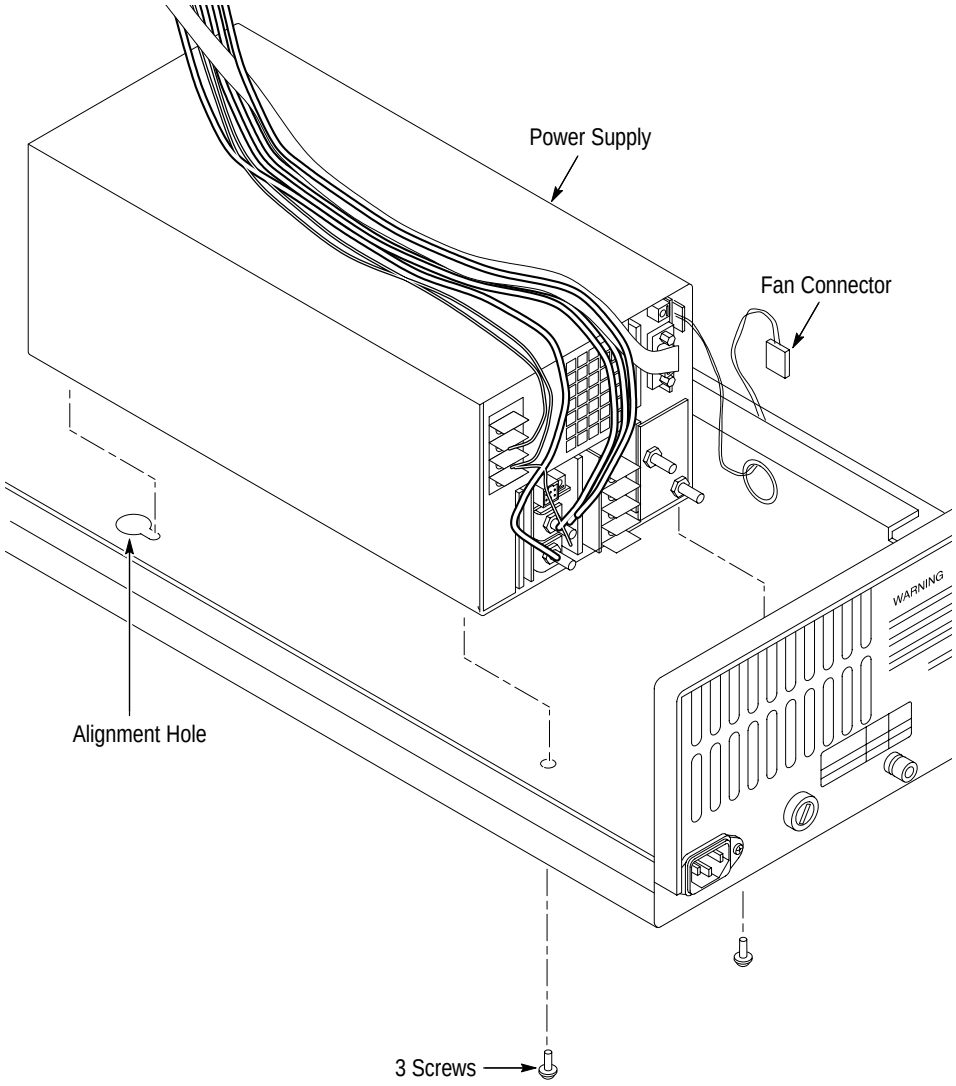


Figure 6–13: Power Supply Screw Locations

Installation Hints. The bottom screws must be torqued to 8-inch pounds when reinstalling the power supply.

Partially install a screw into the power supply module hole that corresponds to the alignment hole (see Figure 6–13). Place the power supply module on the base plate and use the first screw as an alignment aid to orient the power supply so you can install the remaining three screws.

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Procedure #9: Removing the Fan Frame

1. Perform procedures #1 and #2.
2. Refer to Figure 6–14 and remove all 12 screws that hold the fan frame to the chassis.
3. Lift the fan frame up and out of the chassis and remove the power connections from the backplane board.

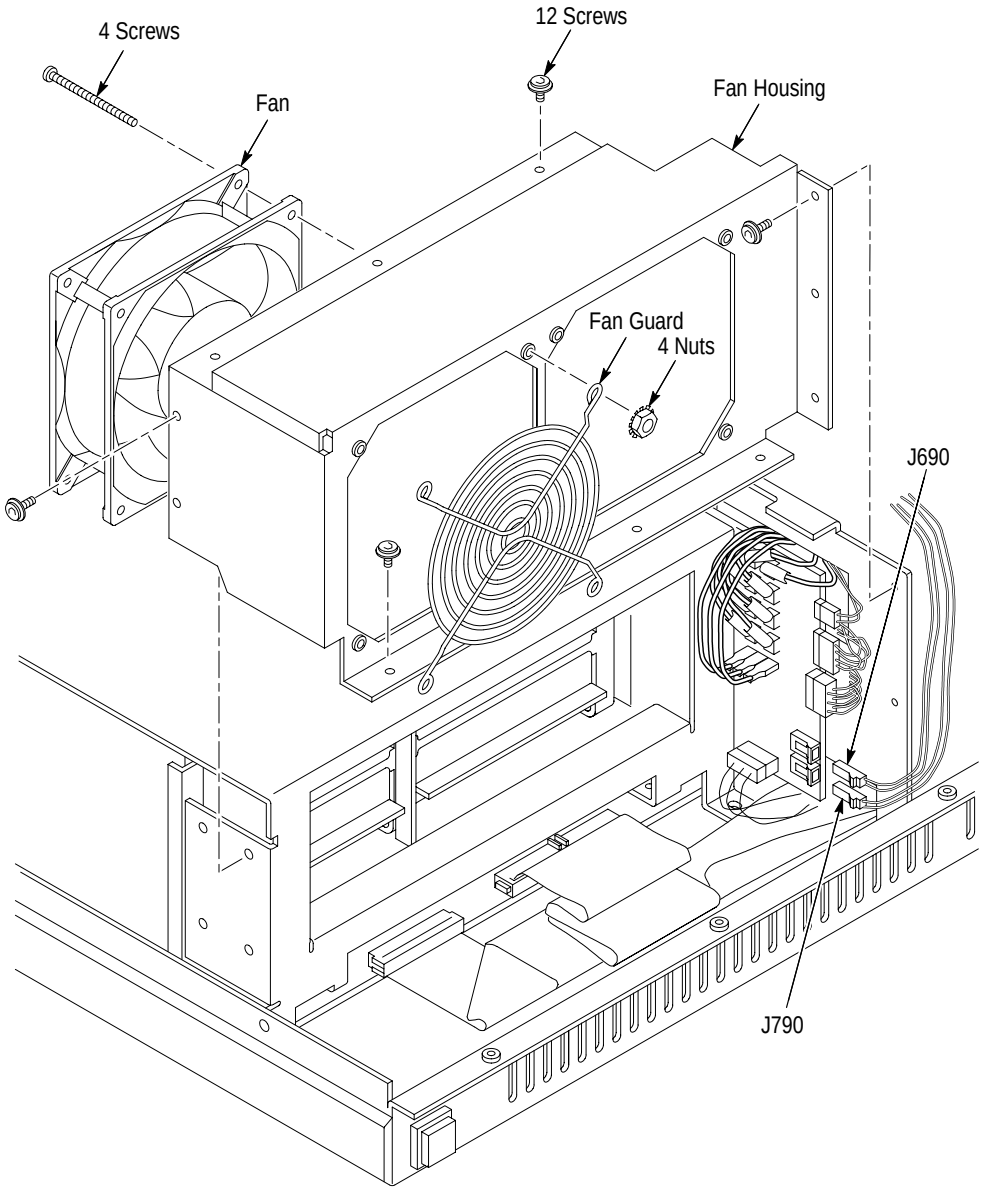


Figure 6–14: Fan Frame Removal

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Installation Hint. When replacing the fan make sure the media ribbon cables are out from under the lip of the fan frame and not in front of the fans. This ensures that the cables are not pinched and that airflow to the card cage is not obstructed.

Procedure #10: Removing the Fans

1. Perform procedures #1, #2, and #9.
2. Refer to Figure 6–14 and remove the fan grills by removing the nuts that attach the grill to the frame.
3. Grasp the back of the fan with one hand and the frame with the other hand and pull the fan from the frame.

Procedure #11: Removing the Card Cage

You must remove the card cage from the system unit before removing the Controller board or the backplane.

1. Perform procedures #1, #2, #3, #4, and #9.

WARNING. *Dangerous electric-shock hazards exist inside the system unit. Be sure the front-panel ON/STANDBY switch is in the STANDBY position and the power cord is disconnected before removing the cabinet. Only qualified service personnel should disassemble the system unit.*

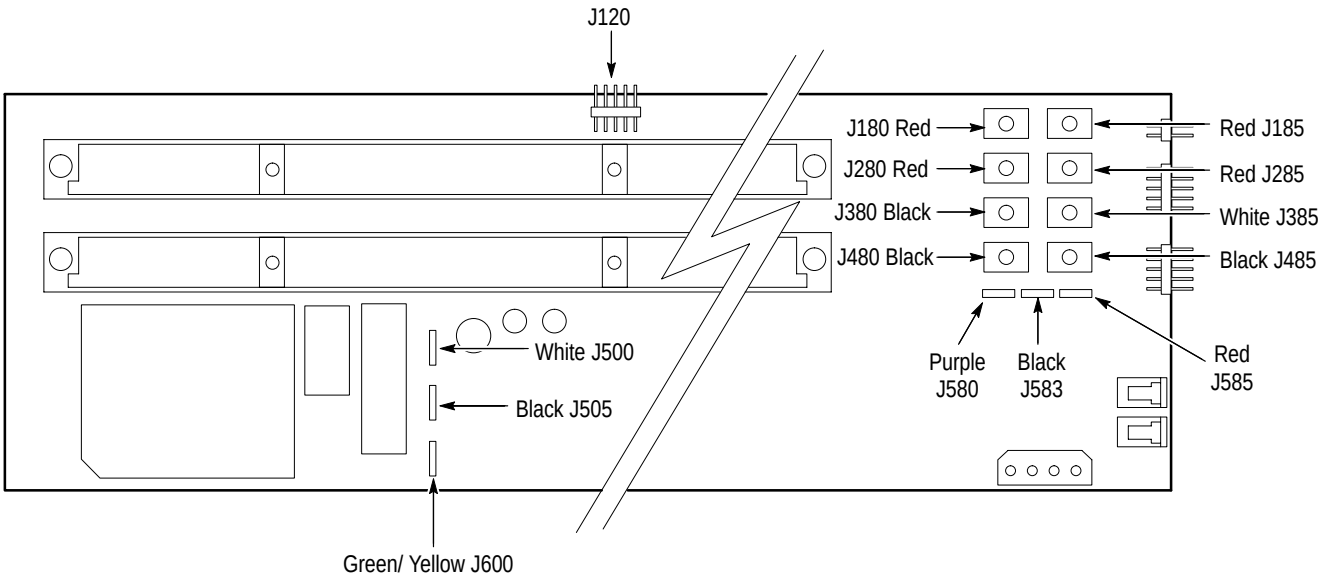


Figure 6–15: Power Supply Cables Attached to the Backplane Board

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2. Refer to Figure 6–15 and disconnect the power supply cables from the front and the rear of the backplane board. Note how the power supply wires on the front of the backplane board are positioned. You will need to place the wires in the same position when replacing the card cage. Otherwise the top cover will not fit properly.

3. Refer to Figure 6–16 and disconnect the RS-232 ribbon cables from the controller board.

***NOTE**. Slip the retaining straps off the RS-232 connectors, do not cut. The retaining straps will easily slip over the connections when you reinstall the controller board.*

---

4. Refer to Figure 6–16 and disconnect the floppy and hard drive ribbon cables from the front of the Controller board.

5. Place the rear power supply cables (white J500, black J505, and green/yellow J600) away from the card cage, without going all the way through the hole in the side plate that separates the power supply from the backplane board. This will make it easier for you to remove and later replace the card cage onto the chassis.

6. Refer to Figure 6–16 and remove the four screws (two short, two long) that hold the card cage to the back panel.

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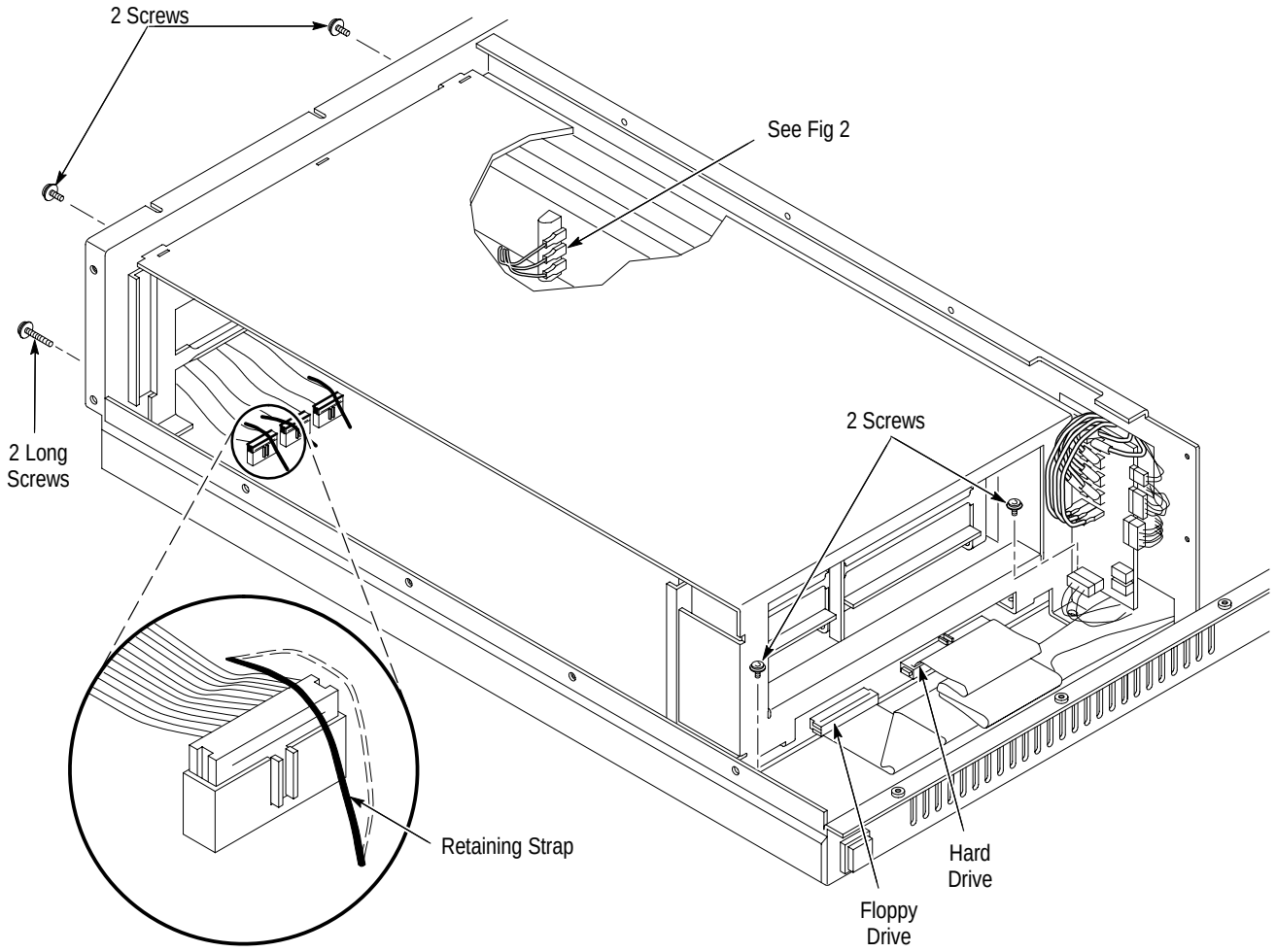


Figure 6–16: RS-232 Cable Locations

7. Remove the screws that hold the card cage to the baseplate, as shown in Figure 6–17.
8. Pull the card cage up from the nylon posts in the baseplate, then forward.

CAUTION. *Carefully slide cables (RS-232, LAN, etc.) out of the rear of the card cage to prevent damaging components on the Controller board.*

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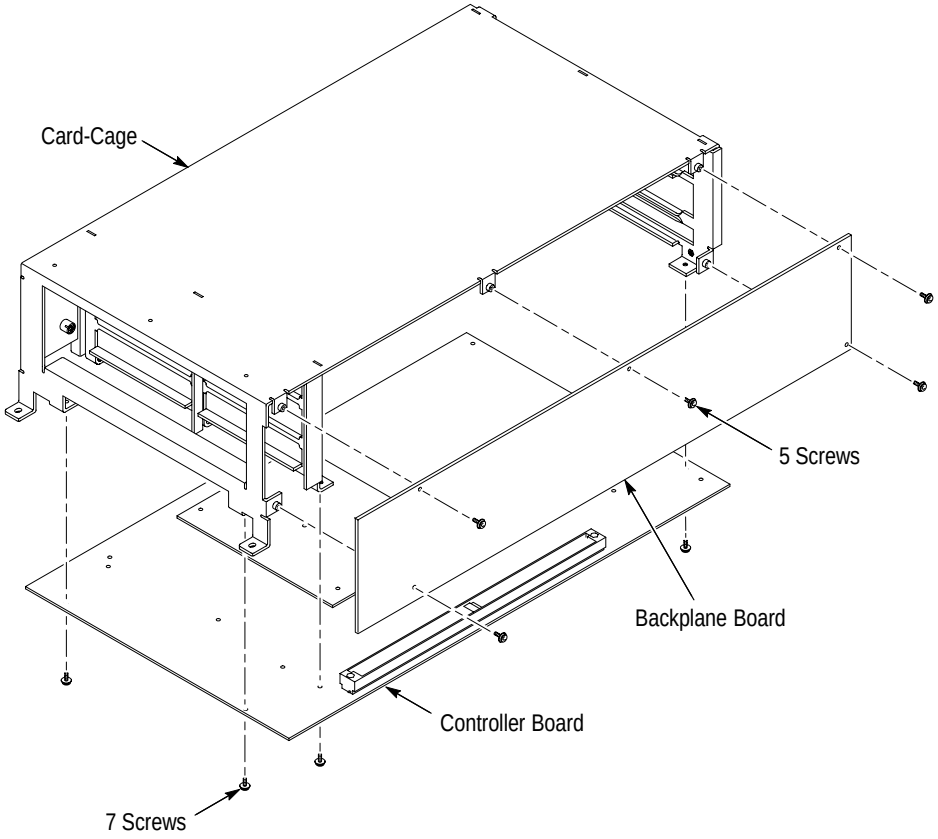


Figure 6–17: Card Cage Screw Locations

Installation Hints. When reconnecting the power-supply wires to the backplane board, torque the screws on the connectors to 10 inch-pounds. Align each nylon support with its mounting hole before pressing the Controller board onto the baseplate.

Procedure #12: Removing the Controller Board

1. Perform procedures #1, #2, and #11.
2. Place the card cage on its top, so the bottom of the Controller board is up.
3. Remove the seven screws holding the Controller board to the card-cage as shown in Figure 6–17.
4. Carefully separate the connection between the Controller board ad the Backplane board. Remove the Controller board from the card cage.

Installation Hints. When reinstalling the Controller board, check that its connections to the backplane are fully mated. Remember to reconnect any cables that were disconnected during disassembly, such as the RS-232 cables.

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Procedure #13: Removing the Backplane

1. Perform procedure #1, #2, and #11.
2. Place the left side of the card-cage assembly on the work surface so that the back of the backplane board is facing up.
3. Remove the five screws holding the Backplane board to the card cage as shown in Figure 6–17.
4. Separate the connection between the Backplane board and the Controller board and then lift the Backplane board off the card-cage assembly.

Installation Hints. When reconnecting the power-supply wires to the Backplane board, refer to Figure 6–15. The screws must be torqued to 8 inch-pounds.

P6463A Probe Procedure

The circuit-board assemblies in the P6463A probe are replaceable. The following steps describe how to disassemble and reassemble each probe, so you can replace the assemblies.

1. With a flat-blade screw driver, unlatch the latches on the side of the P6463A probe.
2. Remove the upper half of the probe housing and set it aside.
3. To remove the ID/Logic board (the smaller board), unscrew the four mounting screws with a POZIDRIV screwdriver. Unplug the ID/Logic board from the Buffer/Driver board by gently pulling the two boards apart.



CAUTION. *The ID/Logic board is connected to the pod ID switch through a two-wire cable. Take care not to stress the cable's connections during disassembly procedures. Unnecessary strain on the cable may cause damage to the cable.*

4. If necessary, free the pod ID switch from the lower probe housing by slightly loosening the mounting nut and lifting the switch out.
5. To remove the Buffer/Driver board, gently pull up on the red and black power leads to free them from the lower probe housing. Grasp the board and lift it from the lower probe housing. To disconnect the cable assembly from the Buffer/Driver board, grasp the cable assembly plug and gently pull it straight out (note pin 1 orientation for reassembly).
6. Reassembly of the probe is the reverse of this procedure.

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Troubleshooting

This section contains troubleshooting information for isolating failures in the TLA 510 or 520 system unit to the module or board level. This troubleshooting information includes diagnostic descriptions and troubleshooting tips for areas not tested by the diagnostics. Terminal diagnostics are also included; refer to the *TekXpress Family of X Terminals* service manual for additional information on the X Terminal. (This manual is not part of the TLA 510 and 520 documentation package; to obtain it, contact your local Tektronix representative.)

Power-On Diagnostics

The system unit and terminal contain diagnostics that normally run when powered up. Since the terminal provides the user interface, it should be powered on and checked first (with the system unit power off). Refer to *X Terminal Diagnostics* for a description of these diagnostic tests. After the terminal diagnostics complete with the word "connected" in the terminal window, turn on the system unit to execute its power-on diagnostics. Refer to the section *System Unit Diagnostics* on page 6–29 for a description of these diagnostic tests.

X Terminal Diagnostics

Three levels of diagnostics check the X Terminal: the Kernel Self-Test, Local Self-Test and Extended Self-Test. Before powering on the terminal, connect the keyboard and mouse to the terminal, and connect the terminal to the system unit; connection information is in Chapter 2: *Operating Information*.

Kernel Self-Test. The Kernel Self-Test runs automatically whenever the terminal is turned on. The Kernel Self-Test is a series of programs, residing in the Boot ROM, that perform minimum hardware checks to ensure that the terminal will boot.

During the self-test programs, status and fault information is indicated by the LED indicators on the keyboard. If an error occurs, a code is displayed in the keyboard's LEDs. Table 6–2 lists the codes.

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Table 6–2: Kernel Self-test Error Codes

FRU Label	Value	LED Status
FRU_NULL	0	All LEDs off
FRU_MAIN	1	Scroll
FRU–ROM	2	Capslock
FRU–SIMM1	3	scroll-capslock
FRU_SIMM2	4	Numlock
FRU_KEYBRD	5	scroll-numlock
FRU_FLASH	6	capslock-numlock
FRU_OPTPORT	7	scroll-numlock-capslock

Local Self-Test. Local Self Tests are performed by users to verify field-kit installations. Local Self-Test is stored in boot memory and is executed from the boot monitor using the *selftest* command. For further information on the Local Self-Tests, refer to the *TekXpress Family of X Terminals* service manual.

Extended Self-Test. The Extended Self-Test is menu driven and contains tests that reside in software. The software is downloaded from the TLA 510 or 520 system unit. To start Extended Self-Test, do the following:

1. Restart the X terminal either by cycling the power or by typing Ctrl-Alt-Del.
2. Enter the Boot Monitor by pressing any key before the boot load indicator reaches 100%.
3. At the BOOT> prompt, type

   ```
   BOOT> bp /bootpath . . . . . /selftest.350

   BOOT> b
   ```

   where *bootpath* . . . . . is the bootpath (bp) listed in the Boot Monitor banner. The file name *selftest.350* replaces *os.350* in the path.

Entering Extended Self-Test displays the Extended Self-Test Menu shown in Figure 6–18.

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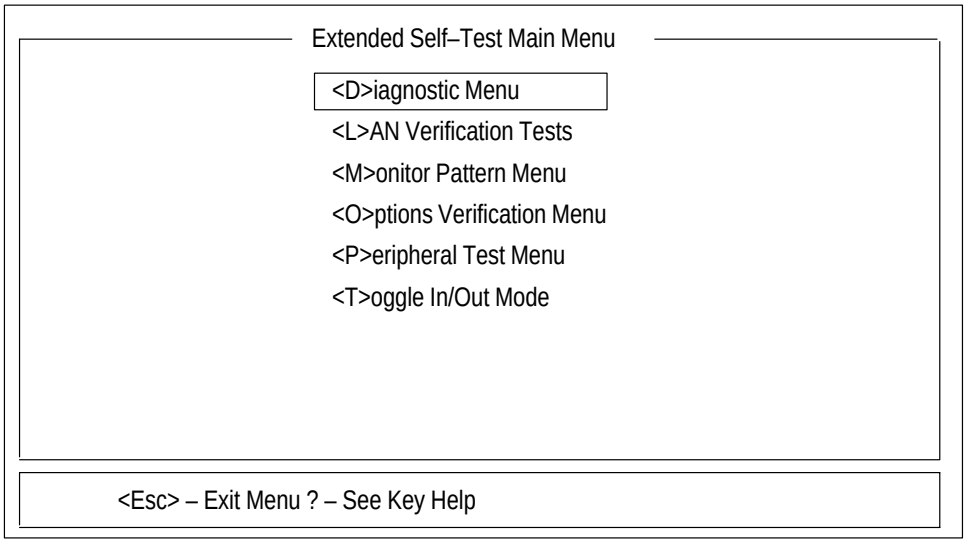


Figure 6–18: Extended Self-Test Main Menu

For further information on the Extended Self-Test Main Menu and the associated checks, refer to the *TekXpress Family of X Terminals* service manual.

System Unit Diagnostics

The TLA 510 and 520 normally perform diagnostics at power on to check the major internal components of the system unit, operating software, and installed modules. There are two levels of diagnostics: 0 and 1.

***NOTE**. Refer to the* Diagnostics, File System Checks, and the Boot Option Overlay *on page 2–16 for information on changing the criteria for running power on diagnostics.*

Level 0 first calculates the power consumption and reports the results. It then checks the system unit and takes approximately 6 seconds. When the level 0 diagnostics are successfully completed, the system unit displays the message **LEVEL 0 diagnostics – complete**; then level 1 diagnostics begin.

Level 1 checks all modules installed in the system units; each check takes up to 6 seconds per module. First, level 1 diagnostics check for incorrect module configurations. When this part of level 1 completes, the system unit displays the message **LEVEL 1 configuration test(s) complete**. Level 1 then runs diagnostics for each module. If Level 1 detects errors, it reports them in the Diagnostics menu with a FAIL message and a corresponding error code. The system unit displays the Menu Selection Overlay after it completes the power-on diagnostics. You can access the Diagnostics menu from the Menu Selection overlay.

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If random characters or no characters appear when you power on the system, you may need to change the terminal's baud rate. (For baud rate selections, refer to the section *DIP Switches on the Controller Board* on page 6–44.)

Level 0 Diagnostics. Level 0 diagnostics detect two types of errors: soft errors and hard errors. Usually, you can correct a soft error by reconfiguring the cards in the system unit. If the error is severe enough (for example, board power requirements exceed power-supply limits), the system unit shuts off. A hard error can usually be corrected by replacing a system unit board, such as the Controller board.

Level 0 diagnostics display the total power used by the modules in the system units, then checks the system units for functionality.

If level 0 diagnostics do not detect an error, level 1 diagnostics begin. If level 0 detects an error, a message may appear on the terminal. In addition, LEDs on the rear of the Controller board report an error pattern. When power-on, the LEDs sequence to track the progress of level 0 diagnostics. These LEDs are described under *Controller Board LEDs* on page 6–31.

Table 6–3 lists error messages that you may encounter when you power on your TLA 510 or 520 system unit. This table also describes the messages and suggests corrective actions.

Table 6–3: Error Messages for TLA 510 and 520 System Units

Message	Description/Corrective Action
POWER FAIL!	Check the power cord connection and the system unit's fuse on the back panel. Dropped cycles in the power source also cause this message. If all of these actions fail to correct the problem, replace the power supply.
FAN FAIL!	The system unit card cage fans may have a problem, so the system unit may overheat. Remove the top cover and check that cables are not blocking airflow from either fan. Visually check that the card-cage and power-supply fans are turning. Check that the power supply fan connection to the backplane board has not come loose. Check that power is connected to the system unit fans. Partially remove the connector from the card-cage fan, so you can measure the voltage across it with a digital voltmeter. It should measure between –11.5 VDC and –14.25 VDC. If it doesn't check to see if the –15 V supply is between –15 VDC and –17 VDC. It not replace the power supply.
Switch OFF	The ON/STANDBY switch, located on the front panel, is in the STANDBY position. If the switch is ON, the power supply, ON/STANDBY switch, backplane board, or the Controller board may be faulty.
WARNING! RS-232 PORT FAILURE	Level 0 diagnostics check each RS-232 port up to the hardware drivers, but not beyond them. If the Terminal port fails, the system unit stops the diagnostic tests. If the Host or Auxiliary ports fail, this message appears and the Controller board LEDs display a troubleshooting code for about three seconds. Refer to Table 6–4 for a description of the LED error codes.
hard panic – unknown type of floppy interrupt	Check the floppy drive hardware.

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Table 6–3: Error Messages for TLA 510 and 520 System Units (Cont.)

Message	Description/Corrective Action
hard panic – floppy interrupt with no buffer queued	Check the floppy drive hardware.
soft panic – Inode overflow:	The hard or floppy disk does not have any more room for storage.
soft panic – Inode address greater than 2 exp 24	The file is too big.
clock lost count	This is not a serious error. If it happens repeatedly, check the Controller board or modules.
failure to reboot from ROM	Problems with ROM or the hard disk could cause this problem.
file descriptor ...	Usually indicates an interprocess-communication problem between the system manager and the menu you were using. Cycle power or rebuild operating-system software to recover from the problem.
Supervisor trap	RAM or a kernel from the disk is bad.
Supervisor bus error exception	RAM or hardware bus (such as the hard disk) problem.
Supervisor address error exception	RAM or hardware bus (such as the hard disk) problem.
Drive is not bad block formatted	Reformat drive, make the file system, and reinstall software. May not be able to access the drive.
Unable to read (write) bit map	Reformat drive, make the file system, and reinstall software. May not be able to access the drive.
Unable to replace bad block	The hard disk does not function. There are not enough replacements for the bad blocks.

Controller Board LEDs. If level 0 diagnostics detect an error, the system unit may pause indefinitely without displaying a message on the terminal. In this case, the set of 10 bar-graph LEDs (0–9) on the rear of the Controller board indicates the fault; you can view the LEDs through the rear of the card cage. These LEDs track the progress of level 0 diagnostics and will halt when an error occurs. The last state of these LEDs before shutdown indicates the fault.

NOTE. *Several other surface-mounted device (SMD) LEDs are visible on the controller board. These are processor-status indicators used during instrument manufacture and module repair.*

LEDs 0–7 display a “scanning” pattern after successfully completing the power-on diagnostics. This scanning pattern indicates that the CPU is operating normally. The scanning pattern may be briefly interrupted based on the operating mode. Table 6–4 lists the LED error code.

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NOTE. *LEDs 0–7 are in hexadecimal code, with the least significant bit at the far left as you face the rear of the system unit.*

The level 0 tests are not necessarily run sequentially. Individual codes within a set of 16s (hex) are run sequentially, however, sets are not run sequentially. For example, 33 always comes before 34; but the 70s may come before the 30s.

If the level 0 diagnostics do not detect an error, LEDs 0–9 indicate the status of the three power-supply voltages as follows:

- If any of LEDs 0–7 are lit, the +5 V supply is present
- If LED 8 is lit, the + and –15 V supplies are present
- If LED 9 is lit, the +3 V current-sink supply is present

NOTE. *You can also verify the presence of the power-supply voltages by checking the test pads on the top-front of the Backplane board with a digital voltmeter.*

Table 6–4: LED Diagnostic Errors

Error Codes †	Test Functions	Possible Failures Other than Controller Board
FF	Reset asserted	power supply
00	Level 0 diagnostics complete	
01	BOOTROM checksumed	none
1X	NVRAM	none
20	VoltAmps summation	a module in a slot
30	Enable PFail exception	power supply
31	Enable xBint2 exception	a module in a slot
33	System clock	none
34	Enable Hard/Floppy disk, I/O exception	Expansion I/O
35	Enable xBINT1 exception	a module in a slot
38 – 3B	Communication ports' interrupts	none
3F	Enable xBint0 exception	a module in a slot
40 – 47	Communication ports' registers	none
48 – 4B	Communication ports' transmit	none
4C – 4F	Communication ports' receive	none
5X	MMU registers	none
6X ‡	DRAM	none

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Table 6–4: LED Diagnostic Errors (Cont.)

Error Codes †	Test Functions	Possible Failures Other than Controller Board
63	Fan fail	power supply/fan
66	Exception vector move	none
70 – 71	Floppy disk registers	floppy disk
73 – 74	8K buffer RAM/alignment	none
7A – 7D	Floppy Disk Controller IC/interrupt	none
9X	MMU operation	none
A1	Calendar access	none
A2	No clock movement	none
A3	Clock movement is wrong	none
A4	10 µs clock period	none
B0	MMU registers disable	none
B1	MMU registers address	none
CX	SCSI testing	SCSI drive
F3	Unexpected Bus Error	system unit memory module
F7	BINTx exception	a module in a slot
F8	Spurious exception	a module in a slot
F9	Undefined exception	none

† **X = "Don't Care"**

‡ **Except error codes 63 and 66**

Level 1 Diagnostics. After the system unit completes level 0 diagnostics, level 1 diagnostics check for incorrect module configurations. This test checks that the installed boards are in legal slots. If this test fails, the terminal displays the message **FATAL: Configuration error in slot (#)**, where # indicates the first slot number with the error. Some modules display configuration errors. The test does not display additional configuration errors until you correct the first error. For information on installing modules in the system unit, refer to *Removal and Replacement Instructions* on page 6–7.

After each FATAL message, the terminal displays the message **System going down** and the system unit powers off. When you correct the problem and the TLA 510 or 520 is powered on again, the configuration test reruns. When this part of level 1 completes successfully, the terminal displays the message **LEVEL 1 Configuration test(s) complete**.

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After level 1 completes the configuration tests, it checks the Event and Correlation buses and installed modules. If the buses or modules fail, the Diagnostics menu displays a FAIL message and error code when the level 1 diagnostics finish. Access the Diagnostics menu through the Menu Selection overlay.

92C96 Configuration Errors. The 92C96 Modules display additional information when errors occur. Table 6–7 lists the possible errors. Refer to the *92C96 and 92C96 Module User Manual* for more information on these errors.

Diagnostic Menu. The Diagnostic menu (Figure 6–19) lists the major system components and reports the status of each component at power on.

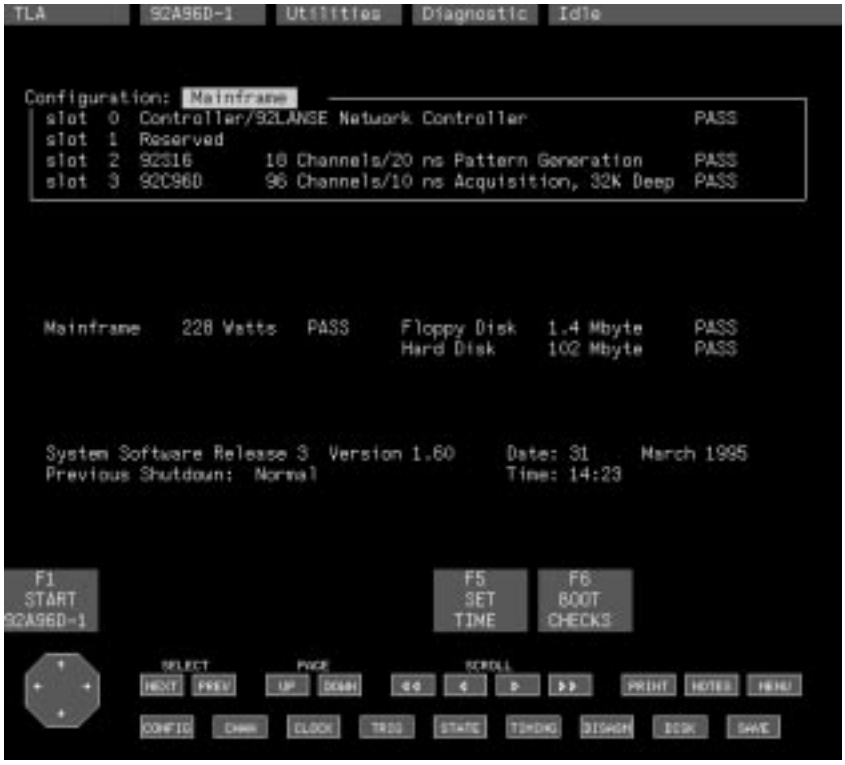


Figure 6–19: Diagnostics Menu

The Diagnostics menu has the following features:

- A report of the results of diagnostic testing (done at power-on) with a PASS or FAIL message; FAIL messages also provide a four-digit error code for use by a qualified service technician. The codes are explained next under *Diagnostic Menu Error Codes.*

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- A summary of the modules installed in each slot. Slots 0 contains the Controller board and the 92LANSE Network Controller; slot 1 is reserved: slots 2 and 3 hold the acquisition module(s) and optional pattern generator.
- The version number of the system software currently loaded from the mainframe hard disk.
- A summary of the conditions surrounding the last power off. These messages are described in Table 6–5.
- The current date and the time (in military format); you can change the values in the Date/Time overlay accessed by function key F5: SET DATE/TIME.

Table 6–5: Previous Shutdown Field Messages

Message	Explanation
Normal	The last system shutdown resulted from pushing the front-panel ON/STANDBY switch to the OFF position. This is the correct way to power off. All open files and interprocess communication channels close properly.
Hard OS Failure	The last system shutdown resulted from a fatal error detected by the operating system from a hardware or software failure. This power off may corrupt the hard disk file system. For information on checking and rebuilding the file system refer to *Loading System Software* on page 6–67.
Software	The last system shutdown resulted from depleted system resources, such as hard disk space or memory. This power off may corrupt the hard disk file system. For information on checking and rebuilding the file system refer to *Loading System Software* on page 6–67.
Power Failure	The last system shutdown resulted from loss of AC power (e.g., power cord disconnected from the power source). Files remain open, resulting in a loss of disk space. For information on checking and rebuilding the file system refer to *Loading System Software* on page 6–67.
Unexpected	The last system shutdown resulted from unknown causes. The operating system assumes this mode at power-on. This power off may corrupt the disk file system. For information on checking and rebuilding the file system refer to *Loading System Software* on page 6–67.
Fan Failure	The last system shutdown resulted from either a system unit fan failure, a power-supply fan failure, or an over-temperature condition. This power off does not corrupt the disk file system.

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Diagnostic Menu Error Codes. Diagnostic provides a PASS, FAIL or No S/W message for every module in the system unit. If a FAIL message appears, a four-digit error code also appears as an index to additional information describing the failure. The first digit in the error code indicates the type of error:

1	Diagnostics were not performed on that module.
2	Module operation is still possible but specifications are no longer guaranteed.
3–7	Unused codes, so they should not be displayed.
9	System operation is possible, but operation of the module is not possible.
C	The problem affects other parts of the system; operation of the module is not possible and the TLA 510 or 520 shuts down. Prior to shutdown, the system unit displays the message **FATAL: Hardware Error** along with the failed module's slot number and error code.

If **No S/W** appears in place of a **PASS** or **FAIL** message, the installed module does not have any software installed on the hard disk. Refer to the HW/SW menu to display a list of the installed software. If you want to install the software for your module, refer to the procedures listed later in this section.

Tables 6–6 to 6–8 list error codes for system unit and module failures. Because the 92LANSE module connects directly to the Controller board, any diagnostics errors for the 92LANSE module are reported as errors for the controller board (see Table 6–6).

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Table 6–6: Controller Board Diagnostic Error Codes

Error Codes	Test Name	Possible Failures Other than system unit Controller Board
X00X	EVENT/CORRELATION LINES	Any card that uses the Event/Correlation lines
X000	Start Lines	
X001	Event Lines	
X002	Correlation Lines	
X10X	TIMEBASE CHECKS	
X100	Time base Chain	
X101	Time base 4	
X102	Time base 1	
X103	Time base 2	
X104	Time base 3	
X20X	FAST MEMORY CHECK	
X200	Access Memory	
X201	Fast memory write/read (2–16 M)	
X202	Parity path	
X30X	92LANSE MODULE CHECKS	92LANSE Module
X300	Hardware Present	92LANSE Module
X301	Control-Status Register	92LANSE Module
X302	Discrete I/O Register	92LANSE Module
X303	ID ROM	92LANSE Module
X304	RAM	92LANSE Module
X305	Lance Chip Registers	92LANSE Module
X306	Lance Chip Initialization	92LANSE Module
X307	Internal Loopback	92LANSE Module

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Table 6–7: 92C96 Diagnostic Error Codes

Error Codes	Test Name	Possible Failures Other than Module
X00X	ACQUISITION MEMORY	
X000	Mem Full Bit	
X001	Ripple MAR	
X002	MAR TC Carry	
X003	Bank Select	
X004	AcqRAM Banks 0 & 2	
X005	AcqRAM Banks 1 & 3	
X10X	TIMESTAMP	
X100	Gray to Binary	
X101	TStamp Rollover	
X102	TSReset/FastClk	
X20X	CSM	
X200	CSM RAM	
X201	START + Clock Paths	
X202	Async Clock Select	
X30X	RTC	
X300	RTC Array Access	
X301	State RAM	
X302	Clock Counters	
X303	Microcode	
X304	Cal. mode Acquire	
X305	CRE Event	
X306	Events Out	Any TLA 510 or 520 board
X307	Events In	Any TLA 510 or 520 board
X40X	WORD RECOGNIZERS	
X400	RTC WR Events	
X401	Address Recognizer Inputs	
X402	Data Recognizer Inputs	
X403	Control Recognizer Inputs	
X404	Address Recognizer Events	
X405	Data Recognizer Events	
X406	Control Recognizer Events	

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Table 6–8: 92S16 Diagnostic Error Codes

Error Codes	Test Name	Possible Failures Other than 92S16
X000	Clk Path – clock	9200 System time base
X100	Program Counter Load	
X101	Program Counter Increment	
X102	Stack Load	
X103	Stack Increment	
X200	S16 Memory – Bit Write	
X201	S16 Memory – Memory Address	
X202	S16 Memory – Memory Test	
X300	Reg. A – Load Mode	
X301	Reg. A – Incr. Mode	
X302	Reg. A – Decr. Mode	
X400	Reg. B – Load Mode	
X401	Reg. B – Incr. Mode	
X402	Reg. B – Decr. Mode	
X500	Instruction – Advance / Jump	
X501	Instruction – Irq	
X502	Instruction – Repeat	
X503	Instruction – If Key	
X504	Instruction – If Ext	
X600	Output Lines – Output	
X700	Low speed Events – Event Output/ Input	Main Controller board
X701	Low speed Events – Start/Stop Control	Main Controller board
X800	Probe ID and interface	Failed, unidentified, or incorrect probe

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TLA 510 or 520 System Unit Troubleshooting

Isolation of a problem is limited to the module or board level; diagnostics only perform checks on individual boards and not the entire system. Items such as power supplies, probe connections, probe functionality, and card-to-card interactions cannot be tested. If the system unit passes the diagnostics, but you still suspect a hardware problem, there are other checks you can do to find the problem. This section contains information to troubleshoot system unit hardware and system software.

System Unit Troubleshooting Overview

Use the following steps as an overview of troubleshooting the TLA 510 or 520 system unit.

1. Ensure that all system unit modules are correctly installed and that all interconnects and cables are properly connected and fully seated.
2. Power on the system unit and check that the card cage and power supply fans are operating.
3. Check that the power-supply voltages are within specification as stated on page 6–42. Also check that the media power supply voltages are at the media power connectors.
4. If the power supply does not power on, check the following:
   - The AC-line power-cord connection
   - AC-line fuse
   - Power-supply secondary wiring and control cable connections
   - Front-panel ON/STANDBY switch connection and operation
   - Power supply fan connection to the backplane board. (Refer to the *Removal and Replacement* Procedures on page 6–7 to locate and check this connection.)



WARNING. *High voltage is present on the Backplane board. To avoid electric shock do not touch conductive parts.*

   - F600 located at the rear of the backplane board. This fuse is for the keep alive circuitry. If it is blown the system unit will not power on.
   - Thermal switch J301 and J302 located at the rear of the backplane board.

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5. Verify that the X terminal is properly connected to the system unit Terminal port with the proper cable. Check that the terminal communication parameters (such as baud rate) match the settings of the system unit. Also check for the proper setting of the Controller board DIP switches for the Terminal port near the back of the system unit.

6. Power on the TLA 510 or 520 with DIP switch 1 in the up position (normal boot) and check the back-panel LED indicators to ensure that no level 0 diagnostic errors have occurred.

7. Power on the TLA 510 or 520 from the BOOT?> prompt (DIP switch 1 in the down position) and run the System Software File System Check and Verify hard-disk maintenance utilities. These floppy-based utilities check if the drive is properly formatted and if the system software is installed and uncorrupted.

Power Supply Check

To determine if the power-supply voltages are within their tolerance, partially remove the fan frame and measure the voltages on the power-supply test pads on the top-front corner of the backplane. The first six test pads are labeled +15 V, +12 V, +5 V, +3 V, GND, and -15 V. Refer to *Removing The Fan Frame* on page 6–21.



WARNING. *High voltage is present on the Backplane board. To avoid electric shock do not touch conductive parts.*

To see if f the 5 V supply is in tolerance, look at the rear panel of the power supply and see if the 5 V tolerance LED is on. Refer to Figure 6–20 for the location of the LED. If the 5 V supply is out of tolerance, the system unit's CPU is held in reset mode and operation of the logic analyzer will not be possible.

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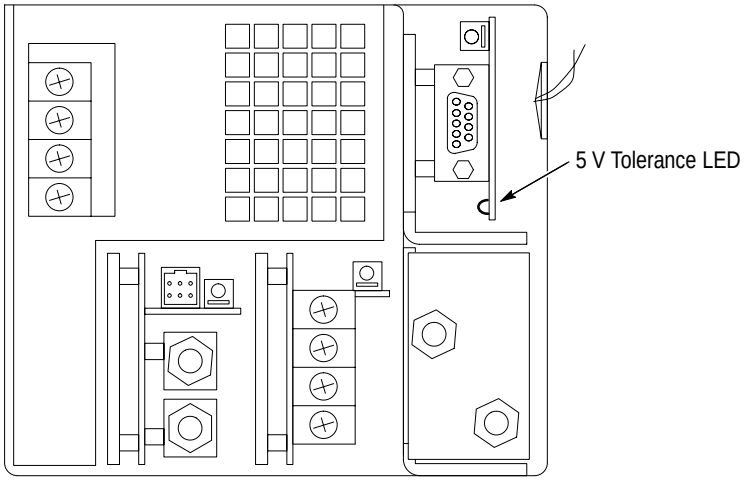


Figure 6–20: Five Volt Tolerance Light

Using a digital multimeter set at 20 VDC range, probe the test pads for the voltages shown in Table 6–9.

Table 6–9: Power-Supply Voltages

Supply	Tolerance
+15 V	15 V min., 17 V max.
+12 V	11.4 V min., 12.6 V max.
+ 5 V	5.05 V min., 5.25 V max.
+ 3 V	–2.0 V min., –2.2 V max. (+5 V ref.)
–15 V	–15 V min., –17 V max.

Backplane Board Fuses. There are four fuses on the backplane board that should be checked if you are experiencing problems with the system unit. Table 6–10 lists the fuses, their location, and possible problems caused if these fuses are blown.

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Table 6–10: Backplane Board Fuses

Fuse	Location	Possible Problems
F600	Rear of the backplane board	F600 is used for the keep alive circuitry. If blown the system unit will not power on.
F785	Lower front of the backplane board	F785 is used for the +5 V media supply. If blown neither the floppy or hard disk drive will operate.
F585	Lower front of the backplane board	F585 is used for the +15 V supply. If blown the system will not boot from the hard disk drive and the application cards will exhibit problems.
F580	Lower front of the backplane board	F580 is used for the –15 V supply. If blown the cooling fans will not operate. Also the controller and application cards will exhibit problems.

Power Control Signals

Check the power control signals to troubleshoot the system unit. These signals travel between the backplane and the power supply. Six test pads for the signals are located below the power-supply test pads on the top-front corner of the backplane. You can check the test pads for active TTL levels with a digital multimeter or an oscilloscope. Table 6–11 shows the name associated with the labels on the test pads and describes the functions of the signals.

Table 6–11: Test-Pad Signal Descriptions

Label	Name	Description
CL~	CURRENT LIMIT	This active-low signal is on the backplane and shuts down the power supply. An instrument module could draw too much current and activate this signal.
TOF	TURNOFF	This active-high signal travels from the backplane board to the Controller board and indicates to the Controller board that the front-panel switch is in the OFF position or that a a card-cage over temperature condition has been detected. When the Controller board receives the TOF signal, it accesses the hard disk to shutdown the operating system orderly. The Controller board then sends SD~ to the power supply.
SS	SUPPLY STABLE	This active-high signal travels from the power supply to the Controller board through the backplane. The signal indicates that the +5 V supply is stable. When this signal is low the CPU is held reset. After this signal goes high the CPU begins executing its program.

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Table 6–11: Test-Pad Signal Descriptions (Cont.)

Label	Name	Description
PF~	POWER FAIL	This active-low signal travels from the power supply to the Controller board through the backplane. If the signal maintains a TTL high, primary power is available. A high-to-low transition indicates that primary power is disabled. When the Controller board receives this signal, it will use NVRAM, instead of the hard disk, to perform an emergency shutdown of the operating system.
SD~	SHUTDOWN	This active-low signal travels from the Controller through the backplane to the power supply to power off the system unit.
ON~	ON/STANDBY	This active-low signal traveling from the backplane to the Power Supply and the Controller board indicates the position of the front-panel switch. When ON, the front-panel switch is pushed in. When in STANDBY mode, the front-panel switch is out.

Refer to the discussion of the Controller board on page 3–3 in *Theory of Operation* for more information on the sequence of events for TURNOFF, POWER FAIL, and SHUTDOWN.

DIP Switches on the Controller Board

The Controller board has eight DIP switches; you access the switches through an opening on the back panel of the system unit. Check these switches if power-on is unsuccessful.

Use DIP switches 1 and 2 when loading the system software from floppy disks. You can also use DIP switches 1 and 2 to force the system unit to loop its level 0 diagnostics; this may be helpful to isolate intermittent power-on errors.

The Communications menu contains communication parameters for the Terminal, Host, and Auxiliary ports (see *TLA 510 & 520 User Manual*). You can override these selected parameters at power-on by using DIP switches 3–8. Refer to Table 6–12 for a summary of the DIP-switch settings. The “restore parameters” setting restores the port’s Communications menu operating parameters at power on, instead of restoring the default operating parameters. You can change the port parameters at any time by making changes in the Communications menu when the system unit is operating.

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Table 6–12: Baud Rate Dip Switches

Switch Use	Setting	Result
Boot Control	1 / 2	
	U / U	normal boot
	D / U	BOOT?> prompt
	U / D	not used
	D / D	loop on level 0 diagnostics
Terminal Port	3 / 4	
	U / U	38.4K baud default
	U / D	2400 baud
	D / U	1200 baud
	D / D	restore parameters
Host Port	5 / 6	
	U / U	9600 baud default
	U / D	2400 baud
	D / U	1200 baud
	D / D	restore parameters
Auxiliary Port	7 / 8	
	U / U	9600 baud default
	U / D	2400 baud
	D / U	1200 baud
	D / D	restore parameters

U = Up (opened) switch; D = Down (closed) switch

RS-232 Ports

System unit diagnostics do not test the output drivers and physical connectors of the RS-232 ports. However, you can use the following procedure to test the serial terminal port if you suspect a problem.

1. Power on the terminal and system unit and verify that the system unit and the terminal are set to the same baud rate, typically 38400 baud.
   - **a.** Press the Setup Key on the keyboard and enter the Setup window on the X Terminal. On some system units it may be necessary to press Shift-Setup.
   - **b.** Enter the Configuration Summaries screen and select Peripheral Ports.
   - **c.** Check that the terminal and the system unit are at the same baud rate.
2. Power on the X Terminal and run the Extended Self-Test. Refer to *X Terminal Diagnostics* on page 6–27.

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3. Run the RS-232 Port Test. You need a RS-232 loopback connector for your terminal. (See the *TekXpress Family of X Terminals* service manual for the X terminal. To obtain this manual, contact your Tektronix representative.)

4. If the test does not detect any errors, replace the RS-232 cable. You can replace the Controller board or the internal 9-pin RS-232 cables.

To check the Host and Auxiliary ports, use a Serial Data Communication Analyzer to analyze the data transferred through the port.

X Terminal LAN Port

System unit diagnostics do not test the ethernet cables and terminators between the system unit and the X Terminal. However, you can use the following procedure to test the X Terminal LAN port if you suspect a problem:

1. Power on the X Terminal and run the Extended Self-Test. Refer to *X Terminal Diagnostics* on page 6–27.

2. Run the X Terminal LAN test. (See the *TekXpress Family of X Terminals* service manual for the X terminal. To obtain this manual, contact your Tektronix representative.)

Hard and Floppy Disk Drive Switch and Jumper Positions

The hard and floppy disk drive circuit boards have several switches and jumpers that are set at the factory for use with the TLA 510 or 520. You should never change these switch and jumper positions. However, if you suspect that the drives are the source of a problem, refer to Figures 6–21 through 6–24 for the correct positions of the switches and jumpers.

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The hard disk drive is a SCSI 3.5-inch disk drive. Three sizes of drives are available: 170 Mbyte (in early versions of the system unit), 270 Mbyte, and 1.2 Gbyte. Figure 6–21 shows the location of the Drive Select pins on the 170 Mbyte drive (the 270 Mbyte drive looks similar). The disk drives are shipped with no jumpers installed on the Drive Select pins.

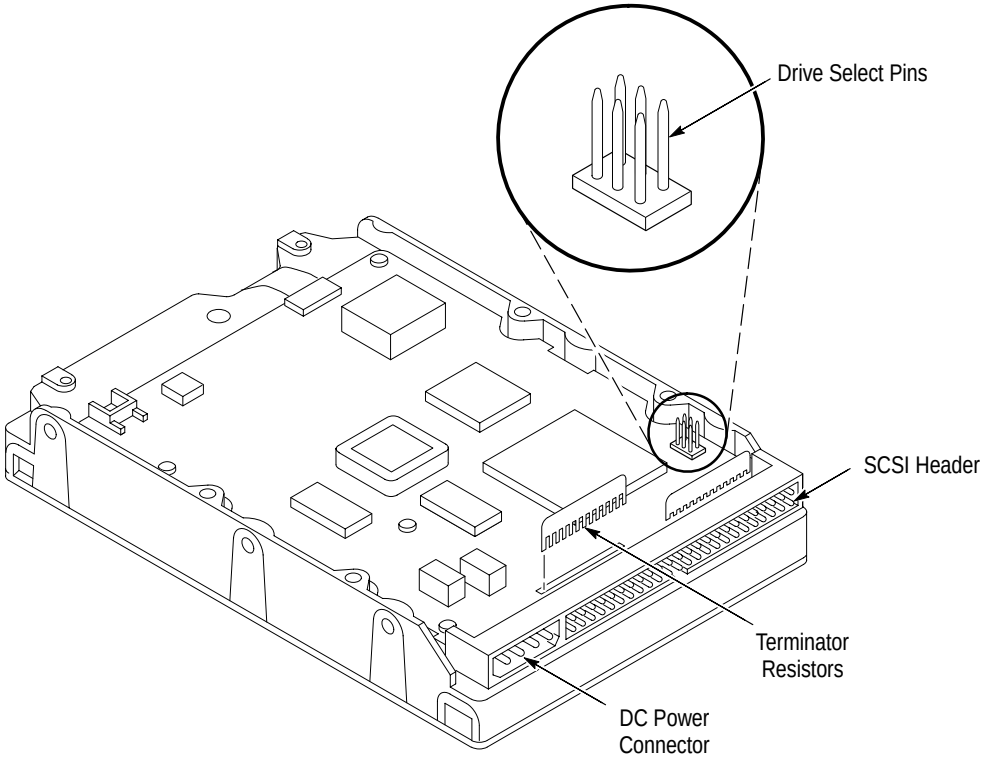


Figure 6–21: 170 and 270 Mbyte Hard Disk Drive

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The 1.2 Gbyte hard disk drive (Figure 6–22) looks similar to the 127 Mbyte and the 170 Mbyte hard disk drives. Locations of the Drive Select pins and connections are similar. The drive is shipped with the TE jumper installed and no Drive Select jumpers (A0-A2) installed, as shown in Figure 6–22.

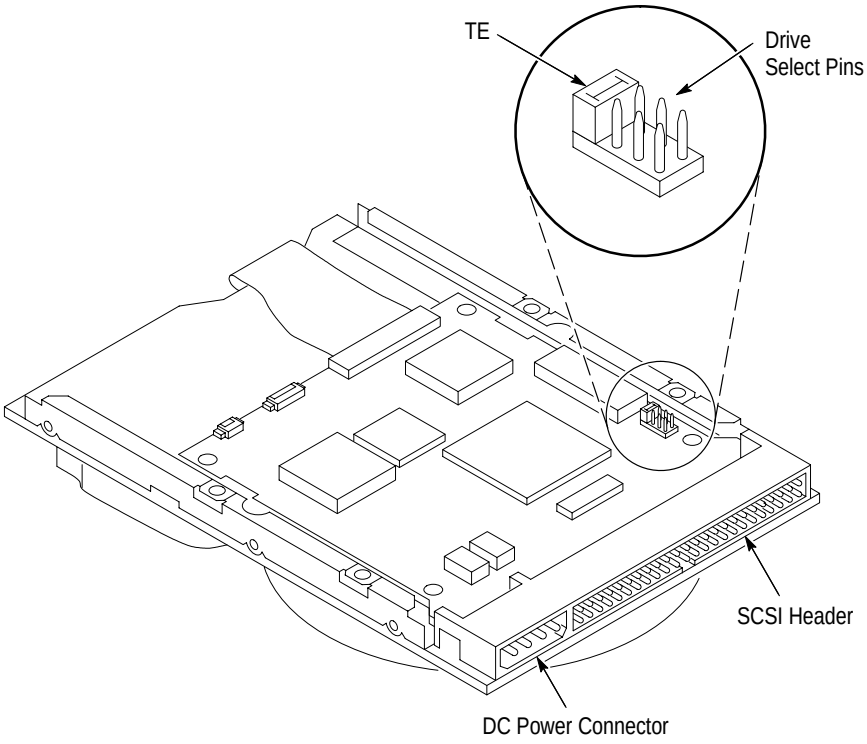


Figure 6–22: Jumper Locations on the 1.2 Gbyte Hard Disk Drive (Factory Settings Shown)

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Figure 6–23 shows the jumper settings for the 3.5-inch, 1.44 Mbyte Teac Model FD-235HF-3201 floppy disk drive.

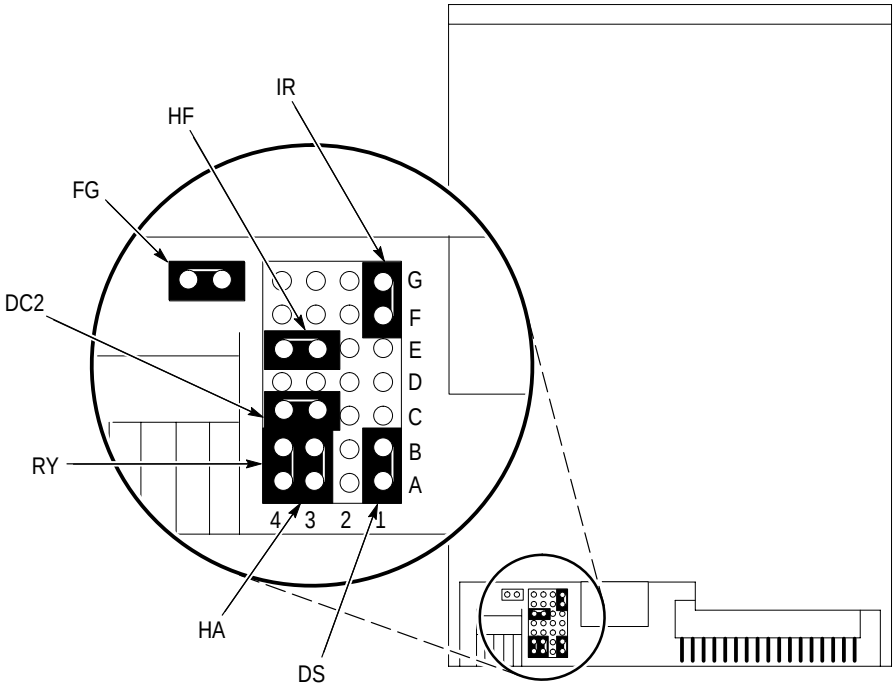


Figure 6–23: Jumper Locations on the 3.5-inch, 1.44 Mbyte Teac Model FD-235HF-3201 Floppy Disk Drive (Factory Settings Shown)

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Figure 6–24 shows the jumper settings for the 3.5-inch, 1.44 Mbyte Teac Model FD-235HF-6529 floppy disk drive.

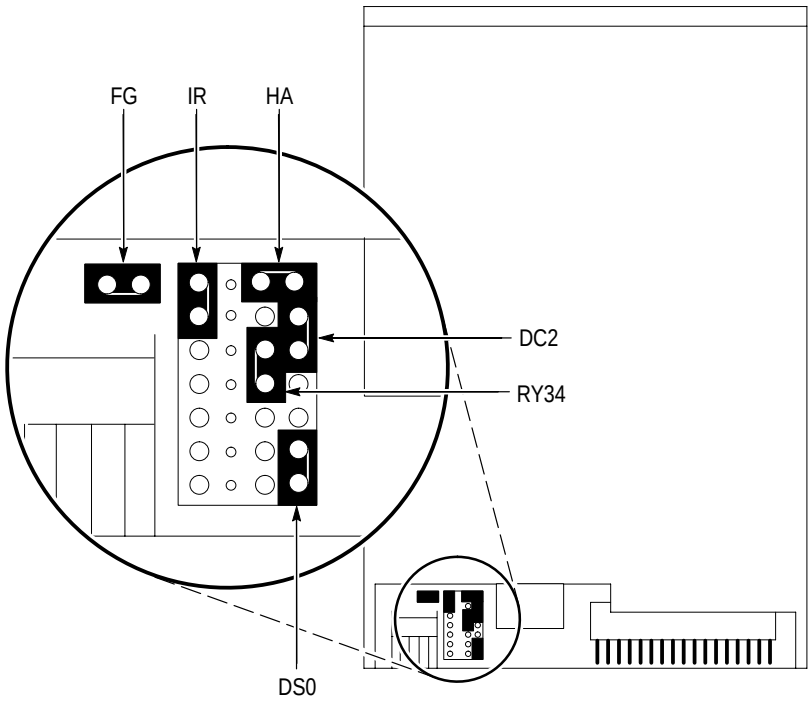


Figure 6–24: Jumper Locations on the 3.5-inch, 1.44 Mbyte Teac Model FD-235HF-6529 Floppy Disk Drive (Factory Settings Shown)

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Figure 6–25 shows the jumper settings for the 3.5-inch 1.44 Mbyte Teac Model FD-235HF-7529 floppy disk drive.

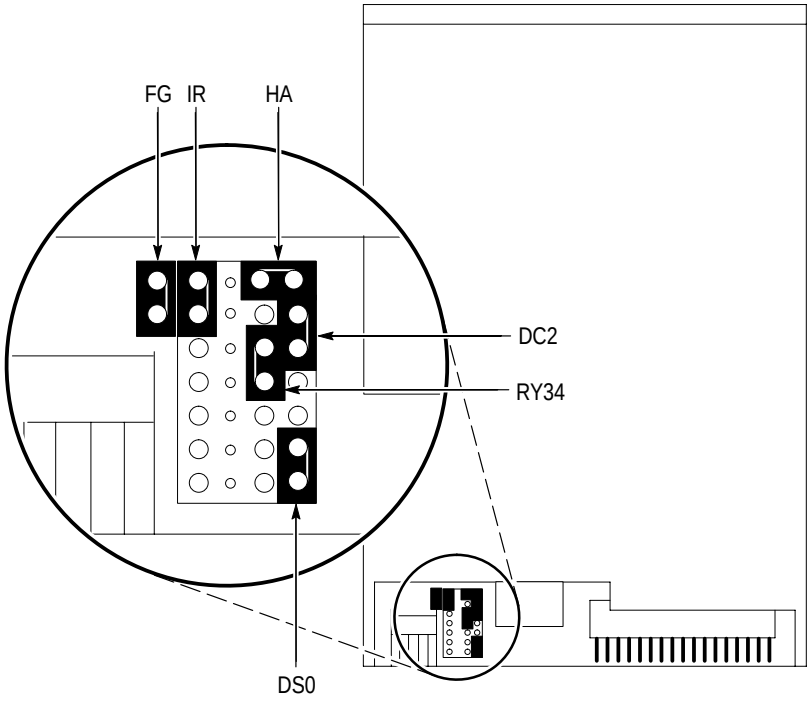


Figure 6–25: Jumper Locations on the 3.5-inch 1.44 Mbyte Teac Model FD-235HF-7529 Floppy Disk Drive (Factory Settings Shown)

Floppy Disk Drive Strapping on the Controller Board

The TLA 510 and 520 have a 1.44 Mybte, 3.5-inch floppy disk drive. The Controller board has two jumpers (J8710 and J9700) for future options. These jumpers select either a 5.25-inch floppy disk drive (not available in a TLA 510 or 520) or the 3.5-inch floppy disk drive. Figure 4–23 show the positions of these jumpers for the 3.5-inch floppy disk drive.

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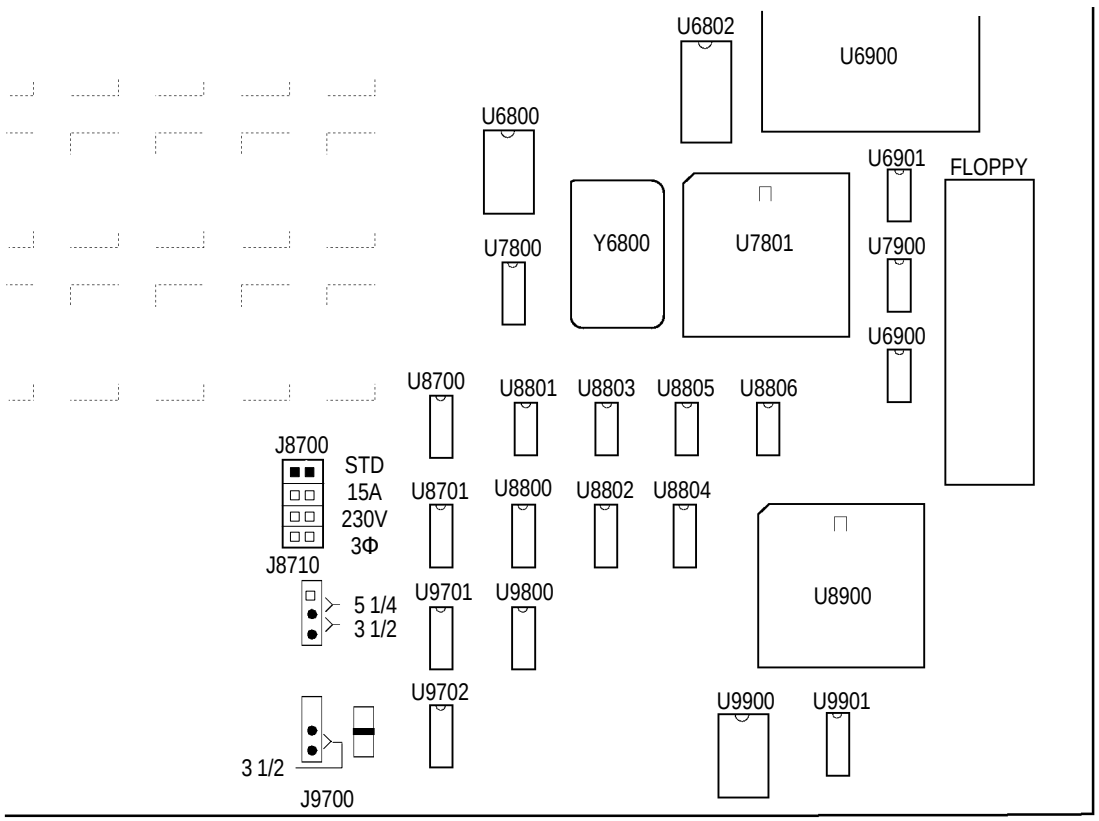


Figure 6–26: Location of Jumpers J8710 and J9700 on the Controller Board

Other Controller Board Jumpers

In addition to the hard and floppy disk drive jumpers, the Controller board has other jumpers that configure the Controller board for certain operations. J8700 shown in Figure 6–26, is used for power inputs. For the TLA 510 and 520, J8700 should always be in the STD position.

J1200 (not shown) is located on the rear of the Controller board near the Backplane board. J1200 is used to configure the Controller board for either the TLA 510 and 520 or for the DAS/SE. J1200 must be installed for TLA 510 and 520 operation. For DAS/SE operation J1200 is removed.

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Troubleshooting Modules

The following paragraphs provide troubleshooting information for the TLA 510 and 520 Modules.

Module Troubleshooting Overview

Use the following steps as an overview of troubleshooting the TLA 510 and 520 modules; detailed troubleshooting information is included later in this section.

1. If the module fails the power-on diagnostics, check the description for the four-digit error code from the Diagnostic menu. Refer to *Diagnostic Menu Error Codes* on page 6–36. If the module has a functional failure, check all connections between the TLA 510 or 520 and the system under test (SUT).
2. Check that the boards are fully seated into the backplane slot connectors. If necessary, power off the system unit, remove the module, reseat it, and power on the system. Verify that all probes and cables are fully seated.
3. If the module still fails, check if the problem is slot-related. Power off the TLA 510 or 520, install the failing module into a different slot, and power on the system. This will isolate system unit slot-related problems.
4. Remove the module and inspect it for physical damage or shorted leads or components.
5. Replace the module with a known-good replacement module. Check that the replacement passes its diagnostic tests.
6. If the module still has a problem, try the following:
   - **a.** Run the file system Check and Verify utilities to check if the problem is due to corrupted system software.
   - **b.** Remove all modules except the failing module to check if another module is interfering with the system bus. If the module no longer fails, reinstall the modules one-by-one to identify the cause of the problem.
   - **c.** Check that the power-supply voltages are within specification as stated on page 6–42.
   - **d.** Inspect the 540-pin connectors on the backplane for damaged, bent, or shorted pins.
   - **e.** Replace the Controller board with a known-good board to check the controller bus interface.

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92C96 Troubleshooting

Diagnostic tests check major portions of the circuitry on the 92C96 Data Module. Refer to page 6–38 for a list of diagnostic error codes. If diagnostics pass, but you still suspect a problem, you can use other methods to isolate the problem. First, operate the module in a different slot and see if the problem still exists. If it does, replace the module with a known-good module. Troubleshooting for the 92C96 module includes replacing fuses and heat sinks and repairing coaxial cables.

- Fusible Runs and Fuses. The 92C96 Modules have two fusible runs (F116 & F117) that require replacement fuse cartridges. On 92A96UD Modules, these runs have been replaced with actual fuses (refer to Figure 5–3 on page 5–7 for the location of the fuses). The fuses and fusible runs protect the +5 V circuitry on the module and to the probe power connector at J200. Refer to the *Replacable Electrical Parts List* for part number information.
- Heat Sinks. When replacing heat sinks for the eight comparator ICs (A27U215, A27U315, A27U415, A27U515, A27U610, A27U615, A27U715, and A27U815), affix them with a thermal-conductive adhesive such as Loctite Thermal Conductive Adhesive-Repairable, Item No. 00241. Make sure the heat sink and IC orientation are the same.
- Coaxial Cable Repair. You can order the optional coaxial probe cables and individual replacement coaxial conductors for the 92C96 Module as replacement parts. Refer to *Replaceable Mechanical Parts* for the appropriate part numbers. The replacement procedure is described below.

Equipment and Material Required. The following equipment and material are necessary to complete the replacement procedure:

- Replacement coaxial wire
- Replacement color-coded probe labels
- Cable assembly header latch release tool
- Masking tape
- Screwdriver, #1 POZIDRIV

Coaxial-Wire Replacement Procedure. Use the following procedure to replace a single coaxial wire in a coaxial-type probe assembly.

1. Identify the faulty channel by functional testing.
2. Swap the suspected faulty cable with another coaxial cable to ensure that the 92C96 board, podlets, and interface housing are functioning properly.
3. Find the pin number of the faulty channel in Table 6–13. If necessary, refer to the *92C96 and 92C96 Module User Manual* to identify the probes and sections.

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4. Locate the faulty coaxial wire by using the pin-number location illustration of the coaxial-cable assembly header (see Figure 6–27).

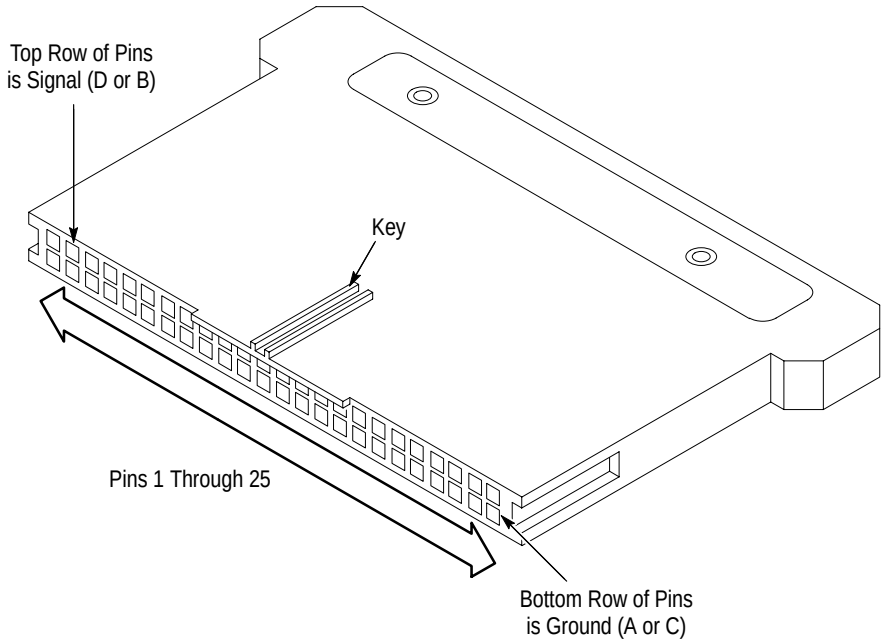


Figure 6–27: Coaxial Probe Cable Header Pin Orientation

Table 6–13: Probe-Cable Pin to Display-Channel Mapping

	Probe			
Pin Number	**A**	**B**	**C**	**D**
1	Clock_0	Clock_1	Clock_2	Clock_3
2	C0_7	C1_7	C2_7	C3_7
3	C0_6	C1_6	C2_6	C3_6
4	C0_5	C1_5	C2_5	C3_5
5	C0_4	C1_4	C2_4	C3_4
6	C0_3	C1_3	C2_3	C3_3
7	C0_2	C1_2	C2_2	C3_2
8	C0_1	C1_1	C2_1	C3_1
9	C0_0	C1_0	C2_0	C3_0
10	A1_7	A3_7	D1_7	D3_7
11	A1_6	A3_6	D1_6	D3_6

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Table 6–13: Probe-Cable Pin to Display-Channel Mapping (Cont.)

Pin Number	Probe			
	A	B	C	D
12	A1_5	A3_5	D1_5	D3_5
13	A1_4	A3_4	D1_4	D3_4
14	A1_3	A3_3	D1_3	D3_3
15	A1_2	A3_2	D1_2	D3_2
16	A1_1	A3_1	D1_1	D3_1
17	A1_0	A3_0	D1_0	D3_0
18	A0_7	A2_7	D0_7	D2_7
19	A0_6	A2_6	D0_6	D2_6
20	A0_5	A2_5	D0_5	D2_5
21	A0_4	A2_4	D0_4	D2_4
22	A0_3	A2_3	D0_3	D2_3
23	A0_2	A2_2	D0_2	D2_2
24	A0_1	A2_1	D0_1	D2_1
25	A0_0	A2_0	D0_0	D2_0

5. At each end of the cable assembly, remove the color-coded label from the side of the cable-header housings opposite the key to access the screws. Remove the screws from the header housings and the upper housing covers.

6. Lift the coaxial wires from the channels in the lower half of the housing. Note the orientation of these wires for later reinstallation.

7. Slide the black cable header forward in the lower housing half and remove it from the housing. Repeat this step for the other end of the assembly.

8. Use the header latch release tool to unlatch both contacts of the faulty coaxial wire from the header at each end of the assembly (refer to Figure 6–28). Do not lift the latches farther than necessary to unlatch the contacts of the coaxial wire to prevent damage to the latches (causing intermittent operation of the coaxial cable assembly). Extract the coaxial wire completely before releasing the latch.

9. Compress the mesh sleeve to increase its inside diameter as possible.

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10. Attach one end of the replacement coaxial conductor to an end of the faulty coaxial conductor in the following manner:

    a. Lay the two coaxial wires end-to-end with a 4-inch to 6-inch overlap.

    b. Wrap the overlapping portion of the two coaxial wires tightly with masking tape to temporarily splice them together.

11. Pull the faulty coaxial wire through the compressed mesh sleeve, so the replacement coaxial wire is drawn into and through the mesh sleeve. Stop when the replacement conductor is located in the proper position in the cable-wire bundle.

12. Unwrap and remove the masking tape from the splice of the two coaxial wires and discard the faulty wire.

13. At each end of the replacement coaxial wire, insert and latch the female contacts for both the signal (limp conductor) and the shield (rigid conductor) conductors into the cable header.

14. Reinsert the cable header into the lower half of the header housings. The cable header should be oriented so the signal-conductor side of the header is towards the key of the housing half.

15. Carefully relocate each coaxial wire into the channels of the lower housing half.

16. Replace the upper housing cover and reinstall the screws at each end of the cable assembly.

17. Stretch the mesh sleeve to its full length.

18. Replace the color-coded labels removed in step 5 with the appropriate colored label.

19. This completes the coaxial cable assembly repair. Test the cable assembly to ensure that the installation is successful.

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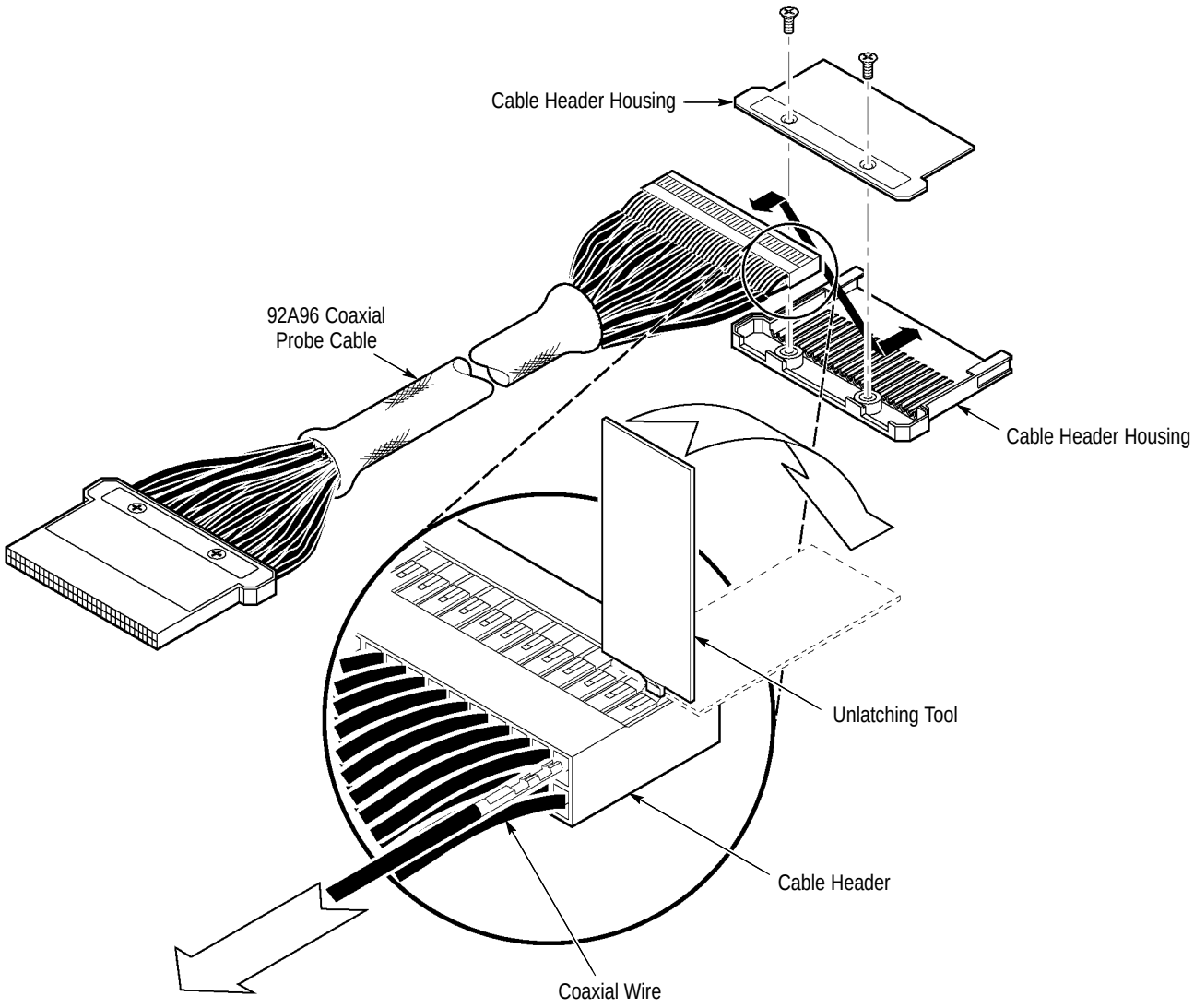


Figure 6–28: Removing a Coaxial Conductor (Wire)

92S16 Troubleshooting

Diagnostic tests check major portions of the circuitry on the 92C96 Pattern Generation Module. Refer to page 6–39 for a list of diagnostic error codes. If diagnostics pass, but you still suspect a problem, you can use other methods to isolate the problem. First, operate the module in a different slot and see if the problem still exists. If it does, replace the module with a known-good module. If you suspect the P6463A probe of being faulty, connect the probe to a known-good 92C96 module. Check that the probe is putting data out by connecting an oscilloscope to the output channels of the probe when the 92S16 is producing an alternating data pattern. (The probe podlets must be powered from an external power supply on the VH and VL probe leads; see the *92S16 Module User Manual*.)

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TLA LAN Troubleshooting

This section discusses problems that could cause the 92LANSE to lose or prevent communications with the X Terminal or host. The major parts of this section are divided between stand-alone operation and hosted operation.

X Terminal Traits

When performing TLA LAN troubleshooting, there are traits of the X Terminals you need to remember. These traits are:

- The terminal senses the network cable type (thinnet or thicknet) when the terminal is powered on.
- The three backpanel network connections (thinnet, thicknet, and twisted pairs) can only be connected one at a time. Multiple connections will prevent the terminal from operating properly.
- If the cable type is changed you must recycle the power in order for the terminal to recognized the cable type.

TLA Stand-Alone LAN Troubleshooting

This section discusses problems that could cause the 92LANSE to lose or prevent communications with the X Terminal. This section also provides suggestions that can help you determine where the problem might be. This section is divided into three parts:

- LAN Hardware
- X Terminal Software
- System Unit Software

LAN Hardware Troubleshooting. To verify that the hardware of the system unit and X Terminal are functioning properly, perform the following steps:

1. Check that the power cords for the terminal and the system unit are plugged into an appropriate socket.
2. Check that the fuses on the terminal and the system unit are good.
3. Check that all cabling between the system unit and the terminal are correct. Refer to *Installation* on page 2–1.
4. Check that the jumper of the 92LANSE board is in the correct position (Thicknet or Thinnet) for the current cabling setup.
5. Check the connections of the cables from the 92LANSE board to the backpanel of the system unit.
6. Power on the X Terminal and check for LED error codes on the keyboard. Refer to *X Terminal Diagnostics* on page 6–27.

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7. Run the complete X Terminal Diagnostics.

8. Power on the system unit and check the LEDs on the back of the system unit's Controller board if level 0 diagnostics halt. Refer to *Controller Board LEDs* on page 6–31.

X Terminal Software Troubleshooting. To verify that the software of the X Terminal and and system unit are functioning properly, perform the following steps. The first steps are for the X Terminal, followed by the system unit steps.

1. Power off the system unit and the X Terminal.

2. Power on the X Terminal and press the space bar until the terminal's Boot Monitor appears.

3. Check the terminal's default boot parameters as shown in Table 6–14.

Table 6–14: Terminal Factory Default Boot Parameters

Parameter	Default Value	Parameter	Default Value
IADDR	10.0.0.2	DNODE	0.0
IHOST	10.0.0.1	BMETHOD	ROM
IMASK	255.0.0.0	BDISPLAY	DISABLED
IGATE	0.0.0.0	BAFROM	NVRAM
BPATH	/XP300/os*		

*** On initial power on, the default value is /XP300/os and then changes to os. The BPATH value is case sensitive.**

4. Power the terminal off then on to boot from the X Terminal's flash ROM.

5. Verify that the serial window appears with the word "connected" inside.

NOTE*. If the serial window does not appear, you may need to reflash the X Terminal's Flash ROM. Refer to* Update Terminal Flash ROM *on page 6–94. You can also try the tftp boot process to boot the X Terminal. Refer to* tftp Boot Process *described after these procedures.*

If the serial window does not appear on the screen, you may need a separate RS-232 terminal to run the Configuration Utility.

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System Unit Software Troubleshooting. To determine that the software of the system unit is functioning properly, perform the following steps:

1. Power on the system unit with DIP switch number 1 down and number 2 up. The terminal will display the prompt BOOT?>.
2. Enter **/config** to display the Configuration Utility menu.
3. Verify that the proper network parameters are set. Refer to Figure 6–31 on page 6–88.
4. Verify the system unit software by running the file system check procedure and the verify function of the Install utility. Refer to *File System Check Procedure* on page 6–75 and *Verifying Base, Optional, and Application Software* on page 6–85. If necessary correct any errors.
5. Power off the terminal and system unit, and set the DIP switches of the system unit to the normal boot position (switches 1 and 2 up).
6. Power on the terminal and system unit. Wait for the system unit to complete its boot process and then verify communication by attempting to Ping the system unit from the terminal using the following procedure:
   a. After the X terminal has booted and the Serial window displays, press the Setup Key on the keyboard and enter the Setup window on the X Terminal. On some terminals it may be necessary to press Shift-Setup.
   b. Select Network Utilities from the Network Tables and Utilities pull-down menu.
   c. Enter the system unit's Internet address then press Enter. (You can get this address from the Configuration Utility menu.)
   d. Perform the Ping test to verify that there is communication between the X Terminal and the system unit.
7. Perform the tftp Boot Process, as described next, if the Ping test was successful but the TLA window does not appear when the system unit is booted normally.

The tftp Boot Process. Use this procedure if you cannot boot the TLA 510 or 520 from the terminals internal flash ROM. The serial window can be used to verify or modify the Configuration Utility settings:

1. Boot the X Terminal and immediately press the space bar until the prompt BOOT?> appears.
2. Set the system units DIP switches (located on the rear of the Controller board) to the normal operation position (all up).

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3. Wait approximately two minutes for the following to complete:
   - Power on diagnostics
   - LEDs at the rear of the Controller board begin to perform a continuous swirling pattern
   - The hard disk activity light no longer glows
4. Verify the proper internet parameters are set in the X Terminal monitor. Refer to Table 6–14 for factory default values.
5. Check that the BPATH is /XP300/os.

NOTE. *Case sensitivity does apply.*

6. Type **boot tftp** at the X Terminal boot prompt, then press Enter.
7. Verify that the boot progress indicator bar progresses from 0% to 100%. This should take approximately one minute. Once 100% is reached the Serial window followed by the TLA window should display.

TLA Network Troubleshooting

This section discusses problems that could cause the 92LANSE Modules to lose or prevent communications with your host. This section is divided into two parts:

- Problem Finding
- Communications

Equipment Required. You need the following equipment to perform these tests.

- One BNC-T connector (Tektronix part number 103-0030-XX)
- Two 50-ohm BNC terminator (Tektronix part number 011-0123-XX)

Problem Isolation. This section consists of the following parts:

- Checking the 92LANSE Module off the net
- Network hardware setup
- Network software setup

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Network Hardware Setup. The following steps check the network and 92LANSE hardware:

1. Determine if other users are connected. Is the status for the servers shown as Listening? If their status is Connected, the LAN is being used by another user or is hung.
2. Check that the thicknet and thinnet jumper (J686) on the 92LANSE module is in the proper position for the type of LAN cabling used.
3. Check that all the connections to the network are correct. Is the network properly terminated? If the network uses thinnet cable, is the thinnet T-connector attached directly to the LAN backpanel BNC connector (on the TLA 510 or 520) without 50-ohm extension cables?
4. Check that no metal part of the LAN cabling is grounded to earth ground. Insulated covers are available for insulating metallic parts of the network cable. Contact site network administrator for assistance.
5. Check that other hosts on the network can communicate with one another. Can they communicate with the TLA 510 or 520? For example, try the Ping procedure starting on page 6–61.
6. Network hardware problems may cause the Module to fail its external loopback test for a variety of reasons, such as a shorted or incorrectly terminated network cable. (This is possible for either a thinnet or thicknet network.)

   With a thicknet cable, tapping block connections to the ethernet cable center conductor may be open, intermittent, or noisy. First, determine if the problem is caused by the connection/termination or the thicknet transceiver. It may be helpful to isolate the 92LANSE Module from the network.
7. Check the LAN back-panel connector for continuity between the connector and the network interface.
8. If the TLA 510 or 520 is connected to a thinnet network with which repeaters are being used, it may be necessary to disable the Heartbeat signals. To disable the signals perform the following:

   a. Refer to *Removing The 92LANSE Module* on page 6–14 and remove the module.

   b. Reposition J790 from pins 1 and 2 to pins 2 and 3. This disables the Heartbeat signals.

   c. Replace and reconnect the module.
9. If the TLA 510 or 520 is connected to a thicknet network, check fuse F640 on the 92LANSE card. This fuse protects power to a media attachment unit.

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Network Software Setup. The following steps check the network and the TLA 510 and 520 LAN software.

1. Check that the proper network names, addresses, gateway options, and subnet mask values are assigned for both the TLA 510 or 520 and the X Terminal.
2. If you have 92XTerm, check if you have assigned a unique TLA 510 or 520 hostname and internet address and entered them in the /etc/hosts file, or its equivalent, on your host computer?

   Use the "cat" or "more" UNIX command to view the entries in the /etc/hosts file.

***NOTE**. The system or network administrator should modify this file.*

3. Does your host use ARP to resolve internet-to-ethernet address correspondence? Use the /etc/arp –a UNIX command, or its equivalent, to view the current contents of the hosts ARP table. If the 92LANSE Module has been exchanged, the entry in this table must be modified or cleared before the host can initiate communication with the new board.

***NOTE**. In most UNIX-like operating systems, unused entries are automatically cleared periodically if communication with the host has not taken place.*

   For example, use the UNIX command string "/etc/ping hostname" to test network operation; substitute the TLA 510 or 520 internet address for *hostname* to test communication to the TLA 510 or 520 via LAN.

4. Check that the LAN overlay contain the correct hostname, internet address, gateway address, and subnet mask. If not, enter the correct information in the Configuration Utility menu and reboot the LAN.
5. Check to see if ftp reports an error when the host issues a command. Refer to *Using ftp* in the *92LANSE Instruction Manual* for error messages.
6. If the host runs the DEC VMS Operating System, check that a third-party TCP/IP-compatible FTP software package been properly installed and set up on the host. If not, contact your system administrator or Tektronix sales engineer.

LAN Communications

The TLA 510 and 520 LAN can interface and communicate with a variety of host computers running various operating systems.

Host computers communicate with the TLA 510 or 520 using either the ftp (file transfer protocol), rsh (remote shell), or rcp (remote copy) commands.

Refer to the *92LANSE Instruction Manual* if you use ftp. The rsh and rcp commands are not discussed in the *92LANSE Instruction Manual*, but they function because the LAN Support Software contains a rshd daemon. You can execute the ftp, rsh, and rcp commands from only a host computer terminal.

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You can use either the assigned *hostname* or the TLA 510 or 520 internet address with these commands. The actual hostname or internet address should be substituted for the *hostname* or the *internet address* shown in the example.

The following examples show the ftp, rsh, and rcp command syntax. Each example is followed by a brief description.

- "ftp hostname" initiates an ftp session with the computer called *hostname*.
- "ftp 8.1.75.128" initiates an ftp session with the host located at internet address 8.1.75.128.
- "rsh hostname date" causes the host called *hostname* to execute the date command and return the output from the command to the requesting host.
- "rsh 8.1.75.128 /bin/sh –i" causes the host at internet address 8.1.75.128 to invoke an interactive shell process. This is similar to a remote login (rlogin) to the host. Use Control-d to end this shell. Be careful when logged into the TLA 510 or 520, since you could damage the software on the hard disk drive.
- "rcp hostname:/la_files/Setup/lan_test lan_test.local" copies the file lan_test from the directory /la_files/Setup on the computer called *hostname* to a file called lan_test_local in the current directory of the host initiating the command.

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Loading System Software

System software is loaded onto the hard disk at the factory. It is only necessary to load the system software using the supplied floppy disks under the following conditions:

- When you upgrade the software version
- When a major system software failure damages one or more system files
- When you replace the hard disk

You can load the system software onto the hard disk using a series of steps described in this section. These steps differ from those used to make copies of floppy disks and to load application software using the Disk Services menus.

The System Software consists of the following floppy disks:

- The SYSTEM UTILITIES disk (FORMAT & MAKE). This disk contains the SCSI Hard Disk Format utility and the file system Make utility. Use the SCSI Hard Disk Format utility to format the hard disk or modify the swap partition size, and the file system Make utility to create a new file system on a newly formatted hard disk. The Make utility also includes the file system Check procedure to check or repair the file system.
- The SYSTEM UTILITIES disk (INSTALL). This disk contains the Install Utility. Use the Install utility to install and verify the Base System Software, the optional system software, and the application software. You can also use the Install utility to remove the optional system software and application software. The file system Verify function is an option to the Install utility.
- Base System Software (volume 1 through volume n). These disks contain the essential software for the logic analyzer. You must install all the files from these floppy disks.
- Optional System Software. These disks contain module specific portions of the system software that are not required for all configurations of the logic analyzer. You must install the portions which correspond to your configuration.
- Applications Software. These disks contain special purpose software that is not available with the base system software or the optional system software disks. Application software can be installed later using the Disk Services menu.

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SCSI Hard Disk Format Utility

You need to reformat your hard disk under the following conditions:

- When you replace the hard disk with an unformatted hard disk
- When a serious system failure corrupts the hard disk format
- When the system reports that it cannot read block 0 of the hard disk



CAUTION. *Reformatting the hard disk or running the file system Make utility destroys all files on the hard disk. If possible use one of the methods described below to save files from the hard disk.*

Formatting prepares the hard disk for data storage; all previous stored data is destroyed. You should use one of the following methods to save user files from the hard disk:

- Copy the files to floppy disks using the Backup/Restore utility supplied in the Disk Services Menu.
- Transfer the files to a host computer using ftp or Kermit.

Running the SCSI Hard Disk Format Utility

To access the main menu of the SCSI Hard Disk Format Utility, follow these steps:

1. Power off the logic analyzer. Face the rear of the system unit and locate the DIP switches mounted on the Controller board (as shown in Figure 6–29).
2. Place DIP switch 1 (the leftmost DIP switch) in the closed (down) position. Place DIP switch 2 in the open (up) position. Leave all other DIP switches in their original positions.
3. Power on the terminal. Power on the system unit, wait for the prompt BOOT?>, and then insert the System Utilities disk labeled FORMAT, MAKE.
4. In response to the BOOT?> prompt, type f:/format and press the Return key.

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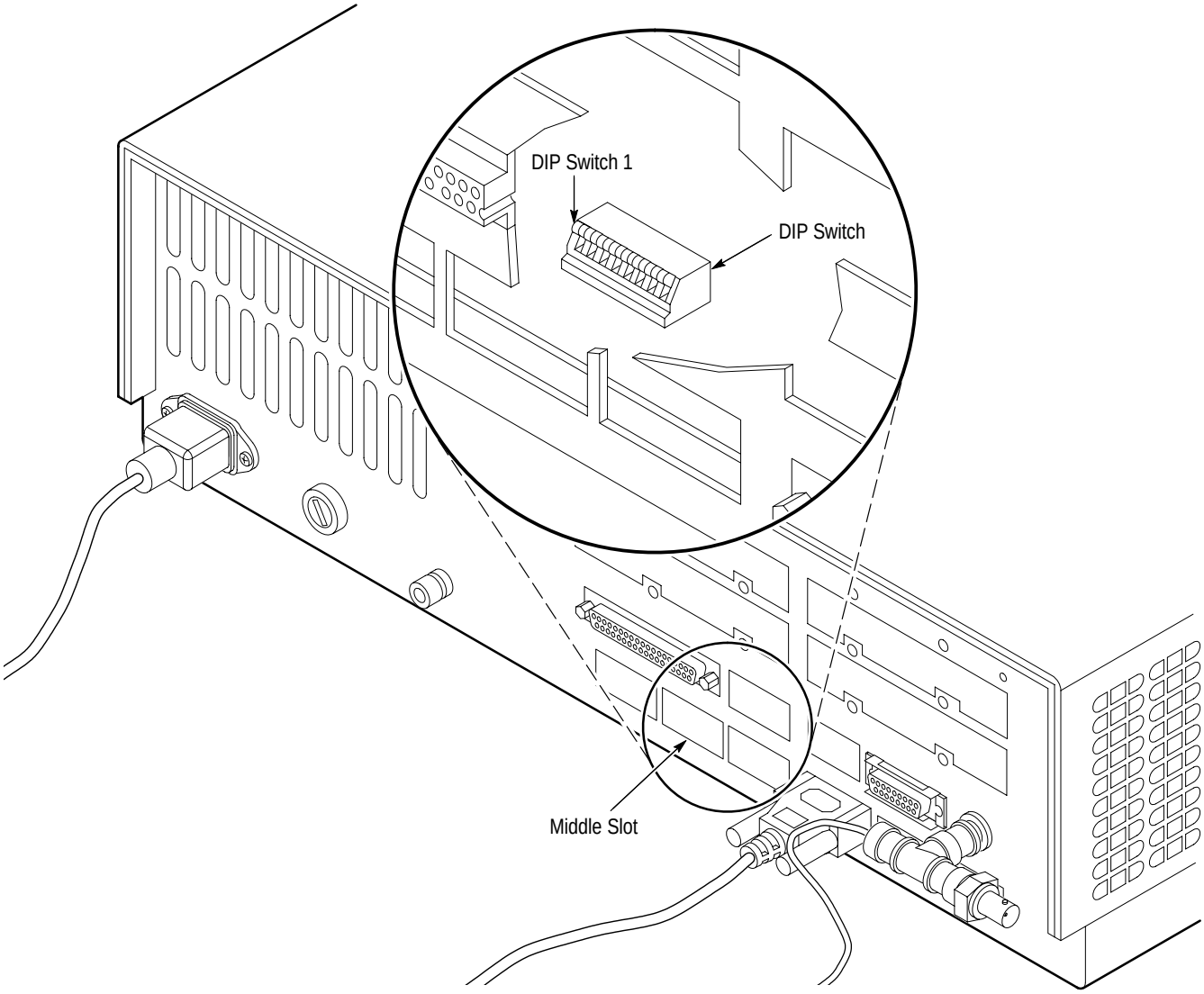


Figure 6–29: DIP Switch Location

The following paragraphs briefly discuss the menus and submenus in the SCSI Hard Disk Format Utility.

SCSI Hard Disk Utility Main Menu

The main menu displays general information about the hard disk and how it is partitioned. If the hard disk has not been formatted, the main menu will indicate that the hard disk has no valid partition information. Figure 6–30 shows an example of the main menu for the SCSI Hard Disk Format Utility.

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```
Main Menu - SCSI HARD DISK FORMATTER

Disk Description   : /xxx/xxxx
  Capacity         : xxxx Kbytes (512 byte logical block size)
  Compatibility    : SCSI-2
  Manufacture ID   : xxxxxxxxxxxx
  Product ID       : xxxxxxxxxxx
  Revision NO      : xxx

Disk Partition List:

NUMBER  NAME     PURPOSE  LOCATION  BLOCKS   (kbytes)
X       /xxx/xxx  ROOT     xxxxx     xxxx    (xxxxxxxxxxx)
X       /xxx/xxx  SWAP     xxxxx     xxxx    (xxxxxxxxxxx)
X       /xxx/xxx  MAP      xxxxx     xxxx    (xxxxxxxxxxx)
X       /xxx/xx   ALL      xxxxx     xxxx    (xxxxxxxxxxx)

Selections Available:
 a. Format Setup Menu
 b. Change Swap Size Menu
 c. Show Bad Block List
 d. Exit

 Enter choice [default = d]
```

Figure 6–30: SCSI Hard Disk Format Utility Main Menu

Select the submenu or information you want to enter. The following choices are:

- Enter the Format Setup Menu (for formatting the hard disk)
- Enter the Change Swap Size Menu (for changing the swap partition space size)
- Show Bad Block Lists
- Exit the menu

To make a selection, enter the letter preceding the selection description. If you only press the Return key, the default action inside the square brackets will be selected.

Format Setup Menu

This menu initiates the formatting of your hard disk; it also lets you specify the swap space size value. This swap space size value will be used the next time you request a swap space size change in the Change Swap Size submenu or Initiate Format in this menu.

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```
FORMAT SETUP MENU

Current Active Options:
    Defects-Manufacturers and Grown (Recommended)
   Swap Size - 6 Meg (Recommended)

Selections Available:
 a. Initiate Format
 b. Use "Recommended" Settings
 c. Defects-Manufacturers and Grown (Recommended)
 d. Defects-Manufacturers Only
 e. Swap Size - 6 Meg (Recommended)
 f. Swap Size - 8 Meg
 g. Go to Main Menu

Enter choice [default = g]:
```

The selections in the Format Setup menu let you format the hard disk, change the swap size option, or return to the main menu. Option c maps out the manufacturer's bad block list and any bad blocks that may have been detected by earlier format operations. Option d maps out the manufacturer's bad block list only. To make a selection, enter the letter preceding the selection description. If you only press the Return key, the default action inside the square brackets will be selected.

If you select Initiate Format, the SCSI hard disk's internal disk format command will be initiated. The current active swap size option will be used during the format operation. The following warning message and prompt will be displayed.

```
!!!WARNING: About to format hard disk. This will destroy
        any data currently stored on the disk!!!!!!!!

Swap size - 6 Meg (Recommended)

Are you sure you want to continue (y/n) [default =n]...
```



CAUTION. *Reformatting the hard disk or running the file system Make utility destroys all files on the hard disk. Before running one of these utilities, use one of the methods described earlier in this section to save the user files from the hard disk.*

At this point, if you want to continue, press y. If you do not want to format your hard disk, press n or press the Return key (default is n – do not continue).

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After formatting the hard disk, the utility verifies that all blocks on the hard disk can be read. During the verification process, a series of **.** and **+** characters are printed on the screen to show the progress of the disk verification. If any errors are found, the utility stops and displays the errors.

The bad block handling is done automatically by the SCSI formatting process. After successfully formatting the hard disk, the partitioning information will be written to the hard disk.

If you select options e or f in the Format Setup menu, the swap space size option will be changed accordingly; for more information on changing the swap space size, refer to the discussion under *Change Swap Size Menu*.

Change Swap Size Menu

Use the Change Swap Size menu to change the swap space size of a previously formatted hard disk. You can also change the swap space size option; this option will be used the next time you request the swap space size through the Make Change selection in this menu or the next time that you use the Initiate Format option in the Format Setup menu.

NOTE. *Changing the size of the swap partition space on your hard disk does not require reformatting the hard disk (unless the disk has never been formatted), but does require you to rebuild the file system using the Make utility. Running the Make utility will destroy the data saved on the disk. Be sure to save all the user files using one of the methods described earlier in this section.*

Swap space is the area reserved on the hard disk for temporarily storing program information during operation. The swap space is only used when there is not enough memory available on the system.

When the instrument runs out of swap partition space, normal operation cannot continue and an error message will be displayed. If this happens, you should use the Change Swap Size option to increase the size of the swap partition. However, increasing the size of the swap partition also decreases the amount of hard disk space available for storing other files such as reference memories, setups, and autorun definitions.

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```
CHANGE SWAP SIZE MENU

Current Active Options:

   Swap Size - 6 Meg (Recommended)

Selections Available:
 a. Make change
 b. Swap Size - 6 Meg (Recommended)
 c. Swap Size - 8 Meg
 d. Go to Main Menu

Enter choice [default = d]:
```

The four selections in the Change Swap Size menu let you initiate the change for the swap size for the hard disk, change the swap size option to 6 Mbytes, change the swap size option to 8 Mbytes, or return to the main menu. To make a selection, enter the letter preceding the selection description. If you press Return only, the default action inside the square brackets will be selected.

If you select options b or c, the swap space size option will change accordingly. Although selecting these options will not change the hard disk, the option that you select will be used when you select Make Change in this menu or when you select Initiate Format in the Format Setup menu.

If you select option a, the SCSI hard disk's swap space size will change. The current active swap size option will be used. The following warning message will be displayed:

```
!!!WARNING: About to change swap space size for hard disk.
        This will destroy any data currently stored on
         the disk!!!!!!!!

Swap size - 6 Meg (Recommended)

Are you sure you want to continue (y/n) [default =n]...
```



CAUTION. *Reformatting the hard disk or running the file system Make utility destroys all files on the hard disk. Use one of the methods described earlier in this section to save files from the hard disk.*

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At this point, if you want to continue, press y. If you do not want to change the swap space size of your hard disk, press n or press the Return key (default is n – do not continue).

If you try to change the swap space size of an unformatted hard disk, an error message will be displayed and the change request will be cancelled.

If the hard disk has never been formatted, you must format it before changing the swap space size. A swap partition is created after the hard disk is formatted or reformatted. The default size of the swap partition is 6 Mbytes; you can change it to 8 Mbytes.

After the change swap space size operation completes, you should return to the BOOT?> prompt by leaving the SCSI Hard Disk Format Utility (Select the Exit option in the Main Menu). You must then run the Make Utility to build the file system and the Install Utility to reload the system software after changing the size of swap partition. If you do not run these two utilities, the instrument will not function properly. Both of these utilities are described later in this section.

Bad Block List Display

The SCSI Hard Disk Format Utility lets you view your hard disk's bad block list (a bad block is an area on the hard disk that contains unusable bytes).

The Bad Block List display shows all known Manufacturer's defects and Grown defects (defects developed on the hard disk after it was shipped from the factory). The bad blocks will be listed by head, cylinder, and sector. The partition or file system block the defects are associated with is not given. It is not necessary (nor possible) to add blocks to these lists.

```
BAD BLOCK LIST DISPLAY

    LIST NAME (defect count) = head:cyl:sector, ...

    Manufacturer Defects (3) =  X:X:X, X:X:X, X:X:X

    Grown defects (0) = None

    Press any key to return to the Main Menu:
```

If the system software detects bad blocks while the instrument is running, the blocks are automatically added to the bad block list by the SCSI hard disk drive.

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File System Make Utility

The file system Make utility either creates a new, empty, file system and destroys all previously stored files on the hard disk, or it checks and repairs the existing file system. The utility prompts you to select one of the two options. Use the file system Check option to repair file system damage which can result from an abnormal shutdown of the instrument. Before running the Make procedure of this utility use the system software Disk Services menu to save all user created files on floppy disks.

***NOTE**. If the hard disk drive has been seriously corrupted, it may not be possible to save files on floppy disks. It is a good idea to perform regular backups of your user-generated files.*

Running the File System Make Utility

If the BOOT?> prompt is displayed, proceed to step 4. If not, follow steps 1, 2, and 3 before continuing with step 4.

1. Power off the logic analyzer. Face the rear of the system unit and locate the DIP switches mounted on the Controller board (refer to Figure 6–29).
2. Place DIP switch 1 (the leftmost DIP switch) in the closed (down) position. Place DIP switch 2 in the open (up) position. Leave all other DIP switches in their original positions.
3. Power on the terminal. Power on the system unit, wait for the prompt BOOT?>, and then insert the floppy disk labeled FORMAT, MAKE.
4. In response to the BOOT?> prompt, type **f:/make** and press the Return key. The following menu is displayed:

```
Press "m" to run the file system Make procedure.
Press "c" to run the file system Check Procedure -->
```

5. Type m to create a new file system. This destroys all files on the hard disk. A warning message and prompt will be displayed; type y to continue with the Make utility.

File System Check Procedure

If you type c in step 4, the file system Check procedure repairs the damaged file system after a system failure occurs. An unexpected loss of power, or certain software or hardware failures can corrupt the file system and cause the logic analyzer to shut down in an uncontrolled fashion. When this happens, recent file system changes may not be completely written to the hard disk and the file system on the hard disk may be inconsistent.

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NOTE. *If you run the File System Check procedure from the floppy disks, the logic analyzer will ignore the settings in the Boot Option overlay.*

The logic analyzer normally performs the file system Check procedure at power on unless you change the parameters in the Boot Option overlay to the Diagnostics menu (refer to *Diagnostics, File Ssytem Checks,and the Boot Option Overlay* on page 2–16 for more information on setting the boot options). Under certain conditions, the logic analyzer may ask you to perform the file system Check procedure manually. (In this case you would perform this procedure.) The file system Check procedure may not be able to completely recover from all types of damage to the file system. If system software files are either corrupted or cleared, you must rebuild the file system using the file system Install utility.

NOTE. *You must run the file system Check procedure when (at power on) a message indicates that the file system has been damaged and cannot be automatically repaired. The logic analyzer will not operate with a damaged file system that it cannot repair.*

There are six phases of the file system Check procedure (described later in detail). During these phases, software attempts to reconstruct the file system by deleting unreferenced files, rebuilding the free block list, and fixing any inconsistencies. It may take multiple attempts to complete the repair process. You should run the file system Check procedures until you no longer get errors or queries (normally no more than five times).

Once you have started the file system Check procedure, it proceeds automatically. The check procedure goes through six phases; these are detailed in Tables 6–15 through 6–19. These tables list typical messages that can be displayed during the file system Check procedure and an explanation of each message. Where a message in these tables is followed by a word in parentheses, the word indicates the actual prompt message you will see on the screen. The tables also contain recommended responses to the error messages.

When the file system Check procedure finds an inconsistency in the file system, it prompts you to take corrective action. There are several approaches to correcting file system problems, depending on the situation. Usually, answering y to a CLEAR? prompt or n to a RECONNECT? prompt corrects the problem without damaging any files on the hard disk. If a file has a size of 0, it can always be cleared. After clearing any files, you should run the Verify option of the Install utility to make sure that no system files were deleted. If the message EXCESSIVE BAD BLOCKS. CONTINUE? appears, you should enter y to continue. (A file system bad block is not the same as a bad block on the hard disk.)

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NOTE. *If you receive the Excessive Bad Blocks message, you must repeat the file system Check procedure until you get through it with no errors reported.*

All problems may not be fixed the on first pass through the file system Check procedure; you may have to rerun the procedure several times. If all checks are successfully completed, the number of files, blocks, and the amount of free space is printed, and the following prompt is displayed:

```
Do you want to rerun the File System Check Procedure
(y/n)[n]:
```

Enter y to the prompt only if all checks did not complete successfully. If you enter n, the BOOT?> prompt is displayed.

1. Phase 1: Check Blocks and Sizes. This phase checks the inode section of the file system; errors uncovered here usually indicate serious corruption of the file system. Table 6–15 summarizes the error messages that can be generated during Phase 1 testing. In the table, a word in parentheses following an error message indicates the actual prompt message that appears on the screen.

Table 6–15: Phase 1 File System Check Error Messages

Message	Explanation
UNKNOWN FILE TYPE I=I (CLEAR?)	This message indicates that the procedure found an unknown type of file. Type y in response to this message.
LINK COUNT TABLE OVERFLOW (CONTINUE?)	An internal error has been found. Repeat the steps for the file system Check procedure after completing the current pass. Type y in response to this message. May require several y responses.
B BAD I=I	The procedure detected an illegal block number B in inode I.
EXCESSIVE BAD BLOCKS I=I (CONTINUE?)	The procedure detected 10 or more bad block numbers. Type y in response to this message. Run the file system Check procedure again after completion.
B DUP I=I	The procedure identified a duplicate block B in inode I.
EXCESSIVE DUP BLKS I=I (CONTINUE?)	The procedure detected too many duplicate blocks in inode I. Type y to continue; when finished, run the file system Check procedure again.
DUP TABLE OVERFLOW (CONTINUE?)	There has been an internal table overflow. Type y to continue; when finished, run the file system Check procedure again.
POSSIBLE FILE SIZE ERROR I=I	A possible error in file size has been detected. After completing the file system Check procedure, run the system software Install utility, Verify option, to ensure that no files are corrupted.

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Table 6–15: Phase 1 File System Check Error Messages (Cont.)

Message	Explanation
DIRECTORY MISALIGNED I=I	A possible directory error has been detected. After completing the file system Check routine, run the system software Install utility, Verify option, to ensure that no files are corrupted.
PARTIALLY ALLOCATED INODE I=I (CLEAR?)	A partially allocated inode has been detected. Respond with y. After completing the file system Check procedure, run the system software Install utility, Verify option, to ensure that no files are corrupted.
PHASE 1B: RESCAN FOR MORE DUPS	This message may be displayed if the procedure is rescanning for additional duplicate block entries in the inode structures.

2. Phase 2: Check Path Names. This phase removes files with corrupted inodes detected in the Phase 1 check. Table 6–16 summarizes the error messages that can be generated during Phase 2 testing.

Table 6–16: Phase 2 File System Check Error Messages

Message	Action
ROOT INODE UNALLOCATED. TERMINATING	You must rebuild the file system. First, run the file system Make procedure. Then, use the file system Install utility to reload the system software.
ROOT INODE NOT DIRECTORY (FIX?)	Try typing y in response to this message. If this generates a large number of errors, you will have to rebuild the system. Do this by running the file system Make procedure followed by the file system Install utility to reload the system software.
DUPS/BAD IN ROOT INODE (CONTINUE?)	Try typing y in response. If this generates a large number of errors, you will have to rebuild the system. Do this by running the file system Make procedure followed by the file system Install utility to reload the system software.
I OUT OF RANGE I=I NAME=F (REMOVE?)	The procedure detected a directory entry with an out-of-range inode number I; type y in response. Run the file system Install utility, Verify option, to ensure that no files are corrupted.
UNALLOCATED I=I OWNER=O MODE=M SIZE=S MTIME=T NAME=F (REMOVE?)	The procedure detected a directory entry with no allocation bits set; type y in response. Run the system file system Install utility, Verify option, to ensure that no system files have been deleted.
DUP/BAD I=I OWNER=O MODE=M SIZE=S MTIME=T DIR=F (REMOVE?)	The procedure detected duplicate or bad block numbers associated with this file; type y in response. Run the file system Install utility, Verify option, to ensure that no system files have been deleted.

3. Phase 3: Check Connectivity. This phase checks for un-referenced directories. Table 6–17 summarizes the error messages that can be generated during Phase 3 testing.

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Table 6–17: Phase 3 File System Check Error Messages

Message	Explanation
UNREF DIR I=I OWNER=O MODE=M SIZE=S MTIME=T (RECONNECT?)	The procedure detected an un-referenced directory; you have no recourse but to clear it. Type n in response to the RECONNECT? prompt. The procedure prompts you to clear the inode. Type y in response to the CLEAR? prompt. Run the file system Install utility, Verify option, to ensure that no system files have been deleted.
SORRY. NO lost+found DIRECTORY	When this message displays, you must rebuild your system. First, run the file system Make procedure, then use the file system Install utility to reload the system software.
SORRY. NO SPACE IN lost+found DIRECTORY	When this message displays, you must rebuild your file system. First, run the file system Make procedure. Then use the file system Install utility to reload the system software.

4. Phase 4: Check Reference Counts. This phase checks link count information in the file system. You will usually see some type of error here. As a general rule, if a file with a SIZE of 0 is un-referenced, you should clear it (do not reconnect it). Table 6–18 summarizes the error messages that can be generated during Phase 4 testing.

Table 6–18: Phase 4 File System Check Error Messages

Message	Explanation
UNREF FILE I=I OWNER = 0 MODE=M SIZE=S MTIME=T (RECONNECT?)	An un-referenced file has been detected; always type n in response. Note the file size; if the file has a size greater than 0, run the file system Install utility, Verify option, to ensure that no system files have been deleted. Most files that show up here are temporary files. Deletion of these files is harmless since the files would not be usable if you were to try to reconnect them.
(CLEAR?)	If you type n at a RECONNECT prompt, another prompt appears telling you to clear the file. You should then type y in response.
LINK COUNT FILE I=I OWNER=O MODE=M SIZE=S MTIME=M COUNT=X SHOULD BE Y (ADJUST?)	An incorrect link count has been detected; type y in response.
LINK COUNT DIR I=I OWNER=O MODE=M SIZE=S MTIME=M COUNT=X SHOULD BE Y (ADJUST?)	An incorrect link count has been detected; type y in response.
LINK COUNT F I=I OWNER=0 MODE=M SIZE=S MTIME=M COUNT=X SHOULD BE Y (ADJUST?)	An incorrect link count has been detected; type y in response.
UNREF FILE I=I OWNER=O MODE=M SIZE=S MTIME=M (CLEAR?)	An un-referenced file has been detected; type y in response. If the file has a size greater than 0, run the file system Install utility, Verify option, to ensure that no system files have been deleted.
UNREF DIR I=I OWNER=O MODE=M SIZE=S MTIME=M (CLEAR?)	An un-referenced directory has been detected; type y in response. If the file has a size greater than 0, run the file system Install utility, Verify option, to ensure that no system files have been deleted.

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Table 6–18: Phase 4 File System Check Error Messages (Cont.)

Message	Explanation
BAD/DUP FILE I=I OWNER=O MODE=M SIZE=S MTIME=M (CLEAR?)	A file inode containing bad blocks of duplicate blocks has been detected; type y in response. If the file has a size greater than 0, run the file system Install utility, Verify option, to ensure that no system files have been deleted.
BAD/DUP DIR I=I OWNER=O MODE=M SIZE=S MTIME=M (CLEAR?)	A directory inode containing bad blocks or duplicate blocks has been detected; type y in response. If the directory has a size greater than 0, run the file system Install utility, Verify option, to ensure that no system files have been deleted.
FREE INODE COUNT WRONG IN SUPERBLK (FIX?)	An inconsistency in the free inode count has been detected. The actual number of free inodes does not match the number stored in the superblock. Type y in response.

5. Phase 5: Check Free List. This phase checks for errors in the free block list. Table 6–19 summarizes the error messages that can be generated during Phase 5 testing.

Table 6–19: Phase 5 File System Check Error Messages

Message	Explanation
EXCESSIVE BAD BLKS IN FREE LIST (CONTINUE?)	More than 10 bad block numbers in the free block list have been detected; type y in response.
EXCESSIVE DUP BLKS IN FREE LIST (CONTINUE?)	More than 10 duplicate block numbers in the free block list have been detected; type y in response.
BAD FREEBLK COUNT	This message indicates that the free block count is incorrect. No action is required.
X BAD BLKS IN FREE LIST	This message indicates that there are X bad blocks in the free list. No action is required.
X DUP BLKS IN FREE LIST	This message indicates that there are X duplicate blocks in the free list. No action is required.
X BLK(S) MISSING	This message indicates that there were X blocks unused by the file system that were not in the free list. No action is required.
FREE BLK COUNT WRONG IN SUPERBLOCK (FIX?)	An inconsistency in the free block count has been detected. The free block count in the superblock is incorrect; type y in response.
BAD FREE LIST (SALVAGE?)	The free block list must be repaired; type y in response.

6. Phase 6: Salvage Free List. This phase rebuilds the file system free block list. There are no error messages generated in this phase of the file system Check procedure.

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File System Install Utility

Use the file system Install utility to install and verify the Base System Software, the optional system software, and application software. You can also use the Install utility to remove the optional system software, and application software.

You must install the Base System Software after you run the file system Make utility, when you upgrade to a new version of system software, or to repair any damage to the system software from an abnormal shutdown of the logic analyzer. You can also install the optional system software and the application software at this time. However, you can also install the application software using the Disk Services menu later.

In all cases, you will need to install some portion of the optional system software together with the Base System Software. You can use the Install utility later to install or remove any optional system software. However, you cannot use the Install utility to remove the Base System Software.

Removing and Installing Software

The file system Install utility has three functions. Its main function is to install the software including the Base System Software, the optional system software, and application software. You can use it to remove optional system software or application software. You can also use it to verify that the installed software is both complete and correct.

Installing Base System Software. The Base System Software contains the essential software for the instrument. Use this program to add or replace Tektronix supplied files. The program will not disturb user generated files (such as, reference memories and system setups).

If the BOOT?> prompt is already displayed, proceed to step 4. If not displayed, begin with step 1.

1. Power off the logic analyzer. Face the rear of the system unit and locate the DIP switches mounted on the Controller board (refer to Figure 6–29).
2. Place DIP switch 1 (the leftmost DIP switch) in the closed (down) position. Place DIP switch 2 in the open (up) position. Leave all other DIP switches in their original positions.
3. Power on the terminal. Power on the system unit, wait for the prompt BOOT?>, and then insert the INSTALL floppy disk.

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4. In response to the BOOT?> prompt, type **f:/install** and press the Return key. The following menu is displayed:

```
Press "i" to install Base System Software, Optional
 System Software, or Application Software.
Press "r" to remove Optional System Software or
 Application Software.
Press "v" to verify currently installed software.

Selection:
```

5. Type **i** to start the system software installation procedure. The following menu will appear immediately:

```
File System Installation Procedure:
When the BOOT?> prompt appears, type /install to continue
with the installation process, or type /config to adjust the
LAN, or Operating mode parameters or save an image of the
current system software.
```

If you need to adjust the network parameters, type /config and refer to the *Configuration Utility* on page 6–86. Otherwise, continue with the next step.

***NOTE**. Do NOT remove the INSTALL disk yet. The program transfers several files from the floppy disk to the hard disk. The BOOT?> prompt will appear.*

6. Type **/install** in response to the BOOT?> prompt and press the Return key. The system will access the hard disk and after a few seconds will display the following message:

```
File System Installation Procedure:
XXXXX Kbytes disk space remaining.
Insert next DAS system floppy disk and press Return.
(When installation is complete press "c") -->
```


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7. Remove the INSTALL disk, insert the OPERATING SYSTEM disk, and press the Return key. When the prompt returns, insert the next disk in the sequence and press the Return key. Continue loading Base System Software disks in sequence until you have installed all of them.

8. After you have installed all the Base System Software disks, install the optional system software disks that you require for your application.

9. When you have installed all the optional system software disks, you can install any other application Software disks. However, you can wait and install the application software disks using the Disk Services menu.

10. After you have installed the last disk, type c to complete the software installation procedure; the system will then power off.

11. After the logic analyzer has completed the power-off sequence, place DIP switch #1 in the open (up) position and power on the system unit.

Installing Optional System Software. Use this part of the File System Install utility to add or replace Tektronix supplied files only. The program will not disturb user generated files (such as, reference memories and system setups).

If the BOOT?> prompt is already displayed, proceed to step 4. If not displayed, begin with step 1.

1. Power off the logic analyzer. Face the rear of the system unit and locate the DIP switches mounted on the Controller board (refer to Figure 6–29).

2. Place DIP switch 1 (the leftmost DIP switch) in the closed (down) position. Place DIP switch 2 in the open (up) position. Leave all other DIP switches in their original positions.

3. Power on the terminal. Power on the system unit, wait for the prompt BOOT?>, and then insert the INSTALL floppy disk.

4. In response to the BOOT?> prompt, type /install and press the Return key. The following menu is displayed:

```
File System Installation Procedure:

Insert next DAS system floppy disk and press Return.
(When rebuild is complete press "c") -->
```

5. When the prompt appears, insert the first optional system software disk that you require for your application. Continue installing the disks at each prompt until you have installed all required disks.

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6. After you have installed the last disk, type c to complete the software installation procedure; the logic analyzer will then power off.

7. Place DIP switch #1 in the open (up) position and power on the system unit.

Installing Application Software. You can install application software using the same procedure given for installing optional system software. However, it may be easier to install the application software disks using the Disk Services menu.

Removing Optional System Software or Application Software. You can remove the optional system software and application software using the Install utility on disk. Removing software in this manner provides additional free space on the hard disk drive. You can also remove application software using the Disk Services Menu (but not the optional system software).

If the BOOT?> prompt is already displayed, proceed to step 4. If not displayed, begin with step 1.

1. Power off the logic analyzer. Face the rear of the system unit and locate the DIP switches mounted on the Controller board (refer to Figure 6–29).

2. Place DIP switch 1 (the leftmost DIP switch) in the closed (down) position. Place DIP switch 2 in the open (up) position. Leave all other DIP switches in their original positions.

3. Power on the terminal. Power on the system unit, wait for the prompt BOOT?>, and then insert the INSTALL floppy disk.

4. In response to the BOOT?> prompt, type f:/install and press the Return key. The following menu is displayed:

```
Press "i" to install Base System Software, Optional
 System Software, or Application Software.
Press "r" to remove Optional System Software or
 Application Software.
Press "v" to verify currently installed software.

Selection:
```


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5. Type r to start the system software installation procedure. A menu similar to the following will appear immediately:

```
DAS Software Removal Procedure:
XXXXX Kbytes space remaining.
The following Optional System Software and/or Application Software
is currently installed

1) .92C96
2) .92S16

To remove a software package, type in the number on the same line
as the name of the package and press Return. To exit, type in "0"
and press Return, or simply press Return with no number specified.

Which Optional System Software or Application Software package
would you like to remove.
```

After you enter your selection, the Install procedure removes the selected package and displays the remaining list of software packages. The You are prompted you for another selection.

If there are no optional system software or application software packages, the procedure displays an appropriate message and then displays the BOOT?> prompt.

Use the verify function of the Install utility to verify that all Tektronix supplied software for the logic analyzer, including the Base System Software, the optional system software, and the application software, is completely and correctly installed and has not been corrupted.

Verifying Base, Optional, and Application Software. Use the verify function of the Install utility after executing the file system Check procedure of the Make utility. Each base, optional, and application software package is individually verified as you install it. Therefore, it is not necessary to use the verify function of the Install utility after installing software.

You can also verify all Tektronix supplied software through the Version menu.

If the BOOT?> prompt is already displayed, proceed to step 4. If not displayed, begin with step 1.

1. Power off the logic analyzer. Face the rear of the system unit and locate the DIP switches mounted on the Controller board (refer to Figure 6–29).
2. Place DIP switch 1 (the leftmost DIP switch) in the closed (down) position. Place DIP switch 2 in the open (up) position. Leave all other DIP switches in their original positions.

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3. Power on the terminal. Power on the system unit, wait for the prompt BOOT?>, and then insert the INSTALL floppy disk.

4. In response to the BOOT?> prompt, type f:/install and press the Return key. The following menu is displayed:

```
Press "i" to install Base System Software, Optional
 System Software, or Application Software.
Press "r" to remove Optional System Software or
 Application Software.
Press "v" to verify currently installed software.
Selection:
```

5. Type v to start the software verification procedure.

Each Base System Software, optional system software, and application software disk have a separate checksum list corresponding to the name of the floppy disk containing the files. Each list contains the name and the expected checksum value for each file on the associated disk. The verification program displays the name of each checksum list as it verifies the checksums for the files. This process takes several minutes to complete.

If any files in a checksum list do not exist, or do not match the expected checksum, an error message displays the name of the disk and the faulty file. After the checksums for all disks have been tested, one of two messages will be printed. If no failures are found, the program displays:

```
Verify Procedure Complete, NO ERRORS.
```

However, if one or more failures occur, the program displays:

```
Verify Procedure Complete, ERRORS OCCURRED
```

In this case, identify the disks where the errors occurred, reinstall the disks, and repeat the verify procedure.

Configuration Utility

Use the Configuration utility to check or set the various parameters for operating the logic analyzer. In most cases, you will use this tool to check or set the network addresses used to enable communications between the instrument and the host or X terminal. Use the utility to set the operating mode and save, restore, or delete system software images. You can also use the utility to check the results of the power-on diagnostics.

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The utility loads onto the hard disk when you initially install the system software. To start the utility, power on the instrument with DIP switch #1 in the down position and type **/config** at the BOOT?> prompt.

User Interface

The Configuration utility is mainly intended for use with network systems or with systems with X terminals. However, a console terminal is required to display status or error messages while using the utility. You can also use the Serial window of an X terminal for this purpose if you do not have an external console terminal.

The utility does not make use of any special characteristics of any terminal. The utility assumes that the terminal can display 80 characters per line and at least 24 lines per screen. No special character positioning or highlighting is used.

The Configuration utility is required under the following conditions:

- When you change networking parameters
- When you change the operating mode
- When you need to update the X terminal's Flash ROM
- When you need to check the results of the power-on diagnostics and configuration (if the instrument's menus do not display)

The basic utility consists of a main menu and several submenus. Each menu has a list of selections to choose from and lists the current values of the parameters. A Help selection is also available for each menu item.

Main Menu

The Main menu displays as soon as you start the utility. Figure 6–31 shows an example of the main menu. To select an item in the main menu, enter the character enclosed in parenthesis following the line number of the item you are interested in, and press the Return key. You can also enter the line number, and press the Return key. For example, to view the diagnostic results, enter a "1" or "c" and press the Return key.

Values of previously defined parameters will appear in the menu. Undefined parameters will be blank.

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```
Configuration Utility:

 1. (C) Display Hardware [C]onfiguration and Diagnostic Results.
 2. (S) [S]ave image of current system software. Available: 9202XT
 3. (R) [R]estore saved image of system software. Available: None
 4. (D) [D]elete saved image of system software.
 5. (T) Show Fac(t)ory Default Network Configuration.
 6. (O) Set [O]perating Mode.                      Current: 9202XT
 7. (N) Set DAS Network [N]ame.                    Current: alpha
 8. (A) Set DAS Internet [A]ddress.                Current: 123.123.125.2
 9. (M) Set Network Subnet [M]ask.                 Current: 255.255.255.0
10. (G) Set [G]ateway Internet Address.            Current: 123.123.125.14
11. (F) Set De[f]ault X-server Name.               Current: eldar:0.0
12. (X) Set Default [X]-server Internet Address.   Current: 123.21.1.0
13. (L) Set [L]ANPCL Port Number.                  Current: 10999
14. (P) Set GPIB [P]ort Number.                    Current: 2
15. (E) Save changes and [E]xit to BOOT? prompt.
16. (U) [U]pdate 9202XT Flash ROM and Exit to BOOT? prompt.
17. (Q) Discard changes and [Q]uit to BOOT? prompt.
18. (H) [H]elp.

Please make a selection:
```

Figure 6–31: Configuration Utility, Main Menu

Display Hardware Configuration and Diagnostic Results. The Configuration utility allows you to check the results of the power-on diagnostics for each module installed in the instrument. It also lets you view the contents of each slot and the configurations of the modules in the instrument. The configuration and diagnostic information are listed when you select item C in the main menu.

Figure 6–32 shows an example of the configuration display listing. The listing looks similar to the Diagnostic menu. For each installed card or module, the diagnostic results are displayed. If a diagnostic failure exists, the resulting error code displays. The diagnostic results are those that were recorded as of the last normal system power-on. A value of No S/W indicates that the corresponding hardware could not be tested because the Optional System Software for that hardware was not installed.

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```
                              CURRENT CONFIGURATION

System Software Release 3 Version 1.40
Previous Shutdown: Normal

Slot                              Card                              Diagnostic
  0     Controller/92LANSE Network Controller                          PASS
  1                                                                    ----
  2     92S16       18 Channels/20ns Pattern Generation                PASS
  3     92A96XD     96 Channels/10 ns Acquisition, 128K Deep           PASS
```

Figure 6–32: Configuration Utility, Hardware Configuration and Diagnostic Results

Save Image of Current System Software. Selecting item S from the main menu lets you save a non-executable image of the current system software in a different location on the hard disk. This is useful when you plan to change the operating mode of the system. You can save an image of the system software for the current mode of operation before installing new software. If you later decide to return to the original mode of operation, you can restore the previously saved image from the hard disk. If you plan to switch modes often, you can alternate between saved images rather than reloading software from the floppy disks.

You must have an image saved on the hard disk before you attempt to restore an image; if not, the current image will be lost. Once you save an image, you cannot use the image. You have to restore an image before you can use it.

User-created files, such as saved setups, reference memories, and trigger libraries remain in place when you save or restore an image. The files do not become part of the saved image and are not replaced when you restore an image. This means that when you convert a system from one mode of operation to another by saving then restoring or installing new system software, existing user files that were present in the original mode will still be present in the new mode. It is not necessary to save the user files separately when switching modes, (although doing a backup before such a major change is always a good idea). Likewise, saving a system software image does not make a copy of the user files and is not a substitute for a backup.

Be aware that saving an image of the current system software causes the software to be removed. Therefore, you must install new software following a Save operation before returning to normal operation. You can install new software either from the floppy disks or by restoring a previously saved image.

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Saved images of system software vary in size according to the amount of optional system software and application software installed. The minimum size is approximately 14 Mbytes. If there is insufficient room on the hard disk to save the complete image, the save operation will abort, leaving the current system software intact. Saving an image takes approximately three minutes.

The Available: field at the right end of the save entry in the Main menu shows the type of system software that is currently installed and available for saving, if any. The value None signifies that the system software has not been installed or has been removed as the result of either a save or operating mode change.

You will be prompted to verify your actions before the save operation occurs. If the save operation cannot be carried out, you will be returned to the Main menu.

Restore Image of Saved System Software. Selecting item R from the Main menu lets you restore a previously saved image of system software. This is useful when you plan to change the operating mode of the system. You can save an image of the system software supporting the current mode of operation before installing new software. If you later decide to return to the original mode of operation, all that is necessary is to restore the image from the hard disk. If you will be switching modes often, you can alternate between saved images rather than reload software from the floppy disks.

NOTE. *You must have an image saved on the hard disk before you attempt to restore an image; if not, the current image will be lost.*

User-created files, such as saved setups, reference memories, and trigger libraries remain in place when you save or restore an image. The files do not become part of the saved image and are not replaced when you restore an image. This means that when you convert a system from one mode of operation to another by saving then restoring or installing new system software, existing user files that were present in the original mode will still be present in the new mode. It is not necessary to save the user files separately when switching modes, (although doing a backup before such a major change is always a good idea). Likewise, saving a system software image does not make a copy of the user files and is not a substitute for a backup.

Be aware that a saved image of system software can only be restored once. After it is restored, the saved image no longer exists. Therefore, if you alternate between different versions of system software, you must resave the current system software before each restore operation. Restoring an image takes about two minutes.

The Available: field at the right of the Restore entry in the Main menu shows the type of system software that is currently saved and available to restore, if any. The value None signifies that there are no saved images present on the hard disk.

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You will be prompted to verify your actions before the restore operation occurs. If the restore operation cannot be carried out, you will be returned to the Main menu.

Delete Saved Image of System Software. Selecting item D deletes saved images of the system software that you no longer need. The Available: field at the right of the Restore entry in the Main menu shows which saved images are present on the hard disk. Each image occupies approximately 14 Mbytes of hard disk space.

You will be prompted to verify your actions before the delete operation occurs. If the delete operation cannot be carried out, you will be returned to the Main menu.

Show Factory Default Network Configuration. Selecting item T lets you see or change the factory default network configuration in a single step. The proper network settings guarantee the proper configuration for stand alone operation when no other network devices are attached to the network cable that connects the instrument and the terminal.

A menu similar to Figure 6–33 will be displayed. Items in the Current column are the current settings shown in the Main menu. Items listed in the Factory column show the settings that allow the instrument to operate in the stand alone mode.

If you want to use the default factory settings, enter Yes or Y at the prompt. The utility will load the default settings. If you do not want to use the default settings, enter No or N at the prompt, and you will be returned to the main menu.

```
                Factory Default network configuration:

NETWORK OPTIONS               Current           Factory
---------------               -------           -------
DAS Network Name.             das1              Tek_La
DAS Internet Address.         123.123.125.2     10.0.0.1
Network Subnet Mask.          255.255.255.0     255.0.0.0
Gateway Internet Address.     123.123.123.14    0.0.0.0
X Server Name.                eldar:0.0         TEK_DISPLAY:0.0
X Server Internet Address.    123.21.1.0        10.0.0.2

Do you want to use the Factory settings? Yes/[No]:
```

Figure 6–33: Configuration Utility: Factory Default Network Configuration

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Set Operating Mode. Select item O to set the operating (start-up) mode for the system software.

There are different operating modes: 9202XT mode, 92XTerm Manual mode, and 92XTerm Automatic mode. The available operating modes depend on the system software. As the names imply, the 9202XT mode is for the stand-alone X terminal, while the two 92XTerm modes are for work station X server displays. (92XTerm auto start can also be used with the stand-alone X Terminal)

Table 6–20 lists the software versions and the operating modes they support.

Table 6–20: System Software vs Operating Modes

Operating Mode	TLA System Software	DAS/NT System Software
9202XT*	X	X
92XTerm Manual		X
92XTerm Autostart		X

*** Use for X Terminals.**

Enter an X for the 9202XT operating mode, an M to select the 92XTerm Manual operating mode, or an A to enter the 92XTerm Autostart operating mode. To retain the current operating mode, press the Return key without entering any characters.

Set DAS Network Name. Selecting item N from the Main menu lets you set the system (network) name for your system. Some applications refer to network devices by a name. The Internet address and name of the system must be entered in the appropriate tables on your host so that the system name of the system can be converted to the correct Internet address. The name can be up to eight alphanumeric characters long.

To set or change the name, enter a new name, and press the Return key. To retain the current name, press the Return key without entering any other characters. You will be returned to the Main menu.

Set DAS Internet Address. Selecting item A from the Main menu lets you set the Internet address for your system. The Internet address is the IEEE802 network address for your system (the Internet address is not the same thing as the Ethernet address-which is set at the factory). This Internet address must be set to an address other than 0.0.0.0 to permit communication between the DAS system and other network devices. The Internet address is normally assigned by your system administrator.

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Enter the new value in the format XXX.XXX.XXX.XXX (where each XXX represents a decimal number in the range of 0 to 255), and press the Return key. To retain the current address, press the Return key without entering any numbers.

Set Network Subnet Mask. Selecting item M from the Main menu lets you set the subnet mask for your system. The subnet mask specifies the portion of an Internet address that is common to all node addresses on a particular subnet. The subnet mask determines which other network devices the instrument may address directly and which ones it must access through a gateway. A value of 0.0.0.0 turns off subnet support. The subnet mask is normally assigned by your system administrator.

Enter the new value in the format XXX.XXX.XXX.XXX (where each XXX represents a decimal number in the range of 0 to 255), and press the Return key. To retain the current value, press the Return key without entering any numbers.

Set Gateway Internet Address. Selecting item G from the Main menu lets you set the gateway Internet address. This is the IEEE802 gateway address for the local network. The value must be set to an address other than 0.0.0.0 to permit communication between the instrument and other devices not on the same subnet. This number is normally assigned by your system administrator.

Enter the new value in the format XXX.XXX.XXX.XXX (where each XXX represents a decimal number in the range of 0 to 255), and press the Return key. To retain the current value, press the Return key without entering any numbers.

Set Default X Server Name. Selecting item F from the Main menu lets you specify the system name of the X server that will display the window in the 9202XT or 92XTerm Autostart operating mode. In this mode, the instrument automatically initiates an X window display on the Default X Server when the instrument is powered on. Most X servers have only one display and one screen, so server_name:0.0 is the most common entry.

Enter the new value in the format server_name:d.s, where server_name is the system name of the X server device, d is the single digit number of the display on that device, and s is the single digit number of the screen on that display. The display number is required; however, the screen value will default to .0 if not specified. To retain the current name, press the Return key without entering any numbers.

This name is only for informational purposes, unless the default X server address parameter is set to Use Name. In this case, there must be an entry in the instrument's /etc/hosts table that associates this name with an X server address.

If the operating mode is set to something other than 9202XT or 92XTerm Autostart, this parameter has no affect. Your system administrator should provide you with the correct name for your default X server.

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Set Default X Server Address. Selecting item X from the Main menu lets you specify the default X server address. The default X server address specifies the Internet address of the X server that displays the window in the 9202XT or 92XTerm Autostart operating modes. In this mode, the instrument automatically initiates an X window display on the default X server when the instrument is powered on. If this parameter is set to the special value of Use Name, then the default X server name is used instead of the address. In this case, the default X server name and address must be entered in the instrument's /etc/hosts file.

If the operating mode is set to something other than 92XTerm Autostart or 9202XT, this parameter has no affect. Your system administrator should provide you with the correct Internet address for your default X Server.

Enter the new value in the format XXX.XXX.XXX.XXX (where each XXX represents a decimal number in the range of 0 to 255), or enter –1 to select the Use Name option, and press the Return key. To retain the current address, press the Return key without entering any numbers.

Set LANPCL Port Number. Selecting item L from the Main menu lets you set the service number assigned to the DAS LAN PCL (LANP) service. This number is used by host software requesting LAN PCL services from the instrument. The legal range of values for the entry is 1025 to 65535. Host software provided by Tektronix assumes that this service is assigned the value 10999. If you specify a different value, you must also change the host-based software.

Enter a new value in the range of 1025 to 65535, or press the Return key without entering number to retain the current value.

Set GPIB Port Number. The TLA 510 and 520 Logic Analyzers do not use GPIB; this selection has no effect.

Update Terminal Flash ROM. If you have a Tektronix X terminal, you can use the Configuration utility to update the terminals internal Flash ROM. Updating the Flash ROM is only necessary when the terminal's software or fonts require updating with a new version. You may also need to update the Flash ROM as a result of any service work done to the terminal. If you desire to update the Flash ROM, you first must set the network configuration parameters for the instrument using the Configuration utility.

NOTE. *You do not need to update the Flash ROM in the terminal to change the Internet address. Use the other selections in the Configuration Utility Main menu to update the internet information for the instrument. Update the terminal internet information in the Boot Monitor. Internet addresses and other networking parameters are normally assigned by your system administrator.*

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After setting the parameters, select item U to begin the Flash ROM update process. You are asked to confirm your actions before starting the operation. Enter y to confirm your actions.

A series of messages is displayed. When the operation is ready to load the X terminal software, information appears on the screen. Follow the steps listed below and the displayed instructions to update the Flash ROM. The following steps assume that you have a 9204XT terminal; the procedure is similar for other TekXpress X terminals.

Read the entire Flash ROM procedure on the terminal screen before continuing. To return to the start of the procedure on the screen, press the Return key.

1. Information about Step 1 of the Flash ROM procedure is displayed. Read the information carefully before proceeding.

2. The configuration parameters that you specified for the instrument are displayed on the terminal. Write these parameters down; you need to enter the parameters in the Boot Monitor (the parameters are not visible after you reset the terminal). Do not continue with the instructions on the terminal screen until you have completed steps 3 through 14 of the following instructions.

   The boot path information is case sensitive (upper or lower case). Be sure to copy the boot path exactly as displayed. The terminal will not boot properly if the boot path is wrong.

3. Reset the terminal by pressing the Control, Alt, and Delete keys simultaneously. When the Boot Monitor appears on the screen, press the space bar to stop the boot process. This prevents the terminal from completing the boot process before the parameters are set.

NOTE. *Some NVRAM parameters cannot be set at the Boot Monitor. If you experience problems with the Flash procedure, try restoring the terminals factory settings by issuing the NVFACTORY command and then returning to this procedure.*

---

4. Enter the Internet address for the terminal. For example:

   ```
   IADDR 123.21.1.0
   ```

5. Enter the Internet address for the instrument. For example:

   ```
   IHOST 123.123.125.2
   ```

6. Enter the Network Subnet Mask. For example:

   ```
   IMASK 255.255.255.0
   ```


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7. Enter the Gateway Internet address (if required). For example:

   ```
   IGATE 123.123.125.14
   ```

8. Enter the boot path name of the boot file. For example:

   ```
   BPATH /XP300/os
   ```

9. Enter the boot method parameter that the X terminal will use after the Flash ROM update is complete by typing:

   ```
   BMETHOD ROM
   ```

10. Save the entries in the terminal's nonvolatile memory by typing:

    ```
    NVSAVE
    ```

11. Enter the BOOT command to use for the Flash ROM update process by typing:

    ```
    BOOT TFTP
    ```

NOTE. *Do not continue with the following steps until the terminal has rebooted. The boot process is complete when the Serial window appears (the word "Connected" is displayed in the window).*

---

12. After the Serial window appears, press the Return key. Disregard the following messages that appear on the screen, and continue to step 13.

    ```
    Answering NO to this question will return you to STEP 1.

    Terminate the Flash procedure and return to the DAS boot
    prompt? Yes/[No].
    ```

13. Press the Return key until the following text appears:

    ```
    Are you ready to continue to STEP #2?
    ```

14. Enter y in response to the prompt. The text for Step 2 will appear on the screen.

    When you start the Flash Update process, the X terminal will write the parameters to the Flash ROM. The process will take approximately 10 minutes. When the terminal boots, the Flash ROM monitor displays the following message: FLASH UPDATE IN PROGRESS. If the message does not appear, the Flash Update process failed. Follow the suggestions displayed on the screen to identify any problems.

15. When you are ready to start the Flash Update process, enter y in response to the prompt on the screen. Verify that the Flash Update in Progress message is displayed.

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CAUTION. *Disturbing the terminal or the instrument can cause the Flash ROM Update process to fail. Do not move the terminal or the mainframe or press any keys unless instructed to do so. If the screen blanks out or goes dark, you can move the mouse or press one of the Shift keys to reactivate the display without disturbing the update process.*

16. If the Flash Operation Completed message is displayed, enter y in response to the next prompt on the screen. The text to Step 3 of the Flash Update procedure is displayed; carefully read this information. Entering n at the prompt returns you to Step 1 of the Flash Update procedure to restart the entire process.
17. Press the Control, Alt, and Delete keys simultaneously to reset (boot) the terminal from the Flash ROM. Verify that the Serial window appears after the boot process is complete.
18. If the Serial window does not appear, restart the Flash Update procedure again from the Configuration Utility Main menu.
19. If the Serial window appears, boot the instrument normally, and verify that the window displays on the terminal.

Typing the final command will exit the Configuration utility and you will be returned to the BOOT?> prompt.

Leaving the Utility

There are two ways to leave the Configuration utility: by saving the changes, or by discarding the changes. Either way, you will be returned to the BOOT?> prompt.

Select item E to save any changes and exit to the BOOT?> prompt. This is the normal way to leave the utility. All changes are saved and in affect when the instrument returns to normal operation.

Select item Q to discard the parameter modifications (except the operating mode changes). Major operating mode changes remain in effect. System changes resulting from the save, restore, or delete options also remain. If you performed the restore operation, you should use the Exit option to save the current parameter values in place of the values that were part of the restored image.

After quitting the Configuration utility, you will return to the BOOT?> prompt, from which you can enter /install to install new software, or reset the DIP switch, restart the instrument, and return to normal operation.

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Optional System Software

Optional system software disks contain parts of the system software that are not required for all operations. This software is optional so that you can free up additional space on your hard disk by installing or retaining software that is required for your logic analyzer. Each optional software disk label tells the approximate size consumed by the software to help you decide which optional software to install. Note that it is possible for this number to be larger than the capacity of the floppy disks.

Base System Software and all optional system software are already installed on all instruments shipped from the factory. You can remove unnecessary optional system software or application software by using the remove option of the Install utility. You can install or exclude optional system software and application software at your discretion when you upgrade your logic analyzer to new software versions. Be sure to remove any optional system software that you do not intend to replace with a newer version when you upgrade the Operating System Software version; if you are unsure, run the Verify function to be sure that all the software on the hard disk is the current version.

There are different optional software packages for the logic analyzer. Two of these relate directly to the instrument module families presently available. The optional software packages are briefly described below:

- 92C96 Support. This package provides the necessary software to operate the 92C96 Data Acquisition Modules.
- 92S16/32 Support. This package provides the necessary software to operate the pattern generation modules. You can remove or exclude this software if your logic analyzer does not contain pattern generation modules.
- Remote Operation Support. This package provides the necessary software to operate the instrument remotely using the Programmatic Command Language (PCL). You can remove or exclude this software in instruments that you will not operate remotely with 92LANP.
- 9204XT Support, XP100 and XP200 Supplement. This package provides the necessary software to update the terminal Flash ROM. It also provides additional software to service the terminal.

Application Software

Application software disks contain special purpose software that provides additional capability not present in the Base System Software or optional system software. Application software (available as separate products) includes microprocessor support and device verification packages.

You can install or remove application software using the Disk Services menu. However, for convenience, you can install or remove the application software using the Install utility when you install the Base System Software or optional system software.

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Options

This chapter lists the options you may find when performing service on the TLA 510 or 520 Logic Analyzers.

Table 7–1 list the options available for the TLA 510 and TLA 520.

Table 7–1: TLA 510 & TLA 520 Options

Option	Description
Option 01	Increase memory depth to 32K
Option 02	Increase memory depth to 128K
Option 03	Increase memory depth to 512K
Option 04	Software Performance Analysis Tool
Option 06	Increase memory depth to 2M
Option 30 (TLA 510 Only)	92S16 Pattern Generator with two P6463A Probes and accessories
Option 1D (TLA 520 Only)	Delete 48 acquisition probes, 2 clock probes, cables and accessories
Option 1X	Subsitute 92XTERM Networked System Software
Option 4X	Subsitute 17-inch terminal for 15-inch terminal
Option 1P	Add six 8-channel lead sets, 72 KlipChips, 12 1-channel lead sets
Option 5C	Thicknet (AUI)
Option 8S	Replace standard 92A96 or 92C96 ribbon cables with high-performance coaxial cables

Table 7–2 lists the Field Kit Options for the TLA 510 and TLA 520.

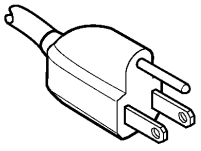
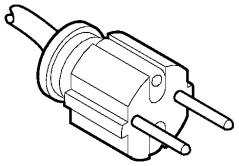
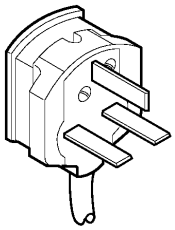
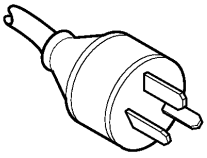
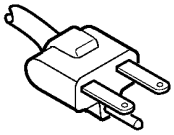
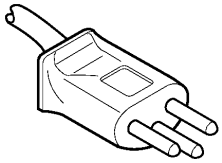
Table 7–2: Field Kit Options

Field Kit	Description
LAF01	Upgrade 92C96 (8K) to 92C96D (32K), includes installation
LAFO2	Upgrade 92C96 (8K) to 92C96XD (128K), includes installation
LAFO3	Upgrade 92C96 (8K) to 92C96SD (512K), includes installation
LAFO4	Upgrade 92C96D (32K) to 92C96XD (128K), includes installation
LAFO5	Upgrade 92C96D (32K) to 92C96SD (512K), includes installation
LAFO6	Upgrade 92C96XD (128K) to 92C96SD (512K), includes installation

Table 7–3 shows the power cord options available for the TLA 510 and 520.

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Table 7–3: Power Cord Options

Plug Configuration	Normal Usage	Option Number	Part Number
	North America 115 V	Standard	161-0066-00
	Europe 230 V	A1	161-0066-09
	United Kingdom 230 V	A2	161-0066-10
	Australia 230 V	A3	161-0066-11
	North America 230 V	A4	161-0066-12
	Switzerland 230 V	A5	161-0154-00

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Replaceable Electrical Parts

This section contains a list of the replaceable modules for the TLA 510 & 520. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Module Replacement

The TLA 510 & 520 is serviced by module exchange or replacement, so there are two options you should consider:

Module Exchange. In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEKWIDE.

New Modules. You may purchase new replacement modules in the same way as other replacement parts.

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Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the TLA 510 & 520. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts List Column Descriptions

Column	Column Name	Description
1	Figure & Index Number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
3 and 4	Serial Number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & Description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. Code	This indicates the code of the actual manufacturer of the part.
8	Mfr. Part Number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

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Manufacturers Cross Index

Mfr. Code	Manufacturer	Address	City, State, Zip Code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001
71400	BUSSMAN DIVISION OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 11460	ST LOUIS MO 63178
TK0946	SAN–O INDUSTRIAL CORP	70 WILBUR PL	BAHEMIA LONG ISLAND NY 11716

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Replaceable Electrical Parts List

Component Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Name & Description	Mfr. Code	Mfr. Part Number
				CIRCUIT BOARD ASSEMBLIES		
A01	671–3165–00			CIRCUIT BD ASSY:BACKPLANE;TLA510 & TLA520	80009	671–2452–01
A01F580	159–0059–00			FUSE,WIRE LEAD 5A,125V	71400	MCR–571400
A01F585	159–0059–00			FUSE,WIRE LEAD 5A,125V	71400	MCR–571400
A01F600	159–0029–00			FUSE,CARTRIDBE 3AG,0.3A,250V,20SEC	71400	MDL 3/10
A01F785	159–0059–00			FUSE,WIRE LEAD 5A,125V	71400	MCR–571400
A70	671–2324–08			CIRCUIT BD ASSY:DAS/TLA CONTROLLER	80009	671–2324–08
A71	671–2452–02			CIRCUIT BD ASSY:LAN IO ADAPTER	80009	671–2452–02
A71F120	159–0153–00			FUSE,WIRE LEAD:1.5A,125V,FAST BLOW,	TK0946	SP5–1.5A DI
A71F170	159–0235–00			FUSE,WIRE LEAD:0.75A,125V,FAST	71400	TR/MCR 3/4
A71F640	159–0153–00			FUSE,WIRE LEAD:1.5A,125V,FAST BLOW,	TK09466	SP5–1.5A DI
A71U810	160–5647–01			IC,DIGITAL:STTL,PROM;32 X 8,3 STATE OUT,PRGM, 74S288, DIP16,CER (92LANSE ONLY)	80009	160564701
A32	671–3254–00			CKT BD ASSY 8K POWERFLEX ACQUISITION MODULE (STANDARD)	80009	671–3254–00
A32F116	159–0116–00			FUSE,CARTRIDGE 1A,125V,0.4SEC0.17	TK0946	SM4–1A
A32F117	159–0116–00			FUSE,CARTRIDGE 1A,125V,0.4SEC0.17	TK0946	SM4–1A
	119–4760–00			POWER SUPPLY:90–250 VAC LINE, 47–64HZ,OUTPUTS, 5.15V,2 VA 13A,+/–15V AT 3AMPS,PPOWER FAIL,DC OK, REMOTE ON/OFF		
				OPTIONAL CIRCUIT BOARDS		
A30	671–1793–00			CIRCUIT BD ASSY:P6463A BUFFER/DRIVER, (P6463A ONLY)	80009	671179300
A31	671–0273–02			CIRCUIT BD ASSY:ID/LOGIC (P6463A ONLY)	80009	671027302
A32	671–3255–00			CKT BD ASSY 32K POWERFLEX ACQUISITION MODULE (OPTION 01)	80009	671–3255–00
A32	671–3256–00			CKT BD ASSY 128K POWERFLEX ACQUISITION MODULE (OPTION 02)	80009	671–3256–00
A32	671–3257–00			CKT BD ASSY 512K POWERFLEX ACQUISITION MODULE (OPTION 03)	80009	671–3257–00
A33	671–3463–00			CKT BD ASSY 100 CH, 2M DEEP ACQUISITION MODULE (OPTION 06)	80009	671–3463–00
A33F116	159–0116–00			FUSE,CARTRIDGE 1A,125V,0.4SEC0.17	TK0946	SM4–1A
A33F117	159–0116–00			FUSE,CARTRIDGE 1A,125V,0.4SEC0.17	TK0946	SM4–1A
A33F118	159–0116–00			FUSE,CARTRIDGE 1A,125V,0.4SEC0.17	TK0946	SM4–1A
A40	670–9593–52			CIRCUIT BD ASSY:PATTERN GENERATOR MDL (OPTION 30 TLA510 ONLY)	80009	670–9593–52

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Replaceable Electrical Parts List (Cont.)

Component Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Name & Description	Mfr. Code	Mfr. Part Number
				9204XT		
	119–4273–01			COLOR MONITOR:TECO 15 INCH 1024 X 768 COLOR W/NEW PANEL	80009	ORDER BY DESC
	119–4254–01			KEYBOARD, ASSY:IBM101,NORTH AMERICAN;ACCOMP XP PRODUCTS, BASE NUMBER (9204XT)	80009	ORDER BY DESC
	156–4382–00			IC,MEMORY:CMOS,DRAM;IMEG X 32,70NS,MODULE,WITH WORD WIDE MONOLITHIC DEVICES 421100A32,SIMM72	0JR04	THM321000AS–70
A1	671–2996–00			CIRCUIT BD ASSY:LUNAR TECO COLOR;MAIN LOGIC	80009	ORDER BY DESC
A2	671–2977–00	B010100	B059999	CIRCUIT BD ASSY:2 MB FLASH BD	80009	ORDER BY DESC
A2	671–3255–00	B060100		CIRCUIT BD ASSY:2MB FLASH BOARD	80009	ORDER BY DESC
		(FOR MORE COMPLETE INFORMATION, REFER TO 070–8860–98)				
				9205XT		
	119–4625–00			17 INCH COLOR MONITOR DIGITAL CONTROLLER MULTI–SCAN TYPE (9205XT)	80009	ORDER BY DESC
	156–4382–00			IC,MEMORY:CMOS,DRAM;IMEG X 32,70NS,MODULE,WITH WORD WIDE MONOLITHIC DEVICES 421100A32,SIMM72	0JR04	THM321000AS–70
	119–5030–02			POWER SUPPLY:40W;5V 4A,12V 1A,45 MIL SQ PIN;90–265 VAC,47 TP 63 HZ, 45 MIL SQ PIN;3 X 5 X 1.45, UL CSA TUV	80009	ORDER BY DESC
A1	671–2998–00			CIRCUIT BD ASSY:LUNAR MODULAR COLOR;MAIN LOGIC	80009	ORDER BY DESC
A2	671–2977–00	B010100	B059999	CIRCUIT BD ASSY:2 MB FLASH BD	80009	ORDER BY DESC
A2	671–3255–00	B060100		CIRCUIT BD ASSY:2MB FLASH BOARD	80009	ORDER BY DESC
		(FOR MORE COMPLETE INFORMATION, REFER TO 070–8860–98)				
				9206XT & 9206XT OPTION 4X		
	119–5434–00			MONITOR, 15 INCH, .28 DOT PITCH	80009	119543400
	119–4847–00	B010155		MONITOR:17 INCH COLOR,MULTISCAN TYPE	80009	119484700
	671–3311–01			CRT BD ASSY:MAIN LOGICCOLOR	80009	ORDER BY DESC
	671–3225–00			CIRCUIT BD ASSY:NEW FLASH ROM XP35X,OPT 1A	80009	ORDER BY DESC
	156–4382–00			IC,MEMORY:CMOS,DRAM;1 MEG X 32,7ONS,MODULE, WITH WORD WIDE MONOLITHIC DEVICES 421000A32,SIMM72	80009	ORDER BY DESC

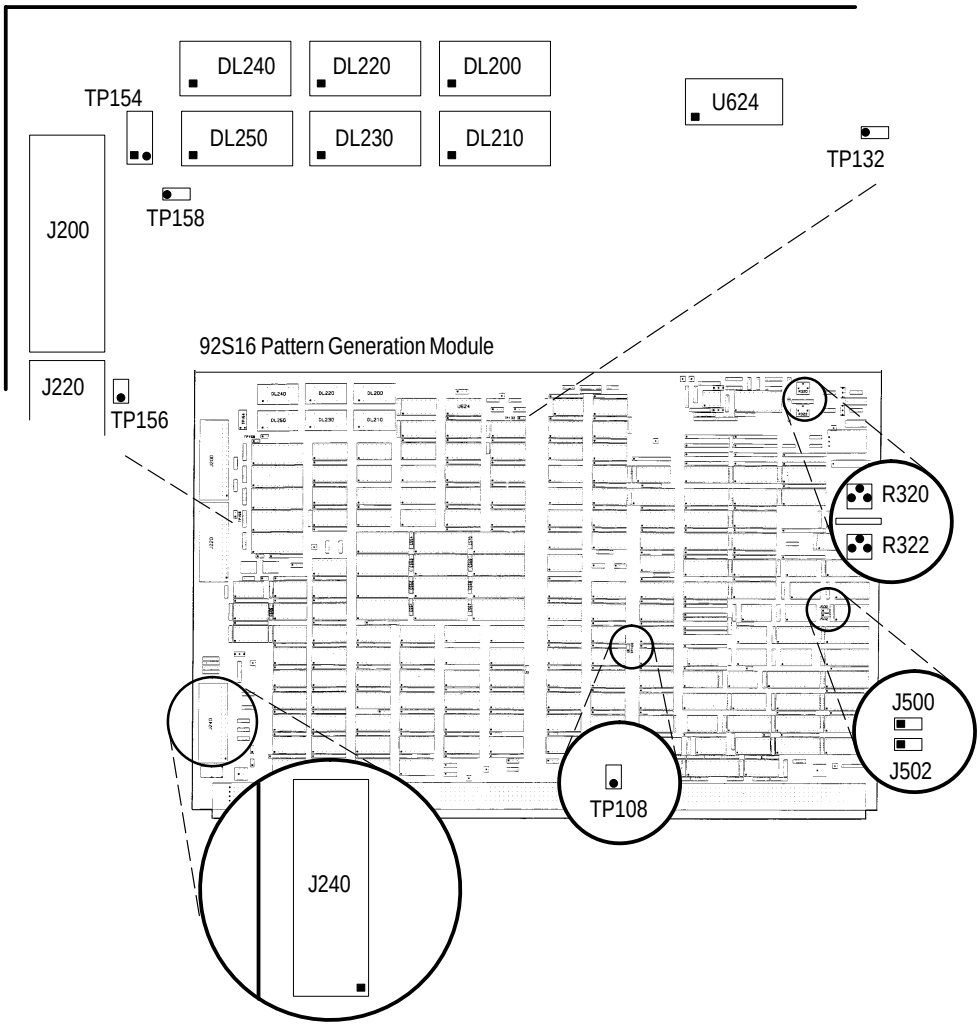
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Diagrams

This section contains the circuit board illustration for the 92S16 Pattern Generation Module. Use this illustration to find components or test points that the *Adjustment Procedures* refer to.

For adjustment locations on the 92A96 Modules, refer to Figure 5–3 on page 5–7 in *Adjustment Proceedures.*



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Replaceable Mechanical Parts

This section contains a list of the replaceable mechanical components for the TLA 510 & 520. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

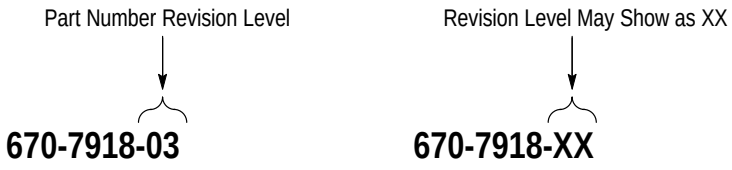
- Part number (see Part Number Revision Level below)
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Part Number Revision Level

Tektronix part numbers contain two digits that show the revision level of the part. For some parts in this manual, you will find the letters XX in place of the revision level number.



When you order parts, Tektronix will provide you with the most current part for your product type, serial number, and modification (if applicable). At the time of your order, Tektronix will determine the part number revision level needed for your product, based on the information you provide.

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Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts List Column Descriptions

Column	Column Name	Description
1	Figure & Index Number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix Part Number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial Number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & Description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. Code	This indicates the code of the actual manufacturer of the part.
8	Mfr. Part Number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

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Manufacturers Cross Index

Mfr. Code	Manufacturer	Address	City, State, Zip Code
S3109	FELLER	72 VERONICA AVE UNIT 4	SUMMERSET NJ 08873
TK0AJ	ELMEC CO LTD	621–41 OHAZA–SHIMOSHINDEN TSURUGASHIMA–CHO IRUMA–GUN	SAITAMA JAPAN
TK0392	NORTHWEST FASTENER SALES INC	7923 SW CIRRUS DRIVE	BEAVERTON OR 97005–6448
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609–3320
TK0588	UNIVERSAL PRECISION PRODUCTS	1775 NW 216TH	HILLSBORO OR 97123
TK1163	POLYCAST INC	9898 SW TIGARD ST	TIGARD OR 97223
TK1415	CABOT CORP E A R DIV	7911 ZIONSVILLE RD	INDIANAPOLIS IN 46268
TK1465	BEAVERTON PARTS MFG CO	1800 NW 216TH AVE	HILLSBORO OR 97124–6629
TK1547	MOORE ELECTRONICS INC	19500 SW 90TH CT P O BOX 1030	TUALATIN OR 97062
TK1920	TOKIN AMERICA INC	155 NICHOLSON LANE	SAN JOSE CA 95134
TK2105	QUALTEK ELECTRONICS CORP FAN–S DIV	7158 INDUSTRIAL PARK BLVD	MENTOR OH 44060
TK2133	SCHAFFNER EMC INC	9–B FADEM RD	SPRINGFIELD NJ 07081
TK2208	NORTHWEST RUBBER EXTRUDERS INC	16748 SW 77TH AVE	PORTLAND OR 97223
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY SUITE #2	VANCOUVER WA 98601
TK2517	N M B TECHNOLOGIES INC	1735 TECHNOLOGY DRIVE SUITE 700	SAN JOSE CA 95110
TK2541	AMERICOR ELECTRONICS LTD	2682 W COYLE AVENUE	ELK GROVE VILLAGE IL 60007
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
TK2586	KEYTRONIC CORP	PO BOX 14687	SPOKANE, WA 99216
TK6027	3M/ASSOCIATED ELECTRONICS	9450 PINENEEDLE DR PO BOX 270	MENTOR OH 44061–0270
0B445	ELECTRI–CORD MFG CO INC	312 EAST MAIN ST	WESTFIELD PA 16950
0GZV8	HUBER AND SUHNER INC	ONE ALLEN MARTIN DRIVE	EXXEX VT 05451
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661–2999
0KB01	STAUFFER SUPPLY	810 SE SHERMAN	PORTLAND OR 97214
0KBZ5	MORELLIS Q & D PLASTICS	1812 16TH AVE	FOREST GROVE OR 97116
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655303	DALLAS TX 75262–5303
05469	BEARINGS INC	3634 EUCLID P O BOX 6925	CLEVELAND OH 44101
06383	PANDUIT CORP	17301 RIDGELAND TINLEY	PARK IL 60477–3048
06915	RICHCO PLASTIC CO	5825 N TRIPP AVE	CHICAGO IL 60646–6013
07416	NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039–241

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Manufacturers Cross Index (Cont.)

Mfr. Code	Manufacturer	Address	City, State, Zip Code
07556	CALABRO INDUSTRIES INC	1372 ENTERPRISE DR GOSHEN CORP PO BOX 1927	WESTCHESTER PA 19380–5960
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
1Y013	DEANCO, ACACIA DIVISION	3101 SW 153RD DRIVE	BEAVERTON OR 97006
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125–4632
15513	DATA DISPLAY PRODUCTS	301 CORAL CIR	EL SEGUNDO CA 90245–4620
22526	BERG ELECTRONICS INC (DUPONT)	857 OLD TRAIL RD	ETTERS PA 17319
27264	MOLEX INC	2222 WELLINGTON COURT	LISLE IL 60532–1613
28520	HEYCO MOLDED PRODUCTS	750 BOULEVARD P O BOX 160	KENILWORTH NJ 07033–1721
3M099	PORTLAND SCREW CO	6520 N BASIN ST	PORTLAND OR 97217–3920
5Y400	TRIAX METAL PRODUCTS INC DIV OF BEAVERTON PARTS MFG CO	1800 NW 216TH AVE	HILLSBORO OR 97124–6629
50356	TEAC AMERICA INC	7733 TELEGRAPH RD P O BOX 750	MONTEBELLO CA 90640–6537
50434	HEWLETT–PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131–1008
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
6D224	CONTEX TRI–TEK ENGINEERING CORP	14500 SOUTH BROADWAY	GARDENA CA 90248
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
61935	SCHURTER INC	1016 CLEGG COURT	PETALUMA CA 94952–1152
63852	QUANTUM CORPORATION	500 MC CARTHY BLVD	MILPITAS CA 95035
64537	KDI ELECTRONICS INC SUBSIDIARY OF KDI CORP	31 FARINELLA DR	EAST HANOVER NJ 07936
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076–9749
74594	COMPONENT RESOURCES INC (DIST) DIV OF CPI INTERNATIONAL CORP	14525 SW WALKER ROAD	BEAVERTON OR 97006
75915	LITTELFUSE INC SUB TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016–3049
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001
81073	GRAYHILL INC	561 HILLGROVE AVE PO BOX 10373	LA GRANGE IL 60525–5914
85471	BOYD CORP	13885 RAMOMA AVE	CHINO CA 91710
86928	SEASTROM MFG CO INC	701 SONORA AVE	GLENDALE CA 91201–243
97124	NORTH STAR NAMEPLATE	1281–S NE 25TTH	HILLSBORO OR 97124
9M860	ELECTRONIC SUB ASSEMBLY MFG CORP (ESAM)	930 SE M STREET PO BOX 376	GRANTS PASS OR 97526–3248

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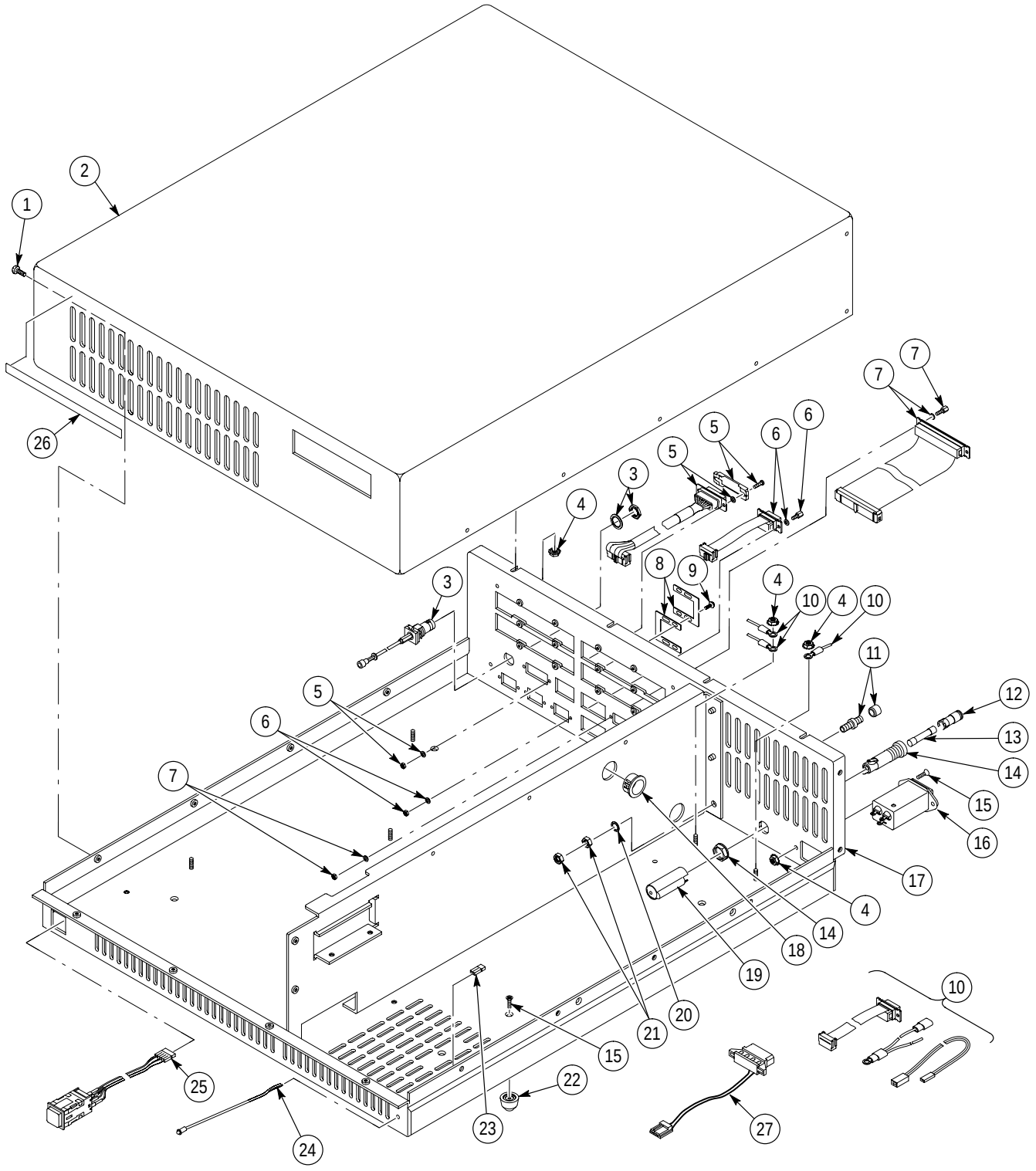


Figure 10–1: Cabinet Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					CABINET ASSEMBLY		
1–1	211–0581–00			16	SCREW,MACHINE:6–32 X 0.375,TRH,STL	TK0435	ORDER BY DESC
–2	437–0447–00			1	CABINET,TOP:ALUMINUM,	80009	437044700
–3	174–3301–00			1	CA ASSY,SP:COAX,;RFD,94 OHM,9.5 INCH,SMB, FEMALE,STR X BNC,JACK,ISOLATED GRD, W/9400 PF CAP,REAR PNL MTG	TK2469	174–3301–00
–4	210–0457–00			6	NUT,PL,ASSEM WA:6–32 X 0.312,STL CD PL	TK0435	ORDER BY DESC
–5	174–3302–00			1	CA ASSY,SP:JKTD RIBBON,LAN;IDC,16,28 AWG, 15 POS,FEMALE,DSUB X 2X8,0.1 CTR,RCPT	TK2469	174–3302–00
–6	174–2665–00			3	CA ASSY,SP,ELEC:3.25 L,DB9 TO 10 PIN HDR	1Y013	67931
–7	174–3303–00			1	CA ASSY,SP:RIBBON,;IDC,37,28 AWG,13.0L,37 POS,FEMALE,DSUB,W/4–40,THD INSERT X 2X20,0.1CTR,RCPT,CTR PLZ	TK2469	174–3303–00
–8	407–4335–00			4	BRACKET,EMI:ALUM,TLA510	80009	ORDER BY DESC
–9	211–0244–00			6	SCR,ASSEM WSHR:4–40 X 0.312,PNH,STL,CD,PL,POZ,MACHINE	0KB01	211–0244–00
–10	198–5821–00			1	WIRE SET,ELEC:TLA 510/TLA 520,12 EA RING TONGUE X RING OR SPADE,1,STRIP X STRIP, 1,2X3 X 1X3,26 AWG,1,DB9 X 2X5,RCPT; (POWER SUPPLY & PRIMARY WIRE SET)	80009	198582100
–11	129–0103–00			1	POST,BDG,ELEC:ASSEMBLY	TK0588	ORDER BY DESC
–12	200–2264–00			1	CAP,FUSEHOLDER:3AG FUSES, (STD 115 V)	61935	FEK 031 1666
	200–2265–00			1	CAP,FUSEHOLDER 5 X 20MM FUSES,(230 V)	61935	FEK 031 1663
–13	159–0046–00			1	FUSE,CARTRIDGE:3AG,8A,250V,15SEC,CER, (STD 115 V)	71400	ABC 8
	159–0353–00			1	FUSE,CARTRIDGE:5MM X 20MM,5A,250V (230V)	61935	75930000
–14	204–0832–00			1	BODY,FUSEHOLDER:3AG & 5 X 20MM FUSES	61935	031 1673 (FEU M
–15	211–0559–00			7	SREW MACHINE 6–32 X 0.375,FLH,100 DEG,STL CD PL,POZ		
–16	119–2944–00			2	FILTER,RFI: 10A,115–230V,48–440H	TK2133	FN321–10–01–0
–17	437–0446–00			1	CABINET,BOTTOM:ALUMINUM,	80009	437044600
–18	348–0532–00			2	GROMMET,PLASTIC:BLACK,ROUND,0.625 ID	28520	2096
–19	200–0237–04			1	COVER,FUHLR:PLASTIC,	0JR05	ORDER BY DESC
–20	210–0046–00			1	WASHER,LOCK:0.261 ID,INTL,0.018 THK,STL	78189	1214–05–00–0541
–21	210–0455–00			1	NUT,PLAIN,HEX:0.25–28 X 0.375,BRS NP	73743	3089–402
–22	348–0080–01			5	FOOT,CABINET:CHARCOAL GRAY, POLYURETHANE	TK2208	ORDER BY DESC

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
1–23	352–0169–00	B010100	B010284	1	HLDR,TERM CONN 2 WIRE,BLACK 0.1 SPACING (TLA510 ONLY)	0JR05	ORDER BY DESC
–23	352–1058–00	B010285		1	HLDR,TERM CONN CRIMP HSG,;FEMALE,CTR,1.25MM, 0.156 X 0.167 W,ACCOM MOLEX 50058 & 50079 TERMINALS (TLA510 ONLY)	0JR05	ORDER BY DESC
–23	352–0169–00	B010100	B010177	1	HLDR,TERM CONN 2 WIRE,BLACK 0.1 SPACING (TLA520 ONLY)	0JR05	ORDER BY DESC
–23	352–1058–00	B010178		1	HLDR,TERM CONN CRIMP HSG,;FEMALE,CTR,1.25MM, 0.156 X 0.167 W,ACCOM MOLEX 50058 & 50079 TERMINALS (TLA520 ONLY)	0JR05	ORDER BY DESC
–24	150–1054–01	B010100	B010284	1	DIODE,OPTO:,LED;GRN,560NM,0.3MCD AT 10MA, T1 IN HOUSING W/6" LEADS,MINI BERG CONN (HOUSING NOT INCLUDED) (TLA510 ONLY)	15513	SP940223–G (P20
–24	150–1054–02	B010285		1	DIODE,OPTO:,LED;GRN,560NM,0.3MCD AT 10MA, T1 IN HOUSING W/6" LEADS,MOLEX CONN (HOUSING NOT INCLUDED) (TLA510 ONLY)	TK1547	150–1054–02
–24	150–1054–01	B010100	B010177	1	DIODE,OPTO:,LED;GRN,560NM,0.3MCD AT 10MA, T1 IN HOUSING W/6" LEADS,MINI BERG CONN (HOUSING NOT INCLUDED) (TLA520 ONLY)	15513	SP940223–G (P20
–24	150–1054–02	B010178		1	DIODE,OPTO:,LED;GRN,560NM,0.3MCD AT 10MA, T1 IN HOUSING W/6" LEADS,MOLEX CONN (HOUSING NOT INCLUDED) (TLA520 ONLY)	TK1547	150–1054–02
–25	262–0360–01			1	SWITCH,PUSH:SPDT;ALTERNATE ACTION,PANEL MNT,ILLUMINATED,0.1A AT 125V,GOLD CONTACTS,W/CABLE &CONNECTOR	74594	IDC–4–01–4552 R
–26	334–8780–00			1	MARKER,IDENT:TLA 510	0KB05	334–8780–00
	334–8781–00			1	MARKER,IDENT:TLA 520	0KB05	334–8781–00
–27	174–3291–00			1	CA ASSY,SP:RIBBON,FLOPPY;CPR,2,22 AWG,6.0 L,1X4,0.25 CTR,RCPT,MATE–N–LOCK X1X4,0.098 CTR,LATCHING.RCPT	TK2469	174–3291–00

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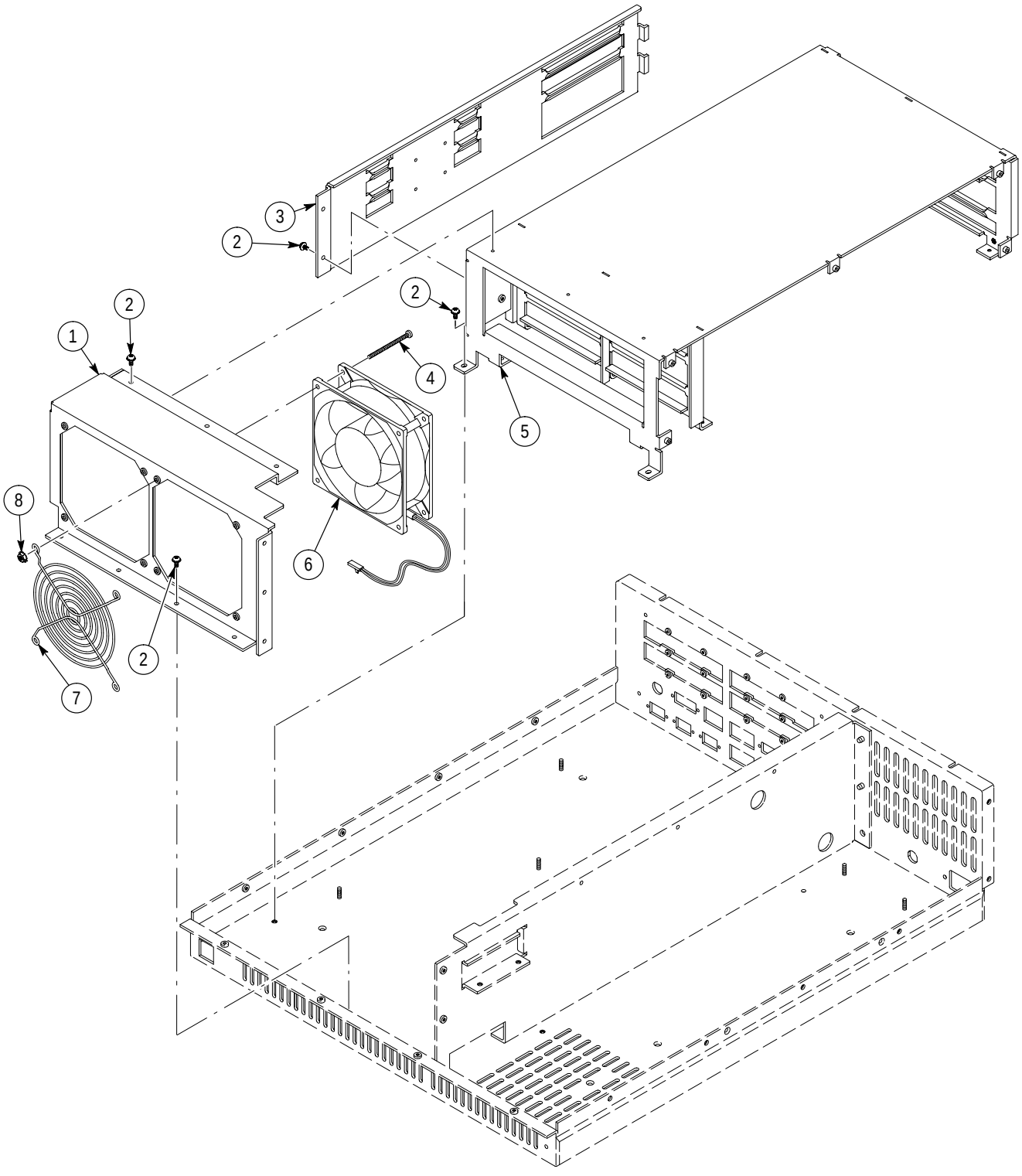


Figure 10–2: Chassis & Fan Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					CHASSIS & FAN ASSEMBLY		
2–1	407–4298–00			1	BRACKET,FAN:ALUMINUM,	80009	407429800
–2	211–0658–00		B010428	11	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ(TLA510)	TK0435	17691–300
	211–0658–00		B010228	11	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ(TLA510)	TK0435	17691–300
–3	386–6737–00			1	BRACKET,GUIDE:STIFFENER,CIRCUIT BOARD EDGE CARD,ALUM	80009	386673700
–4	211–0552–00			8	SCREW,MACHINE:6–32 X 2.0,PNH,STL	TK0435	ORDER BY DESC
–5	441–2058–00			1	CHAS,CARD CAGE:ALUMINUM,	80009	441205800
–6	119–4757–00			2	FAN,DC:TUBEAXIAL;12V,6W,2800/1600RPM,100 CFM,45/31 DBA,120MM X38.4MM	TK2517	4715ML–012P535P
–7	200–2222–00			2	GUARD,FAN:7912AD,	TK2105	08213
–8	210–0457–00			8	NUT,PL,ASSEM WA:6–32 X 0.312,STL CD PL	TK0435	ORDER BY DESC

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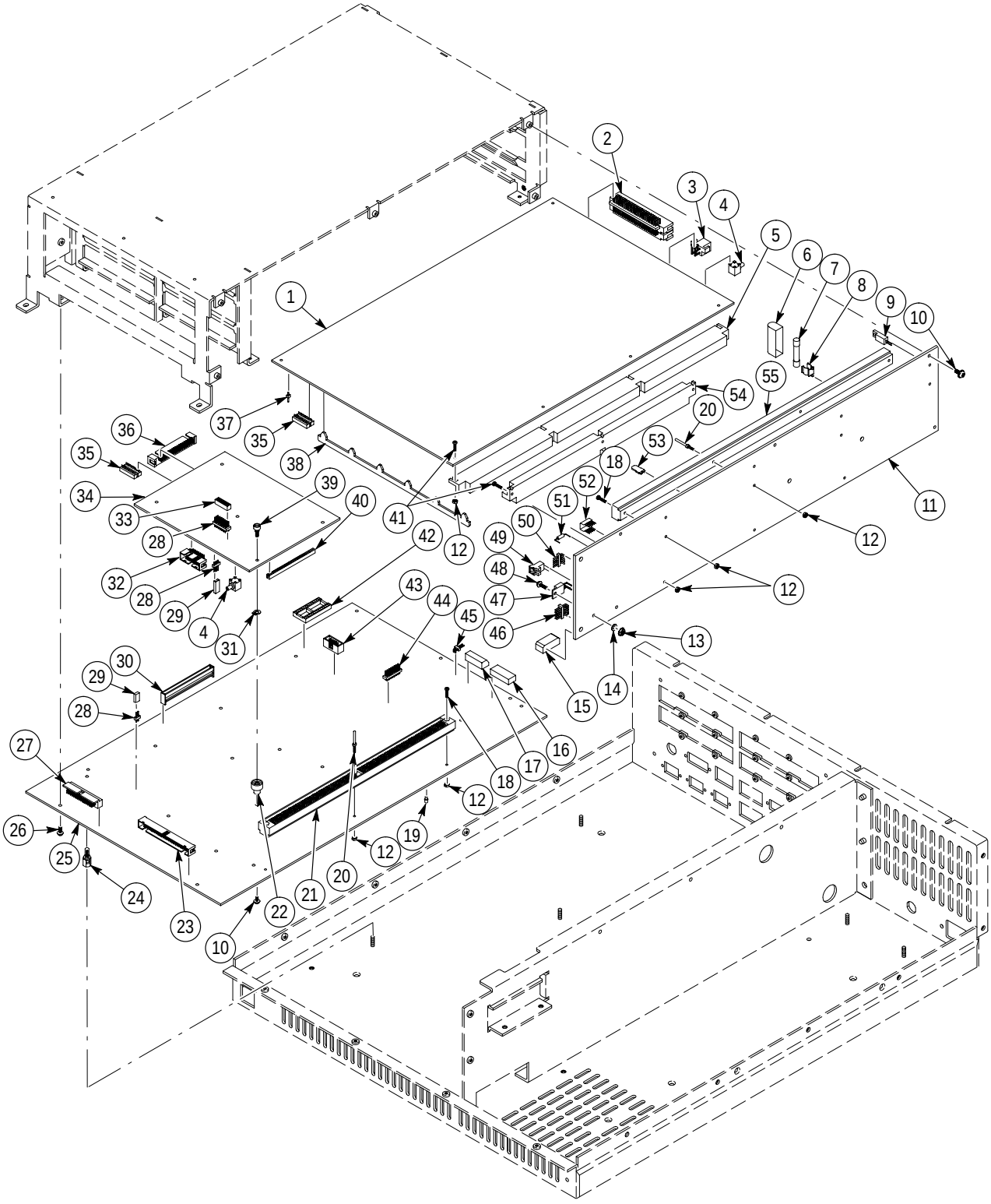


Figure 10–3: Circuit Boards

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					CIRCUIT BOARDS		
3–1	671–3254–00			1	CKT BD ASSY:8K POWERFLEX ACQUISITION MODULE (A32 STANDARD)	80009	671325400
	671–3255–00			1	CKT BD ASSY:32KPOWERFLEX ACQUISITION MODULE (A32 92C96D OPTION 01)	80009	671325500
	671–3256–00			1	CKT BD ASSY:128K POWERFLEX ACQUISITION MODULE (A32 92C96XD OPTION 02)	80009	671325600
	671–3257–00			1	CKT BD ASSY:512K POWERFLEX ACQUISITION MODULE (A32 92C96SD OPTION 03)	80009	671325700
	671–3463–00			1	CKT BD ASSY 100 CH, 2M DEEP ACQUISITION MODULE (A33 92A96UD OPTION 06)	80009	671–3463–00
–2	131–4955–00			2	CONN,HDR::PCB,;MALE,RTANG,4 X 25 0.1CTR, 0.640 H X 0.155 TAIL,SHRD/4 SIDES,CTR PLZ,30 GOLD,(2)2 X 25,W/O LATCH	TK1465	131–4955–00
–3	131–4945–00			1	CONN,HDR PWR::PCB,;MALE,RTANG,2 X 2,0.165 CTR,0.394 H X 0.138 TAIL,SHRD/4 SIDES,PLZ, LATCHING,TIN,94V–2,9 AMP	27264	39–29–1048
–4	131–0265–00			2	CONN,RF PLUG:SMB,;PCB,MALE,RTANG,50 OHM ,0.381 H X 0.15 TAIL,0.043 DIA CTR COND,0.040 SQ TAIL	0GZV8	85SMB–50–0–1
–5	131–3714–01			1	CONN,HDI:PCB,;FEMALE,RTANG,4 X 135,540 POS,0.1 CTR,0.480 MLG X0.120 TAIL,30 GOLD, W/DUAL GUIDE PINS	22526	50005–1540E
–6	200–3299–00		B010510	1	COVER,FUSE,FLEXIBLE,BLUE (TLA510)	06915	840836
–6	200–3299–00		B010270	1	COVER,FUSE,FLEXIBLE,BLUE (TLA520)	06915	840836
–7	159–0029–00			1	FUSE,CARTRIDGE:3AG,0.3A,250V,20SEC,	71400	MDL 3/10
–7	344–0326–00			2	CLIP,ELECTRICAL:FUSE,BRASS,	75915	102071
–7	260–2611–00			1	SWITCH,THRMSTC:;NC,30VDC,0.1A,1W,OPEN AT 75 DEG C,RADIAL LEADED (J301,J302)	TK1920	OHD5R–75B
–10	211–0661–00			5	SCR,ASSEM WSHR 4–40 X 0.25,PNH,STL,CD PL,POZ,MACHINE	TK0435	821–01655–024
–11	671–3165–00			1	CIRCUIT BD ASSY:BACKPLANE (A01 TLA 510 & TLA 520)	80009	671316500
–12	220–0032–00			11	NUT:2–56 X 0.188 X 0.062 THK,SST	0KB01	ORDER BY DESC
–13	210–0586–00			1	NUT,PL,ASSEM WA:4–40 X 0.25,STL CD PL	TK0435	ORDER BY DESC
–14	210–0994–00			1	WASHER,FLAT:0.125 ID X 0.25 OD X 0.022,STL	12327	ORDER BY DESC

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
3–15	131–3545–00			1	CONN,HDR PWR:PCB,;MALE,STR,1 X 4,0.200 CTR(J780)	27264	15–24–4049
–16	150–1083–00			1	DIODE,OPTO:,LED;RED,655NM,10 ELEMENT BAR GRAPH ARRAY	50434	HDSP–4820
–17	260–2285–00			1	SWITCH,ROCKER:SPST;DIP,8 POSITION,SIDE ACTUATED,0.1 OHM CONTACT RES,5A,2PF, 0.980"L,0.281"H,0.380"W,SEALED	81073	76PSB08S
–18	211–0404–00			2	SCREW,MACHINE:2–56 X O.375,PNH, SST POZ	TK0392	ORDER BY DESC
–19	386–1635–00			5	SUPPORT,CKT BD:CHASSIS MT,ACETAL	80009	386163500
–20	351–0778–01			1	GUIDE,PIN:0.585 X 0.080,2–56,SST	22526	77268–002
–21	131–3713–00			1	CONN,HDI:PCB,;MALE,STR,4 X 92,368 POS,0.01 CTR,0.460 H X 0.120TAIL,30 GOLD,W/CTR GUIDE PIN,,	22526	50016–1368J
–22	129–1423–00			5	SPACER,POST:0.44 L,4–40 THRU INT EXCEPT 0.07 TOP,0.312 DIA	TK1465	129–1423–00
–23	131–3182–00			1	CONN,HDR:PCB,;MALE,RTANG,2 X 25,0.1CTR, 0.390 MLG X 0.112 TAIL,0.33 H,SHRD/4 SIDES, CTRPLZ,30 GOLD,HIGH TEMP	22526	75867–008
–24	361–1675–00			5	SPACER:CKT BD,3/8 INCH,NYLON	80009	361167500
–25	671–2324–08			1	CKT BD ASSY:DAS CONTROLLER (A70 TLA 510 & TLA 520)	80009	671232408
–26	211–0244–00			4	SCR,ASSEM WSHR:4–40 X 0.312,PNH,STL,CD PL,POZ,MACHINE	TK0435	7772–312
–27	131–2567–00			1	CONN,HDR:PCB,;MALE,RTANG,2 X 17,0.1CTR, 0.390 H,0.230 MLG X 0.1 TAIL,PLZ WALL,CTR PLZ,30 GOLD,0.15 PCB TO SQ PIN	22526	65461–006
–28	131–1857–00			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD (J680,J681,J682,J683,J684,J685,J686)	58050	082–3644–SS10
–29	131–0993–00			1	CONN,BOX:SHUNT,;FEMALE,STR,1 X 2,0.1 CTR, 0.385 H,30 GOLD,BLACK,JUMPER	22526	65474–006
–30	131–5428–00			1	CONN,HDR:PCB,;MALE,STR,2 X 50,0.050CTR, 0.480 H X 0.100 TAIL,SHRD/4 SIDES,END PLZ, PRESS–IN MTG POST,30 GOLD,0.012 SQ	22526	87434–150
–31	354–0393–00			5	RING,RETAINING:EXT GRIP,U/O 0.156 DIA SFT	05469	5555–15MD
–32	131–3453–00			1	CONN,HDR:PCB,;MALE,RTANG,2 X 8,0.1 CTR, 0.390 MLG X 0.112 TAIL,0.33 H,SHRD/4 SIDES,30 GOLD (J880)	53387	2516–5002UB
–33	131–4550–00			1	CONN,BOX::SHUNT,;FEMALE,STR,2 X 7,JUMPER (P680,P681,P682,P683,P684,P685,P686)	22526	69145–214

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
3–34	671–2452–02			1	CIRCUIT BD ASSY:LAN IO ADAPTER (A71)	80009	671245202
–35	136–0729–00			2	SOCKET,DIP:PCB,;FEMALE,STR,2 X 8,16 POS, (U810)	58050	082–3643–SS02
–36	131–3181–00			1	CONN,HDR:PCB,:MALE,RTANG,2 X 20,0.1CTR	53387	2540–50K2UB
–37	131–1343–00			1	CONN,HDR::PCB,;MALE,STR,1 X 36,0.1 CTR,GOLD	09922	DILB16P–108T
–38	386–5339–01			1	STIF,CIRCUIT BD:BRASS	5Y400	386–5339–01
–39	213–1076–00			4	THUMBSCREW:4–40 X 0.215,0.250 OD, SS,SLOT	TK1465	ORDER BY DESC
–40	131–5213–00			1	PCB,;FEMALE,STR,2 X 50,0.050 CTR,0.180 H X 0.120 TAIL, W/GUIDE,BD RETENTION (J687)		
–41	211–0405–00			4	SCREW,MACHINE:2–56 X 0.375,TRH,SST POZIDRIVE	TK0392	ORDER BY DESC
–42	136–0755–00			1	SOCKET,DIP:PCB,;FEMALE,STR,2 X 14,28 POS,0. 1 X 0.6 CTR,0.175 H X0.130 TAIL,BECU,TIN,AC COM 0.008–0.0015 X 0.014–0.022	09922	DILB28P–108
–43	131–5438–00			4	CONN,HDR:PCB,;MALE,STR,2 X 5,0.100 CTR, 0.0365 H X 0.105 TAIL,SHRD/4 SIDES,CTR PLZ, 0.025 DIA,GXT	22526	66506–066
–44	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
–45	131–3766–00			1	CONN,HDR:PCB,;MALE,RTANG,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30 GOLD,0.025 SQ	00779	87232–2
–46	131–2221–00			1	CONN,HDR:PCB,;MALE,RTANG,2 X 25,0.1 CTR,0.318 MLG X 0.110 TIL,30 GOLD (J120,J390,J290)	22526	2–86479–9
–47	156–2558–00			1	IC,LINEAR:BIPOLAR,VOLTAGE REGULATOR; POSITIVE,12V,1.5A,2%	01295	TL780–12CKC
–48	211–0315–00			1	SCR,ASSEM WSHR:4–40 X 0.437,PHN,STL CD PL POZ	TK0435	ORDER BY DESC
–49	131–4799–00			2	CONN,HDR::PCB,;MALE,RTANG,1 X 2,0.1 CTR,0.3 H X 0.130 TAIL,SHRD/4 SIDES,CTR PLZ, LATCHING, 30 GOLD/TIN TAIL,W/MTG POSTS (J690,J790)	00779	103904–1
–50	131–1406–00			1	CONN,HDR PCB;,MAILE,RTAND,2 X 25,0.1 CTR,0.318 MLG X 0.110 TAIL,30 GOLD	80009	131–1406–00
–51	159–0059–00			3	FUSE,WIRE LEAD:5A,125V, (F580,F585,F785)	61857	SPI–5A
–52	131–4813–00			8	CONN,PWR:PRESSFIT/PCB,;STR,6–32 THD,30 AMP,0.3 X 0.1 (J180,J185,J280,J285,J380,J385,J480,J485)	00779	55556–4

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
3–53	131–2427–00			6	TERM,QIK DISC.:PCB,;MALE TAB,0.250 X 0.032,0.2 CTR, 0.497 H X 0.125 TAIL,0.307 MLG,TIN,0.055 PCB (J500,J505,J580,J583,J585,J600)	00779	62409–1
–54	131–3712–01			1	CONN,HDI:PCB,;FEMALE,RTANG,3 X 92,368 POS, 0.1 CTR,0.48 MLG X 0.145 TAIL,30 GOLD, W/CTR GUIDE PIN (J000)	22526	50004–1368F
–55	131–3715–00			2	CONN,HDI:PCB,MALE,STR,4 X 135,540 POS,0.1 CTR, 0.46 H X 0.177 TAIL,30 GOLD,W/DUAL GUIDE PINS; (J200,J300)	22526	50017–1540A

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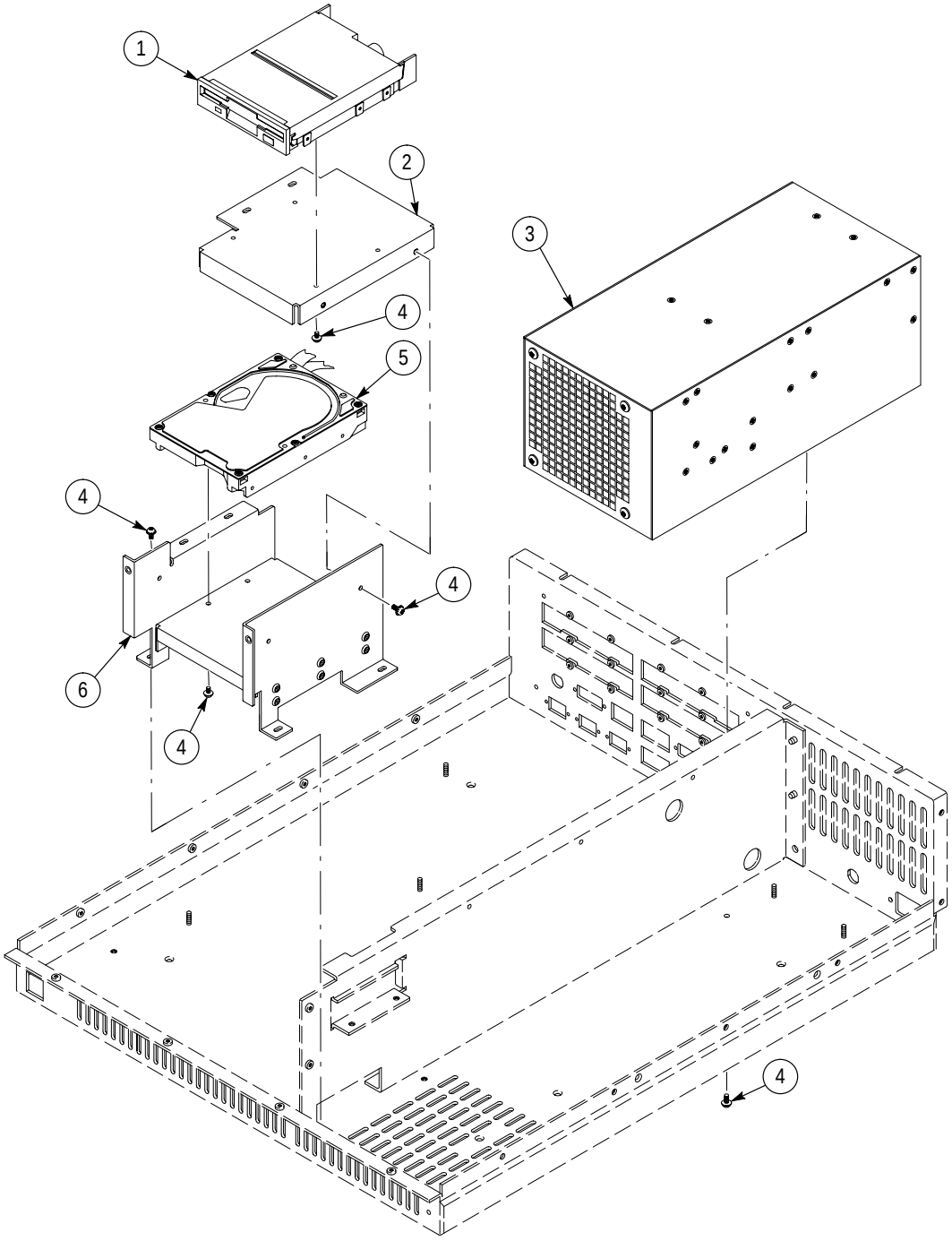


Figure 10–4: Power Supply & Disk Drive Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					POWER SUPPLY & DISK DRIVE ASSEMBLY		
4–1	119–4758–00			1	DISK DRIVE:FLOPPY,3.5 INCH;1.44MB, 1 INCH, TWOSIDED,DOUBLEDENSITY,IBM GRAY	50356	FD–235HF–3201
–2	407–4299–00			1	BRACKET:FLOPPY DRIVE,ALUMINUM,	5Y400	407–4299–00
–3	119–4760–00			1	POWER SUPPLY:90–250 VAC LINE,47–63HZ, OUTPUTS,5.15V,2 VA 13A,+/–15V AT 3AMPS, POWER FAIL,DC OK,REMOTE ON/OFF	80009	119476000
–4	211–0658–00		B010428	11	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ(TLA510)	TK0435	17691–300
	211–0658–00		B010228	11	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ(TLA520)	TK0435	17691–300
–5	119–4787–00	B010100	B010284	1	DISK,DRIVE:WINCHESTER,3.5,170MB,1.0 INCH HIGH, 17MS,SCSI (TLA510 ONLY)	63852	ELS170
–5	119–5089–00	B010285	B010498	1	DISK,DRIVE:WINCHESTER,3.5,270MB,1.0 INCH HIGH, 14MS SCSI (TLA510 ONLY)	63852	QM30270MV/F
–5	119–5491–00	B010499		1	DISK,DRIVE:WINCHESTER,3.5,1.2GB,1.0 INCH HIGH, 14MS SCSI (TLA510 ONLY)	63852	QM31280FBS
–5	119–4787–00	B010100	B010177	1	DISK,DRIVE:WINCHESTER,3.5,170MB,1.0 INCH HIGH, 17MS,SCSI (TLA520 ONLY)	63852	ELS170
–5	119–5089–00	B010178	B010269	1	DISK,DRIVE:WINCHESTER,3.5,270MB,1.0 INCH HIGH, 14MS SCSI (TLA520 ONLY)	63852	QM30270MV/F
–5	119–5491–00	B010270		1	DISK,DRIVE:WINCHESTER,3.5,1.2 GB,1.0 INCH HIGH, 14MS SCSI (TLA520 ONLY)	63852	QM31280FBS
–6	407–4297–00			1	BRACKET,ASSY:MEDIA BRACKET,ALUMINUM	80009	407429700

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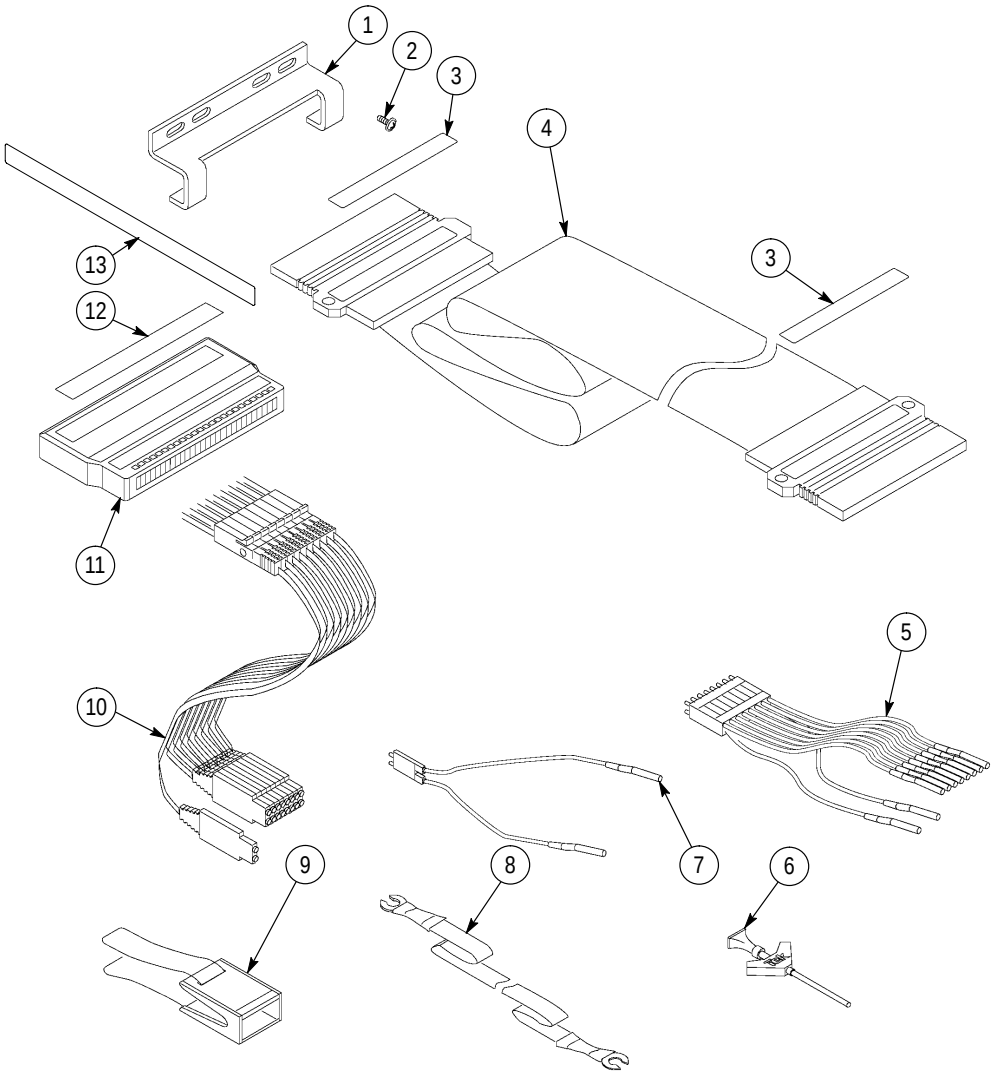


Figure 10–5: TLA Accessories

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					TLA 510 & 520 STANDARD ACCESSORIES		
	P6041			1	PROBE,PASSIVE:1X,3.5 FT	80009	ORDER BY DESC
5–1	407–4096–01			2	BRACKET,CABLE:ALUMINUM (TLA 510)	5Y400	407–4096–01
	407–4096–01			4	BRACKET,CABLE:ALUMINUM (TLA 520)	5Y400	407–4096–01
–2	211–0244–00			4	SCR,ASSEM WSHR:4–40 X 0.312,PNH,STL,CD PL,POZ (TLA 510)	TK0435	7772–312
	211–0244–00			8	SCR,ASSEM WSHR:4–40 X 0.312,PNH,STL,CD PL,POZ (TLA 520)	TK0435	7772–312
–3	334–8029–00			1	MARKER,IDENT:MKD 92A96	07416	334–8029–00
	334–8244–00			8	MARKER,IDENT:92A96/D/XD CABLE LABEL,BLUE	07416	ORDER BY DESC
	334–8245–00			8	MARKER,IDENT:92A96/D/XD CABLE LABEL,GREEN	07416	ORDER BY DESC
	334–8246–00			8	MARKER,IDENT:92A96/D/XD CABLE LABEL,GRAY	07416	ORDER BY DESC
	334–8247–00			8	MARKER,IDENT:92A96/D/XD CABLE LABEL,ORANGE	07416	ORDER BY DESC
–4	174–2117–01			4	CA ASSP,SP,ELEC:25 W/GNDS,60.0 L,RIBBON (TLA 510)	80009	17421170
	174–2117–01			8	CA ASSP,SP,ELEC:25 W/GNDS,60.0 L,RIBBON (TLA 520)	53387	98–0300–5385–8
–5	012–1424–00			6	LEADSET, ELEC 8 CH LEADSET (TLA 510)	80009	012142400
	012–1424–00			12	LEADSET, ELEC 8 CH LEADSET (TLA 520)	80009	012142400
–6	206–0364–00			72	TIP,PROBE:MICROCKT TEST,0.05 CTR (TLA 510)	80009	206–0364–00
	206–0364–00			144	TIP,PROBE:MICROCKT TEST,0.05 CTR (TLA 520)	80009	206–0364–00
–7	196–3347–00			12	LEAD SET,ELEC:PODLET,3.0 L (TLA 510)	1Y013	66314
	196–3347–00			24	LEAD SET,ELEC:PODLET,3.0 L (TLA 520)	1Y013	66314
–8	196–3353–00			1	LEAD,ELECTRICAL:9 AWG,72.0 L,BRAID	1Y013	196–3353–00
	010–0492–00			1	PROBE SET:100 PODLETS,W/HOUSINGS & HOLDERS INDEX ITEMS 9,10 & 11 ARE PART OF 010–0492–00 (TLA 510)	53387	98–0300–3905–5
	010–0492–00			2	PROBE SET:100 PODLETS,W/HOUSINGS & HOLDERS (TLA 520)	53387	98–0300–3905–5
–9	352–0939–00			16	HOLDER,PODLET:POLYCARBONATE	53387	98–0300–5581–2

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
5–10	010–0493–00			12	PODLET CA ASSY:12.0 L,BLACK	80009	010049300
	010–0493–01			12	PODLET CA,ASSY:12.0 L,BROWN	80009	010049301
	010–0493–02			12	PODLET CA,ASSY:12.0 L,RED	80009	010049302
	010–0493–03			12	PODLET CA,ASSY:12.0 L,ORANGE	80009	010049303
	010–0493–04			12	PODLET CA,ASSY:12.0 L,YELLOW	80009	010049304
	010–0493–05			12	PODLET CA,ASSY:12.0 L,GREEN	80009	010049305
	010–0493–06			12	PODLET CA,ASSY:12.0 L,BLUE	80009	010049306
	010–0493–07			12	PODLET CA,ASSY:12.0 L,PURPLE	80009	010049307
	010–0493–08			4	PODLET CA,ASSY:13.0 L	80009	010049308
–11	380–0964–00			4	HOUSING,INTERFA:2 X 25 W/LATCHING FEATURE	53387	98–0300–3903–0
–12	334–8248–00			1	MARKER,IDENT:92A96/D/XD CHANNEL GROUPING BLUE	07416	ORDER BY DESC
	334–8249–00			1	MARKER,IDENT:92A96/D/XD CHANNEL GROUPING GREEN	07416	ORDER BY DESC
	334–8250–00			1	MARKER,IDENT:92A96/D/XD CHANNEL GROUPING GRAY	07416	ORDER BY DESC
	334–8251–00			1	MARKER,IDENT:92A96/D/XD CHANNEL GROUPING ORANGE	07416	ORDER BY DESC
–13	334–8030–00			1	MARKER,IDENT:MKD 92A96,PROBE LOCATION	07416	ORDER BY DESC
	070–8977–XX			1	MANUAL,TECH:USER,TLA 510 & TLA 520	TK2548	070–8977–XX
	070–7832–XX			1	MANUAL,TECH:USERS,92A96/92C96 MODULE	TK2548	070–7832–XX
	161–0066–00			1	CA ASSY,PWR:3,18 AWG,250V/10A,98 INCH,STR, IEC320,RCPT X NEMA 5–15P,US	0B445	ECM–161–0066–00
	119–4273–01			1	COLOR MONITOR:TECO 14 INCH 1024 X 768 COLOR/W NEW REAR PANEL	80009	119–4273–01
	011–0123–00			2	TERMN,COAXIAL:50 OHM,BNC,VSWR DC–4 GHZ 1.15	64537	T190CS
	103–0030–00			2	ADAPTER,CONN:BNC T MALE TO 2 FEMALE	00779	221 543–2
	012–0205–00			1	CA ASSY,INTCON:COAXIAL,;RFD,(1)50 OHM,108L, BNC,MALE,BOTH ENDS	TK2469	012–0205–00
	012–1445–00			1	CA ASSY,INTCON:SHLD CMPST,;MLD,7,26 AWG, 10FT,9 POS,MALE,DSUB,DB9M X9 POS,FEMALE, DSUB,DB9F,W/JACK SCREWS,DUAL SHLD	80009	012144500
					TLA 510 & TLA 520 OPTIONAL ACCESSORIES		
	P6460			1	ACQ PROBE:8/9 CAHN,100MHZ ACQ PROBE INC LEADSET & CLIPS	80009	ORDER BY DESC
	P6465			1	PAT GEN PROBE:9 CHAN,50MHZ PSYGRN PROBE W/1 CLK & RZ/R1 INPUT	80009	ORDER BY DESC
	010–0508–00			1	MICRO P INTFC:90 CHANNEL INTERFACE	80009	ORDER BY DESC
	010–0492–10			1	25 PODLETS W/HOUSING,HOLDERS & LABELS	80009	ORDER BY DESC
	020–2107–00			1	8 CHANNEL LEADSETS,PKG OF 6	80009	ORDER BY DESC
	020–2108–00			1	(6)8–CHANNEL LEAD SETS,(72) KLIPCHIPS,(6) Y–CABLES	80009	ORDER BY DESC
	020–2109–00			1	50 CHANNEL PROBE SET W/LEADSET,KLIPCHIPS,Y CABLES & RIBBON CABLES	80009	ORDER BY DESC

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
	070–8976–XX			1	MANUAL,TECH:SERVICE,TLA 510 & TLA 520	TK2548	070–8976–XX
	020–1888–00			1	ACCESSORIES KIT (PKG 0F 12)	80009	020188800
	020–1890–02			1	ACCESSORIES KIT25 CHANNEL PROBE SET WITH LEADSETS AND GRABBERS	80009	ORDER BY DESC
	020–1386–01			1	ACCESSORY KIT:PACKAGE OF 12 (206–0364–00)	80009	020138601
	070–8499–XX			1	MANUAL,TECH:USER,DAS9200,92PA PERFORMANCE ANALYSIS (OPTION 04 ACCESSORIES)	80009	0708499XX
	070–8653–XX			1	MANUAL,TECH:USER,92XTERM (OPTION 1X)	80009	0708653XX
	070–5950–XX			1	MANUAL,TECH:USERS,92S16 PATTERN GENERATOR MODULE (OPTION 30)	80009	0705950XX
	P6463A			2	PAT GEN PROBE:9.16 CHANNEL MUXED, 50MHZ/25MHZ WITH ACC (OPTION 30)	80009	ORDER BY DESC
					INTERNATIONAL POWER CORDS A1–A5		
	161–0066–09			2	CA ASSY,PWR:3,0.75MM SQ,250V/10A,99 INCH, STR,IEC320,RCPT,EUROPEAN (OPTION A1)	S3109	86511000
	161–0066–10			2	CA ASSY,PWR:3,0.1MM SQ,250V/10A,2.5 METER, STR,IEC320,RCPT X 13A,FUSED UK PLUG(13A FUSE),UNITED KINGDOM (OPTION A2)	S3109	BS/13–H05VVF3G0
	161–0066–11			2	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER, STR,IEC320,RCPT,AUSTRALIA (OPTION A3)	S3109	198–000
	161–0066–12			2	CA ASSY,PWR:3,18 AWG,250V/10A,98 INCH,STR, IEC320,RCPT X NEMA 6–15P,US (OPTION A4)	TK2541	13E68,25–1E–250
	161–0154–00			2	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,S TR,IEC320,RCPT,SWISS (OPTION A5)	S3109	12–H05VVF3G 00–

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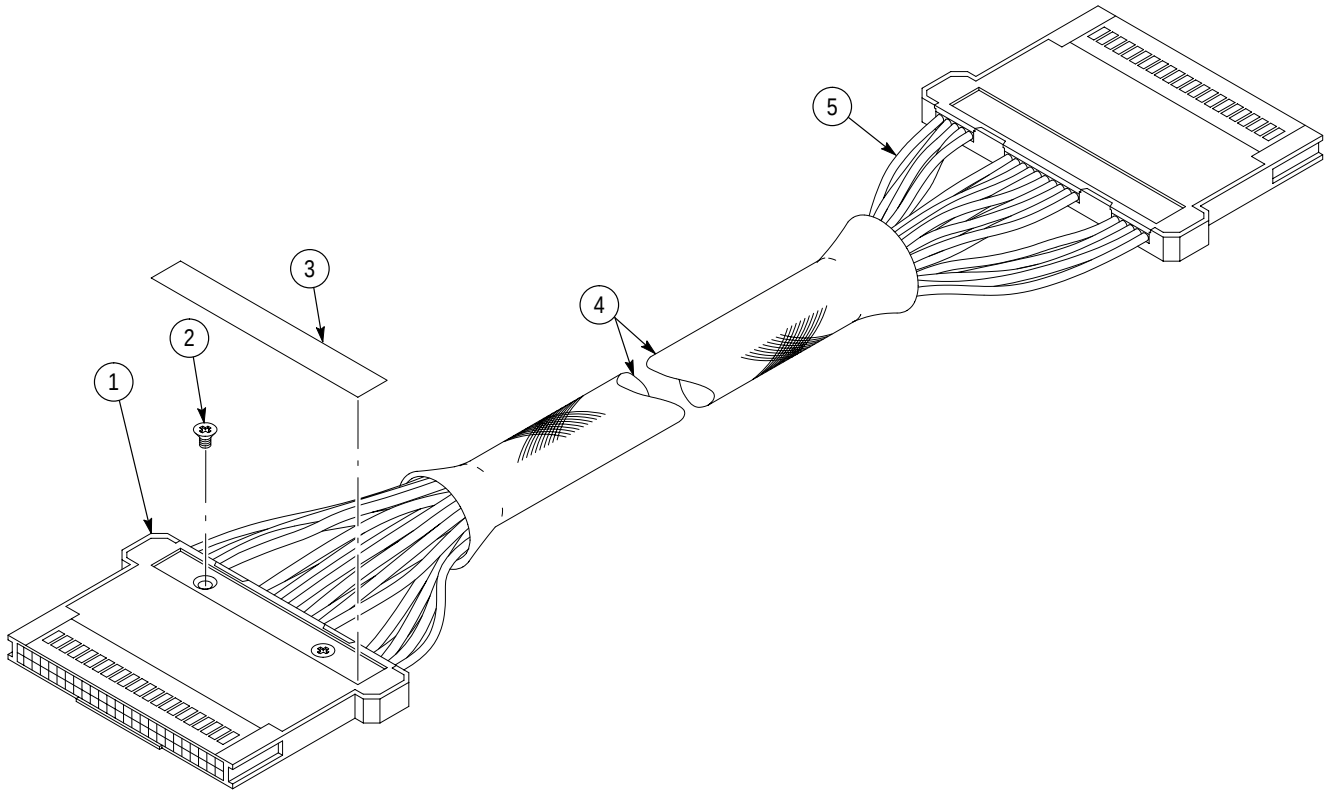


Figure 10–6: Coaxial Probe Cable

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					COAXIAL PROBE CABLE		
6–1	198–5761–00			1	WIRE SET,ELEC:60.0 L,SET OF 4	07556	ORDER BY DESC
–2	211–0105–00			4	SCREW,MACHINE:4–40 X 0.188,FLH,100 DEG,STL	TK0435	MACHINE SCREW:
–3	334–8244–00			4	MARKER,IDENT:92A96/D/XD CABLE LABEL,BLUE	07416	ORDER BY DESC
	334–8245–00			4	MARKER,IDENT:92A96/D/XD CABLE LABEL, GREEN	07416	ORDER BY DESC
	334–8246–00			4	MARKER,IDENT:92A96/D/XD CABLE LABEL,GRAY	07416	ORDER BY DESC
	334–8247–00			4	MARKER,IDENT:92A96/D/XD CABLE LABEL, ORANGE	07416	ORDER BY DESC
–4	174–2571–00			4	CA ASSY,RF:25 CONDUCTOR,60.0L	07556	ORDER BY DESC
–5	174–2622–00			25	CA ASSY,RF:2,39 OHM COAX,26 AWG WIRE,MINI PVC,BOTH ENDS,59.0 L	TK2469	ORDER BY DESC

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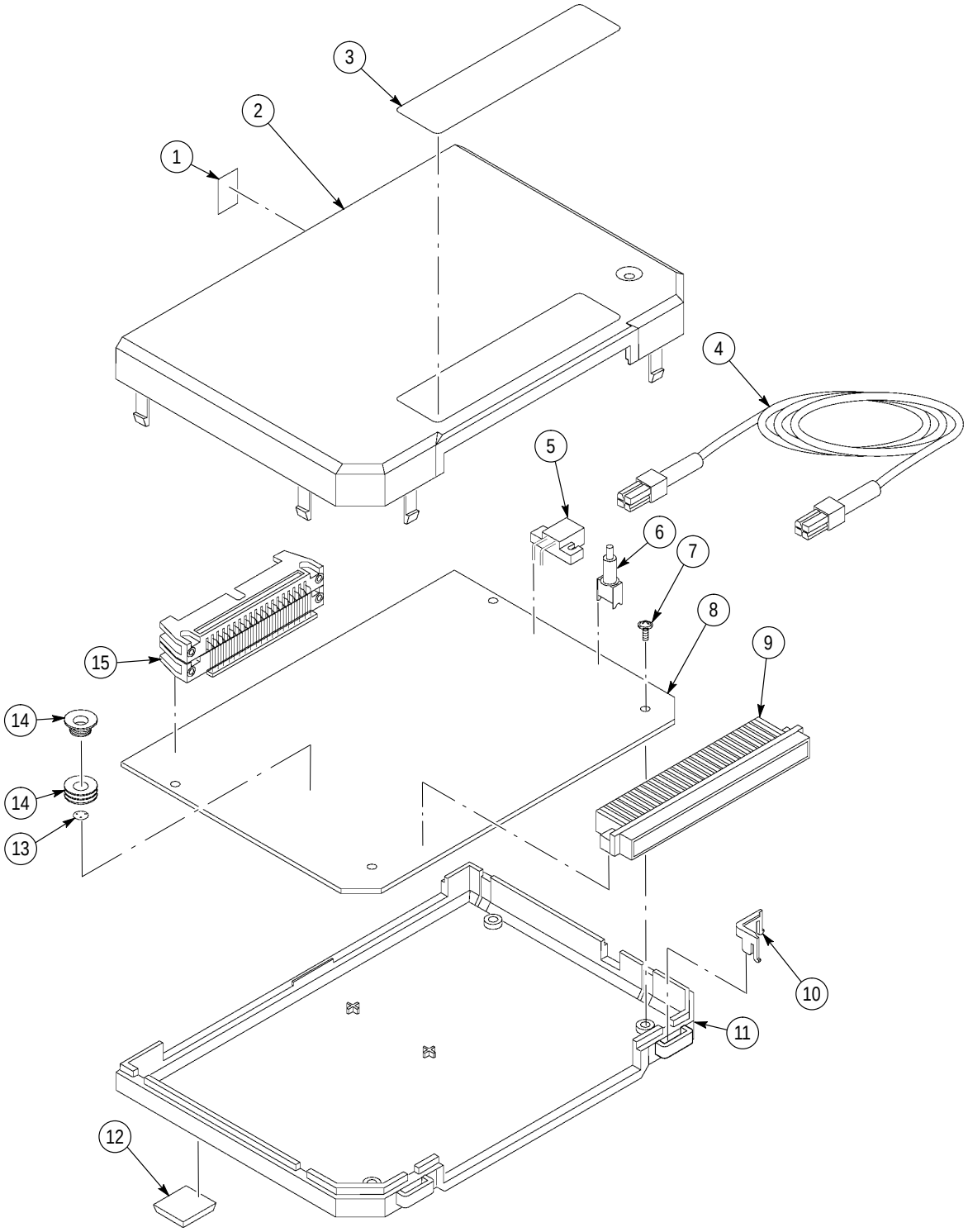


Figure 10–7: 90 Channel Interface

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					90 CHANNEL INTERFACE		
7–0	010–0508–00			1	MICRO P INTFC:90 CHANNEL INTERFACE	80009	ORDER BY DESC
–1	334–8031–00			1	MARKER,IDENT:MKD 92A96,90 CH I/F	07416	334–8031–00
–2	380–0994–00			1	HOUSING,ADAPTER:UPPER,INTERFACE,LEXAN,	TK1163	380–0994–00
–3	334–8011–00			1	MARKER,IDENT:MKD 90 CHANNEL,	07416	334–8011–00
–4	174–2348–00			1	CA ASSY,SP,ELEC:4,22 AWG,72.0 L	1Y013	ASI 65861
–5	131–4945–00			1	CONN,HDR PWR::PCB,;MALE,RTANG,2 X 2,0.165 CTR, 0.394 H X 0.138 TAIL,SHRD/4 SIDES,PLZ,LATCHING,TIN, 94V–2,9 A	27264	39–29–1048
–6	260–2314–00			1	SWITCH,PUSH:SPST,0.4 VA MAX,20VDC	95146	TPD11CG–PC0
–7	211–0661–00			4	SCR,ASSEM WSHR:4–40 X 0.25,PNH,STL,CD PL,POZ	TK0435	ORDER BY DESC
–8	671–1806–00			1	CIRCUIT BD ASSY:90 CHANNEL INTERFACE (A30)	80009	671180600
–9	131–3151–00			1	CONN,DIN:PCB,;MALE,RTANG,3 X 32,0.1 CTR, 0.437 H X 0.104 TAIL,30 GOLD	00779	650473–5
–10	105–1034–00			4	LATCH,PROBE:RIGHT ANGLE	TK1163	105–134–00
–11	380–0995–00			1	HOUSING,ADAPTER:LOWER INTERFACE,LEXAN,	TK1163	380–0994–00
–12	348–0910–00			4	FOOT,CKT BD HSG:92A60	52152	SJ5007
–13	386–1130–00			1	INSULATOR,DISK:TRANSISTOR,NYLON (USED WITH A30U1701)	13103	7717–15N
–14	214–0668–00			1	HEATSINK,SEMIC:TRANSISTOR,TO–5/TO–39;TWO PIECE, 0.625"DIA,50C/W@1W,ALUMINUM, BLACK ANODIZE (USED WITH A30U1707)	13103	2211B
–15	131–4955–00			2	CONN,HDR:PCB,MALE,RTANG,4 X 25 0.1 CTR,0.640 H X 0.155 TAIL,SHRD/4 SIDES,CTR PLZ,30GOLD,(2)2 X 25,W/O LATCH	TK1465	131–4955–00

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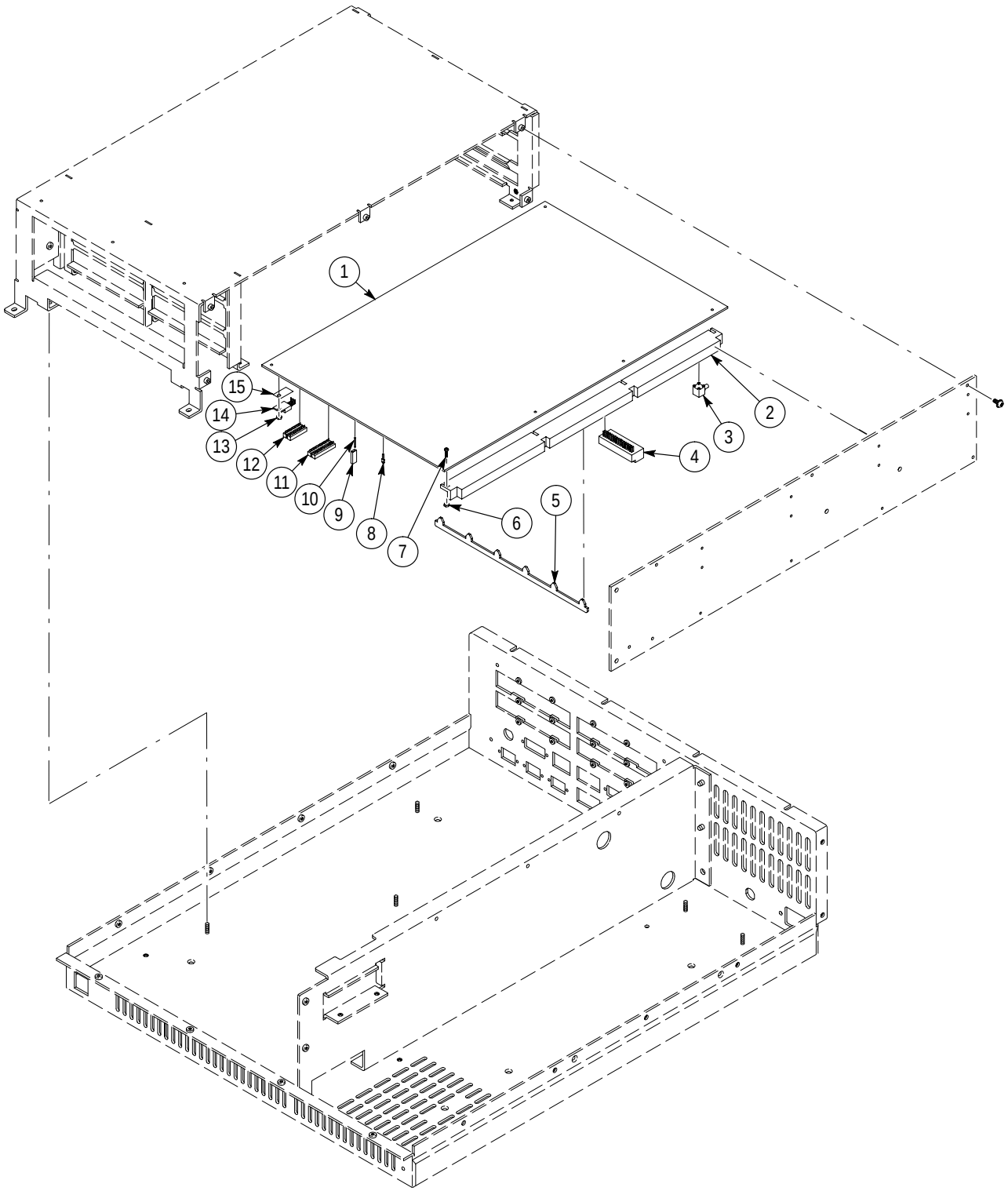


Figure 10–8: 92S16 Pattern Generator Circuit Board

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					92S16		
8–1	670–9593–12			1	CIRCUIT BD ASSY:PATTERN GENERATOR MDL (A40)	80009	670959312
–2	131–3714–00			1	CONN,RCPT,ELEC:FEMALE,540 PIN	22526	67884–004
–3	131–3617–00			1	CONN,RCPT,ELEC:CKT BD,RTANG	80009	131361700
–4	131–3087–00			3	CONN,HDR:PCB,;MALE,RTANG,2 X 17,0.1 CTR, 0.420 H X 0.140 TAIL,SHRD/4 SIDES,CTR PLZ	22526	67950–001
–5	386–5339–01			1	STIF,CIRCUIT BD:BRASS	5Y400	386–5339–01
–6	220–0032–00			11	NUT:2–56 X 0.188 X 0.062 THK,SST	0KB01	ORDER BY DESC
–7	211–0405–00			4	SCREW,MACHINE:2–56 X 0.375,TRH,SST POZIDRIVE	TK0392	ORDER BY DESC
–8	214–0579–00			11	TERM,TEST POINT:PCB,TEST POINT;EYELET 0.055ID,0.4 L X 0.052 WIDE X 0.032 THK,TIN PL,W/0.045 TIP CHAMFER	0KB01	ORDER BY DESC
–9	131–0993–00			1	CONN,BOX:SHUNT,;FEMALE,STR,1 X 2,0.1 CTR, 0.385 H,30 GOLD,BLACK,JUMPER	22526	65474–006
–10	131–0590–03			36	TERMINAL,PIN:0.38 L X 0.025 SQ,NO FERRULE	80009	131059003
–11	136–0634–01			3	SKT,PL–IN ELEK:MICROCKT,20 DIP,LOW PF MACHINED CONTACT	80009	136063401
–12	136–0260–04			1	SKT,PL–IN ELEK:MICROCIRCUIT,16 DIP	80009	136026004
–13	210–0406–00			1	NUT,PLAIN,HEX:4–40 X 0.188,BRS CD PL	73743	12161–50
–14	156–1207–02			1	MICROCKT,LINEAR:VOLTAGE RGLTR,–12V, TO=92	80009	156120702
–15	342–0163–01			1	INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER SONY TEK	80009	342016301

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					STANDARD ACCESSORIES		
	P6463A			2	PAT GEN PROBE:9/16 CHANNEL MUXED,50MHZ/25MHZ WITH ACC	80009	ORDER BY DESC
					92S16 OPTIONAL ACCESSORIES		
	P6041			1	PROBE,PASSIVE:1X,3.5 FT	80009	ORDER BY DESC
	P6460			1	ACQ PROBE:8/9 CAHN,100MHZ ACQ PROBE INC LEADSET & CLIPS	80009	ORDER BY DESC
	P6465			1	PAT GEN PROBE:9 CHAN,50MHZ PSYGRN PROBE W/1 CLK & RZ/R1 INPUT	80009	ORDER BY DESC
	070–5654–XX			1	MANUAL TECH:020–1392–00 CONTROLLED WIDTH PROBELET	80009	0705654XX
	165–0001–11			1	MICROCKT,LINEAR:PATTERN GENERATOR PROBE		
	003–1134–00			1	ALIGN TOOL,ELEK:18–0603	TK0AJ	32–1902–00
	020–1392–01			1	ACCESSORY KIT:OPTIONAL		
	020–1484–01			1	ACCESSORY KIT PKG OF 4 PROBE RETAINER (TLA510 & 520)	80009	020148401

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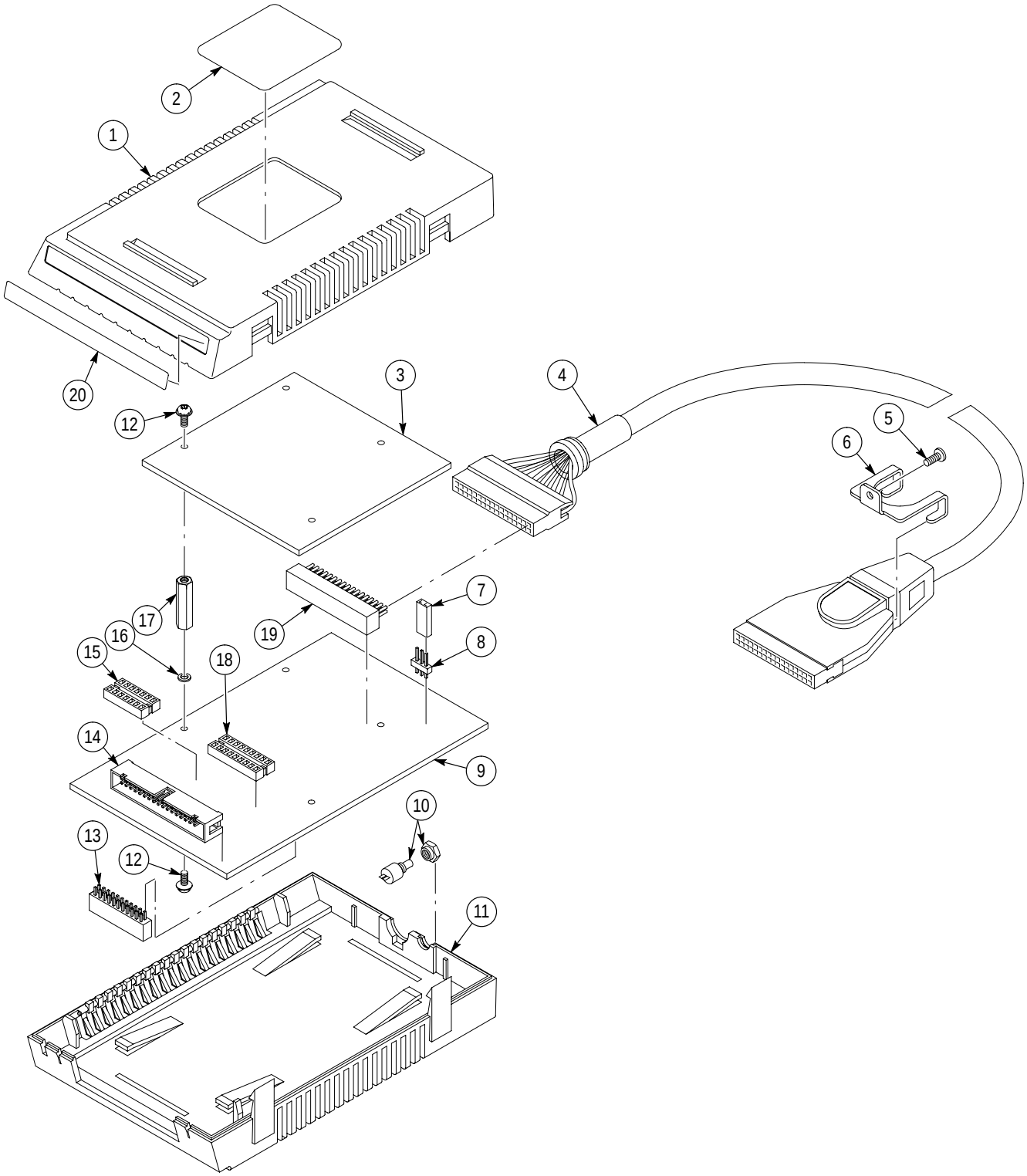


Figure 10–9: P6463A Probe Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					P6463A		
9–0	010–0501–01			1	PROBE,PAT GEN:9/16 CHANNEL MUXED,50MHZ/25MHZ W/ACC	80009	010050101
–1	380–0735–00			1	HOUSING HALF:UPPER,	TK1163	ORDER BY DESC
–2	334–7938–00			1	MARKER,IDENT:MARKED P6463A,	07416	334–7938–00
–3	671–0273–02			1	CIRCUIT BD ASSY:ID/LOGIC	80009	671027302
–4	175–9677–01			1	CA ASSY,SP,ELEC:11 SGL,11 TW PR,28 AWG, 80.0L	6D224	901950
–5	211–0097–00		B010428	1	SCREW,MACHINE:4–40 X 0.312,PNH,STL(TLA510)	TK0435	ORDER BY DESC
	211–0097–00		B010228	1	SCREW,MACHINE:4–40 X 0.312,PNH,STL(TLA520)	TK0435	ORDER BY DESC
–6	343–1292–01			1	RETAINER,PROBE:ALUMINUM	5Y400	343–1292–01
–7	131–0993–00			2	CONN,BOX:SHUNT,;FEMALE,STR,1 X 2,0.1 CTR, 0.385 H,30 GOLD,BLACK,JUMPER	22526	65474–006
–8	131–4157–00			1	CONN,HDR:PCB,;MALE,STR,2 X 11,0.1 CTR,0.230 MLG X 0.110 TAIL, O.380 H STANDOFF, 10 GOLD,0.728 OVERALL LENGTH	53387	924227–24–11–I
–9	671–1793–00			1	CIRCUIT BD ASSY:P6463A BUFFER/DRIVER	80009	671179300
–10	175–9699–01			1	CA ASSY,SP,ELEC:2,26 AWG,6.0 L	80009	175969901
–11	380–0873–00			1	HOUSING,HALF:LOWER,PLASTIC	TK1163	380–0873–00
–12	211–0244–00			4	SCR,ASSEM WSHR:4–40 X 0.25,PNH,STL,CDPL, POZ	TK0435	ORDER BY DESC
–13	136–0939–00			1	SKT,PL–IN ELEK:CKT BD MY,2 X 11,0.1 SPACING	TK6027	929852–01–11–30
–13	136–0939–00			1	SKT,PL–IN ELEK:CKT BD MY,2 X 11,0.1 SPACING	TK6027	929852–01–11–30
–14	131–3363–00			1	CONN,HDR PCB,;MALE,RTANG,2 X 17,0.1CTR,0.33 H X 0.112 TAIL,SHRD/4 SIDES,CTR PLZ,30 GOLD	53387	2534–5002UB
–15	136–0728–00			5	SOCKET,DIP:PCB,;FEMALE,STR,2 X 7,14 POS,0.1X 0.3 CTR, 0.175 H X 0.130 TAIL,BECU,TIN	09922	DILB14P–108
–16	210–0906–00			4	WASHER,FLAT:0.125 OD X 0.2 OD X 0.035,FBR	TK1742	1/8" X 13/64" O
–17	129–0198–00			4	SPACER,POST:0.75 L.4–40 EA END,BRS,0.188 HEX	TK0588	ORDER BY DESC
–18	136–0756–00			2	SOCKET,DIP:PCB,;FEMALE,STR,2 X 9,18 POS,0.1 X 0.3 CTR, 0.175 H X 0.130 TAIL,BECU,TIN	09922	DILB18P–108
–19	131–4226–00			1	CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR, 0.280 MLG X 0.150 TAIL,0.240 H,30 GOLD	22526	65820–035
–20	334–7038–00			1	MARKER,IDENT:MARKED P6463	07416	334–7038–00

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					STANDARD ACCESSORIES		
	070–7971–XX			1	MANUAL,TECH:INSTR,P6463A,DAS 9/16 CHANNEL PATTERN GENERATION PROBE	TK2548	070–7971–XX
	012–1012–01			1	CABLE,INTCON:DAS9100 SERIES TO PROBE	80009	012101201
					OPTIONAL ACCESSORIES		
	012–1236–00			1	LEAD SET,ELEC:FLYING,34 COND,8.0 L	1Y013	63342
	012–1236–20			1	LEAD SET,ELEC:FLYING,34 COND,14.0 L	1Y013	63342
	020–1386–01			1	ACCESSORY KIT:PACKAGE OF 12 (206–0364–00)	80009	ORDER BY DESC
	020–1587–00			1	COMPONENT KIT:P6463 OPTIONAL ACCESSORY	80009	ORDER BY DESC
	196–2963–00			1	LEAD SET,ELEC:2,34 AWG,3.156 L(2 LEADS)	9M860	ORDER BY DESC
	175–9290–00			1	CA ASSY,SP,ELEC:34,28 AWG,59.0 L,RIBBON	22526	ORDER BY DESC

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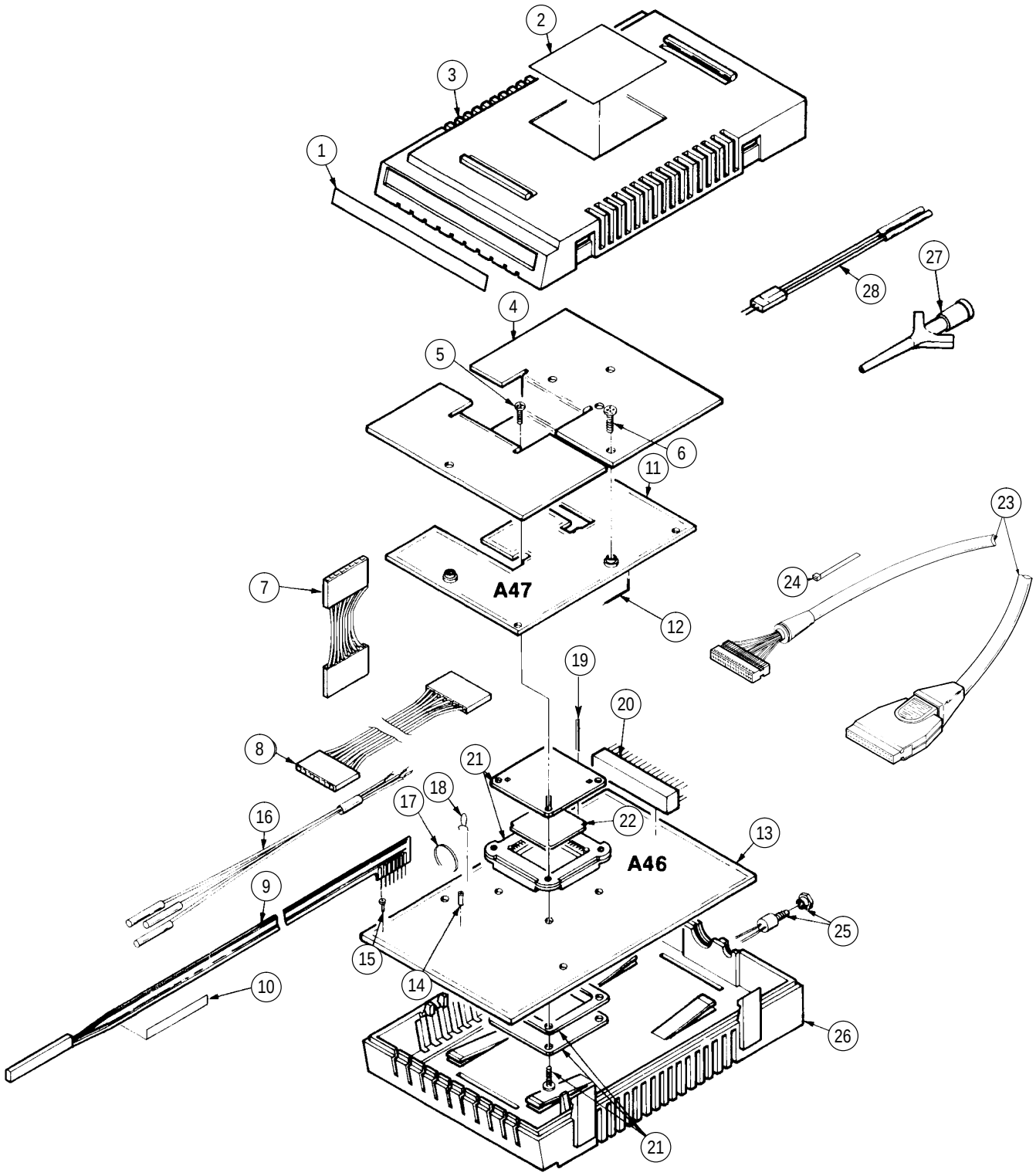


Figure 10–10: P6465 Probe Assembly

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Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					P6465		
10–0	010–6465–03			1	PROBE,PAT GEN:9 CHAN,50MHZ	80009	010646503
–1	334–6651–00			1	LABEL:3.050 X 0.325	07416	ORDER BY DESC
–2	334–6635–01			1	MARKER,IDENT:MARKED TEKTRONIX P6465	07416	ORDER BY DESC
–3	380–0735–00			1	HOUSING HALF:UPPER,	TK1163	ORDER BY DESC
–4	214–3904–00			1	HEAT SINK,ELEC:ALUMINUM	5Y400	ORDER BY DESC
–5	211–0374–00			4	SCREW,MACHINE:2–56 X 0.219 L,PNH,STL,CD	TK0435	ORDER BY DESC
–6	211–0007–00			3	SCREW,MACHINE:4–40 X 0.188,PNH,STL	TK0435	ORDER BY DESC
–7	174–0390–00			1	CA ASSY SP:RIBBON,;CPR,8,26 AWG,2.75 L,1X 8,0.1 CTR, BOTH ENDS	TK1375	174–0390–00
–8	175–4568–00			1	CA ASSY,SP,ELEC:8,26 AWG,4.5 L,RIBBON	1Y013	62310
–9	165–2048–13			1	MICROCKT,DGTL:LET 2048 W/INSUL SLVG	80009	165204813
–10	334–6653–00			10	MARKER,IDENT:MKD PODLET	80009	334665300
–11	670–9602–03			1	CIRCUIT BD ASSY:STROBE (A47)	80009	670960203
–12	131–0787–00			16	TERMINAL,PIN:PCB/PRESSFIT,;MALE,STR,0.025 SQ,0.448 MLG X 0.137 TAIL,0.600 L,PHOS BRZ,50 GOLD	22526	47359–001
–13	670–9603–04			1	CIRCUIT BD ASSY:MAIN (A46)	80009	670960304
–15	136–0252–07			70	SOCKET,PIN TERM:SINGLE,PCB,T/G,0.030 H, 0.054 PCB, 0.012–0.22 PIN SIZE,W/O DIMPLE	22526	75060–012
–16	175–9702–00			1	CA ASSY,SP,ELEC:3,22 AWG,23.0 L	TK1375	ORDER BY DESC
–17	346–0032–00			1	STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2829–75–4
–18	150–0057–01			1	LAMP,INCAND:5V,0.115A,7153AS15,WIRE LD	80009	150005701
–19	131–0608–00			16	CONN,TERMINAL:PRESSFIT/PCB,;MALE,STR,0.05 SQ,0.248 MLG X 0.137 TAIL,50 GOLD,PHZ BRZ, W/FERRULE (USED FOR A46J140 & J580)	22526	48283–018
–20	131–2615–00			1	CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR, 0.230 MLG X 0.090 TAIL,0.240 H,30 GOLD, MATING PIN 0.15 FROM PCB (USED FOR A46J360)	22526	65820–005
–21	——— ———			1	SKT,PLIN,ELEK:CHIP CARRIER 69,CONTACT (NOT REPLACEABLE, ORDER 670–9703–XX) (USED FOR A46J360)		
–22	361–1323–00			1	SPACER,PLATE:0.01 X 0.945 X 0.945,BRS,NP	80009	361132300
–23	175–9677–01			1	CA ASSY,SP,ELEC:11 SGL,11 TW PR,28 AWG, 80.0L	6D224	901950
–24	346–0120–00			1	STRAP,TIEDOWN,E:5.5 L MIN,PLASTIC,WHITE	06383	SST1.5M
–25	175–9699–01			1	CA ASSY,SP,ELEC:2,26 AWG,6.0 L	80009	175969901

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Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
10–26	380–0736–00			1	HOUSING HALF:LOWER	TK1163	ORDER BY DESC
					STANDARD ACCESSORIES		
–27	206–0364–00			23	TIP,PROBE:MICROCKT TEST,0.05 CTR	80009	206–0364–00
	020–1484–01		B010428	1	ACCESSORY PKG,E9 PKG OF 4 PROBE RETAINER 343–1292–00(TLA510)	80009	020148400
	020–1484–01		B010228	1	ACCESSORY PKG,E9 PKG OF 4 PROBE RETAINER 343–1292–00(TLA520)		
–28	196–2963–00			10	LEAD SET,ELEC:2,23 AWG,3.156 LEACHES (2LEADS)	9M860	ORDER BY DESC
	070–5475–XX			1	MANUAL,TECH P6464 & P6465 INSTRUCTIONS	80009	ORDER BY DESC

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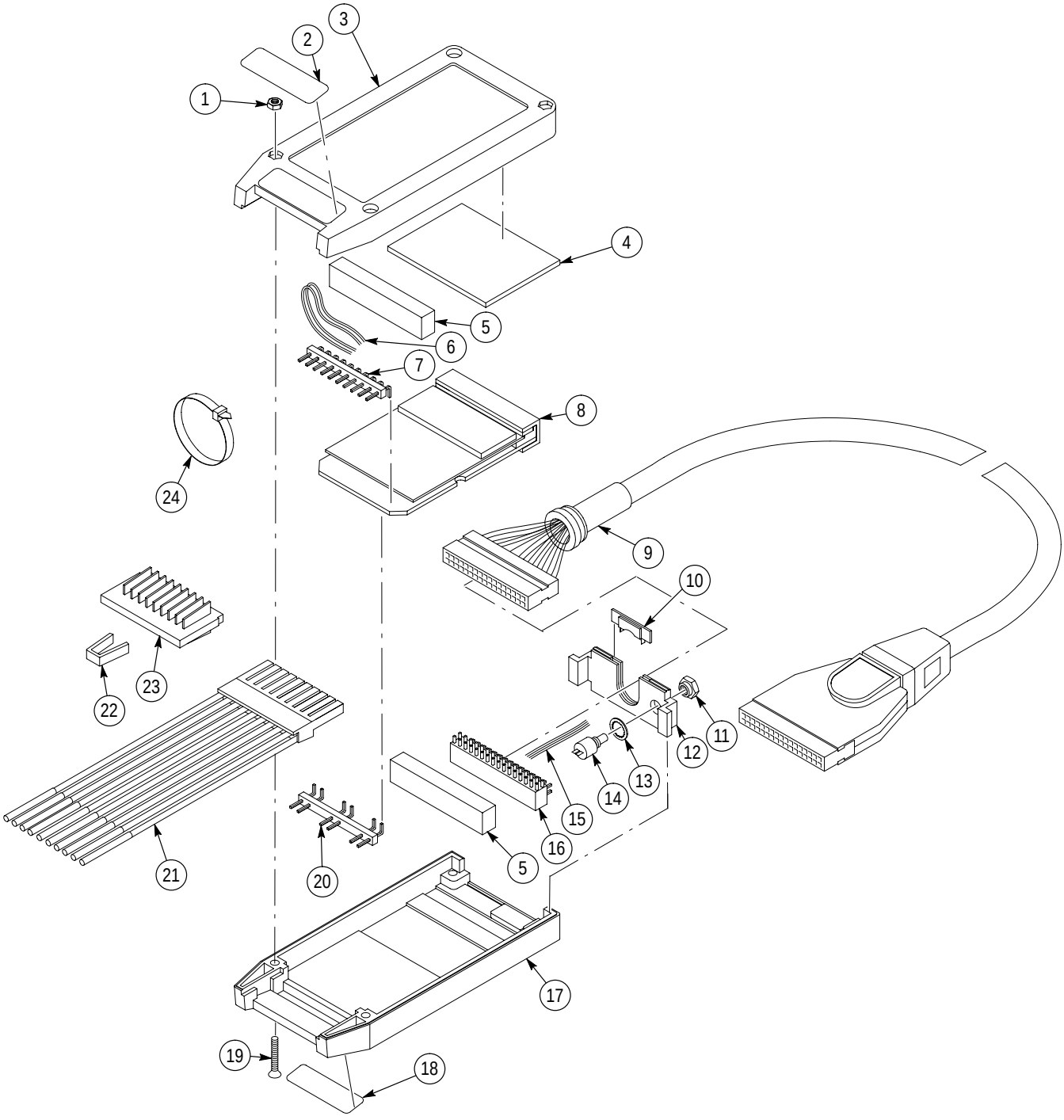


Figure 10–11: P6460 External Control Probe Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					P6460		
11–0	010–6460–01			1	PROBE,DATA ACQ	80009	ORDER BE DESC
–1	210–0406–00			4	NUT,PLAIN,HEX:4–40 X 0.188,BRS CD PL	73743	12161–50
–2	334–4855–00			1	MARKER,IDENT:MKD DIAGNOSTIC	07416	ORDER BY DESC
	334–4854–00			1	MARKER,IDENT:MKD DATA ACQUISTION PROBE	80009	ORDER BY DESC
–3	380–0711–00			1	HOUSING,PROBE:UPPER,PC	TK1163	380–0711–00
–4	348–0390–00			1	CUSHION,PROBE:1.5 X 2.0 X 0.125	TK1415	ORDER BY DESC
–5	348–0782–00			2	CUSHION,HYBRID:SILCON SPONGE	85471	348–0782–00 REV
–6	175–1580–01			1	CABLE,SP,ELEC:26 AWG SOLID TWISTED PAIR	80009	ORDER BY DESC
–7	131–1811–00			1	CONN,HDR:PCB,;MALE,RTANG,1 X 10,0.15 CTR, 0.230 MLG X 0.120 TAIL,30 GOLD	22526	65595–110
–8	672–1119–02			1	CIRCUIT BD ASSY:672–1119–01,WITHOUT 175–6807–00 CABLE (A70)	80009	672111902
–9	175–9843–01			1	CA ASSY,SP,ELEC:22,28 AWG,76.0 L (NOT ILLUSTRATED)	6D224	901951
–10	358–0675–00			1	STRAIN RLF,CA:UPPER	TK1163	358–0675–00
–11	358–0660–00			1	BUSHING,SW MTG:AL	80009	358066000
–12	358–0674–00			1	STRAIN RLF,CA:LOWER	TK1163	ORDER BY DESC
–13	210–0008–00			1	WASHER,LOCK:#8 INTL,0.02 THK,STL	0KB01	ORDER BY DESC
–14	260–0735–01			1	SWITCH,PUSH:T,NO CONTACT,BLACK BTN	81073	39–3
–15	195–1715–00			2	LEAD,ELECTRIAL:26 AWG,2.5 ,9–2	80009	ORDER BY DESC
–16	131–2615–00			1	CONN,HDR::PCB,;MALE,RTANG,2 X 17,0.1 CTR, 0.230 MLG X 0.090 TAIL,0.240 H,30 GOLD,MATING PIN 0.15 FROM PCB	22526	65820–005
–17	380–0710–00			1	HOUSING,PROBE:LOWER,PC	TK1163	380–0710–00
–18	334–4856–00			1	MARKER,IDENT:MKD P6460 ACQUISITION PROBE (92A16/E ONLY)	22670	ORDER BY DESC
	334–6157–00			1	MARKER,IDENT:MKD P6460 EXT CONT PROBE 92S16 PATTERN GENERATOR	07416	ORDER BY DESC
–19	211–0086–00			4	SCREW,MACHINE:4–40 X 0.75,FLH,100 DEG,STL	TK0435	ORDER BY DESC
–20	131–1812–00			1	CONN,HDR:PCB,;MALE,RTANG,1 X 10,0.15 CTR, 0.230 MLG X 0.120 TAIL,30 GOLD	22526	65595–110
–21	012–0987–00			1	LEAD SET,ELEC:10 WIDE,25 CML	1Y013	61502
–22	200–2731–00			3	COVER,HOLE:POLYCARBONATE,GRAY	80009	200273100
–23	361–0758–01			1	SPACER,PROBE:ACETAL SLATE GRAY	80009	361075801
–24	346–0120–00			2	STRAP,TIEDOWN,E:5.5 L MIN,PLASTIC,WHITE	06383	SST1.5M

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Replaceable Parts List (Cont.)

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					STANDARD ACCESSORIES		
	012–0987–00			1	LEAD SET,ELEC:10 WIDE,5.0 L	1Y013	61502
	020–1386–01			1	ACCESSORY KIT:PACKAGE OF 12 (206–0364–00)	80009	020138601
	012–0989–00			2	LEAD SET,ELEC:GROUND OR VL SENSE LEAD 4.0 L,BLACK W/PAMONA CLIP	1Y013	61503
	343–1292–01			1	RETAINER,PROBE:ALUMINUM (NOT ILLUSTRATED)	5Y400	343–1292–01
	211–0097–00			1	SCREW,MACHINE:4–40 X 0.312,PNH,STL (NOT ILLUSTRATED)	TK0435	ORDER BY DESC
	344–0046–00			2	CLIP,ELECTRICAL:ALLIGATOR,1.56 LSTL BRT DIPPED	80009	344004600
	070–4345–XX			1	SHEET,TECHNICAL:INSTR,010–6460–00	80009	ORDER BY DESC
					OPTIONAL ACCESSORIES		
	012–0556–00			1	LEADSET,ELEC:DIAGNOSTIC LEADSET,ELEC:12 WIDE,10.0L	1Y013	61507
	070–4675–XX			1	MANUAL,TECH:INSTR 012–0556–00 DIAGNOSTIC LEAD SET		
	012–1000–00			1	LEAD SET,ELEC:GROUND OR VL SENSE LEAD 4.0 L ,BLACK W/PAMONA CLIP (PKG OF 10)	1Y013	012098901
	012–0989–01			2			
	012–0800–00			1	LEAD SET,ELEC:10.WIDE,9.843 L	80009	012080000
	020–1041–00			1	ACCESSORY PKG:40 PIN UNIVERSAL PROBE INTERFACE	80009	020104100
	103–0209–00			1	ADAPTER,CONN:GPIB TO PROBE CLIP,TEST:16 PIN TEST	80009	103020900
	003–0709–00			1	CLIP,AP1 #923700 OR POMONA 3916	80009	003070900
	015–0330–00			1	ADPTR,TEST CLIP:16 DIP	80009	015033000
	015–0339–00			1	ADPTR,TEST CLIP:40 DIP	80009	015033900
	015–0339–02			1	ADPTR,TEST CLIP:40 DIP	80009	015033902
	380–0560–05			1	HOUSING,TERM:MALE ADAPTER	80009	380056005

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					9204XT TERMINAL ASSEMBLY		
12–1	119–4273–01	B010100	B010239	1	COLOR MONITOR:TECO 14 INCH 1024 X 768 COLOR/W.NEW REAR PANEL (TLA510 ONLY)	80009	119–4273–01
	119–4273–01	B010100	B010154	1	COLOR MONITOR:TECO 14 INCH 1024 X 768 COLOR/W.NEW REAR PANEL (TLA520 ONLY)	80009	119–4273–01
–2	119–4330–00			1	POINTER ASSY:MOUSE FOR BEETLE	80009	119433000
–3	161–0066–00			1	CA ASSY,PWR,:3,18 AWG,250V/10A,98 INCH, STR, IEC320,RCPT X NEMA 5–15P,US	80009	161006600
–4	012–1445–00			1	CA ASSY,INTCON:SHLD CMPST,;MLD,7,26 AWG, 10FT,9 POS,MALE,DSUB,DB9M X9 POS, FEMALE, DSUB,DB9F,W/JACK SCREWS,DUAL SHLD	S3109	012144500
–5	012–0205–00			1	CA ASSY,INTCON:COAXIAL,;RFD,(1)50 OHM,108L,BNC, MALE,BOTH ENDS	TK2469	012–0205–00
–6	103–0030–00			2	ADAPTER,CONN:BNC T MALE TO 2 FEMALE	00779	221 543–2
–7	011–0123–00	B010100	B010220	2	TERMN,COAXIAL:50OHM,BNC,VSWRDC –4GHZ1.15	64537	T190CS
	011–0168–00	B010221			TERMINATOR BNC,;MALE,STR,50 OHM,1 WATT,1.5;, GRAY,PLASTIC (TLA 510 ONLY)	80009	ORDER BY DESC
	011–0123–00	B010100	B010220	2	TERMN,COAXIAL:50OHM,BNC,VSWRDC –4GHZ1.15	64537	T190CS
	011–0168–00	B010137			TERMINATOR BNC,;MALE,STR,50 OHM,1 WATT,1.5;, GRAY,PLASTIC (TLA 520 ONLY)	80009	ORDER BY DESC
–8	119–4254–01	B010100	B010188	1	KEYBOARD,ASSY:IBM101,NORTH AMERICAN	TK2586	101WN63S–45E
	119–4899–00	B010189		1	KEYBOARD:KEYBOARD,101+NORTH AM W/PS/ECABLE (TLA510 ONLY)	80009	119489900
	119–4254–01	B010100	B010115	1	KEYBOARD,ASSY:IBM101,NORTH AMERICAN	TK2586	101WN63S–45E
	119–4899–00	B010116		1	KEYBOARD:KEYBOARD,101+NORTH AM W/PS/ECABLE (TLA520 ONLY)	80009	119489900

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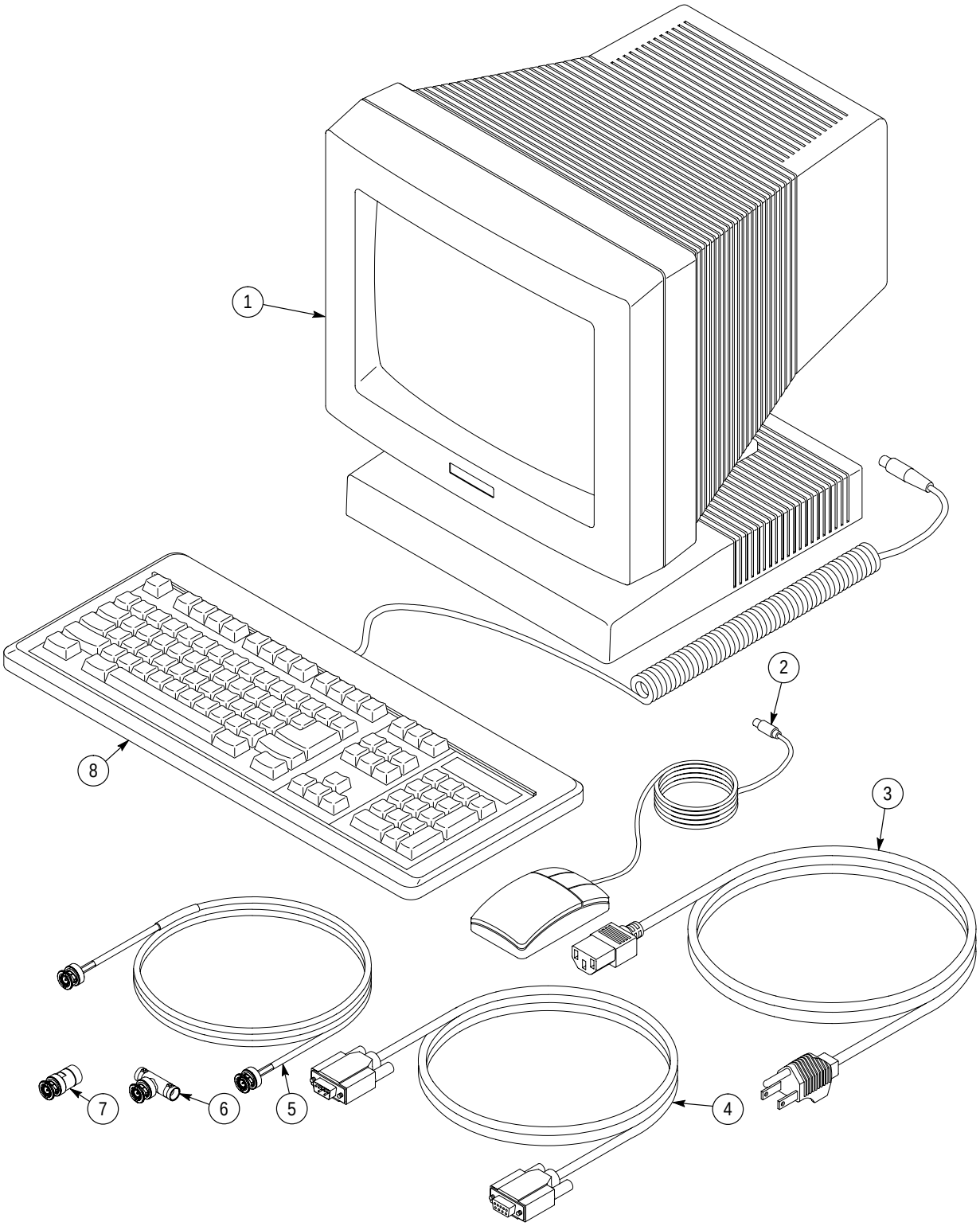


Figure 10–12: 9204XT Terminal Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					9205XT TERMINAL ASSEMBLY		
13–1	119–4625–00	B010100	B010239	1	DAS/TLA X TERMINAL 17 INCH COLOR,1152X900 RES, 2MB FLASH,SERIAL SUPPORT (TLA510 MONITOR ONLY)	80009	9205XT
	119–4625–00	B010100	B010154	1	DAS/TLA X TERMINAL 17 INCH COLOR,1152X900 RES, 2MB FLASH,SERIAL SUPPORT (TLA520 MONITOR ONLY)	80009	9205XT
–2	437–0442–01			1	CABINET ASSY:ESLIPSE/TOKENRING/LUNAR	80009	ORDER BY DESC
–3	012–0205–00			1	CA ASSY,INTCON:COAXIAL,;RFD,(1)50 OHM,108L, BNC, MALE,BOTH ENDS	TK2469	012–0205–00
–4	119–4330–00			1	POINTER ASSY:MOUSE FOR BEETLE	80009	119433000
–5	161–0066–00			1	CA ASSY,PWR,:3,18 AWG,250V/10A,98 INCH, STR, IEC320, RCPT X NEMA 5–15P,US	80009	161006600
–6	012–1445–00			1	CA ASSY,INTCON:SHLD CMPST,;MLD,7,26 AWG, 10FT,9 POS,MALE,DSUB,DB9M X9 POS,FEMALE, DSUB,DB9F, W/JACK SCREWS,DUAL SHLD	80009	012144500
–7	011–0123–00	B010100	B010220	2	TERMN,COAXIAL:50OHM,BNC,VSWRDC –4GHZ 1.15	64537	T190CS
	011–0168–00	B010221			TERMINATOR BNC,;MALE,STR,50 OHM,1 WATT,1.5;, GRAY, PLASTIC (TLA510 ONLY)	80009	ORDER BY DESC
	011–0123–00	B010100	B010136	2	TERMN,COAXIAL:50OHM,BNC,VSWRDC –4GHZ 1.15	64537	T190CS
	011–0168–00	B010137			TERMINATOR BNC,;MALE,STR,50 OHM,1 WATT,1.5;, GRAY, PLASTIC (TLA520 ONLY)	80009	ORDER BY DESC
–8	103–0030–00			2	ADAPTER,CONN:BNC T MALE TO 2 FEMALE	00779	221 543–2
–9	119–4254–01	B010100	B010188	1	IBM101 KEYBOARD (INCLUDED WITH TERMINAL)	80009	XPFXN
	119–4899–00	B010189		1	KEYBOARD:KEYBOARD,101+NORTH AM W/PS/ECABLE (TLA510 ONLY)	80009	119489900
	119–4254–01	B010100	B010115	1	IBM101 KEYBOARD (INCLUDED WITH TERMINAL)	80009	XPFXN
	119–4899–00	B010116		1	KEYBOARD:KEYBOARD,101+NORTH AM W/PS/ECABLE (TLA520 ONLY)	80009	119489900
–10	012–1442–00			1	CA ASST INTCON:SHLD COMPST, RGB/VGA;MLD,3.75 OHM, DUAL SHLD,36 L,15 POS,HIGH DENSITY DSUB,MAKE,X3, BNC,MALE,STR,SILVER GRAY	80009	012144200

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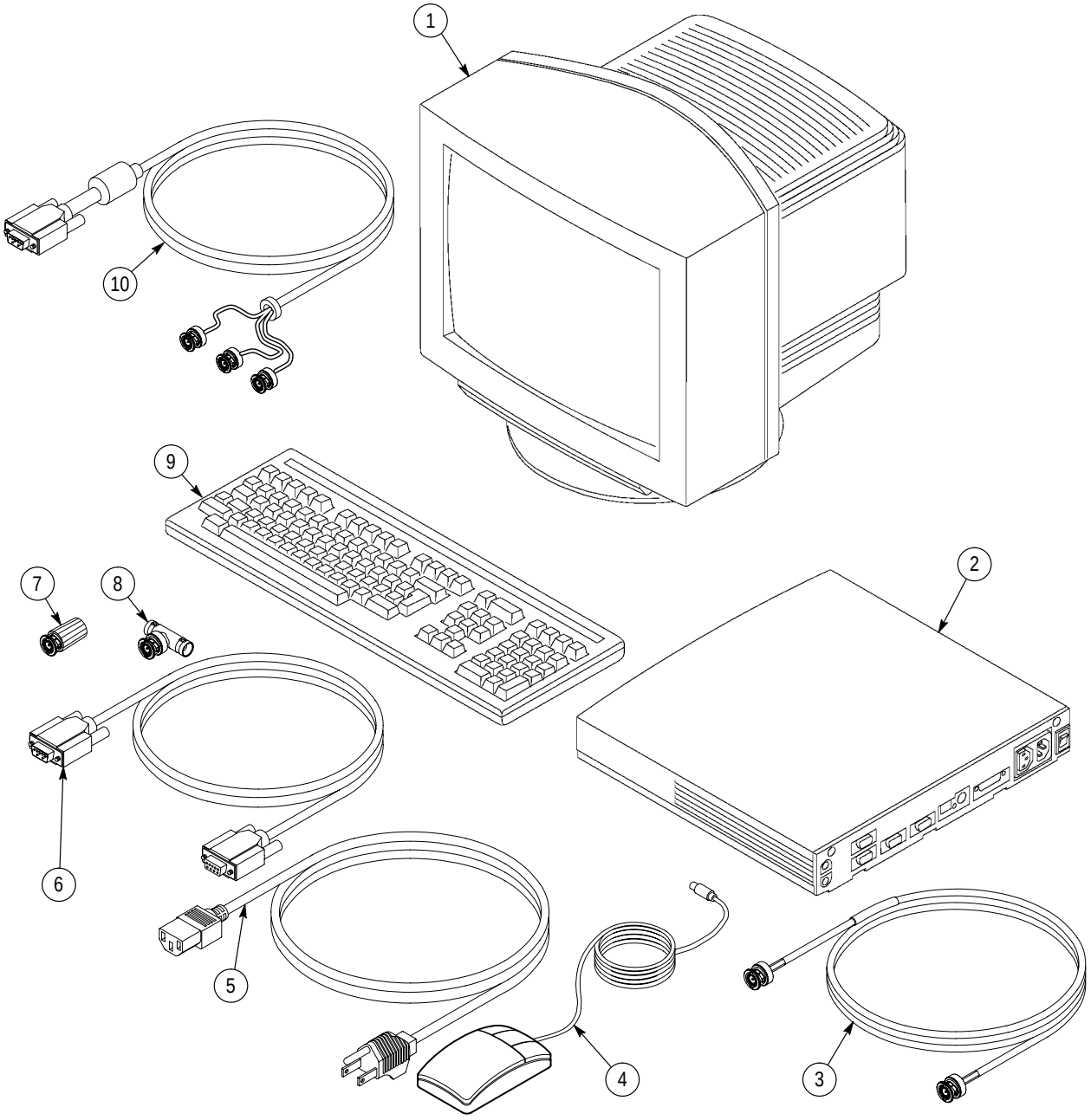


Figure 10–13: 9205XT Terminal Assembly

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Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					9206XT & 9206XT OPTION 4X		
14–1	119–5434–00			1	MONITOR,COLOR:15 INCH,0.28 DOT PITCH, PC TYPE,90/264 VAC (TLA510 92O6XT ONLY)	80009	119543400
	119–4847–00	B010155		1	MONITOR:17 INCH COLOR,MULTISCAN TYPE, 30–65KHZ HORI SCAN RANGE (TLA520 92O6XT OPTION 4X ONLY)	80009	119484700
–2	437–0452–00			1	MECH ASSY:LOGIC MODULE CABINET	80009	437045200
–3	119–4900–00			1	POWER SUPPLY:19W;5.1V 2.5A,12V 0.5A,87–264VAC 47–63HZ,IEC INPUT CONNECTOR, 183CN OUTPUT CABLE W/MINIDIN; UL, CSA,TUV, IEC	80009	119490000
–4	012–0205–00			1	CA ASSY,INTCON:COAXIAL,;RFD,(1)50 OHM,108L, BNC,MALE,BOTH ENDS	TK2469	012–0205–00
–5	012–1445–00			1	CA ASSY,INTCON:SHLD CMPST,;MLD,7,26 AWG, 10FT,9 POS,MALE,DSUB,DB9M X9 POS,FEMALE, DSUB,DB9F,W/JACK SCREWS,DUAL SHLD	80009	012144500
–6	161–0066–00			1	CA ASSY,PWR,:3,18 AWG,250V/10A,98 INCH, STR, IEC320,RCPT X NEMA 5–15P,US	80009	161006600
–7	012–1457–00			1	CABLE,INTCON:SHLD COMPST,VGA;MCD,30 INCH,3.75 OHM DUAL SHLD COAX,15 POS, HIGH DENSITY,DUB,MALE BOTH ENDS (9206XT)		
	012–1486–00			1	CABLE,VGA,SAMSUNG MONITOR,9 PIN TO 15 PIN (HIGH DENSITY)	80009	012–1486–00
	012–1442–00			1	CA ASST INTCON:SHLD COMPST, RGB/VGA;MLD,3.75 OHM, DUAL SHLD,36 L,15 POS,HIGH DENSITY DSUB,MAKE, X3,BNC,MALE,STR,SILVER GRAY (9206XT OPTION 4X)	80009	012144200
–8	103–0030–00			2	ADAPTER,CONN:BNC T MALE TO 2 FEMALE	00779	221 543–2
–9	011–0168–00				TERMINATOR BNC,;MALE,STR,50 OHM,1 WATT,1.5;, GRAY,PLASTIC (TLA 510 ONLY)	80009	ORDER BY DESC
–10	119–4330–00			1	POINTER ASSY:MOUSE FOR BEETLE	80009	119433000
–11	119–4899–01			1	KEYBOARD:KEYBOARD,101+NORTH AM W/PS/ECABLE	80009	119489900

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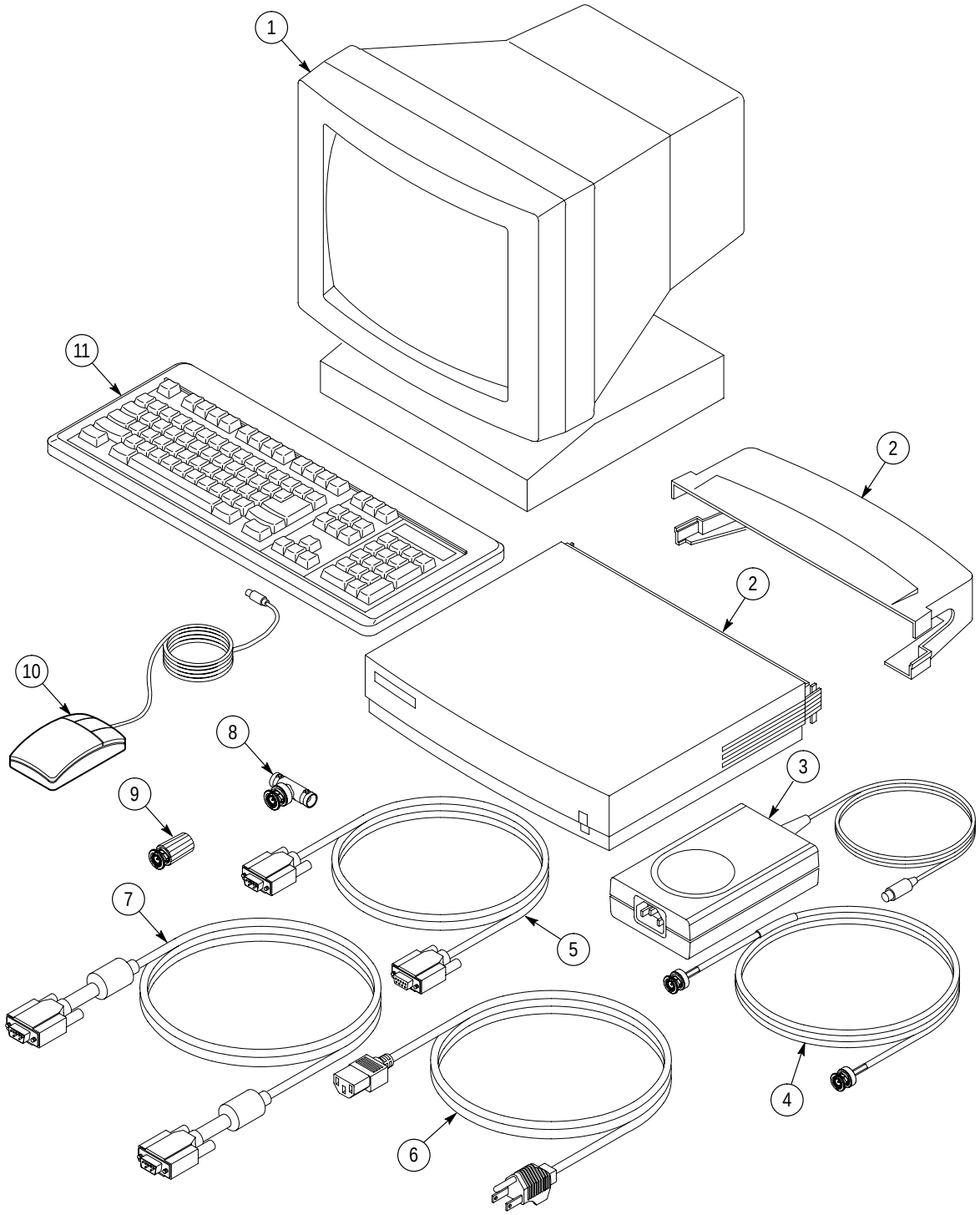


Figure 10–14: 9206XT & 9206XT Option 4X Terminal Assembly

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