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User Manual

Tektronix

VX4223
Universal Counter/Timer

070-7788-01

Please check for change information at the rear of this manual.

First Edition: September 1989
Last Revised: March 18, 1994

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Preface

Purpose of this Document

This manual provides the information necessary to install, configure, and operate the VX4223 Universal Counter/Timer.

Organization of this Manual

This manual consists of the following sections and appendices:

Section 1. General Information — Provides a brief overview of the Counter/Timer and briefly describes standard and optional accessories. Specifications provide the performance conditions of the instrument.

Section 2. Preparation for Installation — Provides the information that the installer must consider when including the VX4223 as a part of a system. Includes installation and configuration.

Section 3. Installation — Provides the information required to operate the VX4223 as a part of a larger system.

Section 4. Instrument Commands — Describes the instrument-level commands that control the VX4223.

Section 5. Maintenance — Provides performance procedures and functional checks to assure correct instrument operation.

Appendix A. VXIbus Glossary — Provides a glossary of VXIbus terms.

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Notational Conventions

This manual uses the following notational conventions:

- Regarding the active state of TTL signals:
  - An asterisk (*) following a signal mnemonic denotes that the signal is active when in the low state (typically, 0 V).
  - A signal mnemonic without a following asterisk (*) denotes that the signal is active when in the high state (typically, 2.8 — 5 V)
- Regarding the base of a number:
  - Unless otherwise noted, all numbers are assumed to be decimal (base 10).

Related Publications

The following documents on related subjects may be useful in efficient use of the Mainframe.

- *VXIbus System Specification, Version 1.3, July 14, 1989*
- *ANSI/IEEE Std 1014-1987, IEEE Standard for a Versatile Backplane Bus: VME bus*

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Operators Safety Summary

The general safety information in this summary is for both operating and servicing personnel. Specific warnings and cautions are found throughout the manual where they apply, and may not appear in this summary.

TERMS

Terms in This Manual

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to the module or other property.

Terms as Marked on Module

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the module itself.

SYMBOLS

Symbols in This Manual



This symbol indicates where applicable cautionary or other information is to be found.



This symbol indicates where special explanatory information is included in the manual. There is no caution or danger associated with the information.

Symbols as Marked on Module



DANGER High Voltage.



Protective ground (earth) terminal.



ATTENTION refer to manual.



Refer to manual before using.

Power Source

This module is intended to operate in a mainframe whose power source does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection through the grounding conductor in the power cord(s) is essential for safe operation.

Grounding the Module

This module is grounded through the grounding connector of the mainframe power cord(s). To avoid electrical shock, plug the mainframe power cord(s) into a properly wired receptacle before connecting to the module connectors. A protective ground connection through the mainframe is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only fuses specified in the module parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications required for the fuse that it replaces.

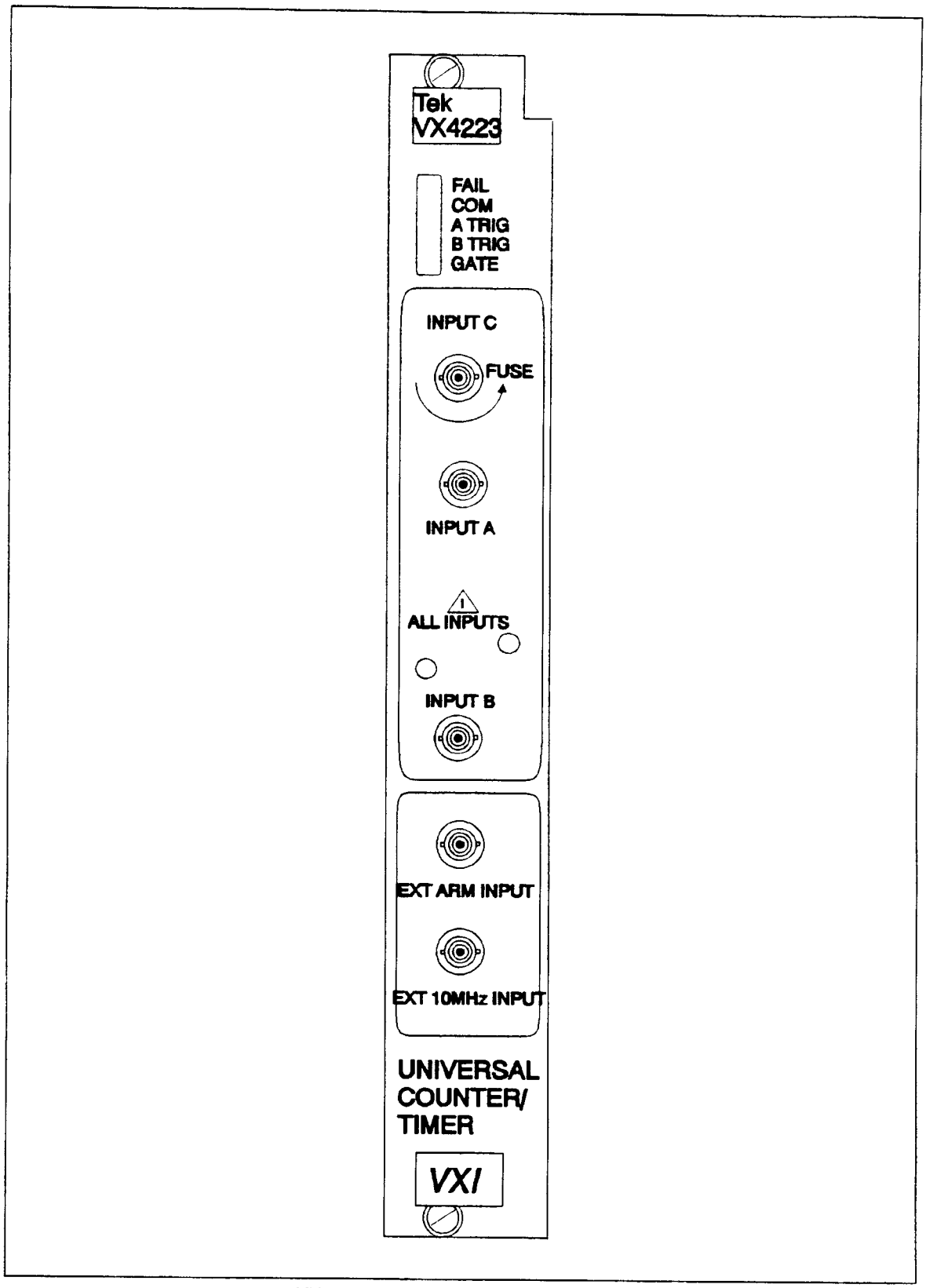
Do Not Operate in Explosive Atmosphere

To avoid explosion, do not operate the module in an explosive atmosphere.

Do Not Remove Covers or Panels

To avoid personal injury, the module covers should be removed only by qualified service personnel. Do not operate the module without covers and panels properly installed.

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VX4223 Universal Counter/Timer

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Section 1
General Information

Introduction

Description

The VX4223 Universal Counter/Timer is a microprocessor controlled instrument with high resolution measurement capabilities. The VX4223 is designed to be used under the control of a Slot 0 Resource Manager and conforms to the *VXIbus System Specification, Version 1.3. July 14, 1989.*

Measurement Capabilities

The VX4223 has the following measurement capabilities:

- Frequency A — frequency measurement up to 160 MHz using input A
- Frequency B — frequency measurement up to 100 MHz using input B
- Period A — period measurement from 6.25 ns — 1700 s using input A
- Period B — period measurement from 10 ns — 1700 s using input B
- Time Interval — time interval measurements in two modes:
  - Separate Mode — events at inputs A and B start and stop the measurement, respectively. Measurement from 5 ns — 800,000 s.
  - Common Mode — events at input A both start and stop the measurement. Measurement from 5 ns — 800,000 s.
- Total A by B — counts the number of events (up to 10^{12}) that occur at input A between events at input B
- Total B by A — up to 10^{12} events.
- Manual Totalize — counts the number of events (up to 10^{12}) between device dependent commands to open and close the counter gate
- Ratio $\frac{A}{B}$ — measures the ratio of the frequencies applied to inputs A and B
- Rise/Fall A — measures the rise or fall time (depending on the slope selected) of a signal at input A

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- Pulse Width A — measures the interval between successive rising to falling or falling to rising edges (depending on the slope selected) of a signal at input A. Measurement from 5 ns — 20 ms.

- Phase A rel B — measures the phase difference between signals at inputs A and B

Additional Capabilities

In addition to the previously described measurement capabilities, the VX4223 has the following features:

- External Arming — An additional qualification of the trigger conditions of a measurement is provided by input D, or by the VXI Trigger bus. Arming conditions are selected by the use of special functions available in the alternate command set.

- External Frequency Standard Input — The VX4223 can be locked to an external reference applied to this input. The selection of the reference frequency is under software control.

- Math Function — When the math function is active, the VX4223 returns values of the form $\frac{(Result - X) Y}{Z}$, where Result = a measured value, and the values of X and Y are constants entered by the user.

- Averaging Mode — An additional digit of resolution is added to the VX4223 output in this mode. The averaging id done over 100 measurements.

- Check Mode — The Check mode allows the user to verify that the VX4223 is operating correctly. The capabilities of the Check mode can be extended by the use of special functions.

- Special Functions — The measurement and diagnostic capabilities of the VX4223 are extended by the special functions available in the alternate command set.

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Input Signal Conditioning

The following signal conditioning capabilities are available to both input A and input B, independently:

- ac or dc coupling
- 1 MΩ or 50 Ω input impedances
- X1 or X10 input attenuations
- + or - slope triggering conditions
- Automatic or user-defined input trigger level setting. (The use of auto-trigger may cause the VX4223 to change the setting of the attenuation.)
- A switchable low pass filter that reduces the bandwidth of input A to 50 KHz (nominal)

Options

The following option is available for the VX4223:

- Option 1 — Input C. This option extends the frequency range of the VX4223 to 1.3 GHz. Input C has a fixed impedance of 50 Ω, and a bandwidth of 40 MHz — 1.3 GHz. This option also provides for a Ratio $\frac{C}{B}$ measurement.

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Specifications

Table 1-1. Environmental

Characteristic	Performance Requirement
Temperature:	
Operating	0 — 50° C
Non-operating	-40 — +70° C

Table 1-2. Electrical

Characteristic	Performance Requirement
Maximum Current Required:	
+24 Vdc	200 mA
+5 Vdc	3.1 A
-5.2 Vdc	1.6 A

Table 1-3. Mechanical

Characteristic	Description
Dimensions:	
Height	261.62 mm (10.3")
Width	30.18 mm (1.188")
Depth	349.89 mm (13.775")
Weight	≈6.6 kg (3 lbs)

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Table 1-4. Input

Note

Inputs A and B are available as front panel BNC connectors. Input A can also receive a signal from any one of the internal SUMBUS lines on the VXIbus Backplane.

Characteristic	Performance Requirement
Input A Frequency Range	dc coupled: dc —160 MHz ac coupled: 10 Hz — 160 MHz
Input B Frequency Range	dc coupled: dc — 100 MHz ac coupled: 10 Hz — 100 MHz
Input Impedance	1 MΩ or 50 Ω, selectable
Input Attenuation	X1 or X10, selectable
Sensitivity	
Sinewave (X1)	25 mV rms to 100 MHz 50 mV rms to 160 MHz
Pulse (X1)	75 mV_{pp}, at 5ns pulse width
Dynamic Range (X1)	36 db to 50 MHZ (75 mV_{pp} — 5 V_{pp}) 30 db to 100 MHz (75 mV_{pp} — 2.5 V_{pp}) 24 db to 160 MHz (150 mV_{pp} — 2.5 V_{pp})
Maximum Input	
50 Ω	5 V rms
1 MΩ	X1: 260 V (dc + ac rms), dc — 2 KHz, decreasing to 5 V rms at 100 KHz and above X10: 260 V (dc + ac rms), dc — 20 KHz, decreasing to 50 V rms at 100 KHz and above
Low Pass Filter	50 KHz (nominal), Input A only
Crosstalk	<-36 db between channels, measured at 100 MHz with 50 Ω input impedance
Input C (Option 1):	
Frequency Range	40 MHz — 1.3 GHz
Sensitivity (sinewave)	25 mV rms to 1 GHz 50 mV rms to 1.3 GHz
Dynamic Range	40 db to 1 GHz
Input Impedance	50 Ω (nominal)
VSWR	<2:1 at 1 GHz
Maximum Input	
Operating	1 V rms
Without damage	7 V rms

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Table 1-5. Trigger

Characteristic	Performance Requirement
Trigger Level Range	X1: ±5.1 V in 20 mV steps (automatic or manual selection) X10: ±51 V in 200 mV steps (automatic or manual selection)
Trigger Level Accuracy	X1: ±1% of trigger level ±30 mV X10: ±1% of trigger level ±300 mV
Auto-trigger Minimum Amplitude	150 mV_{p-p}
Auto-trigger Level Accuracy	+5 through -4 V: ±30 mV relative to displayed reading -4 through -5.1 V: ±100 mv relative to displayed reading
Auto-trigger Frequency Range	dc, 50 Hz — 100 MHz (typically to 160 MHz)

Definitions

The following definitions apply to terms used in Table 1-6:

Trigger Error

$$\frac{SQR\ (e_i^{\,2} + e_n^{\,2})}{\textit{Input slew rate at trigger point}}$$

where:
e_i = input amplifier rms noise (typically 150 µV, 450 µV maximum in a 160 MHz bandwidth)
e_n = input signal rms noise in a 160 MHz bandwidth

Trigger Level Timing Error

$$\pm\frac{^1/_2\ \textit{Hysteresis Band}}{\textit{Input Slew Rate at START Trigger Point}} + \frac{\textit{Trigger Level Accuracy}}{\textit{Input Slew Rate at STOP Trigger Point}}$$

Where:
Hysteresis Band is nominally 25 mV

Trigger Level Setting Error

$$\pm\frac{\textit{Trigger Level Accuracy}}{\textit{Input Slew Rate at START Trigger Point}} + \frac{\textit{Trigger Level Accuracy}}{\textit{Input Slew Rate at STOP Trigger Point}}$$

Differential Channel Delay Error

The difference in propagation times between signals applied to input A and B.

Time Base Error

The fractional deviation of the time base frequency from 10 MHz due to aging, temperature, voltage variations, etc.; determined by the reference frequency used by the VX4223 in the VXI Mainframe. The default reference frequency is the VXIbus CLK10 signal.

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Resolution and Gate Time

Gate time is related to the resolution selected in the frequency, period, ratio, and check functions as follows:

Resolution (number of selected digits) in Frequency, Period, Ratio, and Check[a]	Gate Time
9 = overflow	10 s
9	1 s
8	100 ms
7	10 ms
6	1 ms
5[b]	1 ms
4[b]	1 ms
3[b]	1 ms

[a]The most significant digit is permitted to exceed the resolution by 1 digit, providing a 10% overrange. This precludes unnecessary shifting of digits.
[b]Measurements of frequency, period, ratio, and check are averaged when these gate times are set.

Gate time is also programmable in increments of 25.6 µs — 99.999 s. The default state is 100 ms Gate Time and 8 digits of resolution. Note that the Gate Time can be extended by:

- one period of the input signal on Frequency B and Ratio $\frac{A}{B}$.
- two periods of the input signal on Frequency A and Period A.

When setting the resolution by programming the number of digits, use the following formula to determine the value of the Least Significant Digit (LSD):

$$LSD = F \times 10^{-D}$$

Where:
F = Frequency
D = Number of digits rounded up to the next decade.

Gate Out

A TTL compatible signal coincident with the measurement gate is accessible to any one of the TTLTRG bus lines. The signal is low when the gate is open.

Miscellaneous

The resolution of phase and totalize is determined by the input signal.

Time interval, rise/fall time, and pulse width measurements have the resolution determined by both the input signal and the resolution set.

Resolution is programmable from 3 — 9 digits, but the minimum LSD that the counter will achieve is 1 ns, regardless of programmed gate time or resolution in time interval mode.

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Table 1-6. Measurement

Characteristic	Performance Requirement
Frequency A & B	
Range	Input A: 6×10^{-4} Hz — 160 MHz Input B: 3×10^{-4} Hz — 100 MHz
Least Significant Digit (LSD)	$\frac{1\ ns}{Gate\ Time} \times Frequency$
Resolution	$\pm(2 \times LSD) \pm 1.4 \times \frac{Trigger\ Error}{Gate\ Time} \times Frequency$
Accuracy	±Resolution ±Timebase Error x Frequency
Frequency C (Option 1)	
Range	40 MHz — 1.3 GHz
Least Significant Digit (LSD)	$\frac{1\ ns}{Gate\ Time} \times Frequency$
Resolution	$\frac{1\ ns}{Gate\ Time} \times Frequency$
Accuracy	±Resolution ±Timebase Error x Frequency
Period A	
Range	6.25 ns — 1.7×10^{3} s
Least Significant Digit (LSD)	$\frac{1\ ns}{Gate\ Time} \times Period$
Resolution	$\pm(2 \times LSD) \pm 1.4 \times \frac{Trigger\ Error}{Gate\ Time} \times Period$
Accuracy	±Resolution ±Timebase Error x Period
Time Interval	
Separate Inputs	Input A start / Input B stop Input B start / Input A stop
Common Inputs	Input A start / Input B stop
Range	- 2 ns — 8×10^{5} s
Trigger Slopes	Start, + or - Stop, + or -
Least Significant Digit (LSD)	1 ns (100 ps with Average mode)
Resolution	±LSD ±1 ns ±Start Trigger Error ±Stop Trigger Error
Accuracy	±Resolution ±(Timebase Error x Time Interval) ±Trigger Level Setting Error
Totalize A by B	
Range	0 — 100 Mhz; 1 — 10^{12} - 1 events
Pulse Width	5 ns minimum at trigger points
Maximum Rate	10^{8} events / s
Start / Stop	Input B
Least Significant Digit (LSD)	±1 count
Resolution	LSD
Accuracy	LSD

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Table 1-6. Measurement (cont.)

Characteristic	Performance Requirement
Frequency Ratio $\frac{A}{B}$	
Range, Inputs A and B	dc — 100 MHz
Least Significant Digit (LSD)	$\frac{10 \times Ratio}{F_A \times Gate\ Time}$
Resolution	$\pm LSD \pm \frac{Trigger\ Error\ B}{Gate\ Time}$
Accuracy	$\pm LSD \pm \frac{Trigger\ Error\ B}{Gate\ Time}$
Frequency Ratio $\frac{C}{B}$ (Option 1)	
Input C	40 MHz — 1.3 GHz
Input B	dc — 100 MHz
Least Significant Digit (LSD)	$\frac{640 \times Ratio}{F_C \times Gate\ Time}$
Resolution	$\pm LSD \pm \frac{Trigger\ Error\ B}{Gate\ Time}$
Accuracy	$\pm LSD \pm \frac{Trigger\ Error\ B}{Gate\ Time}$
Rise / Fall Time	
Range	20 ns — 20 ms
Rise Time	Start: + slope, 10% trigger point Stop: + slope, 90% trigger point
Fall Time	Start: - slope, 90% trigger point Stop: - slope, 10 % trigger point
Input Channel	Input A
Minimum Pulse Height	500 mV_{pp}
Minimum Pulse Width	20 ns at signal peaks
LSD Displayed	1 ns (100 ps using Averaging mode)
Resolution	±LSD ±1 ns ±Start Trigger Error ±Stop Trigger Error
Accuracy	±Resolution ±Trigger Level Timing Error ±Trigger Level Setting Error at 10% Trigger Point ±Trigger Level Setting Error at 90% Trigger Point ±2 ns ± (Timebase Error x Rise / Fall Time)

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Table 1-6. Measurements (cont.)

Characteristic	Performance Requirement
Pulse Width	
Range	5 ns — 20 ms
Positive Pulse Width	Start: + slope, 50% trigger point Stop: - slope, 50% trigger point
Negative Pulse Width	Start: - slope, 50% trigger point Stop: + slope, 50% trigger point
Input Channel	Input A
Minimum Pulse Height	150 mV_{pp}
Least Significant Digit (LSD)	1 ns (100 ps using Averaging mode)
Resolution	±LSD ±1 ns ±Start Trigger Error ±Stop Trigger Error
Accuracy	±Resolution ±Trigger Level Timing Error ±Trigger Level Setting Error ±2 ns ± (Timebase Error x Pulse Width)
Phase A rel B	
Range	0.10 — 360°
Least Significant Digit (LSD)	0.1° to 1 MHz 1° to 10 MHz 10° to 100 MHz
Resolution	$\pm LSD \pm \frac{TI\ Resolution \times 360°}{Period\ A}$
Time Interval Delay	
Time Interval	Programmable 200 µs — 800 ms
Resolution	25 µs
Accuracy	±50 µs ±0.1% of reading
Peak Signal Measurement	Indicates the peak maximum, peak minimum, or dc value of the measurement signal.
Frequency Range	dc, 50 Hz — 20 MHz (usable to 100 MHz)
Dynamic Range	150 mV — 51 V_{pp}
Resolution	X1: 20 mV
Accuracy (sinewave)	±6% of peak-to-peak voltage ±50 mV
Accuracy (dc)	±1% of reading ±40 mV
Averaging Mode	Can be applied to all functions except Totalize, Adds an extra digit of resolution.
Sample Size	100
Math	Can be applied to all counting/timing measurement functions except Trigger Level and Gate Time.
Result	$\frac{(Reading - X)\ Y}{Z}$ Where X, Y, and Z are constants entered by the user.
Constant Range	$\pm 1 \times 10^{-9}$ — $\pm 1 \times 10^{9}$

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Table 1-6. Measurements (cont.)

Characteristic	Performance Requirement
Gate Time	
Range	200 µs — 99.9 s
Resolution	25.6 µs
External Standard Input	
Frequency	10 MHz
Level	Minimum, 100 mV rms; maximum, 10 V rms
Maximum Input Level	400 V peak to 500 Hz, decreasing to 10 V rms at ≥30 KHz
Impedance	1 KΩ (nominal) for signals < 1 V peak-to-peak, decreasing to 500 Ω (nominal) for signals 10 V peak-to-peak and above. ac coupled.
External Arming	
Applicability	All functions, except phase, pulse width, and rise/fall time
Input Signal	TTL, available from front panel BNC or eight TTLTRG lines, selected under program control
Arming Mode	1. Start - Off[a] Stop - Off[a] 2. Start - Positive Stop - Off[a] 3. Start - Negative Stop - Off[a] 4. Start - Positive Stop - Positive 5. Start - Negative Stop - Positive 6. Start - Positive Stop - Negative 7. Start - Negative Stop - Negative [a]Off state indicates the counter's internal arm/stop is used
Minimum Start/Stop Arm Period	100 ns

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Section 2
Preparation for Installation

Interrupt Level and Logical Address Setting

The VX4223 is shipped from the factory with the interrupt level set to 2 and the logical address set to 03.

The interrupt level and logical address of the VX4223 can be changed in the following manner:

Interrupt Level

1. Remove the three screws holding the circuit board cover and remove the cover to expose the circuit board.
2. Set switch S1 to the binary equivalent of the interrupt level desired (0 — 7). The OFF positions of switch S1 correspond to binary 1.
3. Replace the cover and cover screws.

Logical Address

1. Remove the three screws holding the circuit board cover and remove the cover to expose the circuit board.
2. Set switch S2 to the binary equivalent of the logical address desired (1 — 255h). The OFF positions of switch S2 correspond to binary 1.
3. Replace the cover and cover screws.

Power-Up

When power is applied to the Mainframe that the Counter/Timer is installed in, the SYSFAIL LED on the front of the Counter/Timer should illuminate, then extinguish after a few seconds to show that the Power-Up Self Test has successfully completed. When the SYSFAIL LED extinguishes, the Counter/Timer is ready for use.

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Configuring the Backplane Jumpers

NOTE

The following instructions pertain to Tektronix Mainframes. If you are installing the Counter/Timer in a different mainframe, refer to the Instruction Manual for that mainframe for the correct jumper strap numbers.

VXIbus mainframes contain daisy-chain jumper straps for the Bus Grant (BG0 — BG3) and Interrupt Acknowledge (IACK) signals. Tektronix Mainframes are shipped with all jumpers installed. All jumper straps must be removed for slots that have cards installed.

NOTE

If your are using a Tektronix Mainframe, the names of the jumper straps (BG0 — BG3 & IACK) are printed on the circuit board facing the front of the mainframe. These jumpers are accessed from the front of the mainframe.

Remove all jumper straps to the immediate left of the slot in which the Counter/Timer will be installed. Retain the straps for possible future reconfiguration.

The Bus Grant jumper straps and their associated component numbers are listed in Table 2-1; the Interrupt Acknowledge jumper straps and their associated component numbers are listed in Table 2-2.

CAUTION

A C-size module can be damaged if installed wrong. Use care when installing modules in a VX1500 D-size mainframe. We recommend using a C-size to D-size adapter (Tek part number 014-0070-00) which should be installed in the mainframe P3 (bottom) connector. When installing the module, insert the module top edge into the mainframe top guide for the slots(s) where the module is to be installed, and insert the module bottom edge into the adapter card guide. Make sure the module is fully seated into the mainframe P1 (top) and P2 (middle) connectors.

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Table 2-1. Bus Grant Jumper Straps

Slot	BG0	BG1	BG2	BG3
1	J1011	J1012	J1013	J1014
2	J1021	J1022	J1023	J1024
3	J1026	J1027	J1028	J1029
4	J1031	J1032	J1033	J1034
5	J1036	J1037	J1038	J1039
6	J1041	J1042	J1043	J1044
7	J1046	J1047	J1048	J1049
8	J1051	J1052	J1053	J1054
9	J1056	J1057	J1058	J1059
10	J1061	J1062	J1063	J1064
11	J1066	J1067	J1068	J1069
12	J1071	J1072	J1073	J1074

Table 2-2. Interrupt Acknowledge Jumper Straps

Slot	IACK Connector
0	J2010
1	J2015
2	J2020
3	J2025
4	J2030
5	J2035
6	J2040
7	J2045
8	J2050
9	J2055
10	J2060
11	J2065
12	J2070

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Section 3
Installation

Introduction

The VX4223 is designed to be controlled remotely over the VXIbus. There are no local or manual controls on the Counter/Timer.

Power-Up Default State

The VX4223 powers up in the following state:

Feature	Power-Up Default
Trigger Levels	Manual, set to 0.00 V
Input Coupling	ac, inputs A and B
Measurement Mode	Frequency A
Time Interval Delay	200 µs, disabled
Gate Time	100 ms
Input Impedance	1 MΩ, inputs A and B
Input Attenuation	X1
Math Constants	X = 0, Y = 1, Z = 1, Math disabled
Input Mode	Separate inputs
Input A Low Pass Filter	Off
Input A Trigger Slope	+
Input B Trigger Slope	+
Hold	Off
SRQ	Off

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Section 4
Instrument Commands

Introduction

The VX4223 is controlled by codes sent through the Slot 0 Resource Manager. All command strings must be terminated with one of the following:

- A carriage return/line feed pair <CRLF>
- A line feed <LF>
- A line feed with *GPIB EOI* asserted
- A *GPIB EOI* on the last character of the command string. (This causes the Resource Manager to set the END bit.)

Gate Time and Resolution Control

The gate time and resolution of the VX4223 can be changed from the default settings by the command codes SGT*n* and SRS*m*, respectively. The use of either command can affect the setting of the other. The relationship between gate time and resolution is as follows:

Digits of Resolution	Gate Time
10	10 s
9	1 s
8	100 ms
7	10 ms
6	1 ms
5	1 ms
4	1 ms
3	1 ms

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Resolution is defined as the number of significant digits in the measurement output string for all measurement modes except Time Interval, Rise/Fall Time, and Pulse Width.

If a reading is made with a reduced resolution or gate time, the measurement output string is not truncated, but digits are shifted to the right, causing more leading zeros to be output.

The values of the gate time and resolution currently in use can be recalled by the command codes RGT and RRS, respectively.

The maximum number of digits that can be output by the VX4223 in any of the Frequency Ratio modes is seven, regardless of the resolution set.

In the Phase A rel B Measurement mode, up to four significant digits are output for frequencies up to 1 MHz; up to three significant digits are output for frequencies above 1 MHz. For frequencies above 10 MHz, the resolution is 10 degrees with a lower case "o" output as the least significant digit.

Special Functions

Special functions are organized by decades, one for each of the nine mantissa output string digits. One special function from each decade can be entered into the special function register, but only the second digit of the special function number is indicated by the position in the output string. The default state has zeros entered in all positions. The special function output string is generated in response to the RSF command code.

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Output Message Format

The output strings generated by the VX4223 are 21 bytes long and of the following form:

<aa><±><nnnnnnnnnnnn><E><±><mm><cr><lf>

Where:

<aa> = a 2 byte header that describes the measurement mode that the VX4223 is in, or the type of data recalled as shown in Tables 4-1 and 4-2.

Note

The <aa> header can be removed by the use of the S81 command code.

<±> = the polarity of the measurement result

<nnnnnnnnnnnn> = numerical data (n = 0 — 9 or a decimal point). Leading zeros will be added to ensure that 11 bytes are output, if required. The decimal point can float to any point in this string except the first.

<E> = an exponent indicator.

<mm> = the exponent (m = 0, 3, 6, or 9) the <E> is raised to.

<cr><lf> = a carriage return line feed.

Table 4-1. Measurement Mode Output String Headers

Measurement Mode	Output String Header
Frequency A	FA
Frequency B	FB
Frequency C (Option 1)	FC
Period A	PA
Time Interval A - B	TI
Totalize A by B	TA
Ratio $\frac{A}{B}$	RA
Ratio $\frac{C}{B}$ (Option 1)	RC
Rise Time A	RT
Fall Time B	FT
Positive Pulse Width A	PW
Negative Pulse Width A	NW
Phase A rel B	PH

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Table 4-2. Recalled Data Output String Headers

Recalled Data	Output String Header
Unit Type	UT
Resolution	RS
Trigger Level A	LA
Trigger Level B	LB
Math Constant X	MX
Math Constant Y	MY
Math Constant Z	MZ
Delay Time	DT
Special Function	SF
Master Software Issue Number	MS
VXI Processor Software Issue Number	GS
Gate Time	GT

Error Messages

To obtain the status of the VX4223, a serial poll must be taken. If bit 6 of the status byte = 1, an error condition is present. The specific error is identified by bits 1, 2 and 3.

Table 4-3 shows the error codes and gives an explanation of each.

Table 4-3. Error Codes

Error	Explanation
01	Signals of different frequencies used in phase measurement mode
02	Measurement result too large
03	Internal counter overflow
04	Numerical entry error
05	GPIB syntax error
50[a]	Check mode error
51[a]	X1/X10 input A relay check failure
52[a]	50 Ω/1 MΩ input A relay check failure
53[a]	ac/dc coupling input A relay check failure
54[a]	Input A low pass filter relay check failure
55[a]	COM A relay check failure
56[a]	X1/X10 input B relay check failure
57[a]	50 Ω/1 MΩ input B relay check failure
58[a]	ac/dc coupling input B relay check failure

[a]These error codes are only used in Check mode, and can be read over the GPIB.

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Code List

Code	Purpose
A0	Selects the front panel connector as the input A signal source
A1	Selects the SUMBUS as the input A signal source
A2	Connects the timebase reference to input A
AAC	Selects ac coupling for input A
AAD	Disables X10 attenuation for input A
AAE	Enables X10 attenuation for input A
AAU	Selects Auto-trigger mode for input A
ADC	Selects dc coupling for input A
AE	Enables the Averaging mode for 100 samples
AFD	Disables the input A low pass filter
AFE	Enables the input A low pass filter
AHI	Sets the impedance of input A to 1 MΩ
ALI	Sets the impedance of input A to 50 Ω
AMN	Selects Manual Trigger mode for input A
ANS	Sets the input A trigger to negative slope
APS	Sets the Input A trigger to positive slope
B0	Selects the CLK10 signal from the VXI Mainframe as the reference frequency
B1	Selects EXT STD INPUT as the reference frequency
BAC	Selects ac coupling for input B
BAD	Disables X10 attenuation for input B
BAE	Enables X10 attenuation for input B
BAU	Selects Auto-trigger mode for input B
BCC	Selects Common mode for inputs A and B
BCS	Selects Separate mode for inputs A and B
BDC	Selects dc coupling for input B
BHI	Sets the impedance of input B to 1 MΩ
BLI	Sets the impedance of input B to 50 Ω
BMN	Selects Manual Trigger mode for input B
BNS	Sets the input B trigger to negative slope
BPS	Sets the input B trigger to positive slope
CK	Selects Check mode
D0	Enables the Gate Out signal on connector P2 A23 (TTLTRG0)
D1	Enables the Gate Out signal on connector P2 C23 (TTLTRG1)
D2	Enables the Gate Out signal on connector P2 A24 (TTLTRG2)
D3	Enables the Gate Out signal on connector P2 C23 (TTLTRG3)
D4	Enables the Gate Out signal on connector P2 C23 (TTLTRG4)
D5	Enables the Gate Out signal on connector P2 A23 (TTLTRG5)
D6	Enables the Gate Out signal on connector P2 A23 (TTLTRG6)
D7	Enables the Gate Out signal on connector P2 A23 (TTLTRG7)
D8	Disables the Gate Output
DD	Disables Time Interval Delay
DE	Enables Time Interval Delay
FA	Selects Frequency A Measurement mode
FB	Selects Frequency B Measurement mode
FC	Selects Frequency C Measurement mode (Option 1 only)
FT	Selects Fall Time A Measurement mode

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Code	Purpose
IP	Sets the VX4223 to its default state (Refer to Section 3 for settings)
MD	Disables the Math function
ME	Enables the Math function
NA	Disables Averaging mode
NW	Selects Negative Pulse Width A Measurement mode
PA	Selects Period A Measurement mode
PH	Selects Phase A Relative to B (A rel B) Measurement mode
PW	Selects Positive Pulse Width A Measurement mode
Q0	Unconditionally inhibits the GPIB SRQ assertion
Q1	Selects assertion of the GPIB SRQ upon detecting an error
Q2	Selects assertion of the GPIB SRQ upon measurement ready
Q3	Selects assertion of the GPIB SRQ upon measurement or upon detecting an error
Q4	Selects assertion of the GPIB SRQ upon a frequency standard change
Q5	Selects assertion of the GPIB SRQ upon a frequency standard change or upon detecting an error
Q6	Selects assertion of the GPIB SRQ upon a frequency standard change or a measurement ready
Q7	Selects assertion of the GPIB SRQ upon a frequency standard change , upon detecting an error, or upon a measurement ready
R0	Enables the Input Arm Receiver on connector P2 A23 (TTLTRG0)
R1	Enables the Input Arm Receiver on connector P2 C23 (TTLTRG1)
R2	Enables the Input Arm Receiver on connector P2 A24 (TTLTRG2)
R3	Enables the Input Arm Receiver on connector P2 C24 (TTLTRG3)
R4	Enables the Input Arm Receiver on connector P2 A26 (TTLTRG4)
R5	Enables the Input Arm Receiver on connector P2 C26 (TTLTRG5)
R6	Enables the Input Arm Receiver on connector P2 A27 (TTLTRG6)
R7	Enables the Input Arm Receiver on connector P2 C27 (TTLTRG7)
R8	Enables the external arm input on the front panel (Input D)
RA	Selects Ratio $\frac{A}{B}$ Measurement mode
RC	Selects Ratio $\frac{C}{B}$ Measurement mode (Option 1 only)
RDT	Recalls the arming delay time
RE	Resets the measurement
RF	Reads the total so far
RGS	Recalls the VXI processor software issue number
RGT	Recalls the gate Time
RLA	Recalls the input A trigger level
RLB	Recalls the input B trigger level
RM*n*	Recalls memory setting *n* (0 — 9). Sets the VX4223 to a previously stored configuration (using the SM*n* code). Note that all stored information is lost upon powering down the VX4223.
RMS	Recalls the master software issue number
RMX	Recalls Math constant X
RMY	Recalls Math constant Y
RMZ	Recalls Math constant Z

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Code	Purpose
RRS	Recalls the measurement resolution
RSF	Recalls a special function number
RT	Selects Rise Time A Measurement mode
RUT	Recalls unit type
S10	Selects Arming mode. Start: Internal; Stop: Internal (used with code SFE)
S11	Selects Arming mode. Start: External +ve — Stop: Internal (used with code SFE)
S12	Selects Arming mode. Start: External -ve — Stop: Internal (used with code SFE)
S15	Selects Arming mode. Start: External +ve — Stop: External +ve (used with code SFE)
S16	Selects Arming mode. Start: External +ve — Stop: External -ve (used with code SFE)
S17	Selects Arming mode. Start: External -ve — Stop: External +ve (used with code SFE)
S18	Selects Arming mode. Start: External -ve — Stop: External -ve (used with code SFE)
S20	Cancels S21 (used with code SFE)
S21	Interchanges inputs A and B (used with code SFE)
S30	Selects continuous auto-trigger measurement (cancels S31) (used with code SFE)
S31	Selects single-hot auto-trigger measurement (used with code SFE)
S50	Cancels +Peak or -Peak Measurement modes (cancels S51 or S52, respectively) (used with code SFE)
S51	Selects +Peak Measurement mode (used with code SFE)
S52	Selects -Peak Measurement mode (used with code SFE)
S60	Selects Totalize A by B Measurement mode (cancels S61) (used with code SFE)
S61	Selects Manual Totalize Measurement mode (used with code SFE)
S70	Selects Check mode (cancels S72 — S78) (used with code SFE)
S72	START TEC short continuous calibration (used with code SFE)
S73	START TEC long continuous calibration (used with code SFE)
S74	STOP TEC short calibration (used with code SFE)
S75	STOP TEC long calibration (used with code SFE)
S76	Checks input A and B DACs by continuously ramping (used with code SFE)
S77	Checks the input A relay (requires a 10 MHz input signal) (used with code SFE)
S78	Checks the input B relay (used with code SFE)
S80	Enables a 2 character function header on the output string (cancels S81) (used with code SFE)
S81	Disables a 2 character heading on the output string (used with code SFE)
SDT*n*	Sets the arming delay time to *n* seconds. The permissible range of *n* is 99.999s > *n* > 200 µs.
SFD	Disables special functions (default)
SFE	Enables special functions (used with codes S10 — S81)
SGT*n*	Sets Gate Time to *n* seconds. (Refer to Section 1 for a description of the relationship between resolution and gate time.)

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Code	Purpose
SLA*v*	Sets the input A trigger level to *v* volts. The permissible range of *v* is -5.1 — +5.1 V in increments of 20 mV for X1 attenuation, or -51 — +51 V in increments of 200 mV for X10 attenuation.
SLB*v*	Sets the input B trigger level to *v* volts. The permissible range of *v* is -5.1 — +5.1 V in increments of 20 mV for X1 attenuation, or -51 — +51 V in increments of 200 mV for X10 attenuation.
SM*n*	Stores the present configuration in the VX4223 RAM memory. The permissible range of *n* is 0 — 9. Stored settings are recalled by the use of the RM*n* code. Note that all stored settings are lost upon power-down.
SMX*a*	Sets Math constant X to value *a*. The permitted ranges of values for *a* are $1 \times 10^{10} > a \geq 1 \times 10^{-9}$, $-1 \times 10^{-9} \geq a > -1 \times 10^{10}$, and 0.
SMY*a*	Sets Math constant Y to value *a*. The permitted ranges of values for *a* are $1 \times 10^{10} > a \geq 1 \times 10^{-9}$, $-1 \times 10^{-9} \geq a > -1 \times 10^{10}$, and 0.
SMZ*a*	Sets Math constant Z to value a. The permitted ranges of values for *a* are $1 \times 10^{10} > a \geq 1 \times 10^{-9}$ and $-1 \times 10^{-9} \geq a > -1 \times 10^{10}$. a can be set to 0, but an error message will be output when the Math function is enabled.
SRS*m*	Sets the measurement resolution to *m* (an integer between 3 and 10).
T0	Selects Continuous Measurement mode
T1	Selects Single Shot Measurement mode
T2	Starts Manual Totalize or trigger measurement cycle
T3	Stops Manual Totalize
TA	Selects Total A by B Measurement mode
TI	Selects Time Interval Measurement mode

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Section 5
Maintenance

Performance Verification Procedures

This section provides the performance verification procedures (PVPs) necessary to verify that the VX4223 conforms to its published specifications. It is recommended that these procedures are carried out at a minimum interval of one year.

The following conditions must be kept throughout the Verification Procedure.

a) The instrument covers must be fitted.

b) The ambient temperature must be 23 °C ± 2 °C.

c) The counter must be allowed to warm up for at least one hour before commencing the PVPs.

In the following procedures, a stable count is defined as one that does not vary by more than plus or minus one count in the least significant digit of resolution between successive readings.

Note that these procedures verify the measurement circuitry of the counter, but not the absolute accuracy. Absolute accuracies must be calculated from the expressions given in the Specifications section of this manual after finding the timebase errors that apply to the external frequency standard or CLK10 signals used by the counter.

Required Test Equipment

- Signal Generator, 10 kHz to 1.3 GHz, Racal-Dana 9087
- Function Generator, DC to 10 kHz, HP 3325
- DC Voltage Calibrator, Fluke 332A
- Digital Multimeter, ± 5% accuracy, DC to 100 kHz, Racal-Dana 5001
- RF Millivoltmeter, Racal-Dana 9303
- Various RF connectors, adaptors, T-pieces, and coaxial cables, as required

NOTE

In the following procedures, it is recommended that all signal levels are measured with the Digital Multimeter or RF Millivoltmeter, as appropriate, and adjusted to give a level as close to its nominal value as can be achieved before being applied to the counter.

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Diagnostic Special Functions

It is recommended that the following Special Functions are enabled in turn in the check mode and the results noted before commencing the Performance Verification Procedures for the counter. Successful completion of this procedure demonstrates that the VX4223 measurement circuitry is functioning correctly. Table 5-1 presents the commands, function names, and expected results of using the commands.

Table 5-1. Enabling the Special Functions in Check Mode

Command	Diagnostic Special Functions	Expected Result
CK	Enter Check Mode	
SFE	Enable Special Functions	
S70	Frequency Measurement Check	CK + 10.000000000e + 06
S72	START TEC Short Calibration	(S73 result) / 2, tolerance + 20, -40
S73	START TEC Long Calibration	800 ± 220
S74	STOP TEC Short Calibration	S75 result) / 2, tolerance + 20, -40
S75	STOP TEC Long Calibration	800 ± 220
S77	Input A relays check	CK + 51 ± 10
S78	Input B relays check	CK + 56 ± 10

Check mode Special Functions S72 - S78 may be exited by selecting S70 (Basic Check function) or any other measurement mode.

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Input A Sensitivity Test

1. Set the VX4223 to its home state. Select 50 ohms input impedance for input A and external frequency standard (command string **IP ALI B1**).

2. Connect the Function Generator to the VX4223 as shown in Figure 5-1.

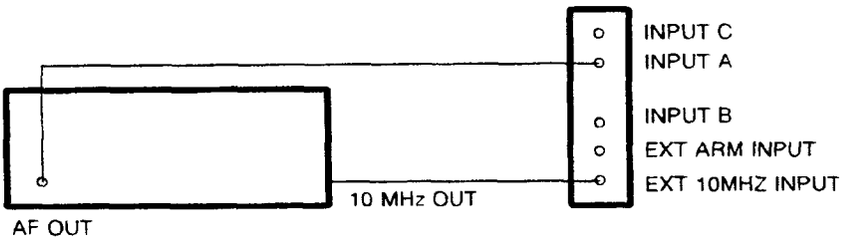


Figure 5-1. Input A Low Frequency Sensitivity Test Configuration

3. Apply the frequencies given in Table 5-2 to the counter. Verify that the VX4223 gives a stable reading within the tolerances given at less that the signal levels given.

Table 5-2. Input A Sensitivity Low Frequency Test

Command String	Frequency	Signal level	Resolution	Tolerance
IP ALI B1	10 Hz	25 mV rms	8	± 1 Hz
IP ALI B1	5 kHz	25 mV rms	8	± 0.1 Hz
IP ALI B1	10 kHz	25 mV rms	8	± 0.1 Hz

4. Disconnect the test equipment.

5. Connect the Signal Generator to the VX4223 as shown in Figure 5-2.

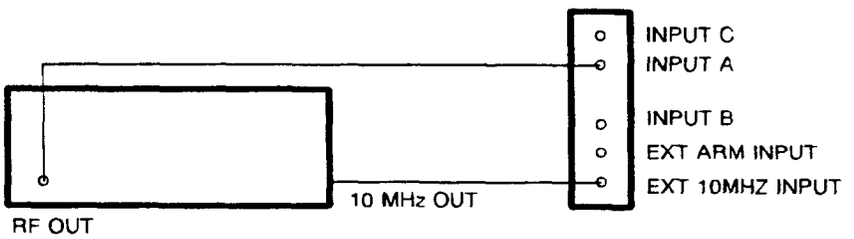


Figure 5-2. Input A High Frequency Sensitivity Test Configuration

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6. Set the VX4223 measurement resolution to the values given in Table 5-3 and apply the frequencies given to the counter's input A. Verify that the VX4223 gives a stable reading within the tolerances given at less than the signal level given.

Table 5-3. Input A Sensitivity High Frequency Performance Limits

Command String	Frequency	Signal level	Resolution	Tolerance
IP ALI B1	100 kHz	25 mV rms	8	± 0.1 Hz
IP ALI B1	10 MHz	25 mV rms	8	± 1 Hz
SRS9	100 MHz	25 mV rms	9	± 1 Hz
SRS9	160 MHz	50 mV rms	9	± 1 Hz

7. Disconnect the test equipment.

Input B Sensitivity Test

1. Set the VX4223 to its home state. Select 50 ohms input impedance for input B, Frequency B as the measurement mode and external frequency standard (command string **IP FB B1 BLI**).

2. Connect the Function Generator to the VX4223 as shown in Figure 5-3.

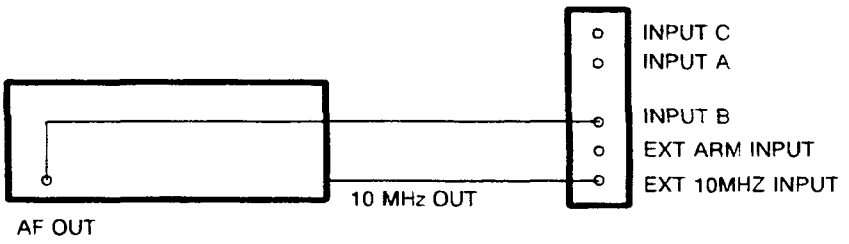


Figure 5-3. Input B Low Frequency Sensitivity Test Configuration

3. Apply the frequencies given in Table 5-4 to the counter's input B. Verify that the VX4223 gives a stable reading within the tolerance given at less than the signal level given.

Table 5-4. Input B Sensitivity Low Frequency Performance Limits

Command String	Frequency	Signal level	Resolution	Tolerance
IP FB B1 BLI	10 Hz	25 mV rms	8	± 1 Hz
IP FB B1 BLI	5 kHz	25 mV rms	8	± 0.1 Hz
IP FB B1 BLI	10 kHz	25 mV rms	8	± 0.1 Hz

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4. Disconnect the test equipment.

5. Connect the Signal Generator to the VX4223 as shown in Figure 5-4.

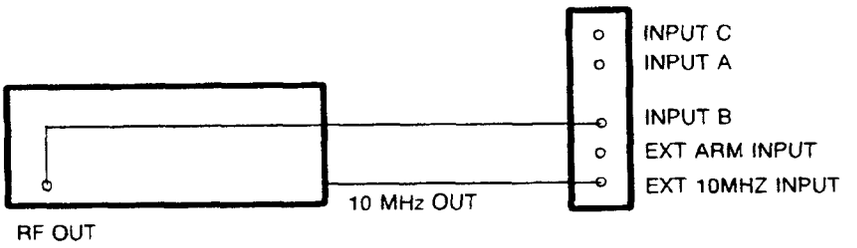


Figure 5-4. Input B High Frequency Sensitivity Test Configuration

6. Set the VX4223 measurement resolution to the values given in Table 5-5 and apply the frequencies given in Table 5-5 to the counter's input B. Verify that the VX4223 gives a stable reading within the tolerances given at less than the signal level given.

Table 5-5. Input B Sensitivity High Frequency Performance Limits

Command String	Frequency	Signal level	Resolution	Tolerance
IP FB B1 BLI	100 kHz	25 mV rms	8	± 0.1 Hz
IP FB B1 BLI	10 MHz	25 mV rms	8	± 1 Hz
SRS9	100 MHz	25 mV rms	9	± 1 Hz

7. Disconnect the test equipment.

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Input C Sensitivity Test

NOTE

This section applies only to VX4223s fitted with Option 01 (Input C).

1. Set the VX4223 to its home state. Select Frequency C as the measurement mode and external frequency standard (command string **IP FC B1**).

2. Connect the Signal Generator to the counter as shown in Figure 5-5.

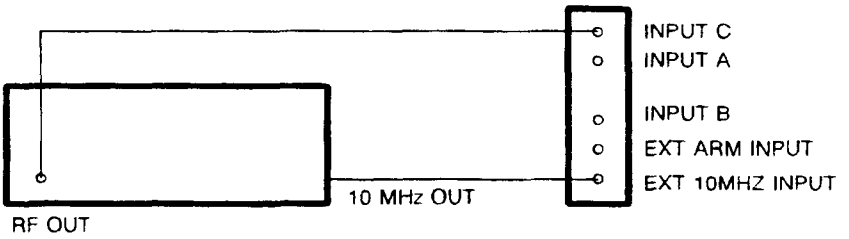


Figure 5-5. Input C Test Configuration

3. Set the VX4223 measurement resolution to the values given in Table 5-6 and apply the frequencies given in Table 5-6 to the counter's input C. Verify that the VX4223 gives a stable reading within the tolerances given at less than the signal level given.

Table 5-6. Input C Sensitivity Performance Limits

Command String	Frequency	Signal level	Resolution	Tolerance
IP FC B1	40 MHz	25 mV rms	8	± 1 Hz
SRS9	100 MHz	25 mV rms	9	± 1 Hz
SRS9	500 MHz	25 mV rms	9	± 1 Hz
SRS9	1.0 GHz	25 mV rms	9	± 2 Hz
SRS9	1.3 GHz	50 mV rms	9	± 2 Hz

4. Disconnect the test equipment.

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Time Interval A-B Test

1. Set the VX4223 to its home state. Select Time Interval A-B as the measurement mode, 50 ohms for input A input impedance, Common mode for inputs A and B and external frequency standard
(command string **IP TI ALI BCC B1**).

2. Connect the VX4223 to the signal generator as shown in Figure 5-6. Set the signal generator to 10 MHz, 0 dBm.

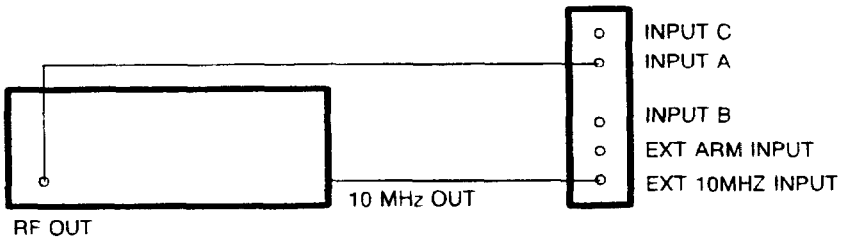


Figure 5-6. Time Interval A-B Test Configuration

3. Set the counter input trigger slopes as shown in Table 5-7 and verify that the counter's measurement result is as given in Table 5-7.

Table 5-7. Time Interval A-B Test Performance Limits

Command String	Input A Slope	Input B Slope	Result	Tolerance
IP TI ALI BCC B1	+	+	0 ns	± 2 ns
ANS	–	+	50 ns	± 2 ns
BNS	–	–	0 ns	± 2 ns
APS	+	–	50 ns	± 2 ns

4. Disconnect the test equipment.

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Totalize A by B Test

1. Set the VX4223 to its home state. Select Totalize A by B as the measurement mode, 50 ohms for input A input impedance, and external frequency standard (command string **IP TA ALI B1**).

2. Connect the VX4223 to the signal generator as shown in Figure 5-7. Set the signal generator to 10 MHz, 0 dBm. Verify that the counter's measurement result is 5000 ± 1.

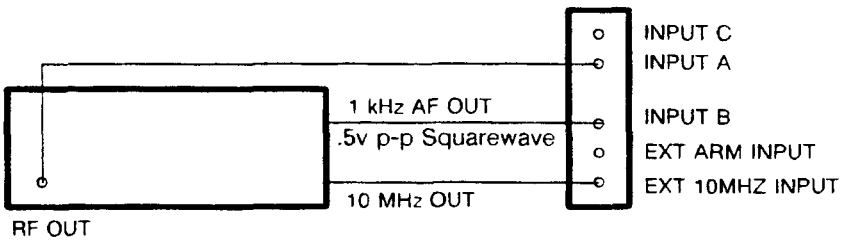


Figure 5-7. Totalize A by B Test Configuration

3. Disconnect the test equipment.

Ratio A/B Test

1. Set the VX4223 to its home state. Select Ratio A/B as the measurement mode, 50 ohms for input A input impedance, DC input coupling for input B, external frequency standard and set the measurement resolution to seven digits (command string **IP RA ALI B1 SRS7**).

2. Connect the VX4223 to the signal generator as shown in Figure 5-8. Set the signal generator to 50 MHz, 100 mV rms. Verify that the counter's measurement result is 50000 ± 10.

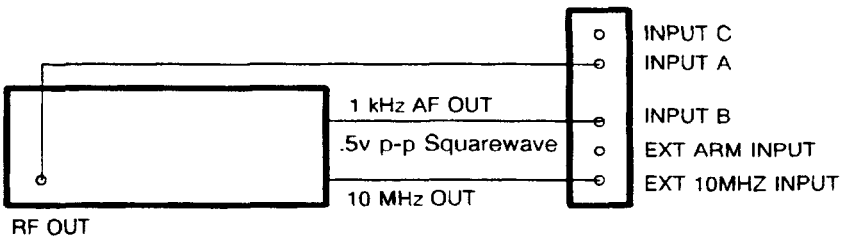


Figure 5-8. Ratio A / B Test Configuration

3. Disconnect the test equipment.

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Ratio C/B Test

1. Set the VX4223 to its home state. Select Ratio C/B as the measurement mode, DC input coupling for input B, external frequency standard and set the measurement resolution to six digits
(command string **IP RC ALI B1 SRS6**).

2. Connect the VX4223 to the signal generator as shown in Figure 5-9. Set the signal generator to 50 MHz, 100 mV rms. Verify that the counter's measurement result is 50000 ± 10.

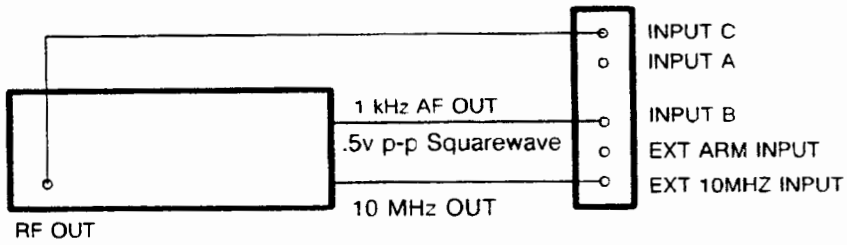


Figure 5-9. Ratio C / B Test Configuration

3. Disconnect the test equipment.

Trigger Level Accuracy Test

1. Set the VX4223 to its home state. Set the counter to DC input coupling for input A and enable special functions
(command string **IP ADC AAU SFE**).

2. Connect the counter to the DC Standard as shown in Figure 5-10 and set the DC Standard output voltage to 5.000 V.

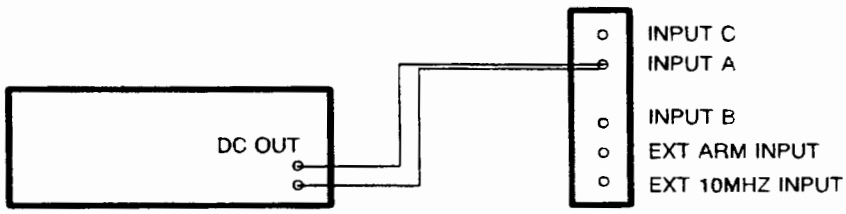


Figure 5-10. Input A Trigger Level Test Configuration

3. Single shot autotrigger the counter (command code **S31**). Recall the VX4223 stored trigger level (command code **RLA**) and verify that it is 5.00 V ± 80 mV.

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4. Reverse the polarity of the DC input to the counter. Set the VX4223 to its home state. Set the counter to DC input coupling for input A and enable special functions (command string **IP ADC AAU SFE**). Single shot autotrigger the counter (command code **S31**) and recall the stored trigger level value (command code **RLA**). Verify that it is -5.00 V ± 80 mV.

5. Set the VX4223 to its home state. Set the counter to DC input coupling for input B and enable special functions (command string **IP BDC BAU SFE**).

6. Connect the DC standard to input B of the counter as shown in Figure 5-11. Single shot autotrigger the counter (command code **S31**). Recall the VX4223 stored trigger level (command code **RLB**) and verify that it is 5.00 V ± 80 mV.

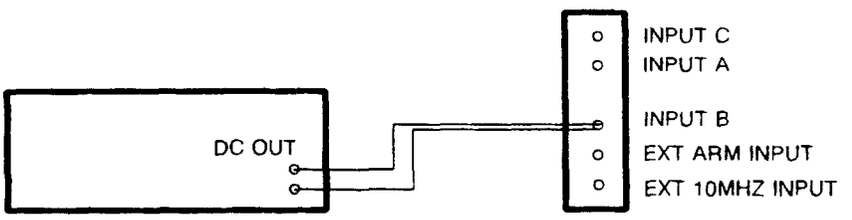


Figure 5-11. Input B Trigger Level Test Configuration

7. Reverse the polarity of the DC input to the counter. Set the VX4223 to its home state. Set the counter to DC input coupling for input B and enable special functions (command string **IP BDC BAU SFE**). Trigger the measurement (command code **S31**) and recall the stored trigger level value (command code **RLB**). Verify that it is -5.00 V ± 80 mV.

8. Disconnect the test equipment.

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Functional Checks

Input A Filter Check

1. Set the counter to its home state. Select 50 ohms input impedance for input A (command code **IP ALI**).

2. Connect the counter to the signal generator as shown in Figure 5-12.

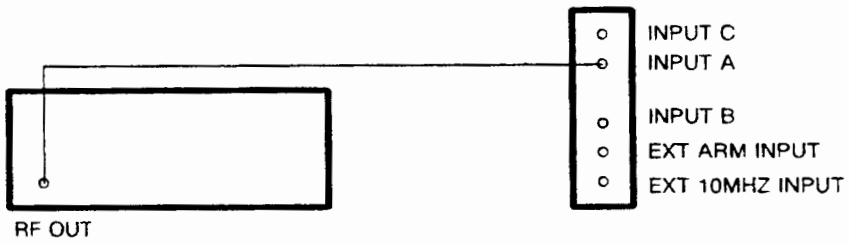


Figure 5-12. Input A Filter Check Configuration

3. Set the signal generator to 50 kHz, 10 mV. Decrease the signal generator output level (while sending the command **IP ALI**) until the counter no longer gives a stable reading. Note the signal generator output level.

4. Enable the counter's input A filter (command code **AFE**) and verify that the VX4223 no longer counts. Increase the signal generator until the counter gives a stable reading. Note the signal generator output level and verify that this level is approximately 1.5 to two times the level previously noted.

5. Disconnect the test equipment.

Input A Attenuator Check

1. Set the counter to its home state. Select 50 ohms input impedance for input A (command code **IP ALI**).

2. Connect the counter to the signal generator as shown in Figure 5-13.

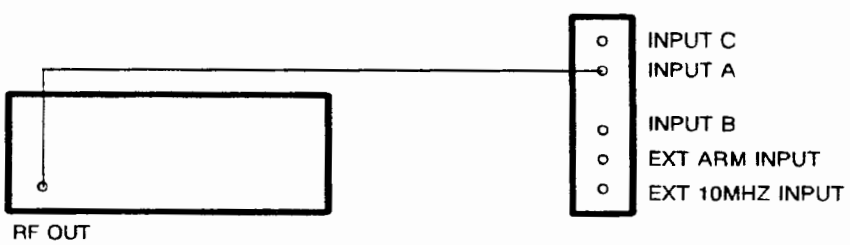


Figure 5-13. Input A X10 Attenuator Check Configuration

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3. Set the signal generator to 1 MHz, 10 mV. Decrease the signal generator output level (while sending the command **IP ALI**) until the counter no longer gives a stable reading. Note the signal generator output level.

4. Enable the counter's input A attenuator (command code **AAE**) and verify that the VX4223 no longer counts. Increase the signal generator (while sending the command **AAE** until the counter gives a stable reading. Note the signal generator output level and verify that this level is approximately ten times the level previously noted.

5. Disconnect the test equipment.

Input B Attenuator Check

1. Set the counter to its home state. Select Frequency B as the measurement mode and 50 ohms input impedance for input B
(command code **IP FB BLI**)

2. Connect the counter to the signal generator as shown in Figure 5-14.

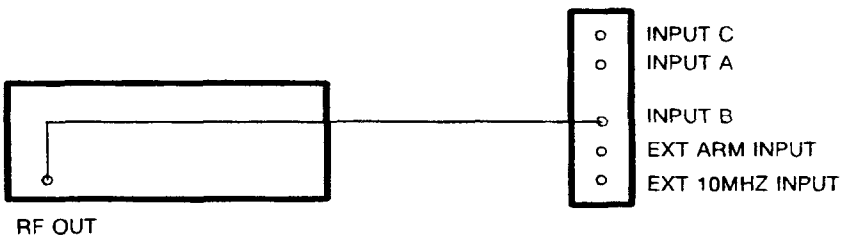


Figure 5-14. Input B X10 Attenuator Check Configuration

3. Set the signal generator to 1 MHz, 10 mV. Decrease the signal generator output level (while sending the command **IP FB BLI**) until the counter no longer gives a stable reading. Note the signal generator output level.

4. Enable the counter's input B attenuator (command code **BAE**) and verify that the VX4223 no longer counts. Increase the signal generator (while sending the command **BAE**) until the counter gives a stable reading. Note the signal generator output level and verify that this level is approximately ten times the level previously noted.

5. Disconnect the test equipment.

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Disassembly Instructions

1. Remove the three panhead screws that secure the aluminum cover to the counter body.

2. Slide the cover along the channel that it sits in, towards the rear of the counter and remove the cover.

3. Remove the ten panhead screws that secure the VX4223 bottom cover to the counter side extrusions, five on each side.

4. Remove the three countersunk screws that secure the cover to the counter.

5. Slide the cover along the channel that it sits in, towards the rear of the counter and remove the cover. The VX4223 PCB is now exposed sufficiently to allow all maintenance procedures to be carried out.

CAUTION

The VX4223 contains static sensitive devices. Observe all Electrostatic Discharge precautions while the counter is disassembled.

Reassembly Instructions

1 Align the bottom cover with the channels in the side extrusions of the counter and slide the cover along the channels.

2. Secure the cover to the counter body with the thirteen screws obtained on the removal of the bottom cover, five along each edge and three on the centerline of the cover.

3. Align the top cover with the channels in the side extrusions of the counter and slide the cover along the channels.

4. Secure the cover to the counter body with the three panhead screws obtained on removal of the cover.

VX4223 Input Amplifier Setup Procedure

Introduction

1. This section provides the setup procedures that are to be carried out after repair of the VX4223 or the failure of a routine specification check.

2. All setup procedures are to be carried out with the counter covers removed, at an ambient temperature of 23 °C ± 2 °C. The counter must be allowed to warm up for a minimum of one hour before commencing any setup procedure. The procedures given here commence with the counter in the Home state.

3. It is recommended that the counter is read repeatedly and the current measurement result displayed by the controller used while adjusting the counter's input amplifiers to obtain a stable count.

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Input A Amplifier Setup Procedure

1. Set R12 fully counterclockwise and R10 to its midposition. R10 and R12 are located on the counter's PCB as shown in Figure 5-15.

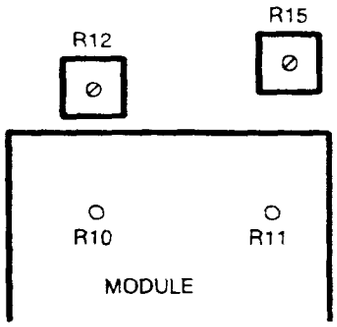


Figure 5-15. Location of R10, R11, R12 and R15

2. Select Frequency A as the measurement function, set Input A input impedance to 50 ohms and set the counter resolution to three digits (command code **FA ALI SRS3**).

3. Connect the counter to the signal generator as shown in Figure 5-16.

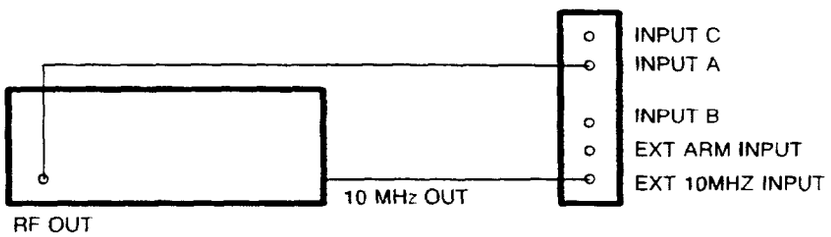


Figure 5-16. Input A Amplifier Setup Configuration

4. Set the signal generator output to 100 MHz, 3.0 mV rms.

5. Adjust R10 to obtain a stable reading of 100 MHz ± 0.1 MHz. Verify that the counter's GATE LED is flashing.

6. Turn off the RF output of the signal generator.

7. Set the counter resolution to eight digits (command code **SRS8**).

8. Increase the signal generator output level to 13 mV rms.

9. Adjust R12 slowly clockwise until the counter measurement result starts to become unstable. Turn R12 slowly counterclockwise until the counter measurement result is stable, value 100 MHz ± 1 Hz.

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10. Reduce the signal generator output level to 7 mV rms and verify that the GATE LED stops flashing. If the LED continues to flash, repeat steps 8 to 10.

11. Disconnect the test equipment.

Input B Amplifier Setup Procedure

1. Set R15 fully counterclockwise and R11 to its midposition. R11 and R15 are located on the counter PCB as shown in Figure 5-15.

2. Select Frequency B as the measurement function, set Input B input impedance to 50 ohms and set the counter resolution to three digits (command code **FB BLI SRS3**).

3. Connect the counter to the signal generator as shown in Figure 5-17.

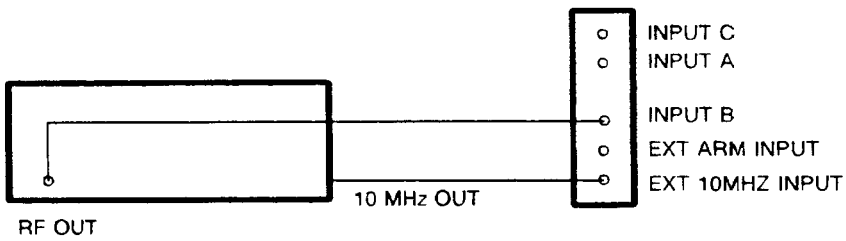


Figure 5-17. Input B Amplifier Setup Configuration

4. Set the signal generator output to 100 MHz, 3.0 mV rms.

5. Adjust R11 to obtain a stable reading of 100 MHz ± 0.1 MHz. Verify that the counter's GATE LED is flashing.

6. Turn off the RF output of the signal generator.

7. Set the counter resolution to eight digits (command code **SRS8**).

8. Increase the signal generator output level to 13 mV rms.

9. Adjust R15 slowly clockwise until the counter measurement result starts to become unstable. Turn R15 slowly counterclockwise until the counter measurement result is stable, value 100 MHz ± 1 Hz.

10. Reduce the signal generator output level to 7 mV rms and verify that the GATE LED stops flashing. If the LED continues to flash, repeat steps 8 to 10.

11. Disconnect the test equipment.

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Input C Amplifier Setup Procedure

1. Connect the signal generator to the counter as shown in Figure 5-18.

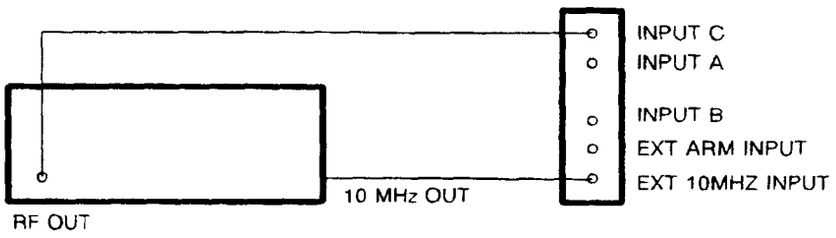


Figure 5-18. Input C Setup Configuration

2. Set R27 on the Channel C amplifier board fully clockwise.
3. Select Frequency C as the measurement function (command code **FC**)
4. Set the signal generator output to 1 GHz, 5.0 mV rms.
5. Adjust R27 slowly clockwise until the GATE LED starts to flash and the measurement result is 1 GHz ± 10 Hz.
6. Turn off the signal generator output. Reduce signal generator output level to 4.5 mV rms.
7. Turn off the signal generator output and verify that the VX4223 is not counting. If the counter continues to count, repeat steps 4 to 7.
8. Disconnect the test equipment.

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Calibrated by _____ Date _____ Serial Number _____

VX4223 Performance Verification Test Record

Input A Sensitivity

Frequency	Signal Level	Resoluton	VX4223 Reading	Tolerance	Pass/Fail
10 Hz	25 mV rms	8		± 1 Hz	
5 kHz	25 mV rms	8		± .1 Hz	
10 kHz	25 mV rms	8		± .1 Hz	
100 kHz	25 mV rms	8		± .1 Hz	
10 MHz	25 mV rms	8		± 1 Hz	
100 MHz	25 mV rms	9		± 1 Hz	
160 MHz	50 mV rms	9		± 1 Hz	

Input B Sensitivity

Frequency	Signal Level	Resoluton	VX4223 Reading	Tolerance	Pass/Fail
10 Hz	25 mV rms	8		± 1 Hz	
5 kHz	25 mV rms	8		± .1 Hz	
10 kHz	25 mV rms	8		± .1 Hz	
100 kHz	25 mV rms	8		± .1 Hz	
10 MHz	25 mV rms	8		± 1 Hz	
100 MHz	25 mV rms	9		± 1 Hz	

Time Interval A-B

Input A Slope	Input B slope	VX4223 Reading	Spec	Pass/Fail
+	+		0 ns ± 2 ns	
–	+		50 ns ± 2 ns	
–	–		0 ns ± 2 ns	
+	–		50 ns ± 2 ns	

Totalize A by B

Input A	Input B	Ext Std In	VX4223 Reading	Spec	Pass/Fail
10 MHz	1 KHz	10 MHz		5000 ± 10	

Ratio A/ B

Input A	Input B	Ext Std In	VX4223 Reading	Spec	Pass/Fail
50 MHz	1 KHz	10 MHz		50000 ± 10	

Trigger Level Accuracy

Input A Trigger Level Voltage	VX4223 Reading	Spec	Pass/Fail
5.000 V		5.00 V ± 80 mV	
– 5.000 V		-5.00 V ± 80 mV	
Input B Trigger Level Voltage			
5.000 V		5.00 V ± 80 mV	
– 5.000 V		-5.00 V ± 80 mV	

	Result Before	Result After	Pass/Fail
Input A Filter			
Input A (10X) Attenuator			
Input B (10X) Attenuator			

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VX4223 Performance Verification Test Record (cont.)

(OPT. 1/Input C)

Input C Sensitivity

Frequency	Signal Level	Resoluton	VX4223 Reading	Tolerance	Pass/Fail
40 MHz	25 mV rms	8		± 1 Hz	
100 MHz	25 mV rms	9		± 1 Hz	
500 MHz	25 mV rms	9		± 1 Hz	
1.0 GHz	25 mV rms	9		± 2 Hz	
1.3 GHz	50 mV rms	9		± 2 Hz	

Ratio C/B

Input A	Input B	Ext Std In	VX4223 Reading	Spec	Pass/Fail
50 MHz	1 kHz	10 MHz		50000 ± 10	

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Appendix A
VXIbus Glossary

This glossary contains terms that are defined according to their use in the VXIbus System. Although some terms may be used in other systems with different meanings, it is important to apply them only to VXIbus applications. In any instance in which a term is applicable only to a particular instrument module, that fact is so noted.

ACCESSED Indicator

An amber LED indicator that illuminates when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.

ACFAIL*

A VXIbus backplane line that is asserted under these conditions: 1) by the Mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction) or 2) by the front panel ON/STANDBY switch when it is switched to STANDBY.

A-Size Card

A VXIbus instrument module that is 100 x 160 x 20.32 mm (3.9 x 6.3 x 0.8"); it is the same size as a VMEbus single-high, short module.

Asynchronous Communication

Communications that occur outside the normal "command-response" cycle. Such communications may have a higher priority than synchronous communication.

Backplane

The printed circuit board that is mounted in a VXIbus Mainframe to provide the interface between VXIbus modules, and between the Mainframe power supplies and the modules.

B-Size Card

A VXIbus instrument module that is 233.4 x 160 x 20.32 mm (9.2 x 6.3 x 0.8"); it is the same size as a VMEbus double-high, short module.

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Bus Arbitration

In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.

Bus Timer

A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.

Client

In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10

A 10 MHz, individually buffered, differential ECL system clock that is sourced from Slot 0 and distributed to each slot (1 — 12) through P2. It is distributed to each module as as a single source, single destination signal with a matched delay of under eight (8) nanoseconds total.

CLK100

A 100 MHz, individually buffered, differential ECL system clock that is sourced from Slot 0 and distributed to each slot (1 — 12) through P3. It is synchronized to CLK10 and distributed to each module as a single source, single destination signal with a maximum timing skew of two (2) nanoseconds, and a matched delay of under eight nanoseconds total.

Commander

A device that controls another device (a servant). A commander may be a servant of another commander.

Command

Any communication from a commander to a message based servant, consisting of a write to the servant's Data Low register, possibly preceded by a write to the data register.

Communication Registers

A set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

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Configuration Registers

A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus Specification requires that all VXIbus devices have a set of such registers, all accessible from P1 on the VXIbus.

C-Size Card

A VXIbus instrument module that is 340 x 233.4 x 30.48 mm (13.4 x 9.2 x 1.2").

Data Transfer Bus

One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

DC FAIL Indicator

A red LED indicator that illuminates when a power fault is detected on the backplane.

Device Specific Protocol

A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card

A VXIbus instrument module that is 340 x 366.7 x 30.48 mm (13.4 x 14.4x 1.2").

DTB

See Data Transfer Bus.

DTB Arbiter

A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT

Device Under Test.

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ECLTRG

Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 Ω; the asserted state is logical High.

Embedded Address

An address in a communications protocol in which the destination of the message is included in the message.

ESTST

Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Device

A device that has VXIbus configuration registers and a subclass register. This category of device is intended to allow for definition of additional device types.

Extended Self Test

Any self test or diagnostic power-up routine that executes after the initial kernel self-test program.

External System Controller

The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator

A red LED indicator that illuminates when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

HI TEMP Indicator

A VX5520 Slot 0 Controller (only) LED indicator that illuminates to signify an excessive temperature condition on the module.

IACK Daisy Chain Driver

The circuit that drives the VXIbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

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ID-ROM

An NVRAM storage area that provides for non-volatile storage of various module attributes, such as device name, serial number, error codes, and calibration data, etc.

Instrument Module

A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device, and/or may occupy more than one mainframe slot.

Interface Device

A VXIbus device that provides an interface to external equipment.

Interrupt Handler

A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter

A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ

(Interrupt ReQuest) A VXIbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus

A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller

The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus Mainframe or several Mainframes. See Resource Manager.

Local Processor

The processor on an instrument module.

Logical Address

An 8-bit number that uniquely identifies each VXIbus Device in a system. It defines a device's A16 register address, and indicates Commander/Servant relationships.

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Mainframe

A rigid framework that provides mechanical support for modules inserted into a VXIbus backplane. It ensures that connectors mate properly, that adjacent modules do not contact each other, and that modules do not disengage from the backplane due to vibration or shock. It also may provide mechanical support and housing for power supplies and their distribution wiring to the backplane.

Memory Device

A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message

A series of data bytes that are treated as a single communication element, with a well defined message body and terminator.

Message Based Device

A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines

Module/system identity lines.

Physical Address

The address assigned to a backplane slot during an access.

Power Monitor

A device that monitors backplane power and reports fault conditions.

P1

The top-most backplane connector for a given module slot in a vertical Mainframe. The left-most backplane connector for a given slot in a horizontal Mainframe.

P2

The middle backplane connector for a given slot in a Mainframe.

P3

The bottom backplane connector for a given module slot in a vertical Mainframe. The right-most backplane connector for a given slot in a horizontal Mainframe.

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Query

A form of command that allows for inquiry to obtain status or data.

READY Indicator

A green LED indicator that illuminates when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5 V power will extinguish this indicator.

Register Based Device

A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols.

Requester

A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.

Resource Manager

A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self-test diagnostics, and initializing system commanders.

Self Calibration

A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for variables such as temperature, power supply variations, and line losses.

Self Test

A set of routines that test the operational functionality of the the instrument module. These routines are performed on power-up, and on command.

Servant

A device that is controlled by a Commander. There are message-based and register-based servants.

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Server

A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol (SMP) channel.

Shared Memory Protocol

A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

Slot 0 Controller

See Slot 0 Module. Also see Resource Manager.

Slot 0 Module

A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 — 12 (CLK10 and the MODID module identity lines), but that may provide other VXIbus services such as CLK100, SYNC100, STARBUS, and trigger control.

SMP

See Shared Memory Protocol.

STARX

Two bidirectional, 50 Ω, differential ECL lines that provide inter-module asynchronous communication. These pairs of time-delay matched lines connect Slot 0 to each of slots 1 — 12 in a Mainframe. These lines have a well matched timing skew and less than five nanoseconds of total timing delay.

STARY

Two bidirectional, 50 Ω, differential ECL lines that provide inter-module asynchronous communication. These pairs of time-delay matched lines connect Slot 0 to each of slots 1 — 12 in a Mainframe. These lines have a well matched timing skew and less than five nanoseconds of total timing delay.

STST

STart/STop protocol; used to synchronize modules.

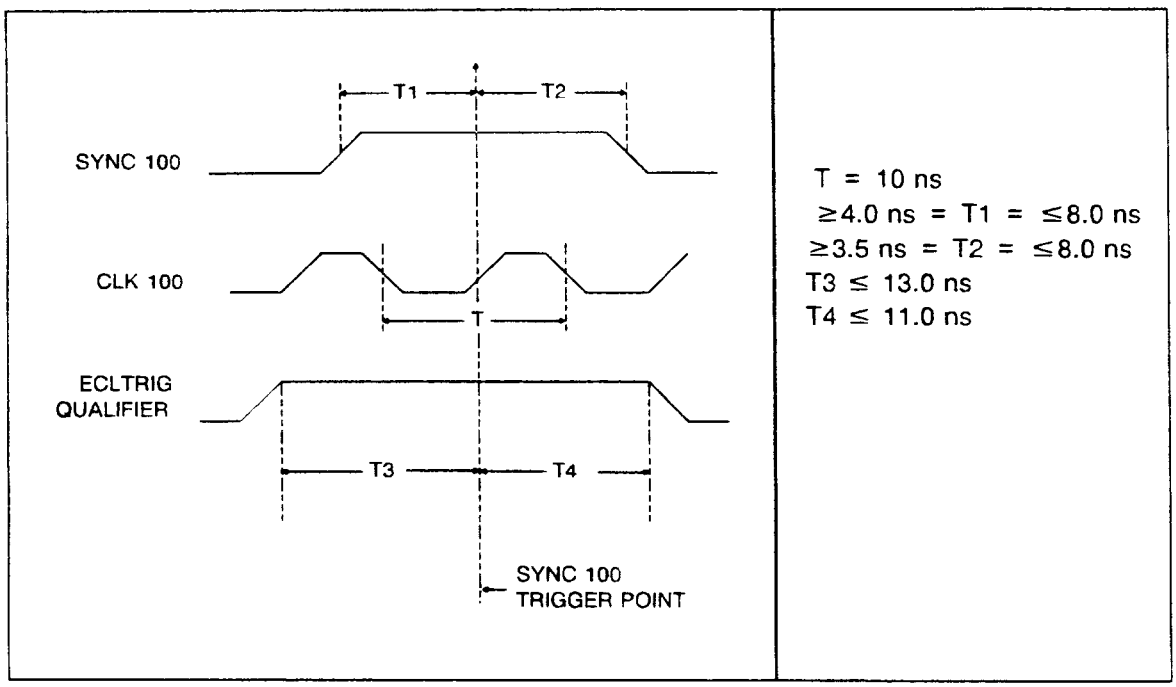
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SYNC100

SYNC100 is a Slot 0 signal used to synchronize multiple VXI devices with respect to a given rising edge of CLK100. The signal distributed to the devices is individually buffered to each slot, and is matched to less than 2 ns of skew between slots.

SYNC100 Trigger Protocol

SYNC100 trigger is a Tektronix designed protocol that allows multiple devices to receive a trigger on the same edge of the 100 MHz System Clock (CLK100). It utilizes the VXI SYNC100 signal to select the particular clock edge and an ECLTRG line as a qualifier to distinguish SYNC100 trigger protocol from ESTST protocol (see timing diagram below). This protocol allows device groups (such as multiple VX5260 Digitizers) to be triggered synchronously.



Synchronous Communications

A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL*

A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

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System Clock Driver

A functional module that provides a 16 MHz timing signal on the Utility Bus.

System Hierarchy

The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

Test Monitor

An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

Test Program

A program, executed on the system controller, that controls the execution of tests within the test system.

Test System

A collection of hardware and software modules that operate in concert to test a target DUT.

TTLTRG

Open collector TTL lines used for inter-module timing and communication.

VXIbus Subsystem

One Mainframe with modules installed. The installed modules include one module in Slot 0 to perform the Slot 0 functions and a given complement of instrument modules in slots 1 — 12. The subsystem also may include a Resource Manager.

Word Serial Protocol

A word oriented, bidirectional, serial protocol for VXIbus communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).

Word Serial Communications

Inter-device communications using the Word Serial Protocol.

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WSP

See Word Serial Protocol.

10 MHz Clock

A 10 MHz timing reference. Also see CLK10.

100 MHz Clock

A 100 MHz clock synchronized to CLK10. Also see CLK100.

488-To-VXIbus Interface

A message based device that provides for communication between the IEEE 488 bus and VXIbus instrument modules.

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