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VX5530/VX5535
VXIbus System Controller
Users Manual

070-7438-00 (Book 1 of 3)
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Preface

Purpose Of This Manual

This manual provides information about how to configure, install and operate the VX5530/VX5535. See either the VX5530/VX5535 C Programmers Manual or the VX5530/VX5535 BASIC Programmers Manual for programming information.

Organization Of This Manual

This manual is organized into the following sections and appendices:

- **Section 1 General Information** – provides an overview of the module's capabilities. Contains the Environmental, Electrical, and Mechanical specifications for the module, and a software overview.
- **Section 2 Preparation for Use** – provides information about how to configure and install the module and software.
- **Section 3 Operation** – describes the connectors and indicators on the module's front panel and the power-up sequence of the module.
- **Section 4 Connector Definitions** – describes the pin and signal assignments for the P1, P2 and P3 VXIbus connectors on the rear panel.
- **Section 5 Software Users Information** – describes how to use the VX5530/VX5535 software, including the functions of the VConnect VXIbus Configurator, the Start-Up Resource Manager, and the BusProbe.
- **Section 6 Options** – lists options currently available for the VX5530/VX5535.
- **Appendix A VX5530/VX5535 Architecture** – describes the architectural features of the VX5530/VX5535, both from a PC/AT perspective and from the VXIbus perspective.
- **Appendix B Bill of Material Control** – describes operation of the ckbom command.
- **Appendix C Interrupt and I/O Port Addresses** – lists all the Interrupts used by the VX5530/VX5535.
- **Appendix D Glossary** – contains a glossary of VXIbus terms and definitions.
- **Appendix E ASCII/GPIB Chart** – contains a listing of the ASCII character set and GPIB codes in terms of 7-bit binary, decimal, octal, and hexadecimal values.

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Notational Conventions

Active Signal States

An asterisk (*) following a signal mnemonic, such as ACFAIL*, denotes that the signal is active when in its low state. Signals without an asterisk (*) are active when in their high state.

Number Base

All numbers used in text are assumed to be decimal, unless otherwise noted with a suffix using the characters 'b', 'h', or 'o' immediately following the number.

- Binary numbers (base 2) are denoted by a 'b' suffix, such as: 1101b.
- Octal numbers (base 8) are denoted by an 'o' suffix, such as: 307o.
- Hexadecimal numbers (base 16) are denoted by an 'h' suffix, such as: 97FFh.

Related Documentation

The following documents on related subjects may be useful for information on the use of the module:

- *VXIbus System Specification, Revision 1.2, June 21, 1988.*
- *ANSI/IEEE Std 1014-1987, IEEE Standard for a Versatile Backplane Bus: VMEbus.*
- *ANSI/IEEE Std 488.2-1987, IEEE Standard Codes, Formats, Protocols, and Common Commands.*
- VX5530/VX5535 C and BASIC ProgrammersManuals

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Operators Safety Summary

The general safety information in this summary is for both operating and servicing personnel. Specific warnings and cautions are found throughout the manual where they apply, and may not appear in this summary.

Terms

Terms in This Manual

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to the module or other property.

Terms as Marked on Module

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the module itself.

Symbols

Symbols in This Manual



This symbol indicates where applicable cautionary or other information is to be found.



This symbol indicates where special explanatory information is included in the manual. There is no caution or danger associated with the information.

Symbols as Marked on Module



DANGER – High Voltage.



Protective ground (earth) terminal.



ATTENTION – refer to manual.



Refer to manual before using.

Power Source

This module is intended to operate in a mainframe whose power source does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection through the grounding conductor in the power cord(s) is essential for safe operation.

Grounding the Module

This module is grounded through the grounding connector of the mainframe power cord(s). To avoid electrical shock, plug the mainframe power cord(s) into a properly wired receptacle before connecting to the module connectors. A protective ground connection through the mainframe is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only fuses specified in the module parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications required for the fuse that it replaces.

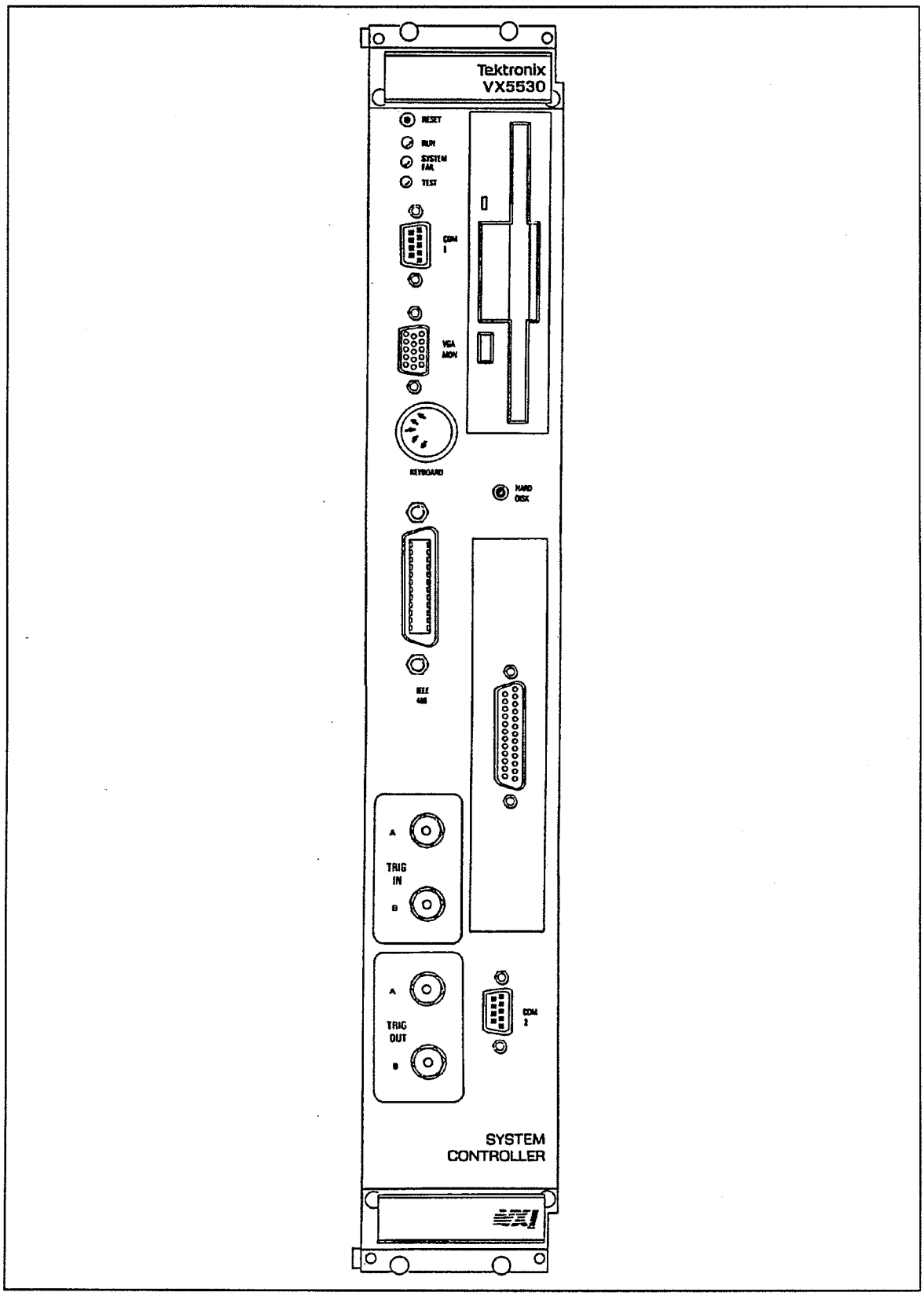
Do Not Operate in Explosive Atmosphere

To avoid explosion, do not operate the module in an explosive atmosphere.

Do Not Remove Covers or Panels

To avoid personal injury, the module covers should be removed only by qualified service personnel. Do not operate the module without covers and panels properly installed.

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VX5530/VX5535 VXIbus System Controller

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Section 1
General Information

Hardware Overview

Description

The VX5530 and VX5535 System Controllers (hereinafter referred to as the VX5530/VX5535) are double-wide, D-size, VXIbus modules that combine an Intel 80386 CPU with the functionality of a VXIbus Slot 0 Resource Manager. The VX5530/VX5535 has two RS232 serial communications interface ports, one parallel input/output port, and an IEEE 488 Controller-in Charge or Talker/Listener interface port.

The VX5530/VX5535 links the high performance PC/AT architecture of the Intel 80386 processor to the VXIbus to create a VXIbus System Controller that can utilize generic PC software (such as MS-DOS, OS/2, Windows, and GWBASIC) to access the advanced instrumentation resources of VXIbus systems. It also links the VXIbus System to other external systems, devices, and peripherals through its serial, parallel, and IEEE 488 ports.

80386 CPU

A 16 MHz 80386 CPU is standard with the VX5530. The VX5535 comes with a 20 MHz 80386 CPU. A 80387 math coprocessor is standard in both models.

Several layers of sophisticated software are provided with the VX5530/VX5535, ranging from on-board BIOS with setup software and power-on self-test, to a Microsoft® Windows-based VXIbus configuration and debugging tool set. Both development and execution environments are supported from this powerful software library.

Standard memory for the VX5530 is 2M bytes of 32-bit, dual-ported, zero wait-state, RAM. 8M bytes of memory comes standard with the VX5535. Hardware memory mapping configures 1M byte (960K bytes) of standard memory to provide 640K bytes of standard DOS base memory and 320K bytes of DOS extended memory. The 4 gigabytes of VXIbus address space can be accessed from within the DOS environment through a hardware feature called a *page frame*, which makes the memory handling techniques of the two architectures compatible.

Internal mass storage is provided on a 40-megabyte hard disk and 1.4-megabyte, 3.5 inch floppy diskette.

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The front panel provides connections for a PC/AT style keyboard, a VGA display monitor, a parallel printer, two RS-232 communications ports, a standard IEEE 488 (GPIB) Talker/Listener and Controller-in-Charge port, two external trigger inputs and two external outputs.

Slot 0 Functionality

The VX5530/VXX5535 provides all of the Slot 0 Module functionality specified by the VXIbus Specification. CLK10 and MODID signal lines are provided on the VXIbus P2 connector. CLK100 signal line is provided on the VXIbus P3 connector. P3 also supports the VXI STARbus (STARX and STARY) to slots 1-12 and the SYNC100 and ESTST (Extended Start Stop) protocols for advanced trigger functions.

Advanced Trigger Functions (ATF)

The VX5530/VX5535 exceeds the VXIbus requirements for Slot 0 functionality with a superset of resources called Advanced Trigger Functions (ATF). These functions provide real time control of VXIbus triggers. Refer to Appendix A, under *Advanced Trigger Functions*, for more details. Four front panel BNC connectors support user level I/O. Internal Function Units utilize, modify or route trigger signals. An 8-channel Instrument Trigger Bus (ITB) provides connections between the internal functions. ITB channels are bi-directional ECL and can have only one active driver but may have multiple receivers. Function Units and routing channels are configured under program control. Function units are broken down as follows:

I/O Unit

Input and output BNC connectors permit the routing of TTL compatible signals to and from the ITB.

Protocol Unit

The VX5530/VX5535 provides two protocol units each of which supports the SYNC100, Start Stop (STST), and Extended Start Stop (ESTST) protocols. The protocol units can be directly controlled by the microprocessor or by an ITB channel.

Linear Delay Unit

The two linear delay units provide programmable delays for 0 to 15 nS in 1 nS increments.

Logic Unit

The logic unit can combine signals on the ITB. Signal input and output polarity are user-programmable, and inputs can be programmed to be edge or level sensitive.

STARbus Routing Unit

The VX5530/VX5535 provides three STARbus routing units. Each routing unit is a 16 point cross matrix switch. Eight of the I/O channels are connected to the ITB channels and provide general purpose routing. The second eight I/O channels are connected to the STARX and STARY channels for four VXIbus slots.

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Clock Unit

The Clock unit generates the VXIbus CLK10 and CLK100 instrument clocks, using either an internal or external reference.

Power/Temperature Monitor

The system power and ambient temperature monitor supports system health feedback.

Standard Accessories

- NEC-2A Color Monitor
- Keytronics Keyboard
- Logitech Serial Mouse
- TekTMS Software
- Users Manual
- Programmers Manual BASIC and C
- MS-DOS® Version 3.3
- Microsoft® BASIC and C Compilers
- Microsoft® Windows/386

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Specifications

Performance Conditions

The performance limits for the specifications listed in Tables 1-1 through 1-3 are valid only when the instrument is operating under the following conditions:

- The instrument module must have at least a 20 minute warm-up period.
- The instrument module must be in an environment whose limits are specified in Table 1-1.
- Any condition not stated above that is unique to a specific characteristic is stated as part of the characteristic in the tables.

The electrical and environmental performance limits, together with their related validation procedure, if any, comprise a complete statement of the performance of a module. For Environmental Specifications, the module meets or exceeds Military Specification MIL-T-28800D, Class 5.

Table 1-1 Environmental Specifications

Characteristic	Performance Requirement
Temperature:	
Operating	0 to +50°C (+32 to +122°F).
Non-Operating	–40 to +71°C (–40 to +159.8°F).
Humidity:	
0 to 30°C	95 ± 5% RH, noncondensing.
30 to 40°C	75 ± 5% RH, noncondensing.
Above 40°C	45 ± 5% RH, noncondensing.
Altitude:	
Operating	3.05 km (10,000 ft). Derate maximum operating temperature –1°C for every 300 m (1,000 ft) above 1.5 km (5,000 ft).
Nonoperating	4.57 km (15,000 ft).
Vibration:	Withstands 0.33 mm (0.013 in) p-p, 5 to 55 Hz, 15 minutes each axis, 10 minutes each axis at resonance or 55 Hz.
Shock:	Withstands 30 g's (1/2 sine), 11 ms duration, 3 shocks in each direction along 3 major axes, 18 total shocks.
Bench Handling:	12 drops from 45 degrees, 4", or equilibrium, whichever comes first.
Transportation:	Qualified under National Safe Transit Association Preshipment Test Procedures 1A-B-1 and 1A-B-2.
Electromagnetic Compatibility:	Within limits of FCC Regulations, Part 15, Subpart J, Class A.
Electrostatic Immunity (operating):	Noninterruptive: 15 kV, 500 pF capacitor discharged in series with 100 Ω resistor. Nondestructive: 25 kV, 500 pF capacitor discharged in series with 100 Ω resistor.

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Table 1-2 Electrical Specifications

Characteristic	Performance Requirement
Advanced Trigger Functions	
Instrument Trigger Bus	Minimum pulse width: 5 nS Maximum frequency: 100 MHz
STARbus routing unit	Minimum pulse width: 2.5 nS Maximum frequency: 200 MHz
Input/Output Unit	Inputs: A = ITB(6), B = ITB(4) Outputs: A and B selectable ITB(0...7)
Inputs	2.0 V $\leq VI_H \leq$ 5.0 V 0.8 V $\geq VI_L \geq$ 0.0 V Impedance $\geq$50 KΩ Capacitance $\leq$10 pF Rise time $\leq$50 nS Maximum safe range ± 15 V
Outputs	2.1 V $\leq VO_H \leq$ 5.0 V into 50 Ω 0.6 V $\geq VO_L \geq$ 0.0 V into 50 Ω Impedance = 50 Ω
Linear Delay A and B	Inputs: A = ITB(0), B = ITB(2) Outputs: A = ITB(1), B = ITB(3) Range: 0 - 15 nS Typical delay: 8 nS (0 nS selected) Settability: 1 nS Resolution: 0.8 nS
Logic Unit	Inputs: ITB(0...6) Output: ITB(7) Input selection: enable, polarity, edge/level Output selection: polarity Input skew: $\leq$ 3 nS
Protocol Unit	Inputs: A = ITB(4), or μP, B = ITB(5) or μP Functions: STST, ESTST and SYNC100 protocols Maximum trigger rate: 20 MHz (50 nS)
Clock Unit	External reference input: Input BNCB Internal accuracy: ± 20 ppm External reference capture range: ± 100 ppm
Temperature Monitor	Operating range: 0 - 70° C Resolution: 2°C/step Accuracy: 1.5°C
Power Supply Monitor	Supplies monitored: +24, +12, +5, −2, −5.2, −12, −24 Resolution: 20 mV/step Accuracy: ± 15 mV

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Table 1-2 Electrical Specifications (Cont)

Characteristic	Performance Requirement
Slot 0 Functions	
CLK100	Accuracy ± 20 ppm 30% < duty cycle < 70%
CLK10	Accuracy ± 20 ppm 45% < duty cycle < 55%
SYNC100	Drive during ESTST and SYNC100 Trigger protocols.
ECLTRIG	Drive lines 0 - 5 during ESTST and SYNC100 Trigger protocols.
TTLTRIG	Drive lines 0 - 7 during ESTST protocol.
Maximum Power Requirements	
Voltage	Current
+5 V dc	10.0 A
–5.2 V dc	6.0 A
+12 V dc	250 mA
–12 V dc	60 mA
+24 V dc	2.5 mA
–24 V dc	2.5 mA
–2 V dc	2.5 A

Table 1-3 Mechanical Specifications

Characteristics	Description
Nominal Weight	1.14 kg (2.5 lbs).
Shipping Weight	Approx. 2.05 kg (Approx. 4.5 lbs).
Overall Module Dimensions: Height	395.20 mm (15.599 in).
Width	60.66 mm (2.388 in) including keys.
Depth	347.396 mm (13.677 in) excluding front panel, but including DIN connectors. 366.42 mm (14.426 in) typical with front panel and Schroff handles. 375.72 mm (14.792 in) typical with front panel, keying plate, and injector/ejector handles.
Cooling Requirements:	For 10°C rise, 0.050 mm H_20 @ 7.50 liters per second.

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Software Overview

The Tektronix VXIbus-based Instrument Communication Software (TekVICS) is a unique and powerful set of development tools and run-time software for system applications containing one or more Tektronix VX5530/VX5535 modules. It allows a VX5530/VX5535 to be the active controller in an embedded system.

TekVICS contains the following five facilities. See Figure 1-1. They are categorized by whether they have a human or software interface, their primary use (system development versus debug versus use in end system), and their form.

Package	Interface	Primary Use	Form
Configurator	Human	Integration	Windows application
Start Up Resource Manager	Human	End-use	DOS application
On Line Resource Manager	Software	End-use	Library
BusProbe	Human	Debug	Windows application
Bus Interface Manager	Software	End-use	Device driver
Programming Interface Libraries	Software	End-use	Library

VXIbus and GPIB Configurators

The VXIbus Configurator is an interactive application that serves as an adjunct to the Start-Up Resource Manager and On Line Resource Manager. Its role is to describe certain types of system information that can't be dynamically obtained from the VXIbus hardware devices themselves by the Start-Up Resource Manager.

The GPIB Configurator allows the user to set various GPIB communication parameters for each instrument on the GPIB. These parameters are placed in a file and are accessed by the Startup Resource Manager to build the internal table for instrument communication.

Resource Management

The VX5530/VX5535 exceeds the VXIbus requirements for Resource Manager functionality. In addition to providing the required configuration control functions, such as device identification, logical address allocation (both static and dynamic Switchless Auto-Configuration), system memory allocation, and address mapping, it provides the software tools to allow VMEbus devices to be configured and mapped.

Resource Manager functionality is provided by the Tektronix *Runtime Resource Manager* software, which allows dynamic reconfiguration of the commander/servant hierarchies and system resources such as the TTLTRIG and ECLTRIG signal lines. This capability expands the virtual instrument performance of the VXIbus subsystem.

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The management of system self-test and diagnostic sequences allows the normal power-up process to be augmented by user-defined utilities running on the 80386 CPU. Should a device fail on power-up, the self-test management function is designed to force the failed device into a safe state, and report its condition to the Resource Manager, prior to initiating normal system operations.

Start Up Resource Manager

The Start-Up Resource Manager (SURM) is a superset of the facility referred to as the resource manager in the VXIbus specification. It does everything required of a resource manager by the VXIbus specification, including both static and dynamic configuration. A key extension of the SURM, in which the Configurator and On Line Resource Manager (OLRM) cooperate, is allowing VMEbus devices to be cleanly incorporated into VXIbus systems. Other key extensions are symbolic naming of devices and extensive error checking.

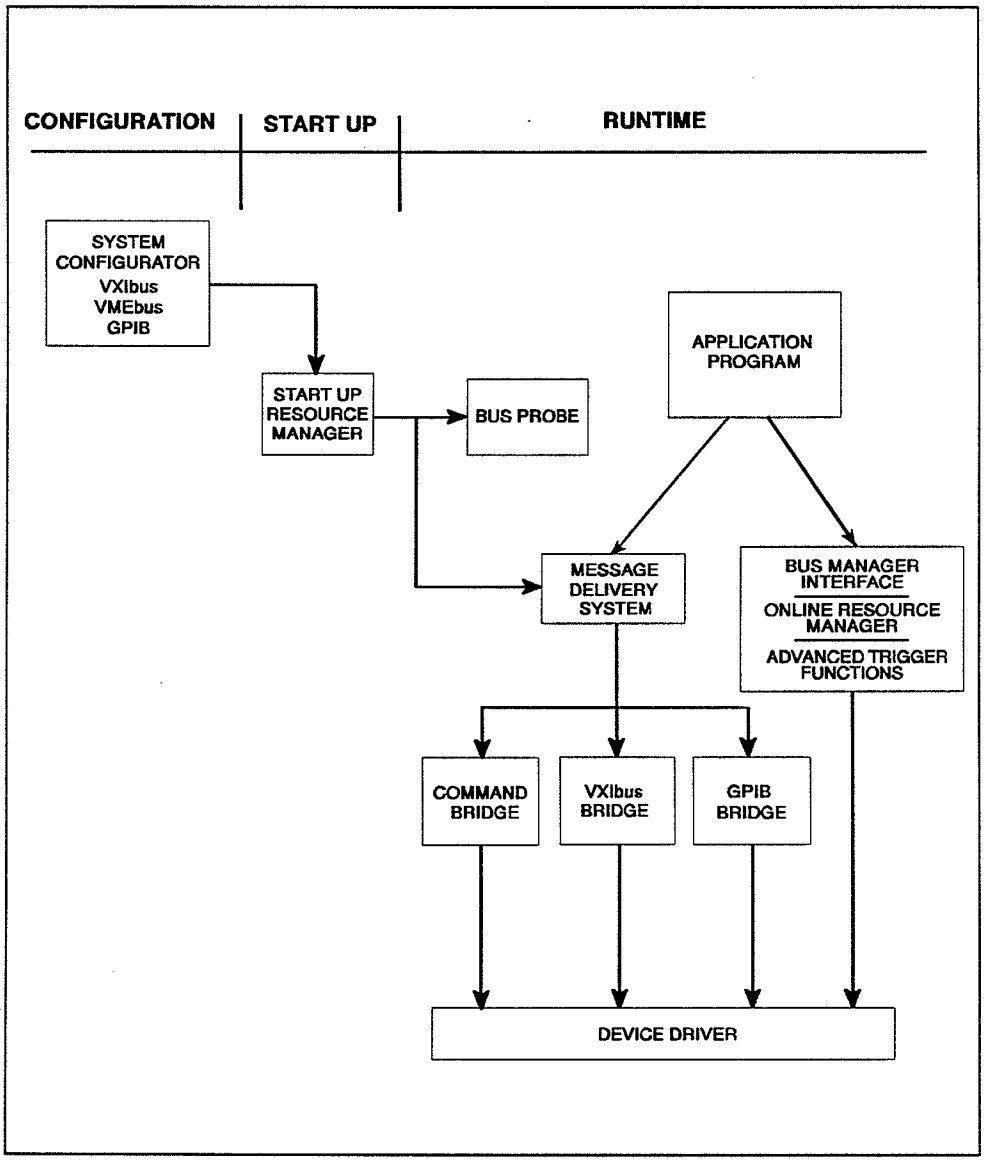


Figure 1-1. VX5530/VX5535 software overview.

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On Line Resource Manager

The On Line Resource Manager (OLRM) provides the VXIbus Resource Manager facilities for drivers and applications programs. It accesses information from the SURM and the Configurator to provide facilities for device identification and location, and the dynamic allocation of resources. Interfaces to the OLRM are provided for C and Microsoft® BASIC programs.

The On Line Resource Manager is described more fully in the *VX5530/VX5535 C (and BASIC) Programmer's* manuals.

BusProbe

BusProbe allows you to stimulate the bus. BusProbe performs higher-level VXIbus functions such as sending messages and commands and receiving results from message based devices. In addition, BusProbe asserts VXIbus interrupts, asserts trigger signals, and generates memory accesses of any type (e.g., address space, address modifier, data width) on the VXIbus.

Message Management

An advanced performance feature of the VX5530/VX5535 is its VXIbus *Message Manager*, which is a transparent set of software functions to make a test engineer's tasks easier. Its basic function is as a message router to handle the VXIbus and GPIB overhead that is required to move information to and from a device, or between devices. It handles the sending of commands to instruments and their responses, as well as asynchronous error, warning, and event messages sent from the devices to the VX5530/VX5535.

Another feature of the *Message Manager* allows for the logical naming of VXIbus devices, thus allowing complex Commander/Servant address paths to be replaced with simple user-defined names. Names may be specified by the user or automatically generated by the controller. The user may query the message manager for existing names, their association to logical addresses, and the physical location of each of the devices named. The message manager allows the user to assign names to logical entities within a device and to change these names at runtime. This feature permits easy reconfiguration of systems and replacement of devices without impacting existing software.

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Advanced Trigger Functions (ATF)

ATF provides advanced trigger, signal, and timing features within a VXIbus mainframe, as well as the necessary real-time links between multiple VXIbus subsystems.

Test Management System (TekTMS)

The Tektronix Test Management System, TekTMS, is a Microsoft® Windows software package for repetitive test software development and execution. TekTMS is provided as three software components: Interactive Procedure Generator (IPG), VXIbus Instrument Front Panel Library, and GPIB Instrument Front Panel Library. (Refer to TekTMS manuals for details.)

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Section 2
Preparation for Use

Introduction

The configuration and installation information in this section is for VX5530 or VX5535 System Controllers that are installed in a VXIbus D-size mainframe such as the Tektronix VX1500.

Configuration

The VX5530/VX5535 can be configured for either slot-0 (factory default) or non-slot-0 operation. Configuring the VX5530/VX5535 involves both hardware and software aspects. This section contains the hardware configuration topics (VX5530/VX5535 Jumper Configurations and VXIbus mainframe Jumper Configurations). The software configuration is discussed in Section 3, Operation, under the topic *Initial Power-up Sequence.*

The Tektronix VX5530 and VX5535 modules are factory configured for Slot-0 operation. Hardware configuration may require that you appropriately position six jumpers on the VX5530/VX5535 main circuit board for non-slot 0 configuration.

Removing a Side Panel

To remove a side panel, unlock the six 1/4-turn fasteners that hold panel to the module chassis. These fasteners unlock when turned 1/4 turn counterclockwise from their locked position, which is indicated when their screwdriver slot is in line with the small plastic insert adjacent to the fastener. When replacing the panel, be sure to lock all of the 1/4-turn fasteners by turning them 1/4 turn clockwise.

VX5530/VX5535 Jumper Configurations

The VX5530/VX5535 is configured with six jumpers: JP590 through JP594, and JP890, which are accessed by removing the right side panel (see procedure above). Jumpers JP590 and JP591 are for test purposes, and jumpers JP592 through JP594 and JP890 determine whether or not the VX5530/VX5535 is configured as a Slot 0 device. Figure 2-1 and Table 2-1 show the location and configuration settings for these jumpers; the factory default settings configure the VX5530/VX5535 as a Slot 0 Device.

A VX5530/VX5535 module that is installed in the two left-most slots of a VXIbus mainframe provides VXIbus system controller functions (bus request arbitration, interrupt acknowledge daisy-chaining, system clock generation, bus time-out generation, ECL clock generation, and MODID generation). These functions must

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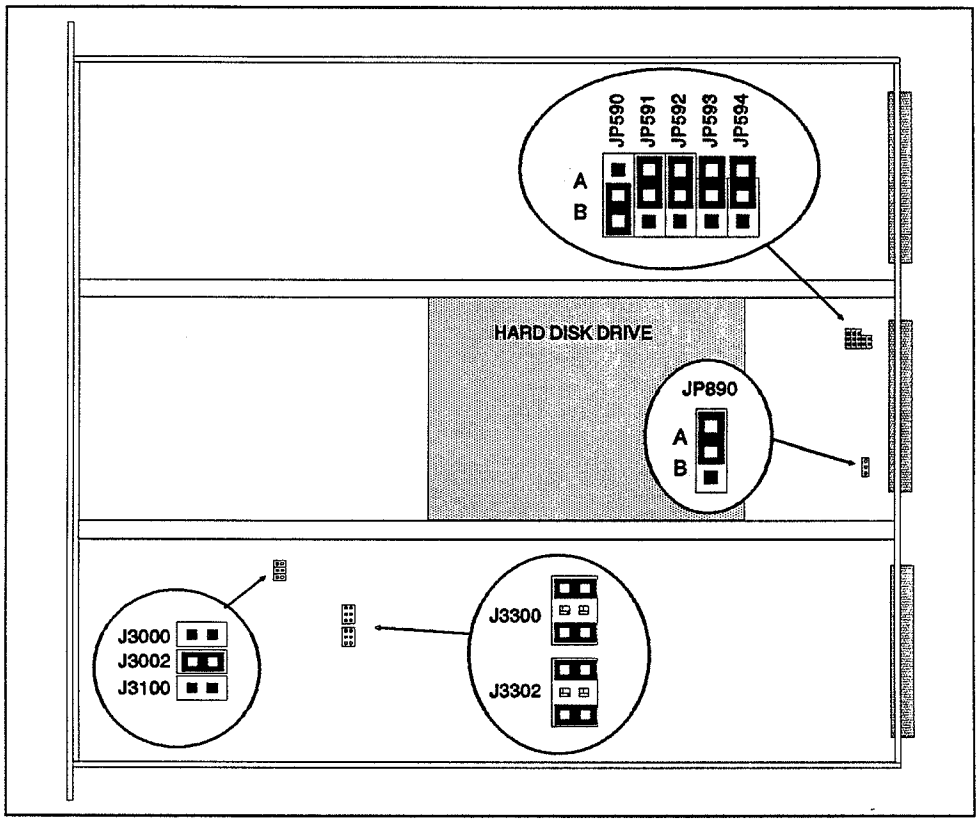


Figure 2-1. Jumper locations.

be enabled only by one module in the mainframe, otherwise the VX5530/VX5535 will not operate properly. If more than one VX5530/VX5535 are installed in the same mainframe, only one may be configured for Slot 0, the second VX5530/VX5535 must be configured for Non-Slot 0 operation.

Table 2-1 Jumper Configuration Settings

Operation Mode	JP590	JP591	JP592	JP593	JP594	JP890
Slot 0	A	B	A	A	A	A
Non-Slot 0	A	B	B	B	B	B

VXIbus Mainframe Jumper Configurations

Before installing the VX5530/VX5535 in the VXIbus mainframe, make sure that mainframe configuration jumpers (if any) are set for your required mode of operation. Refer to the appropriate mainframe instruction manual.

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Module Installation

When the hardware configuration is completed, replace the right side cover and install the VX5530/VX5535 module in the properly configured mainframe slots.

To Install The Module:

1. Turn off main power ON/OFF switches on the VXIbus mainframe and set front-panel ON/STANDBY switch to STANDBY.

2. Insert the module into the top and bottom mainframe guides for the chosen slot position(s) and push it partially into the Mainframe. Pull out the Injector/Ejector Handles to their fully extended position (see the INJECT and EJECT views of Figure 2-2). Push the upper handle fully up and the lower handle fully down.

3. Push the module into the Mainframe as far as it will go without forcing it. Simultaneously pull the upper Injector/Ejector Handle fully down and the lower handle fully up to INJECT the module.

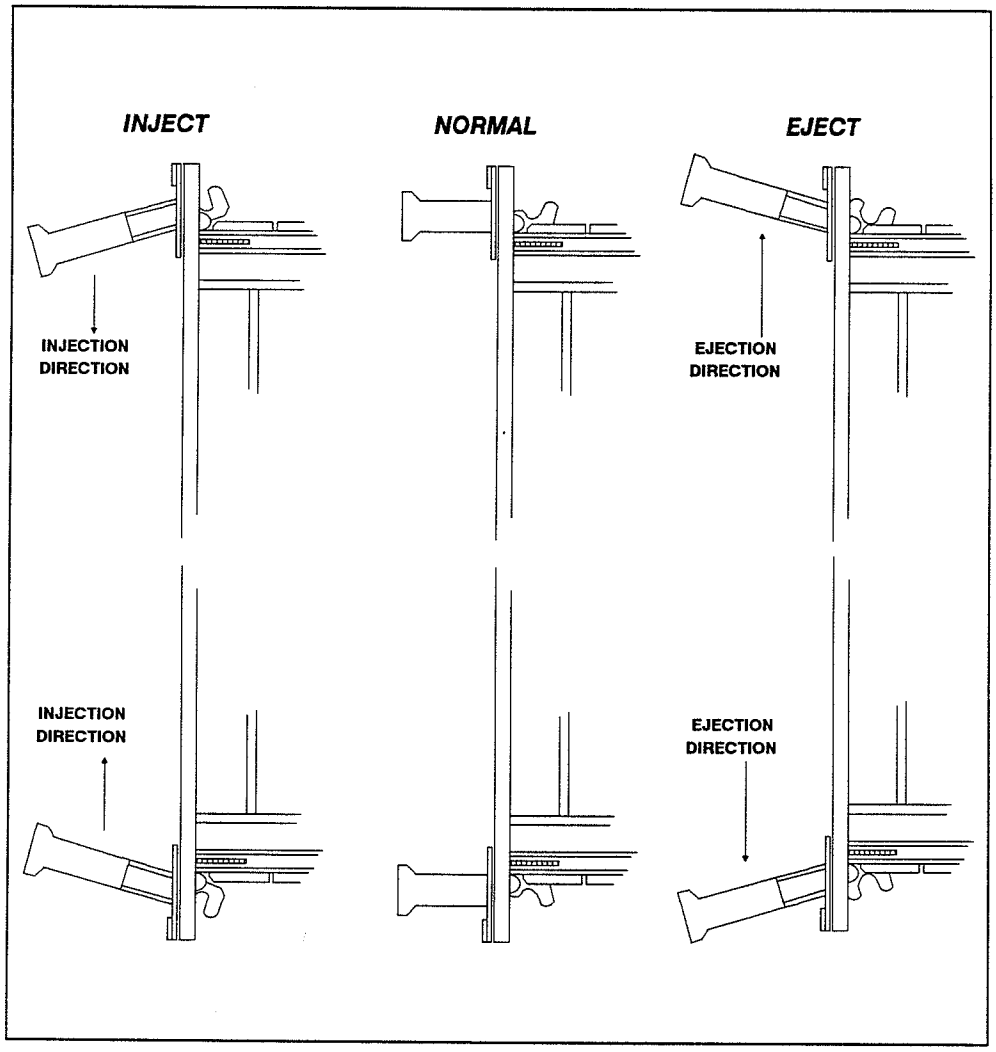


Figure 2-2 Module Installation

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4. Make sure that the module is fully seated into its VXIbus connectors and that the front panel is flush with the front of the Mainframe chassis.

5. Install the top and bottom module retainer screws to secure the module in the Mainframe. Push in the Injector/Ejector Handles and set them to a level horizontal position (see NORMAL view in Figure 2-2).

To Remove The Module:

1. Turn off main power ON/OFF switches on the VXIbus mainframe and set front-panel ON/STANDBY switch to STANDBY.

2. Remove the top and bottom module retainer screws.

3. Pull out the Injector/Ejector Handles to their fully extended position (see the INJECT and EJECT views of Figure 2-2). Simultaneously push the upper Injector/Ejector Handle fully up and the lower handle fully down to EJECT the module. When EJECTed the module can be removed from the Mainframe.

4. Push in the Injector/Ejector Handles and set them to a level horizontal position (see NORMAL view in Figure 2-2).

Keyboard and Monitor Installation

To install the keyboard and monitor, simply plug their cable connectors into the front-panel connectors marked KEYBOARD and VGA MON, respectively. Refer to the discussion of the Keyboard and VGA Monitor connectors in Section 3, Operation, for more information about keyboards and monitors compatible with the VX5530/VX5535.

Serial Mouse Installation

Connect the mouse cable connector to the front-panel connector marked COM1or COM2.

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Software Installation

Directory Structure

The VX5530/VX5535 is shipped with all software installed onto the hard disk. The system is complete and ready to use. The hard disk is partitioned into two 20 MB drives, C: and D:. The C drive is intended for system and program files. The D drive is intended for data files.

The C: directory structure is laid out thusly:

\tekvics	Tektronix TekVICS software
\dos	DOS system files
\win386	Microsoft® Windows/386
\bin	The INTERCHANGE from Systems Manufacturing Technology
\mouse	Logitech mouse files
\basic	Microsoft® BASIC compiler
\msc	Microsoft® C compiler
\tektms	TekTMS system software
\temp	Temporary file directory

Special Files

The following are special files to DOS and the user and are located in the top-level directory

readme.txt	Is the final documentation concerning this software and hardware release. It contains installation directions, plus last minute documentation that didn't make it into the manuals at press time.
config.sys	This file is read when DOS boots. It sets certain system parameters and loads drivers. This is where the directive is that loads the Bus Interface Manager.
autoexec.bat	Is executed by the command interpreter as a batch file after **config.sys** is processed. It sets any environment parameters and starts TSRs (terminate and stay resident programs). Language packages such as Microsoft® C also edit this file as part of their installation.

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Bus Interface Manager Installation

The Bus Interface Manager combines the Message Delivery System (MDS) and the BusManager into a single device driver. It comes installed appropriately in **config.sys** so that the typical user never has to worry about it. The following describes the **config.sys** parameters so that you can change them to fit your particular needs.

The Bus Interface Manager is installed as a DOS device. The format of the line in **config.sys** is

```
device=\tekvics\bimgr.sys/Q=<ersize>/D=<mediasize>
/S=<routesize> /B=<bmqsize> /t=<timer>
```

Where:

<ersize> Number of MDS Event/Response queue entries. Events and responses sit in this queue waiting for application programs to read them. It must be large enough to handle all of the outstanding events and responses, typically one per device. Legal values are 1 to FF. Defaults to F.

<mediasize> Number of MDS Media Table entries. Each different type of MSD media (VXIbus, GPIB, each network connection, each embedded servant, etc.) consumes one entry. If the table is too small, not all devices can be configured and an error message is generated at system initialization. Legal values are 1 to FF. Defaults to F.

<routesize> Number of MDS Router Table entries. Each device consumes one table entry. When the table is full, no new devices may be added. Legal values are 1 to FF. Defaults to F.

<bmqsize> Number of BusManager Event/Response queue entries. This queue holds "bursts" of events and responses while the MDS is busy. If this table fills, devices sending events and responses lock up until space is made available by MDS. Legal values are 1 to FF. Defaults to 10.

<timer> Watchdog timer speed. May be "**F**" for fast (134 msec) or "**S**" for slow (8.9 sec). Defaults to slow.

After initialization, the VXIbus window points to A16 space in Motorola (big endian) byte order. Because of this, configurations that use only VXIbus A16 space can access the VXIbus at E000:0000 through E000:FFFF without changing the mapping.

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Advanced Trigger Functions Driver Installation

The Advanced Trigger Functions driver **atf.sys** is used to directly control the ATF hardware. The ATF driver is installed as a DOS device driver. The format of the line in **config.sys** is:

```
device=\tekvics\atf.sys <hwconfg>
```

where:

<hwconfg> Indicates the Advanced Trigger Functions hardware configuration. Since the ATF hardware can be installed with either one or three STARbus routing units, this parameter is used to indicate the hardware option. Legal values are 1 or 2 as follows:

1 One STARbus routing unit installed (Option 01)
2 Three STARbus routing units installed (standard)

Reinstalling Software

When reinstalling software on the VX5530/VX5535 you need to be aware that there are two types of Conner 40MB 3.5" hard drives that may have been originally installed on them. One is the CP340 and the other is the CP3040. Each drive requires different settings when reinstalling software. Therefore, before reinstalling software on either disk, the disk type should be verified.

To verify the disk type:

1. Boot the system.

2. Wait for the POST (Power-On Self-Test) to complete its operation.

3. Watch the screen for the following display:

   ```
   SCSI Fixed Disk Type : <type display>
   ```

   where < type display> will be one of the following:

   ```
   CONNER Cp340 (40mb 3.5)
   CONNER Cp3040 (40mb 3.5)
   ```


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Once the disk type is determined, the following settings are used:

For the CP340:

	VX5530	VX5535
Interleaving	1:4	1:3
Cylinders	788	788
Heads	4	4
Sectors	26	26

For the CP3040:

	VX5530/VX5535
Interleaving	1:2
Cylinders	1023
Heads	2
Sectors	40

To reload the hard drive:

1. Perform any necessary formatting and partitioning of the drive using the above settings.

To partition the drive, boot from the DOS distribution disk, and load the FDISK program. Follow the instructions in the DOS manual. The drive is partitioned at the factory into two 20MB partitions, C: and D: (512 and 510 cylinders respectively). Do not forget to make partition 1 active. If you forget, the drive will not be bootable.

Format the drives as follows

```
A>FORMAT C: /S /V (Creates a Bootable disk)
A>FORMAT D: /V
```

2. Create a DOS directory and copy the files on the DOS distribution disk to it.

```
A>C:
C>MKDIR\DOS
C>COPY A:*.* C:\DOS
```

3. Create a MOUSE directory and copy the files on the MOUSE distribution disk to it.

```
C>MKDIR\MOUSE
C>COPY A:*.* C:\MOUSE
```


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4. Install the TekVICS Software by placing the distribution disk in drive A: and running the install program.

```
C>A:
A>INSTALL
```

5. Install the Microsoft® C Compiler, following the directions that come with the product. The compiler comes configured from the factory with the following defaults:
   - Product installed in **\msc** directory
   - Product library files installed in **\msc\lib**
   - Product include files installed in **\msc\include**
   - Product source files installed in **\msc\sources**
   - All libraries built at factory

6. Install the Microsoft® BASIC Compiler, following the directions that come with the product. The compiler comes configured from the factory with the following defaults:
   - Product installed in **\BASIC** directory
   - Product library files installed in **\BASIC\LIB**
   - Product include files installed in **\BASIC\INCLUDE**
   - All libraries built at factory

7. Install Microsoft® Windows/386, following the directions that come with the product. Windows comes configured from the factory with the following defaults:
   - Product installed in **\WIN386**
   - System type : Compaq/386 or compatible
   - Keyboard : US Keyboard
   - Mouse : Logitech Mouse
   - Display : VGA (other drivers on TekVICS disk)
   - Printer : HPLaserJet—Lpt1:
     : AppleLaser—Lpt2:
     : Epson FX-80—Lpt3:

   Place the Windows/386 system files in the root directory.

   ```
   C>COPY *.SYS C:\
   ```

   Create a directory for the Window/386 system files.

   ```
   C>MKDIR\TEMP
   ```

8. Install TekTMS, following the directions that come with the product. The compiler comes configured from the factory with the following defaults:
   - Product installed in **\tektms** directory

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9. Create the system files in the root directory.

```
C>CD\
C>copy con:config.sys
files    = 20
buffers  = 20
stacks   = 0,0
device   = c:\dos\ansi.sys
device   = c:\himem.sys
device   = c:\smartdrv.sys 256   (512 if VX5535)
device   = c:\tekvics\gpib.com
device   = c:\tekvics\BImgr.sys
device   = c:\tekvics\ATF.sys    (1 if Option 01)
shell    = c:\command.com /e:512 /p
^Z (Control-Z)

C>copy con:autoexec.bat
prompt $p$g
path c:\;c:\dos;c:\win386;c:\tekvics;
set  epconnect = c:\tekvics
mouse
teklogo
CLS
Cbridge
VXIBrdg
GPIBrdg
SURM
Set TEMP = c:\temp
set include = c:\BASIC\include;c:\msc\include;
              c:\tekvics\include;
set lib = c:\BASIC\lib;c:\msc\lib;c:\tekvics\lib;
win386
^Z (Control-Z)
```

NOTE

Before GPIBRDG is loaded, gpib.com must be loaded. This is done in config.sys with a line as follows:

```
device=c:tekvics\gpib.com
```

If the bridge was successfully loaded, the following message will appear

```
"GPIB Bridge Loaded"
```

If the bridge was not successfully loaded, a diagnostic message will indicate the reason. Any of three conditions may exist: 1) gpib.com was not loaded, 2) MDS was not loaded, 3) TEKDEV1 is not installed in gpib.com. If TEKDEV1 is not found in gpib.com, use the IBCONF program to rename a device to TEKDEV1—no other changes are necessary.

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Section 3
Operation

Front Panel Control, Indicators, Connectors, and Disk Drives

The front panel contains five indicators (RUN, SYSTEM FAIL, TEST, HARD DISK, and a floppy drive indicator), eight connectors (VGA MON, KEYBOARD, COM1, COM2, IEEE 488, LPT1, and EXT CLOCK), and a RESET pushbutton.

Control

RESET

This pushbutton reboots the VX5530/VX5535 System Controller.

Indicators

RUN

A green LED that indicates the module is operating. This LED is lit as soon as the module is turned on, then flickers to show that the processor is operating correctly. When it is the only LED lit (excluding the DRIVE indicator), the module is ready for normal operation.

SYSTEM FAIL

A red LED that indicates the VXIbus SYSFAIL* signal line is asserted. This LED is lit as soon as the module is turned on, then extinguishes after the TEST indicator is extinguished, and the module is ready for normal operation.

TEST

A yellow LED that indicates the module is performing self-tests. This LED is lit as soon as the module is turned on, then extinguishes when the power-up self-tests are successfully completed. If a failure occurs during self-test, or the self-tests take longer than 5 seconds, the power-up sequence halts and the LED remains lit.

HARD DISK

A green LED that is lit whenever the hard disk drive is active.

Floppy Drive Indicator

An amber LED that is lit whenever the floppy disk drive is active.

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Connectors

VGA MON

This connector is driven by a Paradise PVGA1A VLSI circuit to provide a fully IBM VGA compatible, 15-pin, D-type, connector for attaching a VGA compatible analog-input color monitor. VGA monitors may be either color or gray-scale devices. A Software Setup Configuration topic later in this section explains the procedure for making a setup selection.

Multisync-type monitors can be used if they support analog inputs (some compatible multisync monitors have an analog/TTL switch that must be set to analog when used with the VX5530/VX5535). Normal EGA, CGA, or monochrome monitors cannot be used with the VX5530/VX5535.

The VGA BIOS is copied into the high-speed, 32-bit RAM on power up, which doubles the performance over running out of ROM. The VX5530/VX5535 provides a 16-bit data path to the video memory, thus further increasing the graphics performance of the module. This BIOS supports VGA (640 x 480) mode, and emulates all standard IBM EGA, CGA, and monochrome modes.

The VX5530/VX5535 can use any monitor designed to replace IBM VGA monitors, including models 8503, 8512, 8513, and 8514. Monitors with only TTL inputs (EGA, CGA, and monochrome) cannot be used.

Table 3-1 Characteristics Of Compatible VGA Monitors

Monitor Type	Scan Rate	Refresh Rate	Video Rate	Resolution
VGA Standard	31.5 KHz	60 or 70 Hz	26 MHz	640 x 480 720 x 400
Multisync	15-35 KHz	50-80 Hz	30 MHz	800 x 600 maximum

KEYBOARD

This connector provides an IBM PC-AT compatible, 5-pin, circular, DIN connector for attaching a keyboard to the VX5530/VX5535.

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LPT1

This connector provides an IBM PC-AT and Centronics compatible, standard 25-pin, D-type parallel output port for a printer, or it can be changed to a parallel input port for a scanner using the Software Setup Configuration function included with the VX5530/VX5535, and explained later in this section. The power-up default is as an output port.

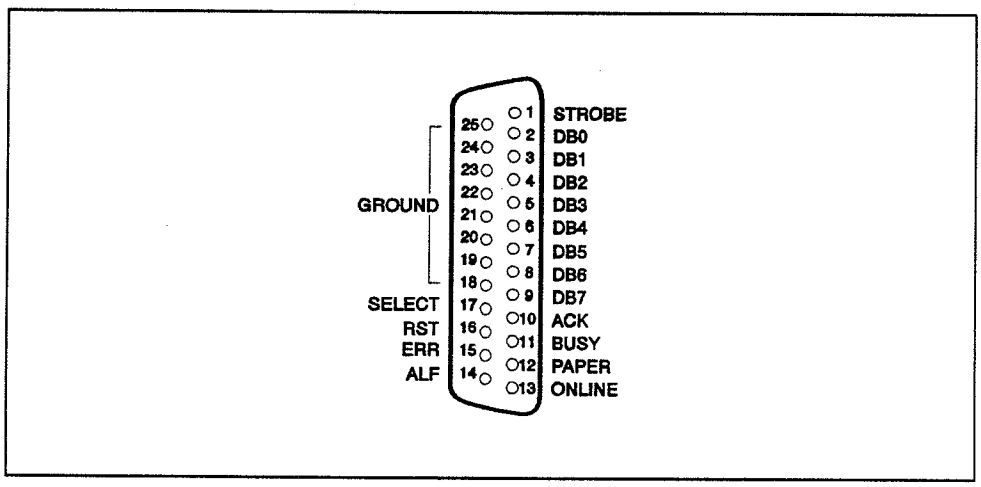


Figure 3-1. Parallel port connector pin assignments.

COM1
COM2

These connectors are IBM PC-AT compatible, standard 9-pin male, D-type, DCE-configured, asynchronous, RS232 I/O ports. COM 1 and COM 2 connector pin assignments are shown in Figure 3-2 and Table 4-5.

The communications parameters for COM1 and COM2 are:

Echo:	on
Baud:	9600
Data Bits:	8
Stop Bits:	1
Parity:	odd

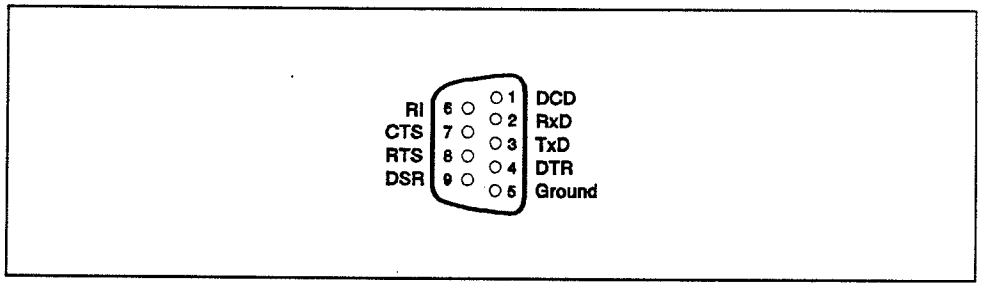


Figure 3-2. COM 1 & 2 port connector pin assignments.

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IEEE 488

This connector provides an IBM PC-AT compatible, 24 pin, GPIB interface. IEEE-488 connector pin assignments are shown in Figure 3-3 and Table 4-5. The IEEE 488 Subsets implemented are:

Function	Subset	Capability
Controller-in-charge	C1-6 & C16	Transfer rate - 250 kilobytes/second
Talker/Listener	T5 & L5	Transfer rate - 250 kilobytes/second

TRIG IN A, B

These BNC input connectors accept a TTL level trigger signal. It may be sourced into either ITB(6)—from TRIG IN A, or ITB(4)—from TRIG IN B.

TRIG OUT A, B

These BNC output connectors source a TTL level trigger signal. It has selectable polarity and can source ITB(0...7).

Disk Drives

The VX5530/VX5535 contains two disk drives. One is a 3.5 inch, 1.44MB flexible (floppy) disk drive that can read and write both 720KB and 1.44MB floppy disks, and the other is a 40MB hard disk drive. The Software Setup Configuration allows the floppy disk to be set for 720KB (NONE mode) or 1.44MB (1.4M mode).

Activity on the floppy disk is indicated by an LED on the drive's front panel.

Activity on the 40MB hard disk is indicated by a green LED marked HARD DRIVE.

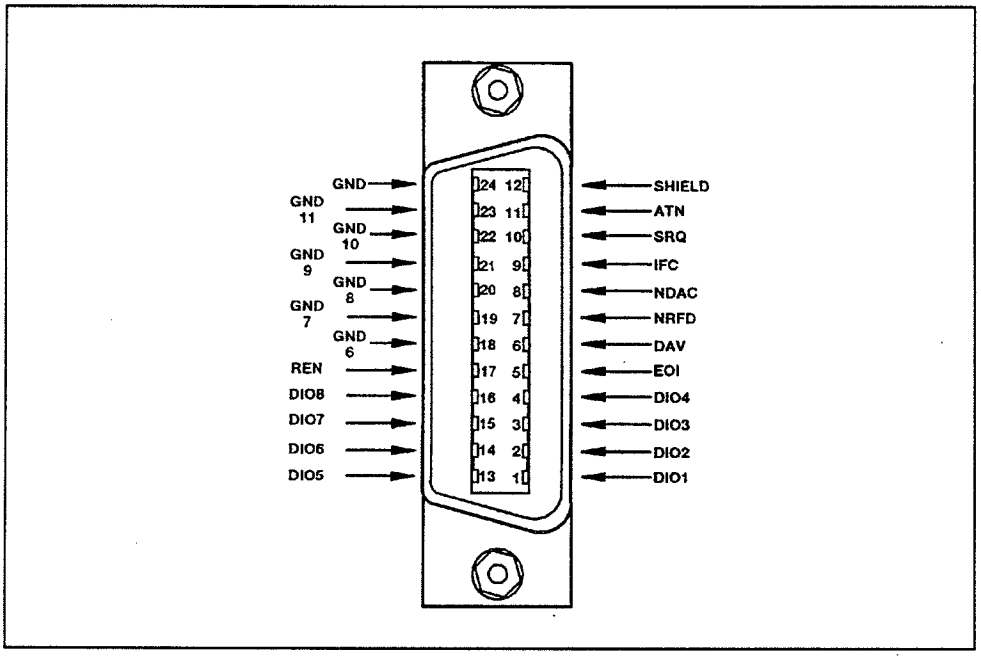


Figure 3-3. IEEE-488 connector pin assignments.

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Initial Power-up Sequence

Power-up Diagnostics

Turn on the monitor and power up the VX5530/VX5535 system.

First, the SYSFAIL, RUN, and TEST indicators on the module will be lit. The screen will go blank and the RUN indicator will flicker, indicating that the processor is operating correctly. The system will begin executing power-on self-test (POST) diagnostics, checking memory and the other hardware on board. As these tests proceed, the monitor will display test progress and results. For a 2 MB system, the screen should look like Figure 3-4, although version numbers for the BIOS and SCSI drivers may vary. With an 8 MB system the memory sizing and testing lines will be different, indicating the actual amount of memory found and tested. After checking the hardware, the system configuration is checked. Both the floppy and hard disk activity indicators will flash.

When the POST is completed, the red and yellow SYSFAIL and TEST indicators on the front panel are extinguished, and the system loads its operating system from disk. If a floppy disk is present, the system will boot from it; otherwise the hard disk will be used, and the hard disk indicator will be lit almost continuously during this period.

```
386 Modular BIOS Version 3.03, Copyright Award Software
 Copyright 1988 Radix MicroSystems, Inc. BIOS V2.05

 TESTING INTERRUPT CONTROLLER #1  . . . . . OK
 TESTING INTERRUPT CONTROLLER #2  . . . . . OK
 TESTING CMOS BATTERY . . . . . OK
 TESTING CMOS CHECKSUM  . . . . . OK
 SIZING SYSTEM MEMORY . . . . . .640K FOUND
 TESTING SYSTEM MEMORY  . . . . . .640K OK
 CHECKING UNEXPECTED INTERRUPTS AND STUCK NMI . . . . . OK
 TESTING PROTECTED MODE . . . . . OK
 SIZING EXPANSION MEMORY  . . . . . .01024K FOUND
 TESTING MEMORY IN PROTECTED MODE . . . . . .01664K OK
 TESTING PROCESSOR EXCEPTION INTERRUPTS . . . . . OK
 TESTING VME INTERFACE  . . . . . OK
 TESTING VXI INTERFACE  . . . . . OK
 TESTING IEEE 488 INTERFACE . . . . . OK


 SCSI Disk L BIOS Version 1.00
 Copyright (c) 1988 Award Software Inc.

 SCSI Fixed Disk Type: CONNER Cp340 (40mb 3.5)
```

Figure 3-4. Power-on Self Test Screen (VX5530).

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When the DOS boot process is complete, the start-up resource manager will run, determining the VXIbus system configuration and displaying it for the user. To exit the resource manager to DOS, press the escape key twice. The resource manager documentation describes how to configure it to come up in other modes.

In the rare case where the VX5530/VX5535 is not configured as a slot-0 controller, the start-up resource manager must not be executed. Consult the resource manager documentation for methods to remove or disable the resource manager. In these cases, instead of the resource manager window, you will see the DOS prompt C>, indicating that the system has booted DOS correctly and is ready to load and execute your programs.

If any serious POST problems are detected, the process will halt and display an appropriate message on the screen between the "TESTING VXIbus INTERFACE" and "SCSI Disk..." lines. Configuration errors are caught after the POST procedures have confirmed basic hardware functionality, and display after the "SCSI Disk..." messages.

Set-up Program

The first time the system is powered up you may wish to enter the set-up mode to configure the VX5530/VX5535 software controlled options. You will also need to enter this mode if a "configuration mismatch" warning was generated when the system powered up.

Enter configuration mode by simultaneously pressing the ALT-CTRL-ESC keys during the POST process, before the system starts booting. The default configuration is shown in Figure 3-5.

The setup program allows the user to configure both the normal PC-type features of the CPU, as well as the VMEbus and VXIbus features. This information is then stored in non-volatile memory, where it is used whenever the CPU is rebooted.

```
                    VX5530 SETUP SCREEN
            16 MHZ CPU WITH 387 AND 2 MBYTE MEMORY


DATE (MM/DD/YY HH:MM:SS)    1/02/89              09:34:56
               ERROR HALT   HALT ON ALL ERRORS

   DISKETTE DRIVES A & B    1.4M         &       NONE
             SCSI DRIVER    ENABLED

           BUS PRIORITY     PRI 3
   BUS RELEASE MECHANISM    RONR (VXI)
         BUS ARBITRATION    PRIORITY
        SLOT 0 FUNCTIONS    INTERNAL CLOCK

     PARALLEL PORT MODE     NORMAL (PRINTER)
             VGA MONITOR    COLOR
```

Figure 3-5. Default configuration of setup screen.

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The up and down cursor keys move you between the set-up parameters: the left and right cursor keys rotate through the choices available for any parameter. If necessary, set the time and date by typing the desired information into the field, then set the rest of the configuration parameters. When the system is correctly configured, press F10, then F5, to save the results and reboot.

The individual options are discussed below.

Error Halt

This option controls how the system responds to errors during the POST process. There are several options available. The default is HALT ON ALL ERRORS (which does just that). Self-explanatory options range from IGNORE KEYBOARD ERRORS (useful when a system doesn't have a keyboard) through IGNORE ALL ERRORS.

Diskette Drives A & B

Since the VX5530/VX5535 has a single 3.5" 1.44 MB floppy disk drive that can read and write both 720K and 1.44MB diskettes, leave these parameters at the default settings of 1.44M and NONE.

SCSI Driver

This rarely-used option disables the SCSI driver, and allows you to disable all accesses to hard disk by causing the boot process to skip the SCSI bus initialization and device configuration. It is useful when testing software that may damage information on the hard disk.

If you need to reformat the hard disk, the function key F3 moves you to another dialog screen that lets you perform these functions. The procedure is defined in detail later in this section.

Bus Priority

Whether or not the VX5530/VX5535 is the slot-0 controller, it is a bus master and needs to use a specific bus grant signal to request bus access. This option selects the signal used. Higher numbers (they range from 0 to 3) have higher access priority.

Bus Release Mechanism

The VX5530/VX5535 can use either of two bus release mechanisms. The options are ROR, which is a standard VMEbus mechanism, and RONR, the VXIbus specified fair requestor protocol.

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Bus Arbitration

If the VX5530/VX5535 is providing bus arbitration for the system (which it will be if it is the slot-0 controller), then there are two available methods. PRIORITY arbitration implies that the bus request lines with higher numbers have higher priority. ROUND ROBIN implies that all bus request lines have equal priority and are essentially time-sliced.

These options have no effect if the VX5530/VX5535 is not the slot-0 controller.

Slot 0 Functions

When the VX5530/VX5535 is configured as the slot-0 controller, there are two relevant clock options. INTERNAL CLOCK selects an on-board 10MHz clock to drive the ECL backplane clock. EXTERNAL CLOCK uses the front-panel clock input for the clock source.

If the VX5530/VX5535 is not the slot-0 controller, the NONE option should be selected.

Parallel Port Mode

The parallel port can be configured into either of two modes. The NORMAL (PRINTER) mode is just that. The ports buffers are set to drive a Centronics standard output device. The second mode, INPUT ONLY (SCANNER), is used when a parallel-port input device is used.

VGA Monitor

VGA monitors are either color or gray-scale devices. This option allows the user to set the video accordingly.

Common Initial Power-up Problems

Monitor

There are only a few power-up problems that can occur. All are easy to correct.

Symptoms: the monitor cable doesn't fit the video connector.

This indicates that your cable is designed for use with an EGA video controller, which uses a 9-pin connector. VGA controllers use 15-pin connectors. Many multi-sync monitors are shipped with both cables, or with a cable adapter for VGA systems. Use the cable or cable adapter with the 15-pin VGA connector that came with your monitor.

Symptoms: the monitor displays nothing, display has "snow," or the colors are either washed out or too intense.

These are typically connection or cable problems, conditions alleviated by using a grounded, shielded cable between the monitor and the VX5530/VX5535. Make sure the cable is well attached to the VX5530/VX5535 by using the jackscrews on the cable.

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This problem can also occur if an analog/TTL monitor is configured for TTL input. Make sure the monitor is set for analog.

Symptoms: the monitor display is jittery or garbled.

This indicates that the monitor itself is not synchronizing with the incoming video signals, and is not unusual when a analog/TTL monitor has just been moved from an EGA environment. Change the horizontal and vertical sync adjustments on the monitor until the display is correctly aligned.

Power-on Self Test Errors

Only one condition generates a message after the basic POST messages but before the SCSI messages.

```
Keyboard Error Or No Keyboard Present
```

This occurs when the keyboard is not plugged into the VX5530/VX5535 correctly, or if keys are depressed while POST is executing. During the POST procedure the keyboard indicators (cap lock, etc.) should flash on and off once, verifying to the user that the keyboard is plugged in.

Configuration Errors

The following messages may be displayed after the "`SCSI Disk BIOS ..`" line in Figure 3-3.

```
SCSI Disk Failed
```

This message indicates the BIOS did not find a disk drive, and replaces the "`SCSI Disk Type:...`" message. If this problem occurs after having had the side cover off to change the slot-0 configuration jumpers, go back and check the disk drive power cable and data cable for correct seating.

```
Diskette Drives Or Types Mismatch Error Run Setup
```

If this message appears after the "`SCSI Drive Type:..`" message, one of two situations exists. If the VX5530/VX5535 is not expecting a 1.4M drivefor diskette A, and NONE for drive B (as shown in Figure 3-5), reset the configuration by resetting the VX5530/VX5535 and entering the set-up procedure as described previously. If the configuration is correct, then a drive cable (either the power or data cable) has probably been knocked loose during slot-0 re-configuration.

Other Errors

If any other errors occur, or if the POST indicates that any test failed, contact your local Tektronix field office representative.

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Reformatting And Reinitializing SCSI Drives

The following describes the processes required to reformat and reinitialize a SCSI disk drive in an VX5530/VX5535. Because all the software needed to add and initialize a SCSI hard disk is included in the BIOS ROM of the VX5530/VX5535, the process is very straightforward. The discussion assumes DOS will be run on the VX5530/VX5535: if this is not the case, follow Step 1 to format the drive and use the instructions in the Operating System manual for initializing, partitioning the drive and loading software.

CAUTION

The VX5530/VX5535 SCSI drive is formatted and initialized at the factory. The procedures outlined in this section will completely and irretrievably erase all the information on a drive. Make sure you understand the procedures before you use them to format and initialize a working drive.

Step 1: Formatting A Drive

Reset the system with the front-panel switch. Watch the POST process closely, and after the SCSI BIOS... message appears on the screen (see Figure 3-4), press CTL-ALT-ESC simultaneously to get into the Set-up mode. Then press F3 to enter the SCSI setup screen. If the message "SCSI Driver not loaded" appears, restart the system and wait a little longer before breaking into set-up with CTL-ALT-ESC.

You are now ready to format the disk. First, press F1 to do a low level format. Low-level formatting includes setting the interleave factor on the disk. For information about disk settings and how to format the disk, see *Reinstalling Software* in *Section 2, Preparation for Use*. Do not use the BIOS formatter to split the drive into multiple volumes, this can be done more flexibly later, using standard DOS utilities. Finally, to prevent unauthorized access to the hard disk, you can use the F3 function to set a password. When you are done with all this, exit to setup, and use F10 / F5 to reboot. The SCSI drive has now been formatted, and is ready for the DOS initialization and formatting utilities.

Step 2: Initializing The Drive

At this point, when the system boots it will not find anything on the hard drive, though it will show the manufacturer's information. Insert a DOS system disk in the floppy drive and boot from it.

First run FDISK, following the instructions in the DOS manual. No drive specification is necessary.

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Step 3: DOS Formatting And Copying The System Files

After running FDISK the system will reboot (still from floppy). Now run the DOS SELECT command, as follows:

```
A> SELECT C:\DOS 001 US
```

At this point the hard disk has been formatted, initialized, and set up to be a bootable disk. When the system is reset, it will boot from the hard disk without further action required, and the system is ready to accept installation of other applications.

Notes On SCSI Drives With Embedded Controllers

SCSI drives behave differently than older styles (ST506, 412 or ESDI) in that all sectors on the drive are referenced by logical sector numbers, as opposed to track/head/sector triplets. This simplifies driver software by making it independent of drive type, size, and mechanical configuration. Drive formatting and similar hardware-related procedures are also simplified, since the drive has the intelligence internally (in the controller) to know what the appropriate parameters are. All that is left to the user is to determine and specify the optimum interleave factor, which will be a function of the host interface.

DOS keeps a "drive configuration table" for every drive in the system, and stores the table on the disk in a special sector. This is read into memory when the system is booted, and used by the BIOS. The table is used to convert a DOS logical sector number (used by the DOS file system) into track/head/sector triplets used by the standard BIOS disk driver for accessing the disk. The SCSI driver then converts this triplet into a SCSI logical sector number.

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Section 4
Connector Definitions

Front Panel Connectors

Table 4-1 TRIG IN and TRIG OUT BNC Connectors

Connector Name	Communication Direction	ITB Channel	Description
TRIG IN A	Input	ITB(6)	Accepts a TTL level trigger signal.
TRIG IN B	Input	ITB(4)	Accepts a TTL level trigger signal.
TRIG OUT A	Output	ITB(0...7)	Sources a TTL level trigger signal. Has selectable polarity
TRIG OUT B	Output	ITB(0...7)	Sources a TTL level trigger signal. Has selectable polarity

Table 4-2 VGA MON Pin And Signal Assignments

Pin Number	Signal Name	Communication Direction	Description
1	Red	Output	Red Signal Data
2	Green	Output	Green Signal Data
3	Blue		Blue Signal Data
4	nc		
5	Gnd	Output	Ground
6	Gnd	Output	Ground
7	Gnd	Output	Ground
8	Gnd	Output	Ground
9	nc		
10	Gnd	Output	Ground
11	nc		
12	nc		
13	H Sync	Output	Horizontal Sync
14	V Sync	Output	Vertical Sync
15	nc		

Red, green, and blue signals are analog signals; horizontal and vertical sync signals are active-HIGH TTL signals.

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Table 4-3 KEYBOARD Pin And Signal Assignments

Pin Number	Signal Name	Communication Direction	Description
1	CLK	Input/Output	Serial Clock
2	DATA	Input/Output	Keyboard Data
3	nc		
4	Ground		
5	+5V		Keyboard Power

Table 4-4 PRINTER Pin And Signal Assignments

Pin Number	Signal Name	Communication Direction	Description
1	Strobe*	Input/Output	Indicated Valid Data
2	DB0	Input/Output	Data Bit 0
3	DB1	Input/Output	Data Bit 1
4	DB2	Input/Output	Data Bit 2
5	DB3	Input/Output	Data Bit 3
6	DB4	Input/Output	Data Bit 4
7	DB5	Input/Output	Data Bit 5
8	DB6	Input/Output	Data Bit 6
9	DB7	Input/Output	Data Bit 7
10	ACK*	Input	Printer Acknowledge
11	BUSY	Input	Device Unavailable
12	PAPER	Input	Printer's Out of Paper
13	ONLINE	Input	Printer's On-Line
14	ALF*	Output	Enables Auto Line Feed
15	ERR*	Input	Device Error
16	RST*	Output	Reset Device
17	SELECT*	Output	Select Device
18-25	Ground		

*Signals followed by an asterisk are negative true TTL logic; signals without the asterisk are positive true TTL logic. The direction of the data buffers (for input or output) is controlled by the Parallel Port Mode parameter (NORMAL or INPUT ONLY [SCANNER]), which can be set with the setup configuration software.

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Table 4-5 COM1 and COM2 Pin And Signal Assignments

Pin Number	Signal	Communication Direction	Description
1	DCD	Input	Data Carrier Detect
2	RxD	Input	Received Data
3	TxD	Output	Transmitted Data
4	DTR	Output	Data Terminal Ready
5	Ground		Signal Ground
6	DSR	Output	Data Set Ready
7	RTS	Output	Request to Send
8	CTS	Input	Clear to Send
9	RI	Input	Ring Indicator

All signals are buffered with standard RS232 drivers and operate at +12 to -12V. Signals are TRUE at voltages below -5V. The static voltage levels of idle outputs will be -11V (nominal).

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Table 4-6 IEEE 488 Pin And Signal Assignments

Pin Number	Signal	Communication Direction	Description
1	DI01	Input/Output	Data I/O
2	DI02	Input/Output	Data I/O
3	DI03	Input/Output	Data I/O
4	DI04	Input/Output	Data I/O
5	EOI (24)	Output	End or Identify
6	DAV	Output	Data Valid
7	NRFD	Output	Not Ready For Data
8	NDAC	Output	Not Data Accepted
9	IFC	Output,Interface Clear	
10	SRQ	Input	Service Request
11	ATN	Output	Attention
12	Shield		
13	DI05	Input/Output	Data I/O
14	DI06	Input/Output	Data I/O
15	DI07	Input/Output	Data I/O
16	DI08	Input/Output	Data I/O
17	REN (24)	Output	Remote Enable
18	Gnd [6]		Gnd Rtn DAV
19	Gnd [7]		Gnd Rtn NRFD
20	Gnd [8]		Gnd Rtn NDAC
21	Gnd [9]		Gnd Rtn IFC
22	Gnd [10]		Gnd Rtn SRQ
23	Gnd [11]		Gnd Rtn ATN
24	Logic Gnd		Gnd Rtn EOI/REN

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VXIbus Interface Connectors P1, P2, and P3

Table 4-7 P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	−12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

nc = noconnection

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Table 4-8 P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	ECLTRG0	+5 V	CLK10+
2	–2 V	GND	CLK10–
3	ECLTRG1	RSV1	GND
4	GND	A24	–5.2 V
5	MODID12	A25	LBUS C00
6	MODID11	A26	LBUS C01
7	–5.2 V	A27	GND
8	MODID10	A28	LBUS C02
9	MODID09	A29	LBUS C03
10	GND	A30	GND
11	MODID08	A31	LBUS C04
12	MODID07	GND	LBUS C05
13	–5.2 V	+5 V	–2 V
14	MODID06	D16	LBUS C06
15	MODID05	D17	LBUS C07
16	GND	D18	GND
17	MODID04	D19	LBUS C
18	MODID03	D20	LBUS C09
19	–5.2 V	D21	–5.2 V
20	MODID02	D22	LBUS C10
21	MODID01	D23	LBUS C11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5 V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID00	D31	GND
31	GND	GND	+24 V
32	SUMBVS	+5 V	–24 V

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Table 4-9 P3 Slot 0 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	ECLTRG2	+24 V	+12 V
2	GND	–24 V	–12 V
3	ECLTRG3	GND	RSV4
4	–2 V	RSV5	+5 V
5	ECLTRG4	–5.2 V	RSV6
6	GND	RSV7	GND
7	ECLTRG5	+5 V	–5.2 V
8	–2 V	GND	GND
9	STARY12+	+5 V	STARX01+
10	STARY12–	STARY01–	STARX01–
11	STARX12+	STARX12–	STARY01+
12	STARY11+	GND	STARX02+
13	STARY11–	STARY02–	STARX02–
14	STARX11+	STARX11–	STARY02+
15	STARY10+	+5 V	STARX03+
16	STARY10–	STARY03–	STARX03–
17	STARX10+	STARX10–	STARY03+
18	STARY09+	–2 V	STARX04+
19	STARY09–	STARY04–	STARX04–
20	STARX09+	STARX09–	STARY04+
21	STARY08+	GND	STARX05+
22	STARY08–	STARY05–	STARX05–
23	STARX08+	STARX08–	STARY05+
24	STARY07+	+5 V	STARX06+
25	STARY07–	STARY06–	STARX06–
26	STARX07+	STARX07–	STARY06+
27	GND	GND	GND
28	STARX+	–5.2 V	STARY+
29	STARX–	GND	STARY–
30	GND	–5.2 V	–5.2 V
31	CLK100+	–2 V	SYNC100+
32	CLK100–	GND	SYNC100–

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Internal Sockets and Connectors

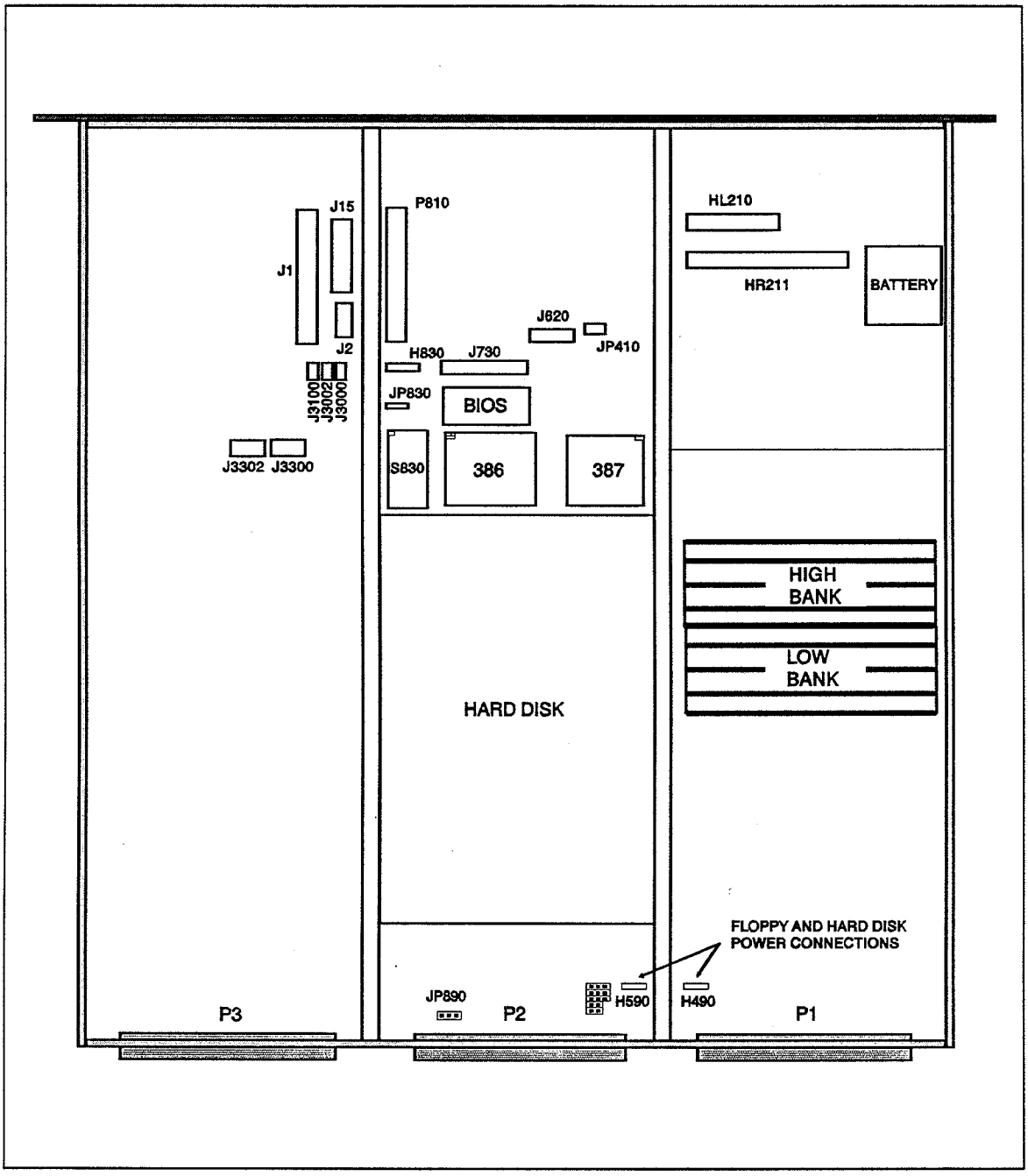


Figure 4-1. Internal connector locations.

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Table 4-10 Floppy Disk Connector (HL210)

Pin	On-Board Signal	Direction	Description
2	LDENS	out	read and write at high density
4	no connection		
6	no connection		
8	IDX	in	index mark seen
10	MO1	out	motor on
12	DS2	out	drive select
14	DS1	out	drive select
16	MO2	out	motor on
18	DIR	out	direction to step, (in or out)
20	STEP	out	step to next track
22	WD	out	write data
24	WE	out	write enable
26	T0	in	heads positioned at track 0
28	WP	in	media is write-protected
30	RDD	in	read data stream from disk
32	HS	out	selects head (side) 0 or 1
34	DCHG	in	drive door has been opened
all odd	ground		

All signals are low-true TTL with 48MA drive capability.

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Table 4-11 SCSI Connector (HR211)

Pin	Signal	Direction	Description
2	DB0	in/out	data bus low order bit
4	DB1	in/out	data bus bit 1
6	DB2	in/out	data bus bit 2
8	DB3	in/out	data bus bit 3
10	DB4	in/out	data bus bit 4
12	DB5	in/out	data bus bit 5
14	DB6	in/out	data bus bit 6
16	DB7	in/out	data bus high order bit
18	DBP	in/out	data bus parity bit
20-24	ground		
26	no connection		termination power
28-30	ground		
32	ATTN	in/out	attention
34	ground		
36	BSY	in/out	Bus busy
38	ACK	in/out	Acknowledge command
40	RST	in/out	Bus reset
42	MSG	in/out	enter message mode
44	SEL	in/out	select device
46	C/D	in/out	
48	REQ	in/out	
50	I/O	in/out	controls data direction
all	odd	in/out	

All signals are low-true TTL with 48MA drive capability.

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Table 4-12 Internal Test Interface (P810)

Pin	Signal	Pin	Description
1	A19	2	DB7
3	A18	4	DB6
5	A17	6	DB5
7	A16	8	DB4
9	A15	10	DB3
11	A14	12	DB2
13	A13	14	DB1
15	A12	16	DB0
17	A11	18	SMW*
19	A10	20	SMR*
21	A9	22	IOW*
23	A8	24	IOR*
25	A7	26	IRQ12
27	A6	28	CHCK*
29	A5	30	REF*
31	A4	32	DAK0*
33	A3	34	CHRDY
35	A2	36	IRQ3
37	A1	38	DRQ0
39	A0	40	ground
41	AEN	42	TC
43	V_{CC}	44	ground
45	OSC	46	BALE
47	V_{CC}	48	ground
49	RESET	50	SCLK

The internal test connector, located along the lower edge of the circuit board near the front panel, is described here. This connector is not available external to the VX5530/VX5535. The signals on this connector are a subset of the internal I/O bus, and similar to the PC-bus. The signals have minimal drive capacity and should not be extended.

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Section 5
Software Users Information

Configurator

The Configurator communicates system information that cannot be dynamically obtained from the VXIbus hardware devices to the Start-Up Resource Manager. The Configurator is a Windows application, and thus can be run only in a Windows environment.

The Configurator provides the following functions:

Symbolic device name relationships. The Start-Up Resource Manager can preassign symbolic (ASCII) names to VXIbus devices. To do this, it uses relationships established in the Configurator. The Configurator gives you a number of ways of expressing these relationships to the resource manager, such as name any Tektronix VX5260 device as "digitizer" and "name the device in slot 10 as 'dvm_1'".

Commander/servant hierarchies. The Configurator allows you to describe an arbitrary multilevel hierarchy of VXIbus devices. This information is used by the Start-Up Resource Manager.

Describing VMEbus devices. Since VMEbus boards can be used in VXIbus systems, the resource manager needs to know the static attributes of the VMEbus devices so that it doesn't create conflicts when dynamically configuring VXIbus devices. The Configurator gives you a way to describe VMEbus devices.

A second purpose of this information is to allow other software (e.g., the On Line Resource Manager) to deal with these devices as if they were VXIbus devices.

Manufacturer/model database. The system contains two files used by the resource manager to convert encodings of devices' manufacturer and model-number attributes into ASCII manufacturer and model names. The Configurator provides an interface for updating these files (e.g., to add a new VXIbus device).

GPIB device configurator. The GPIB Configurator allows the user to set various GPIB communication parameters for each instrument on the GPIB. These parameters are placed in a file and are accessed by the Startup Resource Manager to build an internal table for instrument communication.

Help menu. The Configurator also includes a Help menu for online help information.

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Symbolic Device Naming

This facility maintains a set of device naming relationships. Five types of relationships can be expressed:

1) Name to be assigned to a device having a specific manufacturer and model name.

2) Name to be assigned to a device having a specific manufacturer and model name and residing in a specific VXIbus slot.

3) Name to be assigned to a device having a specific logical address (usually useful only for VXIbus devices that do not support automatic assignment of their logical address).

4) Name to be assigned to a device in a specific VXIbus slot.

5) Name to be assigned to the nth device (implying a multidevice module) in a specific VXIbus slot.

Figure 5-1 shows an example of the appearance of the screen. Here several symbolic name relationships have already been established. They appearin a scrollable box in the center. The name that is currently selected appears above the box, and the relationship appears at the bottom. In this case (name TopCmdr), the relationship expressed is: if a device is found in slot 0 with a manufacturer name of Tektronix and model VX5530/VX5535, name it TopCmdr.

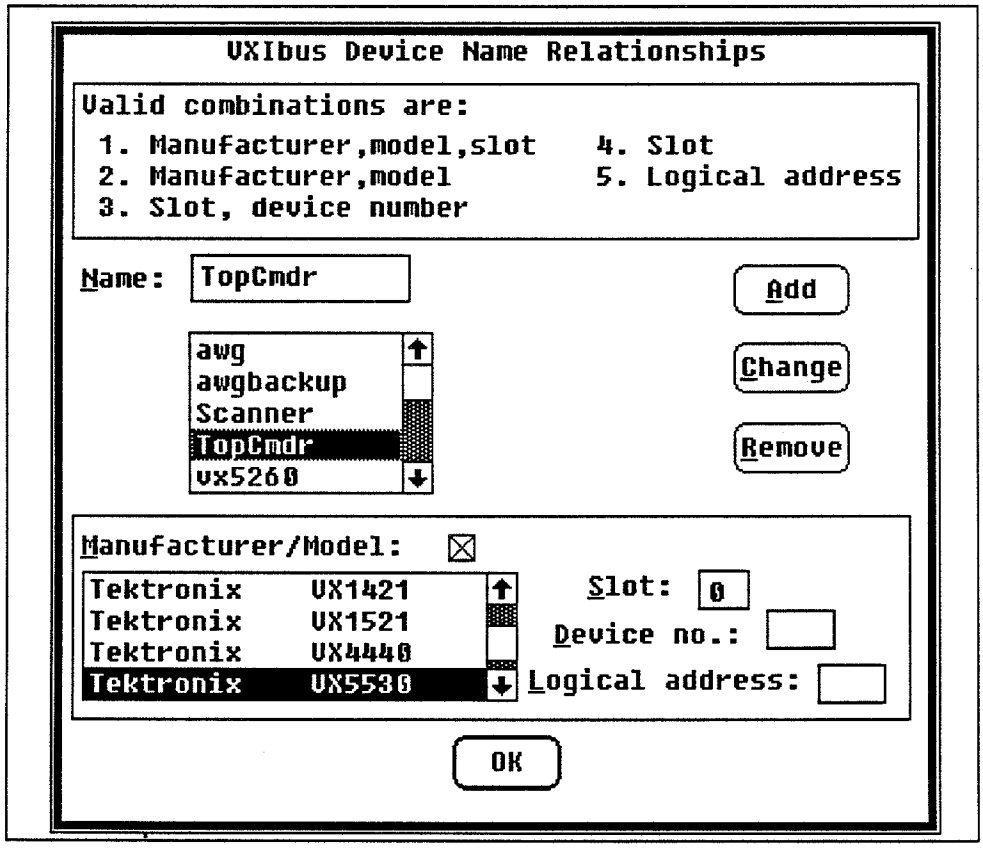


Figure 5-1 Screen appearance.

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Names are defined by typing the name in the name box and then expressing the relationship. Names can be from 1-12 characters in length. Legal characters are letters, numbers, and underscore (_). A name must begin with a letter, and must not end with an underscore.

The relationship expressed can be one of the five listed above. For instance, if you want the relationship to be manufacturer/model and slot, check the manufacturer/model box, scroll through the list and select the desired entry, and enter the slot number in the slot box. Finally, select the ADD button to complete the operation. If you enter an incomplete or invalid relationship, an error message explaining the problem appears.

To view an existing name relationship, simply select the name from the scrollable name box. To change something about the relationship (or the name itself), make the changes and select the CHANGE button. To delete the currently selected name, select the REMOVE button.

The information is maintained in a file named **\tekvics\config.hwf.** This file is updated each time the ADD, CHANGE, and REMOVE buttons are pushed. The OK button simply returns control to the main menu.

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Commander/Servant Hierarchies

This facility is used to describe the hierarchy (if any) of VXIbus devices that should be established by the Start-Up Resource Manager. The hierarchy is described by defining one or more commanders and their individual servants (which in turn may be commanders of lower-level servants).

Figure 5-2 illustrates the appearance of the screen. The bottom box is a listing of all names established by the symbolic device naming facility. The top box shows all devices (if any) that have been defined as commanders. If and when a commander is selected in the top box, the middle box lists all of the servants. In the example, there are five named devices, one of them has been defined as a commander, and the highlighted commander *TopCmdr* has two servants—*awg,* and *awgbackup*.

A device is defined as a commander by selecting (highlighting) it from the bottom box and depressing the ADD-COMMANDER pushbutton. A device is defined as a servant to a specific commander by selecting it from the bottom box, selecting a commander from the top box, and depressing ADD-SERVANT. To see a device's commander (if any), select the device from the bottom list box and depress SHOW-COMMANDER; if the device has a commander, the commander will be highlighted in the top box and all of its servants will be listed in the middle box. To remove the commander or servant status of a device, select it from the top or middle box and depress DELETE.

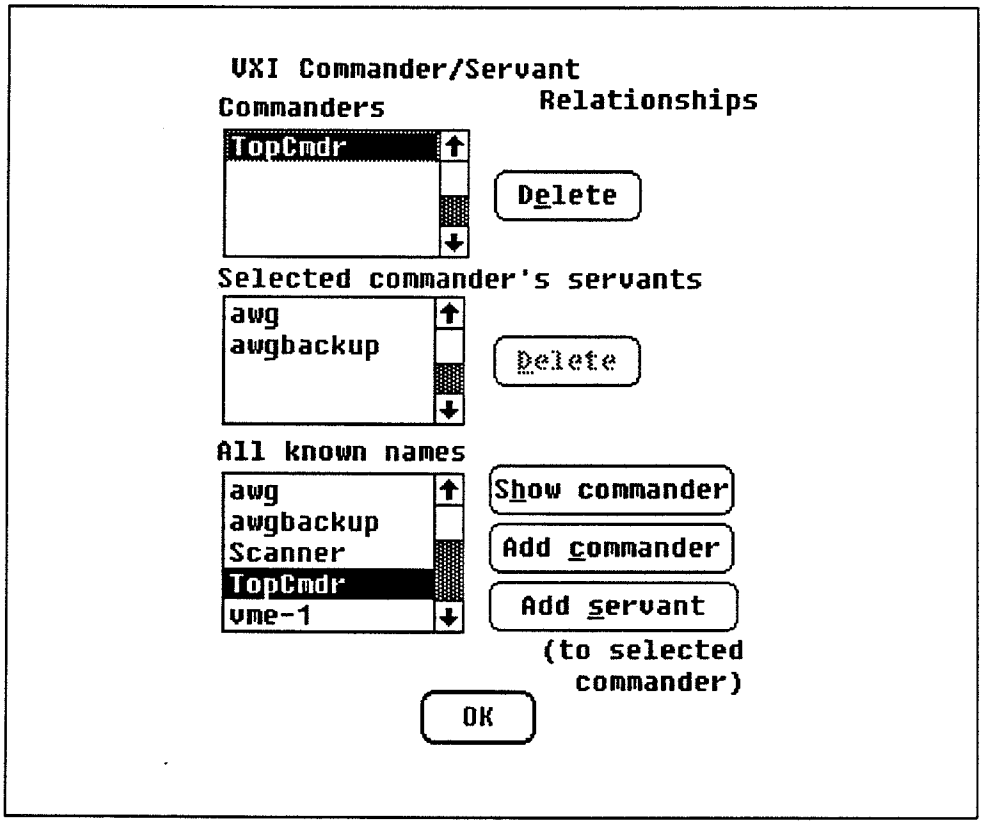


Figure 5-2 Menu for commander/servant hierarchies.

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Describing VMEbus Devices

This facility is used to describe VMEbus, or "pseudo-VXIbus," devices present in your VXIbus system. The devices are described as if they were VXIbus devices. In other words, you can view this facility as part of a software simulation of the VXIbus configuration registers of a VMEbus device.

This simplifies the integration of VMEbus devices into a VXIbus system. Representing a VMEbus device as a pseudo-VXIbus device allows the resource manager to avoid any potential conflicts when allocating system resources. It also allows for a consistent programming interface across all devices in the system.

Figure 5-3 shows that three VMEbus devices, symbolically named *globalmem, vme-1,* and *VMECPU*, have been defined. The device currently selected, globalmem, has been described as a VXIbus memory device.

The VXIbus specification defines four device classes. These are register, message, memory, and extended devices. Each device class has its own set of VXIbus registers and defined attributes. The center left box allows the user to define the pseudo device as belonging to one of three standard classes: register, memory, or message.

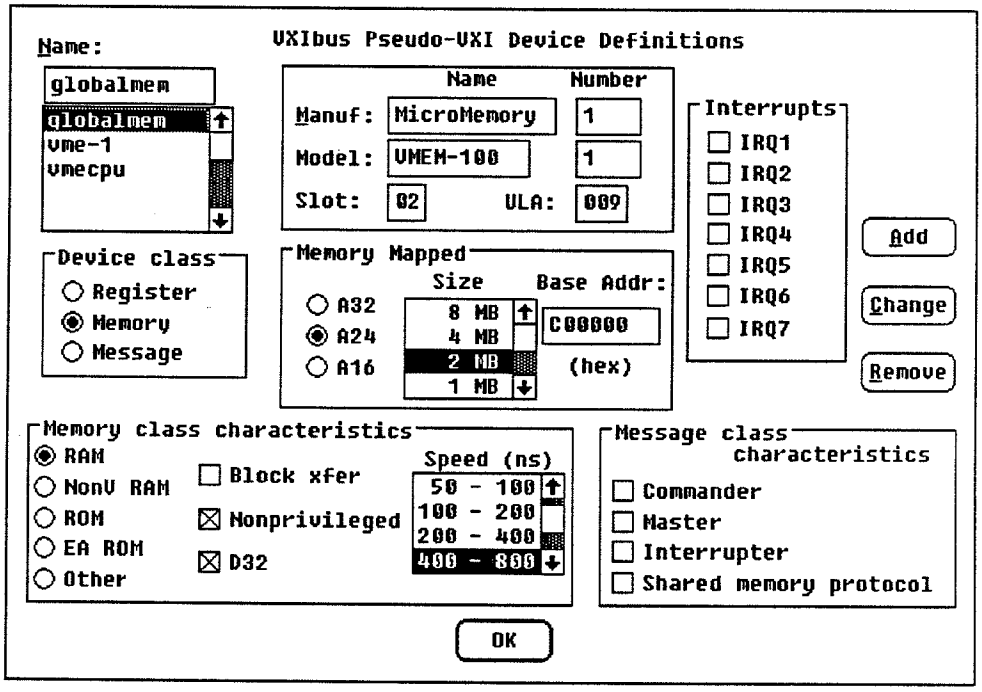


Figure 5-3 Menu for describing devices.

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The box at the middle top shows that the device has been given a symbolic manufacturer and model name. These do not have to be (and normally will not be) names of VXIbus manufacturers and models; these names, however, are used by other software components when there is a need to associate symbolic manufacturer and model names with the device. One can also give the device numeric manufacturer and model encodings, similar to the way this is done for VXIbus devices.

A VXIbus device is required to have a 12-bit manufacturer ID and a 12-bit model number which together uniquely identify the product model. These values are encoded within the configuration registers of a VXIbus device. The user may arbitrarily select those values for non-VXIbus devices. These values are only used if one asks the On Line Resource Manager for the encoded forms. Also, it is specified that the memory board resides in VXIbus slot 2, and that addressing be permitted through the On Line Resource Manager either as device having logical address 009, or as globalmem.

A logical address is an 8-bit value which uniquely identifies a device within a VXIbus system. A logical address is either statically selected by the device or dynamically allocated by the Start-Up Resource Manager at power-up. A device may have a logical address anywhere between 1 and 255. Logical address 0 is reserved for the resource manager. Assigning a logical address of 255 causes the Start-Up Resource Manager to assign the device a unique logical address (as it does for VXIbus dynamically configured devices).

VMEbus, and consequently VXIbus, specifies three different system address spaces: A16, A24, and A32. A device's memory may be mapped into one or more of these spaces. A VXIbus device must support A16 addressing and may support either A24 or A32. Its VXIbus configuration registers specify which it supports and the amount of system memory that it requires. At power-up the Startup Resource Manager assigns each device its A24 or A32 VMEbus memory by supplying the device with a starting address.

This information may be pre-selected for non-VMEbus devices using the center box. Here the device has been described as being mapped into the A24 address space, at which time the valid VXIbus memory size options for the A24 space popped into the list box, and 2 MB was selected. The base address was specified as C00000.

Since this is a memory device, it is modeled as a VXIbus memory device, meaning that it needs an attribute register specifying additional information about the device. The memory class is RAM (as opposed to nonvolatile RAM, ROM, electrically alterable ROM, or other), it does not support block transfers, it supports both privileged and nonprivileged accesses, it supports 32-bit transfers, and its access time is 400-800 ns.

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If you select the device VMECPU, the screen would change to that shown in Figure 5-4. It is represented as a VXIbus register device mapped into the A24 address space. We have also specified that VMECPU uses VMEbus interrupt line IRQ7 so that the Resource Manager knows that this line is allocated and doesn't attempt to dynamically allocate it to another device.

To define a new VMEbus device, you enter a unique name in the name box, select a device class, fill out the remaining information pertaining to that device class, and depress the ADD button. To view an existing definition, select its name from the list box in the upper left. To change its definition, change whatever is necessary and depress the CHANGE button. To remove the definition, depress REMOVE.

As with the name relationships in the previous section, the VMEbus device information is maintained in a file named **\tekvics\config.hwf.** This file is updated each time the ADD, CHANGE, and REMOVE buttons are pushed. The OK button simply returns control to the main menu.

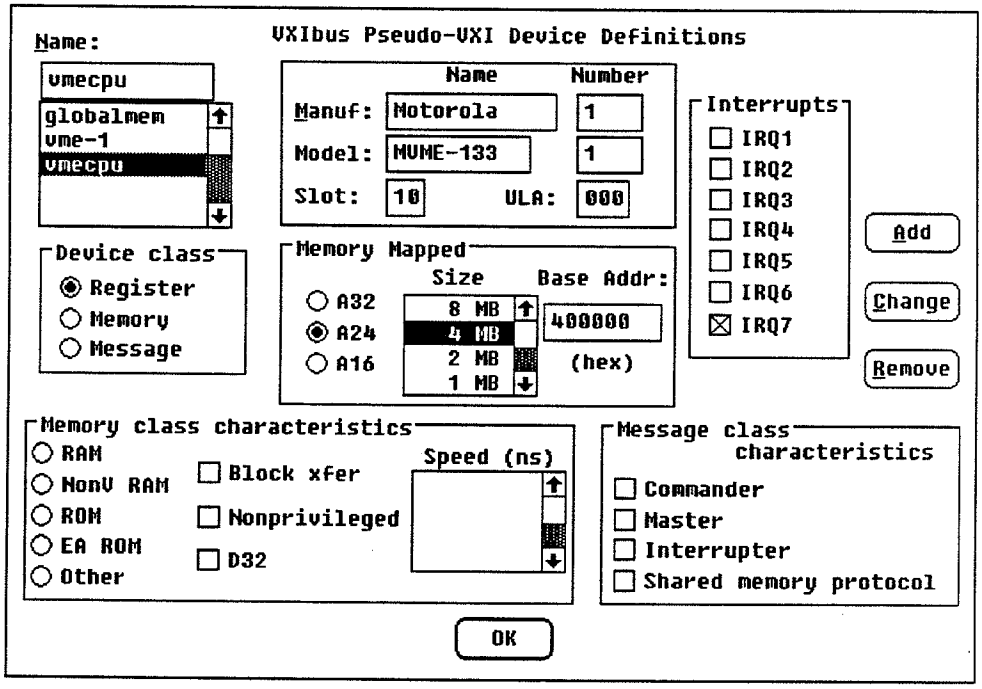


Figure 5-4 VMECPU screen appearance.

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Manufacturer/Model Database

This facility allows you to view and manipulate information about VXIbus manufacturers and model numbers/names. Selecting "Manufacturer" from the submenu produces an image like the one shown in Figure 5-5. The scrollable list box contains the names and encoded numbers of all companies holding VXIbus manufacturer numbers at the time of last distribution of the **vximanuf.txt** file. You can do the obvious, namely, add, change, and remove entries. Depressing OK at the end rewrites the **vximanuf.txt** file; depressing CANCEL leaves the file untouched.

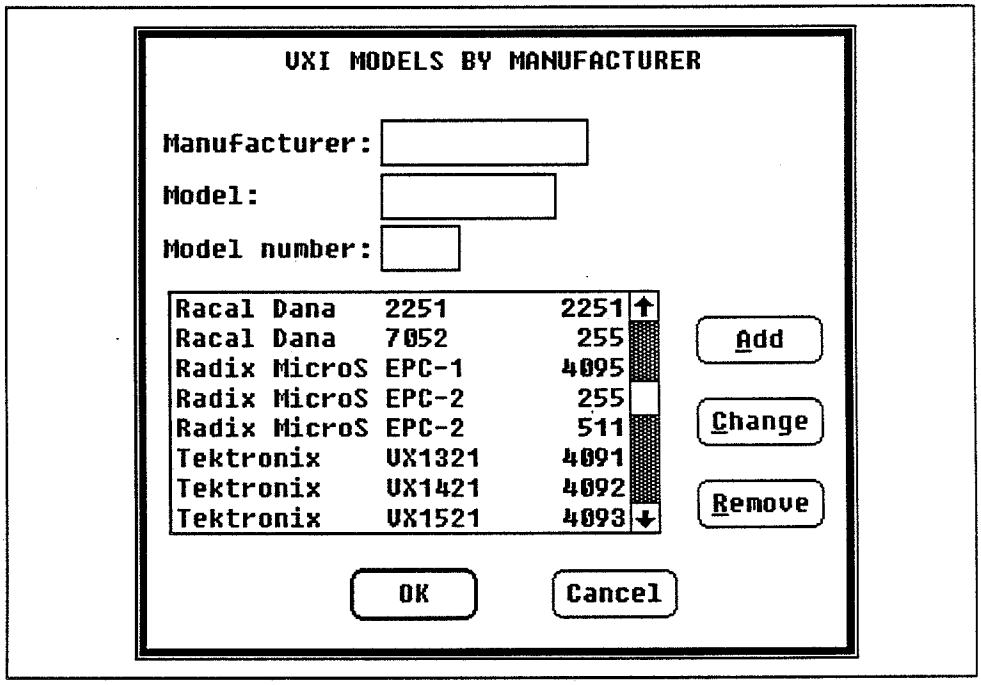


Figure 5-5 Manufacturer's models menu.

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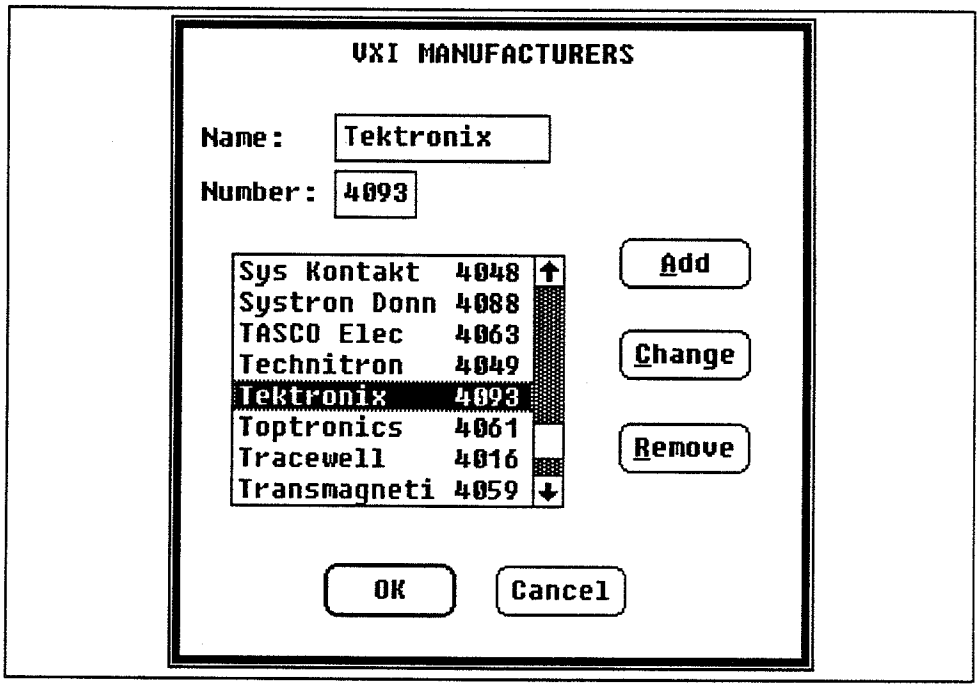


Figure 5-6 Manufacturer menu.

Selecting the Models entry from the submenu produces the display shown in Figure 5-6. Models are described with the ASCII manufacturer's name, the ASCII model name/number, and the encoded number. The latter are the responsibility of individual manufacturers and need not be unique among manufacturers. The typical usage of this facility is to update the file (**vximodel.txt**) containing this information because of the announcement of a new VXIbus device subsequent to the last distribution of the file.

When defining a new device, it is important to enter the manufacturer name in exactly the same fashion as it appears in the manufacturer list.

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GPIB Configurator

The GPIB Configurator executes under Microsoft® Windows on the VX5530 or VX5535. It allows the user to set various GPIB communication parameters for each instrument on the GPIB. See GPIB Configurator menu display Figure 5-7. These parameters are placed in a file and are accessed by the Startup Resource Manager to build an internal table for instrument communication.

Name

The Name edit box holds the device name chosen by the user. Each name throughout the system must be unique to avoid conflicts in message routing. When an instrument is added to the configuration table, the name is tested for uniqueness against the GPIB instrument list, the VXIbus instrument list, and the pseudo-VXIbus instrument list. If the name is not unique, an error is displayed and the instrument is not added to the list.

Name List

The Name List list box holds all the currently defined GPIB instruments. Although only the device name is displayed in the list box, all GPIB parameters are included in each entry. When an entry is selected, the parameters are reflected in the controls of the dialog box.

Only those instruments shown in the Name List are defined for the system. If a new instrument in entered in the dialog controls, but not added to the Name List list box, that instrument is not defined and is not included in the file. A warning is displayed if the user tries to exit when a change has been made but not saved. The warning dialog allows a second change to save the changes.

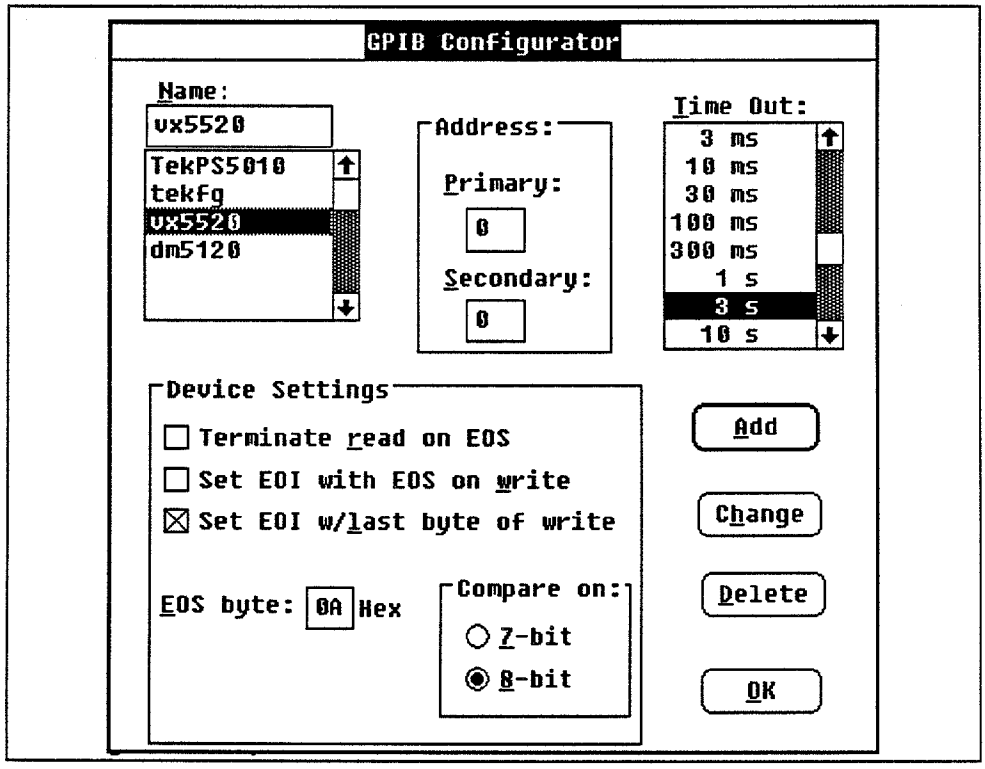


Figure 5-7. GPIB Configurator menu.

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Primary Address

This edit box holds the GPIB primary address. It must be an integer between 0 and 30, inclusive. An error is generated when an illegal value is entered. The default setting is 0.

Secondary Address

This edit box holds the GPIB secondary address. It must be an integer between 0 and 30, inclusive. An error is generated when an illegal value is entered. The default setting is 0.

Time Out

The valid time out values are listed in a list box. One value is always selected, with the default being 10 seconds.

Terminate Read on EOS

Checking this box indicates that reads from the instrument are to be terminated when the EOS (End Of String) character is encountered. (See EOS Byte below).

Set EOI with EOS on Write

Checking this box indicates that the EOI line is to be asserted when the EOS byte is send on writes to the instrument.

Set EOI w/Last Byte of Write

Checking this box indicates that the EOI line is to be asserted on the last byte of all writes to the instrument. This is the default setting.

EOS Byte

The End Of String byte is entered as a hexadecimalvalue from 00 to FF inclusive. An error is generated when illegal characters are entered. This value is used in conjunction with the EOS type settings above. The default value is 0A.

7-Bit or 8-Bit Compare

These radio button select the type of compare to be used for EOS. A 7-bit compare is a ASCII type compare that ignores the high order bit. A 8-bit compare demands all eight bits match the EOS character before the end of string is recognized.

Add

The Add push button places the instrument configured in the dialog controls into the Name List. The name of the instrument to be added must be different than any other instrument in the system. This includes GPIB, VXIbus, and Psuedo-VXIbus instruments.

Change

The Change push button modifies the currently selected instrument in the Name List to the values in the dialog controls.

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Delete

The Delete push button removes the currently selected instrument from the Name List.

OK

When OK is pushed all the non-GPIB instruments in the old configure file (**config.hwf**) are copied to a temporary file. Then the Name List is appended to the file. The old file is deleted and the temporary file is renamed to **config.hwf**.

Overall Usage

The Configurator has the same style of usage as other Windows applications. It can be used with or without a mouse. When using it without a mouse, the TAB key causes the selection to jump from one major set of controls to the next, and the cursor keys move the selection to controls within a group, and scroll.

If you have difficulty entering text within a box (i.e., the keyboard appears to be stuck), what is happening is that blank characters are permitted in the boxes, your act of depressing a key is actually inserting a character into the string in the box, and you are pushing trailing blanks over the character limit of that particular box. If this occurs, use the DEL key to remove some of the invisible blanks.

Files

The Configurator uses four files in directory **\tekvics**. Files **vximanuf.txt** and **vximodel.txt** are the database of manufacturer and model names/numbers. These files are also read by the Start-Up Resource Manager. These files use a stylized record format and thus should not be edited directly; use only the Configurator to alter these files.

The file **config.hwf** is where the Configurator stores the name relationships, and VMEbus (pseudo-VXIbus) and GPIB device definitions. This file is read by the Start-Up Resource Manager. Again, use only the Configurator to alter this file.

File **vxichelp.txt** is used by the Configurator when you ask for help information.

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Start Up Resource Manager

Your VX5530/VX5535 comes with DOS installed. The SURM is run automatically when the VX5530/VX5535 is reset since SURM is in the **autoexec.bat** file. The **autoexec.bat** file can be changed as desired to use a different SURM command-line option (as discussed under Invocation Options).

Operation

The overall operation of the SURM is summarized below.

VX5530/VX5535 Initialization. The SURM initializes the bus interface of the VX5530/VX5535 and sets the VX5530/VX5535's ULA to 0 (because it is the resource manager).

Static Device Identification. The SURM searches the devices on the VXIbus for logical-address positions for statically configured VXIbus devices (devices whose ULAs are preestablished rather than being assigned by the SURM). If a static device is found at ULA 255, dynamic configuration is bypassed and the user is given a warning message to that effect.

VMEbus Device Configuration. The next step is an examination of the Configurator's file (**config.hwf**) to determine if you've described any VMEbus devices in the system. For each device found, the information is extracted from **config.hwf** and eventually passed off to the OLRM as "pseudo-VXIbus registers" that make the VMEbus devices look like VXIbus devices to application programs.

GPIB Device Configuration. The SURM then extracts all GPIB device information from the Configurator file (**config.hwf**). This information is passed onto the message delivery system where it is used for managing all communication with GPIB devices in the system.

Dynamic ULA Configuration. Next the SURM goes through the process described in the VXIbus specification for DC devices, devices whose ULA can be dynamically assigned by the resource manager. The SURM contains complete support for multiple-device modules and address-blocked devices as described in the VXIbus specification.

Starting with slot 1, the SURM looks for address-blocked devices. If present, it tries to allocate them a block of logical addresses on the appropriate boundary (e.g., if the number of devices is 33 to 64, there are three possible blocks of ULAs that can be assigned, starting at 64, 128, and 192. Once an available ULA or block of ULAs is found, it is written to the device's ID register, and the SURM then checks to determine if the device (or devices) have been successfully relocated.

Since modules can have multiple non-address-blocked devices, and multiple sets of address-blocked devices, the SURM continues to probe the module. When it finds nothing more, it moves to the next slot.

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Slot Search. Since the search for static devices did not necessarily determine the devices' slots, the SURM next makes a pass through all slots to determine (1) for each device, the slot in which it resides and (2) the state of each slot. Each slot is determined to be in one of five states: *empty, operating, nonoperating* (no device responds, but something is pulling its MODID line down), *indeterminate* (converse of nonoperating – a device responds but the slot's MODID is not pulled down), and *VME* (containing a VMEbus device).

Address Map Configuration. The next step is assigning address ranges to devices that have some mapping into A24 and A32. Note the importance of the information from the Configurator here; it tells SURM where VMEbus devices are mapped, so that it can avoid conflicts.

With one exception (the allocation of Tektronix VX5530/VX5535 Controllers), the algorithm is the same for A24 and A32. The address space is divided into 32 blocks (512K blocks for A24, 128 MB blocks for A32). Each device's required-memory value establishes how many blocks it needs, although the smallest space the SURM allocates is one block.

Starting from the devices that require the most blocks and working down to the one-block devices (to minimize fragmentation), the SURM attempts to find the required number of blocks on the required boundary. (The SURM avoids use of the first four and last four blocks of each address space as long as possible, since the VXIbus specification doesn't require all bus masters to be able to generate these addresses.) The SURM stores the allocated boundary in the device's offset register and sets the device's A24/A32 enable bit. Detected error situations are: unable to allocate, inoperable offset register, and inoperable A24/A32 enable bit.

Two things are done prior to the algorithm above. When dealing with A32, the SURM first searches for devices with partially ROM'ed offset registers and allocates them into the eight slots whose bases are 18000000, 19000000, ..., 1F000000. These all fall into one allocatable block, and therefore reduce the number of available blocks to 31.

Second, for both A24 and A32, the information about VMEbus devices is used to preassign space occupied by these static devices. That is, the blocks into which VMEbus devices have been mapped by the Configurator are marked as unavailable. (VMEbus devices need not consume a block apiece.)

Self-Test Management. Each device's PASS bit is examined; if not set, an error message is written and the device is placed into the safe state by setting the sysfail-inhibit and reset flags in its control register. If a device has passed its selftest but is still in extended selftest, the SURM simply issues a warning message.

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Symbolic Naming. The next task is assigning symbolic names to all devices. GPIB and VMEbus devices already have symbolic names (from the Configurator information). For each VXIbus device, the SURM searches the Configurator's config.hwf file for VXIbus naming information. For each naming relationship found, the SURM determines whether it applies to something in the current VXIbus system configuration and, if it does, attaches the name to the applicable device. For more information on naming relationships, see the information on the Configurator at the beginning of this section.

If a name cannot be found, the SURM assigns default names of the form vdev0, vdev1, ...

Commander/Servant Initialization. In this initial version of the SURM, the hierarchy assumed is that all devices are servants of the top-most commander, which is the SURM's computer module. A begin normal operation message is sent to all message-based servants. An error message is recorded for any such servants who are not in the state of being able to receive a word-serial message.

Termination. SURM reads the **vximanuf.txt** and **vximodel.txt** for symbolic manufacturer and model information, and puts information about the configuration and errors in files **surm.lst** and **surm.err**. Unless the /NO command-line option was specified, the SURM invokes two internal interfaces to pass information along to other software components—the Message Delivery System (MDS) and the On Line Resource Manager (OLRM).

Depending on the command-line option selected, the SURM either immediately terminates, or displays the configuration and errors on the VX5530/VX5535 screen and waits for operator action.

Errors

The SURM performs extensive error checking during each of its operations. These errors are written to file **surm.err** and may, depending on the command-line option used, appear in a window on the VX5530/VX5535 screen.

The errors are categorized as fatal, significant, and warning. Fatal errors usually cause the resource manager to terminate prematurely. An example is the VX5530/VX5535 not residing in slot 0. Significant errors are those where one or more devices may be configured incorrectly. An example is a device whose VXIbus registers apparently cannot be written to successfully. Warning messages represent cautionary information (e.g., a device is still in its extended selftest).

Since the SURM contains online help information with explanations of each error message, the individual messages are not included in this manual.

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Invocation Options

You have a number of choices concerning when SURM should just perform its operations and terminate, and when it should display information on the screen and interact with the user. The command line options are

/DF display if a fatal error occurs

/DE display if a fatal or significant error occurs

/DW display if any error occurs (including warnings)

/DN display if SURM assigned any default symbolic names to devices

/NO do not pass system configuration information on to the OLRM and Message Delivery System.

For instance, the command line

```
\tekvics\surm /DE /DN
```

causes SURM to terminate after configuring the system and writing the **surm.lst** and **surm.err** files, unless one or more fatal or significant errors occur or SURM had to assign a default name to a device. When no /D options are present, SURM displays and awaits user action always.

Configuration Display

Prior to terminating, theSURM writes information about the configured system into file **surm.lst**, and optionally displays this information on the VX5530/VX5535's screen. The configuration information is formatted in the following sections:

1. A report of all devices. This shows, for each device, its symbolic name, whether its logical address was static, dynamic, or Configurator derived, the logical address, the manufacturer's name, the model name, and the assigned address range in A24 or A32 memory.

2. Supplemental information on memory-based devices. This shows, in symbolic form, the memory type, subtype, privilege level, speed, block-transfer, and D32 attributes.

3. Supplemental information on message-based devices. For each message-based device, checkmarks denote whether the device has the following attributes: commander, signal register, bus master, interrupter, fast-handshake mode, and shared-memory message protocol.

4. Slot report. This matrix shows which of four states (discussed earlier) each of the 13 slots is in.

5. Commander/servant hierarchy. Displays the commander/servant hierarchy.

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A sample display is shown in Figure 5-8. The first section lists all devices found and their ULA (logical address). The ULA value is prefixed with S (static), D (dynamically assigned), or V (VMEbus, preassigned by the Configurator). The devices' slots, manufacturers, and models are also shown. If a manufacturer or model is not shown, it is unknown to SURM. Finally, for devices which needed address space in the A24 and A32 address spaces, the addresses assigned by SURM are shown (in hexadecimal).

The next section shows additional attributes for VXIbus memory devices and VMEbus devices represented as VXIbus memory devices through the Configurator. The third section shows all VXIbus message-based devices and VMEbus devices represented as message devices through the Configurator. The attributes are commander, possesses signal register, is a bus master, is an interrupter, supports fast handshake mode, and supports the shared-memory message protocol.

The next section shows the state (of five possible states) of the 13 maximum possible slots. Note that an "empty" slot could truly be empty, or be an electrically inactive slot occupied by a multislot device. The final section shows the initial ownership hierarchy which, as mentioned earlier, is simply that every device is a servant to the slot-0 VX5530/VX5535.

```
                    VXI System Configuration
--All Devices--
NAME          ULA SL MANUFACTURER MODEL       A32/A24 MEMORY
TopCmdr      S000  0 Tektronix    VX5530      18000000-18FFFFFF
awg          S001 10 Tektronix    VX5790      200000-20FFFF
globalmem    V009  2 MicroMemory  VMEM-100    C00000-DFFFFF
vmecpu       V002 10 Motorola     MVME-133    400000-7FFFFF
vme-1        V003  4 Tektronix    vme-A/D     800000-9FFFFF

--Memory Devices--
NAME          TYPE  SUBTYPE      PRIV  SPEED       BLKT D32
globalmem     RAM                both  400-800ns        √

--Message Devices--
NAME          CMD'R SIGREG MASTER INT'R FASTHS SHMEM
TopCmdr         √     √       √     √              √
awg                   √             √              √

--Slot Report--
                0  1  2  3  4  5  6  7  8  9 10 11 12
EMPTY              √     √     √  √  √  √  √     √  √
OPERATING       √                                  √
NON-OPERATING
INDETERMINATE
VME (NONVXI)             √     √

--Commander/Servant Hierarchy--
TopCmdr
   ├── awg
   ├── globalmem
   ├── vmecpu
   └── vme-1

********** BOTTOM **********
```

Figure 5-8 Configuration display.

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User Interaction

When SURM displays on the VX5530/VX5535 screen, it uses multiple color windows (but is not a Windows application). You can flip from one window to another, and can scroll windows using the directions displayed on the screen. One window shows the configuration reports (i.e., the same information as in file **surm.lst**). Another shows any error messages generated. Function key F1 displays a help window, a scrollable window with detailed explanations of each error message and the information inthe configuration window. The partitioning of errors into fatal, significant, and warning is also explained in the help information.

When use of a command-line option has led to SURM's displaying of the above information, you are given the option of changing any of the device names (default or otherwise).

Other Usage Notes

SURM can be run as an application at any time. However, before doing so, you need to consider the consequences.

As distributed, **autoexec.bat** runs SURM after the Command Bridge and VXIbus Bridge. If the Command or VXIbus Bridges are not run before SURM, then SURM will report "Media not supported" errors. Running the Command Bridge and VXIbus Bridge afterwards will correct these errors.

The initial version of SURM assumes that the VX5530/VX5535 on which it is run is also the VXIbus slot-0 controller. If you have multiple VX5530/VX5535s in your system, only the one acting as the slot-0 controller should run SURM.

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If the SURM Hangs

Although the SURM does a thorough job of error checking, there are certain circumstances where the SURM "hangs", or does not complete its execution.

When this happens, it is almost always the result of the VX5530/VX5535 not being able to gain control of the data-transfer bus. Possible causes are:

1. The VX5530/VX5535 is not properly seated in the backplane.

2. The VX5530/VX5535 has not been configured as a slot-0 controller. This might have happened in two ways. First, reboot, hit CTRL-ALT-ESC, and check the BIOS setup screen. Second, check the slot-0 jumpers inside the VX5530/VX5535.

3. The system contains one or more other devices that are also configured as slot-0 controllers. Check this by removing all other devices and rebooting.

4. There is something wrong with the VXIbus backplane, typically the bus-grant or bus-request lines.

File Usage

SURM reads files **vximanuf.txt, vximodel.txt**, and **config.hwf** for information. It writes files **surm.lst** and **surm.err**. It also reads file **surmhelp.txt**, which contains the help information. All files are assumed to be in directory **\tekvics.**

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BusProbe

The BusProbe is an interactive tool for stimulating devices on the VXIbus. The BusProbe provides mechanisms for sending VXIbus commands and messages, generating read and write accesses on the bus, sending interrupts, and manipulating some of the bus interface signals. The program is a Windows application.

Bus operations are selected from pull-down menus, which in turn produce form fill-out dialog boxes prompting for the specific information needed to perform the selected operation. For each executed command, a line summarizing the operation is displayed on the main BusProbe window, followed by the data generated by the command (if any). At any point, the user can scroll back through this data to recall the results of a previous operation. A log of all the transactions performed in this session can be saved to a file for later reference.

Input and the Main Window

The BusProbe is best used in conjunction with a mouse for easy selection of menu items; however, the application can be run completely from the keyboard using the usual Windows keyboard interface to move around in and select items. See the Windows documentation for information on the keyboard-only interface.

The main window of the BusProbe application is a viewport into a complete log of this session's BusProbe operations. The viewport can be moved by using the scroll bars on the window edges, or by using the Page Up, Page Down, Home, End, or arrow keys. The scroll-bar "thumb" (that little box in the scroll bar that moves up and down) always reflects the viewport position in the context of the complete session transcript.

The information logged when executing an operation is always appended to the end of the session transcript, regardless of where the viewport is located. If the last line in the transcript is visible as the last line on the viewport, then when new data is added to the transcript the viewport scrolls to keep the end of the transcript in the viewport; however, if the last line of the transcript is not in the viewport, then the viewport is not moved when data is added to the transcript.

The size of the viewport can be changed by grabbing one of the corners or borders of the main window and adjusting it to the desired size. The initial viewport size chosen by BusProbe when it first starts is a compromise between providing a useful amount of context and minimizing the screen space commandeered by the program.

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FILE Menu

The transcript of a session can be written to a file for manipulation by other programs, documentation, etc. The FILE menu provides control over the saving and restoring of session transcripts.

NEW Command

The NEW command ends the current session transcript and begins a new transcript. Subsequent data is logged in the new transcript. The new transcript does not have a file name associated with it.

If the current transcript has had data added to it, the user is asked whether the current transcript should be saved before the new transcript is started.

OPEN Command

The OPEN command ends the current session transcript and loads in an old transcript file as the new transcript. Subsequent data is appended to the new transcript. At the user's option, the new transcript may later be saved to any file, including the old transcript file. This provides a mechanism for continuous transcripts across different sessions.

When the OPEN command is selected, a dialog box is put onto the screen for the user to fill out. The user selects which file to open by either typing the name into the OPEN FILE NAME box, or by selecting one of the files in the list box, or some combination thereof.

If the current transcript has had data added to it, the user is asked whether the current transcript should be saved before the new transcript is started.

SAVE AS Command

The SAVE AS command saves the current transcript to a file. Subsequent data is appended to the current transcript, but the file reflects only the transcript as of the point at which the transcript was saved.

When the SAVE AS command is selected, a dialog box is put onto the screen for the user to fill out. The user selects which file to save to by filling in the SAVE AS FILE NAME box. The box is initially filled with the name of the last file either opened by the OPEN command, or saved using the SAVE or SAVE AS commands.

The SAVE AS command is disabled and grayed when the transcript is empty.

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SAVE Command

The SAVE command saves the current transcript to a file. Subsequent data is appended to the current transcript, but the file reflects only the transcript as of the point at which the transcript was saved.

If a file name has been previously specified in an OPEN or SAVE AS command, that file name is used; otherwise, the user is prompted as if for a SAVE AS command.

The SAVE item is disabled and grayed when the current transcript has not changed since it was opened or started.

EXIT Command

The EXIT command ends the current session transcript and exits the application.

If the current transcript has had data added to it, the user is asked whether the current transcript should be saved before the application terminates.

VMEbus Menu

The VMEbus menu provides selections to read and write data across the bus, send interrupts, reset the system, and control how the VX5530/VX5535 arbitrates for the bus.

Data Transfer Commands

The data transfer commands READ DATA, WRITE DATA, and FIND PATTERN all share two characteristics: first, a common BUS ACCESS dialog box that appears before the dialog box for the particular command, and second the common behavior that the command's dialog box remains after the requested data transfer is performed. This second behavior anticipates that the same or related transfers are likely to be performed again, and allows for several data transfer commands to be pending, requiring only a single keystroke to invoke them.

With several of these dialog boxes simultaneously on the screen, the potential exists for the screen to become cluttered, with individual dialog boxes blocking important parts of the display. The user can solve this problem by selecting the title bar of any of the data transfer boxes and dragging them anywhere on the screen. (The boxes are not constrained to lie within the borders of the main window of BusProbe.)

The upper left corner of the title bar of these boxes is called the control bar. Selecting it produces a menu with two important options on it: CLOSE and PARAMETERS. When selected, the CLOSE option deletes the data transfer box. The PARAMETERS option pops up the BUS ACCESS dialog box again, allowing the user to change the bus access parameters associated with that data transfer box.

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BUS ACCESS Dialog

Since the three data transfer commands make data accesses across the bus, they share the BUS ACCESS dialog box to specify the VXIbus address modifier, the data transfer width, and the byte order for the transfer. See Figure 5-9.

The VXIbus address modifier is a 6-bit field which selects the address space in which the transfer takes place. (Encoded in this field are whether the address is a 32-bit address, a 24-bit address, or a 16-bit address, and whether the access is a supervisory, non-privileged, data, or program access. See the VXIbus specification for more information.) The BUS ACCESS dialog box allows the user to select one of 10 different address modifiers, and displays the hex-encoding of the selection in a box in the lower right corner of the address modifier section.

The data transfer width specifies whether the operation is performed using 8-bit accesses, 16-bit accesses, or 32-bit accesses. The beginning address for any data transfers is required to be aligned on an even address boundary for 16-bit accesses, and a 4-byte boundary for 32-bit accesses. Furthermore, the transfer beginning and ending addresses are required to select a transfer length which is an exact multiple of the data width selected.

The byte order indicates whether the data transfer is associated with a device that follows the Intel byte order convention or the Motorola byte order convention. The BusProbe uses the VX5530/VX5535 byte swapping hardware to convert the data to and from the native Intel ordering and the ordering selected here.

When the BUS ACCESS dialog box first appears, before a data transfer box has been created, it suggests as defaults the parameters of the last data transfer selected (if any). When the dialog is entered from a data transfer box's control-bar selection, the parameters of that box are displayed and set.

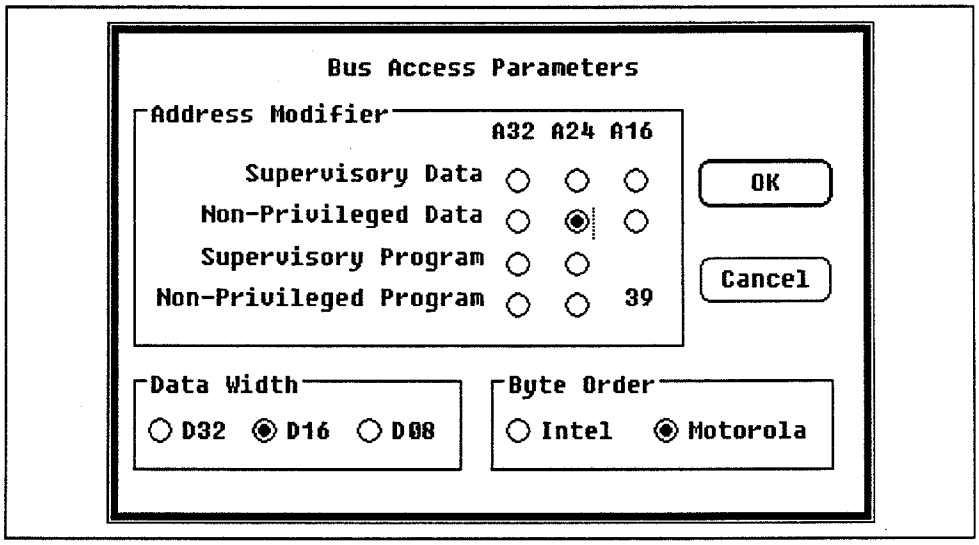


Figure 5-9 Bus access menu.

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READ DATA Command

The READ DATA command performs one or more read accesses on the bus, and places the acquired data into the transcript.

When the READ DATA command is selected and the BUS ACCESS style has been chosen, a dialog box is put onto the screen for the user to fill out. See Figure 5-10. The user selects the starting address and the byte transfer length, and then initiates the transfer by selecting the READ pushbutton. The numeric fields all assume hexadecimal input.

When a consistent starting address and byte transfer length are chosen, the ending address of the transfer is displayed to the right of the starting address. This provides the user a second check that the correct starting address and transfer length have been selected.

The acquired data is displayed in the transcript with an address field on the left, several columns of the data values represented as hexadecimal numbers, followed by the same data represented as ASCII string data. The displayed address is the requested address truncated to the nearest 16-byte aligned address (lower 4 bits are zero). This is done so that the data lines up nicely for longer transfers. The address field for a 32-bit address space access is displayed as a 8-digit value, a 24-bit address as a 6-digit value, and a 16-bit address as a 4-digit value.

The data fields in the hexadecimal and ASCII sections are written as blanks when they are not part of the transfer. The ASCII section displays non-printable characters as dots. The hex section displays 8-bit accesses as 2 digit values, 16-bit accesses as 4-digit values, and 32-bit accesses as 8-digit values. The initial viewport size chosen by the BusProbe makes the hex display entirely visible and the ASCII data entirely hidden. Resizing the window to be larger horizontally will allow the ASCII data to be visible.

If a bus error occurs (VME BERR) in the data transfer, the transfer is aborted and a message written to the transcript which reports the address where the bus error occurred. The hex field of the data item for which the bus error was generated is marked with asterisks.

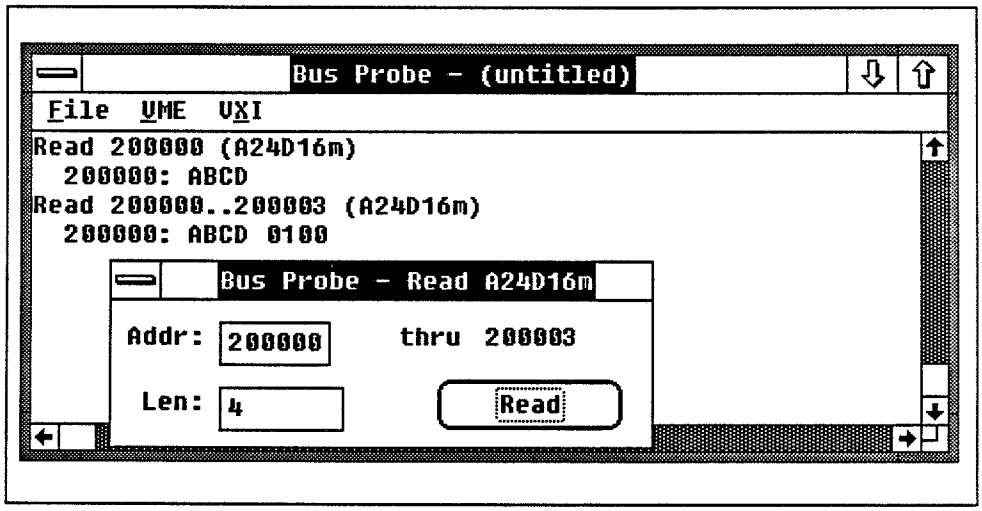


Figure 5-10 Read Data command dialog box.

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WRITE DATA Command

The WRITE DATA command performs one or more write accesses on the bus, writing the value specified by the user.

When the WRITE DATA command is selected and the BUS ACCESS style has been chosen, a dialog box is put onto the screen for the user to fill out. See Figure 5-11. The user selects the starting address, byte transfer length, the data value to write, and then initiates the transfer by selecting the WRITE button. The three numeric fields all assume hexadecimal input.

When a consistent starting address and byte transfer length are chosen, the ending address of the transfer is displayed to the right of the starting address. This provides the user a second check that the correct starting address and transfer length have been selected.

The data value found in the DATA field is left padded with zeroes as necessary to fill it out to the data width of the bus access. Just the one value is written repeatedly, so the write is effectively a fill operation and not a generalized data copy.

If a bus error occurs (VME BERR) in the data transfer, the transfer is aborted and a message written to the transcript which reports the address where the bus error occurred.

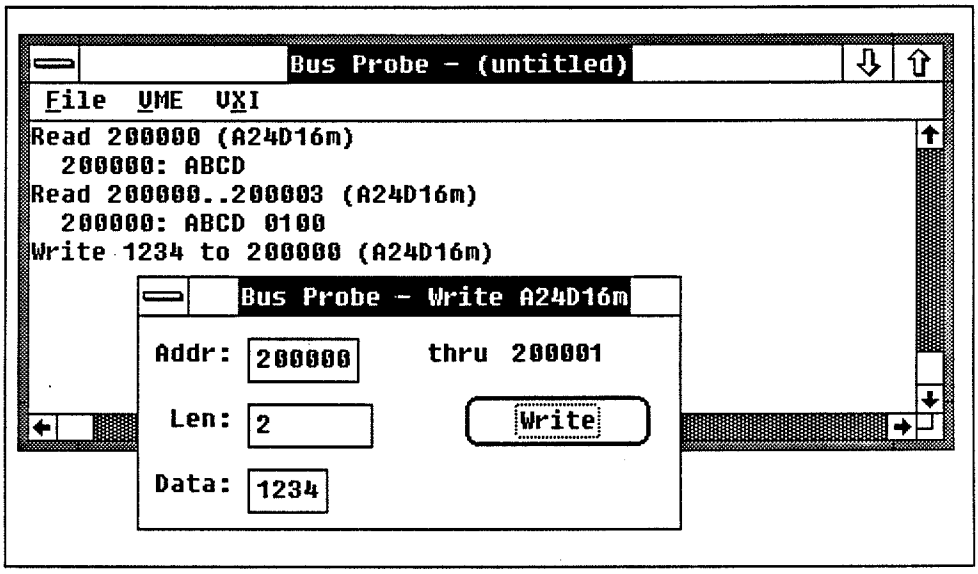


Figure 5-11 Write Data command dialog box.

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EDIT DATA Command

The EDIT DATA command performs read and write accesses on the bus, allowing the user to selectively modify the data values of successive addresses on the bus. This command is useful for modifying several adjacent memory locations.

When the EDIT DATA command is selected and the BUS ACCESS style has been chosen, a dialog box is put onto the screen for the user to fill out. See Figure 5-12. The user selects the starting address and then tabs to the next field. When the cursor is moved out of the address field, a read access is made to the selected address, and the data field is filled in with the value read. The user has the option of modifying the data field, or leaving the field with the same value. The user then selects either the WRITE pushbutton or the NEXT pushbutton. The numeric fields all assume hexadecimal input.

If the WRITE pushbutton is selected, the value in the DATA field is written out to the address in the ADDRESS field. If the NEXT pushbutton is selected, no write access is made. After either pushbutton is selected, the ADDRESS field is incremented to the next item, a read access is made to that new address, and the data value read is recorded in the DATA field. The ENTER key is a shorthand for the WRITE pushbutton, and the ESC key is a shorthand for the NEXT pushbutton.

If a bus error occurs (VME BERR) in the data read, the DATA field is left blank. If a bus error occurs (VME BERR) in the data write, the transfer is aborted and a message written to the transcript which reports the address where the bus error occurred.

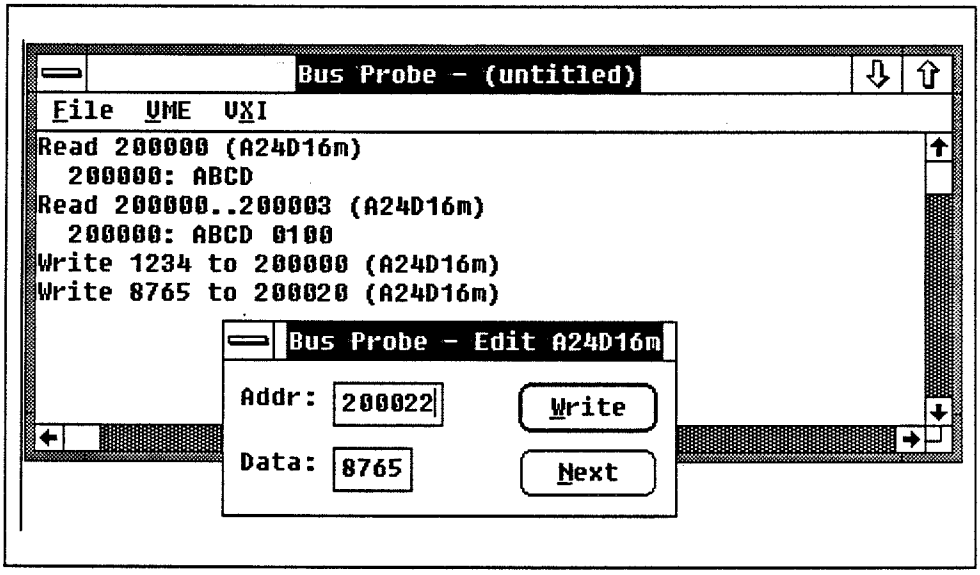


Figure 5-12 Edit Data command dialog box.

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FIND PATTERN Command

The FIND PATTERN command performs one or more read accesses on the bus, logically ANDs the acquired data with a user-supplied mask, and if that matches the user-supplied expected data value, places the acquired data into the transcript.

When the FIND PATTERN command is selected and the BUS ACCESS style has been chosen, a dialog box is put onto the screen for the user to fill out. See Figure 5-13. The user selects the starting address the byte transfer length, a data mask and match values, a step, and then initiates the transfer by selecting the FIND pushbutton. All the numeric fields assume hexadecimal input.

When a consistent starting address and byte transfer length are chosen, the ending address of the transfer is displayed to the right of the starting address. This provides the user a second check that the correct starting address and transfer length have been selected.

While scanning, a "percent done" number is displayed to indicate progress. When a match occurs, the acquired data is displayed in the transcript in the same format used for the READ DATA displayed. If multiple matches occur in the same 16-byte address range, those matches are displayed on the same line in the transcript. Items which are not read or do not match are displayed as blank. If no match occurs in a 16-byte address range, nothing is recorded in the transcript for that address range.

In the event of a bus error or no match occurs, no messages are added to the transcript, and the operation continues.

The STEP field is used to specify how much to increment the address between successive read operations. This allows the user to more quickly scan large address ranges for matches. For instance, to look on every 64K boundary for any board that responds over the range of addresses selected, such as the entire 32-bit address space, select a mask value of 0, an expected data value of 0, and a step of 10000.

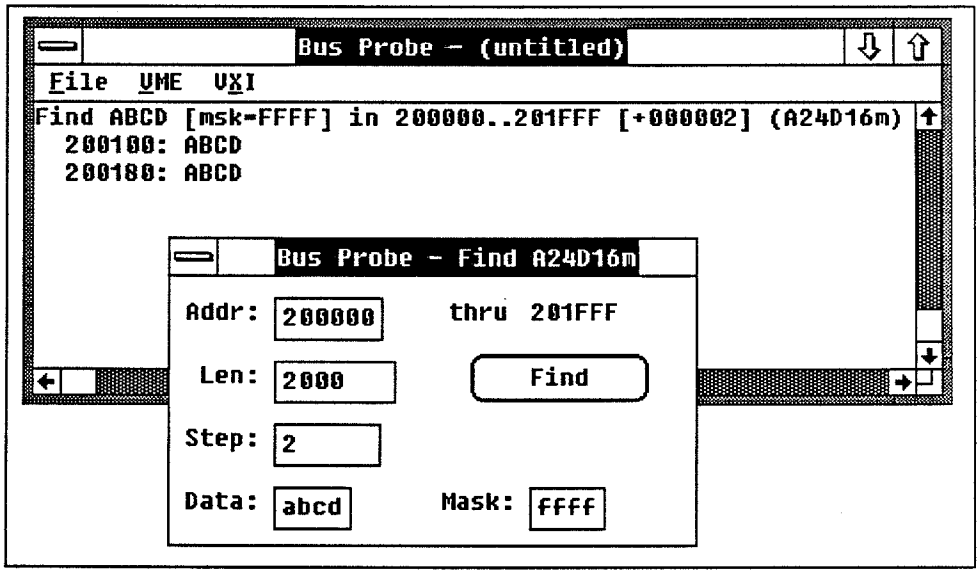


Figure 5-13 Find Pattern command dialog box.

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SEND INTERRUPT Command

The SEND INTERRUPT command signals a VMEbus interrupt.

When the SEND INTERRUPT command is selected, a dialog box is put onto the screen, prompting the user to select one of the seven VMEbus interrupts to assert, or to clear any interrupt that the VX5530/VX5535 may be asserting. See Figure 5-14. The default selection is to clear any interrupt currently asserted by the VX5530/VX5535.

If the user attempts to signal one of the VMEbus interrupts and another VMEbus interrupt is being asserted by the VX5530/VX5535, BusProbe alerts the user and asks whether to ABORT the SEND INTERRUPT operation, RETRY in case the interrupt has been acknowledged or removed, or IGNORE the error and force the VX5530/VX5535 to signal the selected interrupt.

RESET SYSTEM Command

The RESET SYSTEM command allows the user to assert or not assert the VXIbus SYSRESET signal. It also allows the user to control whether the VX5530/ VX5535 ignores the VXIbus SYSRESET signal, or responds by going through a power-on reset sequence.

When the RESET SYSTEM command is selected, a dialog box appears on the screen with two check boxes. The first box is checked if the VX5530/VX5535 is currently asserting SYSRESET. The second box checked if any board asserting SYSRESET will reset the VX5530. The user toggles the check boxes to the desired state, and commits to the action by pushing the OK button.

If both boxes are checked, then BusProbe gives the user the opportunity to save the current transcript before the inevitable reset. The user is *not* prompted to save the transcript when the VX5530/VX5535 is not asserting SYSRESET but the VX5530/VX5535 is being made sensitive to SYSRESET, which implies that there is a possibility that the current transcript will be lost.

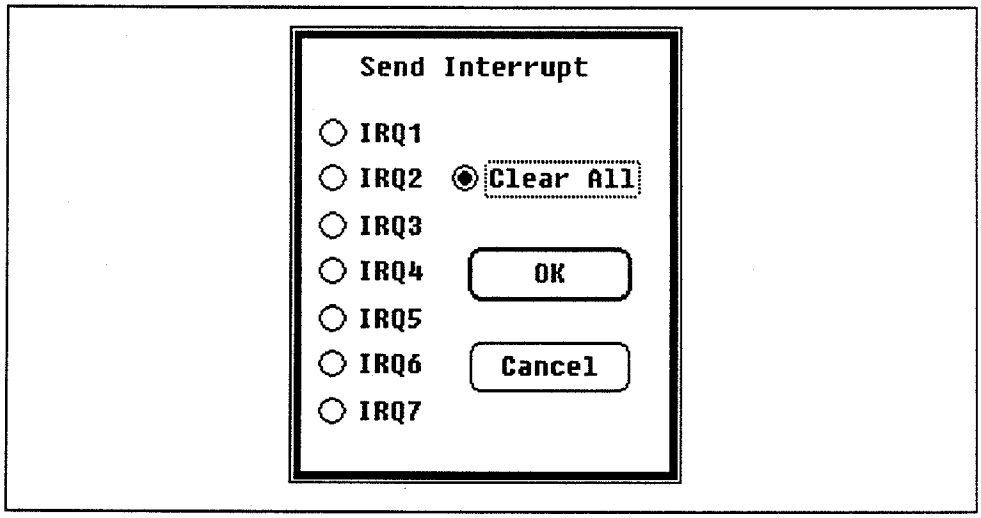


Figure 5-14 Send Interrupt command dialog box.

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VXIbus Menu

SEND/RECEIVE MESSAGE Command

This command allows the user to send and receive messages to/from a servant device as well as to/from Advanced Trigger Functions (ATF). When the user selects this menu item, a dialog box appears prompting for message parameters. See Figure 5-15. There are three types of selections that can be made:

1) Device name is chosen by selecting its name from a list box listing all of the message-based devices on the system. Exactly one device must be selected. After selecting a device, the OK button lights up. The parameters below can be selected, or the user may proceed by clicking on OK.

2) Message terminator. This selects a string to be appended to the message before sending it. There are three radio buttons for choosing between linefeed (newline) termination, carriage return/linefeed, or no termination. The default is linefeed, which is the IEEE 488.2 standard. If NONE is chosen, then nothing is added to the message.

3) Message list order. As seen in the next window, there is a list box containing past messages which is displayed while the user is sending messages. The user can choose whether the entries are ordered in alphabetical or most recently used order.

After clicking the OK button on the Message Parameters dialog box, that box disappears and is replaced by the dialog box for composing and sending the messages. See Figure 5-16. At any time the user may return to the Message Parameter dialog box by choosing the PARAMETERS entry from the command bar menu.

There are two ways of composing a message:

- Click on a previous message in the Previous Message box.
- Type a message in the Message box.

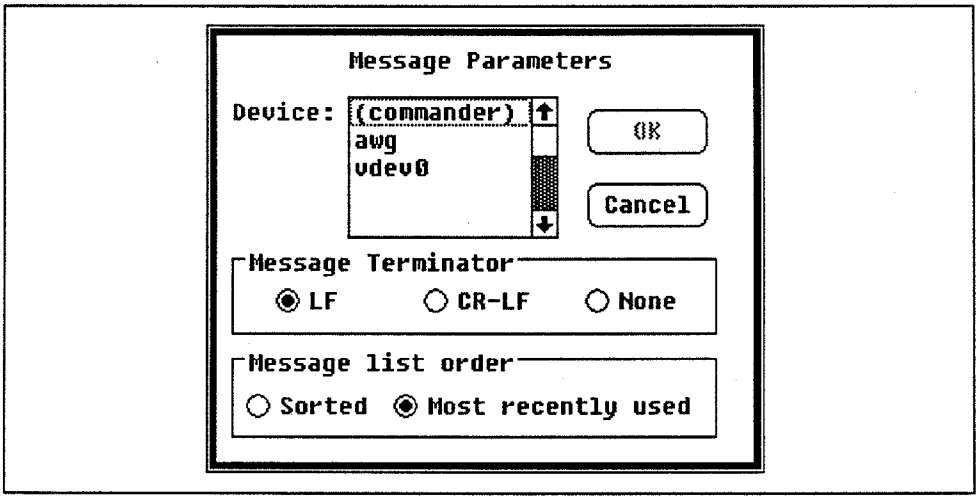


Figure 5-15 Message Parameters dialog box.

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Either way, the user can then edit the message in the Message box. Long messages will horizontally scroll in the Message edit box.

To receive a result when sending a message, check the AUTO-RECEIVE check box. If a message from the previous menu list is chosen, BusProbe remembers whether a receive was done the last time this message was sent and sets the AUTO-RECEIVE check box appropriately.

Push the SEND button to send the message. The message and its result (if any) are put into the transcript.

The user can push the RECEIVE button to just receive a result; however, most devices generate a result only after they receive a message, so there is a chance it will time out.

A shortcut to sending a message is to double-click on an entry in the Previous Message box. This sends that message and does an auto-receive, if appropriate.

When a message that isn't already on the list of previous messages is sent, that message is added to the list of previous messages. If the message was sent with auto-receive, then that entry is marked with "*". The same message with and without auto-receive marked are recognized as being different and so each of them shows up separately in the Previous Message box.

The servant's VXIbus word serial status information is displayed before and after sending the message. This is in the section on the center left of the message dialog box. A grayed field means that the condition is false, and a normal (lit) text field indicates that the condition is true. The fields are

DIR Data Input Ready. If lit, the servant will accept *byte available* commands (i.e., the servant is ready to input data).

DOR Data Output Ready. If lit, the servant will accept *byte request* commands (i.e., the servant is ready to output data).

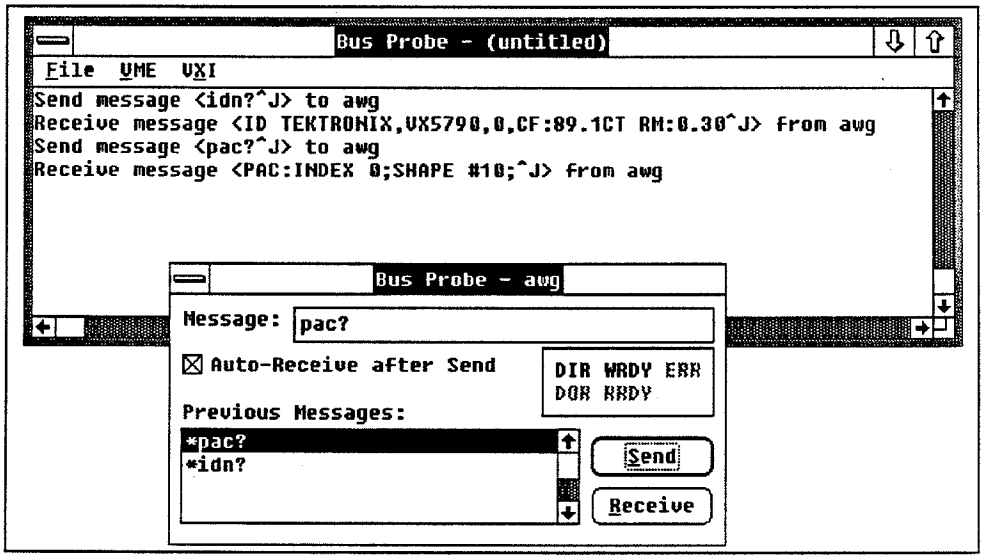


Figure 5-16 Send/Receive dialog box.

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ERR If lit, the servant is asserting an error condition to its commander.

WRDY Write Ready. If lit, the servant is ready to accept an incoming VXIbus command. Note that *byte request* and *byte available* commands must be additionally enabled by DOR and DIR, respectively.

RRDY Read Ready. If lit, the servant's data registers contain outgoing VXIbus response.

Advanced Trigger Functions commands can be sent through the "commander" device. "commander" is a virtual device which handles device configuration information and Advanced Trigger Functions. See the heading **Advanced Trigger Function Commands** later in this section for more information.

WORD SERIAL Command

This command sends low-level, 16-bit VXIbus word serial commands to a servant and optionally reading back a reply. The user chooses a destination device in the DEVICE box. Clicking on a device name selects just that device.

There are two ways to select a command.

- Select a command from the NAME box at the bottom of the dialog box (Figure 5-17). This causes the appropriate hex value to be put into the COMMAND box. Note that some commands (e.g., Byte Available) have fields that must be filled in with data. These fields show up as "XX" and must be edited before the command can be sent.

  The NAME box contains all of the standard commands defined by the VXIbus specification. Refer to the VXIbus specification for a detailed description of the commands.

- Type a hex value into the COMMAND box. As the user types, the list of known commands is searched for a match. If one is found, the name of the command is displayed above the NAME box.

Commands may have responses. These are 16-bit values that the servant generates in response to some commands. If the READ REPLY box is checked BusProbe automatically fetches the reply. The READ REPLY box is automatically

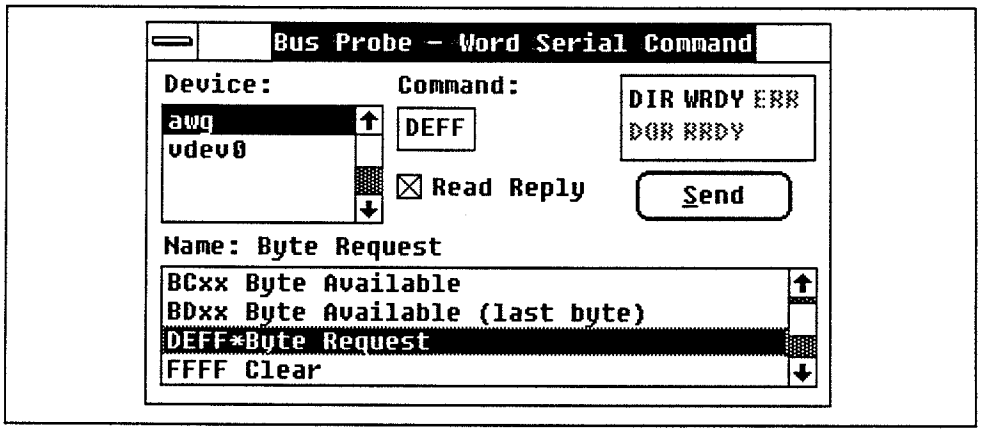


Figure 5-17 Word Serial command dialog box.

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set correctly when choosing a command from the NAME box — commands which return a response are marked by an "*".

When a device is selected and there is a valid hex number in the COMMAND box, the SEND button is enabled. Pushing SEND sends the command to all selected devices and optionally fetches the reply. The commands and replies are entered into the log.

A shortcut to sending a command is to double-click a command in the NAME box. This is the same as selecting from the NAME box and then clicking SEND.

As with the SEND/RECEIVE MESSAGE dialog box, the WORD SERIAL COMMAND dialog box has a display of the servant's VXIbus word serial status. This is described under the SEND/RECEIVE MESSAGE menu selection, above.

The initial set of commands is read from file **\tekvics\busprobe\initial.wsc**when BusProbe starts. BusProbe never updates this file.

LONG WS Command

This dialog box (see Figure 5-18) works the same as WORD SERIAL command, except that it deals with 32-bit word serial commands rather than 16-bit commands. The initial set of commands is read from file **\tekvics\busprobe\initial.lws**when BusProbe starts. BusProbe never updates this file. As delivered, this file is empty because currently there are no longword serial commands defined.

EXTENDED WS Command

This dialog box (see Figure 5-19) works in a similar fashion to WORD SERIAL command with two differences:

- It deals with 48-bit word serial commands rather than 16-bit commands, and
- Since EXTENDED LONGWORD SERIAL is a write-only protocol, it does not read back a reply.

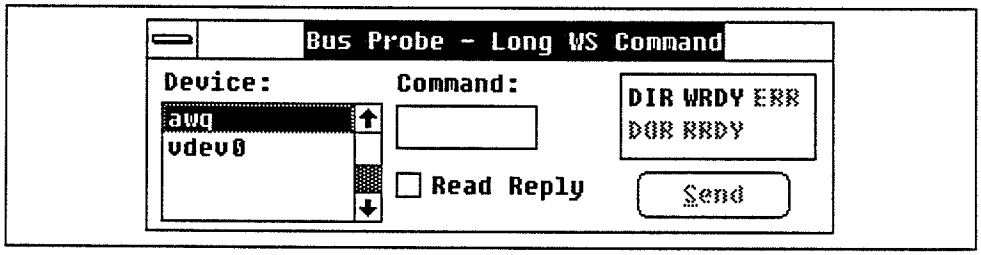


Figure 5-18 Long Word Serial command dialog box.

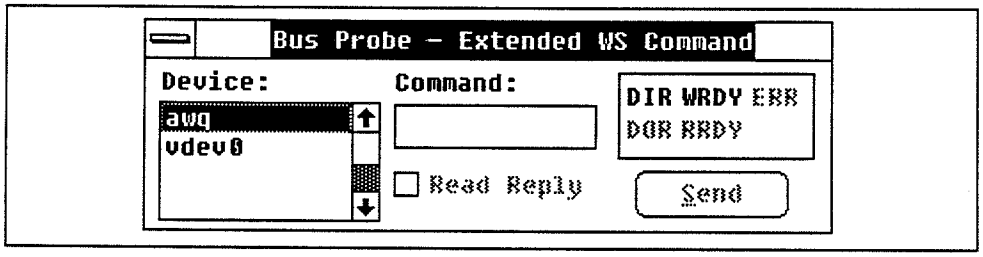


Figure 5-19 Extended Word Serial command dialog box.

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The initial set of commands is read from file**\tekvics\busprobe\initial.xws** when BusProbe starts. BusProbe never updates this file. As delivered, this file is empty because currently there are no extended longword serial commands defined.

TRIGGER Command

The TRIGGER command allows the VXIbus TTL and ECL triggers to be monitored, set, and cleared. Upon selecting the Trigger command from the menu, a SELECT TRIGGER dialog box appears prompting the user to select a particular trigger line. See Figure 5-20. Pushing the CANCEL button will cancel the trigger command.

Pushing the OK button causes the SELECT TRIGGER dialog box to disappear and a small TRIGGER box to appear. This dialog box has the trigger name in the title bar. In the middle of the box is the word LOW or HIGH, indicating the current state of the trigger line. The dialog box has two controls on the trigger.

L On the left side of the dialog box is a button marked "L". Pushing this button will generate a *falling edge* on the trigger line. This falling edge is generated by first setting the trigger line high (i.e., deasserting it) and then asserting the line low. The line is left in the low state.

So, if the line was previously low, then the line will be set high then low. If the line was previously in the high state, it will transition from high to low and stay there.

H On the right side of the dialog box is a button marked "H". Pushing this button will generate a *rising edge* on the trigger line. This rising edge is generated by first asserting the trigger line low and then deasserting the line, allowing it to go high. The line is left in the high (deasserted) state.

So, if the line was previously high, then the line will be set low then high. If the line was previously in the low state, it will transition from low to high and stay there.

For example, if a device triggers on the rising edge of a trigger, repeatedly pushing the "H" button will repeatedly trigger the device.

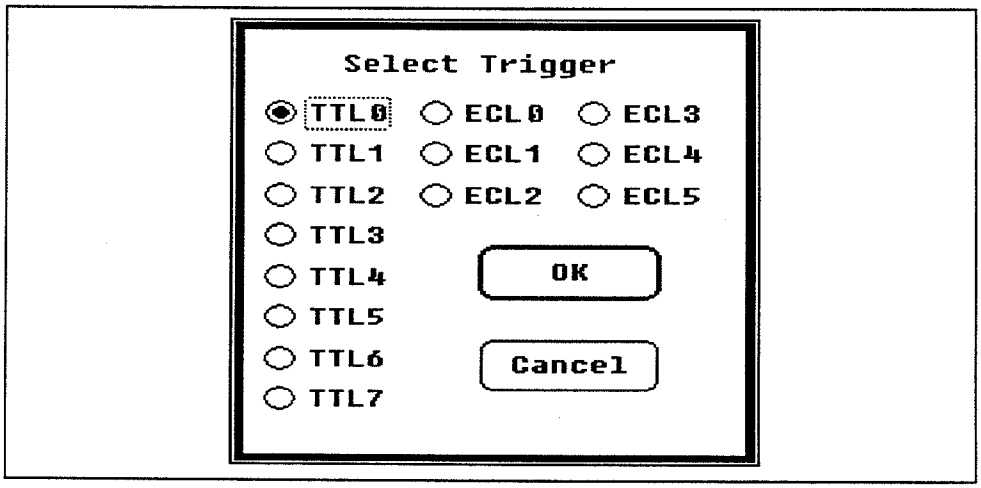


Figure 5-20 Trigger command dialog box.

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NOTE

VXIbus trigger lines are shared between Bus Probe and the ATF. Care must be taken when using the ATF. Refer to Appendix A for more detail.

INITIALIZE DEVICE Command

This command provides a means for selectively disabling or resetting individual devices. See Figure 5-21. After choosing a device from the Device box, the user may force the device into one of three states:

SOFT RESET — This selection is for resetting a device in the hope of making it operational again. It clears the SYSFAIL INHIBIT bit and asserts the RESET bit in the device's control register, which causes the device to reset and go through self test. From this state the device should transition to either the PASSED, EXTENDED SELF-TEST, or FAILED states. If the device fails self test, the SYSFAIL signal is asserted on the backplane.

DIAGNOSTIC — This selection is for diagnosing a failed device. It sets the SYSFAIL INHIBIT bit and asserts the RESET bit in the device's control register, which causes the device to transition through the SAFE state and to the DIAGNOSTIC state. The device may not become operational.

SAFE — This selection is for shutting off a device. It sets the SYSFAIL INHIBIT and RESET bits in the device's control register. Unlike the SOFT RESET and DIAGNOSTIC operations, the device is left in the SAFE state and will not become operational.

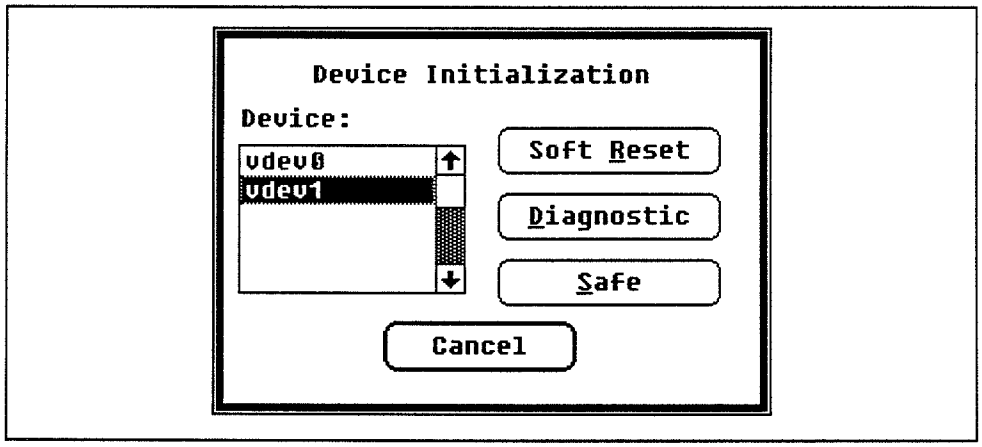


Figure 5-21 Initialize Device command dialog box.

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Message Management

The TekVICS programming environment provides programmers access to the TekVICS Message Manager and On Line Resource Manager.

The TekVICS Message Manager is a software package which coordinates all communication to instruments in the system. Currently, this includes both VXIbus and GPIB instruments. There are five parts to the Message Manager:

1) **Programming Interface Libraries.** The programming interface libraries are for the C and BASIC programming languages. In the C version, there are five different libraries. These are libraries for the small, medium, compact and large memory models for Microsoft® C, as well as a medium memory model library for Microsoft® Windows applications. In the BASIC version, there are two libraries, one for Microsoft® BASIC and one for QuickBASIC.

   The programming interface libraries provide access to the Message Delivery System and the BusManager.

2) **Message Delivery System (MDS).** This is the transport mechanism for application programs to communicate with intelligent instruments. Most programmers use the MDS facilities only.

3) **BusManager** . This is a lower-level facility for communicating over the VXIbus. It manages a bus window by which programs can directly read and write locations on the VXIbus. It also manages VXIbus interrupts and signals. Programmers should use the BusManager only for communicating with VXIbus register-based devices or VMEbus devices.

4) **GPIB Device Driver.** The GPIB device driver is a low-level driver controlling the GPIB hardware on the VX5530/VX5535. Programmers should never have to directly access this driver.

5) **Communication Bridges.** Bridges interface the Message Delivery System to the various interface busses and communication protocols supported by the VX5530/VX5535. There are three bridges. These are the *VXIbus Bridge* for communicating with VXIbus message-based devices using Word Serial or Shared Memory protocol, the *GPIB Bridge* for communicating with GPIB devices, and the *Command Bridge*. The *Command Bridge* represents local capabilities of the VX5530/VX5535 and does not communicate with any physical instruments. All bridges are implemented as terminate and stay resident (TSR) programs.

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Advanced Trigger Functions Commands

The following listing gives the ATF commands which control the majority of the Advanced Trigger Functions. These ASCII commands are used in the same manner as instrument control commands. They may be accessed through TekTMS, BusProbe or the programming interface.

Additional ATF features can be accessed only through the programming interface. For details, see the *VX5530/VX5535 C Programmers Manual* or the *VX5530/VX5535 BASIC Programmers Manual*.

ATF Error Codes and Descriptions

-100 Parameter error. One or more parameters of the command are invalid.

-200 Hardware not available error. The hardware required to perform the command is not available. This may be caused by trying to access STARbus Routing Units not available when using Option 01 hardware. Or the **atf.sys** device driver may have been installed incorrectly by using the wrong parameter in **config.sys.** See *Advanced Trigger Functions Driver Installation* in Section 2 for more detail.

-201 Routing resource not available error. The source or destination of the route has been used. All resources are available after installing the Command Bridge. If one or more previous routes have used the resource, this error occurs. The route that used the resource must be disabled in order to free the resource.

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Alphabetical ATF Command Listing

The following is an alphabetical listing of the ATF commands and a brief description of each. More detailed descriptions follow, in alphabetical order, in the remainder of this section.

ATFRSC?	Reports the current usage of all STAR lines (resources).
BNCAIN	Routes a signal from Input BNC A to other functional units.
BNCAOUT	Routes a signal to Output BNC A.
BNCBIN	Routes a signal from Input BNC B to other functional units.
BNCBOUT	Routes a signal to Output BNC B.
CMDIN	Sets up protocol unit for command trigger.
CMDTRG	Sends a trigger command to protocol unit.
POWER?	Reads the current voltage for each of the power supplies.
STAROUTEA	Routes a signal from any VXIbus STAR line to one or more STAR lines.
STAROUTEB	Routes a signal from any VXIbus STAR line to one or more STAR lines.
TEMP?	Reads the current board temperature in the VX5530/VX5535.

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ATFRSC? ATFRSC?

Purpose: Reports the current usage of all STAR lines (resources).

Syntax: `ATFRSC? {SRC|DEST}`

Parameters: `{SRC|DEST}`

Selects either the source or the destination as the resource to be reported.

Result: A string of 24 characters consisting of ASCII 0's and ASCII 1's.

The first character in the 24-character string indicates the status of STARX1, the second character indicates the status of STARX2, etc. The thirteenth character indicates the status of STARY1, the fourteenth character indicates the status of STARY2, etc., to the end of the string.

If a character is an ASCII 0, the resource is not in use. If the character is a 1, the resource is in use.

Description: This command reports the current usage of all STAR lines.

Examples:

```
ATFRSC? SRC
100000001000001000100100
```

In this example, the string response to the ATFRSC? SRC query indicates that the STARX1, STARX9, STARY3, STARY7 and STARY10 lines are used as routing sources.

```
ATFRSC? DEST
010001000101110101000110
```

In this example, the string response to the ATFRSC? DEST query indicates that the STARX2, STARX6, STARX10, STARX12, STARY1, STARY2, STARY4, STARY6, STARY10, and STARY11 lines are used as routing destinations.

Related Commands: None.

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BNCAIN BNCAIN

Purpose: Routes a signal from Input BNC A to other functional units.

Syntax:

```
BNCAIN <destination>

<destination> ::= CLK|
                  {STARXx|STARYx}[,{STARXx|STARYx}[,...]]|
                  CLK,{STARXx|STARYx}[,{STARXx|STARYx}[,...]]|
                  NONE
        where x ::= 1-12
```

Parameters: <destination>

The signal destination can be CLK10, and/or one or more STAR lines. If NONE is selected, the Input BNC A will be disabled.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available
-201	Routing resource not available

Description: The BNCAIN command routes a signal from Input BNC A to the CLK10 and/or one or multiple STAR lines.

Only STARX2...5 and STARY2...5 are available for Option 01 hardware.

The Input BNC A signal can be disabled by selecting NONE as the destination.

Example:

```
BNCAIN CLK,STARX3
```

In this example, a signal from Input BNC A is routed to both CLK10 and STARX3.

```
BNCAIN STARX5,STARX8,STARY5
```

In this example, the signal from Input BNC A is routed to STARX5, STARX8 and STARY5.

```
BNCAIN NONE
```

In this example, Input BNC A is disabled.

Related Commands: None.

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BNCAOUT

BNCAOUT

Purpose: Routes a signal to Output BNC A.

Syntax:

```
BNCAOUT <source>

<source> ::= {CLK|STARXx|STARYx|NONE}
        where x ::= 1-12
```

Parameters: `<source>`

The signal source can be CLK10, or one of the STAR lines.

If NONE is selected, Output BNC A is disabled.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available
-201	Routing resource not available

Description: The BNCAOUT command routes a signal from either CLK10 or one of the STAR lines to Output BNC A.

Only STARX2...5 and STARY2...5 are available for Option 01 hardware.

Example:

```
BNCAOUT STARX2
```

In this example, the signal from STARX2 is routed to Output BNC A.

Related Commands: None.

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BNCBIN

BNCBIN

Purpose: Routes a signal from Input BNC B to other functional units.

Syntax:

```
BNCBIN {<start stop>|<extended start stop>|<sync100>|
        <and function>|<or function>|NONE}

<start stop>::= <STST,TTLTRGx>
        where x ::= 0-7
<extended start stop>::= <ESTST,ECLTRGx,TTLTRGy>
        where x ::= 0-5
        where y ::= 0-7
<sync100>::= <SYNC100,ECLTRGx>
        where x ::= 0-5
<and function> ::= <AND,<star source>,<star destination>
                    {,<star destination>[,...]]>
        <star source> ::= {STARXx|STARYx}
        <star destination> ::= {STARXx|STARYx}
                where x ::= 1-12
<or function> ::= <OR,<star source>,<star destination>
                   {,<star destination>[,...]]>
        <star source> ::= {STARXx|STARYx}
        <star destination> ::= {STARXx|STARYx}
                where x ::= 1-12
```

Parameters:

`<start stop>`

Uses the Input BNC B signal as trigger signal to Protocol Unit 1, which is set up for Start Stop protocol. One of the TTL trigger lines is selected to transmit START/STOP values.

`<extended start stop>`

Uses the Input BNC B signal as trigger signal to Protocol Unit 1, which is set up for Extended Start Stop protocol. One of the TTL trigger lines is selected to transmit START/STOP values and one of the ECL trigger lines is selected as qualifier.

`<sync100>`

Uses the Input BNC B signal as trigger signal to Protocol Unit 1, which is set up for SYNC100 protocol. One of the ECL trigger lines is selected as qualifier.

`<and function>`

Performs logical AND with the Input BNC B signal and one of the STAR lines' signal, then routes the resulting signal to one or multiple STAR lines. The `<star source>` cannot be the same as any `<star destination>`.

`<or function>`

Performs logical OR with the Input BNC B signal and one of the STAR lines' signal, then routes the resulting signal to one or multiple STAR lines. The `<star source>` cannot be the same as any `<star destination>`.

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NONE

Disables the Input BNC B.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available
-201	Routing resource not available

Description: The Input BNC B signal can be used as a protocol trigger, or it can be logically AND'd or OR'd with one of the STAR lines and the resulting signal routed to one or more STAR lines.

Only STARX2...5 and STARY2...5 are available for Option 01 hardware.

Example: `BNCBIN ESTST,ECLTRG4,TTLTRG1`

In this example, Input BNC B is used as an Extended Start Stop protocol trigger. ECL trigger line 4 is used as the ESTST qualifier and TTL trigger line 1 is used to transmit the START/STOP value.

`BNCBIN STST,TTLTRG0`

In this example, Input BNC B is used as a Start Stop protocol trigger. TTL trigger line 0 is used to transmit the START/STOP value.

`BNCBIN SYNC100,ECLTRG2`

In this example, Input BNC B is used as a SYNC100 protocol trigger. ECL trigger line 2 is used as the qualifier.

`BNCBIN OR,STARX2,STARY5,STARY8`

In this example, the signal from Input BNC B is logic ORed with the signal from STARX2, and the resulting signal is routed to STARY5 and STARY8.

`BNCBIN AND,STARX7,STARX4,STARY3,STARX10`

In this example, the signal from Input BNC B is logic ANDed with the signal from STARX7, and the resulting signal is routed to STARX4, STARY3 and STARX10.

Related Commands: None.

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BNCBOUT

BNCBOUT

Purpose: Routes a signal to Output BNC B.

Syntax:

```
BNCBOUT <source>

<source> ::= {CLK|STARXx|STARYx|NONE}
        where x ::= 1-12
```

Parameters: <source>

The signal source can be CLK10, or one of the STAR lines.

If NONE is selected, Output BNC B is disabled.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available
-201	Routing resource not available

Description: The BNCBOUT command routes a signal from either CLK10 or one of the STAR lines to Output BNC B.

Only STARX2...5 and STARY2...5 are available for Option 01 hardware.

Example:

```
BNCBOUT NONE
```

In this example, Output BNC B is disabled.

Related Commands: None.

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CMDIN CMDIN

Purpose: Sets up Protocol Unit for command trigger.

Syntax:

```
CMDIN {<start stop>|<extended start stop>|<sync100>|NONE}

<start stop> ::= <STST,TTLTRGx>
        where x ::= 0-7
<extended start stop> ::= <ESTST,ECLTRGx,TTLTRGy>
        where x ::= 0-5
        where y ::= 0-7
<sync100> ::= <SYNC100,ECLTRGx>
        where x ::= 0-5
```

Parameters:

`<start stop>`

Uses the Command Trigger (CMDTRG) command as a trigger signal to Protocol Unit 2. Protocol Unit 2 is set up for Start Stop protocol. One of the TTL trigger lines is selected to transmit START/STOP values.

`<extended start stop>`

Uses the Command Trigger (CMDTRG) command as a trigger signal to Protocol Unit 2. Protocol Unit 2 is set up for Extended Start Stop protocol. One of the TTL trigger lines is selected to transmit START/STOP values and one of the ECL trigger lines is selected as qualifier.

`<sync100>`

Uses the Command Trigger (CMDTRG) command as a trigger to Protocol Unit 2. Protocol Unit 2 is set up for SYNC100 protocol. One of the ECL trigger lines is selected as qualifier.

If NONE is selected, Protocol Unit 2 is disabled.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available

Description: This command sets up Protocol Unit 2 for a command trigger. Then the CMDTRG command can be used to send a trigger.

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Example:

```
CMDIN ESTST,ECLTRG3,TTLTRG4
```

In this example, Extended Start Stop protocol is selected for Protocol Unit 2 and ECL trigger line 3 is used as a qualifier. TTL trigger line 4 is used to transmit the START/STOP value.

```
CMDIN STST,TTLTRG0
```

In this example, Start Stop protocol is selected for Protocol Unit 2 and TTL trigger line 0 is used to transmit the START/STOP value.

```
CMDIN SYNC100,ECLTRG3
```

In this example, SYNC100 protocol is selected for Protocol Unit 2 and ECL trigger lilne 3 is used as a qualifier.

Related Commands: CMDTRG

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CMDTRG

CMDTRG

Purpose: Sends a trigger command to protocol unit.

Syntax: `CMDTRG {START|STOP}`

Parameters: `{START|STOP}`

Selects either the START or STOP trigger command.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available

Description: When this command is executed, a START or STOP trigger command will be sent to Protocol Unit 2. The protocol unit must first be set up by the CMDIN command.

NOTE

Always follow a START command with a STOP command before attempting to send another START command.

Example: `CMDTRG START`

In this example, a START trigger command is sent to Protocol Unit 2.

Related Commands: CMDIN

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POWER? POWER?

Purpose: Reads the voltages of the current system power supplies.

Syntax: `POWER?`

Parameters: None.

Results: Returns a string which indicates the current voltages in the power supplies. On error, returns:

-200 Hardware not available

Description: This command returns the current voltage for the +24V, +12V, +5V, –24V, –12V, –5.2V and –2V power supplies.

Example:

```
POWER?
+24V:24.1V +12V:11.9V +5V:5.0V -24V:-23.9V -12V:-12.1V
-5.2V:-5.1V -2V:-2.0V
```

In this example, the response to the POWER? query indicates that the current voltage for the +24V supply is 24.1V; for the +12V supply, voltage is 11.9 V, etc.

Related Commands: None.

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STAROUTEA STAROUTEA

Purpose: Routes a signal from any one of the VXIbus STAR lines to one or more STAR lines.

Syntax:

```
STAROUTEA <source>[,<destination>]...

<source> ::= {STARXx|STARYx|NONE}
        where x ::= 1-12
<destination> ::= {STARXx|STARYx}
        where x ::= 1-12
```

Parameters: `<source>`

One of the VXIbus STAR lines is used as a signal source. If NONE is selected, the signal route will be disabled and the second parameter will be omitted. The `<source>` cannot be the same as any `<destination>`.

`<destination>`

One or more STAR lines can be selected as a signal destination. If NONE is selected on the first parameter, this parameter is omitted. Any one of the `<destination>` values cannot be the same as `<source>`.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available
-201	Routing resource not available

Description: The STAROUTEA command routes a signal from any one of the STAR lines to one or more STAR lines. STARROUTEA and STARROUTEB provide identical functionality. They allow for two STAR routes to be concurrently defined.

Only STARX2...5 and STARY2...5 are available for Option 01 hardware.

NOTE

If NONE is selected, the driver and receiver of the previous route will be disabled.

Example:

```
STAROUTEA STARY5,STARX2
```

In this example, a signal from STARY5 is routed to STARX2.

Related Commands: STAROUTEB

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STAROUTEB STAROUTEB

Purpose: Routes a signal from any one of the VXIbus STAR lines to one or more STAR lines.

Syntax:

```
STAROUTEB <source>[,<destination>]...

<source> ::= {STARXx|STARYx|NONE}
        where x ::= 1-12
<destination> ::= {STARXx|STARYx}
        where x ::= 1-12
```

Parameters:

`<source>`

One of the VXIbus STAR lines is used as a signal source. If NONE is selected, the signal route will be disabled and the second parameter will be omitted. The `<source>` cannot be the same as any `<destination>`.

`<destination>`

One or more STAR lines can be selected as a signal destination. If NONE is selected on the first parameter, this parameter is omitted. Any one of the `<destination>` values cannot be the same as `<source>`.

Results: None for success. On error, returns one of the following error numbers:

-100	Parameter error
-200	Hardware not available
-201	Routing resource not available

Description: The STAROUTEB command routes a signal from any one of the STAR lines to one or more STAR lines. STARROUTEA and STARROUTEB provide identical functionality. They allow for two STAR routes to be concurrently defined.

Only STARX2...5 and STARY2...5 are available for Option 01 hardware.

NOTE

If NONE is selected, the driver and receiver of the previous route will be disabled.

Example:

```
STAROUTEB STARX3,STARY2,STARY4
```

In this example, a signal from STARX3 is routed to STARY2 and STARY4.

Related Commands: STAROUTEA

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TEMP? TEMP?

Purpose: Reads the current board temperature in the VX5530/VX5535.

Syntax: `TEMP?`

Parameters: None.

Results: Returns a floating point value which indicates the current temperature of the VX5530/VX5535 in degrees Celsius.

Description: The TEMP? command returns the current board temperature in the VX5530/VX5535. On error, returns:

-200 Hardware not available

Example:

```
TEMP?
37.1
```

In the example, the string response to the TEMP? query indicates the current temperature in the VX5530/VX5535 is 37.1°C.

Related Commands: None.

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Section 6
Options

The following options are available for the VX5530/VX5535.

Option 01

This option removes STARbus routing units 2 and 3, reducing the STARbus functionality to VXIbus slots 2 through 5.

Option 03

This option provides Ethernet functionality by replacing the parallel printer port with a factory installed Western Digital Ethernet card. The WD80003EB supports most major Ethernet software packages. Additional drivers can be obtained through Western Digital. The Ethernet hardware has been optimally configured at the factory. The settings are as follows (See Figure 6-1):

I/O Address: 280H
Interrupt Req: 3
DMA: None
RAM Address: D0000
ROM Address: D8000
Network Type: BNC

The WD80003EB Ethernet PC adapter card comes with two interface ports for connection to a network. The 15 pin D-Sub connector is used for connection to an external transceiver, usually found on thick Ethernet networks. The BNC port allows connection to a thin Ethernet network. Refer to the Western Digital EtherCard Plus documentation for more information.

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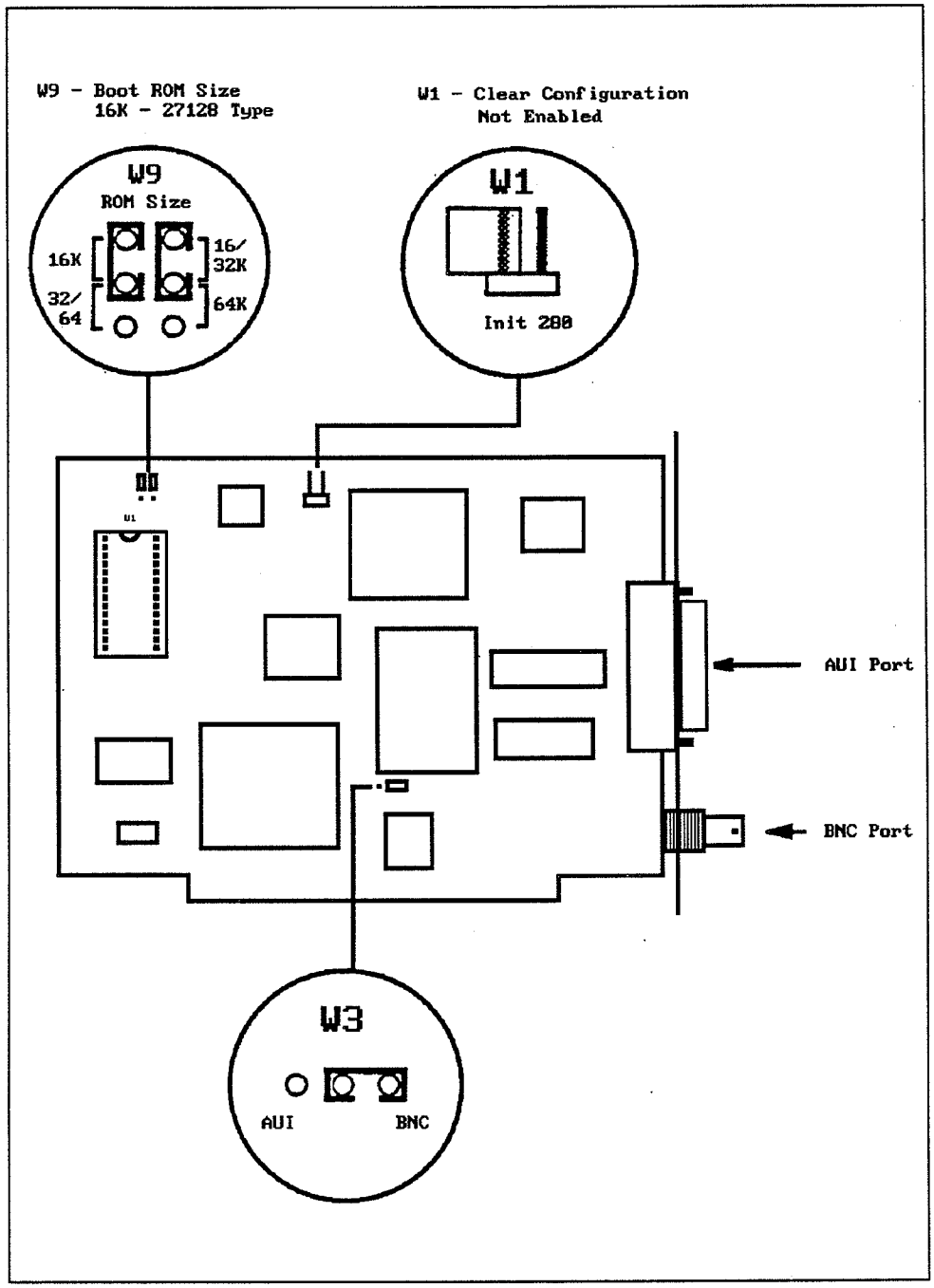


Figure 6-1. Factory default settings for Ethernet.

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Option 04

This option provides Token-Ring functionality by replacing the parallel printer port with a factory installed IBM Token-Ring Network PC Adapter. This card supports the IBM PC Lan Program and many other Token-Ring network applications. Additional drivers can be obtained from your network dealer. The Token-Ring hardware has been optimally configured at the factory. The settings are as follows:

I/O Address: N/A
Interrupt Req: 3
DMA: None
RAM Address: D8000
ROM Address: DC000
Adapter Type: Primary

The IBM Token-Ring PC adapter card comes with a standard interface port for connection to a network. The 9-pin D-Sub connector is used for connectioi to an IBM Token-Ring Cable. The Token-Ring Cable connects to a multi-station access unit. Refer to the IBM Token-Ring Adapter documentation for more information.

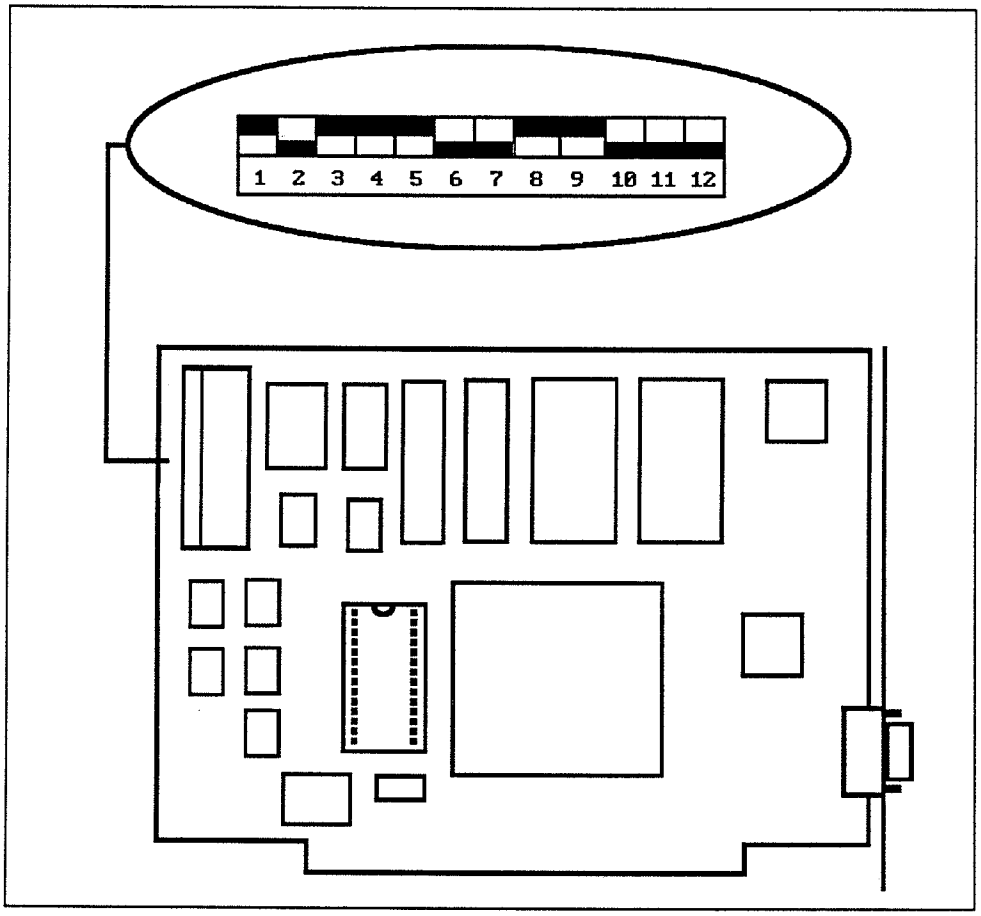


Figure 6-2. Factory default settings for Token-Ring.

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Option 1E (European Customers Only)

European orders for the VX5530/VX5535 must include this option. This option deletes the NEC 2A Video Display from the system. Customers are urged to purchase the NEC 2A E version monitor from their local distributor. The VX5530/VX5535 can use any VGA 640 x 480 style display, preferably one with multi-sync capability to achieve the maximum video resolution of 800 x 600.

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Appendix A
VX5530/VX5535 Architecture

The architectural features of the VX5530/VX5535 are described in three parts within this section. The first part describes the features and implementation of the CPU from the inside, as a PC/AT architecture. The second part describes the implementation from the VXIbus perspective, describing its special VXIbus features. The third part describes the Advanced Trigger Functions (ATF).

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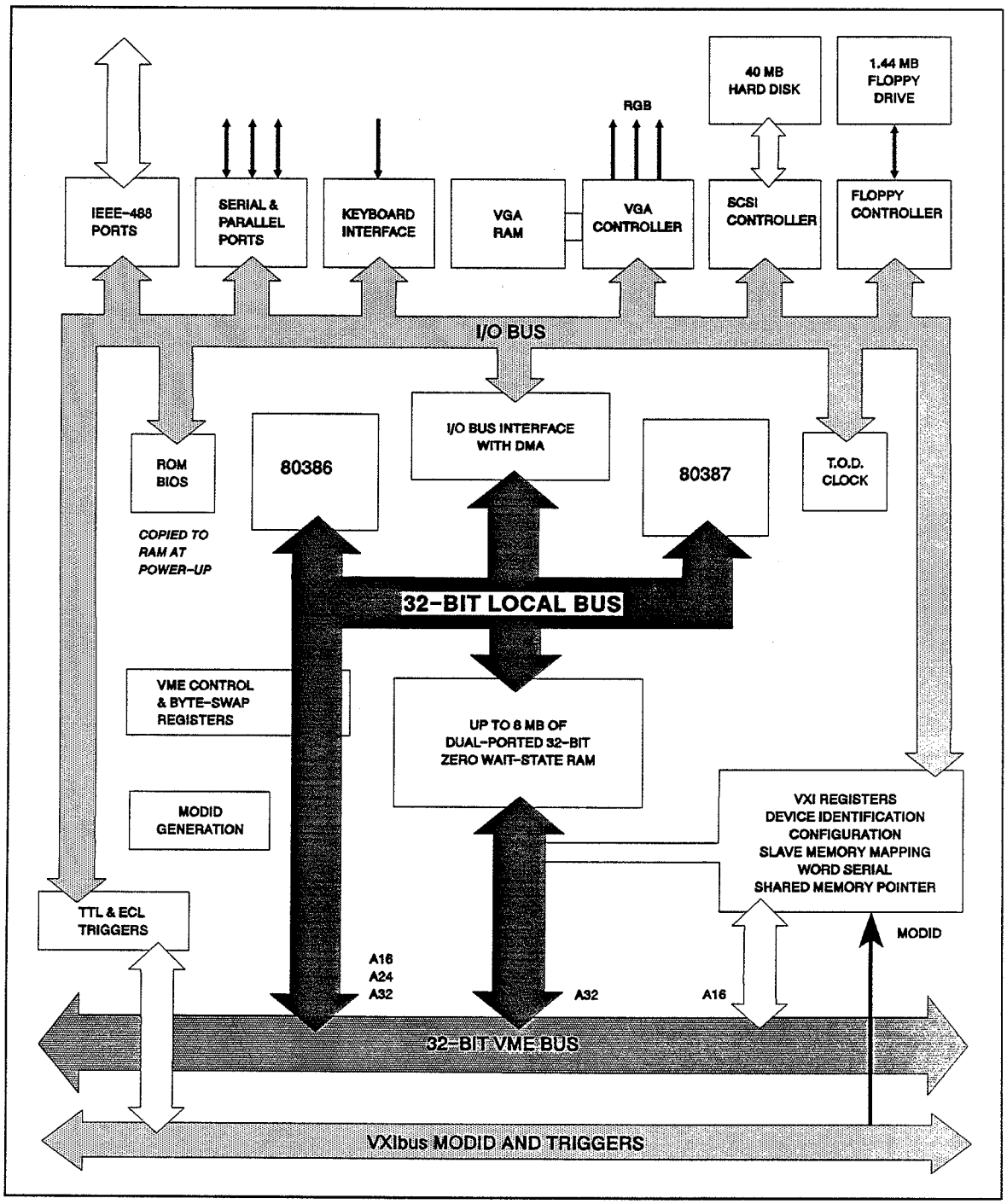


Figure A-1. VX5530 CPU Block Diagram.

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VX5530/VX5535 Architecture (as a PC/AT)

The VX5530/VX5535 is physically implemented as a single circuit board, enclosed in a dual-wide module that includes both hard and floppy disk drives.

An Intel 80386 with an 80387 arithmetic coprocessor performs the basic processor functions in the system. The processor(s) run at rates of either 16 (VX5530) or 20 MHz (VX5535), and are connected with each other and with memory by 32-bit data and address buses.

Peripheral devices (I/O ports) connect through an onboard I/O bus connected to the CPU's local 32-bit data bus through an interface that provides AT compatible addressing with full DMA capabilities.

Memory Architecture

The on-board RAM memory array provides for up to 8 MBytes of memory on the 386's local 32-bit bus. Page mode DRAM's allow zero wait-state access at either 16 or 20MHz.

On-board RAM is addressable linearly, starting at address 0. Boot ROM's reside in high memory. All addresses between the lower 32M and the upper 16M of the 4GB address space (02000000 to FEFFFFFF hex) are mapped to the VXIbus. Refer to the second part of this section for a more complete description of memory mapping.

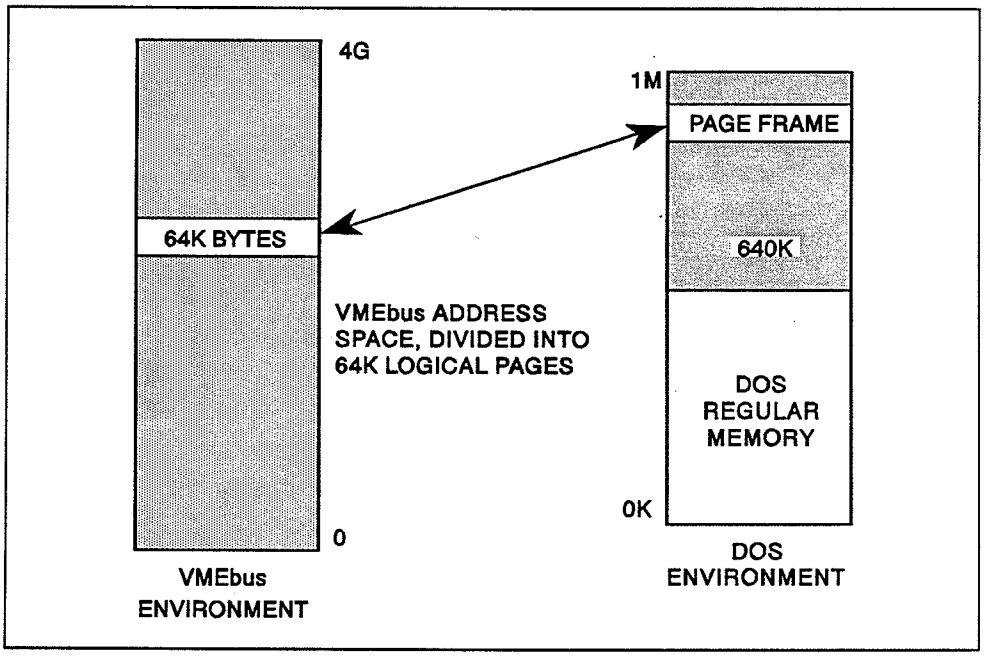


Figure A-2. VXI page frame.

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VXIbus Page Window

Special hardware has been provided to allow accessing the full 32-bit VXIbus from within the DOS environment. A special area of the memory map, called the VXIbus page frame, is located in the reserved memory area above the conventional DOS 640K-byte memory boundary. On a VX5530/VX5535, as in other DOS systems, portions of this area are also used for VGA video RAM and BIOS ROM's.

The VX5530/VX5535 Bus Interface Manager provides a complete interface to the VXIbus Window, designed to be used by both applications programs and interrupt handlers.

VXIbus windowing hardware works by dividing the VXIbus address space into 64K-byte logical pages that can be accessed through a block of DOS addressable memory called the *page frame*. See Figure A-2. Each of the VXIbus address spaces (A16, A24, and A32) can be addressed through this mechanism.

By appropriate calls to the Bus Interface Manager, any logical page on the VXIbus can be made to appear in the page frame, so that a read, write, or block move to the DOS physical page becomes a read, write, or block move to the VXIbus logical page. This is very similar to the technique defined by the Lotus/Intel/Microsoft Expanded Memory Specification (LIM 4.0 EMS) to access memory outside the normal DOS address range.

BIOS

The BIOS, configured specifically for the VX5530/VX5535, is licensed from Award Software. The single ROM, which includes a standard BIOS with VGA and SCSI drivers, is at physical address FFFF0000. To guarantee the highest possible performance, the BIOS is copied into the processor's 32-bit RAM at the normal DOS addresses.

VXIbus Features

The VXIbus is a major addition to the PC/AT architecture. VXIbus features are controlled by both local configuration registers and the VXIbus register set.

With the exception of the hardware jumpers that enable VXIbus slot-0 functions, all VXIbus features are software controlled by special interface registers. The on-board ROM-based set-up program provides the configuration control, and the BusManager provides a transparent high-level software interface to these registers.

The TekVICS software package provides a complete, easy to use software interface to all the VXIbus features of the VX5530/VX5535, so that the programmer rarely if ever needs to deal with the hardware at the register level.

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Table A-1 VX5530/VX5535 VXIbus Interface Register Summary

External Registers	Function	VXIbus offset	PC I/O addresses
VXIbus ID	Identifies class, manufacturer	0	140, 141
VXIbus Device Type	Memory and model code	2	142, 143
VXIbus Status & Control	Miscellaneous	4	144, 145
VXIbus Slave Offset	Sets shared memory base address	6	146, 147
VXIbus Protocol/Signal	Indicates communications capabilities	8	148, 149
VXIbus Response	Status indicators for critical items	A	14A, 14B
VXIbus Data High	Word-serial Read / Write data buffer	C	14C, 14D
VXIbus Data Low	Word-serial Read / Write data buffer	E	14E, 14F
VXIbus A32 Shared Mem.	High word address register	14	none
VXIbus A32 Shared Mem.	Low word address register	16	none
VXIbus Alt Response	Alternate Bus response register	18	none
Internal Registers	**Function**		**PC I/O address**
Bus Window Address	Sets Base address for bus windowing		150
Bus Window Modifier	Sets bus address modifiers / special functions		151
Bus Interrupt State	State info of VXIbus and bus interrupts 1-7		152
Bus Interrupt Enable	Enable masks for VXIbus and bus interrupts 1-7		153
Bus Event State	Contains state info of "special" conditions		154
Bus Event Enable	Enable mask for special condition interrupts		155
TTL Trigger State	Captures TTL trigger lines		156
	(reserved)		157
MODID/Interrupt	Generates MODID and Interrupt signals		158
MODID	Generates MODID High byte		159
TTL Trig Drive	Generates TTL Triggers		15A
ECL Triggers	Generates / captures ECL triggers		15B
Unique Logical Addr	Sets ULA		15C
Int Status/Control	Internal status/control		15D
Signal Reg Low	VXIbus Signal register FIFO, low byte		15E
Signal Reg High	VXIbus Signal register FIFO, high byte		15F

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VXIbus Master

As a VXIbus master, the VX5530/VX5535 can generate A32, A24, and A16 accesses, and can handle D32, D24, D16, D08(EO) and UAT data transfers. Block-transfer modes are not supported.

A register-based hardware interface provides a window into the VXIbus and enables generation of the different types of VXIbus access. The two registers required to do this, the VXIbus Window Address register and the VXIbus Window Modifier register are used together or independently to access the bus. The Window Modifier register determines the address mode used, selecting the A16, A24, or A32 address space and setting the VXIbus-defined address-modifier bits. It also controls the byte-order used for the access. As such, the register is used with or without the VXIbus Window Address register, which sets the page frame address described in and used by the TekVICS package.

A write buffer is provided to decouple the speed of the 386 from the slower speed of the VXIbus. Memory locking operations (read-modify-write cycles) are fully supported, allowing transparent and reliable semaphores to be built.

The board can respond to any of the seven VXIbus interrupts, as well as ACFAIL, BERR and SYSFAIL, and is compatible with vector passing release-on-acknowledge (ROAK) devices. Six hardware registers monitor and control interrupt response and generation of the VXIbus and VXIbus-defined interrupts.

Slave Operation

The VX5530/VX5535 is an A32 and A16 VXIbus slave device, that is, it will respond to both A16 addresses and A32 addresses. It will not respond to A24 addresses.

The VXIbus registers respond to A16 addresses. Typically, since the VX5530/VX5535 is usually the slot-0 controller and logical device 0, they are at address C000. The VX5530/VX5535 is a "dynamic configuration" device, and if the VX5530/VX5535 is not the slot-0 controller, the logical address is assigned by the system resource manager.

On-board memory responds to A32 addresses. This dual-ported memory can be mapped to any of 8 consecutive 16M blocks of A32 space, starting at 32-bit address 18000000 (hex). The first two digits of the valid addresses are thus 18, 19, ... through 1F. Assignment of address ranges is done by the Start-Up Resource Manager in the system.

Since the VX5530/VX5535 can be both a master and a slave, it can address itself across the VXIbus. If the on-board memory is mapped to VXIbus address 18000000, it can be addressed at either local address 00000000 or at VXIbus address 18000000. Local addressing is faster, of course, but VXIbus addressing allows use of byte-swapping hardware.

Likewise, the board's VXIbus registers can be addressed at either their local I/O space addresses or on the VXIbus at their A16 addresses.

The board can generate any of the 7 VXIbus interrupts, and will release the interrupt line on interrupt acknowledge (ROAK).

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System Controller Functions

When the VX5530/VX5535 is acting as a slot-0 controller, it also needs to provide bus arbitration functions. These functions, disabled if the VX5530/VX5535 is not a slot-0 device, include priority and round-robin bus arbitration, IACK daisy-chain driving, SYSRESET and SYSCLK generation and bus timeout detection.

Any time the VX5530/VX5535 is a bus master, whether or not it is the system controller, a bus access/release mechanism must be used. ROR (release-on-request) and RONR (request-on-no-request) bus release mechanisms are supported, with RONR as the default.

VXIbus Registers

A custom gate array designed specifically for the VX5530/VX5535 provides the full compliment of VXIbus registers. All the registers required to support shared-memory protocols and to implement a message based commander (or slave) are implemented, in full compliance with the VXIbus version 1.2 specifications.

The VXIbus registers map into the VXIbus A16 address space at the address determined the module's unique logical address. The register starting address is at 40 x (logical address) + C000 (all values are hex). The VX5530/VX5535 supports Dynamic Address Configuration. These registers are dual ported, available both from the VXIbus and locally on the CPU I/O bus. Complete definitions of the functionality and use of the registers can be found in the VXIbus System Specification, available from VITA, (the VMEbus Industry Trade Association) 10229 N. Scottsdale Rd., Suite E, Scottsdale, AZ 85253. The second part of this section describes the VX5530/VX5535 specific usage.

The TekVICS software package provides a complete, easy to use software interface to the VXIbus functions of the VX5530/VX5535, so that the programmer rarely if ever needs to deal with the hardware at the register level.

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VX5530/VX5535 Architecture (VXIbus-Specific)

This second part provides the details of the VXIbus-specific aspects of the VX5530/VX5535 architecture. In general, features that are exactly equivalent to those provided by an IBM PC/AT are not discussed. Virtually all of the VX5530/VX5535 hardware features are supported at a software interface level by TekVICS, so the vast majority of programmers and designers will never need to directly manipulate the hardware described in this section.

All the features of the VX5530/VX5535 that are represented on a standard PC/AT are functionally identical to the feature on the AT. Specifically, the serial and printer ports, DMA, general I/O, floppy disk interface, and keyboard interface are exactly the same and will not be discussed further. For details, refer to the "IBM Personal computer AT Technical Reference Manual", IBM document number 62280070 S299-9611-00 and the "IBM Personal System/2 Model 50 and 60 Technical Reference Manual", number 68x2224 for VGA details.

VXIbus Registers

The eleven 16-bit VXIbus registers reside in the A16 address space at a VXIbus-defined offset determined by the device's unique logical address. The VX5530/VX5535 can have logical addresses 00 through FF, so the registers will be addressed at any A16 addresses C000, C040, ..., through FFC0. The register set aliases in the allocated board address space, with offsets 32 through 63 aliasing offsets 0 through 31. No offsets within the 64-byte space generate a bus error when read from the VXIbus.

The VXIbus registers are accessible with D16 accesses from the VXIbus. However, they appear as pairs of 8-bit ports in the VX5530/VX5535's I/O address space. To avoid any possible conflict with standard PC I/O device addresses, these registers map into the upper 32K of the 16-bit address space. Address bits 15 (which must be 1) and 9 through 0 are used to decode them. In the following descriptions the registers are described as addressed at 8xxx.

The following table defines the VXIbus registers. Field/bit descriptions include designations as required or DD (device dependent), and RO, R/W for read-only or read/write capabilities. For further elaboration of the usage and the intent of the required registers or fields, refer to rev 1.2 of the VXIbus specification. The offset from the A16 base address is shown with a letter U or L. U means that these bits are bits 8-15 when read from VXI, and L means that they are bits 0 through 7.

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Table A-2 VXIbus Register Bit Definitions

Name	PC I/O port addr	VXI A16 offset	7	6	5	4	3	2	1	0
VID	8141	0U	1	0	0	1	1	1	1	1
	8140	0L	1	1	1	0	1	1	0	0
VDT	8143	2U	0	1	1	1	0	0	0	S
	8142	2L	1	1	1	1	1	1	1	1
VSC	8145	4U	SLE	MODI	SYSR	1	1	1	1	1
	8144	4L	SRIE	POSR	SYSC	1	R	PASS	NOSF	RSTP
VSO	8147	6U	0	0	0	1	1	SB2	SB1	SB0
	8146	6L	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
VPR	8149	8U	0	0	0	1	1	0	1	1
	8148	8L	1	1	1	1	1	1	1	1
VRE	814B	AU	0	1	R	R	R	RRDY	WRDY	1
	814A	AL	R	1	ABMH	SIG	MLCK	WRCP	FSIG	LSIG
VMH	814D	CU	RAM							
	814C	CL								
VML	814F	EU	RAM							
	814E	EL								
VSL		14U	RAM							
		14L								
VSL		16U	RAM							
		16L								
VARE		18U	1	1	1	1	1	1	1	1
		18L	R	1	ABMH	SIG	MLCK	WRCP	FSIG	LSIG

VID—VXIbus ID Register

The fields in this register define the VX5530/VX5535 as a message-based A16/A32 device built by Tektronix. Bits 15-12 define the characteristics, and the remaining bits are Tektronix's VXIbus manufacturer's code of 4076.

A write to the low-order eight bits of this register from either the PC or VXIbus ports is interpreted as setting the VX5530/VX5535's logical address, as described in the VXIbus Specification for the optional dynamic logical address configuration option.

VDT—VXIbus Device Type Register

This read-only register defines the VX5530/VX5535 as occupying 16MB of the A32 address space, and having a model designator of 4095. Bits 15-12 define the memory capacity, and bits 11-0 are the VX5530/VX5535 model code. The model code is 255 if the VX5530/VX5535 is configured as a slot-0 controller, and is 511 if it is not.

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VSC—VXIbus Status/Control Register

This register is dual-ported: readable and writeable from both the VX5530/VX5535 and the VXIbus. It contains both "required" and "device-dependent" bits.

SLE (Required, R/W) Slave-memory enable. If *set*, A32 accesses are permitted from the VXIbus bus into the VX5530/VX5535's DRAM. If *clear,* the VX5530/VX5535 doesn't respond to A32 accesses from VXIbus.

MODI (Required, RO) MODID*. This bit is connected to pin 30 in row A of the VMEbus/VXIbus P2 connector. A 0 value denotes that the device is being selected by someone pulling the pin high.

SYSR (DD, R/W) Setting this bit asserts VXIbus SYSRESET.

SRIE (DD, R/W) SysReset In Enable. If *set*, SYSRESET on the bus resets the VX5530/VX5535.

POSR (DD, RO) This bit is the low-order bit of the POS shift register, and is used to examine the POS while shifting it. There is a discussion of the POS register at the end of this section.

SYSC (DD, RO) This bit is cleared by writing to the lower 8 bits of this register, and is set after 4 SYSCLK rising edge transitions. This is a diagnostic bit that indicates that the VX5530/VX5535 is receiving SYSCLK.

R (Required, R/W) Extended self-test. This is solely a RAM bit, completely under software control. When PASS is 1, EXTE 0 indicates that the VX5530/VX5535 is executing an extended self test. See also the discussion of RESET behavior below.

PASS (Required, R/W) Passed self-test. A 0 indicates that the VX5530/VX5535 has not yet passed its power-on self-test (POST). This bit is connected to the test indicator on the front panel, which is on when the bit is zero. See also the discussion of RESET behavior below.

NOSF (Required, R/W) No SYSFAIL. Setting this bit prevents the VX5530/VX5535 from asserting the VXIbus SYSFAIL line.

RSTP (Required, R/W) Reset. Setting this bit forces a reset of the VX5530/VX5535. Actual behavior is discussed in the RESET section.

The VSC register contains some critical information located in the "device-dependent" positions as per VXIbus. Because of this, a device must not blindly write into another device's VSC register. Rather it should read VSC, modify under mask whatever VXIbus bit(s) it wishes to alter, and then write the value back into VSC.

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The PASS and EXTE bits of the VSC register are intimately tied to the reset sequence of the VX5530/VX5535. The VXIbus specification makes specific provisions for devices like the VX5530/VX5535 that may take a long time to become fully operational, and the VX5530/VX5535 follows the VXIbus guidelines exactly. The POST routine, upon completion but before DOS boots, sets PASS and EXTE, indicating to the VXIbus systems that the module is up and working but not yet fully self-tested. When the extended self-test is completed by R, EXTE is zeroed.

Setting NOSF when RSTP is set denotes the safe state. When in the safe state, the VX5530/VX5535 can only be restarted by another VXIbus device or by a full power-up reset. The RUN light will not be illuminated, the display will be blank, and the front panel reset switch will not be effective.

VSO—VXIbus Slave Offset Register

This register defines the size and sets the location of the VX5530/VX5535 in the A32 address space. It is only meaningful if the slave-enable bit (SLE) in the VSC register is set.

BASE (Required, R/W) These bits define the variable portion of the VX5530/VX5535 slave address.

OF7-0 (Required, RO) These bits are read-only from the VXIbus, and written/read from the PC I/O address. They are the same as the lower 8 bits of the VSH register, where they may be written.

The register value indicates that the VX5530/VX5535 occupies a 16 MB address space. The three slave base bits allow the memory to be mapped into any of the 8 16MB areas starting at 18000000H. Thus, if SLE is set, the VX5530/VX5535 responds to VXIbus A32 accesses where bits A31-A24 are 00011aaa, where aaa are bits 10-8 of this register.

VPR—VXIbus Protocol/Signal Register

When read, this register describes the communication protocols the VX5530/VX5535 supports. The first six bits define the VX5530/VX5535 as both a servant and commander, with a signal register, bus master and interrupter capabilities, shared memory registers, and without the ability to receive fast-handshake word-serial transfers.

The VX5530/VX5535 can only read this register. Writing to it has no effect.

Writing from the VXIbus writes to the two-deep signal register FIFO. This asserts an VX5530/VX5535 interrupt, shuffles the signal register FIFO, and will return a BERR if the FIFO is full.

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VRE—VXIbus Response Register

Reading this register returns the status of the VX5530/VX5535's word-serial communications registers (VML, VMH) and their associated functions. There are hardware side-effects associated with the act of reading the register. Program logic provides control of the four "R" bits.

R — RAM bits associated with VXIbus bits DOR, DIR, and ERR functions. Initial settings are 001 for 13-11, and 1 for bit 7.

RRDY — (required, RO) Read ready. A 1 denotes that VML and/or VMH contain data from the VX5530/VX5535 to be read by some other master.

WRDY — (required, RO) Write ready. A 1 denotes that the message register is available for an incoming message. A 0 denotes that someone has written into register VML.

ABMH — (DD, R/W) This flag bit is associated with the VMH location monitor. It is set when VMH is written to from the VXIbus and is cleared when VMH is read or written by the VX5530/VX5535.

SIG — (DD, RO) A 1 means that the signal register FIFO is not empty.

MLCK — (DD, R/W) This message Lock bit allows synchronization of multiple senders of messages to this module. A 0 means that a message sender has locked the message register for the sending of a message. A 1 means the message register is available for locking.

FSIG — (DD, RO) If SIG = 1 the number (0...1) of the FIFO register holding the first (earliest) signal; otherwise undefined. Used in testing.

LSIG — (DD RO) If SIG = 1 the number (0...1) of the FIFO register holding the last (most recent) signal; otherwise undefined. Used in testing.

A read of VRE from the VXIbus returns the current values of RRDY, WRDY and MLCK.

VMH—VXIbus Message High Register

This register holds the most-significant half of 32-bit (long-word serial) messages. An access to this register clears AVMH.

VML—VXIbus Message Low Register

This register holds 16-bit (word serial) messages from VXIbus, or the least-significant half of 32-bit (long-word serial) messages. There are ordering protocols to be followed in accessing this register, and accesses to this register alter bits in VRE. Note that word serial protocols are half-duplex.

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VSH—VXIbus Shared memory pointer (High) Register

This register holds the most-significant half of a 32-bit (long-word) memory pointer. It is used by software, along with VSL, to implement the VXIbus shared-memory protocol. These 16 bits are physically the same register as the VSO register. The upper 8 bits of VSH are read-only (using this address). The lower 8 bits are read/write.

VSL—VXIbus Shared memory pointer (Low) Register

This register holds the least-significant half of 32-bit (long-word) memory pointer. It is used by software, along with VSH, to implement the VXIbus shared-memory protocol. All bits in these registers may be written only from the VXIbus. The low order bit is RAM to implement rule G.1.17 of the VXIbus Specification, and must be initialized to 1 by software until VSH contains a valid CSDA pointer.

VARE—VXIbus Alternate Response Register

This register is read-only and contains a copy of the lower 8 bits of the VRE register. Reading this register performs a test-and-set operation on MLCK, clearing it after the read if WRDY is set.

The protocol for sending a message to the VX5530/VX5535, if there are multiple potential senders, is the following. The sender first reads VARE. If both WRDY and MLCK are 1, he may then proceed to send the message; if not, he must spin or wait for this condition. For 16-bit messages, he writes into VML. For 32-bit messages, he must write first into VMH and then into VML.

RRDY, ABMH, WRDY and MLCK are altered by hardware-detected conditions. A write into all of, or the lower 8 bits of BML clears WRDY. A read or write to all of, or the lower 8 bits of, VMH clears AVMH. A read from VML clears RRDY. As mentioned above, a read of BRE from the VXIbus clears MLCK if WRDY is set. The valid states are:

RRDY	WRDY	MLCK	State
0	1	1	Write ready (awaiting incoming msg)
0	1	0	Write ready, locked by a sender
1	0	X	Read ready (outgoing data present)
0	0	X	Not ready for write or read

The specific interpretation the VX5530/VX5535 assigns to MLCK in the VXIbus response register is used for synchronizing multiple message senders. The ability to deal with multiple message senders is a capability that exceeds the current requirements of the VXIbus specification.

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VXIbus Control Registers

The control registers used to integrate the VXIbus are another addition to the architecture. This discussion will completely define their behavior. These 8-bit registers in the processor's I/O space are not accessible from the VXIbus.

The registers and associated hardware provide the interface to the following functional elements:

1. A window in the PC address space below one megabyte in which one can perform a wide variety of VXIbus access types.

2. A direct mapping of the 386's physical address space (02000000 - FEFFFFFF) into VXIbus.

3. TTL and ECL trigger control.

4. Interrupt processing, generation and response.

5. Signal register operation.

6. MODID generation and unique logical address control.

The VXIbus control registers are enumerated below. These registers are addressable as 8-bit I/O ports from the VX5530/VX5535, and are not addressable from the VXIbus.

Table A-3. VXIbus Control Register Bit Definitions

Name	PC I/O addr	7	6	5	4	3	2	1	0
BWA	8150	WA31	WA30	WA29	WA28	WA27	WA26	WA25	WA24
BWM	8151	WA23	WA22	BSEX	IACK	AM5	AM4	AM2	AM1
BIS	8152	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR
BIE	8153	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR
BES	8154	1	1	1	SIGR	WDT	ACFA	BERR	SYSF
BEE	8155	DSOR	VWR	1	SIGR	WDT	ACFA	BERR	SYSF
BTTS	8156	TTS7	TTS6	TTS5	TTS4	TTS3	TTS2	TTS1	TTS0
reserved	8157	1	1	1	1	1	1	1	1
BMOL	8158	M04	M03	M02	M01	M00	OINT3	OINT2	OINT1
BMOH	8159	M12	M11	M10	M09	M08	M07	M06	M05
BTTD	815A	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0
BET	815B	ES1	ES0	ED1	ED0	1	SBER	1	BSAM
BULA	815C	ULA7	ULA6	ULA5	ULA4	ULA3	ULA2	ULA1	ULA0
MSC	815D	1	IST	POSW	BTOE	WDTR	FWDT	1	1
SRFL	815E	RAM							
SRFH	815F	RAM							

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BWA—Bus Window Address Register

This register holds the value driven on VXIbus address lines A24-A31 for accesses from the VX5530/VX5535 through the 64K "window" into the VXIbus.

BWM—Bus Window Modifier Register

This register holds information used by the VXIbus interface during bus accesses. WA23 and WA22 only affect accesses through the window: the others affect all accesses to the VXIbus.

WA23-WA22 — These are the values driven on VXIbus address lines A23 and A22 for accesses from the VX5530/VX5535 through the VXIbus window.

BSEX — Byte sex. Controls byte-ordering for all D16 and D32 bus accesses. If 0, the bytes are transmitted in little-endian (e.g., 8086 style) order. If 1, the bytes are transmitted in big-endian (e.g., 68000 style) order.

IACK — Interrupt-acknowledge cycle. If 1, a read from the VX5530/VX5535 to VXIbus is treated as a VXIbus interrupt-acknowledge operation. The interrupt being acknowledged must be encoded by the VX5530/VX5535 software as a value on VXIbus address lines A1-A3. See the VMEbus specification for more information.

AMx — Address modifiers. These bits are used to drive the VXIbus address-modifier lines for accesses from the VX5530/VX5535, and are used to distinguish, for instance, A16/A24/A32 cycles. (VXIbus signal AM3 is always asserted, and AM0 is the inverse of AM1 for all VX5530/VX5535 bus accesses. Direct "Non-windowed" VXIbus accesses always generate an A32 address modifier.)

BIS—Bus Interrupt State Register

This read-only register contains the interrupt flags for the 7 VXIbus interrupts and the VXIbus message register location monitor.

IRQx — Interrupt request. These bits are clear if the corresponding VXIbus interrupt line is asserted.

MSGR — Message request. This bit is clear if both of bits RRDY and WRDY in register BRE are clear.

The MSGR interrupt source allows VX5530/VX5535 software to detect, without resorting to polling, (1) when an incoming message is present and (2) when outgoing data placed in VML has been read. If software expects no incoming messages and has no need to store outgoing data, the interrupt condition is present. Therefore, software needs to understand when it needs to mask MSGR.

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BIE—Bus Interrupt Enable Register

This is the VXIbus interrupt-enable register. If a bit in BIE is 1 and the corresponding bit in BIS is 0, an interrupt (INT 10) is sent to the VX5530/VX5535.

BES—Bus Event State Register

This read-only register contains state information on additional VXIbus-related conditions that may result in a VX5530/VX5535 interrupt. See the discussion of the watchdog timer in the description of the MSC register

SIGR This bit is clear if the signal register FIFO is not empty.

WDT This bit is clear if the watchdog timer's period has expired.

ACFA This bit is clear if VXIbus ACFAIL is asserted.

BERR This bit is clear if BERR was the response to the last operation from the PC to VXIbus.

SYSF This bit is clear if VXIbus SYSFAIL is asserted.

BEE—Bus Event Enable Register

This is another VXIbus interrupt-enable register, controlling the "bus event" interrupts. If a bit in BEE is 1 and the corresponding bit in BES is 0, an interrupt is sent to the VX5530/VX5535. Two other read-only bits in this register are status bits available to track the state of the data transfer bus. They are:

DSOR This bit is the logical OR of the DS0 and DS1 pins, and is clear if either DS0* or DS1* is asserted.

VWR This bit is clear during VMEbus WRITE operations.

BTTS—TTL Trigger Sample Register

This read-only register indicates the status of the TTL trigger lines. Note that reading BTTD and BTTS is not the same because of the open-collector nature of the triggers.

TTS0-7 A 1 in bit means that open-collector TTL trigger line TTLTRGx is asserted (zero) on the backplane.

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BMOL and BMOH—Bus MODID/Interrupter Register

These registers are readable and writable from the VX5530/VX5535, and control the LBUSA signals (the local bus on the "A" row of the VX5530/VX5535). These signals are used primarily for MODID generation when the VX5530/VX5535 is the slot-0 controller.

If this VX5530/VX5535 is not the slot-0 controller, the signals M01-M12 can be used for local bus communication with the module "on the left". In this case the bit controlling M00 should always be zero to avoid conflict with the slot-0 controller.

The second use of BMOL is to control the VX5530/VX5535's VMEbus/VXIbus interrupter capability.

M12 - 00 These read/write bits control the corresponding MODID signals. Writing to BMOH drives the 13 MODID pins. In other words, a write to BMOH causes the VXIbus MODID lines to be driven (assuming the VX5530/VX5535 is in slot 0). Reading the BMOH register deasserts the control pin. Reading BMOH and/or BMOL samples the MODID lines.

OINT3-0 These bits are the binary code for the interrupt to be asserted. If the three bits are not all zero, one of the seven VMEbus interrupt lines is asserted (e.g., IRQNUM=110 corresponds to IRQ6). An interrupt-acknowledge cycle from whomever responds to the interrupt causes these bits to be cleared.

Any VX5530/VX5535 reset, or setting bit RSTP in the VSC register, will cause it to terminate driving the MODID lines and reset IRQNUM to 0.

BTTD—TTL Trigger Drive Register

This register may be read and written from the VX5530/VX5535. A 1 in bit x asserts (low) VXIbus trigger line TTLTRGx. The outputs are synchronized with the 10 MHz ECL clock to allow use of the VXIbus start/stop protocol. Reading this register does not sample the bus's TTL trigger lines; to do this, use the BTTS register.

TTD0-7 A 1 in bit means that open-collector TTL trigger line TTLTRGx is asserted by the VX5530/VX5535.

Any condition that causes the VX5530/VX5535 to reset will clear BTTD.

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BET—ECL Trigger Register

This register may be read and written from the VX5530/VX5535, and controls the 2 ECL trigger signals. Any condition that causes the VX5530/VX5535 to reset will clear BET.

ED0 - 1 A 1 asserts the corresponding VXIbus ECL trigger line .

ES0 - 1 Read-only bits that show the state of ECLTRG0/1 (1 meaning asserted).

BSAM This bit is zero if a pipelined write from the VX5530/VX5535 is still outstanding on the VXIbus. Thus, it may be used to determine when it is safe to both look at SBER and/or proceed to the next VMEbus access.

SBER This is cleared whenever an VX5530/VX5535 VMEbus access results in BERR* being asserted. This bit may be written by software.

Any condition that causes the VX5530/VX5535 to reset will clear BET.

BULA—Bus Unique Logical Address Register

This register is readable and writable from the VX5530/VX5535. It contains the VX5530/VX5535's VXIbus device address. A write into register BID alters the value of BULA. Until and unless the value of BULA is altered after reset the VX5530/VX5535 will only respond to the combination of A16 address FFC0 and MODID# asserted. This allows the module to be dynamically auto configured.

Note that VXIbus observation F.3.1 requires that the resource manager reside at ULA 0 and not be dynamically configured. If the VX5530/VX5535 is the resource manager, the resource manager software explicitly stores a ULA of 0 into this register before it begins the dynamic configuration steps.

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MSC—Module Status/Control Register

This register controls several auxiliary functions, and is readable and writable. Many of these functions are critical to the correct operation of the VX5530/VX5535. Misuse can have catastrophic results.

IST — Determines whether a *response* status/ID word or an *event* status/ID word is used in response to an interrupt acknowledge cycle.

When the VX5530/VX5535 responds to an interrupt acknowledge, it returns a 16-bit status/ID value in either a *response* format or an *event* format, as defined by the VXIbus spec rule C.2.40. In both cases the lower 8 bits are the ULA.

If IST is 0, a *response* format is used. The upper 8 bits are the upper 8 bits of the Response Register (VRE), with bit 15 guaranteed to be 0.

If IST is 1, an *event* format is used. The upper 8 bits are settable by software, with data taken from the upper 8 bits of VMH, the upper longword serial message register. Though this means you can't be doing longword serial transfers at the same time, this is not a major constraint. Note that the user must set the highest order bit per rule C.2.40.

POSW — If set, this enables writing to the POS register. It is almost certainly a mistake to set this bit without having interrupts disabled. See the discussion on the POS register later in this section for further description of the POS hardware.

BTOE — If set, the bus time-out timer is enabled. This is set by the BIOS if the VX5530/VX5535 is the slot-0 controller.

WDTR — If set, expiration of the watchdog timer's period generates a reset of the VX5530/VX5535. If *clear*, an interrupt is generated instead.

FWDT — Fast watchdog timer. If *clear*, the period of the watchdog timer is about 6.7 seconds. If *set*, the period is about 210 ms.

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VX5530/VX5535 VXIbus Interrupt Generation And Response

When the VX5530/VX5535 responds to an interrupt-acknowledge, it returns a 16-bit status/ID value where the upper 8 bits are the value of the upper 8 bits of VRE, and the lower 8 bits are the logical address. This implements the VXIbus spec rule C.2.40 for message-based interrupters. See also the discussion of the IST bit in the MSC register, immediately preceding this section, for more on interrupt responses.

Software can read the BMOL register after writing to it to test if the interrupt has been acknowledged. Software can also write zeros into the BMOL register after sending an interrupt (explicitly de-asserting the interrupt), although this should only be done if one understands the behavior of to whomever the interrupt was signaled.

When using the Bus Interface Manager linked to a standard DOS interrupt handler, interrupt processing overhead from receipt of interrupt to when the interrupt handler gets called is about 36 microseconds. Handling time after the interrupt handler relinquishes control is about 26 microseconds. These times are for a 16MHz system, and does not include any DOS or Windows overhead.

RESET Behavior

The VX5530/VX5535 supports two device states specified by the VXIbus specification: soft reset and safe. These states are identical except that, in the safe state, the VX5530/VX5535 cannot drive SYSFAIL. The soft reset state is entered by setting bit RSTP in the VSC register. Setting NOSF when RSTP is set denotes the safe state. When in the safe state, the VX5530/VX5535 can only be restarted by another VXIbus device or by a full power-up reset. The RUN light will not be illuminated, the display will be blank, and the front panel reset switch will not be effective (the VXIbus register is grounding the reset line, so the panel reset switch has no effect) . When the VX5530/VX5535 is in a soft reset or safe state, the VXIbus registers are unchanged, as they have to be to enable a resource manager to reactivate the VX5530/VX5535. When the VX5530/VX5535 comes out of the safe state, a "hard" reset is generated and it completely reinitializes as it would on a power-up. The VXIbus registers (including the logical Address) are cleared to the reset state, and the VX5530/VX5535 is ready to be reconfigured by the dynamic address allocation scheme.

Three other conditions generate "hard" resets. One is the front panel reset button. Another is receipt of VXIbus SYSRESET (unless it is masked), and the third is expiration of the watchdog timer period, when the WDTR bit is set (meaning that one wants the watchdog timer to generate a reset rather than an interrupt).

The watchdog timer can be configured to either reset or interrupt the CPU when its timer period expires by the WDTR bit of the MSC register. The timer is reset whenever register MSC is read. The time period is controlled by the FWDT bit in the MSC.

Finally, there is a one more reset available to the DOS programmer. When the CNTL-ALT-DEL keys are depressed simultaneously, DOS reboots. This generates a software reset that does not modify the VXIbus registers, or the ULA. This type of reset is transparent to an external resource manager, which does not have to interact with or reconfigure the VX5530/VX5535.

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Memory Mapping and the VMEbus Window

The hardware memory mapping registers on the VX5530/VX5535 perform three functions:

1. In conjunction with the VXIbus control registers BWA and BWM, these mapping registers allow a fixed "DOS" 64K window at address 0E0000 to generate all possible VMEbus addresses.

2. Provides a means to copy, protect, and map multiple BIOS address areas into the 0-wait state DRAM BIOS area for better performance.

3. Provides 256KB of memory, addressable at a 1M offset from the board base address in the VXIbus A32 address space, that is completely isolated from the on-board DOS software. It can be accessed by DOS at its VXIbus address.

The following table shows how the different regions of the 386 address space are treated by the VX5530/VX5535 hardware. In addition, it shows the regions of the 386 address space that are translated to other addresses by the VX5530/VX5535's *mapping register* hardware. The DRAM designation below indicates that the 386 memory access goes to the on-board, 0 wait-state, 32-bit wide DRAM. The mapping registers incur no DRAM wait-state overhead when compared to non-mapped accesses. Note that memory reads to the BIOS areas are treated differently than memory writes.

Table A-4. VX5530/VX5535 memory map

386 address	trans?	usage/destination
00000000-0009FFFF	No	DRAM
000A0000-000BFFFF	No	VGA video RAM (via AT-bus)
000C0000-000CFFFF	No	DRAM (shadowed VGA BIOS)
000D0000-000DFFFF	No	AT bus
000E0000-000EFFFF	Yes	VMEbus window
READ 000F0000-000FFFFF	Yes	DRAM (shadowed BIOS)
WRITE 000F0000-000FFFFF	No	Ignored
00100000-0013FFFF	Yes	DRAM (Extended memory)
00140000-00FEFFFF	No	DRAM (Extended memory)
READ 00FF0000-00FFFFFF	Yes	DRAM (uses 000Fxxxx map reg's)
WRITE 00FF0000-00FFFFFF	No	Ignored
01000000-1FFFFFFF	No	DRAM
02000000-FEFFFFFF	No	VMEbus (A32 access only)
FF000000-FF7FFFFF	No	Regular of Flash EPROM
FF800000-FF8FFFFF	No	EPROM BIOS

To perform the required address translation, the VX5530/VX5535 uses 24 eight-bit wide mapping registers, addressable with normal input and output instructions at I/O addresses 8100-813x. Bits A15 and A9-A0 are decoded, and only the even addresses in this I/O range are used. Appendix C provides a full list of the register addresses.

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One of the 24 mapping registers is enabled on every access to addresses in the 000E0000-0013xxxx or 00FFxxxx regions. When an access to one of these regions occurs, bits A18 - 14 are decoded to select the mapping register which supplies the (translated) address bits A21 - A14.

A set of four memory mapping registers are provided for each of seven 64K byte regions, providing a 16KB mapping granularity. Two regions, 000Fxxxx and 00FFxxxx (the BIOS region on 8086 and 80286-based PC's), use the same mapping registers, so only 24 registers are needed.

Table A-5. Address bit generation

Access Type	Address bits (from BWA/M)	Address bits (mapping register)	Address bits (from 386)
On-board, direct	none	none	A31 - A00
On-board, translated region	none	A21 - A14	A13 - A00
VXIbus A16, through window	none	A15 - A14	A13 - A00
VXIbus A24, through window	A23 - 22	A21 - A14	A13 - A00
VXIbus A32, through window	A31 - 22	A21 - A14	A13 - A00
VXIbus A32, direct	none	none	A31 - A00

The VXIbus page frame is a special case of the mapping registers. As usual, the mapping registers provide address bits A21-14 (as needed). In this case, since addresses to the A24 or A32 VXIbus are being generated, registers BWA and BWM provides the upper 2 (for A24 accesses) or 10 (for A32 accesses) address bits.

The only mapping registers that are normally modified by the user are the VMEbus mapping registers (I/O addresses 8130,8132,8134, and 8136), and even this is done through operating system calls to the Bus Interface Manager. The rest of the registers should not be modified by the user for proper DOS operation. These other registers are used as follows when the VX5530/VX5535 is booted:

1. The EPROM-based BIOS is copied into DRAM address 000Fxxxx using the mapping registers associated with the 386 address 00100000 (base 16). The 386 address of 000Fxxxx can not be used to copy the BIOS into the DRAM since this address is write protected.

2. The mapping registers associated with 386 addresses 001000xx are then changed to translate these addresses to the 000Axxxx, 000Bxxxx, 000Dxxxx, and 000Exxxx DRAM addresses. The mapping registers associated with 386 address 000Fxxxx are changed to perform a "noop" translation to a DRAM address of 00Fxxxx. The remaining mapping registers are initialized and may subsequently be modified by the user. After this initialization process there is no way to write the BIOS area, except by changing an "extended" or VMEbus mapping register to point to the BIOS area in the DRAM.

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Using the VXIbus window

This section provides a pseudo code example that shows, at the debug level, how to use the VMEbus window hardware to access (arbitrarily) address 27000000 in the VMEbus A32 address space. All numbers are in hex unless otherwise noted. This code is presented as an example of how the hardware works; DOS users will typically use the Bus Interface Manager to perform these functions.

```
output 8150,27;      Setup BWA (VMEbus master address
                     generation) to point to VMEbus
                     address 27XXXXXX

output 8151,00;      Setup BWM to allow A32, non-
                     IACK, little endian access and
                     set VMEbus master address bits
                     A23,A22=0.

output 8145,9F;      Enable the VMEbus accesses to the
                     dual port.

output 8130,0;       Point VMEbus mapping registers bits
                     A21-to 2700XXXX

output 8132,1;       Note that these four mapping registers
output 8134,2;       could also point to non-contiguous
output 8136,3;       16K byte VMEbus regions.

mov ax,00E0000;      See below
```

The final instruction of the pseudo code above actually generates a VMEbus read access that accesses VMEbus address 27000000.

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RAM Memory

The VX5530/VX5535 uses page-mode DRAM on industry-standard SIMM modules. VX5530/VX5535's with a 16 MHz clock require parts with a 100ns (or faster) access time. Units with a 20 MHz clock require 80ns parts.

2MB systems use eight 265KB-by-9 SIMM modules. 4MB systems use four 1MB-by-9 modules plugged into the sockets labeled "low bank" on Figure A-3. 8MB systems use eight 1MB-by-9 modules, filling all 8 sockets.

A 5MB configuration, not available from the factory, is also supported. This configuration has four 1MB SIMMs in the "low bank" and four 256K SIMMs in the "high bank". The smaller parts must be in the low bank for this to operate.

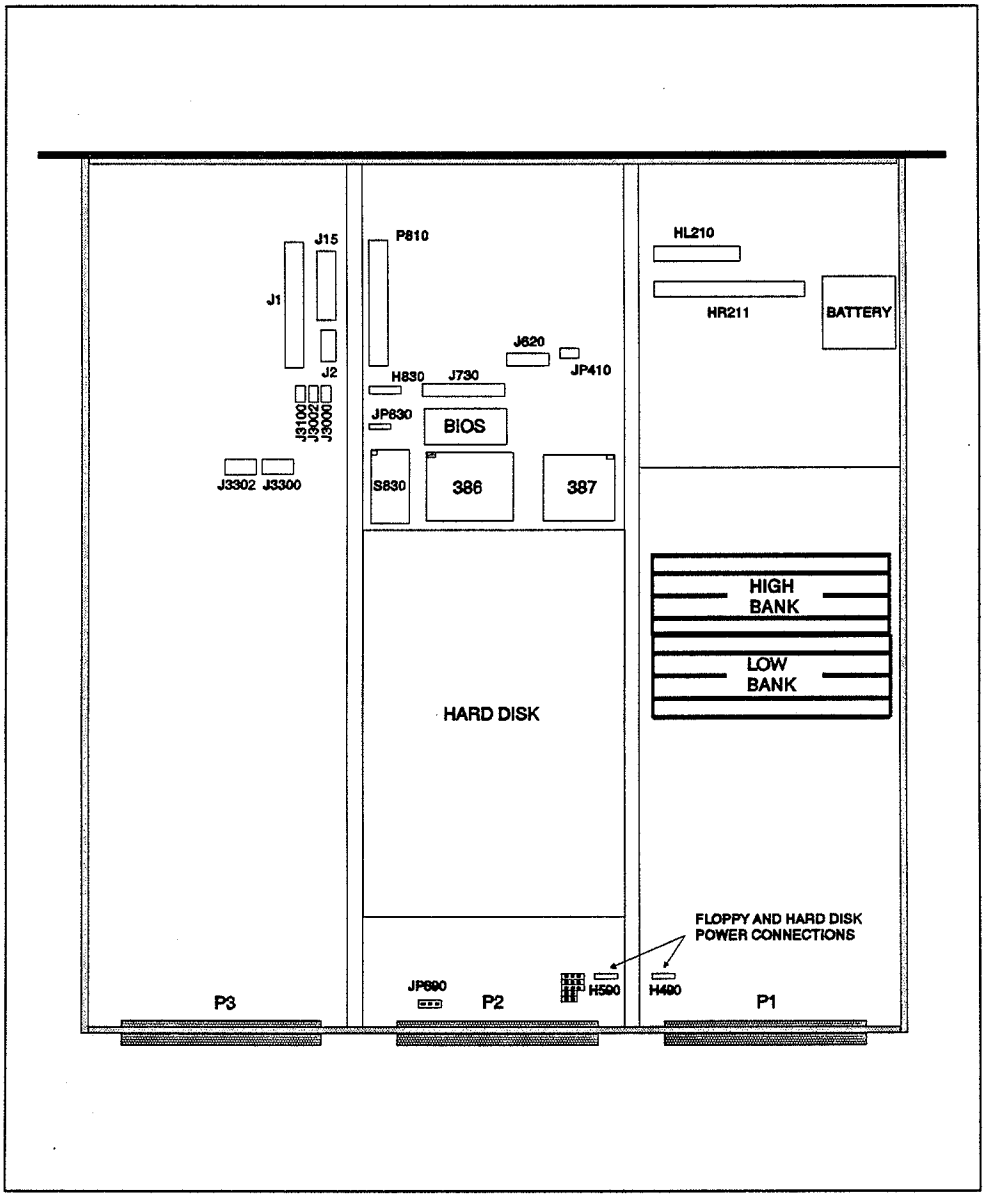


Figure A-3. Internal connector locations.

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VX5530/VX5535 Architecture (Advanced Trigger Functions)

This third part provides the details of the Advanced Trigger Functions.

The VX5530 ATF hardware is an ECB assembly which, when combined with an appropriate controller, provides high performance VXI P3 control. The ATF supports the VXI STARbus for slots 1-12, controls of the STST, ESTST and SYNC100 protocols, trigger routing and control. It provides the required CLK10 and CLK100 signals with the ability to synchronize these system clocks with an external 10 MHz reference.

The ATF hardware is controlled via an 8 bit microprocessor interface cable. Control of the ATF hardware is presented as an array of registers. Software which controls the ATF hardware resides on the mating mother board. Additional connections are made to the mother board to provide ECL signals on the high speed connector. These signals control the TTLTRIG and ECLTRIG interfaces.

The ATF hardware block diagram is shown in Figure A-4. Four front panel BNC's support user level I/O. Internally function units utlilize, modify or route trigger signals. An 8 channel Instrument Trigger Bus (ITB) provides connections between the internal functions. ITB channels can have only one active driver but may have

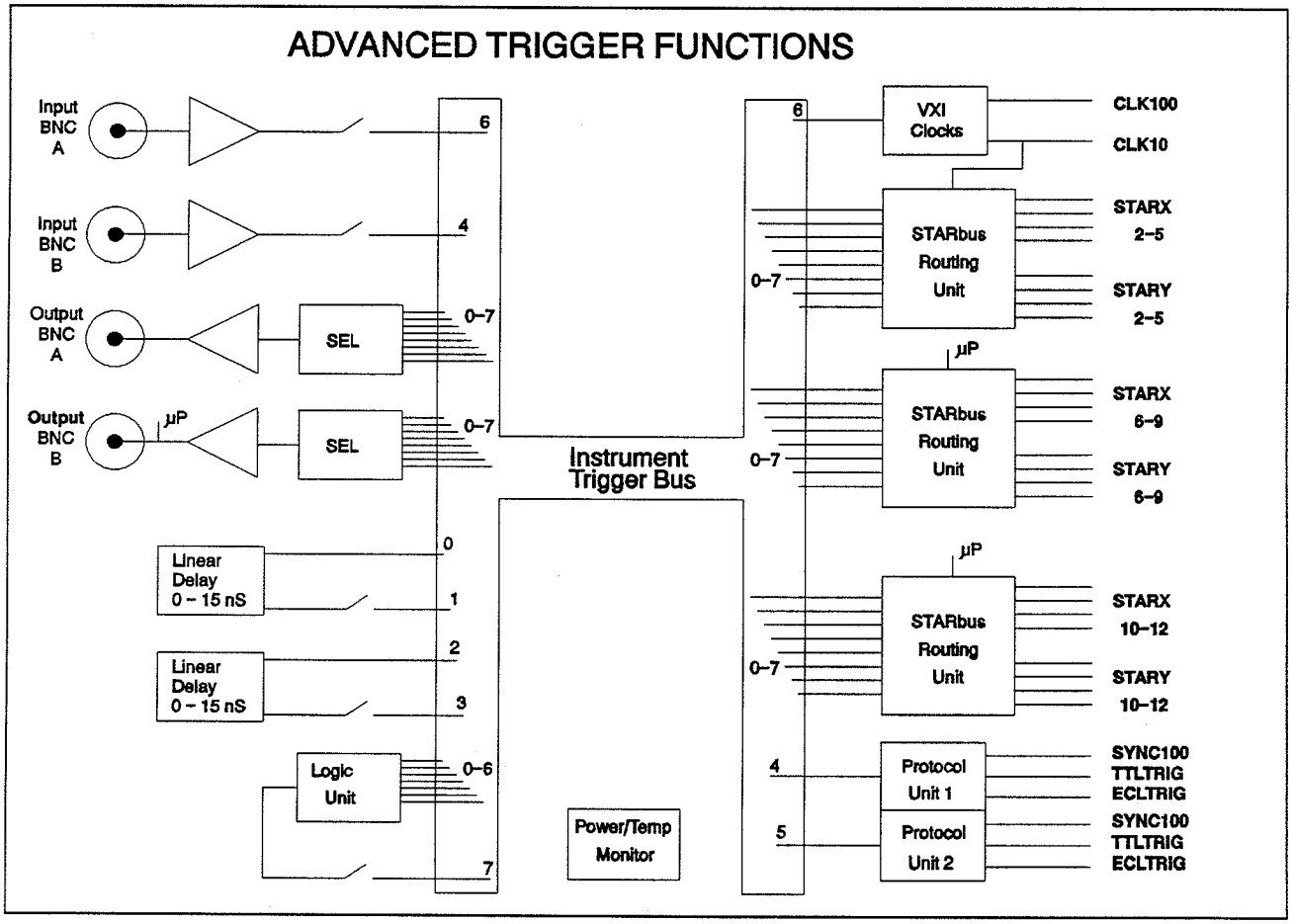


Figure A-4. ATF hardware block diagram.

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multiple receivers. Functional units and routing channels are configured under program control. These functions provide real time control of VXI triggers.

Input BNC's A and B bring user supplied triggers into the ATF system. The inputs are high impedance and have TTL threshold levels. The buffered signal is driven onto an ITB by enabeling its driver. Output BNC's A and B can selectively output any of the ITB channels. The output polarity is selectable and is capable of driving TTL levels into a 50 Ohm load.

The two Linear Delay units provide programmable delays from 0-15 nS. The delayed signal is driven onto an ITB channel by enabling the delay units output. Delay is selected in 1 nS increments.

The Logic Unit (Fig. A-5) logically combines ITB (0-6) signals into a single output. It can perform the logical functions OR, AND, NOR, NAND, and INVERTOR. Input signals are wire ORed together and may be programmed to be level or edge sensitive. Signal input and output polarity are selectable. The output of the Logic Unit is driven onto an ITB channel by enabling its output.

The Clock unit generates the VXI CLK10 and CLK100 instrument clocks. It can use either an internal reference or a reference supplied from an ITB channel. CLK10 can be driven onto an ITB channel via one of the STARbus routing units. This allows one mainframe to export its reference clock and a second mainframe to import the reference providing synchronous operation.

Each STARbus routing unit is a 16 point cross matrix switch. Eight of the I/O channels are connected to the ITB channels and provide general purpose routing. The second eight I/O channels are connected to the STARX and STARY channels for four VXI slots. Three routing units provide support for a full 13 slot VXI mainframe. An additional 17th input is provided. This input supports the export of CLK10 on STARbus routing unit 0 and supplies two microprocessor input channels on STARbus routing units 1 and 2. The routing of the STARbus routing unit is programmably controlled.

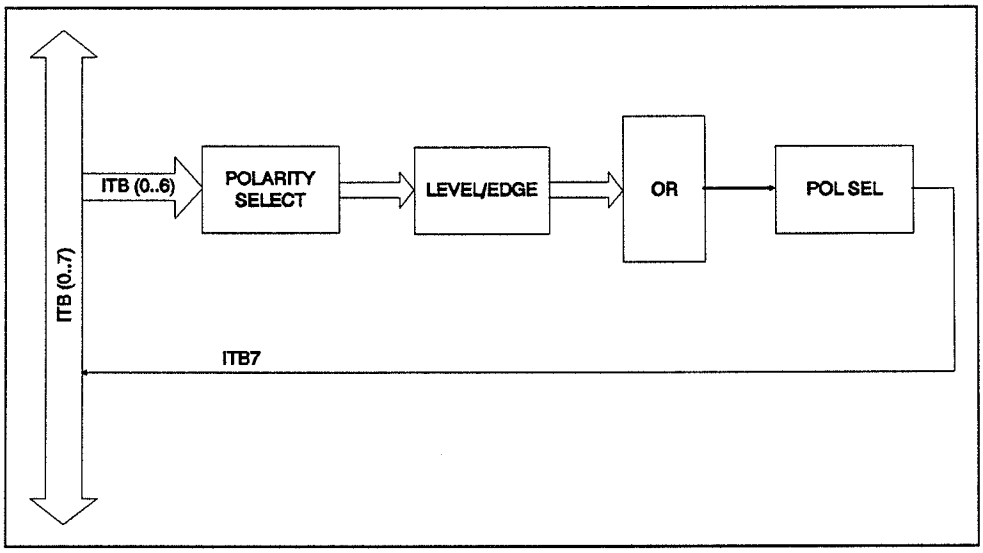


Figure A-5. Logic unit.

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The ATF hardware supplies two independent STST, ESTST, and SYNC100 protocol controllers (Fig. A-6). These two units allow two independent instrument clusters to exist in the system. The purpose of the protocol is to synchronously start and stop groups of modules. Modules in an instrument cluster start and stop coherently. Each unit requires a unique selection of a VXIbus TTLTRG and ECLTRG line. It can be controlled by the microprocessor or by an ITB channel. Note that STST and ESTST protocols are VXIbus communication protocols, but SYNC100 which does not contain a TTLTRG line is a Tektronix defined protocol.

The Power and Temperature monitor supports system health feedback. All power supplies and the board temperature in the VX5530 are monitored. An 8 bit A-D convertor supports the measurement and sets the fundamental accuracy of the measurement.

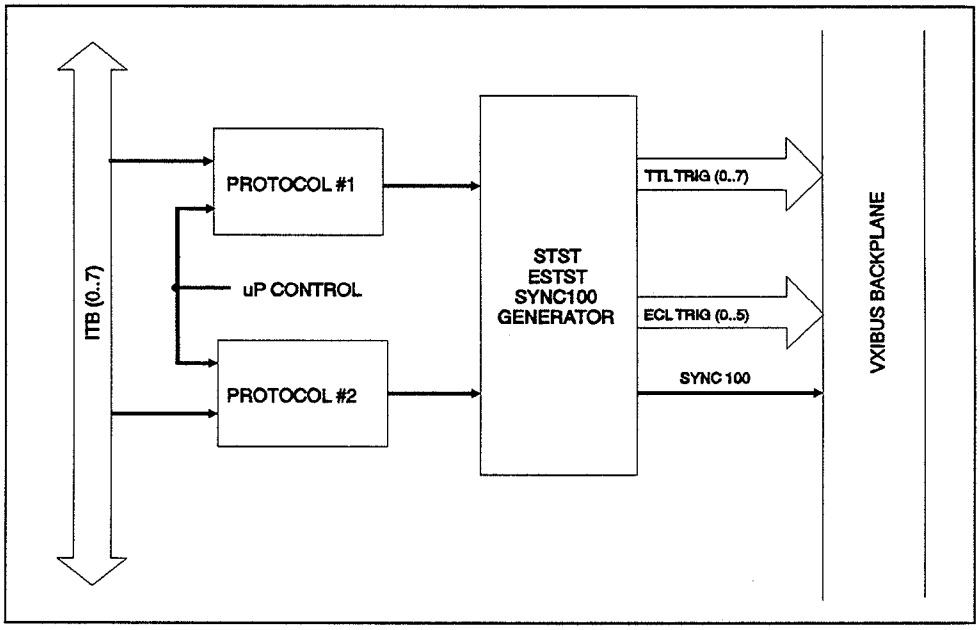


Figure A-6. Protocol unit.

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Appendix B
Bill Of Material Control

To ensure that our customers receive a correct, uncorrupted product, TekVICS software is shipped with a machine-readable bill of materials which describes every file that makes up TekVICS. This description includes the full file name, its size, checksum, modification time, and attributes.

This descriptions are kept in the file **\vXYY.bom**, where *X* is the major version number, and *YY* is the minor version number. For example, release 2.05 would contain the bill of material in the file **\v205.bom**.

Checking the Bill of Material

Bill of material files are created and managed by the program ckbom, which is included in TekVICS. If you suspect that TekVICS files may have been deleted or corrupted, you can run **ckbom** to verify that your files are correct. For example, to check the contents of the hard drive against the distributed version of TekVICS release 2.05, execute the following command in the root ("\") directory:

```
ckbom /b=v205
```

This will report any changes from the distribution, but some changes are to be expected. For instance, you may have personalized **autoexec.bat** or **config.sys** so that they no longer match the distribution but are correct for you.

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Ckbom Parameters

The syntax of the ckbom command is:

```
ckbom [<options>]<directory>
```

for most commands, or

```
ckbom [<options>]/c<src_directory><dest_directory>
```

when copying files. The <options> can be:

/b=<file>	Specify up to four BOM databases. Defaults to standard input. If no file extension is provided and "" does not exist, ckbom tries to use ".bom".
/c	Copy files mentioned in the BOM database from src to dest directories.
/f	Fix file attributes and modification times on files.
/g	Treat all files under <directory> (or <src_directory>, if the /c flag is used) as being in the database. Used in place of /b= when creating initial database.
/n=<file>	Create new database file. If no file name extension is specified, ".bom" is used.
/s	Speed checking—skip checking CRCs on the disk. Note that the CRC of the file is always checked when copying a file.
/v	Verbosity ON. The name of every file is listed as it is processed.
/?	To get help.

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BOM database file is a text file with one line per file to be checked. Within each line fields are separated by whitespace (a string of blanks and/or tabs). The fields are, in order:

```
<file name><size><crc><last mod time><attributes>
```

Where:

`<file name>`	The pathname of the file, relative to the root of the directory tree.Typically, the root of the directory tree is the top-level directory, "\".
`<size>`	Decimal file size in bytes
`<crc>`	CRC16 of the file in hexadecimal
`<last mod time>`	Last file modification date and time: <month>-<day>-<year>;<hour>:<minute>:<second>
`<attributes>`	DOS file attributes, in the string "drwhsm", where d: directory r: readable w: writable, h: hidden s: system m: modified Missing attributes are marked by a "-". The minimal permission ("-r----") always allows reading

Comments are anything from "#" to the end of line. Blank lines are ignored.

Fields containing just a question mark ("?") or that are omitted at the end of line are considered empty. The file information associated with empty fields is not checked. Directories contain empty fields for file size, CRC, and modification date.

Here is a fragment of a BOM database file:

```
INSTALL.BAT    1398   d47a   03-10-89;16:41:46          -rw
CONFIG.SYS     126    087d   03-10-89;16:21:14          -rw
AUTOEXEC.BAT   145    bf90   08-14-88;06:58:02          -rw
TEKVICS        ?      ?      ?                          drw
TEKVICS\BUSMON.EXE   5664   f1e8   08-12-88;10:52:56    -rw
TEKVICS\BUSPROBE.EXE0272   ea7f   03-01-89;21:33:02    -rw
TEKVICS\AXPIMSG.EXE1541    25e0   08-10-88;11:49:06    -rw
TEKVICS\CONFIG.EXE 129855 5226    11-13-88;09:21:42    -rw
```


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Ckbom Examples

To quickly check the contents of the distribution floppy without reading every file, type

```
ckbom /s /b=a:\v205 A:\
```

The /s option causes the CRC checking to be skipped. This saves a lot of time (especially with floppies) but also means that some file corruption may go undetected.

If you want to build your own bill of material database (e.g., for your own value added software), there are two ways of doing it. The first method is to explicitly list all the files you want in the distribution, one per line, and use ckbom to create a full database file. (Create "**filelist.tmp**" in your favorite text editor)

```
ckbom /b=filelist.tmp /n=myfiles
```

This would cause a new database **myfiles.bom** to be created listing only the files you want, and with all the appropriate fields filled in. Ckbom searches for these files starting at the current directory. If the files are instead in directory distrib, then type:

```
ckbom /b=filelist.tmp /n=myfiles distrib
```

The second way of building a BOM database is to put all the files that you want to distribute in a directory and use the /g option:

```
ckbom /g /n=myfiles distrib
```

This is much easier when dealing with a large number of files.

To copy files mentioned in the database from one place to another, type

```
ckbom /c /b=myfiles oneplace another
```

Every file is checked before copying and CRC'ed as it is copied. Directories are created *if they are mentioned in the database*. After each file is copied, it is again CRC'ed to make sure it was correctly copies, and its file attributes and modification times are set to those in the database. Mentioning /s causes the CRC'ing of the destination file to be skipped, which halves the timer required to copy (but each file is still CRC'ed as it's copied).

Finally, ckbom can correct minor problems with files such as incorrect attributes or mod times. Running

```
ckbom /f /b=myfiles distrib
```

will instruct ckbom to change modification times and attributes on the files to match the database.

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Appendix C
Interrupt and I/O Port Addresses

This appendix lists all the Interrupts and I/O port addresses used by the VX5530/VX5535. Refer to any of the generic PC/AT programmers guides, and to the Chips and Technologies hardware manuals for operational details of the standard-architecture components.

In the I/O address table, values are listed for registers that can be read (with debug) and have "normal" values. Registers with values indicated as * are active, and will have values determined by the ongoing operations. Many registers have substantial side effects when read. Most have effects when written.

Standard PC I/O addresses use only 10-bit address decoding, so the highest address available is 3FF. Bits 15-10 are ignored. All VX5530/VX5535 specific registers decode A15 as well as A9-A0. For simplicity they are listed at only their primary address, 8xxx, and not at all their aliases.

Table C-1 Interrupt Signals

Signal Name	Description
IRQ1	Keyboard
IRQ2	Does not exist
IRQ3	Com port 2, also available on test connector
IRQ4	Com port 1
IRQ5	IEEE-488 port
IRQ6	Floppy disk controller
IRQ7	Parallel printer port
IRQ8	Clock
IRQ9	VGA controller
IRQ10	VMEbus and VXIbus interrupts (through gate array)
IRQ11	
IRQ12	Not used, available on test connector
IRQ13	Coprocessor (387)
IRQ14	SCSI controller
IRQ15	

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Table C-2 I/O Addresses

Address	Register Function	Used By/Initialized To
	First (8-bit) DMA Controller: C&T chip emulating 8237 of PC/AT	
x000	DMA 1 Chan 0 addr	RESERVED
x001	DMA 1 Chan 0 count	
x002	DMA 1 Chan 1 addr	IEEE-488 Port
x003	DMA 1 Chan 1 count	
x004	DMA 1 Chan 2 addr	FLOPPY DISK
x005	DMA 1 Chan 2 count	
x006	DMA 1 Chan 3 addr	SCSI DISK
x007	DMA 1 Chan 3 count	
x008	DMA 1 Status	
x009	DMA 1 DMA requestor	
x00A	DMA 1 Command	
x00B	DMA 1 Mode	
x00C	DMA 1 Byte pointer FF	
x00D	DMA 1 Master Clear	
x00E	DMA 1 Clear mode	
x00F	DMA 1 Request mask	
	First Interrupt Controller: C&T 82C301/304 emulating 8259 of PC/AT	
x020	I/O Control Word 1	
x021	I/O Control Word 2-4	
x022	82C301/304 Config	
x023	82C301/304 Config	
	Counter-Timer Functions: C&T 82C206 emulating 8254 of PC/AT	
x040	Counter 0	TOD CLOCK
x041	Counter 1	RAM REFRESH
x042	Counter 2	SPEAKER
x043	Counter control	
	Keyboard Port: C&T 82C301/304 and 8742, as on PC/AT	
x060	8042 Port A/Data	
x061	Port B (82C301/304)	MISC CONTROL
x062		
x063		
x064	8042 Status/Command	
	Time-of-Day Clock/NVRAM: C&T 82C206 emulating MC6818 of PC/AT	
x070	Bit 7 = NMI, 0..6 RTC address	
x071	RT clock or NOVRAM data	

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Table C-2 I/O Addresses (Cont)

Address	Register Function	Used By/Initialized To
	DMA Page Registers: C&T 82C206 emulating 74LS612 of PC/AT	
x080	Manufacturing port	
x081	8-bit DMA chan 2 page reg	
x082	8-bit DMA chan 3 page reg	
x083	8-bit DMA chan 1 page reg	
x084		
x085		
x086		
x087	8-bit DMA chan 0 page reg	
x088		
x089	16-bit DMA chan 2 page reg	
x08A	16-bit DMA chan 3 page reg	
x08B	16-bit DMA chan 1 page reg	
x08C		
x08D		
x08E		
x08F	Refresh cycle page reg	
	Second Interrupt Controller: C&T 82C206 emulating 8259 of PC/AT	
x0A0	I/OCW1	*
x0A1	I/OCW2-4	*
	Second (16-Bit) DMA Controller: C&T 82C206 emulating 8237 of PC/AT	
x0C0	DMA 2 Chan 0 addr	RESERVED
x0C1		
x0C2	DMA 2 Chan 0 count	*
x0C3		
x0C4	DMA 2 Chan 1 addr	RESERVED
x0C5		
x0C6	DMA 2 Chan 1 count	*
x0C7		
x0C8	DMA 2 Chan 2 addr	RESERVED
x0C9		
x0CA	DMA 2 Chan 2 count	*
x0CB		
x0CC	DMA 2 Chan 3 addr	RESERVED
x0CD		
x0CE	DMA 2 Chan 3 count	*
x0CF		

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Table C-2 I/O Addresses (Cont)

Address	Register Function	Used By/Initialized To
x0D0	DMA 2 Status	*
x0D1		
x0D2	DMA 2 DMA requestor	*
x0D3		
x0D4	DMA 2 Cmd	
x0D5		
x0D6	DMA 2 Mode	
x0D7		
x0D8	DMA 2 Byte ptr FF	
x0D9		
x0DA	DMA 2 Master Clear	
x0DB		
x0DC	DMA 2 Clear mode	
x0DD		
x0DE	DMA 2 request mask	
x0DF		
	Coprocessor Interface:	
	On VX5530/VX5535, a 80387 replaces the 80287 of PC/AT	
x0F0	Clear 387 busy	Clear 287 busy
x0F1	Reset 387	Reset 287
	SCSI Interface:	
	Logical Devices 53c80, NCR 5830 Compatible	
	See discussion in Section 3	
x2B0	SCSI data register	
x2B1	SCSI initiator register	
x2B2	SCSI mode	
x2B3	SCSI target command	
x2B4	SCSI ID selection	
x2B5	SCSI DMA start/status	
x2B6	SCSI	
x2B7	SCSI reset/start	
	IEEE-488 Interface:	
	NEC uPD7210, emulates National Instruments GPIB-PC2A	
	See discussion in Section 3	
x2B8	IEEE-488 data register in/out	
x2B9	IEEE-488 interrupt 1 status/mask	
x2BA	IEEE-488 interrupt 2 status/mask	
x2BB	IEEE-488 serial poll status/mode	
x2BC	IEEE-488 address status/mode	
x2BD	IEEE-488 cmd passthrough/aux mode	
x2BE	IEEE-488 address 0/addr flag	

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Table C-2 I/O Addresses (Cont)

Address	Register Function	Used By/Initialized To
x2BF	IEEE-488 address 1/EOS flag	
	Serial I/O (COM2) Port: C&T 82C606 emulating 8251 of PC/AT	
x2F8	RCV/Xmit buf	
x2F9	Intr enable	
x2FA	82C606 config/intr flags	
x2FB	Byte format	
x2FC	Modem ctrl	
x2FD	Line status	
x2FE	Modem status	
x2FF	Scratchpad	
	Parallel I/O (Printer) Port: C&T 82C606 emulating 8255 of PC/AT	
x378	Parallel data	
x379	Parallel status	
x37A	Parallel control	
	Monochrome Video Adapter Port: Paradise PVGA1A emulating monochrome adapter	
x3B0		
x3B1		
x3B2		
x3B3		
x3B4	CRTC index register	
x3B5	CRTC data register	
x3B6		
x3B7		
x3B8	Mode control register	
x3B9	Preset light pen latch	
x3BA	Feature control/input status 1	
x3BB	Clear light pen latch	
x3BF	Hercules register	
	EGA Video Controller Port: Paradise PVGA1A emulating EGA adapter	
x3C0	Index register/attribute register	
x3C1	Attribute register	
x3C2	EGA mis out/input status 0	
x3C3	Video system enable register	
x3C4	Sequencer index register	
x3C5	Sequencer data register	
x3C6		
x3C7		

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Table C-2 I/O Addresses (Cont)

Address	Register Function	Used By/Initialized To
x3C8		
x3C9		
x3CA	Read graphics B position	
x3CB		
x3CC	Read graphics A position	
x3CD		
x3CE	Graphics index register	
x3CF	"Other" graphics register	
	CGA I/O Ports: Paradise PVGA1A emulating CGA adapter	
x3D0		
x3D1		
x3D2		
x3D3		
x3D4	CRTC index	
x3D5	CRTC register	
x3D6		
x3D7		
x3D8		
x3D9	Color select register	
x3DA	EGA feature ctrl & input stat 1/CGA stat	
x3DB	EGA/CGA clear light pen latch	
x3DC	EGA/CGA set light pen latch	
x3DE	AT&T/M24 compatibility register	
	Floppy Disk Port: WD37C65A, emulates NEC765 of PC/AT	
x3F0		RESERVED
x3F1		RESERVED
x3F2	Operations register	
x3F3		RESERVED
x3F4	Command register	
x3F5	Data register	
x3F6		RESERVED
x3F7	Control register	
	Serial Port 1: C&T 82C606 emulating 8552 of PC/AT	
x3F8	RCV/Xmit buf	
x3F9	Intr enable	
x3FA	82C606 config/intr flags	
x3FB	Byte format	

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Table C-2 I/O Addresses (Cont)

Address	Register Function	Used By/Initialized To
x3FC	Modem ctrl	
x3FD	Line status	
x3FE	Modem status	
x3FF	Scratchpad	
	Memory Mapping Registers: No PC/AT equivalent: see Appendix A for discussion Address bits 15 and 10-0 are decoded, others are "don't care" Read as: EPS 386 address 00100000 maps to physical memory at A0000	
8100	EMS 00100xxx map reg	Maps to A0xxx/28
8102	EMS 00104xxx map reg	Maps to A4xxx/29
8104	EMS 00108xxx map reg	Maps to A8xxx/2A
8106	EMS 0010Cxxx map reg	Maps to ACxxx/2B
8108	EMS 00110xxx map reg	Maps to B0xxx/2C
810A	EMS 00114xxx map reg	Maps to B4xxx/2D
810C	EMS 00118xxx map reg	Maps to B8xxx/2E
810E	EMS 0011Cxxx map reg	Maps to BCxxx/2F
8110	EMS 00120xxx map reg	Maps to D0xxx/34
8112	EMS 00124xxx map reg	Maps to D4xxx/35
8114	EMS 00128xxx map reg	Maps to D8xxx/36
8116	EMS 0012Cxxx map reg	Maps to DCxxx/37
8118	EMS 00130xxx map reg	Maps to E0xxx/38
811A	EMS 00134xxx map reg	Maps to E4xxx/39
811C	EMS 00138xxx map reg	Maps to E8xxx/3A
811E	EMS 0013Cxxx map reg	Maps to ECxxx/3B
8120	Unused, behaves as RAM	
8122	Unused, behaves as RAM	
8124	Unused, behaves as RAM	
8126	Unused, behaves as RAM	
8128	Unused, behaves as RAM	
812A	Unused, behaves as RAM	
812C	Unused, behaves as RAM	
812E	Unused, behaves as RAM	
8130	EMS 000E0xxx map reg	Maps to VMEbus/*
8132	EMS 000E4xxx map reg	Maps to VMEbus/*
8134	EMS 000E8xxx map reg	Maps to VMEbus/*
8136	EMS 000ECxxx map reg	Maps to VMEbus/*
8138	EMS 000F0xxx & 00FF0xxx map reg	Maps to F0xxx/3C
813A	EMS 000F4xxx & 00FF4xxx map reg	Maps to F4xxx/3D
813C	EMS 000F8xxx & 00FF8xxx map reg	Maps to F8xxx/3E
813E	EMS 000FCxxx & 00FFCxxx map reg	Maps to FCxxx/3F

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Table C-2 I/O Addresses (Cont)

Address	Register Function	Used By/Initialized To
	VXIbus Registers: Implemented in VX5530/VX5535 gate array: No PC/AT equivalent See Appendix A for discussion	
8140	Low byte VXIbus ID reg	
8141	High byte VXIbus ID reg	
8142	Low byte VXIbus device type reg	
8143	High byte VXIbus device type reg	
8144	Low byte VXIbus status/control reg	
8145	High byte VXIbus status/control reg	
8146	Low byte VXIbus slave offset reg	
8147	High byte VXIbus slave offset reg	
8148	Low byte VXIbus protocol reg	
8149	High byte VXIbus protocol reg	
814A	Low byte VXIbus response reg	
814B	High byte VXIbus response reg	
814C	Low byte VXIbus message low reg	
814D	High byte VXIbus message low reg	
814E	Low byte VXIbus message high reg	
814F	High byte VXIbus message high reg	
	VMEbus Control Registers: Implemented in gate array: No PC/AT equivalent See Appendix A for discussion	
8150	VMEbus window address reg	
8151	VMEbus window mofifier reg	
8152	VMEbus interrupt state reg	
8153	VMEbus interrupt enable reg	
8154	VMEbus event state reg	
8155	VMEbus event enable reg	
8156	VMEbusTTL trigger sample reg	
8157	Reserved	
8158	VXIbus MODID/Interrupter reg	
8159	VXIbus MODID upper reg	
815A	VXIbus TTL trigger drive reg	
815B	VXIbus ECL trigger sample/drive reg	
815C	VXIbus device unique logical address	
815D	VXIbus module status/control reg	
815E	VXIbus signal reg FIFO (lower)	
815F	VXIbus signal reg FIFO (upper)	
8160... 82AF	**Reserved for future use**	

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Appendix D
VXIbus Glossary

The following glossary list contains terms that are defined according to use in the VXIbus System. Although some of these terms may be used in other systems with different meanings, it is important to apply these listed definitions for purposes of VXIbus applications. In any instance in which a term is applicable only to a particular instrument module, that fact is so noted.

Term	Definition
ACCESSED Indicator	An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.
ACFAIL*	A VMEbus backplane line that is asserted under two conditions: by the Mainframe Power Supply when power failure has occurred (either ac line source or power supply malfunction), or by the Resource Manager if it is necessary to disable the Power Supply.
A-Size Card	A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.
Asynchronous Communication	Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.
Backplane	The printed circuit board that is mounted in a VXIbus Mainframe to provide the interface between VXIbus modules and between those modules and the external system.
B-Size Card	A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.
Bus Arbitration	In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.
Bus Timer	A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.

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Client — In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10 — A 10-MHz, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1 through 12 on P2. It is distributed to each module slot as a single source, single destination signal.

CLK100 — A 100-MHz, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1 through 12 on P3. It is distributed to each module slot as a single source, single destination signal with a maximum system timing skew of 2 microseconds.

Commander — In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command — A directive to a device. There are three type of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers — In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers — A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card — A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

Custom Device — A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

Data Transfer Bus — One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

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DC SUPPLIES Indicator — A red LED indicator that illuminates when a DC power fault is detected on the backplane.

Device Specific Protocol — A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card — A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 by 14.4 in by 1.2 in).

DTB — See Data Transfer Bus.

DTB Arbiter — A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT — Device Under Test.

ECLTRG — Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.

Embedded Address — An address in a communications protocol in which the destination of the message is included in the message.

ESTST — Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Self Test — Any self test or diagnostic power-up routine that executes after the initial kernel self-test program.

External System Controller — The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator — A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

HI TEMP Indicator — A VX5520 Slot 0 Controller (only) LED indicator that lights to signify an excessive temperature condition on the module.

IACK Daisy Chain Driver — The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

ID-ROM — An NVRAM storage area that provides for non-volatile storage of diagnostic data.

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Instrument Module	A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.
Interface Device	A VXIbus device that provides one or more interfaces to external equipment.
Interrupt Handler	A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.
Interrupter	A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.
IRQ	The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.
Local Bus	A daisy-chained bus that connects adjacent VXIbus slots.
Local Controller	The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus Mainframe or several Mainframes. See Resource Manager.
Local Processor	The processor on an instrument module.
Logical Address	The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.
Mainframe	In the instance of the Tektronix VX1500 Mainframe, an operable housing that includes 13 D-size VXIbus instrument module slots.
Memory Device	A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).
Message	A series of data bytes that are treated as asingle communication, with a well defined terminator and message body.
Message Based Device	A VXIbus device that supports VXIbus configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.
MODID Lines	Module/system identity lines.
Physical Address	The address assigned to a backplane slot during an access.

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Power Monitor — A device that monitors backplane power and reports fault conditions.

P1 — The top-most backplane connector for a given module slot in a vertical Mainframe such as the Tektronix VX1500. The left-most backplane connector for a given slot in a horizontal Mainframe.

P2 — The middle backplane connector for a given slot in a D-size Mainframe. The bottom backplane connector for a given slot in a C-size Mainframe.

P3 — The bottom backplane connector for a given module slot in a vertical D-size Mainframe such as the Tektronix VX1500. The right-most backplane connector for a given slot in a horizontal D-size Mainframe.

Query — A form of command that allows for inquiry to obtain status or data.

READY Indicator — A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-volt power will extinguish this indicator.

Register Based Device — A VXIbus device that supports VXIbus register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.

Requester — A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.

Resource Manager — A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self-test diagnostics, and initializing system commanders.

Self Calibration — A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.

Self Test — A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self-test routine is performed upon power-up.

Servant — A VXIbus message-based device that is controlled by a commander.

Server — A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.

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Shared Memory Protocol — A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

Slot 0 Controller — See Slot 0 Module. Also see Resource Manager.

Slot 0 Module — A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.

SMP — See Shared Memory Protocol.

STARX — A bidirectional, differential ECL line that provides for inter-module asynchronous communication. One line connects slot 0 and each of slots 1 through 12 in a Mainframe.

STARY — Two bidirectional, differential ECL lines that provide for inter-module asynchronous communication. One set of lines connects slot 0 and each of slots 1 through 12 in a Mainframe.

STST — STart/STop protocol; used to synchronize modules.

SYNC100 — A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100.

Synchronous Communications — A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL* — A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

System Clock Driver — A functional module that provides a 16-MHz timing signal on the Utility Bus.

System Hierarchy — The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

Test Monitor — An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

Test Program — A program, executed on the system controller, that controls the execution of tests within the test system.

Test System — A collection of hardware and software modules that operate in concert to test a target DUT.

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TTLTRG	Open collector TTL lines used for inter-module timing and communication.
VXIbus Subsystem	One Mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.
Word Serial Protocol	A VXIbus word oriented, bidirectional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).
Word Serial Communications	Inter-device communications using the Word Serial Protocol.
WSP	See Word Serial Protocol.
10-MHz Clock	See CLK10.
100-MHz Clock	See CLK100.
488-To-VXIbus Interface	A message based device that provides for communication between the IEEE 488 bus and VXIbus instrument modules.

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Appendix E
ASCII/GPIB Code Chart

B7 B6 B5 / BITS / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0	20 DLE 16	40 SP 32 0	60 0 48	100 @ 64	120 P 80	140 ` 96	160 p 112
0 0 0 1	1 GTL SOH 1	21 LLO DC1 17	41 ! 33	61 1 49	101 A 65	121 Q 81	141 a 97	161 q 113
0 0 1 0	2 STX 2	22 DC2 18	42 " 34	62 2 50	102 B 66	122 R 82	142 b 98	162 r 114
0 0 1 1	3 ETX 3	23 DC3 19	43 # 35	63 3 51	103 C 67	123 S 83	143 c 99	163 s 115
0 1 0 0	4 SDC EOT 4	24 DCL DC4 20	44 $ 36	64 4 52	104 D 68	124 T 84	144 d 100	164 t 116
0 1 0 1	5 PPC ENQ 5	25 PPU NAK 21	45 % 37	65 5 53	105 E 69	125 U 85	145 e 101	165 u 117
0 1 1 0	6 ACK 6	26 SYN 22	46 & 38	66 6 54	106 F 70	126 V 86	146 f 102	166 v 118
0 1 1 1	7 BEL 7	27 ETB 23	47 ' 39	67 7 55	107 G 71	127 W 87	147 g 103	167 w 119
1 0 0 0	10 GET BS 8	30 SPE CAN 24	50 (40	70 8 56	110 H 72	130 X 88	150 h 104	170 x 120
1 0 0 1	11 TCT HT 9	31 SPD EM 25	51) 41	71 9 57	111 I 73	131 Y 89	151 i 105	171 y 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 42	72 : 58	112 J 74	132 Z 90	152 j 106	172 z 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 43	73 ; 59	113 K 75	133 [91	153 k 107	173 { 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 44	74 < 60	114 L 76	134 \ 92	154 l 108	174 | 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 45	75 = 61	115 M 77	135] 93	155 m 109	175 } 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 46	76 > 62	116 N 78	136 ^ 94	156 n 110	176 ~ 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 47	77 UNL ? 63	117 O 79	137 UNT 95	157 o 111	177 DEL (RUBOUT) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS (PPE)	(PPD)

KEY

octal	25 PPU	GPIB code
	NAK	ASCII character
hex	15 21	decimal

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REF: ANSI STD X3. 4-1977
IEEE STD 488-1978
ISO STD 646-1973

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