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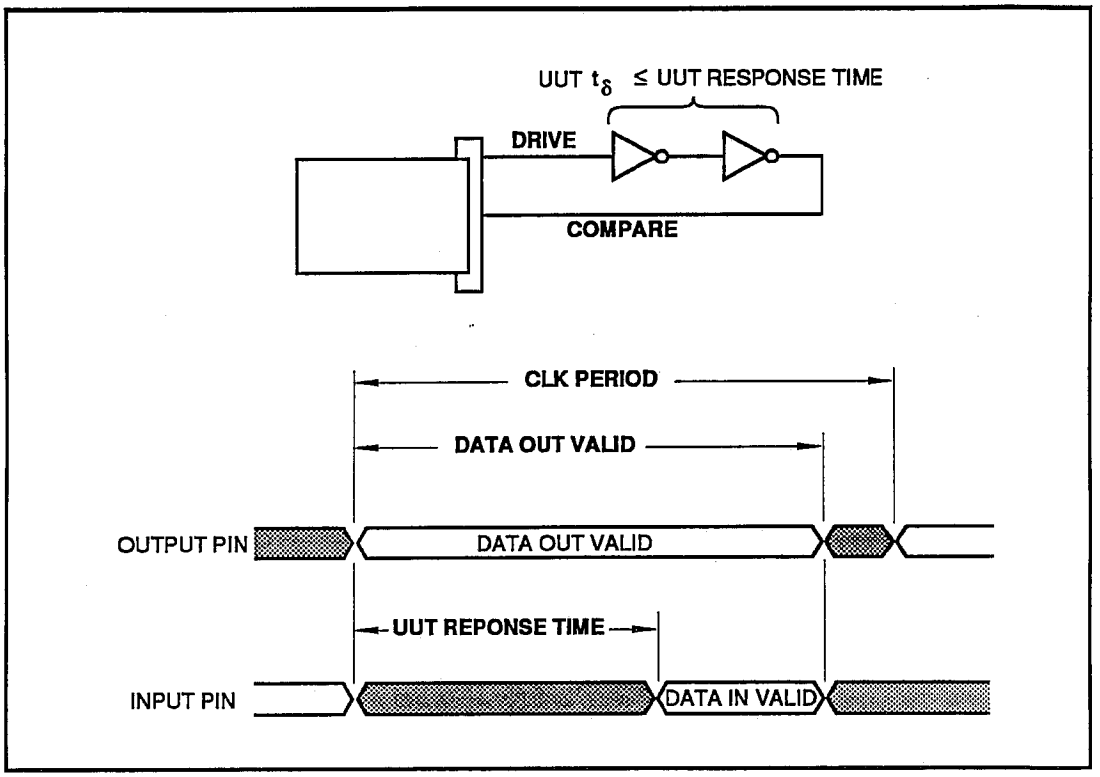


Figure 1. UUT Response Time Specification

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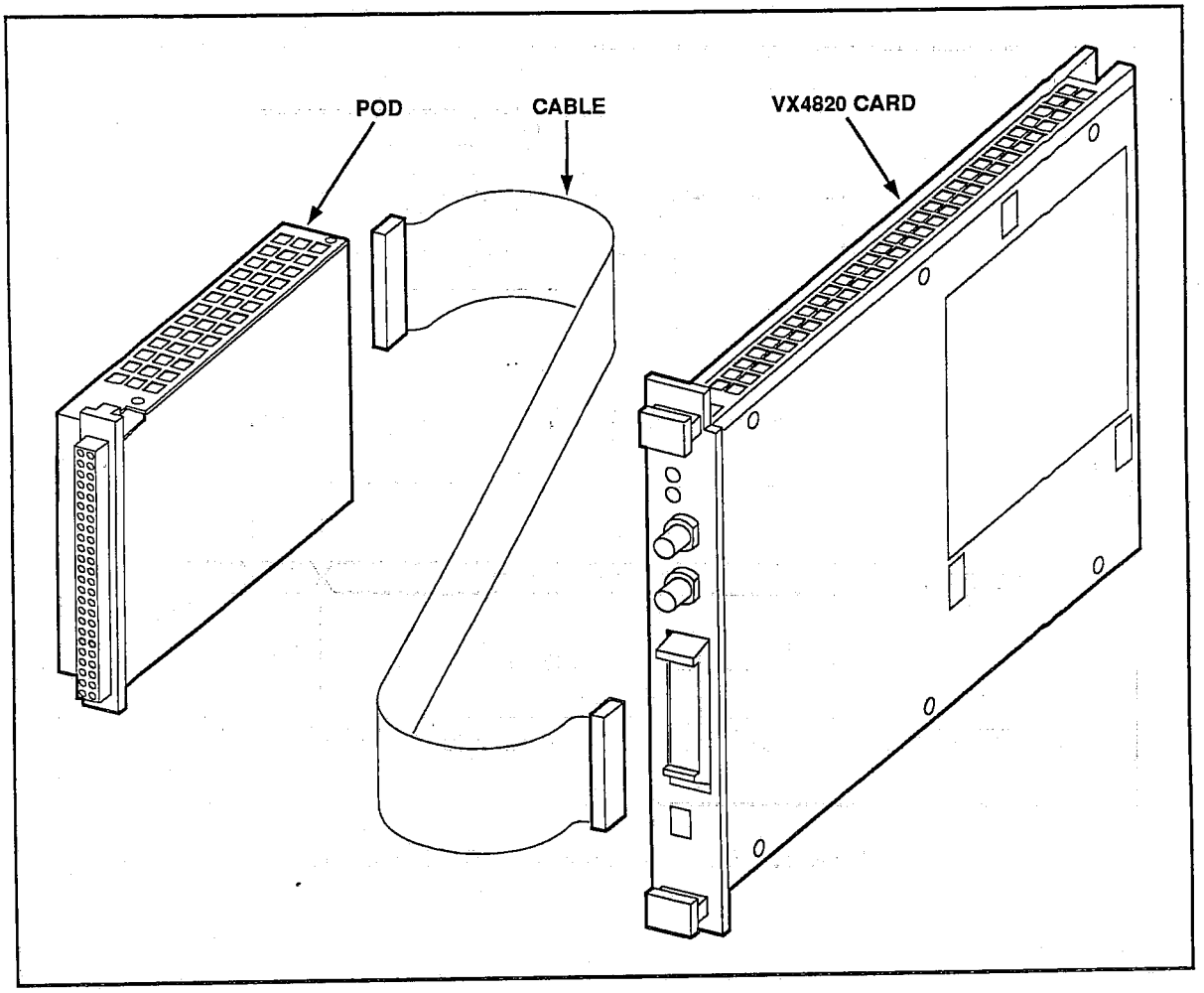


Figure 2. POD, cable, and VXI card assemblies.

STANDARD ACCESSORIES

The VX4820 Pods come with the following standard accessories:

- 1.8-meter (6 ft.) Pod Cable
- Connector Set [020-1953-00]
  - (1) Virginia Panel 64-pin Connector Housing (vendor part # 510-108-101)
  - (70) Virginia Panel Crimp Male Pins (vendor part # 610-110-108)
  - (2) Cap Head Screws, 4-40 X 0.625"

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Instructions

Tektronix

VXP16T & VXP64T
VX4820 TTL Pods

063–0980–00

First Printing: November 1991

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Instrument Serial Numbers

Each instrument manufactured by Tektronix has a serial number on a panel insert or tag, or stamped on the chassis. The first letter in the serial number designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B010000	Tektronix, Inc., Beaverton, Oregon, USA
E200000	Tektronix United Kingdom, Ltd., London
J300000	Sony/Tektronix, Japan
H700000	Tektronix Holland, NV, Heerenveen, The Netherlands

Instruments manufactured for Tektronix by external vendors outside the United States are assigned a two digit alpha code to identify the country of manufacture (e.g., JP for Japan, HK for Hong Kong, IL for Israel, etc.).

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

Printed in U.S.A.

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These instructions contain information about the two TTL Pods designed to be used with the VX4820 Digital Test Module. The information presented here covers key features and differences between the Pods and should be used as a supplement to the main VX4820 Digital Test Module Users Manual.

GENERAL INFORMATION

Two TTL Pods are offered to be used with the VX4820 Digital Test Module: the VXP16T and the VXP64T. The difference between these Pods is the maximum number of sequence steps each can support. With a VXP16T, up to 16351 sequence steps can be programmed. If more sequence steps are needed, the VXP64T can support up to 65503 sequence steps.

The main VX4820 Digital Test Module Users Manual assumes a VXP16T Pod is connected to the VX4820. Some differences will be noticed when using the VXP64T. The differences are in the queries:

DEVINFO?

PODTYPE?

DEVINFO?

The valid sequence step range is the smallest number of sequence steps in the VX4820 Digital Test Module or either Pod connected to it. This range can be found using the DEVINFO? query.

Example:

DEVINFO?

returns

DEVINFO 65503,16351,65503,64,50,3276700,50,2

This shows a VX4820 system with the module supporting a maximum of 65503 sequence steps, Pod 0 supporting a maximum of 16351 sequence steps, and Pod 1 supporting a maximum of 65503 sequence steps. The valid sequence step range for this system is 16351.

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NOTE

VX4820 Digital Test Modules with serial numbers below B010136 support a maximum of 16351 sequence steps, as does Digital Toolbox V1.1. These modules must be upgraded to 65503 sequence steps, and Digital Toolbox must be updated to V1.2 before the additional sequence steps of the VXP64T can be used. Contact your local Tektronix Field Office for further information.

PODTYPE?

From the DEVINFO? example, the maximum number of sequence steps each Pod supports are known, but not what type of Pod is actually connected to the VX4820 Digital Test Module. To determine this, use the PODTYPE? query.

Example:

PODTYPE? 0

returns

PODTYPE 289

and

PODTYPE? 1

returns

PODTYPE 273

Table 1 shows that Pod 0, with its POD ID of 289, is 32 Pins of TTL I/O, capable of operating up to 20MHz, and supports 16351 sequence steps. Pod 1, with a POD ID of 273, is also 20MHz TTL I/O, but can support 65503 sequence steps.

Table 1
Pod Types

POD	POD ID	Pod Description
NA	–1	No Pod Present
VXP64T	273	32 Pins of TTL I/O, 20 MHz, 65503 sequence steps
VXP16T	289	32 Pins of TTL I/O, 20 MHz, 16351 sequence steps
VXP64C	785	32 Pins of CMOS I/O, 20 MHz, 65503 sequence steps
VXP16C	801	32 Pins of CMOS I/O, 20 MHz, 16351 sequence steps

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SPECIFICATIONS

Table 2
Environmental Specifications

Characteristics	Description
Temperature	
Operating	0°C to +50°C
Nonoperating	–55°C to +75°C

Table 3
Electrical Specifications

Characteristics	Performance Requirements	Supplemental Information
Number of pins		32
Number of sequence steps		16,351 VXP16T; 65,503 VXP64T
Pin functions		DRIVE INHIBIT COMPARE w/MASK DRIVE & COMPARE w/MASK LEARN (Learn mode only)
Drive	High Level ≥ 2 V @ I_{OH} ≤ 15 mA Low Level ≤ 0.8 V @ I_{OL} ≤ 64 mA (sink)	High Level ≥ 2.4 V when I_{OH} ≤ 3 mA (source) Low Level ≤ 0.55 V when I_{OL} ≤ 48 mA (sink)
Short Circuit Current	–225 mA maximum	
Format		Fixed NRZ
Skew between any two pins	≤ 10 ns	
Inhibit		Presents a single FTTL load –0.6 mA max.
Compare	Low ≤ 0.8 V High ≥ 2 V	0.8 V < Intermediate band < 2 V Setup time 25 ns prior to end of cycle. Hold time 0 ns prior to end of cycle (first output transition)
Pin termination		Diode clamp to +5 V and Gnd, optional AC termination to Vcc (100 pF in series with 100 Ω).
Pin Capacitance		50 pF in parallel with the optional AC termination

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Table 3 (Cont.)
Electrical Specifications

Characteristics	Performance Requirements	Supplemental Information
Nondestructive I/O Voltage	–0.5 V to +7 V	Drivers and receivers are socketed.
Pod CLK IN	25 ns min, Clk low 25 ns min, Clk high $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2$ V	Impedance: 1 FTTL load (–0.6 mA max). Typical delay CLK to STB: 84 ns
Pod STB OUT		PIN data valid prior to STB ≥ 25 ns; PIN data valid after STB ≥ 7 ns. Compare input setup time prior to STB OUT ≥ 10 ns. Compare input hold time after STB ≥ 1 ns
UUT Response Time		Data Out Valid ≥ CLK period – 10 ns. UUT Response Time ≤ CLK period – 25 ns (for same cycle compare). See the UUT Response Time figure for details.

Table 4
Mechanical Specifications

Characteristics	Description
Overall Pod dimensions Height Width Depth	 30.48 mm (1.2") 144.2 mm (5.6") 226.1 mm (8.9")
Weight Nominal Pod and cable	 3.1 kg (6.8 lbs) 0.8 kg (1.7 lbs)
Cooling Requirements	Pods can dissipate up to 10 W of heat when operated at a 100% duty cycle at 20 MHz. Care should be taken to ensure adequate airflow is available in the test head. In most manufacturing test environments, the actual test execution duty cycle is much less than 50%, and there are no special cooling requirements.

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