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TECHNOLOGY GROUP

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Find the *Teledyne Dalsa / Coreco Imaging PC-DIG* at our website: *Click HERE*

CORECO iMAGING
EXCELLENCE IN MACHINE VISION

Acquisition constraints and Video Input Timing

Features

Video input	Number of camera input	• 1 Digital input (LVDS or RS-422))
	Pixel format	• Monochrome • Up to 4 taps of 8-bits/pixel • Up to two taps of 16-bits/pixel • Up to one tap of 32-bits/pixel • RGB 24-bits
	Scanning	• Progressive • Multi-taps • Multi-channels • Four quadrant • Interleaved pixels • Interline • Interlace • Tap reversal
	Resolution	Horizontal minimum: • 4 Pixels x tap Horizontal maximum: • 8-bits/pixel x 64K Pixels/line • 16-bits/pixel x 32K Pixels/line • 32-bits/pixel x 16K Pixels/line **Note:** The number of bits is per pixel, not the total input bits • Vertical minimum 1 line • Vertical maximum 64K lines
	Pixel clock range	• Up to 20 MHz Maximum for RS-422. • Up to 40 MHz Maximum for LVDS.
	Timing outputs	• External Synchronization (EXSYNC) programmable period 210 ns to 18.75 s, programmable pulse width 140 ns to 572 us. • Programmable Integration (PRI) or exposure control, programmable start and end points.

Timing Parameters

Parameter	*Definition*	RS-422	LVDS
LEN*min*	Minimum LEN inactive (H Blanking)		
	synchronous mode	1 PCLK cycle	1 PCLK cycle
	asynchronous mode	20 ns	10 ns
FEN*min*	Minimum FEN inactive (V Blanking)	1 PCLK cycle	1 PCLK cycle
MULTI*min*	Minimum MULTI inactive	1 PCLK cycle	1 PCLK cycle
V*p*	Minimum PCLK period	50 ns	25 ns
V*h*	Minimum PCLK high	20 ns	10 ns
V*l*	Minimum PCLK low	20 ns	10 ns
T*su*	Data and timing set-up to selected edge of PCLK (synchronous mode)	12 ns	8 ns
T*h*	Data and timing hold from selected edge of PCLK (synchronous mode)	6 ns	2 ns

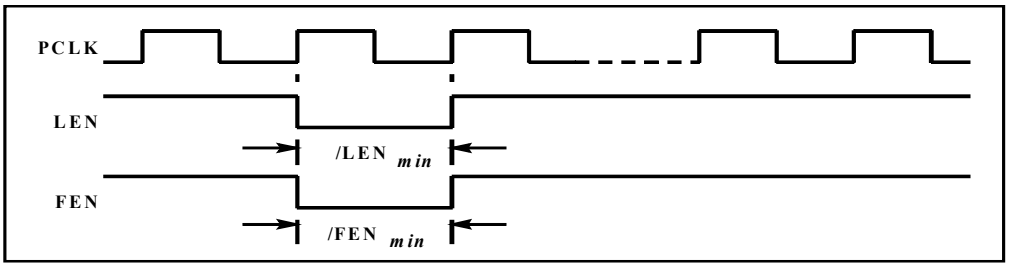


Figure 1. Line and Frame Timing

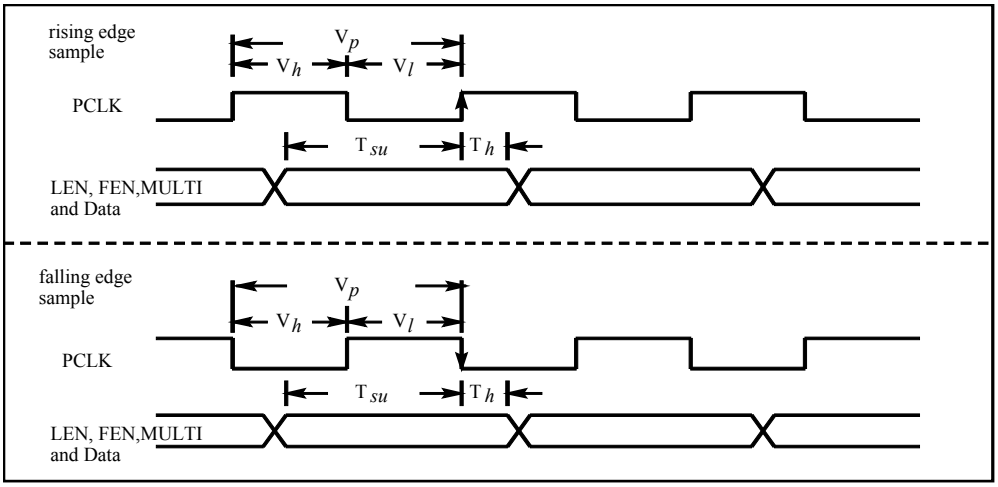


Figure 2. Synchronous Timing

- Synchronous mode: LEN, FEN, and MULTI are sampled on selected edge of clock input PCLK.
- Asynchronous LEN mode: LEN is edge sampled with programmable polarity. FEN and MULTI are still sampled on selected edge of PCLK.
- Polarity of LEN, FEN, PCLK and MULTI are programmable.
- Programmable image size (window) H Offset, H Active, V Offset, V Active.

Parallel Port

- OPTO-22 compatible Parallel I/O port: 8 TTL inputs, 8 TTL/CMOS outputs

Triggering Inputs

- 2 independent programmable triggers
- 2 TTL inputs, 2 differential inputs, 2 opto-coupled inputs, 2 software triggers.
- Input divider 8-bit

Physical Description

- Requires a 3/4-length PCI slot

Environmental

- Operating Temperature: 10 to 50 degree C
- Relative Humidity: 5% to 90% (non-condensing)

Power Consumption

- 2.0 Amp on 5 Volts (10.0 Watts) typical

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