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http://www.dalsa.com

PC2-Vision

User's Manual

Part number OC-PC2M-VUM00
Edition 2.52



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Introduction

Overview of the Manual

PC2-Vision Board

- The PC2-Vision
  Description of the PC2-Vision board, package contents, and a brief summary of its capabilities as well as installation information.
- Configuring Sapera
  Describes Sapera servers and contiguous memory.
- Theory of Operation
  Detailing PC2-Vision features.
- Technical Reference
  PC2-Vision specifications including connector and pinout diagrams.

Sapera LT

- Sapera Server and Parameters
  Lists the Sapera server available and describes the Sapera parameters and values supported by PC2-Vision.
- PC2-Vision Specific Sapera Examples
  Illustrates three Sapera examples specific to PC2-Vision.
- Sapera Software Example
  Describes in detail the Sapera Grab Demo example and how use it.
- Using Sapera CamExpert with PC2-Vision
  Describes CamExpert and how to use it with PC2-Vision.

IFC

- IFC Software Examples
  Twenty-four IFC example programs illustrating PC2-Vision features.
- Applying IFC Camera Configurator to PC2-Vision
  Illustrates how to setup an imaging system using the DALSA Camera Configurator®.
- PCVision IFC Parameter Comparison
  PCVision parameters are compared with the corresponding PC2-Vision parameters.

Troubleshooting

- Offers suggestions for resolving installation or usage problems.

DALSA Contact Information

- Phone numbers, web site, and important email addresses.

About the Manual

This manual exists in Adobe Acrobat (PDF) and .chm help formats. These formats make full use of hypertext cross-references and include links to the DALSA home page on the Internet, located at http://www.dalsa.com/, accessed using any web browser.

For PC2-Vision specific information, visit the DALSA web site at http://www.dalsa.com/.

This manual applies to both the PCI and PCIe versions of the board.

Using the Manual

File names, directories, and Internet sites will be in bold text
(for example, **image2.bmp**, **c:\IFC**, **http://www.dalsa.com**).

Text that must be entered using the keyboard will be in typewriter-style text
(for example, `c:\temp`).

Menu and dialog actions will be indicated in bold text in the order of the instructions to be executed, with each instruction separated by bullets. For example, going to the **File** menu and choosing **Save** would be written as **File•Save**.

PC2-Vision Board

The PC2-Vision

Overview

Two versions of the PC2-Vision are available; as a PCI version 2.1 or PCI Express compatible plug-in board. Both versions provides image capture for cost sensitive machine vision applications. This manual applies to both versions.

The acquisition circuitry interfaces with standard (RS-170 and CCIR) and non-standard (progressive scan) analog cameras, RGB and dual-channel analog cameras. PC2-Vision makes interfacing with cameras easy by offering fully programmable timing coupled with efficient cabling and a variety of trigger, strobe and asynchronous reset options. To further simplify the integration task, PC2-Vision provides general-purpose parallel I/O capabilities for controlling or monitoring the status of external events.

PC2-Vision provides a very efficient 32-bit PCI or PCI Express interface, which is capable of bus mastering image data directly to a memory destination within the system (that is, system memory or another PCI or PCI Express target, such as VGA). Transfer rates up to 100 MB/second are sustained, depending upon host capabilities. Consequently, images can be transferred to host memory in a fraction of the time acquired. More bandwidth is, therefore, available for other system resources to utilize by minimizing PC2-Vision transfer time on the PCI or PCI Express bus.

PC2-Vision provides a number of interrupt sources such as image acquisition and bus master transfer completion.

PC2-Vision contains 8MB of memory for buffering image data between the camera and the host system. Onboard memory assures that image information is not lost during transfer to system memory due to PCI bus latency issues. The memory is addressed linearly for maximum utilization. Images are grabbed into local memory and then transferred at very high speeds to the host for processing or display.

PC2-Vision is supported by both Sapera LT and IFC. It is also fully supported by the Sapera Image Processing library.

Note: You can install the PC2-Vision device driver for either IFC or for Sapera LT. You cannot use both IFC and Sapera LT at the same time for PC2-Vision.

PC2-Vision Features and Block Diagram

Features

- Half-size PCI or PCI Express form factor
- Six analog video inputs, AC coupled and terminated to 75Ω
- Acquires up to six monochrome or two RGB cameras; simultaneous acquisition up to three genlocked monochrome cameras
- Supports standard RS-170 and CCIR, non-standard progressive cameras and RGB formats
- External Trigger input; synchronizes acquisition to external events
- Resolution up to 2048 x 2048 interlaced or non-interlaced
- Video controls allow brightness and contrast
- Windows® XP, Windows® Vista and Windows 7
- 40MHz digitization rate (8-bit)
- Anti-aliasing filters: 6 MHz, 12 MHz or bypass (software selectable)

See "PC2-Vision Specifications" on page 72 for detailed information on PC2-Vision specifications.

Functional Block Diagram

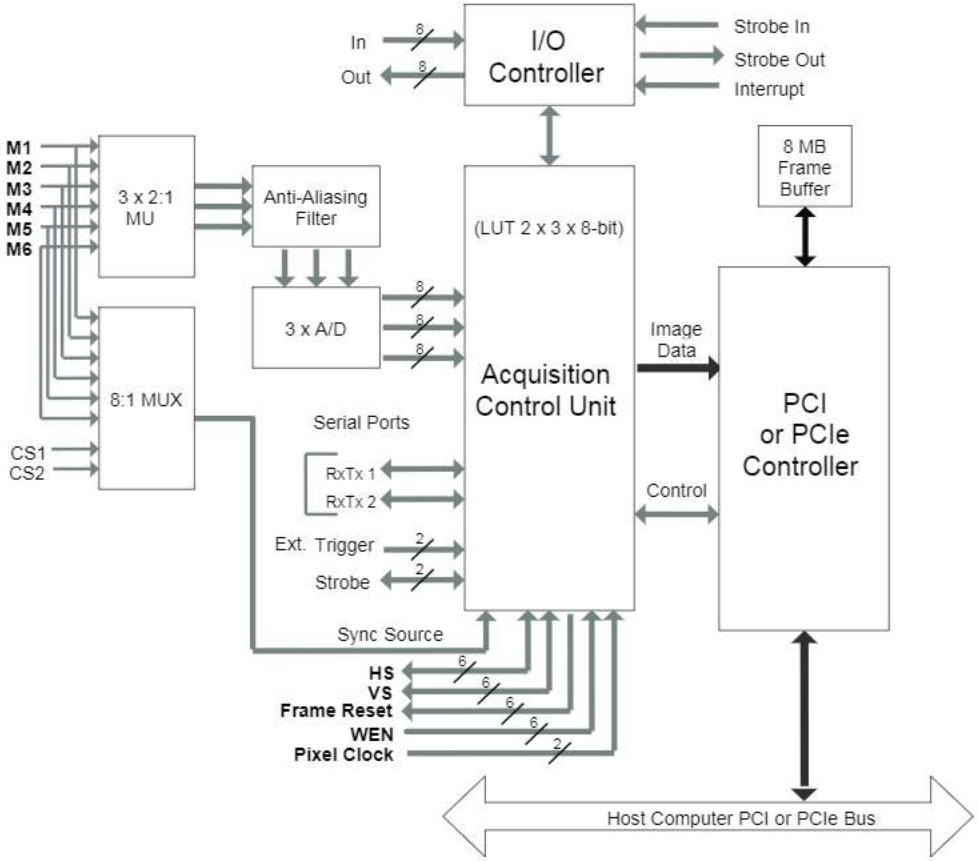


Figure 1: PC2-Vision Block Diagram

Components & Part Numbers

The following table lists the components and part numbers for the PC2-Vision:

Item	Part Number
Board	
PC2-Vision PCI	Contact Sales
PC2-Vision PCI Express	Contact Sales
Cables & Accessories	
Floppy power connector	OC-COMC-POW03
Single camera BNC cable	OC-PC2C-V1B00
Single RGB camera BNC cable	OC-PC2C-V1B01
PCVision Series adapter cable	OC-PC2C-V3A00
Single camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V1H00
Three camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V3H00
Single camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V1H01
Three camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V3H01
Single camera Hirose-12 + Hirose-6 for Jai A-series camera	OC-PC2C-V1H02
Three camera Hirose-12 + Hirose-6 for Jai A-series camera	OC-PC2C-V3H02
Jai CV-M77 RGB camera cable	OC-PC2C-V1D00
Pulnix camera cable (supporting three cameras)	OC-PC2C-V3H03
Jai M-series camera cable (supporting three cameras)	OC-PC2C-V3H04
Parallel I/O connector to female DB25 bracket assembly	4816
Documentation	
PC2-Vision User's manual	OC-PC2M-VUM00

EC & FCC Certificate of Conformity

PC2 Vision Board



EC & FCC DECLARATION OF CONFORMITY

We : DALSA Montreal Inc.
7075 Place Robert-Joncas, Suite 142,
St. Laurent, Quebec, Canada H4M 2Z2

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 89/336 EEC on the approximation of the laws of member states relating to electromagnetic compatibility, as amended by directive 93/68/EEC:

FRAME GRABBER BOARD: **PC2-Vision**

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55022:1998- Residential, Commercial and Light Industry
ENV50204: 1995
EN61000-4: 1995, 1996

Further declare under our sole legal responsibility that the product listed conforms to the code of federal regulations CFR 47 part 15 for a class B product.

St. Laurent, Canada — Location
2010/11/04 — Date

Eric Carey, ing
Director,
Research & Development

EC & FCC DECLARATION OF CONFORMITY

We : DALSA Montreal Inc.
7075 Place Robert-Joncas, Suite 142,
St. Laurent, Quebec, Canada H4M 2Z2

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 89/336 EEC on the approximation of the laws of member states relating to electromagnetic compatibility, as amended by directive 93/68/EEC:

FRAME GRABBER BOARD: PC2 Vision Express

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55022:1998- Residential, Commercial and Light Industry
ENV50204: 1995
EN61000-4: 1995, 1996, 1998, 2001
EN60255-22: 2002

Further declare under our sole legal responsibility that the product listed conforms to the code of federal regulations CFR 47 part 15 for a class A product.

Montreal, Canada — Location
2008/05/22 — Date

Ghislain Beaupré
Vice-President,
Research & Development

Development Software Overview

Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards.

Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

Installing the PC2-Vision

Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation.

If you do not feel comfortable performing the installation, please consult a qualified computer technician.



Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

Upgrading Sapera or any Board Driver

When installing a new version of Sapera or a DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Upgrade scenarios are described below.

Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are typically distributed as ZIP files available in the DALSA web site http://www.dalsa.com/. Board driver revisions are also available on the next release of the Sapera CD-ROM.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version, contact DALSA Technical Support (see "Technical Support" on page 170).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- From the Windows start menu select **Start • Control Panel • Add or Remove Programs**.
- Select the DALSA PC2-Vision Device Driver, click **Remove**, and then in the InstallShield dialog click on **Remove** to uninstall the board driver.
- When the driver un-install is complete, reboot the computer.
- Logon the computer as an administrator again.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.
- If the new driver is on a Sapera CD-ROM follow the installation procedure described in the section "Installing PC2-Vision Hardware and Driver" on page 13.
- Note that you can not install a DALSA board driver without Sapera LT installed on the computer.

Sapera and Board Driver Upgrades

When both Sapera and the acquisition board driver are upgraded, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- From the Windows start menu select **Start • Control Panel • Add or Remove Programs**.
- Select the DALSA PC2-Vision Device Driver, click **Remove**, and then in the InstallShield dialog click on **Remove** to uninstall the board driver.
- From the Windows start menu select **Start • Control Panel • Add or Remove Programs**.
- Select the DALSA Sapera LT program, click **Remove**, and then in the InstallShield dialog click on **Remove** to uninstall Sapera.
- If prompted to do so, reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. For installation procedures, see "Sapera LT Library Installation" on page 13 and "Installing PC2-Vision Hardware and Driver" on page 13 for installation procedures.

Sapera LT Library Installation

Note: to install Sapera LT and the PC2-Vision device driver, logon to the workstation as administrator or with an account that has administrator privileges.

The Sapera LT Development Library (or 'runtime library' if application execution without development is preferred) must be installed before the PC2-Vision device driver.

- Insert the DALSA Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the installation menu is presented.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu and install the required Sapera components.
- The installation program will prompt you to reboot the computer.

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

Installing PC2-Vision Hardware and Driver

In a Windows /XP/Vista/7 System

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the PC2-Vision into a PCI slot or the PCI Express in a x1 expansion slot. The PC2 Express can also be installed in a PCI Express x4, x8 slot, or x16 slots.
- Close the computer chassis and turn the computer on. Driver installation requires administrator rights for the current user of the computer.
- Windows will find the PC2-Vision and start its **Found New Hardware Wizard**. Click on the **Cancel** button to close the Wizard.
- Insert the DALSA Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the installation menu is presented. Install the PC2-Vision driver.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu. Click **Software Installation**, then **Install Hardware Device Driver**, **Frame Grabbers - Device Drivers,** and **PC2 Series**. Select the **PC2-Vision** board and install the PC2-Vision driver. Note, if you are using Vista with the User Account Control feature enabled, a dialog is displayed when you execute **launch.exe**; click **Allow** to continue with the driver installation.
- Choose the device driver setup type, full installation (required for application development) or runtime installation (supports application execution only).
- When using **Windows XP**, if a message stating that the PC2-Vision software has not passed **Windows Logo testing** is displayed, click on **Continue Anyway** to finish the PC2-Vision driver installation. Reboot the computer if prompted to do so.
- When using **Windows Vista/7**, a message asking to install the DALSA device software is displayed. Click **Install**.



- During the installation the PC2-Vision Device Manager firmware loader application starts. Click Update All.
- When the installation is complete, the following dialog box is displayed:



Connecting Camera and Devices

Connector Bracket

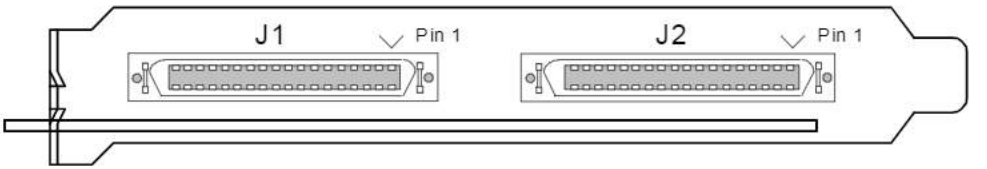


Figure 2: Connector Bracket

There are two MDR (Mini Delta Ribbon) 36-pin female camera connectors on the front bracket of the PC2-Vision board labeled J1 and J2. Both connectors control a group of cameras called 'channels.' J1 controls channels 1 to 3. J2 controls channels 4 to 6. Therefore, six monochrome cameras can be connected to the PC2-Vision. See the "PC2-Vision Connector and Jumper Locations" on page 74 for further information.

Note: PC2-Vision's J6 connector must be connected to a floppy power cable to provide 12V to the cameras. Refer to "PC2-Vision component view" on page 74 section for connector locations.

PC2-Vision boards are able to provide up to 500mA of power to the camera from the PCI or PCI Express connector (fused protected). Nonetheless, DALSA recommends connecting the floppy power connector to ensure sufficient current is driven to the cameras from the PC power supply.

Caution: Sinking more than 500mA from the PC2-Vision PCI or PCI Express connector may result in the auto-reset fuse blowing or in erratic behavior with the camera if it requires more than 500mA. Check your camera datasheet for the required camera current.

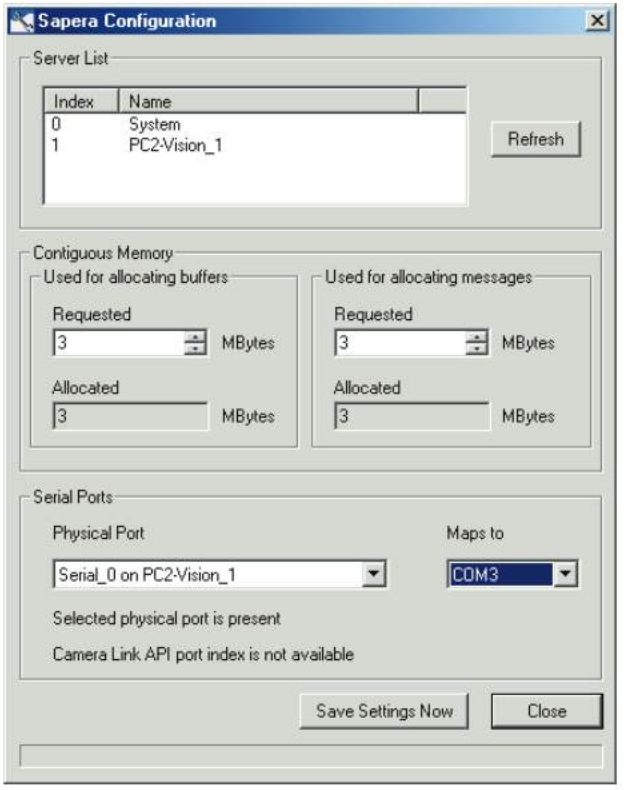


Warning: Some cameras have frame reset located on pin 9 of the Hirose-12 connector while other cameras have it on pin 11. It is imperative to use the appropriate camera cable that matches the frame reset pinout. Failure to do so could result in board damage.

COM Port Assignment

The lower section of the Sapera Configuration program screen contains the serial port configuration menu. Configure as follows:

- Open the 'Sapera Configuration' program by selecting **Start•Programs•DALSA•Sapera LT•Sapera Configuration**.
- Use the **Physical Port** drop menu to select the Sapera board device from all available Sapera boards using serial ports (when more then one board is in your system).
- Use the **Maps to** drop menu to assign an available COM number to the Sapera board serial port.
- Click on the **Save Settings Now** button and then the **Close** button. You are prompted to reboot your computer to enable serial port mapping.
- The PC2-Vision serial port (mapped to COM3 in this example) is available as a serial port to any serial port application for camera control. Note that this serial port is not listed in the **Windows•Control Panel•System Properties•Device Manager** because it is a logical serial port mapping.

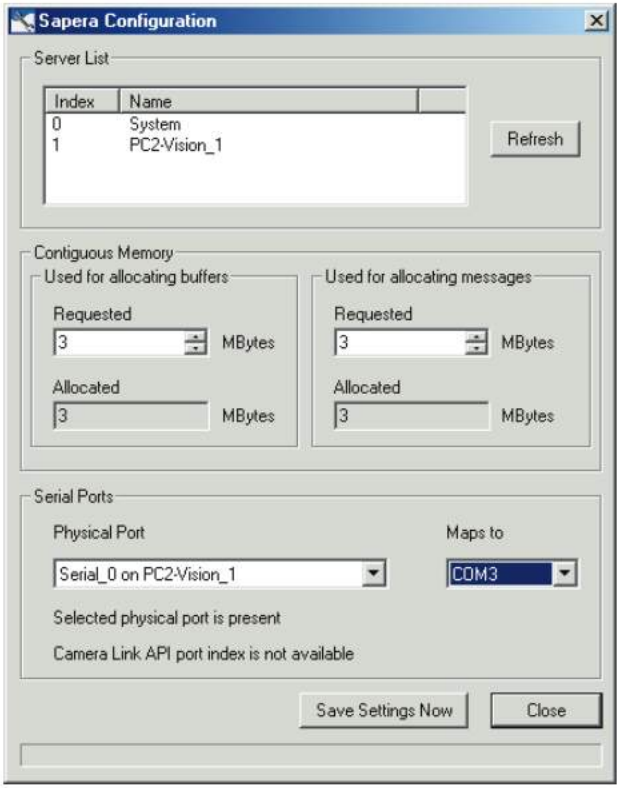


Configuring Sapera

Viewing Installed Sapera Servers

The Sapera Configuration program (**Start•Programs•DALSA•Sapera LT•Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards.

The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should be present at all times. As shown in the following screen image, server index 1 is the PC2-Vision board installed. If required, update the server list by clicking the **Refresh** button.



Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory occupying consecutive addresses) reserved for the resources needed for **Sapera buffer** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the default driver memory setting while the **Allocated** value displays the amount of contiguous memory that has been allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffer** values determine the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for host frame buffer management, such as DMA descriptor tables as well as other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers. You can approximate the amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for frame buffers (number of frame buffers • number of pixels per line • number of lines • (2 (if buffer is 10 or 12 bits)).
- Provide 1MB for every 256MB of host frame buffer memory required.
- Add an additional 1MB if the frame buffers have a short line length, for example, 1k or less (increased number of individual frame buffers requires more resources).

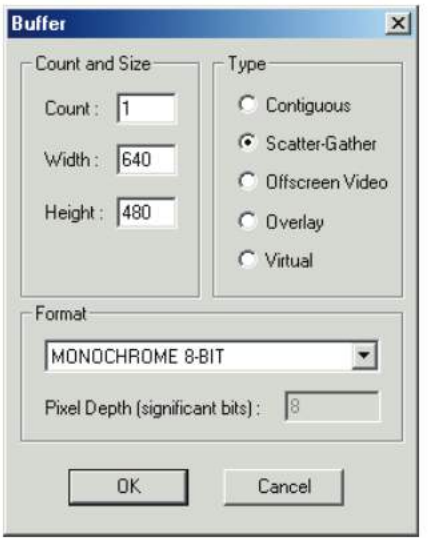
Add an additional 2MB for various static and dynamic

- Sapera resources.
- Test for any memory error when allocating host buffers. Simply use the "General Options" in the Grab Demo Main Window (see page 115) menu of the Sapera Grab Demo program (see "Using the Grab Demo" on page 115) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum host buffer limit possible in your host system – Grab Demo will not crash when the requested number of host frame buffers cannot be allocated.

Host Computer Frame Buffer Memory Limitations

When planning a Sapera application and the host frame buffers used, as well as other Sapera memory resources, do not forget the needs of the Windows operating system memory. Window® XP, as an example, should always have a minimum of 128MB for its own use.

A Sapera application using *scatter-gather buffers* could consume most of the remaining system memory. When using frame buffers allocated as a *single contiguous memory block*, typical limitations are one third of the total system memory with a maximum limit of approximately 100MB. Click on **Buffer** under Grab Demo Main Window (see page 115) to select from a list of host buffer memory allocation types.



Contiguous Memory for Sapera Messaging

The current value for **Sapera messaging** determines the total amount of contiguous memory reserved at boot time for message allocation. This memory space is used to store arguments when a Sapera function is called. Increase this value if you are using functions with large arguments, such as arrays, and when experiencing any memory errors.

IFC Development Software Overview

IFC-SDK™

The IFC (Imaging Foundation Classes) library offers a C++ Application Program Interface (API) intended for use with the DALSA PC2-Vision board (requires IFC version 5.8 or higher).

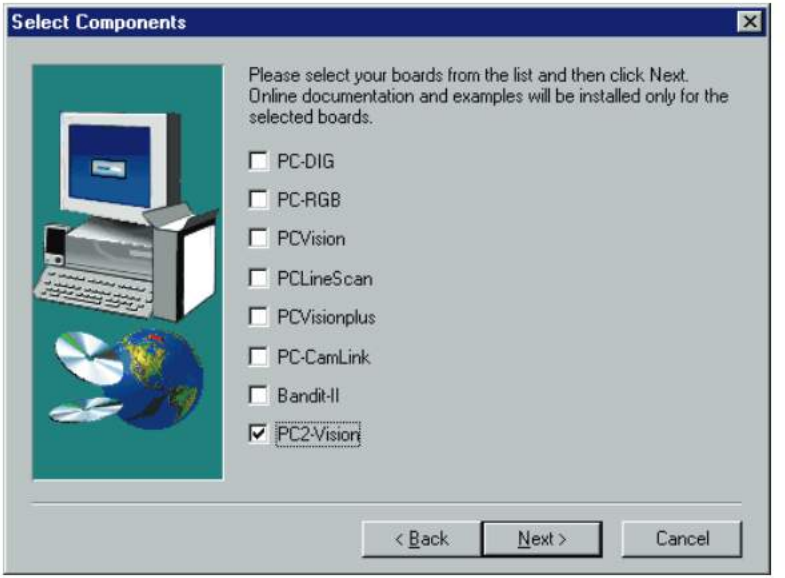
IFC is packaged within the "Imaging Studio CD-ROM".

See the *IFC-SDK™ Software Manual* for information concerning IFC.

Information in this manual matches IFC 5.8 service pack 1.

IFC Software Installation

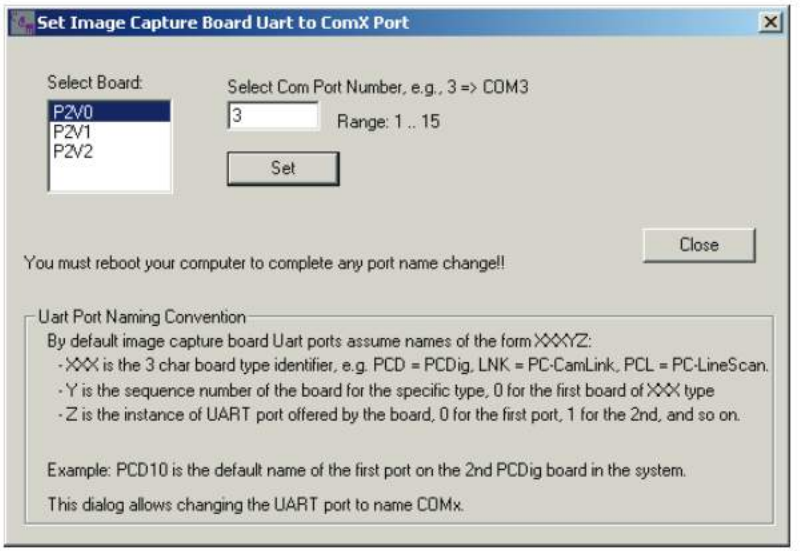
- Make certain that you are logged into your machine with 'administrator' privileges.
- Insert the "Imaging Studio CD-ROM".
- Click on Install Software after auto-start initiates.
- Select OS system and software to install in the pull-down menu and click Start Install.
- Make certain that all window applications are closed before clicking Next in the "Welcome" window.
- Click Yes after reading the Software License Agreement.
- Enter your name and company in the "User Information" window and click Next.
- Click Next in the "Choose Destination Location" window if you want the software to install in the default folder. Click Browse to select another folder if desired.
- If **Browse** is selected, click **OK** in the "Choose Folder" window after path, directory, and driver selections are made.
- The "Setup" window opens and asks if it can create the destination folder displayed. Click **Yes**.
- The "Choose Destination Location" window reopens. Click **Next**.
- The "Setup Type" window is displayed. It is recommended to select the *typical* installation. Click Next.



- The "Select Components" window is displayed (see above screen shot). Check *PC2-Vision* and click Next. Note that only the support, configuration files and examples for the board(s) chosen get copied to your hard drive.
- The "Select Components" window is displayed a second time with a default list of cameras. Select a camera from the default list or select None. If None is selected, a camera file is not installed; however, you can use the Camera Configurator® at anytime after installation to install a camera file.
- After clicking Next in the "Select Program Folder" window, the software and files install unto your hard drive.
- A window appears asking if you want Acrobat Reader installed to view and print installed manuals. Click Yes if you do not already have Acrobat Reader installed on your system.
- Click Yes or No after a window appears asking to view readme files.
- The "Service Pack Update Check" window is displayed. This allows you to check for an IFC service pack update via the DALSA web site. Note that you need an active Internet connection. Click Yes if you want to check for an update.
- The "Setup Complete" window appears and asks whether you want to restart the computer now or at a later time. Choose desired option and click Finish. Note that the computer must be restarted for drivers to take effect.

Optional COM Port Assignment

The IFC "Set Board COM port" application tool is used to assign the COM port. Run the program from the Windows Start menu: **Start♦Programs♦IFC version 5.8♦Set Board COM port**.



To assign a standard COMx name to PC2-Vision:

- Under "Select Board" choose the PC2-Vision board you want to map (P2V0 is the first PC2-Vision board, P2V1 is the second…).
- Under "Select COM port Number" assign an unused COM port number to the PC2-Vision board and click **Set**.
- Click **Close**.
- Reboot PC for the new settings to take effect.

Theory of Operation

PC2-Vision Flow Diagram

The following three diagrams represent the sequence and components in which the data acquired from the camera is piloted and processed through the PC2-Vision. The process is broken down into three stages:

- Analog Stage
- Pre-Memory Operations
- Post-Memory Operations

Note: the diagrams are broken into three stages for user clarity. In reality the data flow in 'real-world' operation is a continuous stream in which all three stages act as a single process.

The remainder of this chapter will detail features associated with this flow diagram in order of appearance from the camera control to the PCI or PCI Express controller.

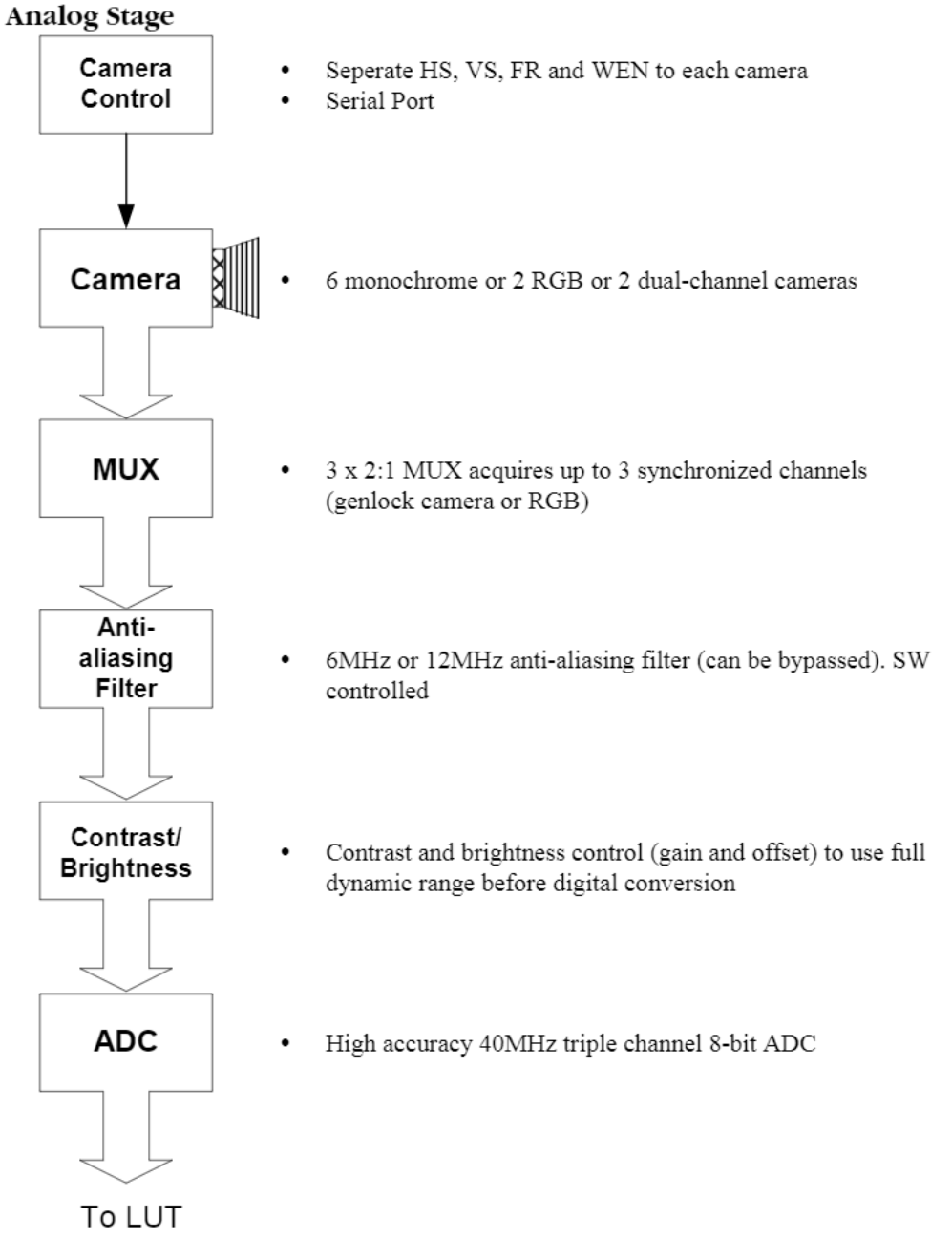
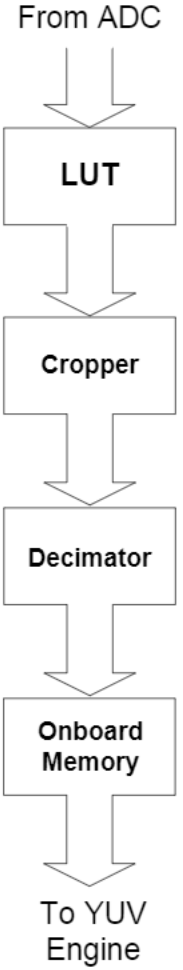


Figure 3: Analog Stage of Flow Diagram

Pre-Memory Operations



- 8-bit LUT, 1 per camera (total of 6 LUTs onboard)
- Create region of interest
- Image decimation by 2, 4, or 8 horizontally and vertically (pixel dropping)
- 8MB
- Maximum frame size of 2k x 2k mono, or 1k x 1k RGB. Ensures 2 frames in onboard memory for double buffering
- All cameras must have the same frame size when starting an acquisition

Figure 4: Pre-Memory Stage of Flow Diagram

Post-Memory Operations

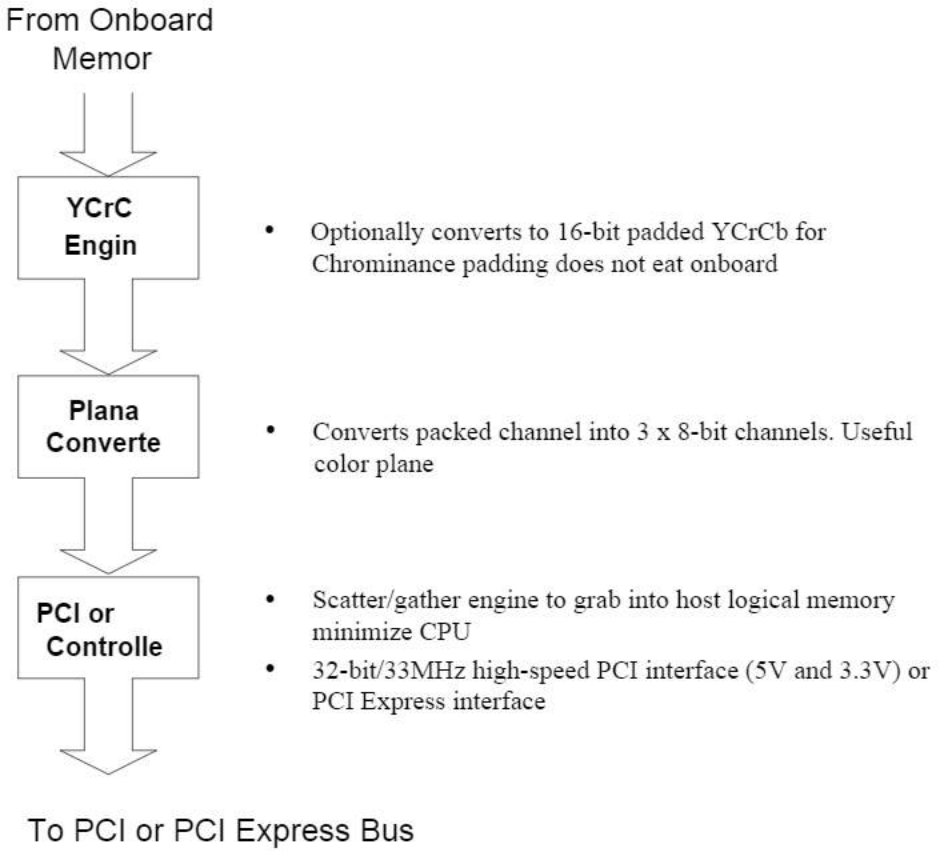


Figure 5: Post-Memory Stage of Flow Diagram

Camera Control and Synchronization

Source of Synchronization

PC2-Vision offers a selection of synchronization sources allowing it to interface with various cameras. All six cameras have their own HS, VS, frame reset and WEN signal. The Acquisition and Control Unit (ACU) is the main controller responsible for supervising the acquisition process. It manages all the signals coming from the cameras and recovers the timing information to accurately digitize the video signal into pixels.

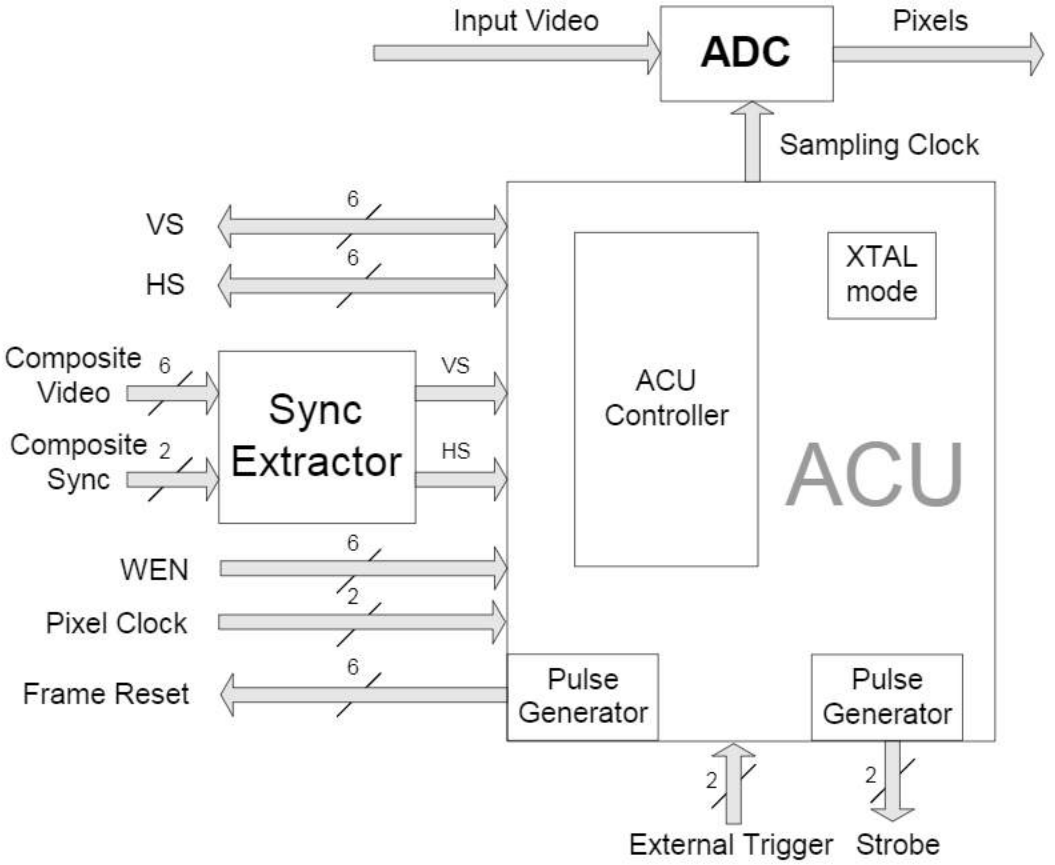


Figure 6: Synchronization Block Diagram

Sync on Composite Video

Vertical Sync (VS) and horizontal sync (HS) signals are extracted from the composite video output signal by the Sync Extractor. The PLL receives the stripped horizontal sync and outputs a pixel clock which is line-locked to the incoming video and is used to digitize video and generate frame timing. The PLL is programmed based on the timing requirements of the incoming video. The ADC uses the PLL generated pixel clock to digitize the video input.

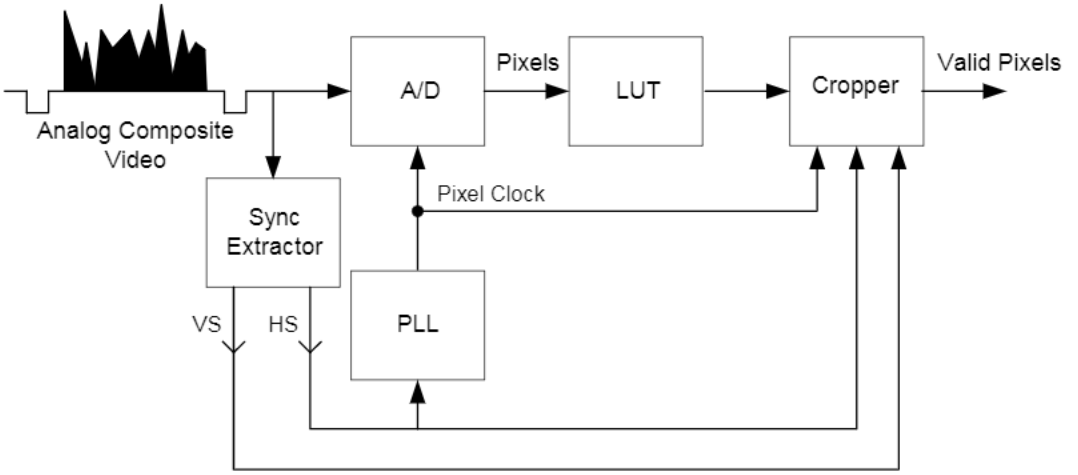


Figure 7: Composite Video

Synchronization on composite video is commonly used for standard RS-170 and CCIR cameras as well as for many non-standard cameras. Video input pins are 75Ω terminated.

Sapera parameters for Sync on Composite Video:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_COMP_VIDEO
CORACQ_PRM_HSYNC: Size of horizontal sync pulse
CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch
CORACQ_PRM_HACTIVE: Number of valid pixels per line
CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch
CORACQ_PRM_VSYNC: Size of vertical sync pulse
CORACQ_PRM_VBACK_PORCH: Size of vertical back porch
CORACQ_PRM_VACTIVE: Number of valid line from camera
CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch
In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Sync on Composite Video:

P2V_SYNC_SOURCE = P2V_SYNC_COMPOSITE_VIDEO
P_HSYNC_FREQ: Horizontal sync frequency
P_HSYNC_WIDTH: Size of horizontal sync pulse
P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}
P2V_HORZ_FRONT_PORCH: Size of horizontal front porch
P2V_HORZ_BACK_PORCH: Size of horizontal back porch
P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Sync on R, G, or B

Sync on R, G, or B behaves like sync on composite video with the exception that only one color channel is used to synchronize the three-color inputs. Timing information is extracted from the selected composite video signal and is common to all three inputs. Asynchronous inputs are not supported by the PC2-Vision. The timing and synchronization settings apply to all three channels.

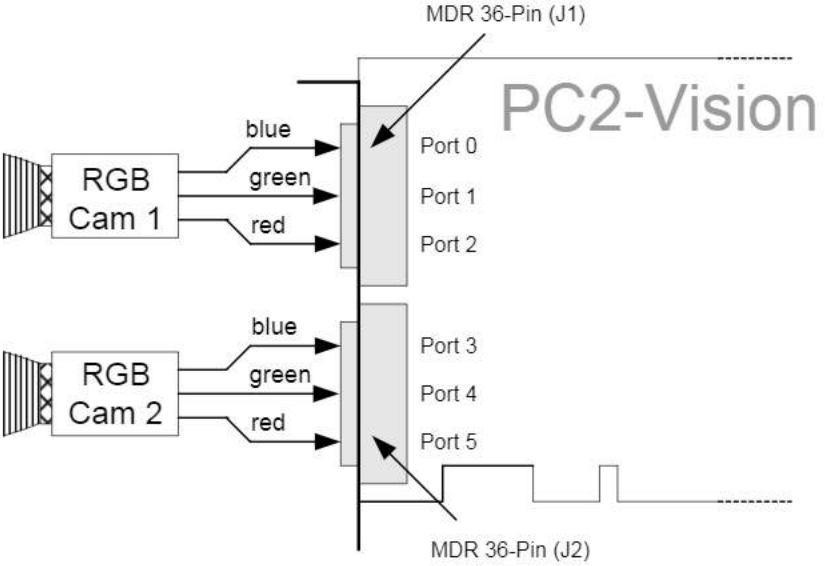


Figure 8: Sync on R, G, or B

Note: that for an RGB camera, the green channel is used as the timing reference if sync on composite video is selected.

Note: Dual-channel cameras are not currently supported with the PC2-Vision Sapera driver.

Sapera parameters for Sync on R, G or B:

CORACQ_PRM_VIDEO = CORACQ_VAL_VIDEO_RGB

CORACQ_PRM_SYNC = { CORACQ_VAL_SYNC_RED, CORACQ_VAL_SYNC_GREEN, CORACQ_VAL_SYNC_BLUE}

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

Dual-channel cameras must use the blue and green channels paired together. PC2-Vision supports the following dual-channel cameras under IFC:

- Channel 1 is always even field (blue channel, port 0 or 3)
- Channel 2 is always odd field (green channel, port 1 or 4)

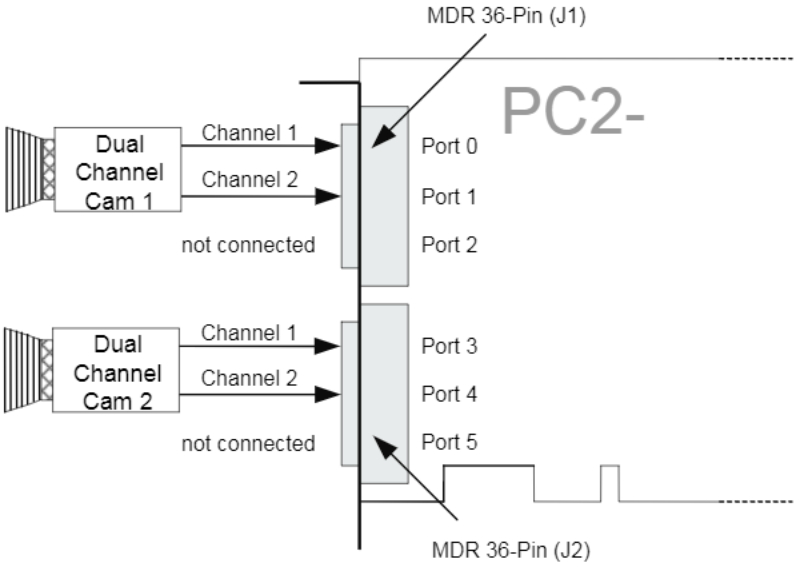


Figure 9: Dual Channel Cameras for IFC

IFC parameters for Sync on R, G or B:

P2V_SYNC_SOURCE = {P2V_SYNC_RED, P2V_SYNC_GREEN, P2V_SYNC_BLUE}

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

P_PIXEL_COLOR = IFC_RGB

P2V_MULTITAP_MODE = {P2V_SINGLE_TAP, P2V_2TAP_ILACE_FIXED}

Sync on Composite Sync

The VS and HS signals are extracted from the composite sync camera output signal and fed into the Sync Extractor to recover horizontal and vertical timing. This information is then used by the PLL to generate the Pixel Clock used by ADC. PC2-Vision supports an analog composite sync signal with a maximal voltage range from 0V to 5V.

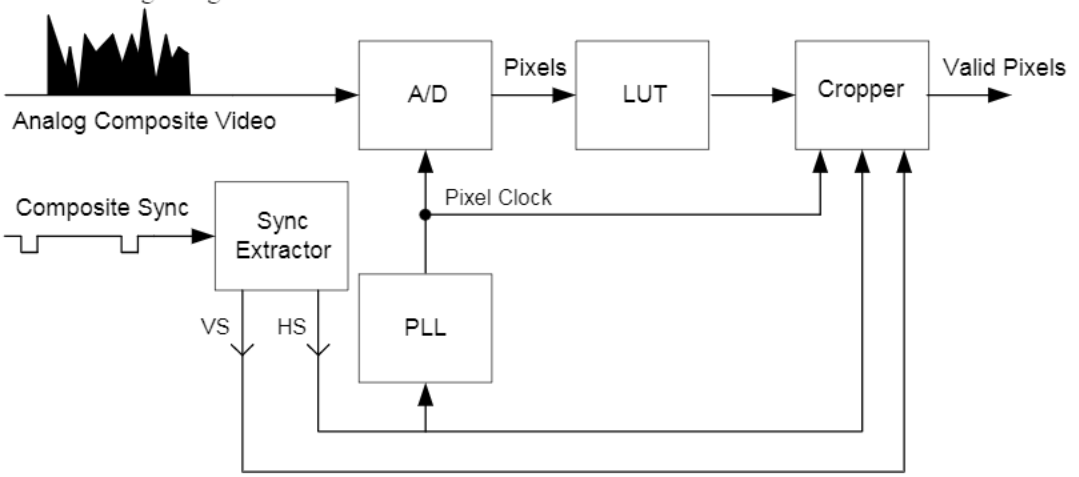


Figure 10: Composite Sync

This mode is generally used for RGB cameras. As such, two composite sync inputs are available on PC2-Vision: one on the first MDR-36 connector (J1) and one on the second (J2).

Sapera parameters for Sync on Composite Sync:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_COMP_SYNC

CORACQ_PRM_VIDEO = CORACQ_VAL_VIDEO_RGB

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Sync on Composite Sync:

P2V_SYNC_SOURCE = P2V_SYNC_COMPOSITE_SYNC

P_PIXEL_COLOR = IFC_RGB

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Sync on Separate Sync

In this mode the VS and HS signals are each input to the PC2-Vision. The Sync Extractor is bypassed. The PLL compares the separate horizontal sync input to the internal feedback and generates the PLL clock. The ADC uses the PLL clock to digitize the video input. The polarity of the sync inputs is programmable, allowing positive or negative polarity inputs (active-high or active-low signals). The incoming signals must be referenced to ground.

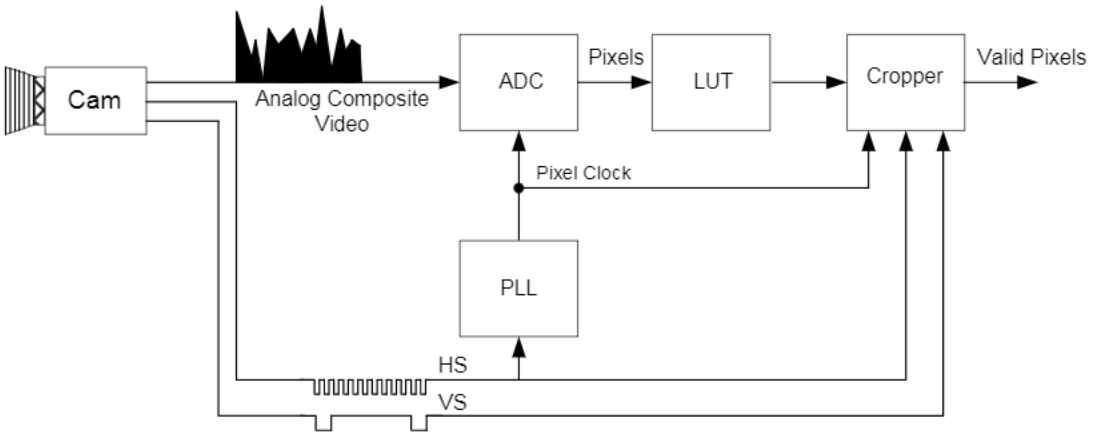


Figure 11: Separate Sync

Each camera has its own VS and HS pin. They are TTL level and are typically implemented using a LVT245 device.

Sapera parameters for Sync on Separate Sync:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_SEP_SYNC

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Sync on Separate Sync:

P2V_SYNC_SOURCE = P2V_SYNC_SEPARATE_SYNC

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Internal Sync

In Internal Sync (XTAL) mode, a clock generator is programmed to generate the desired pixel clock and time base signals. The Clock Generator produces separate horizontal and vertical sync signals that match the desired video format. These signals are then output to the camera. The frequency synthesizer can be programmed to generate any clock frequency up to 40MHz with less than 1ns jitter. In XTAL mode, the Clock Generator can be programmed to standard and non-standard camera timing.

The horizontal and vertical timing created by the Clock Generator is output to the camera as HD/VD signals: called Master Mode. It is also possible to deactivate the VD output so it does not reach the camera. In Master Mode, the PC2-Vision generates VD and/or HD to the camera if the source of synchronization used for digitization is Internal Sync.

Note that a PC2-Vision in Master Mode (that is, driving VD/HD) is independent from the selected source of synchronization. It is therefore possible for PC2-Vision to drive VD/HD to the camera, but still synchronize to the VS/HS present in the composite video signal.

PC2-Vision allows the same VD/HD to be sent to all six cameras simultaneously. This is useful to genlocked cameras together.

HD is used on some cameras to minimize jitter with respect to the frame reset signal. Note that for this to work successfully the HD edge must be aligned with frame reset (refer to camera user's manual). One HD signal is output per active camera.

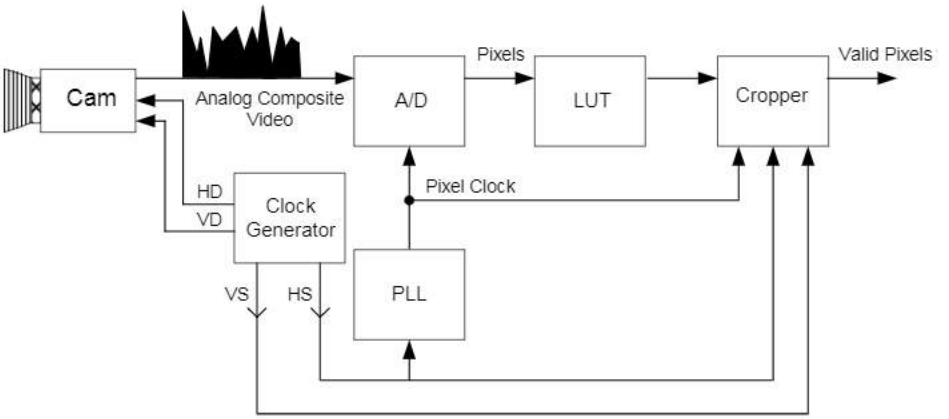


Figure 12: Internal Sync

When using Internal Sync, the horizontal reference for acquisition is HD. This is equivalent to a horizontal front porch of 0 pixels. The horizontal reference is used as a time reference to configure the clamping pulse delay and duration parameters.

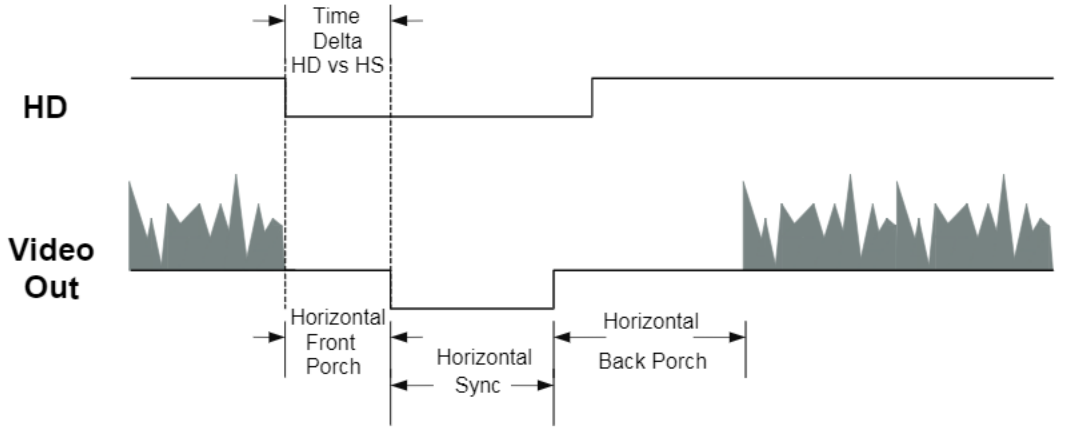


Figure 13: HD relation to HS

Each camera has its own VS and HS pin. They are 3.3V low-voltage TTL level and are typically implemented using a LVT245 device with the following electrical characteristics.

Electrical parameters	Description	Value
$V_{OH\ typ}$	Typical high-level output voltage	3.1V @ -100µA
$I_{OH\ max}$	Maximum high-level output current	-32mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	64mA (sinking)

Sapera parameters for Sync on Internal Sync:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_INT_SYNC

CORACQ_PRM_MASTER_MODE = CORACQ_VAL_MASTER_MODE_HSYNC_VSYNC

CORACQ_PRM_MASTER_MODE_HSYNC_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_MASTER_MODE_VSYNC_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' and the 'Advanced Control Parameters" tabs.



IFC parameters for Sync on Internal Sync:

P2V_SYNC_SOURCE = P2V_SYNC_INTERNAL_SYNC

P2V_MASTER_HSYNC = IFC_ENABLE

P_HSYNC_FREQ: Horizontal sync pulse frequency

P_HSYNC_WIDTH: Horizontal sync pulse width

P_HSYNC_POLARITY: Horizontal sync pulse polarity

P2V_VS_PULSE_ENABLE = IFC_VSYNC_LINE_WIDTH

P_VSYNC_FREQ: Vertical sync pulse frequency

P_VSYNC_WIDTH: Vertical sync pulse width

P_VSYNC_POLARITY: Vertical sync pulse width

P2V_VSYNC_OUT_ENABLE = {IFC_DISABLE, IFC_ENABLE}

P2V_SYNC_OUT_ALL_CONN = {IFC_DISABLE, IFC_ENABLE}

Note: With Asynchronous Reset mode and synchronization on Internal Sync, use P2V_VS_PULSE_ENABLE = IFC_VSYNC_DISABLE in order for the frame reset and internal VS pulse to be synchronized together. Otherwise, your image will shift vertically while grabbing since the Master Mode VS is not synchronized to frame reset.

WEN

Some cameras indicate when valid data is being delivered by generating WEN, or Write ENable. The function of WEN is similar to a vertical sync pulse. When enabled, the PC2-Vision uses WEN as the vertical timing reference instead of VS. Some cameras generate WEN, but with no VS pulse embedded inside the composite video signal.

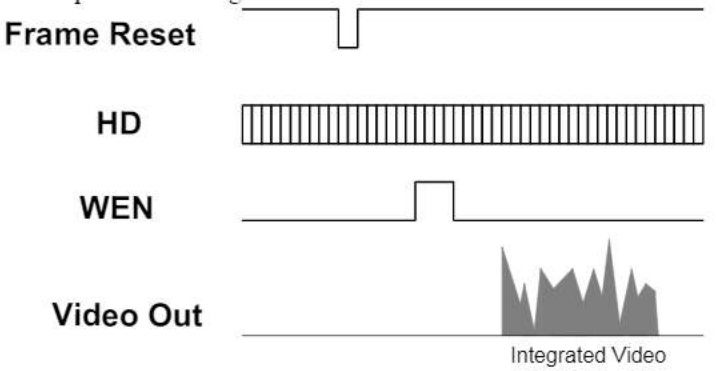


Figure 14: WEN

One WEN signal is available per connected camera. WEN has programmable polarity; it can be selected to be active high or active low. WEN input signal is TTL level and is typically implemented using a LVT244 device.

Sapera parameters for WEN :

CORACQ_PRM_WEN_ENABLE = {TRUE, FALSE}

CORACQ_PRM_WEN_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_VBACK_INVALID: Number of lines to skip for valid video after WEN pulse

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab.

IFC parameters for WEN :

P_WEN_ENABLE = IFC_ENABLE

P_WEN_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_WEN_VERTICAL_OFFSET: Number line to skip for valid video after WEN pulse

Variable Scan Mode

Variable Scan mode is similar to Separate Sync with the addition of a pixel clock signal. Variable Scan mode allows the camera to completely generate the timing information (HS, VS, and pixel clock). The incoming signals must be referenced to ground.

The Pixel Clock (rising edge TTL) is used by the ADC to sample the video signal. One pixel clock signal is available per MDR 36-pin connector. The minimum frequency rate is 7MHz and the maximum is 40MHz. Pixel clock signal supports a TTL voltage range from 0 to 5V.

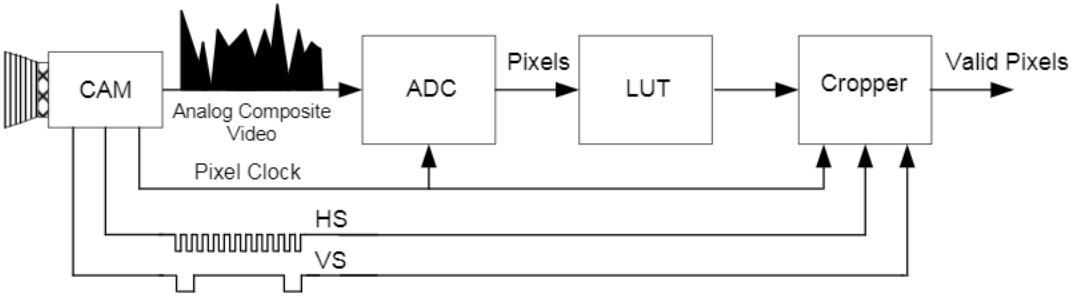


Figure 15: Variable Scan Mode

Sapera parameters for Variable Scan Mode:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_SEP_SYNC

CORACQ_PRM_PIXEL_CLK_SRC = CORACQ_VAL_PIXEL_CLK_SRC_EXT

CORACQ_PRM_PIXEL_CLK_EXT: External pixel clock frequency in Hz

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Variable Scan Mode:

P2V_SYNC_SOURCE = P2V_SYNC_SEPARATE_SYNC

P_PIXEL_CLK_SIGNAL_TYPE = P2V_PIXEL_CLOCK_EXTERNAL

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Camera Control

Pulse Generator

PC2-Vision has three independent timers that control pulse generation. This is necessary for camera control. This allows to position pulses precisely (to a resolution of 1µs) relative to the triggering event. This flexibility proves very handy considering the wide range of camera control modes (edge pre-select, pulse width control, E-Donpisha, etc.).

An independent timer is available for each of the following signals:

- VS
- Frame Reset
- Strobe

VS and Frame Reset timers can be combined to generate a double-pulse on the same camera pin. This is required for some camera modes, like long time exposure.

Each timer has the following capabilities:

- Programmable polarity (active high or active low)
- Programmable delay from trigger event (up to 65 seconds)
- Programmable duration (up to 65 seconds)

Timer granularity is 1µs when the delay and duration values are below 65ms. Granularity falls to 1ms for delay or duration above 65ms. Delay and duration always have the same granularity level.

Each timer can be started by any of the following events:

- VS
- External trigger
- Software trigger

VS is the default.

Frame Reset

Frame reset—also known as camera reset or camera trigger—is a signal sent by the PC2-Vision to the camera to trigger an acquisition. One frame reset signal is available per camera. The pulse duration and polarity are programmable. Frame reset can be triggered either by an external trigger signal, a software trigger or a VS. After the trigger is initiated, an internal frame reset counter counts up to 65 seconds. This pulse is normally used to control the exposure of the camera CCD (Edge Pre-Select mode or Pulse Width Control mode). The frame reset output signal is 3.3V low-voltage TTL. It is typically implemented using a LVT244 device with the following electrical characteristics.

Electrical parameters	Description	Value
$V_{OH\ typ}$	Typical high-level output voltage	3.1V @ -100µA
$I_{OH\ max}$	Maximum high-level output current	-32mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	64mA (sinking)

Two parameters control the frame reset pulse. First, the offset indicates the delay from the trigger before asserting frame reset. Then, the size specifies the time the frame reset pulse is asserted. The duration of the pulse controls the exposure period on some cameras.

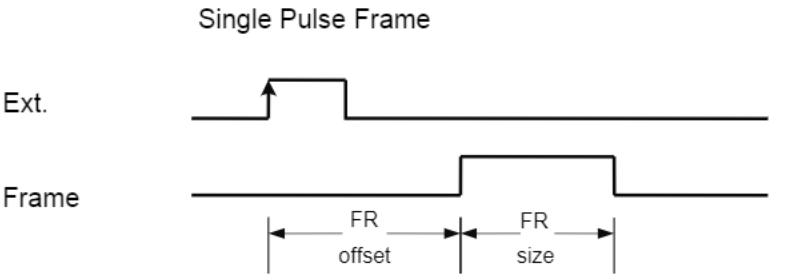


Figure 16: Single pulse frame reset

Warning: Some cameras have frame reset located on pin 9 of the Hirose-12 connector while other cameras have it on pin 11. It is imperative to use the appropriate camera cable that matches the frame reset pinout. Failure to do so could result in board damage.

PC2-Vision provides an additional protection circuit that inhibits an erroneous connection of the frame reset pin, preventing a 12V power level damaging the frame reset output. Nevertheless, it is not recommended to put a 12V level on the frame reset pin.

Sapera parameters for Frame Reset :

Refer to Time Integration method of Sapera documentation.

CORACQ_PRM_TIME_INTEGRATE_METHOD: Method to use for time integration

CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY: Pulse offset from trigger event

CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION: Size of pulse

CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

Note: Frame reset pulse is always aligned on HS in Sapera.

CamExpert: parameters are located under the 'Advanced Control Parameters' tab.

Under IFC, Frame Reset shares the VS parameters to create a double pulse. A control is offered to add VS to frame reset. In this case, both pulses will be sent to the frame reset pin. Then, it is only a matter of providing the appropriate offset and size for Frame Reset and VS. The distance between the first and second pulse controls the exposure period on some cameras.

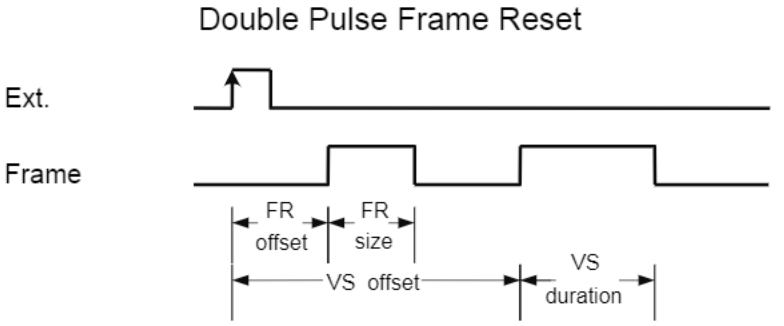


Figure 17: Double pulse frame reset for IFC

IFC parameters for Frame Reset :

P_FRAME_RESET_MODE = IFC_ENABLE

P_FRAME_RESET_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_FRAME_RESET_OFFSET: Pulse offset from trigger event

P_FRAME_RESET_SIZE: Size of pulse

P2V_ADD_FRAME_RESET_TO_VSYNC = {IFC_DISABLE IFC_ENABLE}

P_FRAME_RESET_ALIGN_ON_HS = {IFC_DISABLE, IFC_ENABLE}

VSync

One VS signal is output per active camera. This feature is used on some cameras to control the exposure rate when in Master Mode (XTAL). The VS can generate up to two pulses, each with a different duration up to 65 seconds. VSync output signal is 3.3V low-voltage TTL level. It is typically implemented using a LVT245 device.

Two parameters control the VS pulse. First, the offset indicates the delay from the trigger before asserting VS. Then, the duration specifies the time the VS pulse is asserted.

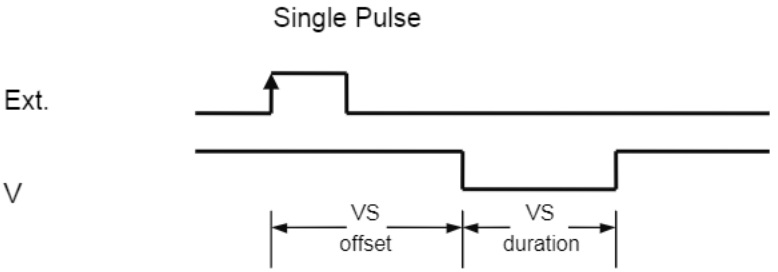


Figure 18: Single pulse VS

Sapera parameters for VSync :

Refer to Time Integration method of Sapera documentation

CORACQ_CAP_TIME_INTEGRATE_METHOD: Method to use for time integration

CORACQ_PRM_TIME_INTEGRATE_PULSE_DELAY: Pulse offset from trigger event

CORACQ_PRM_TIME_INTEGRATE_PULSE_DURATION: Size of pulse

CORACQ_PRM_TIME_INTEGRATE_PULSE_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

Note: VSync pulse is always aligned on HS in Sapera.

CamExpert: parameters are located under the 'Advanced Control Parameters' tab.

Under IFC, VS shares the frame reset parameters to create a double pulse. A control is offered to add Frame Reset to VS. In this case, both pulses will be sent to the VS pin. Then, it is only a matter of providing the appropriate offset and duration for VS and Frame Reset.

Figure 19: Double pulse VS for IFC

IFC parameters for VSync :

P2V_VS_PULSE_ENABLE = P2V_VSYNC_TIME_WIDTH

P_VSYNC_FREQ: Frequency of VSync pulse

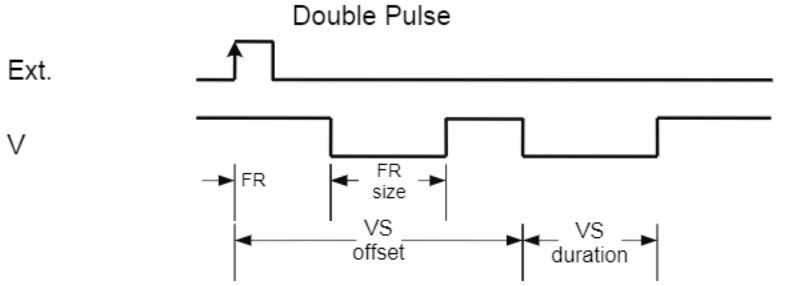
P_VSYNC_WIDTH: Width of VSync pulse

P_VSYNC_POLARITY = { IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_ADD_VSYNC_TO_FRAME_RESET = {IFC_DISABLE, IFC_ENABLE}

P2V_VSYNC_ALIGN_ON_HS = {IFC_DISABLE, IFC_ENABLE}

P2V_VSYNC_OUT_ENABLE = {IFC_DISABLE, IFC_ENABLE}



External Trigger and Strobe

External Trigger

External Trigger allows image acquisition to be synchronized to external events. When acquiring an image in External Trigger mode, the acquisition will not start until the PC2-Vision receives a trigger signal. Acquisition begins with the next valid frame after the trigger.

One external trigger signal is available per MDR 36-pin connector. The external trigger is protected by an opto-coupler. The external trigger can be driven by any voltage source from 3.3V low-voltage TTL up to 24V, as long as it can provide at least 2mA.

The incoming trigger pulse is "debounced" to ensure that no glitch would be detected as a valid trigger pulse. This debouncer can be programmed from 0µs to 255µs. Any pulse smaller than the programmed value will be blocked and therefore not be seen by the acquisition circuitry.

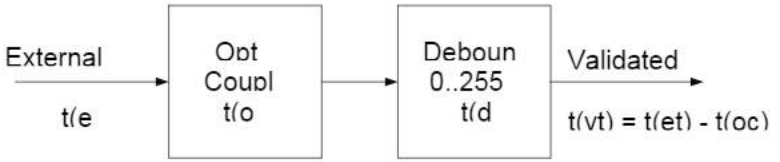


Figure 20: External Trigger

Let t(et) = time of external trigger in µs
t(vt) = time of validated trigger in µs
t(oc) = time opto-coupler takes to change state
t(d) = debouncing duration from 0 to 255µs

For an active high external trigger, t(oc) = 10µs:
t(vt) = t(et) – 10µs – t(d)

For an active low external trigger, t(oc) = 50µs:
t(vt) = t(et) – 50µs – t(d)

Note: DALSA recommends using a rising edge external trigger in order to minimize the time it takes for the opto-coupler to change state. That is, the opto-coupler response time is 10µs for rising edge compared to 50µs for falling edge. DALSA also recommends putting a debouncing duration of at least 1µs to guaranty that opto-coupler transitions cannot be falsely detected by the TTL logic.

If t(vt)> 0, then a valid trigger is detected and acquisition is fired. Therefore, the external pulse with rising edge polarity must be at least 10µs (if debouncer is set to 0) in order to be acknowledged. Any pulse larger than 265µs is always considered valid.

It is possible to emulate an external trigger using the software trigger. The latter is generated by a function call from the application.

External trigger is supported using two pins: Ext_Trigger- and Ext_Trigger+. RS-422 level can be directly connected to those pins. When using TTL level, connect the Ext_Trigger- to ground and drive Ext_Trigger+ with the TTL trigger.

The PC2-Vision external trigger interfaces to the external world through the use of an opto-coupled device. Formed by an LED emitter combined with a photodetector in close proximity, an opto-coupler (or opto-isolator) connects the PC2-Vision external trigger and the user circuit together while using separate grounds. This "galvanic isolation" approach prevents ground loops and protects both circuits. A serial resistor of 650Ω is connected in serial to the opto-coupler to limit the current.

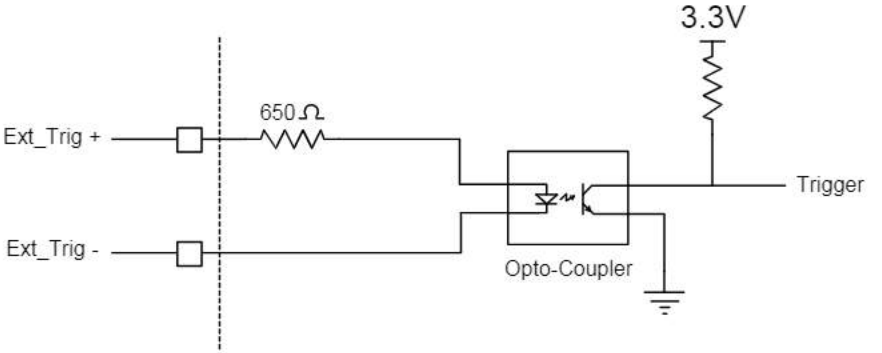


Figure 21: Opto-coupler

When current flows inside the LED, the emitted light acts as a base current for the transistor. Depending on the amount of light being emitted, the transistor can be turned ON just like a switch. Data in the form of a voltage is transmitted on one side to the other like a transistor being ON or OFF. The opto-coupler input is an inverting circuit, but the PC2-Vision software compensates for this when specifying the polarity.

The surrounding circuit that converts the voltage to flow as a current into the LED is therefore crucial to the good performance of the opto-coupler. The emitted light will not turn the transistor ON if the current flowing through the LED is too small. The opto-coupler on the PC2-Vision is typically a Fairchild HMHA281 with the following characteristics:

Electrical parameters	Description	Value
$V_{IL\ max}$	Maximum voltage difference to turn OFF	0.8 V
$V_{IH\ min}$	Minimum voltage difference to turn ON	2 V
$I_{I\ min}$	Minimum input current to turn ON	2 mA
$I_{I\ max}$	Maximum input current to turn ON	50 mA
$t_{I\ min}$	Minimum input pulse width to turn ON	10 us
$V_{f\ max}$	Maximum forward voltage	24 V
$V_{r\ max}$	Maximum reverse voltage	-25 V

Note: TTL signals are approximately 0 and 3.3/5V, corresponding to logical 0 and 1, respectively. A standard TTL output can sink 16mA and could be used as a sink to drive an opto-coupled input. That is, +5V is connected to Ext_Trig+ and the sink trigger source is connected to Ext_Trig-. This will normally require the application to invert the polarity of the trigger in the camera configuration file.



Sapera parameters for External Trigger:

CORACQ_PRM_EXT_TRIGGER_ENABLE = CORACQ_VAL_EXT_TRIGGER_ON

CORACQ_PRM_EXT_TRIGGER_SOURCE = {0: Same connector as video source, 1: first MDR-36, 2: second MDR-36}

CORACQ_PRM_EXT_TRIGGER_DETECTION = {CORACQ_VAL_RISING_EDGE, CORACQ_VAL_FALLING_EDGE, CORACQ_VAL_ACTIVE_LOW. CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_EXT_TRIGGER_DURATION: Debouncing duration

CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT: Number of frame to acquire per trigger

Note: CORACQ_PRM_EXT_TRIGGER_LEVEL always represents the opto-coupler trigger input independent of its actual value (CORACQ_VAL_LEVEL_TTL or CORACQ_VAL_LEVEL_422). This means this parameter "does not matter" for the PC2-Vision driver.

In CamExpert, these parameters are located under the 'External Trigger Parameters' tab.



IFC parameters for External Trigger:

P_TRIGGER_ENABLE = IFC_ENABLE

P_TRIGGER_SRC = {IFC_SOFT_TRIG, IFC_EXT0_TRIG, IFC_EXT1_TRIG, IFC_EXT_AUTO_TRIG}

P_GEN_SW_TRIGGER = {0, 1}

P_TRIGGER_POLARITY = {IFC_FALLING_EDGE, IFC_RISING_EDGE}

P_FRAMES_PER_TRIGGER: Number of frames to acquire per trigger

P_TRIGGER_DEBOUNCE: Debouncing duration

P2V_VSYNC_WAIT_COUNT: Number of VS to count before acquiring after a trigger

Strobe

One strobe signal is output per MDR 36-pin connector. The pulse duration and polarity are programmable (up to 65 seconds).

The strobe signal is achieved using a LVT244 driver with the following electrical characteristics:

Electrical parameters	Description	Value
$V_{OH\ typ}$	Typical high-level output voltage	3.1V @ -100µA
$I_{OH\ max}$	Maximum high-level output current	-32mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	64mA (sinking)

Sapera parameters for Strobe :

Refer to Strobe Method in Sapera documentation

CORACQ_PRM_STROBE_ENABLE = TRUE

CORACQ_PRM_STROBE_LEVEL = CORACQ_VAL_LEVEL_TTL

CORACQ_PRM_STROBE_METHOD = {CORACQ_VAL_STROBE_METHOD_1, CORACQ_VAL_STROBE_METHOD_2}

CORACQ_PRM_STROBE_POLARITY = {CORACQ_VAL_ACTIVE_LOW

, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_STROBE_DELAY: Pulse offset from trigger event

CORACQ_PRM_STROBE_DELAY_2: Duration of exclusion region

CORACQ_PRM_STROBE_DURATION: Pulse duration

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab.

Under IFC, PC2-Vision offers two types of strobes: Fast Strobe (equivalent to Strobe Method 1 of Sapera) and Slow Strobe. Fast strobe occurs immediately after the trigger. See below for diagram. The first falling edge of the trigger immediately generates a strobe pulse. The strobe pulse duration is programmable. This mode is often used with asynchronous reset cameras.

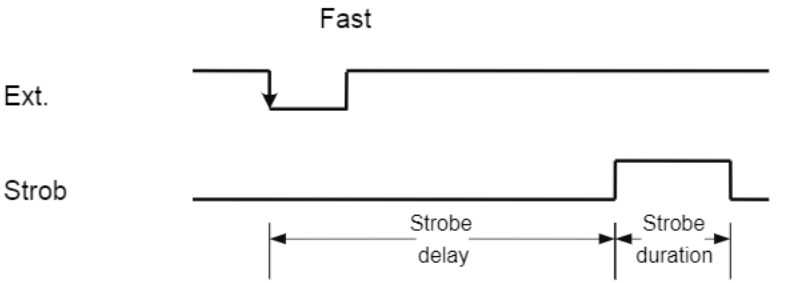


Figure 22: IFC Fast Strobe

Note: PC2-Vision does not support an exclusion region in Fast Strobe mode. Strobe delay parameter represents the time from the external trigger to strobe pulse assertion.

In Slow Strobe mode, the strobe pulse occurs after a certain delay following the VS and the trigger, respectively. Strobe duration is programmable. See below for diagram. Basically, the strobe pulse is asserted from the first VS following the trigger. This mode is often used with free-running cameras.

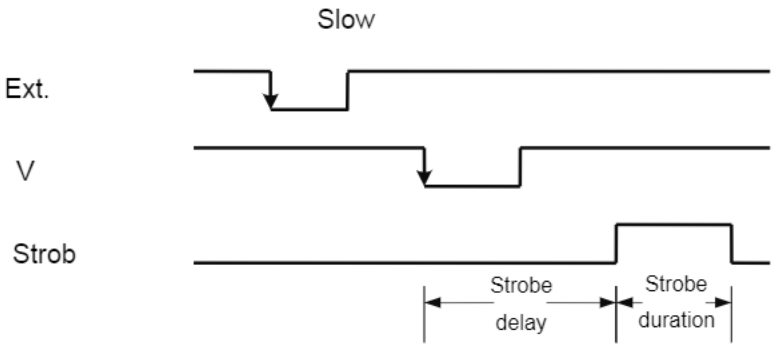


Figure 23: IFC Slow strobe

IFC parameters for Strobe :

P_STROBE_ENABLE = IFC_ENABLE

P_STROBE_MODE = {IFC_FAST_STROBE, IFC_SLOW_STROBE}

P_STROBE_POLARITY = {IFC_ACTIVE_HIGH, IFC_ACTIVE_LOW}

P_STROBE_DELAY: Pulse offset from trigger event

P_STROBE_DURATION: Pulse duration

P_STROBE_ALIGN_ON_HS = {IFC_DISABLE, IFC_ENABLE}

Serial Port

PC2-Vision hosts a serial port UART that can be dynamically mapped to the first or second MDR-36 connector. Therefore, you have two Rx/Tx pairs available from PC2-Vision (even though they both are driven from the same physical UART).

This serial port is intended for camera control.

Default name for this serial port is: **PC2-Vision_*X*_Serial_0**, where *X* represents the PC2-Vision board number, from 1 to 8.

Note: A typical configuration would use 9600 baud•8-bit•no parity•1 stop bit (9600-8-N-1).

Note: After booting your computer, you must run an IFC or a Sapera application, such as the Configurator® or CamExpert, to make the serial port accessible. This is required to initialize resources on the PC2-Vision.

Ports can be used with their default names (for example: PC2-Vision_1_Serial_0) by many camera control applications. Additionally, the serial port can be mapped as a standard Windows COMx port for convenience or compatibility with any communication program (such as HyperTerminal).



Sapera parameters for Serial Port

In Sapera, the serial port is mapped as a regular COM Port. It can be configured through WIN32 API.

Note: In Sapera, the serial port selection always follows the current video source.



IFC parameters for Serial Port

P2V_SELECT_UART_PORT = { P2V_UART_PORT_AUTO, P2V_UART_PORT_CON1, P2V_UART_PORT_CON2}

P_COM_PORT_NAME : String that specifies serial port name

P_COM_PORT_BYTESIZE = {IFC_COM_7BITS, IFC_COM_8BITS}

P_COM_PORT_BAUDRATE = {IFC_BAUD_4800, IFC_BAUD_9600, IFC_BAUD_14400, IFC_BAUD_19200, IFC_BAUD_38400, IFC_BAUD_56000, IFC_BAUD_57600, IFC_BAUD_115200, IFC_BAUD_128000}

P_COM_PORT_PARITY = {IFC_NOPARITY, IFC_ODDPARITY, IFC_EVEN_PARITY}

P_COM_PORT_STOPBITS = {IFC_ONE_STOPBIT}

IFC uses those parameters to communicate with the serial port in the following two cases:

- when the application calls **CICamera::WriteUartCommand()**.

- when IFC uses the rule evaluation from the config file.

Camera Selection (MUX)

The PC2-Vision communicates with the camera through two MDR 36-pin connectors located on the bracket. Each connector can support up to three monochrome, one RGB, or one dual-channel camera(s). Up to six monochrome, two RGB, or two dual-channel cameras, therefore, can be connected to the PC2-Vision at the same time. But only one MDR-36 connector is MUXed to the ADC.

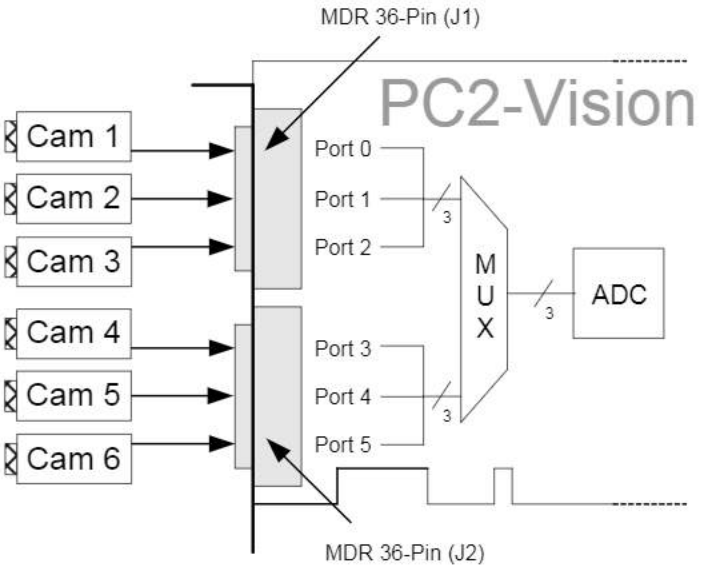


Figure 24: Six monochrome connections

The PC2-Vision can also genlock monochrome cameras attached to the same MDR-36-pin connector and digitize data simultaneously. A 12V power pin (500mA) is supported for each camera (fuse protected). Note that the J6 connector on the PC2-Vision must be connected to a floppy power cable to provide 12V to the cameras. Refer to the "PC2-Vision component view" (on page 74) section for connector locations.

The input is selected by the software control. The timing is common to all three inputs. Independent timing is not available. Asynchronous inputs are not supported by the PC2-Vision. The timing and synchronization settings apply to all three channels synchronously. Multiple monochrome cameras must be externally genlocked or driven by the PC2-Vision timing (see "Internal Sync" on page 34).

PC2-Vision Input	Monochrome Camera	RGB Camera
video 1	CAM 1	CAM1 blue
video 2	CAM 2	CAM1 green
video 3	CAM 3	CAM1 red
video 4	CAM 4	CAM2 blue
video 5	CAM 5	CAM2 green
video 6	CAM 6	CAM2 red

IFC Port	Monochrome Camera	RGB Camera	Dual-Channel Camera
0	CAM 1	CAM1 blue	CAM1 even field
1	CAM 2	CAM1 green	CAM1 odd field
2	CAM 3	CAM1 red	Not used
3	CAM 4	CAM2 blue	CAM2 even field
4	CAM 5	CAM2 green	CAM2 odd field
5	CAM 6	CAM2 red	Not used

For RGB or dual-channel cameras, use IFC port 0 for J1 MDR-36 or port 3 for J2 MDR-36 to control the camera in the application source code.

Anti-aliasing Filter

Following the MUX stage, the video passes through a selectable low-pass filter, optimized for standard video frequencies. The filter values are 6MHz and 12MHz, with the possibility to bypass filters. All three channels are selected together; independent low-pass selection not available. The low-pass filter strips high frequency signal content from the incoming video signal, to avoid sampling aliasing artifacts in the signal. Standard video (RS-170, CCIR) has useful frequency content up to approximately 6MHz. Frequencies above this can be eliminated using the low-pass filters. Sampling rates for standard video are 10MHz (up to 14MHz). If frequencies at or above the sampling rate are present, they represent noise rather than useful video. These frequencies can "alias" into the real video signals causing corruption. The low-pass filters can eliminate any high frequency signal content before digitization.

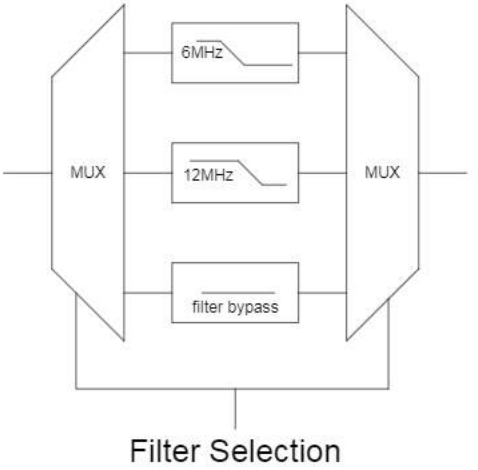


Figure 25: Anti-Aliasing Filter

Sapera parameters for Anti-aliasing Filter:

CORACQ_PRM_FIX_FILTER_ENABLE = {TRUE, FALSE}

CORACQ_PRM_FIX_FILTER_SELECTOR = {0 for 6 MHz, 1 for 12 MHz}

Note: Bypass filter is selected when CORACQ_PRM_FIX_FILTER_ENABLE = FALSE.

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab under the 'Analog Signal Conditioning' entry.

IFC parameters for Anti-aliasing Filter:

P2V_LOW_PASS_FILTER = { P2V_LPF_6_5_MHZ, P2V_LPF_12_MHZ, P2V_LPF_BYPASS}

Contrast and Brightness Adjustment

Contrast and Brightness are controlled through the input gain of the ADC; the PC2-Vision was calibrated during the manufacturing process to support this feature.

Brightness controls the offset of the digitization line while contrast controls its gain (the slope of the line). See below for diagram. The vertical axis represents the voltage level of the incoming video signal (black level is 53mV, white level is 714mV in NTSC) while the horizontal axis shows the resulting pixel value. For instance, using default brightness and contrast, an incoming video signal of 350mV gets digitized into a value of 115. By increasing the brightness, the digitization line gets shifted down, which creates a brighter image (same input voltage leads to a higher pixel value). Decreasing brightness leads to a darker image. Note that changing the brightness only affects the offset of the digitization line, not its slope. This latter attribute is controlled through contrast. By increasing contrast, the slope of the digitization line is decreased, which lowers the voltage difference between two consecutive pixel values.

Default values of brightness and contrast use the full resolution of the ADC for a standard RS-170 source.

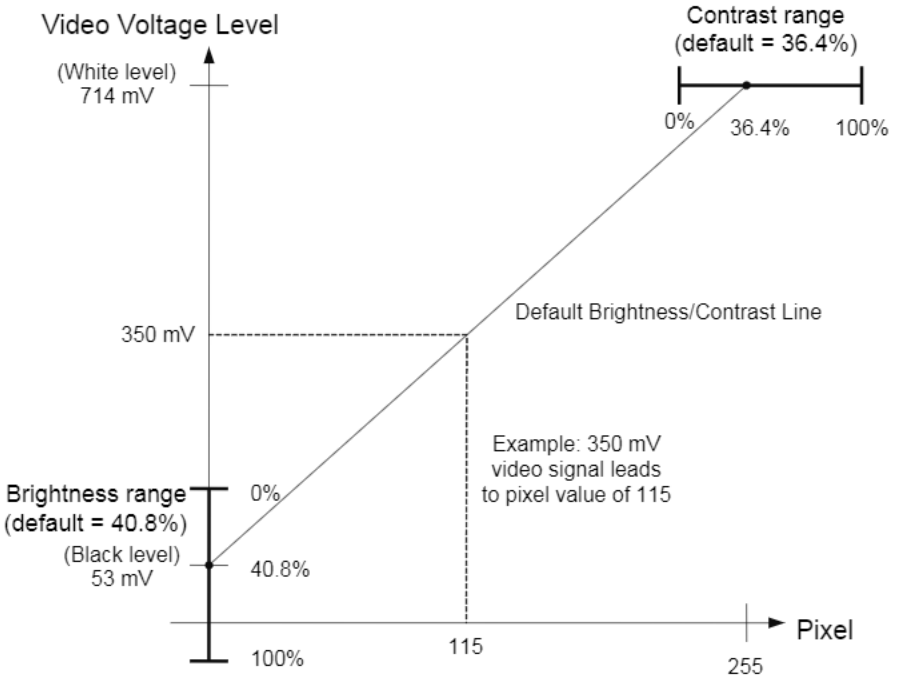


Figure 26: Video voltage level

Sapera parameters for Contrast and Brightness :

CORACQ_PRM_CONTRAST: Contrast percentage

CORACQ_PRM_BRIGHTNESS: Brightness percentage

CORACQ_PRM_VIDEO_LEVEL_MIN: Minimum value (in µV) of the video signal

CORACQ_PRM_VIDEO_LEVEL_MAX: Maximum value (in µV) of the video signal

Note: Under Sapera, contrast percentage ranges from 60% to 170% with 100% being the default value. Brightness percentage ranges from –20% to 29% with 0 % being the default value. Typically, you do not need to adjust the default contrast and brightness if the video level min and video level max parameters matches your camera.

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab under the 'Analog Signal Conditioning' entry.

IFC parameters for Contrast and Brightness :

P_CONTRAST: Contrast percentage

P_BRIGHTNESS: Brightness percentage

Note: Under IFC, contrast percentage and brightness percentage are normalized from 0% to 100%.

AD Converter

The PC2-Vision uses a 40MHz triple ADC (Analog to Digital Converter). The triple ADC outputs three 8-bit unsigned binary values from 0x0 to 0xFF based on: the sampled analog input signal level, the ADC sampling window of each input channel, and by the clamping voltage level (independent for each channel). The Pixel Clock used by the ADC comes from one of three sources: the PLL clock (PLL mode), the Clock Generator (XTAL mode), or the externally input Variable Scan Clock (Vscan mode).

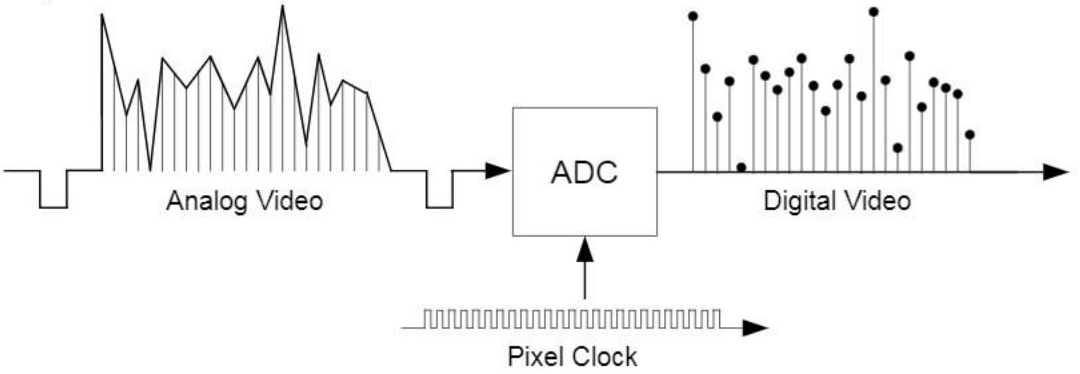


Figure 27: AD Converter

The Pixel Clock is used to sample incoming video signal at the specified frequency. The result is a series of 8-bit digital values representing the analog video signal.

DC Restoration

DC Restoration uses a programmable clamp pulse. It uses the horizontal back porch to establish the reference black video level.

Two parameters are required to indicate the location of the region used as the reference. The *clamp_start* and *clamp_end* parameters refer to the HS edge. The *clamp_width* is the time difference between *clamp_start* and *clamp_end*. See below for diagram.

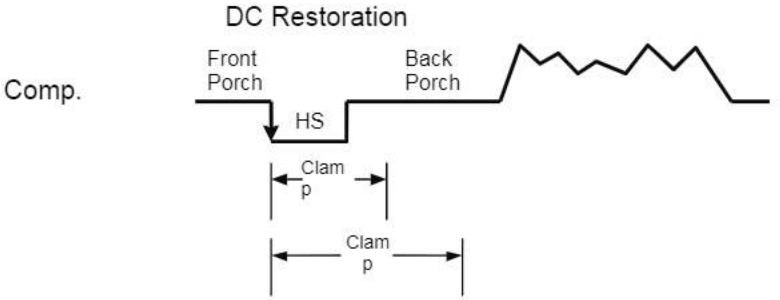


Figure 28: DC restoration

Note: With Internal Sync mode, the horizontal reference is the edge of HD, as shown in "Figure 13: HD relation to HS" (on page 35). With this synchronization scheme, clamp start and clamp end values refer to first edge of HD, not to HS coming from composite video.

Sapera parameters for ADC Converter:

CORACQ_PRM_PIXEL_CLK_INT: Internal pixel clock frequency (in Hz)

CORACQ_PRM_PIXEL_DEPTH = 8

CORACQ_PRM_DC_REST_MODE = { CORACQ_VAL_DC_REST_MODE_AUTO , CORACQ_VAL_DC_REST_MODE_ON, CORACQ_VAL_DC_REST_MODE_OFF}

CORACQ_PRM_DC_REST_START: Start of clamp pulse relative to HS or HD

CORACQ_PRM_DC_REST_WIDTH: Clamp pulse duration

In CamExpert, DC restoration parameters are located under the 'Advanced Control Parameters' tab under the 'Analog Signal Conditioning' entry.

IFC parameters for ADC Converter:

P_PIXEL_CLK_FREQ: Pixel clock frequency

P_PIXEL_SIZE = 8

P_CLAMP_MODE = IFC_ENABLE

P2V_CLAMP_START: Start of clamp pulse relative to HS or HD

P2V_CLAMP_END: End of clamp pulse relative to HS or HD

Lookup Table

A different LUT is assigned to each of the six monochrome inputs. (for a total of six independent LUTs). It operates at the resolution of 8-bits in and 8-bits out. The Lookup Table can be used for point transfer as well as for thresholding.

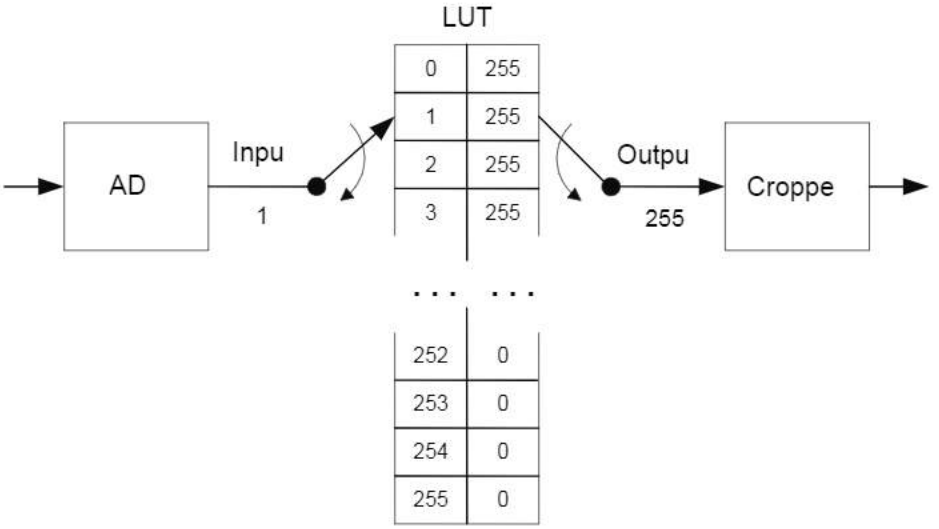


Figure 29: Lookup Table Example

Sapera parameters for Lookup Table:

CORACQ_PRM_LUT_ENABLE = {TRUE, FALSE}

CORACQ_PRM_LUT_FORMAT = CORACQ_VAL_OUTPUT_FORMAT_MONO8

CORACQ_PRM_LUT_MAX = 1

CORACQ_PRM_LUT_NENTRIES = 256

CORACQ_PRM_LUT_NUMBER = 0

Use **CorAcqSetLut()** to load a LUT into PC2-Vision.

CamExpert does not provide direct access to these parameters. They must be activated programmatically from your Sapera application via the SapLut class.

IFC parameters for Lookup Table:

P_INPUT_LUT1_FILE: filename for LUT

Cropper

The Cropper extracts a window from the incoming image. This window is represented by a rectangle where the upper-left corner is given by horizontal and vertical offset from the start of valid video and the rectangle size by width and height parameters. See below for diagram. Note that image widths must be a multiple of four bytes. For interlaced scan camera, image heights must be a multiple of two lines.

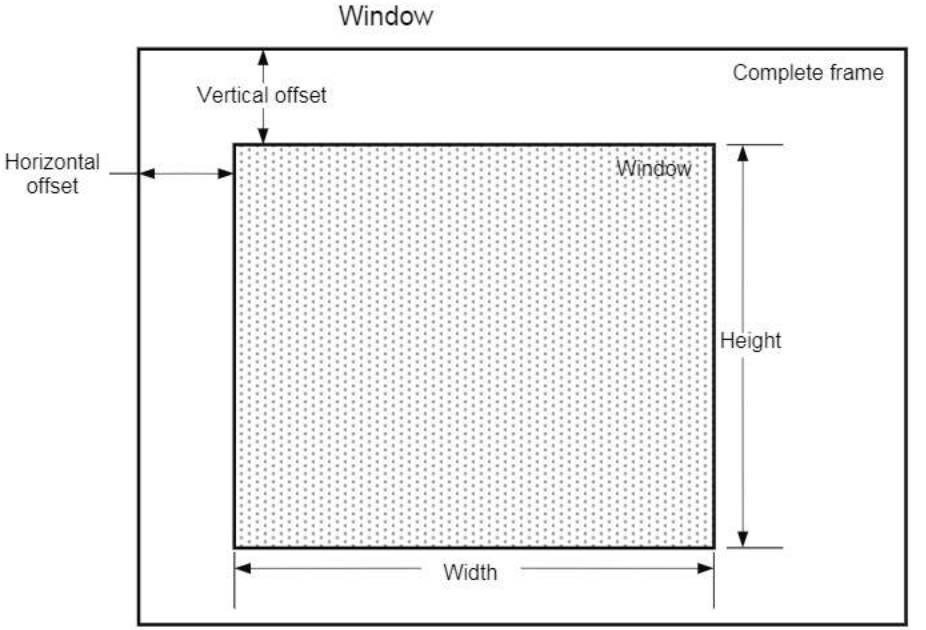


Figure 30: Window generator

Most of the time, the Cropper is configured to let the whole image pass through, that is no special region of interest is defined. This means the horizontal and vertical offset are left to their default value of 0.

Partial Scan Mode

Partial Scan mode reduces the number of lines output by a camera in order to increase the frame rate. PC2-Vision sees the output of a partial scan camera as an image with reduced height. One simply needs to adjust the frame rate (vertical sync frequency) and image height in order to acquire from a partial scan mode camera.

Sapera Parameters for Cropper:

CORACQ_PRM_CROP_LEFT: Horizontal offset

CORACQ_PRM_CROP_HEIGHT: Vertical height of area of interest

CORACQ_PRM_CROP_TOP: Vertical offset

CORACQ_PRM_CROP_WIDTH: Horizontal width of area of interest

In CamExpert, these parameters are located under the 'Image Buffer and AOI Parameters' tab.

IFC Parameters for Cropper:

P_HORZ_OFF: Horizontal offset

P_WIDTH_PIXELS: Horizontal width of area of interest

P_VERT_OFF: Vertical offset

P_HEIGHT_PIXELS: Vertical height of area of interest

Decimator

Decimation is performed horizontally and vertically by a factor of two, four, or eight. Decimation is useful in reducing memory consumption, lowering PCI bandwidth usage as well as being an easy way to scale an image. Note that horizontal and vertical decimation work independently of each other.

Horizontal decimation is accomplished by dropping pixels. See below for diagram. Only the first pixel of each pair is kept for a horizontal decimation factor of 2.

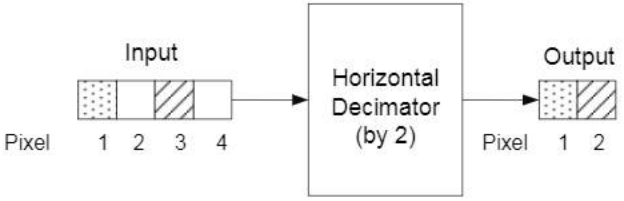


Figure 31: Horizontal decimator

Note: Horizontal decimation can be used to lower the effective pixel clock sampling rate below 7MHz. To perform this, double the pixel clock rate and activate horizontal decimation. This allows an application to grab with a pixel clock as low as 3.5 MHz.

Vertical decimation is performed by dropping lines. See below for diagram. Only the first line of each pair is kept for a vertical decimation factor of 2.

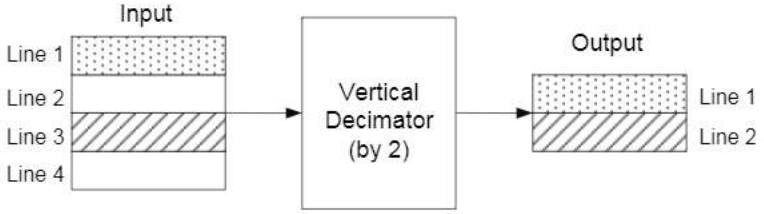


Figure 32: Vertical decimator

IFC Support for Decimator:

Use CICamera::SetZoom().

Onboard Memory

The onboard memory behaves as a temporary buffer between the camera interface and the host PCI-bus system. The total onboard memory capacity is 8MB. There is a maximum frame size of 2K x 2K for monochrome data or 1K x 1K for RGB. Two frames can be securely stored within onboard memory for double buffering. Total bandwidth to onboard memory is 320MB/second (40MHz x 4 bytes x 2 directions (IN/OUT)). Onboard memory allows the capture from cameras requiring a bandwidth exceeding the PCI theoretical maximum of 132MB/second.

The following pixel formats are supported in onboard memory:

1. 32-bit packed (for single monochrome camera)

pixel 4		pixel 3		pixel 2		pixel 1	
31	24	23	16	15	8	7	0

2. 32-bit zero padded (for three genlocked cameras as well as RGB). This pixel format allows planar transfer (see Planar Converter section on page 59).

0		CAM3 or R		CAM 2 or G		CAM1 or B	
31	24	23	16	15	8	7	0

YCrCb Engine

The YCrCb Engine converts an 8-bit monochrome image into a 16-bit padded YCrCb image to display in overlay (Windows secondary surface). The engine places the value 0x80 in chrominance. This value is added during the PCI transfer to free onboard memory from chrominance data. Furthermore, the YCrCb Engine eliminates CPU involvement when copying host buffers into display by transferring directly into overlay, bypassing the CPU.

YCrCb Engine is only available for monochrome cameras.

Sapera Support for YCrCb Engine:

YCrCb engine is not supported in current version of PC2-Vision Sapera driver.

IFC Support for YCrCb Engine:

Create an image connection using `IfxCreateImgConn()` with the flag IFC_YCRCB_SINK or use IfxCreateImgSink() with the YCRCB_SINK flag.

Planar Converter

The Planar Converter extracts RGB color components into three different buffers during PCI transfer to facilitate image processing (see the diagram below). It can also be used with three genlocked monochrome cameras.

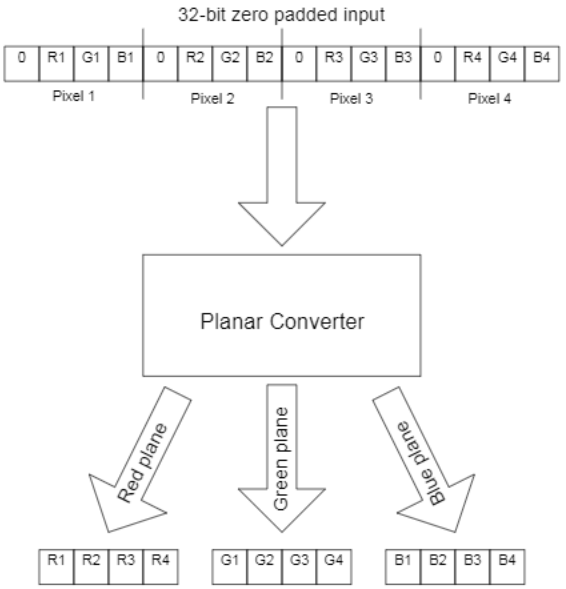


Figure 33: Planar converter

Sapera parameters for Planar Converter:

CORACQ_PRM_CAMSEL: Index of camera selector to take timing from.

CORACQ_PRM_PLANAR_INPUT_SOURCES: Flag indicating input sources to simultaneously acquire from. Bit 0 represents video1, bit 1 represents video 2 and so on.

Note: In Sapera, the planar converter is used to acquire from up to 3 genlocked monochrome cameras.

In CamExpert, these parameters are located under the 'Multi-Camera Control Parameters' tab.

IFC parameters for Planar Converter:

P_PIXEL_COLOR = IFC_RGB_PLANAR

P2V_PLANAR_MODE = {P2V_PLANAR_DISABLED, P2V_PLANAR_HORZ, P2V_PLANAR_VERT}

When using the grab option IFC_GOPT_PLANAR_INIT, CICamera::Grab must be called to start three concurrent grabs on all three channels offered by one connector. The acquisition does not actually start until the third CICamera::Grab call is made.

PCI Controller

The PCI controller has scatter-gather support to reduce CPU usage to a minimum. It retrieves a buffer descriptor list from host memory. It also supports packed data and planar data. Each color component can have a different scatter/gather list in RGB. This is also true for three genlocked cameras.

The PCI controller can sustain an average transfer rate up to 100 MB/second with bursts of 132 MB/second.

Parallel I/O

PC2-Vision provides digital I/O capability for controlling or monitoring external events. The digital input and output lines, which are available on a 26-pin header at the top of the board, can be cabled to a 25-pin D-Sub connector that occupies an open slot in the PC chassis. The functionality of the I/O port is as follows:

- IN(7-0): Eight digital TTL input lines provide capability to read these as either raw or latched (by STROBE_I) inputs. Each input pin can generate a dedicated interrupt (programmable edge).
- OUT(7-0): Eight digital TTL output lines driven by a programmable register.
- STROBE_I: Input strobe signal can be used to latch the 8-bit input data (if this mode is selected). The polarity of STROBE_I is programmable.
- STROBE_O: Output strobe signal is an output line under software control.
- I/O_INT: An interrupt input line that can be used to generate an interrupt (programmable edge)

Refer to "J3: Parallel I/O 26-Pin Dual-Row Connector" section (on page 76) for the pinout of this connector. A bracket assembly (part number 4816) is available to cable the Parallel I/O pins to a female DB25.

The Parallel I/O is backward compatible with PCVision and it has the ability to provide power to an external box: 2 dedicated 5V, 500mA power pins (with fuse protection) are available.

The Parallel I/O is achieved using HCT244 drivers with the following electrical characteristics. Note that this is a 5V TTL device.

Electrical parameters	Description	Value
$V_{IH\ min}$	Minimum high-level input voltage	2V
$V_{IL\ max}$	Maximum low-level input voltage	0.8V
$V_{I\ max}$	Maximum input voltage	5.5V
$I_{OH\ max}$	Maximum high-level output current	-6mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	6mA (sinking)



Sapera support for Parallel I/O:

Access to Parallel I/O is achieved using members of the SapGio class. Refer to *Sapera++ Programmer's* manual for a complete description of the SapGio functions.

The resource indexes for the Parallel I/O are:

0: 8-bit output resource

1: 8-bit input resource

2: 1-bit interrupt resource

Example:

```
// Assert output pin 0 of Parallel I/O
m_pGioOutput = new SapGio(SapLocation("PC2-Vision_1", 0));
m_pGioOutput->Create();
m_pGioOutput->SetPinConfig(dwBitScan, SapGio::PinOutput);
m_pGioOutput->SetPinState (0, SapGio::PinHigh);
```

Note: Sapera LT 5.10 does not support the input strobe and output strobe pins.CamExpert does not provide direct access to the I/O. It must be activated programmatically from your Sapera application using the SapGio class.



IFC Support for Parallel I/O:

Access to Parallel I/O is achieved using members of the CICapMod class:

CICapMod::InportInterruptPolarity

CICapMod::InportMode

CICapMod::InportVal

CICapMod::OutportStrobeVal

CICapMod::OutportVal

Under IFC, each input pin of the parallel I/O has an associated interrupt event:

-P2V_INTR_DATAPIN0

-P2V_INTR_DATAPIN1

-P2V_INTR_DATAPIN2

-P2V_INTR_DATAPIN3

-P2V_INTR_DATAPIN4

-P2V_INTR_DATAPIN5

-P2V_INTR_DATAPIN6

-P2V_INTR_DATAPIN7

Acquisition Interrupts

The PC2-Vision frame grabber provides acquisition interrupts that allow an application to accurately monitor acquisition status, one of the many elements that make up the "trigger-to-image reliability"

model supported by PC2-Vision and its *Acquisition and Control Unit* (ACU). See "Trigger To Image Reliability" section (on page 71).

These interrupts are grouped into four families representing each acquisition stage:

- Trigger Interrupt
- Start of Image from Camera
- End of Image Capture
- End of PCI Transfer

The following block diagram illustrates the acquisition process and indicates at which stage each interrupt occurs.

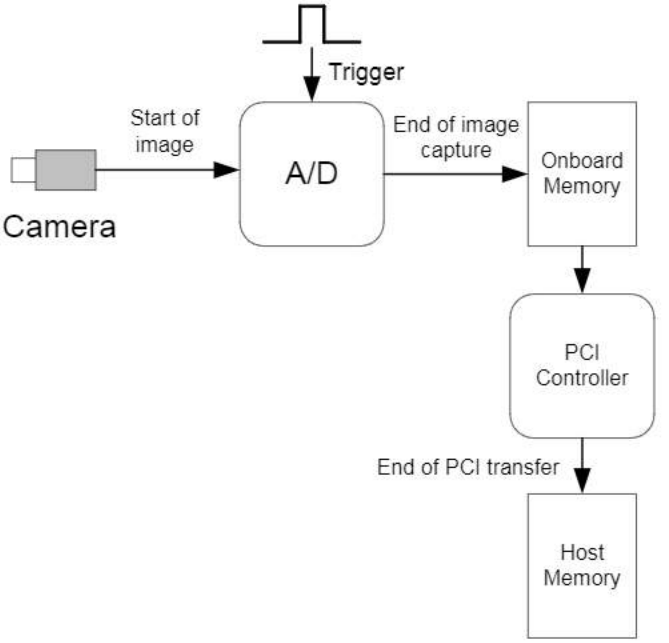


Figure 34: Acquisition interrupts

Under IFC, an interrupt event object is created using the *IfxCreateInterrupt*() global scope function. This returns a pointer to a *CInterrupt* object that is used to manage interrupts. Refer to the IFC-SDK™ Software Manual for more information using *CInterrupt* objects.

Interrupt-related Definitions

Interrupt	An interrupt is an electrical signal sent by the PC2-Vision board to the computer CPU to indicate an event on the frame grabber. The PC2-Vision driver has excellent reaction time to interrupts since interrupts are processed inside an interrupt service routine (ISR) at kernel level.
Event	An event is a WIN32 object that can take two states: signaled and non-signaled. It is used for thread synchronization. In this context, an event is associated with an interrupt so that a WIN32 thread can be unblocked when the event it is waiting for gets signaled. For example, when an interrupt is received, the corresponding event is signaled and the thread waiting for this event resumes execution.
Interrupt event object	Under IFC, an interrupt object is an IFC virtualization of an event associated to an interrupt.

Start of Trigger

The Start of Trigger interrupt is generated when the external trigger pin is asserted, usually indicating the start of the acquisition process. In IFC, this is represented by P2V_INTR_SOT. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER.

On PC2-Vision, the external trigger is protected by an opto-coupler; therefore, a minimum pulse width of 10µs is necessary to detect an active high trigger pulse while a minimum pulse width of 50µs is required for an active low trigger pulse. The PC2-Vision is also equipped with debouncer circuitry that allows the user to define the minimum acceptable pulse width programmatically.

Note: There is no Start of Trigger interrupt for a software trigger. This particular interrupt is only asserted for a pulse on the external trigger pin.

Start of Image from Camera

The Start of Image interrupt family indicates a vertical sync has been detected. Note that this does not necessarily mean the image will be captured. For instance, if you have a free-running camera at 30fps with external trigger enabled, you will get 30 interrupts per second even though the PC2-Vision waits for an external trigger to actually capture the next image. This allows the application program to count frames coming from the camera.

Start of Frame

The Start of Frame interrupt represents the beginning of a full frame output by the camera. It is asserted on the VS pulse (at the beginning of the frame). For interlaced cameras, you get one Start of Frame interrupt for each pair of fields. In IFC, this is represented by P2V_INTR_START_OF_FRAME. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_FRAME.

Start of Field

The Start of Field is only activated for interlaced scan cameras. You get a Start of Field interrupt for each incoming vertical sync (two per frame). In IFC, this is represented by P2V_INTR_START_OF_FIELD. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_FIELD.

Start of Odd Field

Start of Odd Field is only activated for interlaced scan cameras. You get a Start of Odd Field interrupt at the beginning of each incoming odd field coming from the camera. In IFC, this is represented by P2V_INTR_START_OF_ODD. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_ODD.

Start of Even Field

Start of Even Field is only activated for interlaced scan cameras. You get a Start of Even Field interrupt at the beginning of each incoming even field coming from the camera. In IFC, this is represented by P2V_INTR_START_OF_EVEN. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_EVEN.

Note: For reasons of performance, each Start of Image interrupt is only enabled if a user function has been registered to process them.

End of Image Capture

The End of Image interrupt family is asserted when image capture is completed and data is available in onboard memory.

End of Frame

An End of Frame interrupt is generated when the last pixel from the image has been acquired and transferred to onboard memory. In IFC, this is represented by P2V_INTR_EOFRM. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_FRAME.

End of Field

The End of Field is only activated for interlaced scan cameras. You get an End of Field interrupt when the last field has been acquired and transferred into onboard memory. In IFC, this is represented by P2V_INTR_VB. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_FIELD.

End of Odd Field

The End of Odd Field is only activated for interlaced scan cameras. You get an End of Odd Field interrupt when the odd field has been acquired and transferred to onboard memory. In IFC, this is represented by P2V_INTR_ODD_VB. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_ODD.

End of Even Field

The End of Even Field is only activated for interlaced scan cameras. You get an End of Even Field interrupt when the even field has been acquired and transferred to onboard memory. In IFC, this is

represented by P2V_INTR_EVEN_VB. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_EVEN.

End of PCI transfer

The End of PCI transfer interrupt is generated when each frame/field has been transferred to host memory.

In Sapera, CORXFER_PRM_EVENT_TYPE provides the various transfer events. The following are available on PC2-Vision:

- CORXFER_VAL_EVENT_TYPE_END_OF_FRAME
- CORXFER_VAL_EVENT_TYPE_END_OF_FIELD
- CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER

On IFC, a different PCI transfer interrupt is available for each of the three AD channels.

Cameras	IFC Designation
Cameras 1 and 4 (blue channel)	P2V_INTR_BMDONE
Cameras 2 and 5 (green channel)	P2V_INTR_BMDONE2
Cameras 3 and 6 (red channel)	P2V_INTR_BMDONE3

Note: In IFC, most applications use the GrabWaitFrameEx() member function of the CICamera class in order to wait for the end of transfer to host memory.

When performing a planar transfer, an application receives a different interrupt for each of the three color planes (red, green, and blue).

For a progressive scan cameras, only one bus master done interrupt is received. For an interlaced scan camera, each field has its own bus master done interrupt.

Timing Diagrams

The following diagram illustrates the exact location in time for each of the interrupts previously described. An interlaced scan camera is shown since it can generate all acquisition interrupts.

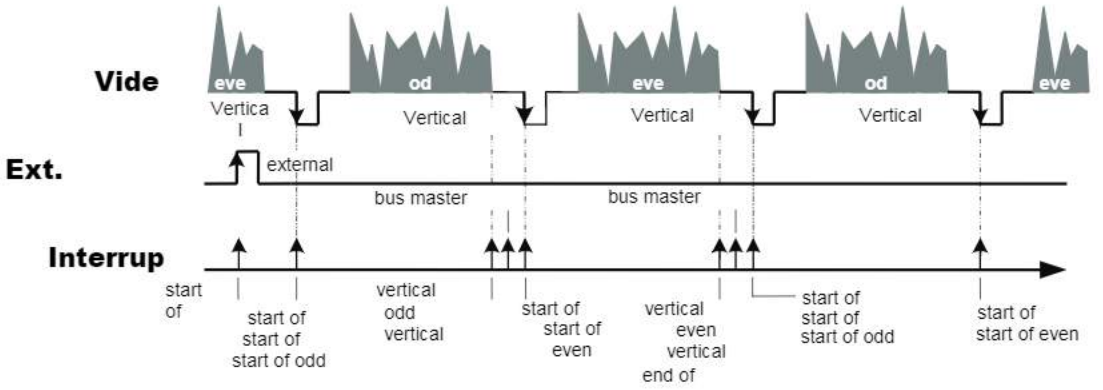


Figure 35: Acquisition Interrupts

Note: The Bus Master Done interrupt location is dependant upon PCI bus traffic as well as the size of the vertical front porch. It, therefore, may occur after the vertical sync of the next field/frame.

Error Support Interrupts

PC2-Vision supports a number of interrupts generated when problematic conditions occur within the system. These interrupts are used to notify applications that something erroneous occurred. Error Support Interrupts are part of the "trigger-to-image reliability" support.

Skipped Field

The skipped field condition is signaled when onboard memory is full resulting in the currently acquired frame being discarded.

A typical cause of this problem is an insufficient PCI bandwidth. Maximal theoretical bandwidth of the PCI bus is 132MB/second. If many bus master PCI devices are active simultaneously, it is possible that not enough bandwidth is left for PC2-Vision's PCI controller.

Another possible cause could be a high bandwidth RGB camera. PC2-Vision supports pixel clocks up to 40MHz. When using 32-bit padded data from an RGB camera, the maximal acquisition rate can reach 160MB/second. (40MHz x 4 bytes). Using asynchronous reset, this acquisition rate can be buffered by onboard memory, as long as the rate of the external trigger allows an average PCI bandwidth of about 80MB/second. In free-running mode, however, PC2-Vision will not be able to sink the 160MB/second. into the PCI bus. Note that this depends on the duration of the blanking period (since no data is digitized during blanking). One can use the Cropper or the Decimator to accommodate a high-bandwidth RGB camera. Planar transfer can also be an option as it only uses 75% of the bandwidth required for 0-padded 32-bit RGB value.

Loss of Sync

Loss of Sync is a condition that happens when PC2-Vision does not detect an HS signal coming from the currently selected camera. This typically happens when the camera cable is disconnected. When this condition is detected, image acquisition is stopped until an HS is received. Loss of Sync is also signaled if horizontal line is too short, that is, if two HS pulses are too near to each other.

Fast Camera Switching

PC2-Vision supports a Fast Camera Switching mode permitting efficient use of the six inputs by its triple-channel ADC. Fast camera switching proceeds in two steps:

1. Defines the sequence of cameras to be cycled through. No actual grab takes place during this sequence definition.
2. Starts the fast camera switching acquisition.



Note: Fast Camera Switching is not supported in Sapera LT 5.10. Use manual camera switching (that is, modifying the camera selector parameter to switch between cameras). A demo of manual camera switching is provided with the Sapera LT driver.

Note: All cameras in the switching group must have the same camera configuration file. Failure to do so may result in erratic grab or stop the grab altogether.

Best switching performance is achieved with genlocked cameras. In this case, the PC2-Vision can switch within the vertical blanking to reach maximal frame rate (all cameras have their vertical blanking aligned). This is not the case for asynchronous cameras; in this case, after switching to the next camera, PC2-Vision must wait for the VS before capturing the next frame.



Note: IFC requires the use of a single ring of buffers in order to achieve frame rate switching.

Genlocked Cameras

Genlocking cameras is generally achieved using the Master Mode capabilities of the PC2-Vision. In this scenario, the frame grabber drives the HD and VD line to all cameras. The output timing of all cameras is thus aligned, enabling PC2-Vision to go from one camera to the next within the vertical blanking and therefore not skipping any frames. Refer to the "Internal Sync" section (page 34) for a complete description of Master Mode setup.

The following diagram illustrates a group of two genlocked cameras. Because cameras are genlocked, their synchronization pulses are aligned. The internal synchronization capability of PC2-Vision prevents the PLL from unlocking, ensuring a stable image with minimal pixel jitter.

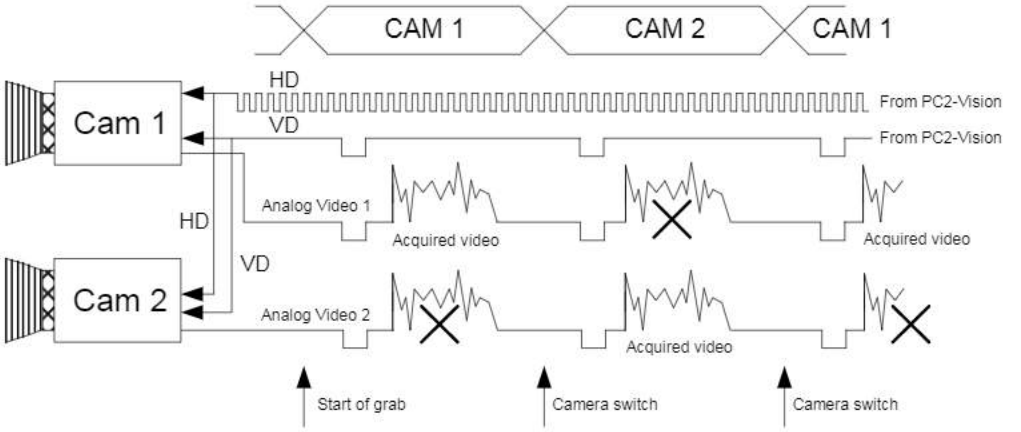


Figure 36: Fast Camera Switching for Free-Running Genlocked Cameras

Genlocking can be used for free-running or asynchronous reset mode cameras. The acquisition rate for free-running cameras is determined by the vertical sync pulse rate. For asynchronous reset mode, this rate depends on the exposure time and on the time it takes to transfer analog video signals from the camera CCD.

Example 1: Free-running genlocked cameras

- Six free-running RS-genlocked cameras @ 30fps.
- Cameras connected as two groups of three cameras (J1 controls the first group, J2 controls the second)

In this scenario, the PC2-Vision is able to acquire simultaneously from the first group of three cameras and switch to next group of three during vertical blanking. Total frame rate, therefore, is 90fps (three cameras x 30fps), or 15fps per camera.

Example 2: Edge pre-select

- Three 30fps cameras configured in edge-pre-select
- Integration period of 1/100 seconds
- Each camera receives frame reset and HD from the PC2-Vision

Acquisition time is the sum of the exposure (1/100 seconds) and the analog video transfer (1/30 seconds). This gives about 43.3ms. For most environments using asynchronous reset, an external trigger will dictate the rate of acquisition.

Asynchronous Cameras

Each camera of an asynchronous group has its own timing. They are out of phase with respect to each other. This means after switching to the next camera, the PC2-Vision must resynchronized (PLL must lock in phase with the new camera) and then wait for the VS to capture the next valid image. This overhead leads to a lower frame rate when compared to the genlocked case. As such, it is always better to use genlocked cameras when acquisition rate is an issue.

To better illustrate the difference between genlocked cameras and PLL mode camera switching, consider two free running asynchronous camera (typically two RS-170). Since the cameras are not genlocked, their frames are not in phase. This means that after grabbing from the first camera and switching to the second, the PLL must relock and then wait for the next VS (next valid frame). The same phenomenon applies when switching back to the first camera. In theory, if the PLL relocks instantly, the average frame rate would be 2/3 of the nominal frame rate; that is, a total of 20 frames per second for two 30fps cameras (10fps per camera). This is illustrated in the figure below.

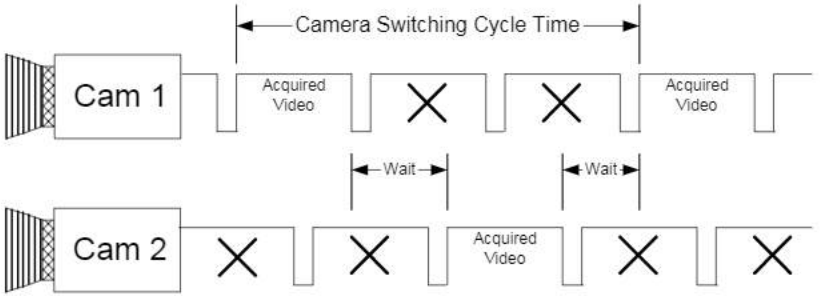


Figure 37: Asynchronous cameras fastest theoretical switching

In practice, the PLL needs to relocked before capturing the next valid frame. This further reduces the frame rate below 2/3 of its nominal value.

IFC Support for Fast Camera Switching:

IFC support fast camera switching through the following CPCVision2 member functions:

SwitchCameraDefineStart: Start definition of a sequence of camera switching grab

SwitchCameraDefineEnd: End definition of a sequence of camera switching grab

SwitchCameraGrab: Start a defined switching camera grab

SwitchCameraFreeze: Freeze a switching camera grab

Frame Delay Readout Support

Frame Delay Readout is a special mode of operation available on certain cameras that allows simultaneous acquisition from multiple cameras using a single channel ADC. This is an easy way to concurrently capture from up to six cameras using the PC2-Vision.

Note: Frame Delay Readout is not supported in Sapera LT 5.10.

Operation of Frame Delay Readout is straightforward. The frame reset pulse is sent to all cameras at the same time, thus triggering simultaneous acquisition. Once the exposure period is over, PC2-Vision selects the first camera and fires a VD pulse. The first camera outputs its analog video signal. Once the first camera signal has been digitized, PC2-Vision switches to the next camera and sends it a VD pulse. This process continues up to the last camera.

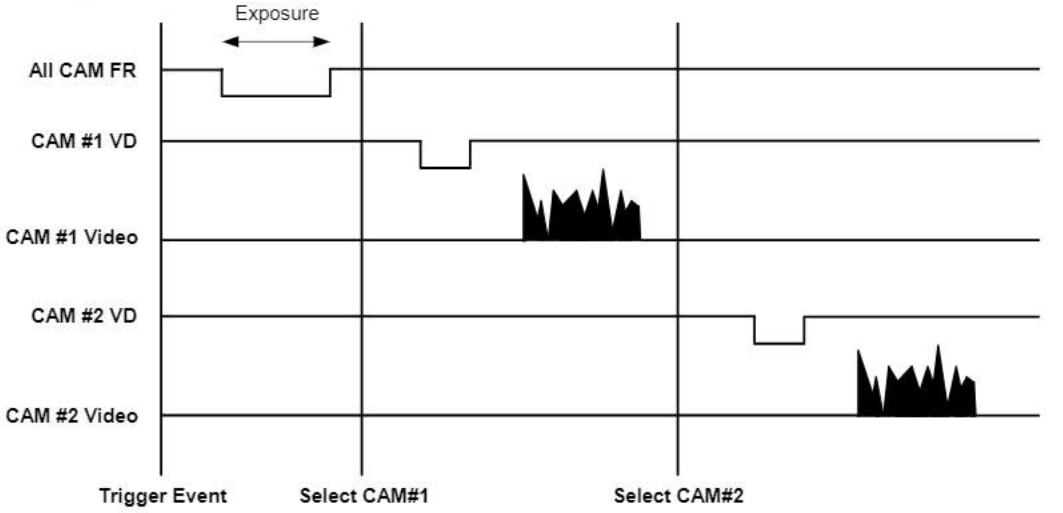


Figure 38: Frame Delay Readout

When building a system with Frame Delay Readout, consult your camera manufacturer's datasheet for any restrictions concerning this mode of operation.

Setting up the Frame Delay Readout is as simple as creating a list of cameras associated with an external trigger. All cameras must have the same camera configuration file. The list is first registered before being triggered for acquisition. A different list can be separately created for both external triggers and a third list for the software trigger.

Note: In Frame Delay Readout, IFC camera configuration files must use "Master HSync Enable = IFC_ENABLE" and "Source of Input Sync = P2V_SYNC_INTERNAL_SYNC".

IFC Support for Frame Delay Readout:

IFC support frame delay readout through the following CPCVision2 member functions:

SetFrameDelaySequence: Define the sequence of cameras for a frame delay acquisition

FrameDelaySnap: Perform a frame delay snap on a set of cameras

FrameDelayWait: Wait for a frame delay snap to complete

Trigger To Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger to image reliability model fuses together all the elements required to acquire images so that a central unit manages them coherently. These elements include, among others, I/O to control timing to the camera, onboard memory to compensate for PCI bus latency and error notification. Whenever PC2-Vision detects a problem, the user application is immediately informed and can take appropriate action to return to normal operation. PC2-Vision offers this robustness through its ACU (Acquisition and Control Unit), which manages all six frame grabber inputs and monitors in real-time the acquisition state of each input. As such, it is transparent to user applications for the most part.

On PC2-Vision, user application can interact with trigger-to-image through the following:

- Glitches on the external trigger line are debounced by the ACU. A parameter is available to indicate the minimal pulse duration to consider an external trigger pulse valid. Refer to "External Trigger" (on page 43) for more information.
- For each frame/field, a number of interrupts are generated to indicate the following events:
  - a) Trigger interrupt
    b) Start for frame/field interrupt
    c) End of frame/field interrupt
    d) End of transfer interrupt
- By monitoring these events, it is possible to know the flow of acquisition of the system as demonstrated in "Acquisition Interrupts" section (on page 61).
- If something goes wrong during the acquisition process, a notification is sent for the following:
  - a) Field skip:
    This happens when PCI bandwidth is limited or onboard memory is full (8MB of onboard memory on PC2-Vision). Frame being acquired is discarded.
    b) Loss of Sync:
    This event represents a mismatch between the expected camera configuration and what is sent by the camera. This means the image received by the frame grabber is smaller than expected or no horizontal synchronization is received from the camera. Note that an image larger than expected is compensated by the Cropper, so you will not get a bad synchro interrupt.

    Refer to the "Error Support Interrupts" (on page 66) for more information on this topic.

The rest of trigger-to-image is handled internally by the ACU to correctly synchronize acquisition among the different inputs. This is done automatically and does not require user application involvement. This covers HS, VS, WEN, frame reset, external trigger, strobe signal and transfers over the PCI bus.

Technical Reference

Hardware Specifications

The following provides specific information related to PC2-Vision hardware specifications.

PC2-Vision Specifications

Function	Description
Acquisition	
	Standard RS-170 and CCIR, RGB, dual-channel and non-standard progressive scan providing composite video (non-standard progressive scan can be driven with external TTL timing: HSYNC, VSYNC, and Frame Reset)
	Six analog video inputs, AC coupled and terminated to 75Ω
	Triple 8-bit flash A/C; Input pixel rates to 40MHz
	Simultaneous capture from any three synchronized monochrome cameras
	DC Restoration – programmable clamp pulse
	Partial scan mode
	Input gain – software selectable
	Low-pass filter – software selectable
	Pixel clock from 7MHz up to 40MHz (minimum 3.5MHz using horizontal decimator)
	Programmable time-base generator and programmable resolution to 2048 x 2048 interlaced or non-interlaced

Synchronization and timing control	
	Composite sync
	Separate sync, TTL
	Pixel clock input, TTL
	Trigger input, opto-isolated TTL or RS-422
	Programmable trigger de-bounce delay from 1 to 255 microseconds
	One External Trigger input per group of three cameras; synchronizes acquisition to external events
	Programmable trigger, slow strobe, fast strobe
	One strobe output per group of three cameras
	I/O controls – 8 TTL inputs, 8 TTL outputs, Interrupt driven for immediate software response.
	Onboard RS-232 COM port for camera control (mapped as a COM port in the system)
Host transfers and data format	
	Pixel format: MONO8, YUV16, RGB32, RGB planar
	Simultaneous transfer of three camera images into host memory in a packed pixel format (C1,C2,C3,x)
	DMA engine supports transfers up to 100MB/second
	DMA engine supports scatter/gather
	DMA engine supports de-interlacing images
I/O Pins	
	I/O pins include: Parallel I/O, frame reset, VS, HS, WEN, Pixel clock, composite sync.
Onboard Processing	
	Input lookup-tables – following A/D
	Area of Interest transfers
	YCrCb converter
Power	
	Camera power onboard, +12 V @ 500mA, fused protected
	Parallel I/O power, 2-pins at +5V @ 500mA, fused protected

PC2-Vision Connector and Jumper Locations

PC2-Vision component view

The PCI Express and PCI board versions have the same component layout (except the PCI Express version does not have LED 3).

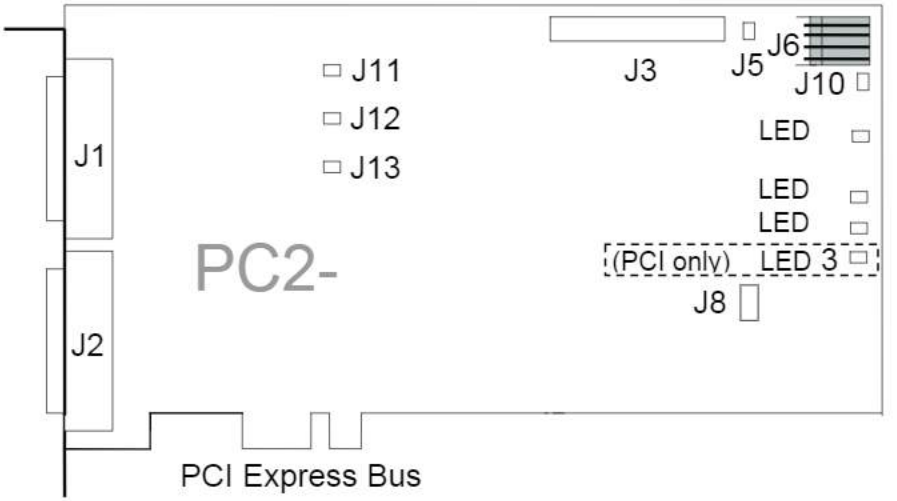


Figure 39: Component View

Connector Bracket

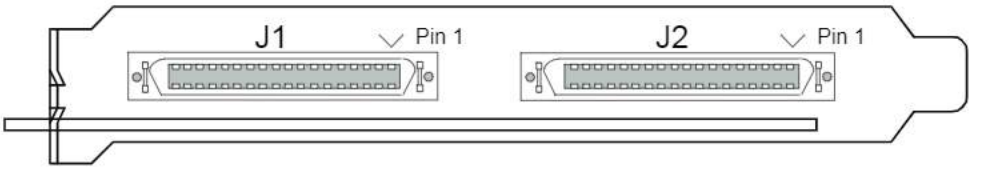
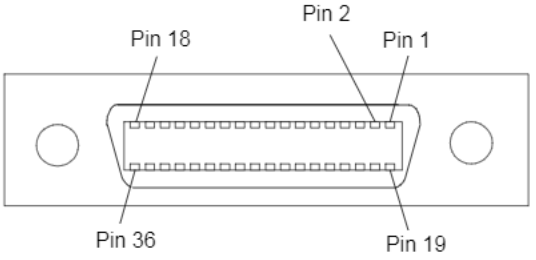


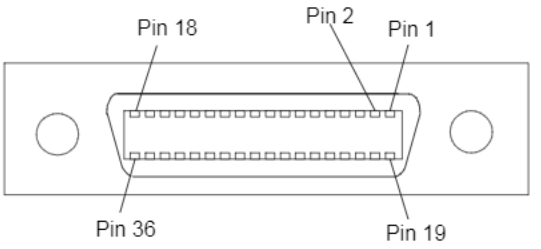
Figure 40: Connector Bracket

J1: MDR 36-Pin Female Group 1 Camera Connector



Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	Video1	Input	19	Video1 AGND	
2	HS1	Input/Output	20	VS1	Input/Output
3	Camera_Trigger 1	Output	21	WEN1	Input
4	Digital GND		22	Digital GND	
5	Video2	Input	23	Video2 AGND	Input
6	HS2	Input/Output	24	VS2	Input/Output
7	Camera_Trigger 2	Output	25	WEN2	Input
8	Video3	Input	26	Video3 AGND	
9	HS3	Input/Output	27	VS3	Input/Output
10	Camera_Trigger 3	Output	28	WEN3	Input
11	Strobe1	Output	29	Digital GND	
12	Digital GND		30	+12V	
13	-CSync1	Input	31	+12V GND	
14	Reserved		32	+12V	
15	Reserved		33	+12V GND	
16	Digital GND		34	RX1	Input
17	Ext_Trig1-	Input	35	TX1	Output
18	Ext_Trig1+	Input	36	Pixel_Clk1	Input

J2: MDR 36-Pin Female Group 2 Camera Connector



Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	Video4	Input	19	Video4 AGND	
2	HS4	Input/Output	20	VS4	Input/Output
3	Camera_Trigger 4	Output	21	WEN4	Input
4	Digital GND		22	Digital GND	
5	Video5	Input	23	Video5 AGND	Input
6	HS5	Input/Output	24	VS5	Input/Output
7	Camera_Trigger 5	Output	25	WEN5	Input
8	Video6	Input	26	Video6 AGND	
9	HS6	Input/Output	27	VS6	Input/Output
10	Camera_Trigger6	Output	28	WEN6	Input
11	Strobe2	Output	29	Digital GND	
12	Digital GND		30	+12V	
13	-CSync2	Input	31	+12V GND	
14	Reserved		32	+12V	
15	Reserved		33	+12V GND	
16	Digital GND		34	RX2	Input
17	Ext_Trig2-	Input	35	TX2	Output
18	Ext_Trig2+	Input	36	Pixel_Clk2	Input

J3: Parallel I/O 26-Pin Dual-Row Connector

PC2-Vision provides a digital I/O capability for controlling or monitoring external events. The digital input and output lines, available on a 26-pin header at the top of the PC card, can be cabled to a 25-pin female D-Sub connector that occupies an open slot in the chassis using a bracket assembly (part number 4816).

25	23	...	3	1
26	24	...	4	2

Header Pin #	Signal name	Description	Connector Pin #
1	GND	Digital ground	1
3	GND	Digital ground	2
5	GND	Digital ground	3
7	GND	Digital ground	4
9	IN1	Digital Input pin 1	5
11	IN3	Digital Input pin 3	6
13	IN5	Digital Input pin 5	7
15	IN7	Digital Input pin 7	8
17	OUT0	Digital Output pin 0	9
19	OUT2	Digital Output pin 2	10
21	OUT4	Digital Output pin 4	11
23	OUT6	Digital Output pin 6	12
25	+5V	+5V power output	13
2	STROBE_0	Strobe Output	14
4	STROBE_1	Strobe Input	15
6	I/O_INT	Interrupt Input	16
8	IN0	Digital Input pin 0	17
10	IN2	Digital Input pin 2	18
12	IN4	Digital Input pin 4	19
14	IN6	Digital Input pin 6	20
16	+5V	+5V power output	21
18	OUT1	Digital Output pin 1	22
20	OUT3	Digital Output pin 3	23
22	OUT5	Digital Output pin 5	24
24	OUT7	Digital Output pin 7	25
26	n/c	no connection	n/a

J4, J7, J8, J14: Reserved

Reserved.

J5: Recovery Jumper

Recovery jumper for flash update.

J6: Power Connector

J6 must be connected to a computer floppy disk power cable to provide 12V to the camera through the J1 and J2 camera connectors.

To remove the floppy disk power cable from the J6 connector, carefully lift the cable connector head from the J6 connector to unlatch the locking mechanism underneath the connector, then carefully pull cable from the board connector.

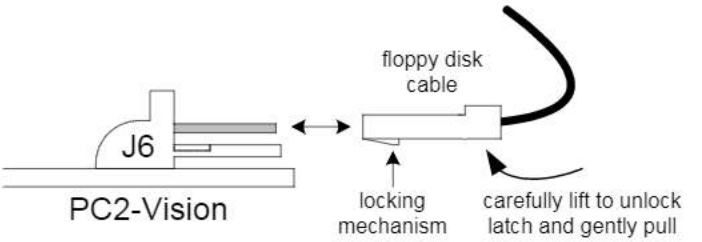


Figure 41: Removing floppy power cable

J10: Camera Power from PCI Connector

When this jumper is set, 12V power for the camera comes from the PCI connector. When this jumper is removed, the J6 power connector must be connected to a computer floppy disk power cable to provide 12V to the camera (alternatively, you can supply your own power supply to the J6 connector).

J11, J12, J13: Video Signal

These test points provide access to the video signal just before conversion by the ADC.

J11: CAM1 or CAM4

J12: CAM2 or CAM5

J13: CAM3 or CAM6

LEDs

LED1: indicates a 3.3V PCI bus.

LED2: indicates the fail-safe boot mode (when jumper J5 is removed). It is not to be turned ON during the normal operation of the board

LED3: indicates a 5V PCI bus (PCI board version only).

LED4: PCI 12V

Note: LED1 and LED3 are mutually exclusive.

Computer Requirements for the PC2-Vision

The PC2-Vision requires at minimum an Intel Pentium III or compatible computer system with a free PCI or PCI Express local bus slot, depending on your board version.

Operating System Support

Windows XP, Windows Vista, and Windows 7.

PC2-Vision Physical Dimensions

Approximately 6.675" W×4.2" H (16.95 cm W×10.67 cm H)

Power Requirements

	Typical	Maximum
+ 5 Volts	3 A	5 A
+ 12 Volts	120 mA	250 mA
- 12 Volts	75 mA	100 mA

Environment

Ambient Temperature:	0° to 55° C (operation) -40° to 125° C (storage)
Relative Humidity:	5% to 95% non-condensing (operating) 0% to 95% (storage)

Camera Compatibility

Review the DALSA web page for the latest compatible camera information for the PC2 Vision at http://dalsa.com/mv/products .

Interfacing Cables

MDR-36 Connector

DALSA offers a variety of camera cables for PC2-Vision (listed in the following section). To build your own camera cable, you can select MDR-36 components from 3M (http://www.3m.com).

Part Description	3M part number	3M Id
MDR-36 shielded solder plug	10136-3000VE	JE-1501-8028-7
MDR-36 plastic solder plug junction shell	10336-52F0-008	JE-1501-8040-2

DALSA Interfacing Cable Diagrams and Specifications

The following ten cables are available from DALSA to interface between the specific camera used and the PC2-Vision. For purchasing information , see "Sales Information" on page 169.

Cables	Part Number
Single camera BNC cable	OC-PC2C-V1B00
Single RGB camera BNC cable	OC-PC2C-V1B01
PCVision Series adapter cable	OC-PC2C-V3A00
Single camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V1H00
Three camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V3H00
Single camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V1H01
Three camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V3H01
Single camera Hirose-12 + Hirose-6 for Jai A-series	OC-PC2C-V1H02
Three camera Hirose-12 + Hirose-6 for Jai A-series	OC-PC2C-V3H02
Jai CV-M77 RGB camera cable	OC-PC2C-V1D00
Pulnix camera cable (supporting three cameras)	OC-PC2C-V3H03
Jai M-series camera cable (supporting three cameras)	OC-PC2C-V3H04

Warning: Some cameras have frame reset on their Hirose-12 pin 9 while other have it on pin 11. It is imperative to use the appropriate camera cable that matches the frame reset pinout. Failure to do so could result in board damage.

Cable 1: Standard input cable for one camera using BNC connector

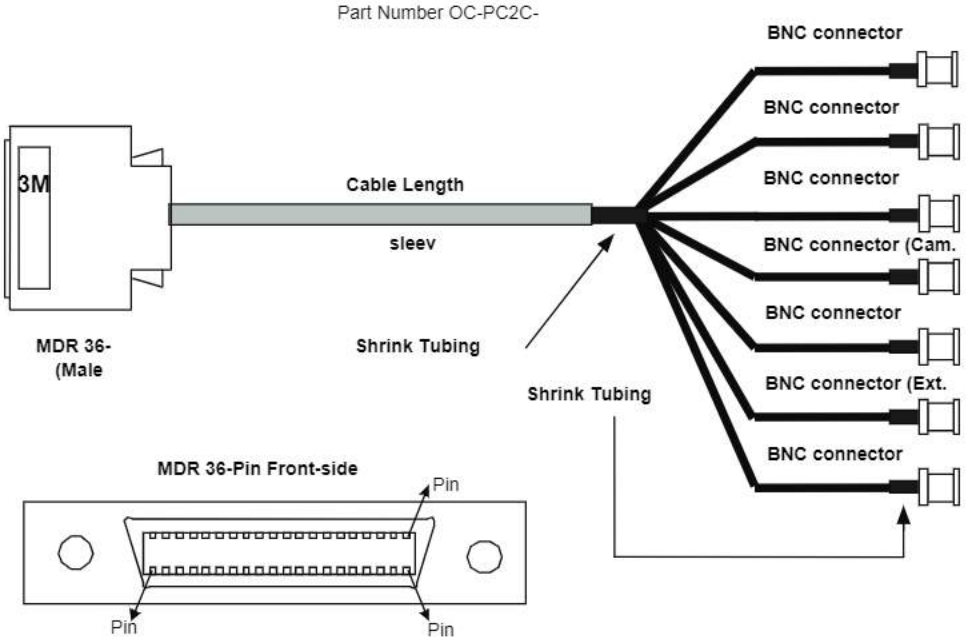


Figure 42: Single camera BNC cable

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Video
1	Video1		Coax Wire
19	Video1 AGND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: HS
2	HS1		Coax Wire
4	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: VS
20	VS1		Coax Wire
22	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Cam Trigger
3	Camera Trigger1		Coax Wire
29	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: PCLK

36	PCLK1		Coax Wire
29	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Ext. Trigger
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Strobe
11	Strobe1		Coax Wire
12	Digital GND		Coax Shield

Cable 2: Standard RGB input cable for one camera using BNC connectors

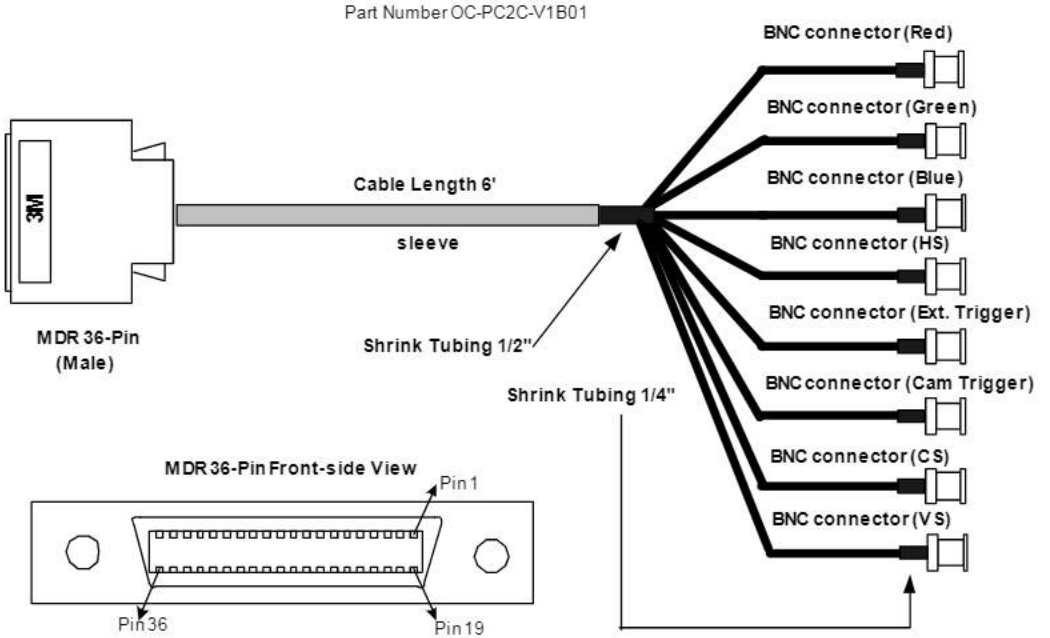


Figure 43: Single RGB camera BNC cable

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Blue
1	Blue		Coax Wire
19	Blue AGND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Green
5	Green		Coax Wire
23	Green AGND		Coax Shield
Pin	MDR 36-Pin (Male) Frame	Pin	BNC Male Connector Label: Red

#	Grabber	#	
8	Red		Coax Wire
26	Red AGND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: HS
2	HS1		Coax Wire
4	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: VS
20	VS1		Coax Wire
22	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Trigger In
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Cam Trigger
3	Camera Trigger1		Coax Wire
29	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: CS
13	CS		Coax Wire
12	Digital GND		Coax Shield

Cable 3: PC2-Vision to PCVision adapter cable

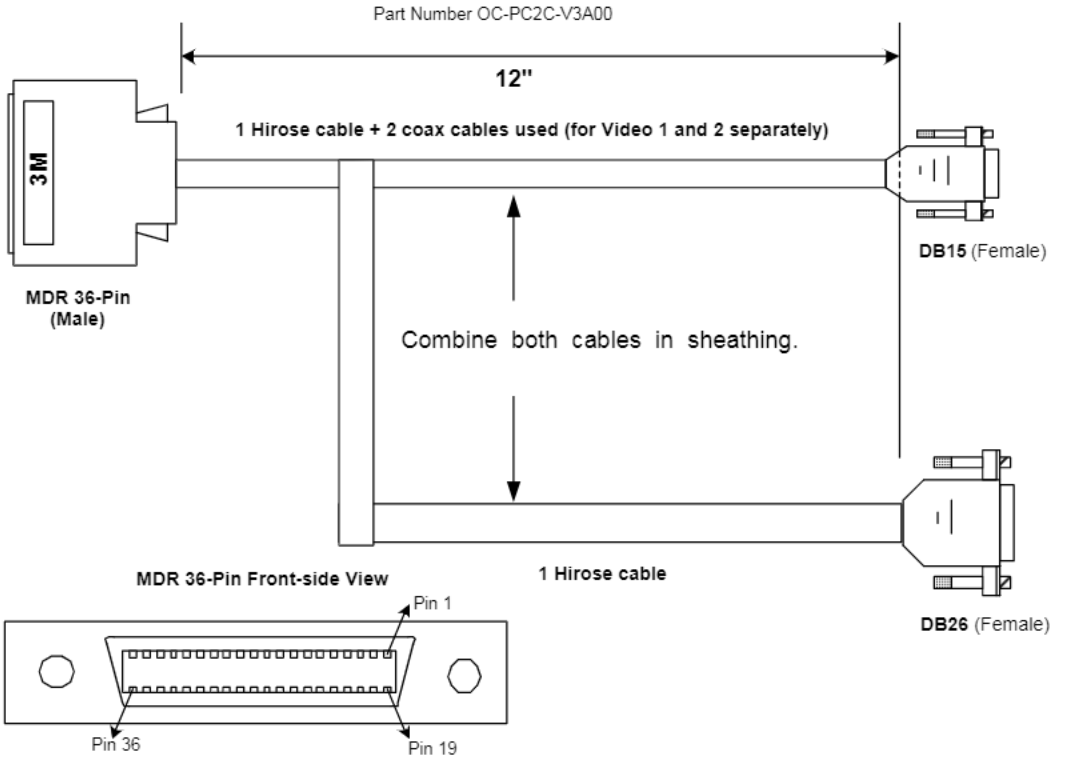


Figure 44: PCVision Series adapter cable

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	DB15 (Female)	Wire Type
1	Video1	2		Coax Cable
19	Video1 AGND	7		Coax Cable
2	HS1	13		Coax 1 Wire
4	Digital GND	5		Coax 1 Shield
20	VS1	14		Coax 2 Wire
4	Digital GND	5		Coax 2 Shield
3	Camera Trigger1	9		Wire
30	+12V	15		Wire
31	+12V GND	10		Wire
5	Video2	1		Coax Cable
23	Video2 AGND	6		Coax Cable
6	HS2	11		Coax 3 Wire
22	Digital GND	4		Coax 3 Shield

24	VS2	12		Coax 4 Wire
22	Digital GND	4		Coax 4 Shield
7	Camera Trigger2	8		Wire
Pin #	**MDR 36-Pin (Male) Frame Grabber**	**Pin #**	**DB26 (Female)**	**Wire Type**
8	Video3	2		Coax 1 Wire
26	Video3 AGND	11		Coax 1 Shield
9	HS3	21		Coax 2 Wire
29	Digital GND	3		Coax 2 Shield
27	VS3	22		Coax 3 Wire
29	Digital GND	3		Coax 3 Shield
10	Camera Trigger3	13		Coax 4 Wire
29	Digital GND	3		Coax 4 Shield
32	+12V	23		Wire
33	+12V GND	14		Wire
18	Ext_Trig1+	17		Wire
17	Ext_Trig1-	24		Jumper Wire
11	Strobe1	6		Wire
29	Digital GND	24		Jumper Wire

Cable 4: Standard interface to one Hirose 12-pin with trigger pulse on pin 9

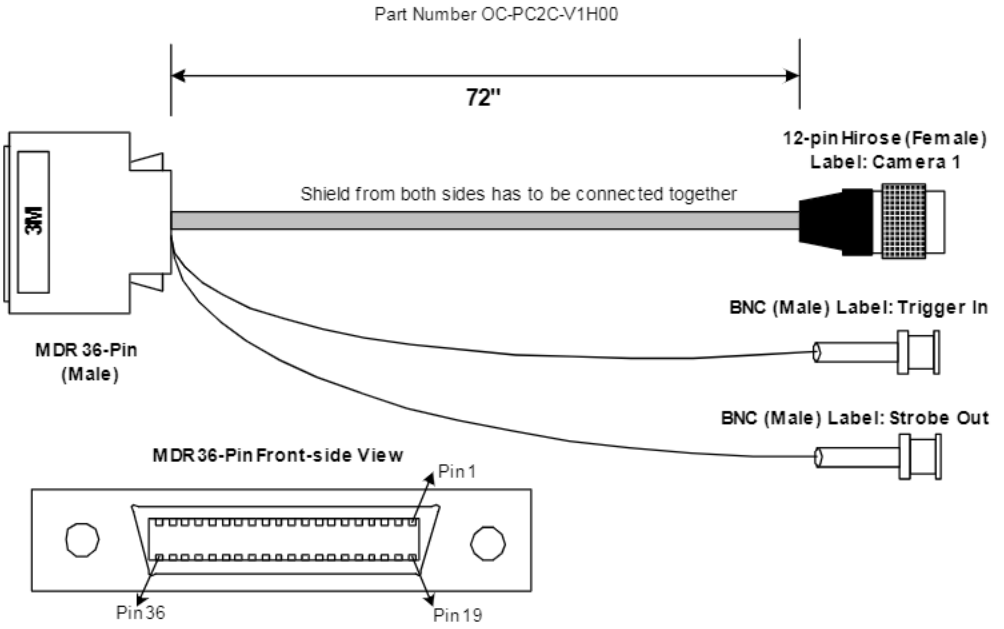


Figure 45: Single camera Hirose-12 cable, trigger on pin 9

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-pin (Female) Camera 1
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
3	Camera Trigger1	9	Coax 4 Wire
29	Digital GND	8	Coax 4 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
11	Strobe1		Coax Wire
12	Digital GND		Coax Shield

Cable 5: Standard interface to three Hirose 12-pin connectors with trigger pulse on pin-9

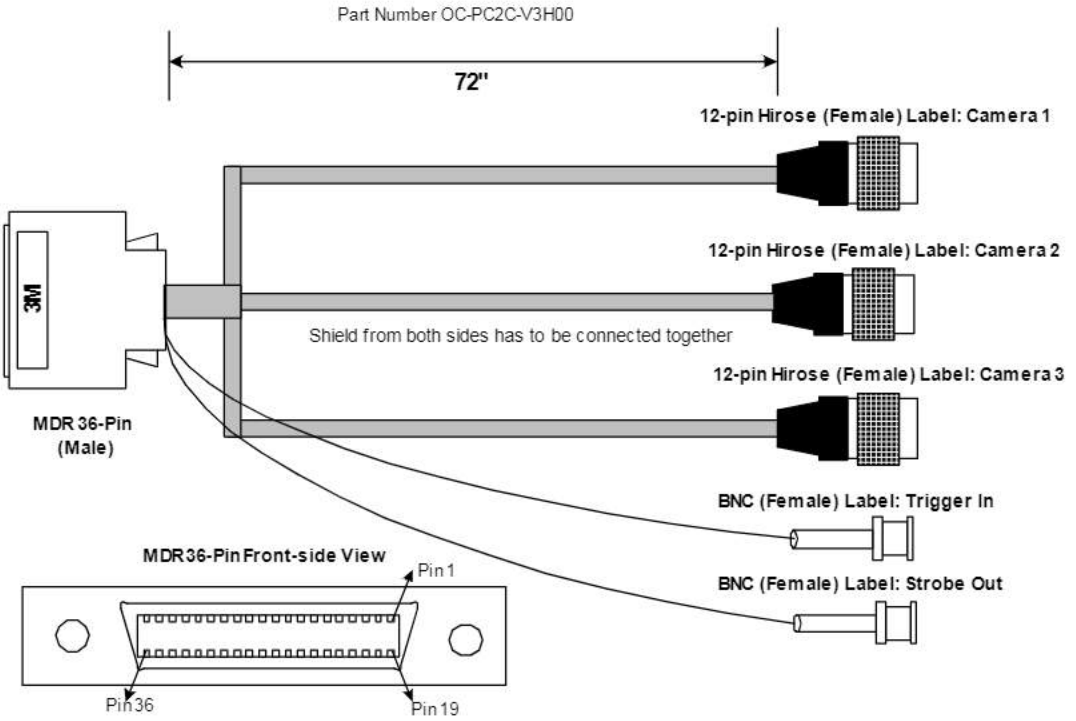


Figure 46: Three camera Hirose-12 cable, trigger on pin 9

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Camera 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 1
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
4	Digital GND	12	Coax 3 Shield
3	Camera Trigger1	9	Coax 4 Wire
4	Digital GND	8	Coax 4 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
Camera 2			

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