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13 Nov 96 - 6 Feb 97

ARINC 429 VXI Interface Modules

PAC-429C-X8 Series

- 8 Programmable Parametric Channels

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Receive or Transmit
High, Low, and Variable Speed
Variable Voltage, Bit Gap & Word Size
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- 8 Additional Low Speed Receivers
- On-board Engineering Unit Conversion
- 256 KBytes of Dual-Port RAM for Real-time Data
- Available in B or C Size
- RS232/422 Port
- Bus Master Capability

Description

The PAC-429C-X8 Series modules are available in B or C size, to provide a high performance communications a VXI host and an ARINC 429 Data Bus. The X8 Series modules are factory configured as either register or me devices.

The modules' architecture is a multiprocessor design that provides reliable high-integrity ARINC 429 reception transmission. This module is designed for high performance applications, capable of off-loading tasks from the computer that could not previously be performed by a single ARINC 429 interface module.

The X8 modules conform with the Mark 33 Digital Infor mation Transfer System 429-14 specifications, and ar of parametric testing that handles communications which deviate from the standard specification. This is useful and validation phases of LRU develop ment, and at repair depots for margin testing to detect "phantom" errors

The modules support eight "configurable" parametric channels that can be set as either receivers or transmitters acting as transmitters, these channels can output signals from 0 to 12 Volts.

Transmitters or receivers can be configured for variable word sizes (2 · bits), appropriate parity (EVEN/ODD /I variable frequency (5 kHz 120 kHz), and variable bit gap.

In addition to the eight configurable channels, the modules also provide eight low speed receiver channels, for a to 16 independent ARINC 429 channels.

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2 captures
13 Nov 96 - 6 Feb 97
199

Module Models

All X8 VXI modules have eight configurable (transmit or receive) parametric channels and eight low speed rec following model types are available:

PAC-429C-X8B/R

A register based B size VXI 429 module

PAC-429C-X8B/M

A message based B size VXI 429 module

PAC-429C-X8C/R

A register based C size VXI 429 module

PAC-429C-X8C/M

Module Features

ARINC 429 Reception

Each receiver channel independently time-stamps and buffers the incoming data. The data is then converted to units (if desired), and sent to the VXI host. Received words are automatically checked for parity. A built-in erro indicates the number of errors that have occurred during data reception. The module can also filter received wo off-loading the host processor by only collecting data of interest.

ARINC 429 Transmission

Each transmitter channel processes scheduled transmissions and transmits buffered sequential words. When the a transmit word from the host, it is converted from engineering units to the ARINC 429 word and proper parity automatically generated.

Time Stamping

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2 captures
13 Nov 96 - 6 Feb 97
199

Built-In-Testing

The modules' firmware contains built-in-tests which are performed on power-up. When these tests pass, the mo indicates to the host that it successfully completed power-up self testing. If any test fails, this information is pas host and LEDs, including the main "FAIL" light, on the module front panel are lit to indicate a failure code.

The following tests are performed during power up: proces sor tests, memory tests, math co-processor tests, a F checksum test, and channel processor communication tests. In addition, the module contains an Analog to Digit (ADC) that allows testing of the Digital to Analog Converter controlling the variable voltage outputs of the AR transmitters.

The host has the ability to perform a complete system test when the user connects an "external loopback" conne module. This connects input discretes to output discretes, and ARINC 429 transmitters to receivers. The host ca data on the transmitters and verify that the data was received correctly by the ARINC 429 receivers.

A message based C size VXI 429 module

Host Communications

Modules are available as message or register based devices.

Register Based:

The modules communicate to the host via 256 KBytes of Dual-Port RAM, a Command FIFO, a Response FIFC optional interrupts. The Command and Response FIFOs are used to communicate commands to the module fro and responses to those commands back to the host. The 256 KBytes of Dual-Port RAM is used primarily to cor large volumes of ARINC 429 real-time data.

Message Based:

As message based devices, the modules communicate using the communication registers in A16 space. The me modules provide the same functionality as the register based modules through "SCPI-like" commands.

Interrupt Generation

The robust interrupt generation capability in the PAC-429

X8 modules allows the modules to asynchronously signal the host (VXI system controller) when certain events events include receive and transmit events, error events, FIFO events, discrete I/O events, and board processor Through program control, any of the interrupts

can be selectively enabled or masked. The modules can be configured to interrupt on any one of the 7 interrupt

Indicator LEDs

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2 captures
13 Nov 96 - 6 Feb 97
199

channel activity and channel built-in-test status.

Input/Output Discretes

There are 8 output discretes (TTL compatible) on the mod -ules. These are used for a variety of purposes, inclu

VXI trigger lines, indicating status, and general purpose use. These outputs can sink up to 10 mA of current. Th input discretes (TTL and CMOS compatible). Each input discrete accepts any input from 2.4 5 volts as a "true" from 0 0.8 volts as "false."

Module Firmware

Firmware is supplied with each 429 VXI module which supports an extensive set of ARINC 429 functions. The allow users to program their module without specific knowledge of the module's architecture.

When transmitting, the host can request that the module send data sequentially from a First-In-First-Out (FIFO that the module automatically send scheduled data and allow the host to update the data asynchronously. If both scheduled modes are selected, the scheduled data always takes priority over the FIFO data, with the FIFO data "filling-in" the gaps between scheduled data.

When receiving, the host can get data sequentially from a FIFO, or get the most recent data for any label/SDI c from a "mailbox" slot. The data placed in the

Examples of Standard Firmware Functions: DefineRxFilterWords, ModifyRxChannel

· **Transmitting**
DefineTxScheduleTable, ModifyTxChannel

· **Engineering Units**
LoadEngineeringConversionTable

· **Discrete Control**
ReadInputDiscrete, WriteOutputDiscrete

· ***Configuration***
ConfigureSerialPort, SetInterruptConditions

· ***Card Control***
DequeueErrors, ResetClock, RunDiagnostic

· ***Channel Control***
HaltChannel, StartChannel

· ***Receiving***

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13 Nov 96 - 6 Feb 97
199

converts raw data to and from engineering unit format, and transfers it to the four channel processors.

The channel processors manage and control the 429 communication. Each channel processor handles 2 configu receive or transmit channels (high or low speed), and

2 low speed receive channels.

Since each channel processor can filter received data and schedule transmit data, the performance of the board not depen dent on bus loading, but only on the amount of received data being transferred to the host, and the am transmit data the host generates. The receivers can not unknowingly lose data since each of the channel proces buffer fully loaded buses.

receive FIFO is time-stamped by the module. The FIFO words can be filtered by label/SDI combination.

The host can configure the size of the FIFOs in Dual-Port RAM to be from 16 words to 32K ARINC 429 words. address for each FIFO is therefore dependent on how the host configures the module. Each routine that configu returns the offset for that FIFO.

The host can download an Engineering Unit Conversion Table to the module that enables conversion between r 429 words and engineering units. The format for all ARINC 429 data placed in Dual-Port RAM is determined b If no table has been defined, all words default to "raw" format. When engineering unit conversion is enabled, b engineering data and the raw data are available to the host.

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*Specifications**

Physical Characteristics:
B size: *Height 9.2" (23.37 cm)*
Width 0.8" (2.03 cm)
Depth 6.2" (15.75 cm)

C size: *Height 9.2" (23.37 cm)*
Width 1.2" (3.05 cm)
Depth 13.4" (34.04 cm)

Weight:
B size: *Net 12 oz (0.34 kg)*
Shipping 28 oz (0.79 kg)

C size: *Net 22 oz (0.62 kg)*
Shipping 38 oz (1.07 kg)

Device Type:
Register or Message Based

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2 captures
13 Nov 96 - 6 Feb 97
199

1 7, switch selectable

Address Space:
A16/A32 or A16/A24, D16 Slave/Master Device
Uses 256 KBytes of A24 or A32 Space

****Specifications apply to all models of the PAC-429 VXI Modules unless otherwise noted.***

Ordering Guide

Model Number Description

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PAC-429C-X8B/R  429 B Size, register based VXI module
PAC-429C-X8B/M  429 B Size, message based VXI module
PAC-429C-X8C/R  429 C Size, register based VXI module
PAC-429C-X8C/M  429 C Size, message based VXI module
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Optional Software

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PAC-429S-X8/LVI VXI/VME LabVIEW driver
PAC-429S-X8/LWPP        LabWindows Plug & Play driver
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