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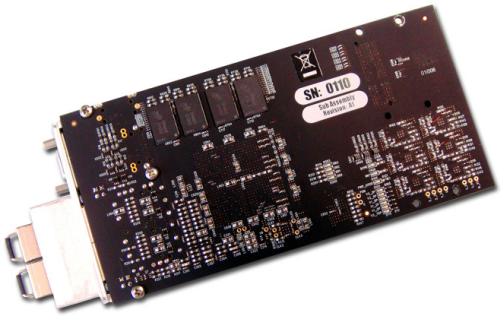
Find the *Teradyne / Avionics Interface Technologies XMC-FC4* at our website: ***Click HERE***

AVIONICS INTERFACE TECHNOLOGIES
A Teradyne Company

XMC-FC4

Dual-Port Simulator/Analyzer Interface Test Module for XMC

AIT's PCIe-FC4 SimulyzerTM is a two port, multi-function, intelligent Fibre Channel interface PCI Express module. This module offers both data generation/simulation and monitor/ analyzer functions for simulation and test verification of nodes and/or switches communicating via the international communication protocol standards of Fibre Channel.



DUAL-PORT CHRONOLOGICAL MONITOR/ ANALYZER

- Monitor functions allow for data to be captured and archived to host PC storage mediums, and provide statistics for receive stream status
- Analyzer functionality builds on the monitor function by providing powerful triggers and filters to capture pertinent data before and after defined events
- Precision time stamping of captured data with 10ns resolution
- Live capture and current value monitoring
- Allows simultaneous capture of two receive data streams on separate ports, which may also be archived to Host PC storage mediums
- Analyzer allows multiple triggers (including external triggers) to define when capture is to begin, and filters to define what data is to be captured or replayed

DUAL-PORT DATA GENERATOR/SIMULATOR

- Data Generator provides creation of Fibre Channel transmit primitives/frames using data generation algorithms to saturate Fibre Channel line rates
- Error injection on any frame header or payload parameter
- Hardware Replay of recorded data with precision timing or corrected protocol timing
- Provides data generation at full line rates on any Fibre Channel architectural level (FC-1, FC-2, FC-4)
- Allows complete control of the transmit side of a Fibre

Key Features

- Multi-topology support including point-to-point, fabric switched, and arbitrated loop
- Supports standard 1.0625, 2.125, and/or 4.25 Gigabaud transfer rates
- Supports non-standard clock frequencies ranging from 1.0625 up to 4.25 Gigabaud
- Independent port speed settings
- Onboard IRIG-B time code decoder/generator provides precision time stamping of all captured data
- Full line rate Data Capture plus Streaming Archive
- Hardware Replay from Data Capture file
- In-line port configuration provides the capability to monitor the receive data stream and reroute to the other port without "disturbing" the data stream
- Operates in a single PCIe x4 slot, supporting bus mastering with DMA
- Windows, Linux and LabView device drivers for 32-bit and 64-bit systems
- fcXplorer Windows-based FC Simulator and Analyzer Test Software

Channel link including: frame content (header and payload), timing, sequence, frame gaps, fill words and other legal primitives, as well as illegal 40-bit codes

- Data generator functions include random, incrementing, decrementing, or custom-defined data
- Four generator output queues available for transmission, each with a pre-emptive degree of priority
- User-defined simulation can be triggered by any receive stream characteristic including: frame content, timing, sequence, and/or frame gaps

TRIGGERS AND FILTERS

- Trigger modules provide mechanism for trigger/filter, including:
  - Ordered set or Frame delimiter
  - Frame Header or Payload (up to an entire frame on which to trigger)
  - FC1/FC2 errors
  - External triggers or triggers from another port
  - Expiration of a timer trigger module
  - Counting events from other trigger modules (listed above)
- Internal sequencers allow the user complete flexibility to define the events and the sequence of events that must occur to trigger the start of capture
- Output triggers are available for trigger signal output via the external connector (multiple modules may share these triggers between ports)

LIVE CAPTURE AND CURRENT VALUE MONITORING

- Immediate access to captured data buffers (prior to monitor buffer full event) allows the user's application to access "Live" capture data for use in a real-time display of captured data in a chronological format.
- The internal sequencer FIFO allows the application to be provided with monitor buffer offsets for immediate access to individual locations within a receive frame. This feature allows the user to easily generate "Current Value Tables" for critical parameters in the receive data stream.

Technical Data

Memory	4 GB configuration
Time Tagging	IRIG-B with 10 ns resolution
Fibre Channel Interface	From 1.0625 Gbps to 4.25 Gbps (custom, non-Fibre Channel based speeds allowed)
Connectors	(2) SFP sockets accepting either copper or fibre optic transceivers Micro DB15 connector for Triggers and IRIG
Backplane	PCI Express Peripheral Module - x4 PCI Express 2.0
Power Consumption	10 Watts (active, 2 ports full line rate)
Operating Temp. Range	0° C to +45° C ambient
Storage Temp. Range	-45º C to +85º C
Humidity	5 to 95% non-condensing

PROTOCOL SUPPORT

- FC-AE-ASM
- FC-AE-RDMA
- FC-AE 1553
- FC-AV
- ARINC-818
- MIL-STD-1760E (HS1760)
- SAE Profiles —AS5653, AS5725, AS5726

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