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1553 PCI CARD

User's Manual

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PREFACE

The 1553 PCI CARD provides an intelligent interface between a PCI slot in a PC compatible computer and up to four (4) MIL-STD-1553 channels. The card is designed and manufactured by TEST SYSTEMS, Inc., in Phoenix, Arizona. TEST SYSTEMS, Inc., is an Arizona corporation, and has been specializing in MIL-STD-1553 test equipment since 1979.

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1.0 INTRODUCTION

The 1553 PCI CARD provides an intelligent interface between a PCI slot in a PC compatible computer and up to four (4) MIL-STD-1553 channels. Each channel is dual standby redundant and can operate as a Bus Controller (BC), Remote Terminal (RT), Bus Monitor (BM) or Remote Terminal/Bus Monitor (RT/M). This allows it to be used in developing, testing and simulating the MIL-STD-1553 bus functions from a personal computer.

1.1 Organization of Manual

Section 1 presents a brief introduction to the capabilities of the 1553 PCI CARD. Section 2 provides electrical, environmental and physical specifications. Section 3 describes the board-level configuration of the card. Section 4 discusses the operation of the card. Section 5 explains how to program the card and use the software provided with the card.

1.2 Installation

The 1553 PCI CARD can be provided with up to four (4) modules where each module is a dual standby redundant MIL-STD-1553 channel. The card has a 25 pin D-subminiature female connector to provide the connections to the 1553 data bus networks and the Trigger Output from the channels. Each of the channels provides for either direct coupled or transformer coupled connections to the data bus (see section 3.1). The data bus connectors must be terminated properly into a resistive load or a bus network. The SuMMIT chip in each of the channels may be configured through external pins on the modules or through internal control register bits (depending on the state of the *LOCK pin). Pads are provided to set the external configuration pins of the SuMMIT (see section 3.2). Following installation, it is recommended that the 1553 PCI CARD Test Program be run to verify operation of the card (see section 5.1).

1.3 Operation

The 1553 PCI CARD has up to four (4) modules where each module is a dual standby redundant MIL-STD-1553 channel. Each 1553 channel has a 1553 interface, 128K words (16 bit) of memory, a

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status/control register and control logic. For the 1553 interface the 1553 channel uses the SuMMIT from United Technologies Microelectronics Center to manage the critical functions of the MIL-STD-1553 protocol. The PC has full access and control of the SuMMIT. The 32 registers internal to the SuMMIT and the status/control register are mapped into the upper part of memory on the module. The operation of each of the 1553 channels on the 1553 PCI CARD is based on the combination of the information written into the 32 16 bit registers in the SuMMIT and the information written to various blocks in memory. For detailed operation of the SuMMIT refer to the SuMMIT Product Handbook from United Technologies Microelectronics Center, Inc., 1575 Garden of the Gods Road, Colorado Springs, CO 80907, (800)722-1575.

1.4 Software

The 1553 PCI CARD Driver, the WINDOWS 1553 PCI CARD DLL and the 1553 PCI CARD Test Program are provided with the 1553 PCI CARD.

The 1553 PCI CARD Test Program is provided so that it can be run to verify that the 1553 PCI CARD is functioning properly. Sample programs with source code are provided with the WINDOWS 1553 PCI CARD DLL to illustrate the use of the functions in the DLL to aid in developing custom application software.

2.0 SPECIFICATIONS

Card Size: 4.25" by 9.0"

Memory: 128K words / channel

Word Size: 16 bits

Communication Protocol: MIL-STD-1553 A or B

Data Bus: Dual Standby Redundant

Data bus Coupling: Transformer or Direct

Voltage: +5 V ± 5%

Current Drain: 0.9 Amps Maximum / channel

Operating Temperature Range: 0 to 40 Degrees Celsius

Storage Temperature Range: -25 to +85 Degrees Celsius

Relative Humidity: 10% to 90% Noncondensing

Connector: 25 pin D-subminiature female

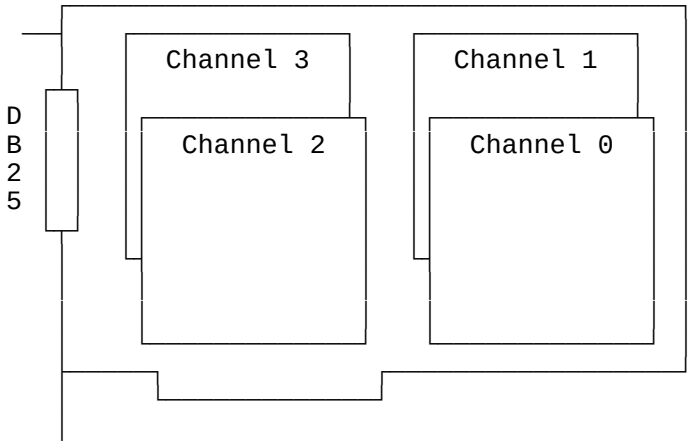
Pin #	Description	Pin #	Description
1	2BH	14	3BH
2	2BL	15	3BL
3	2AH	16	3AH
4	2AL	17	3AL
5	2T	18	3T
6	2G	19	3G
7	-	20	1BH
8	0BH	21	1BL
9	0BL	22	1AH
10	0AH	23	1AL
11	0AL	24	1T
12	0T	25	1G
13	0G		

2BH = Channel 2 Bus B High
2T = Channel 2 Trigger Output
2G = Channel 2 Ground Return

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3.0 CARD CONFIGURATION

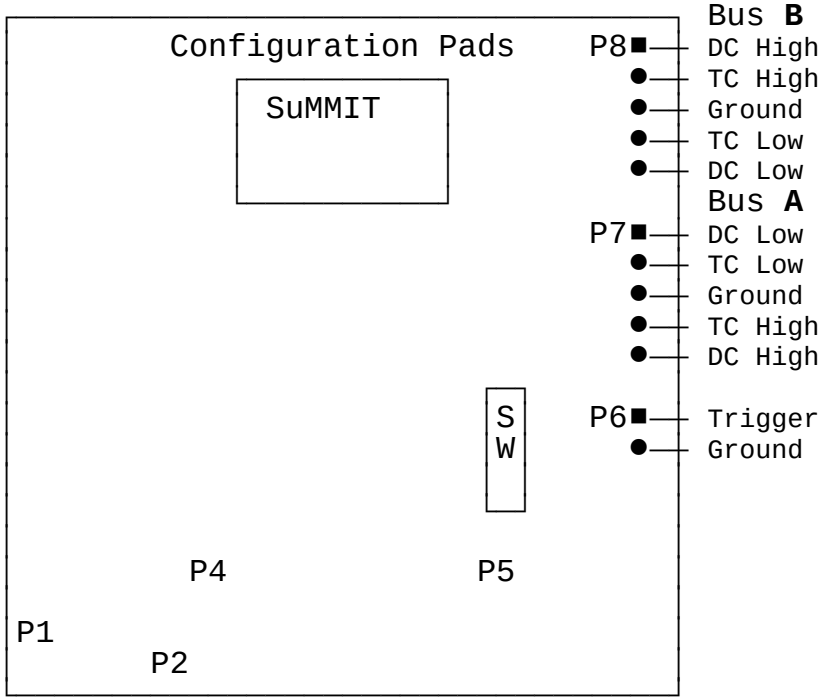
The 1553 PCI CARD can be provided with up to four (4) modules where each module is a dual standby redundant MIL-STD-1553 channel. For a single 1553 channel, one module is provided for Channel 2. For two 1553 channels, two modules are provided for Channel 0 and Channel 2. For three or four 1553 channels, three or four modules are provided where the third and fourth module provide for Channel 3 and Channel 1 respectively. Modules for Channel 2 and Channel 3 and modules for Channel 0 and Channel 1 are stacked. When there are three or four channels on the card and the modules are stacked, the card exceeds the thickness form factor for PCI and requires space from the adjacent slot.



The user can change the form of bus coupling and select the optional SuMMIT configuration on each of the modules on the 1553 PCI CARD. In addition, switch position 8 on the DIP switch on the modules must be set to ON for Channel 2 and Channel 0 and it must be set to OFF for Channel 3 and Channel 1.

3.1 Bus Coupling

Each module can be connected transformer coupled or direct coupled to the 1553 data bus. The 1553 PCI CARD is configured from the factory to be connected to a transformer coupled stub of the 1553 data bus. The user can change the form of coupling by connecting to the appropriate pins on the P7 and P8 connectors on the modules which go to the 25 pin D-subminiature connector. For transformer coupling, pins 2 and 4 on the P7 and P8 connectors are connected. To change to direct coupling, connect to pins 1 and 5 on the P7 and P8 connectors.

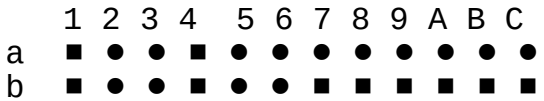


3.2 Optional Configuration

The SuMMIT may be configured through external pins or through internal control register bits (depending on the state of the LOCK pin). Pads are provided to install jumpers to set the external configuration pins of the

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SuMMIT for LOCK, A/B STD, MODE M0 & M1 and the RT ADDRESS & PARITY. All pins except the RT ADDRESS & PARITY have jumpers on the bottom side of the module PCB which must be cut if the configuration is to be changed. The configuration pads are located above the SuMMIT on the module.



3.2.1 LOCK

The jumper pads for the LOCK pin are b:1,2,3. The factory default for the LOCK pin is unlocked with a jumper from b:1 to 2. This allows the SuMMIT to be configured through the internal control registers. If the jumper from b:1 to 2 is removed and a jumper is installed from b:2 to 3 the SuMMIT will be configured from the configuration pins and cannot be changed through the internal control registers.

3.2.2 A/B STD

The jumper pads for the A/B STD pin are a:1,2,3. The factory default for the A/B STD pin is B STD with a jumper from a:2 to 3. To change the default to the A STD, cut the jumper on the bottom side from a:2 to 3 and installed a jumper from a:1 to 2.

3.2.3 MODE M0 & M1

The jumper pads for the MODE M0 & M1 pins are a:4,5,6 and b:4,5,6. The factory default for mode is BC. The MODE M0 & M1 pins have jumpers from a:5 to 6 and b:5 to 6. To change the default to another mode of operation, cut the jumpers on the bottom side from a:5 to 6 and b:5 to 6 and installed jumpers as shown below:

Mode	MODE M0 JUMPER	MODE M1 JUMPER
BC	b:5 - 6	a:5 - 6
RT	b:4 - 5	a:5 - 6
BM	b:5 - 6	a:4 - 5
RT/M	b:4 - 5	a:4 - 5

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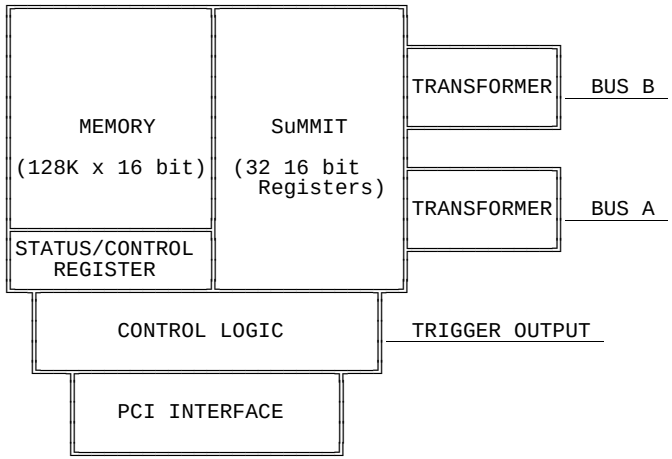
3.2.4 RT ADDRESS & PARITY

The jumper pads for the RT ADDRESS & PARITY pins are b:7 to C (RTA4 - b:7, RTA3 - b:8, RTA2 - b:9, RTA1 - b:A, RTA0 - b:B, RTPTY - b:C). Ground is provided on pads a:7 to C. The default is a logic 'one' with no jumper installed. To set the default RT ADDRESS or PARITY bit to a logic 'zero' install a jumper for the desired bit.

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4.0 CARD OPERATION

A Block Diagram of the 1553 PCI CARD with one 1553 channel is shown below. The PCI Interface can control up to four 1553 channels. A brief description of the operation is given in the following sections.



4.1 PCI Interface

The 1553 operation of the 1553 PCI CARD is controlled by transferring information to and from Memory for the 1553 channel. The PCI Interface is implemented using the PCI 9052 from PLX Technology in Sunnyvale, CA. The PCI Interface provides for four (4) memory regions of 128K words (256K bytes) each, identified as S0, S1, S2 and S3. Memory region S0 is for Channel 0, S1 for Channel 1, S2 for Channel 2 and S3 for Channel 3. The base for each memory region is established during system initialization. Memory for the 1553 channel is addressed as 16 bit words. The Status/Control Register and the 32 internal registers in the SuMMIT are mapped into the upper 33 words of Memory on a channel. The Status/Control Register is mapped to location 0x1FFDF and the 32 internal registers in the SuMMIT are mapped to locations 0x1FFE0 to 0x1FFFF with Register 0 at 0x1FFE0.

4.2 Status/Control Register

The Status/Control Register provides additional information and control for the operation of the 1553 channel. A read of Memory location base+0x1FFDF provides the channel Status. A write to Memory location base+0x1FFDF provides the channel Control. The Status Definition and Control Function for the 16 bits in the Status/Control Register are as follows:

Bit	Status Definition	Control Function
15	0	Reset Page Switch Enable
14	Page Switch Enable	Set Page Switch Enable
13	0	Reset SuMMIT Page
12	SuMMIT Page Status	Set SuMMIT Page
11	0	N/A
10	0	N/A
9	0	Reset Timer Resolution
8	Timer Resolution	Set Timer Resolution
7	Ready Status	Master Reset SuMMIT
6	Terminal Active Status	N/A
5	0	Reset Subsystem Flag
4	Subsystem Flag	Set Subsystem Flag
3	0	Reset Interrupt Enable
2	Interrupt Enable	Set Interrupt Enable
1	You Fail Interrupt	Reset You Fail Interrupt
0	Message Interrupt	Reset Message Interrupt

Bit 15 is the most significant bit.

4.2.1 Description of Status Register Bits

The Message Interrupt signal (MSG_INT) from the SuMMIT is a 125 ns pulse which is latched and provided in bit 0. The You Fail Interrupt signal (YF_INT) from the SuMMIT is a 125 ns pulse which is latched and provided in bit 1. Once an interrupt is latched the status bit will remain high until it is reset by writing the appropriate bit in the Control Register. The channel interrupts can be enabled or disabled by writing to the Control Register and a 'one' in bit 2 of the Status Register indicates the channel interrupts are enabled.

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When the channel is used as an RT, the Subsystem Flag bit in the 1553 RT status word can be set by writing to SuMMIT Register 9 or by writing to the Control Register. A 'one' in bit 4 of the Status Register indicates the Subsystem Flag has been set from the Control Register.

Bit 6 provides Terminal Active status from the SuMMIT which indicates that the SuMMIT is actively processing a 1553 command. Bit 7 provides Ready status from the SuMMIT which indicates that the SuMMIT has completed initialization or BIT, and regular execution may begin.

Bit 8, Timer Resolution, indicates the frequency selected and applied to the Timer Clock input to the SuMMIT. When Timer Resolution is a 'zero' the Timer Clock frequency is 250 KHz yielding a timer resolution of 4 us. When Timer Resolution is a 'one' the Timer Clock frequency is approximately 976 Hz yielding a timer resolution of 1,024 us. Note that the internal frequency of 24 MHz yields a timer resolution of 64 us. To use the Timer Clock frequency for a timer resolution of 4 us or 1,024 us, bit 10 of Register 0 in the SuMMIT must be set to a 'one'.

Bit 12, SuMMIT Page Status, indicates which page of memory the SuMMIT is set to access. A 'zero' in bit 12 indicates Page 0 and a 'one' indicates Page 1.

When automatic page switching is enabled, bit 14, Page Switch Enable, is set to a 'one'.

4.2.2 Description of Control Register Bits

When a 'one' is written to a bit in the Control Register, the function of that bit is executed. When writing to the Control Register, if both the Set and the Reset bits are 'one' for Interrupt Enable, Subsystem Flag, Timer Resolution, SuMMIT Page and Page Switch Enable, the function is reset. To actually set Page Switch Enable, the SuMMIT must be in the monitor mode.

4.3 Interrupts

The SuMMIT can be configured to generate two different interrupts during operation. The interrupts are 125 ns pulses which are latched in the channel Status Register. The interrupts will be sent to the PCI Interface if

interrupts are enabled (channel status bit 2 is 'one'). The interrupt from Channel 0 and the interrupt from Channel 1 are ORed together to generate the Local Interrupt 1 in the PCI Interface. The interrupt from Channel 2 and the interrupt from Channel 3 are ORed together to generate the Local Interrupt 2 in the PCI Interface. Once the PC is interrupted, the channel Status Register can be read to determine which interrupt caused the interrupt. The interrupt must be reset by writing to the channel Control Register. If interrupts are not enabled (channel status bit 2 is 'zero'), the interrupts can be polled by reading the channel Status Register. Interrupt Enable is set or reset by writing to the channel Control Register.

4.4 Memory Control

Since the SuMMIT can only directly address 64K of memory, the 128K words of memory is divided into two pages of 64K words each. Page 0 is the lower half of memory and Page 1 is the upper half of memory. Page selection is controlled via the Status/Control Register. The upper 33 words of Page 1 are used for the Status/Control Register and the 32 internal registers in the SuMMIT and are not be used for SuMMIT operation or data.

4.5 SuMMIT Operation

The SuMMIT operation is based on the combination of the information written into the 32 16 bit registers in the SuMMIT and the information written to various blocks in memory. The SuMMIT can be set up to operate as a Bus Controller (BC), Remote Terminal (RT), Bus Monitor (BM) or Remote Terminal/Bus Monitor (RT/M). For detailed operation of the SuMMIT refer to the SuMMIT Product Handbook from United Technologies Microelectronics Center, Inc., 1575 Garden of the Gods Road, Colorado Springs, CO 80907, (800)722-1575.

4.6 Monitor Operation

A 1553 channel on a 1553 PCI CARD can be configured for monitor operation either with or without automatic page switching.

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4.6.1 Monitor Without Automatic Page Switching

The monitor is setup by writing registers in the SuMMIT. If bit 14 of the channel Status Register is a 'zero', automatic page switching is not enabled. Once the monitor is setup and started by the PC, it runs autonomously until the operation is stopped. The application software, however, must unload the monitored data before new monitored data overwrites it. This is overhead for the application program.

4.6.2 Monitor With Automatic Page Switching

A 1553 channel on a 1553 PCI CARD can be enabled for automatic page switching by writing a 'one' to bit 14 of the Control Register after the SuMMIT has been configured as a monitor. For proper operation of the automatic page switching, the SuMMIT must be configured with the Monitor Block Count Interrupt enabled and the Message Error Interrupt masked.

When all the monitor blocks have been written, the SuMMIT Page is toggled and a Message Interrupt is generated. This interrupt can be used as a 1/2 full interrupt so the application software can then unload all the monitored data in the monitor blocks from the other SuMMIT Page.

4.7 Trigger Output

A Trigger Output is provided as a 665 ns active high pulse. The Trigger Output is generated from the Message Interrupt (MSG_INT) signal from the SuMMIT.

For Bus Controller operation the Interrupt/Continue op code can be used in a command block at the beginning of a frame to provide a Trigger Output at the beginning of the frame. (Other conditions that could cause a message interrupt should be masked in register 3.)

For Remote Terminal operation specific subaddresses or mode commands could be configured for Interrupt When Accessed. A Trigger Output would indicate that the specific valid command was received.

For Bus Monitor operation when Page Switch Enable is set the Trigger Output is delayed till monitor block 0 is complete. If Page Switch Enable is not set, the Trigger Output occurs after monitor block 1 is complete.

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5.0 SOFTWARE SUPPORT

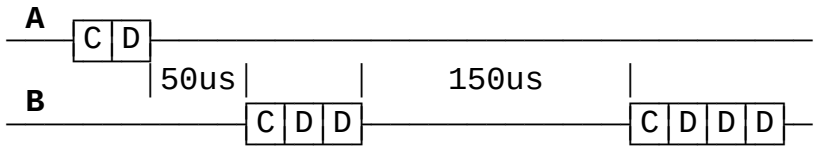
The 1553 PCI CARD Driver, the WINDOWS 1553 PCI CARD DLL and the 1553 PCI CARD Test Program are provided with the 1553 PCI CARD.

5.1 1553 PCI CARD Test Program

The 1553 PCI CARD Test Program is provided so that it can be run to verify that the 1553 PCI CARD is functioning properly.

5.1.1 1553 PCI CARD Verification

Install the 1553 PCI CARD in the PC following the installation information given in section 1.2. Install a restive load on the data bus connectors of 70 ohms for Transformer coupled or 35 ohms for Direct coupled. Connect a scope probe across each of the load resistors. Run the Test Program and observe the waveforms on Bus A and Bus B for the following patterns:



5.2 WINDOWS 1553 PCI CARD DLL

The WINDOWS 1553 PCI CARD DLL is a Dynamic Link Library (DLL) that provides the basic support for programming in Windows or LabView to operate the 1553 PCI CARD. Sample programs with source code are provided to illustrate the use of the functions in the DLL to aid in developing custom application software.

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5.2.1 1553 PCI CARD Programming

The 1553 PCI CARD has four memory regions of 128K words each and up to four 1553 channels. Each channel has a Status/Control Register and the 32 16 bit registers in the SuMMIT mapped into the upper part of memory. The sample programs with source code provide simple examples to illustrate initialization and operation of a channel on the card.

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