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TEWS TECHNOLOGIES

TIP114

10 Channel Absolute Encoder Interface (SSI)

Version 1.0

User Manual

Issue 1.0.10

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TIP114-10

10 Channel Absolute Encoder Interface (SSI)

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	November 1998
1.1	Add Current Requirement	March 2000
1.2	General Revision	October 2003
1.3	Change of Control Register description	September 2004
1.4	New address TEWS LLC	September 2006
1.5	New Board Revision	August 2007
1.6	Amended missing reset register values	November 2007
1.0.7	New notation for HW Engineering Documentation Releases	December 2008
1.0.8	Changed Temperature Range to Extended Temperature	November 2009
1.0.9	New Board Revision with improved Clock Output Protection	December 2010
1.0.10	Added “SSI Short Description”	December 2012

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1 Product Description

The TIP114 is an IndustryPack® compatible module for motion control applications.

The TIP114 offers ten independent SSI interfaces with programmable clock rates from 1µs to 15µs and programmable data bits from 1 bit to 32 bit. The position feedback is provided by an absolute encoder with a synchronous serial interface (SSI) and a corresponding 32 bit (maximum) shift register at the IP. The level of the encoder signals is RS422.

The data inputs are galvanically isolated by high speed optocouplers. Each SSI channel can handle a data stream which is encoded in Binary or in Gray Code, without or with parity as well as with even or odd parity.

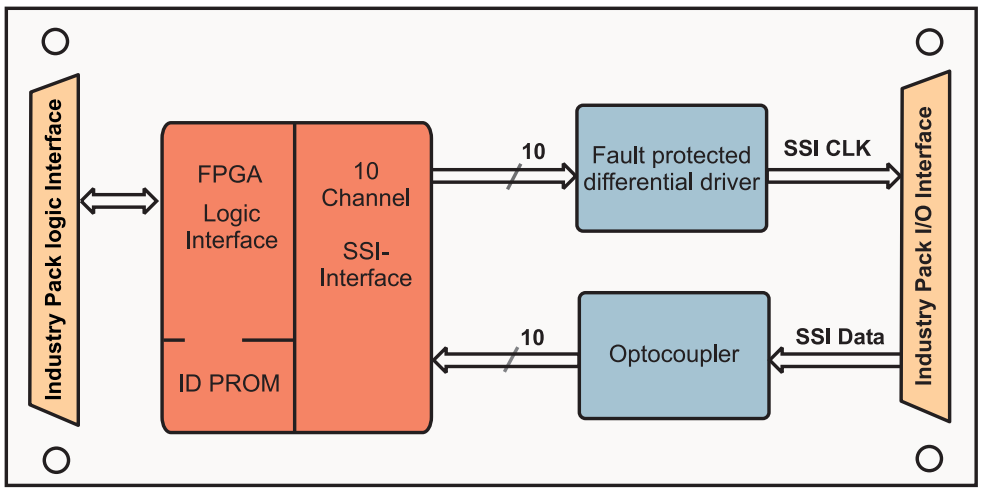


Figure 1-1 : Block Diagram

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2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used with no wait states	
Memory Space	Not used	
Interrupts	Only INTREQ0# is used	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
SSI Interface	10 independent channels	
SSI Data Input	Optically isolated differential input	
SSI CLK Output	Fault protected MAX3441E differential driver, additional protection with SM712 TVS array	
SSI Clock Rate	Programmable from 1µs to 15µs	
SSI Data word length	Programmable from 1 bit to 32 bit	
Interrupts	IP interrupt 0 for all 10 SSI channels; 2 registers and one Interrupt Vector for individual interrupt handling	
Interface Connector	50-conductor flat cable	
Power Requirements	50mA typical @ +5V DC, no load	
Physical Data		
Temperature Range	Operating Storage	-40°C to +85°C -45°C to +125°C
MTBF	440000 h	
Humidity	5 – 95 % non-condensing	
Weight	25 g	

Table 2-1 : Technical Specification

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3 ID PROM Contents

Address	Function	Contents
0x01	ASCII 'I'	**0x49**
0x03	ASCII 'P'	**0x50**
0x05	ASCII 'A'	**0x41**
0x07	ASCII 'C'	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x2A**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0D**
0x17	CRC	**0xC3**
0x19	Version -10	**0x0A**

Table 3-1 : ID PROM Contents

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4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP114 is accessible in the I/O space of the IP.

Address	Symbol	Description	Size (Bit)	Access
0x00	CONT0	Control Register Channel 0	16	R/W
0x02	DATAL0	Data Word Low Channel 0	16	R/W
0x04	DATAH0	Data Word High Channel 0	16	R
0x06	CONT1	Control Register Channel 1	16	R/W
0x08	DATAL1	Data Word Low Channel 1	16	R/W
0x0A	DATAH1	Data Word High Channel 1	16	R
0x0C	CONT2	Control Register Channel 2	16	R/W
0x0E	DATAL2	Data Word Low Channel 2	16	R/W
0x10	DATAH2	Data Word High Channel 2	16	R
0x12	CONT3	Control Register Channel 3	16	R/W
0x14	DATAL3	Data Word Low Channel 3	16	R/W
0x16	DATAH3	Data Word High Channel 3	16	R
0x18	CONT4	Control Register Channel 4	16	R/W
0x1A	DATAL4	Data Word Low Channel 4	16	R/W
0x1C	DATAH4	Data Word High Channel 4	16	R
0x1E	CONT5	Control Register Channel 5	16	R/W
0x20	DATAL5	Data Word Low Channel 5	16	R/W
0x22	DATAH5	Data Word High Channel 5	16	R
0x24	CONT6	Control Register Channel 6	16	R/W
0x26	DATAL6	Data Word Low Channel 6	16	R/W
0x28	DATAH6	Data Word High Channel 6	16	R
0x2A	CONT7	Control Register Channel 7	16	R/W
0x2C	DATAL7	Data Word Low Channel 7	16	R/W
0x2E	DATAH7	Data Word High Channel 7	16	R
0x30	CONT8	Control Register Channel 8	16	R/W

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Address	Symbol	Description	Size (Bit)	Access
0x32	DATAL8	Data Word Low Channel 8	16	R/W
0x34	DATAH8	Data Word High Channel 8	16	R
0x36	CONT9	Control Register Channel 9	16	R/W
0x38	DATAL9	Data Word Low Channel 9	16	R/W
0x3A	DATAH9	Data Word High Channel 9	16	R
0x3C	READY	Data Ready Status Register	16	R
0x3E	PAR_ERR	Parity Error Status Register	16	R
0x40	INTSTAT	Interrupt Status Register	16	R/W
0x42	INTENA	Interrupt Enable Register	16	R/W
0x45	INTVEC	Interrupt Vector Register	8	R/W
0x47	CONVERT	Start Convert CH0-CH9 Register	8	W

Table 4-1 : Register Set

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4.2 Control Register Channel X

The Control Register is used to program the clock speed, parity, the data encoding of the SSI encoder and the number of data bits coming from the serial absolute encoder. Each of the ten SSI interfaces can be configured independently of the other by the corresponding Control Register.

This register is cleared automatically with the IP_RESET signal.

Bit	Symbol	Description	Access	Reset Value
15:14		Unused		
13	BC5	Number of Data Bits Bits are used to program the number of bits of the serial absolute encoder. It can be read and written by software. The data bits can be programmed in the range from 1 to 32. BC5 .. BC0 = 0x01 to 0x20 means 1 to 32 bit. BC5 .. BC0 = 0x00 not used BC5 .. BC0 = 0x21 to 0x3F not used	R/W	0
12	BC4			
11	BC3			
10	BC2			
9	BC1			
8	BC0			
7	Gray Code	Gray Code to transmit the data 1 = Gray Code 0 = Binary Code	R/W	0
6	With Zero Bit	Parity Bit with Zero Bit, controls the clock cycles 1 = two additional clock cycles 0 = one additional clock cycle are provided to get the parity bit	R/W	0
5	Even / Odd	Controls the parity detection 1 = odd parity 0 = even parity This bit is only useful if bit 4 is set to '1'.	R/W	0
4	With Parity	Encoder with parity - If encoder provides a parity bit: 1 = detect parity errors	R/W	0
3	CR3	Clock Rate for encoder serial clock speed The clock can be programmed in steps of 1µs in the range of 1 to 15. A value of 0 for the clock rate is not allowed and will stop the operation of the SSI interface.	R/W	0
2	CR2			
1	CR1			
0	CR0			

Table 4-2 : Control Register Channel X

Note that a value of 0x00 for BC5 .. BC0 is not used and will result an invalid SSI Data.

A value from 0x21 to 0x3F will also result an invalid SSI Data because of the limited 32 bit input shift register of the TIP114.

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4.3 Data Word Low Channel X

The serial data of the encoder is shifted into the word wide registers Data Word Low and Data Word High. The Data Word Low Register holds the least significant word of the 32 bit shift register.

With a write access to the Data Word Low Register Channel X the data transfer from the encoder is initiated independently of the other channels.

This register is cleared automatically with the IP_RESET signal.

The data register is undefined if the serial data transfer is in progress (the corresponding ready bit is read as '0').

4.4 Data Word High Channel X

The serial data of the encoder is shifted into the word wide registers Data Word Low and Data Word High. The Data Word High Register holds the most significant word of the 32 bit shift register.

This register is cleared automatically with the IP_RESET signal.

The data register is undefined if the serial data transfer is in progress (the corresponding ready bit is read as '0').

4.5 Ready Status Register

The Ready Status Register is a word wide read only register. This register indicates that the data transfer between the encoder is completed and the position data can be read.

After IP_RESET this register is read as 0x03FF.

Bit	Symbol	Description	Access	Reset Value
15:10		Always as '0'		
9:0	RDY9 …. RDY0	Ready Bit of Channel X 1 = Data Ready 0 = data transmission in progress	R	0x3FF

Table 4-3 : Ready Status Register

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4.6 Parity Error Status Register

The Parity Status Register is a word wide read only register. The register indicates that a parity error is detected at the last data transmission.

The parity error status is updated only if the parity enable bit of the corresponding channel is set to '1'. Otherwise the parity status is read as '0'.

This register is cleared automatically with the IP_RESET signal.

Bit	Symbol	Description	Access	Reset Value
15:10		Always as '0'		
9:0	Parity Error 9 …. Parity Error 0	Parity Error of Channel X 1 = parity Error 0 = no error	R	0

Table 4-4 : Parity Error Status Register

4.7 Interrupt Status Register

The Interrupt Status Register is a word wide read/write only register.

The interrupt status is updated only if the interrupt enable bit of the corresponding channel is set to '1'. Otherwise the interrupt status is read as '0'.

This register is cleared automatically with the IP_RESET signal.

Bit	Symbol	Description	Access	Reset Value
15:10		Always as '0'		
9:0	Interrupt Status 9 …. Interrupt Status 0	Interrupt Status of Channel X 1 = Data Ready Interrupt channel x 0 = no interrupt To quit the interrupt status writing a '1' to the corresponding bit.	R/W	0

Table 4-5 : Interrupt Status Register

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4.8 Interrupt Enable Register

The Interrupt Enable Register is a word wide read/write register. The register controls the data ready interrupt of the channel 0 to channel 9.

This register is cleared automatically with the IP_RESET signal.

Bit	Symbol	Description	Access	Reset Value
15:10		Always as '0'		
9:0	Interrupt Enable 9 …. Interrupt Enable 0	Interrupt Enable of Channel X 1 = Data Ready Interrupt enabled channel x 0 = interrupt disabled	R/W	0

Table 4-6 : Interrupt Enable Register

4.9 Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register. It is cleared automatically with the IP_RESET signal. Interrupt vector is loaded by software.

4.10 Start Convert CH0-CH9 Register

The Start Convert Register is a byte wide write only register. It is used to start the data transmission for all SSI channels simultaneously.

If the clock rate is set to 0x00 in a Control Register Channel X the corresponding SSI channel don't start the data transmission.

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5 Functional Description

5.1 SSI Short Description

The Synchronous Serial Interface (SSI) is based on two differential signal lines, CLOCK and DATA. The CLOCK line is an input, the DATA line is an output of the absolute encoder.

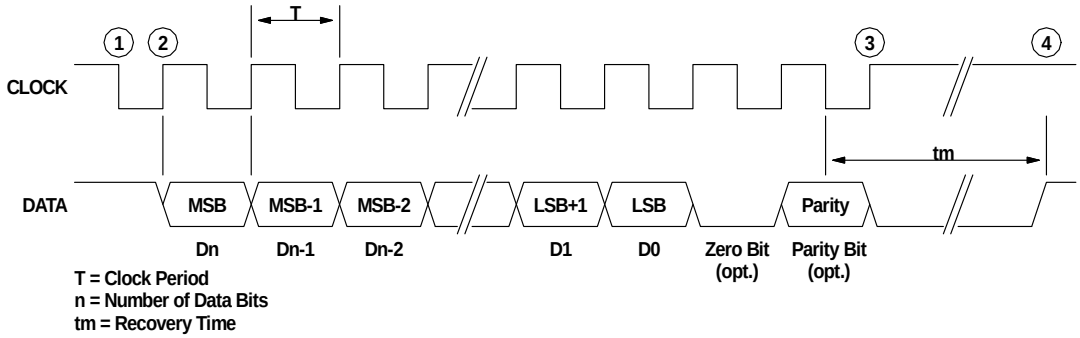


Figure 5-1 : SSI Timing Example

When not transmitting, the clock and data lines are high. To read out the positional data of an absolute encoder, the controller transmits a pulse train on the CLOCK line. The first falling edge of CLOCK ① latches the positional data of the absolute encoder. At the first rising edge of CLOCK ② the absolute encoder presents the most significant bit on the DATA line. On each subsequent rising edge in the CLOCK pulse train the next bit in order is transmitted to the controller.

In addition to the data bits the absolute encoder can transmit a parity bit for error detection. As an option a zero bit can be placed between the data and the parity bit.

After all bits are transmitted ③, the absolute encoder holds the data line low for 10-30µs (recovery time tm). After that the absolute encoder is ready for a new transmission ④. A new transmission must not started before ④.

The maximum achievable baud rate depends on the propagation delay depending of cable length, the internal propagation delay of the TIP114 and the clock to data delay of the encoder. The sum of all delay must be smaller than the clock period to archive a reliable signal transfer.

TIP114 → Cable Delay → Sensor → Cable Delay → TIP114

The internal propagation delay of the TIP114 is about 250 ns and includes driver and receiver delays. A typical cable delay is about 7 ns/m, cables should be twisted pair and screened. Both ways, TIP114 to sensor, and sensor back to TIP114, must be included in the calculation.

Typical achievable baud rate are:

Cable length (m)	Baud rate (kHz)
< 50	< 400
< 100	< 300
< 200	< 200
< 400	< 100

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6 Pin Assignment – I/O Connector

Pin	Signal	Comment
1	DATA0 +	SSI DATA +
2	DATA0 -	SSI DATA -
3	CLK0 +	SSI CLK +
4	CLK0 -	SSI CLK -
5	GND	Clock Signal Ground
6	GND	Clock Signal Ground
7	DATA1 +	SSI DATA +
8	DATA1 -	SSI DATA -
9	CLK1 +	SSI CLK +
10	CLK1 -	SSI CLK -
11	DATA2 +	SSI DATA +
12	DATA2 -	SSI DATA -
13	CLK2 +	SSI CLK +
14	CLK2 -	SSI CLK -
15	GND	Clock Signal Ground
16	GND	Clock Signal Ground
17	DATA3 +	SSI DATA +
18	DATA3 -	SSI DATA -
19	CLK3 +	SSI CLK +
20	CLK3 -	SSI CLK -
21	DATA4 +	SSI DATA +
22	DATA4 -	SSI DATA -
23	CLK4 +	SSI CLK +
24	CLK4 -	SSI CLK -
25	GND	Clock Signal Ground

Pin	Signal	Comment
26	GND	Clock Signal Ground
27	DATA5 +	SSI DATA +
28	DATA5 -	SSI DATA -
29	CLK5 +	SSI CLK +
30	CLK5 -	SSI CLK -
31	DATA6 +	SSI DATA +
32	DATA6 -	SSI DATA -
33	CLK6 +	SSI CLK +
34	CLK6 -	SSI CLK -
35	GND	Clock Signal Ground
36	GND	Clock Signal Ground
37	DATA7 +	SSI DATA +
38	DATA7 -	SSI DATA -
39	CLK7 +	SSI CLK +
40	CLK7 -	SSI CLK -
41	DATA8 +	SSI DATA +
42	DATA8 -	SSI DATA -
43	CLK8 +	SSI CLK +
44	CLK8 -	SSI CLK -
45	GND	Clock Signal Ground
46	GND	Clock Signal Ground
47	DATA9 +	SSI DATA +
48	DATA9 -	SSI DATA -
49	CLK9 +	SSI CLK +
50	CLK9 -	SSI CLK -

Table 6-1 : Pin Assignment I/O Connector

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