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TEWS TECHNOLOGIES

TIP119

Six Channel 16 bit Quadrature Decoder Counter

Version 1.0

User Manual

Issue 1.1

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TIP119-10

Six Channel 16 bit Quadrature Decoder Counter

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1.0	Initial Issue	December 2005
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1 Product Description

The TIP119 is an IndustryPack® compatible module providing six channels of quadrature decoder inputs. Each channel has a dedicated 16 bit wide quadrature decoder counter.

The input signals can be of RS422A and RS423A level and pass a digital filter for noise suppression before they are fed into the counter.

An interrupt can be generated at counter over- or underflow or on assertion of the index input. An 8 bit interrupt vector is supported.

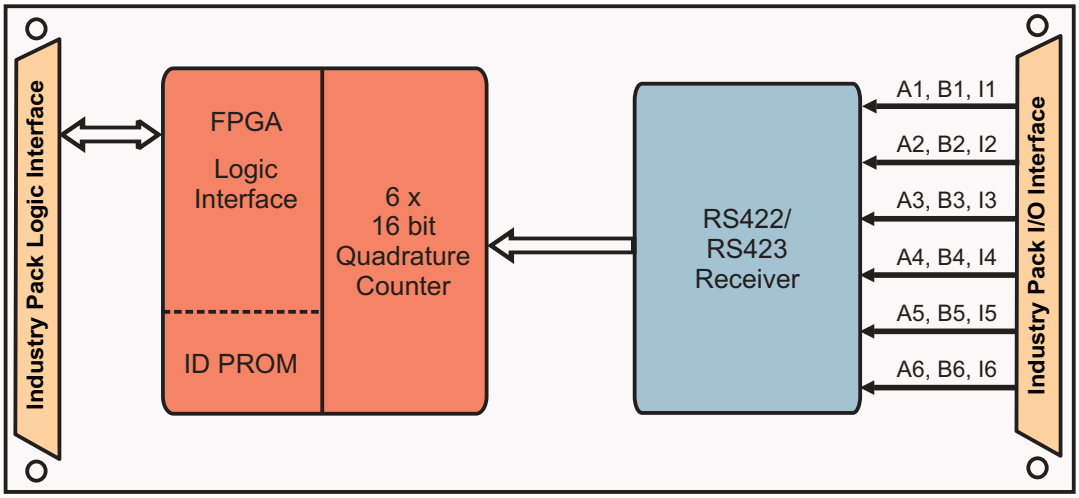


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	1 wait state	
Memory Space	not used	
Interrupts	INT0 / INT1 used	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
I/O Interface		
Interface Connector	50-conductor flat cable	
Input Signal Level	RS422A, RS423A	
Input Common Mode Volt.	±15V	
Input Differential Voltage	±25V	
Input Impedance	220Ω	
Max. Encoder Tracking Freq.	1.3MHz	
Power Requirements	230 mA typical @ +5V DC	
Physical Data		
Temperature Range	Operating Storage	0 °C to +70 °C -40°C to +125°C
MTBF	738000 h	
Humidity	5 – 95 % non-condensing	
Weight	26 g	

Figure 2-1 : Technical Specification

3 ID PROM Contents

Address	Function	Contents
0x01	ASCII ‘I’	**0x49**
0x03	ASCII ‘P’	**0x50**
0x05	ASCII ‘A’	**0x41**
0x07	ASCII ‘C’	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x3D**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0C**
0x17	CRC	**0xF7**

Figure 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP119 is accessible in the I/O space of the IP.

Address	Symbol	Description	Size (Bit)	Access
0x00	-	Counter channel 1	16	R
0x02	-	Counter channel 2	16	R
0x04	-	Counter channel 3	16	R
0x06	-	Counter channel 4	16	R
0x08	-	Counter channel 5	16	R
0x0A	-	Counter channel 6	16	R
0x0C	-	Reset All Channels Register	16	R
0x0E	-	-	-	-
0x10	-	Overflow Register	16	R/W
0x12	-	Index Register	16	R/W
0x14	-	Up/Down Register	16	R
0x16	-	Interrupt Vector Register	16	W
0x18	-	Interrupt Overflow Mask Register	16	W
0x1A	-	Interrupt Index Mask Register	16	W

Figure 4-1 : Register Set

4.2 Counter Channel

Bit	Symbol	Description	Access	Reset
15:0		Each channel's count can be read with a 16 bit wide read access.	R	0

Figure 4-2 : Counter Channel

The counters multiply the resolution of the input signals by four.

4.3 Reset all Channels

A single read access to this register resets all the channel counters.

4.4 Overflow Register

Bit	Symbol	Description	Access	Reset
15:6		Reserved. Undefined for read access.	-	-
5	CH6	Counter overflow Read access: 0 – asserted (counter overflow) 1 – nonasserted Write: A write clears the state of all channels in the Overflow and the Up/Down Register.	R/W	1
4	CH5		R/W	1
3	CH4		R/W	1
2	CH3		R/W	1
1	CH2		R/W	1
0	CH1		R/W	1

Figure 4-3 : Overflow Register

4.5 Index Register

Bit	Symbol	Description	Access	Reset
15:6		Reserved. Undefined for read access.	-	-
5	CH6	Counter index Read access: 0 – asserted (index passed) 1 – nonasserted Write: A write clears the state of all channels. The register bits stay ‘0’ until cleared.	R/W	1
4	CH5		R/W	1
3	CH4		R/W	1
2	CH3		R/W	1
1	CH2		R/W	1
0	CH1		R/W	1

Figure 4-4 : Index Register

4.6 Up/Down Register

Bit	Symbol	Description	Access	Reset
15:6		Reserved. Undefined for read access.	-	-
5	CH6	Counter up/down Read access: 0 – up 1 – down Bits are set when the corresponding Overflow Register bit is set. This register is cleared by a write to the Overflow Register.	R	1
4	CH5		R	1
3	CH4		R	1
2	CH3		R	1
1	CH2		R	1
0	CH1		R	1

Figure 4-5 : Up/Down Register

4.7 Interrupt Vector Register

Bit	Symbol	Description	Access	Reset
15:8	-	Reserved. Undefined for read access.	-	-
7:1	IVEC	Interrupt Vector	W	0xFE
0	A1	Interrupt acknowledge response This bit reflects the A1 address line during an interrupt acknowledge cycle 0 – INTRQ0 interrupt acknowledge cycle 1 – INTRQ1 interrupt acknowledge cylce	-	0

Figure 4-6 : Interrupt Vector Register

4.8 Interrupt Overflow Mask Register

Bit	Symbol	Description	Access	Reset
15:6	-	Reserved. Undefined for read access.	-	-
5	CH6	Overflow interrupt mask 0 – unmask overflow interrupt. 1 – mask interrupt.	W	1
4	CH5		W	1
3	CH4		W	1
2	CH3		W	1
1	CH2		W	1
0	CH1		W	1

Figure 4-7 : Interrupt Overflow Mask Register

Each of the channels interrupts may be masked by setting the interrupt mask register; the overflow register will have the channel's bit latched asserted but will not cause an interrupt to the host.

4.9 Interrupt Index Mask Register

Bit	Symbol	Description	Access	Reset
15:6	-	Reserved. Undefined for read access.	-	-
5	CH6	Index interrupt mask 0 – unmask Index interrupt. 1 – mask interrupt.	W	1
4	CH5		W	1
3	CH4		W	1
2	CH3		W	1
1	CH2		W	1
0	CH1		W	1

Figure 4-8 : Interrupt Index Mask Register

Each of the channels interrupts may be masked by setting the interrupt mask register; the index register will have the channel's bit latched asserted but will not cause an interrupt to the host.

5 Functional Procedures

5.1 Initialization

- Read to offset 0x0C to reset the counters.
- Clear both Overflow and Index Register.

5.2 Virtual Counter

The interrupt on counter over- or underflows can be used by the software driver to maintain an infinitely wide virtual counter.

- Set up an interrupt service routine for INTRQ0.
- In the ISR increment or decrement the virtual counter, depending on the Up/Down Register bit.
- Reset the Overflow Register to acknowledge the interrupt request.

5.3 Indexing

- Set up an interrupt service routine for INTRQ1.
- Save the counter value in the ISR.
- Reset the Index Register to acknowledge the interrupt request.

The index input is low-active.

5.4 Interrupt Setup

An Interrupt Vector can be set in the lower byte of the Interrupt Vector Register. The vector is presented on an interrupt acknowledge cycle. The D0-bit indicates which interrupt line is going to be acknowledged. Unused channels can be masked in the Interrupt Overflow and Interrupt Index Mask Registers.

6 Pin Assignment – I/O Connector

Pin	Channel	Signal
1	GND	
2	Channel 6	I+
3	Channel 6	I-
4	Channel 6	B+
5	Channel 6	B-
6	GND	
7	Channel 6	A+
8	Channel 6	A-
9	GND	
10	Channel 5	I+
11	Channel 5	I-
12	Channel 5	B+
13	Channel 5	B-
14	GND	
15	Channel 5	A+
16	Channel 5	A-
17	GND	
18	Channel 4	I+
19	Channel 4	I-
20	Channel 4	B+
21	Channel 4	B-
22	GND	
23	Channel 4	A+
24	Channel 4	A-
25	GND	

Pin	Channel	Signal
26	GND	
27	Channel 3	I+
28	Channel 3	I-
29	Channel 3	B+
30	Channel 3	B-
31	GND	
32	Channel 3	A+
33	Channel 3	A-
34	GND	
35	Channel 2	I+
36	Channel 2	I-
37	Channel 2	B+
38	Channel 2	B-
39	GND	
40	Channel 2	A+
41	Channel 2	A-
42	GND	
43	Channel 1	I+
44	Channel 1	I-
45	Channel 1	B+
46	Channel 1	B-
47	GND	
48	Channel 1	A+
49	Channel 1	A-
50	GND	

Figure 6-1 : Pin Assignment I/O Connector

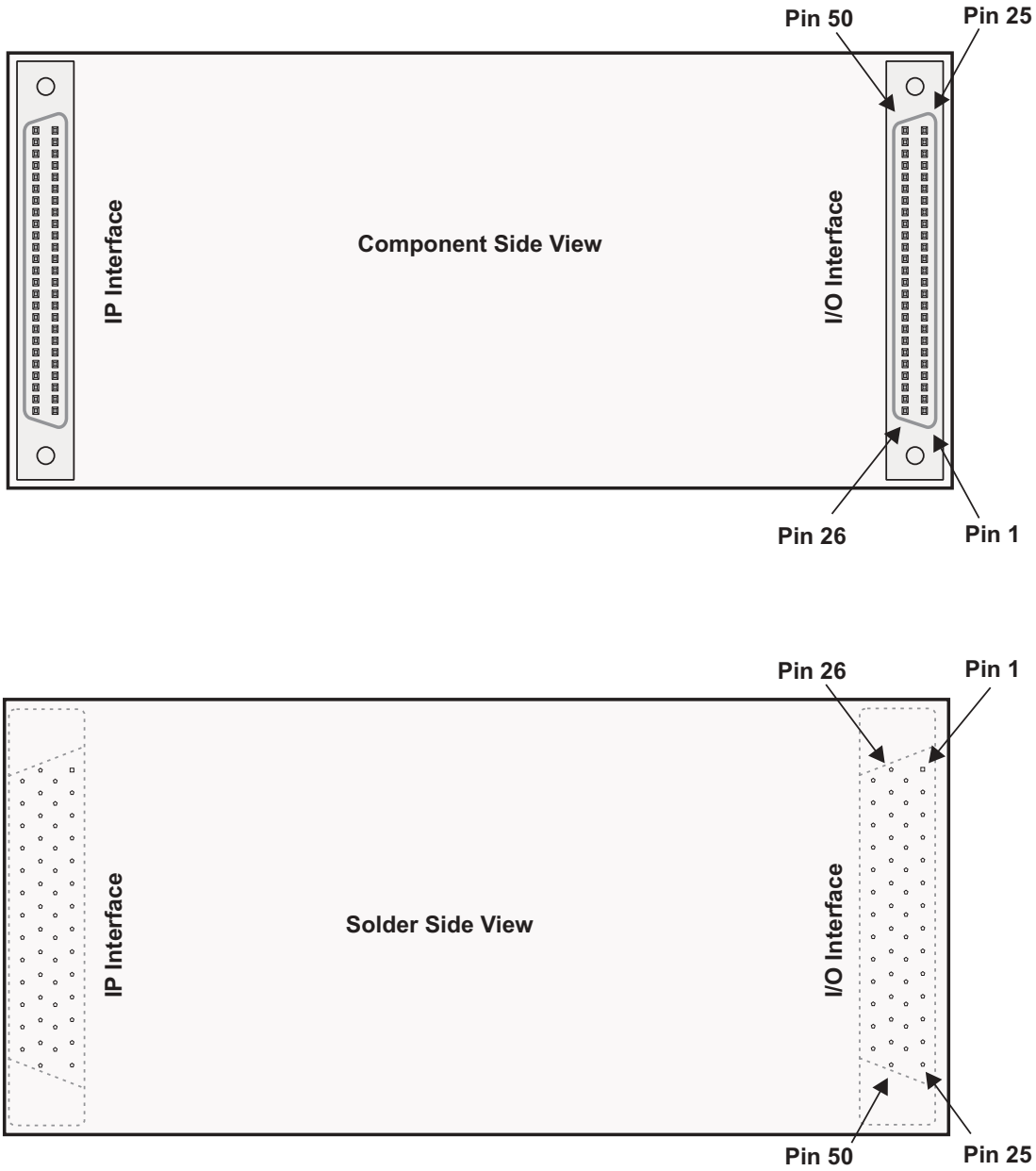


Figure 6-2 : IP Connector Orientation

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