

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

TEWS DATENTECHNIK

TIP102

Motion Controller with
Incremental Encoder Interface
Version 1.0 Revision B

User Manual

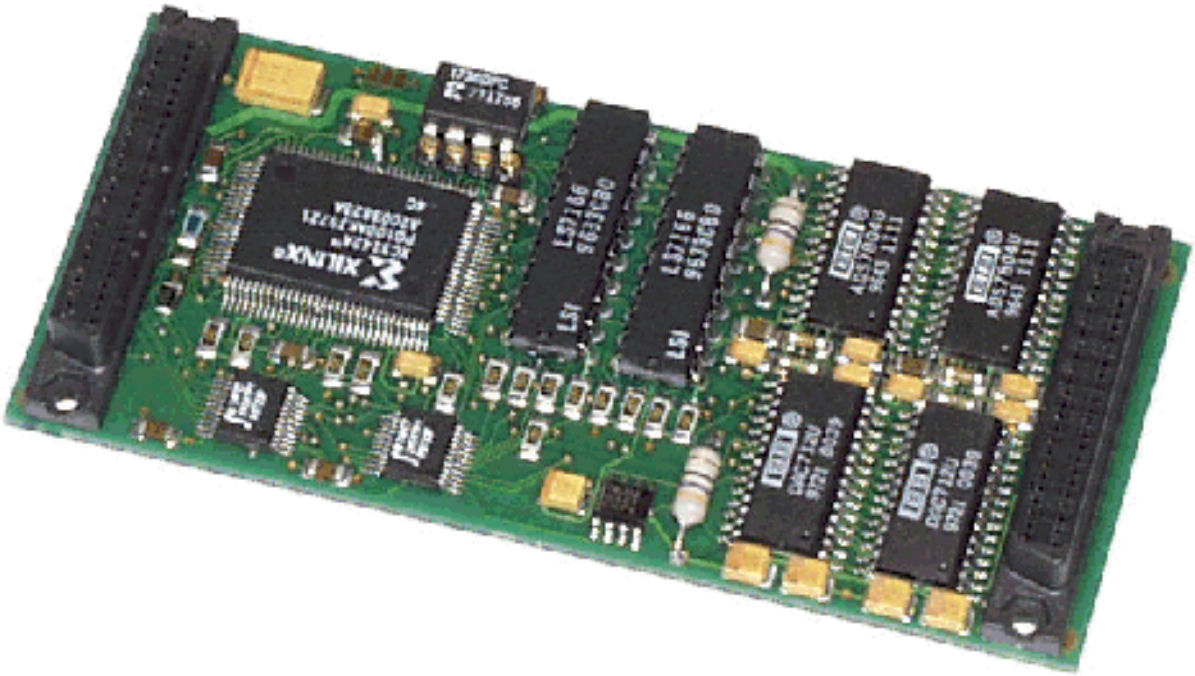
Issue 1.2

09 April 1996

D75102800

TEWS DATEN*TECHNIK* GmbH
Am Bahnhof 7
D-25469 Halstenbek
Germany
Tel. +49 (0) 4101 4058-0
Fax +49 (0) 4101 4058-19

TEWS DATENTECHNIK



TIP102-1x
One axis motion controller with incremental encoder interface

TIP102-2x
Two axis motion controller with incremental encoder interface

This manual covers both products

This document contains information, which is proprietary to TEWS DATEN*TECHNIK* GmbH. Any reproduction without written permission is forbidden.

TEWS DATEN*TECHNIK* GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS DATEN*TECHNIK* GmbH reserves the right to change the product described in this document at any time without notice.

This product has been designed to operate with IndustryPack® compatible carriers. Connection to incompatible hardware is likely to cause serious damage.

TEWS DATEN*TECHNIK* GmbH is not liable for any damage arising out of the application or use of the device described herein.

Issue	Desscription	Date
1.0	First issue	11 April 1994
1.1	Extended	20 Dec 1994
1.2	Technical Spec.	09 april 1996

©1994 by TEWS DATEN*TECHNIK* GmbH
IndustryPack is a registered trademark of GreenSpring Computers, Inc

TEWS DATENTECHNIK

1. Product Description 6

2. Technical Specification 7
2.1. TIP102-XX 7
2.2. TIP102-TM-XX 8

3. ID Prom Contents 9

4. VMEbus Addressing 10
4.1. INPSR Input and Status Register 11
4.1.1. Low Limit Switch Input 11
4.1.2. High Limit Switch Input 11
4.1.3. Reference Switch Input 11
4.1.4. External Trigger Input 11
4.1.5. General Input 11
4.1.6. Encoder Error Status 11
4.1.7. Reference Done Status 12
4.1.8. Interrupt Status 12
4.2. CNTDA Counter Data Register 12
4.2.1. Reading Counter Data 12
4.2.2. Writing Counter Data 12
4.3. CNTCS Counter Control and Status Register 13
4.3.1. MCR Master Control Register 13
4.3.1.1. Reset PR/OL address pointer 13
4.3.1.2. Transfer CNTR to OL 13
4.3.1.3. Reset of CNTR, BWT, CYT, Set sign register 13
4.3.1.4. Transfer PR to CNTR 13
4.3.1.5. Reset COMPT 13
4.3.1.6. Master reset 14
4.3.2. ICR Input Control Register 14
4.3.2.1. A/B Input mode 14
4.3.2.2. Increment counter 14
4.3.2.3. Decrement counter 14
4.3.2.4. A/B input enable 14
4.3.2.5. Configuration ABGT/RCTR 14
4.3.2.6. Configuration LCTR/LLTC 15
4.3.3. OCCR Output Control Register 15
4.3.3.1. Binary / BCD mode 15
4.3.3.2. Interrupt / Trigger mode 16
4.3.4. QR Quadrature Register 16
4.3.4.1. Quadrature mode 16
4.4. DACDA DAC Data Register 17
4.5. ADCCS ADC Control and Status Register 17
4.6. ADCDA ADC Data Register 18
4.7. OUTCR Output Control Register 18
4.7.1. Servo Amplifier Enable 18
4.7.2. Status LED 18
4.8. CONCR Configuration Control Register 19
4.8.1. Reference Mode 19
4.8.2. Auto Reference Enable 19
4.8.3. Encoder Difference Signal 20
4.8.4. Interrupt Enable 20

4.9. Interrupt Vector Register 20

5. Functional Description 21
5.1. Reference Logic 21
5.1.1. Reference Mode - without reference switch 21
5.1.2. Reference Mode - with reference switch 21
5.2. External Trigger Input 22

6. Programming Hints 23
6.1. LS7166 counter chip 23
6.1.1. Initialization 23
6.1.2. Reading actual counter data value 23

7. Jumper Configurations 24
7.1. TIP102-xx IP 24
7.2. TIP102-TM-xx Transition Module 24
7.2.1. Trigger I/O Jumper Configuration 24
7.2.2. Encoder Input Jumper Configuration 24
7.2.3. TIP102-TM-xx Jumper Layout 25

8. IP I/O connector 26
8.1. 50 pin IP I/O connector 26

9. Transition Module 28
9.1. I/O Connection TIP102-TM 28
9.1.1. X1/X201 DB9 female Servo Amplifier Signals 28
9.1.2. X2/X202 DB15 male Power and I/O Signals 28
9.1.3. X3/X203 DB15 female Encoder Signals 29

Figure 1: TIP102-2x Block Diagram 6
Figure 2: ID PROM contents 9
Figure 3: TIP102-1x Register Map 10
Figure 4: TIP102-2x Additional Register Map 10
Figure 5: INPSR Input and Status Register 11
Figure 6: CNTDA Counter Data Register 12
Figure 7: Counter MCR Master Control Register 13
Figure 8: Counter ICR Input Control Register 14
Figure 9: Counter OCCR Output Control Register 15
Figure 10: Counter QR Quadrature Register 16
Figure 11: DACDA DAC Data Register 17
Figure 12: ADCCS ADC Control and Status Register 17
Figure 13: ADCDA ADC Data Register 18
Figure 14: OUTCR Output Control Register 18
Figure 15: CONCR Configuration Control Register 19
Figure 16: INTVEC Interrupt Vector Register 20
Figure 17: State diagram - Reference with reference switch 21
Figure 18: Jumper J1 (J200) configuration for trigger input 24
Figure 19: Jumper J1 (J200) configuration for trigger output 24
Figure 20: TIP102-TM-xx Jumper Layout 25

1. Product Description

The TIP102 family are IndustryPack® compatible modules for motion controller applications using incremental encoders as position feedback. There are two versions available: The TIP102-1x is the implementation of a one axis controller and the TIP102-2x is the implementation of a two axis controller on a single size IP. The TIP102 requires the use of a TIP102-TM-xx transition module. The transition module is necessary for the signal conditioning and optional galvanically isolation of the various input and output signals.

The position feedback is provided by an incremental encoder interface and a 24 bit up-/down-counter. The level of the encoder signals can be TTL or RS422. Optionally the encoder signals can be isolated on the transition module by high speed optical coupler. The encoder signals pass a digital filter for noise suppression before they are feed into the counter and the reference logic. The counter is programmable for single, double and quadruple analysis of the encoder two phase signals.

Calibration of the position feedback to an absolute reference point is done by a programmable reference logic. Several modes of operation and hardware configurations of a reference switch and the encoder zero pulse are selectable. An 'Auto-Reference' mode provides the possibility of the automatic recalibration of the measurement system during normal operation, whenever the system passes the reference location.

Two isolated 24V DC digital inputs have limit switch functionality. Each of these inputs drives a floating optical coupler output as hardware feedback. These outputs can be used to disable direction depended power on the motor power amplifier. One additional isolated 24V digital input is for free use by the software, for example as emergency stop input. A floating optical output can be controlled by software, for example as enable for the motor power amplifier.

A 16 bit digital to analog converter (DAC) produces a ± 10V controller output signal which can be used as speed or torque source for the power amplifier of the motor drive system. A galvanically isolation of this signal with the help of an isolation amplifier is available as an transition module option.

A 12 bit analog to digital converter (ADC) with an configurable input voltage range can for example be used together with a joystick for the implementation of jogging functions. Also this signal may be galvanically isolated as an option on the transition module.

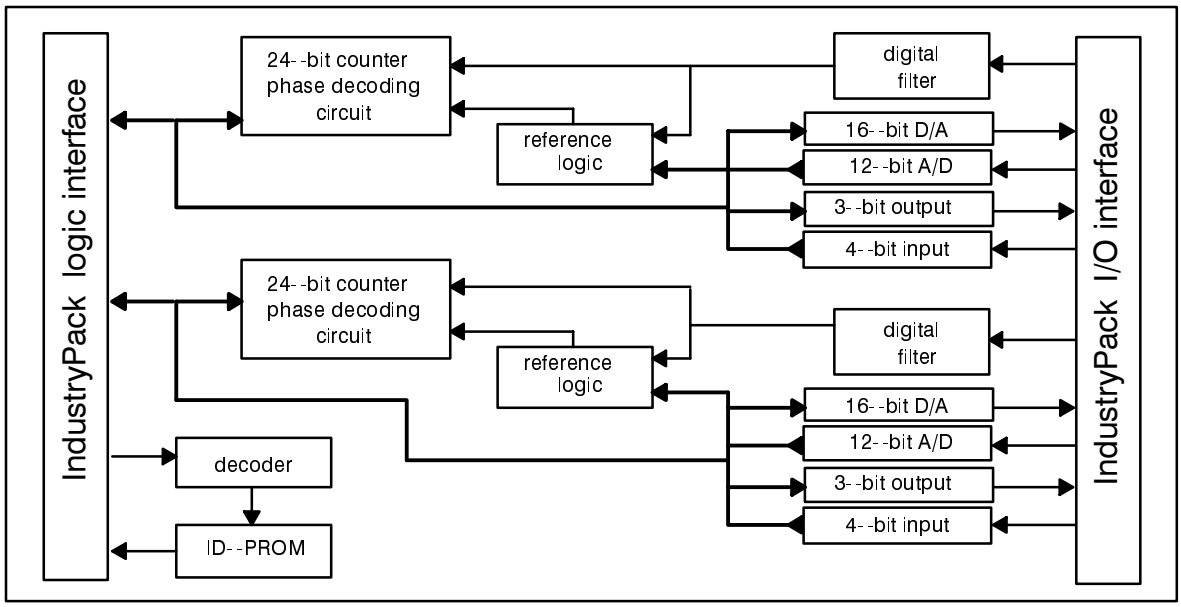


Figure 1: TIP102-2x Block Diagram

2. Technical Specification

2.1. TIP102-XX

Logic Interface	IndustryPack® Logic Interface
Size	single wide IP
I/O Interface	50-conductor flat cable
Number of Axis	1 axis for TIP102-1x 2 axis for TIP102-2x
Encoder	incremental encoder with 24 bit up-/down-counter
Input Count Frequency	up to 1.2 MHz
Analog Input	1 ADC per axis, 12 bit, 10µs, input voltage ±10V
Analog Input Over Voltage	input over voltage protection up to 25V p-p
Analog Output	1 DAC per axis, 16 bit, output voltage ±10V
Analog Output Current	±5mA
Digital Inputs	5 inputs per axis TTL level
Digital Outputs	2 outputs per axis TTL level
External Trigger	TTL Input and TTL output
Wait States	no wait states
Power Requirements	typ. mA @ 5V
Temperature Range	operating 0°C to 70°C storage -45°C to 125°C
Humidity	5 - 95% non-condensing
Transition Module	TIP102-TM-XX required, provides signal conditioning and optional isolation of digital and analog I/O signals

2.2. TIP102-TM-XX

Size	one VMEslot	
Number of Axis	1 axis for TIP102-1x 2 axis for TIP102-2x	
Encoder Interface	Signal level TTL or RS485 optional galvanically isolated	
Analog Input	1 input per axis, input voltage ±10V optional isolated (ADC on TIP102)	
Analog Input Over Voltage	Over voltage protection up to 100Vp-p with galvanically isolation up to 12Vp-p without galvanically isolation.	
Analog Output	1 output per axis, output Voltage ±10V optional isolated (DAC on TIP102)	
Analog Output Current	±20mA with galvanically isolation ±50mA without galvanically isolation	
External Trigger	isolated TTL I/O per axis (jumper selectable input or output of TIP102)	
Digital Inputs per Axis	input TIP102 (TTL)	isolated input TIP102-TM
	$\overline{\text{General Input}}$	General Purpose 24V DC
	$\overline{\text{Reference Switch}}$	REFERENCE_SWITCH24V DC
	$\overline{\text{High Limit Switch}}$	LIMIT_SWITCH_2 24V DC
	$\overline{\text{Low Limit Switch}}$	LIMIT_SWITCH_1 24V DC
	$\overline{\text{Encoder Error}}$	$\overline{\text{ENC_ERROR}}$ Input TTL
Digital Outputs per axis	output TIP102 (TTL)	isolated output TIP102-TM
	Status LED	LED in Position (no output)
	Servo Ampl. Enable	Release Output 24V DC
Digital Outputs direct driven from Inputs	isolated input TIP102-TM	isolated output TIP102-TM
	LIMIT_SWITCH_1	Current_Limit_1 Output 24V DC
	LIMIT_SWITCH_2	Current_Limit_2 Output 24V DC
Output Load	max. 1000 Ohm	
Power Requirements	typ. mA @ 5V typ. mA @ +12V	
Temperature Range	Operating 0°C to 70°C Storage -45°C to 125°C	

3. ID Prom Contents

ADDRESS	FUNCTION	TIP102-1x	TIP102-2x
$ 01	ASCII 'I'	$ 49	$ 49
$ 03	ASCII 'P'	$ 50	$ 50
$ 05	ASCII 'A'	$ 41	$ 41
$ 07	ASCII 'C'	$ 43	$ 43
$ 09	Manufacturer ID	$ B3	$ B3
$ 0B	Model Number	$ 0A	$ 0B
$ 0D	Revision	$ 10	$ 10
$ 0F	RESERVED	$ 00	$ 00
$ 11	Driver-ID low-byte	$ 00	$ 00
$ 13	Driver-ID high-byte	$ 00	$ 00
$ 15	number of bytes used	$ 0C	$ 0C
$ 17	C R C	$ 3E	$ 5F

Figure 2: ID PROM contents

4. VMEbus Addressing

The TIP102 is accessed in the I/O space through a set of registers

ADDRESS	NAME	FUNCTION AXIS 1	SIZE
$ 01	INPSR1	Input and Status Register	byte
$ 03	OUTCR1	Output Control Register	byte
$ 05	CNTDA1	Counter Data Register	byte
$ 07	CNTCS1	Counter Control and Status Register	byte
$ 08	DACDA1	DAC Data Register	word
$ 0B	ADCCS1	ADC Control and Status Register	byte
$ 0C	ADCDA1	ADC Data Register	word
$ 0F	CONCR1	Configuration Control Register	byte
$ 3F	INTVEC	Interrupt Vector Register	byte

Figure 3: TIP102-1x Register Map

On the TIP102-2x two axis motion controller the second axis can be accessed through a second set of control and status registers. Only the INTVEC Interrupt Vector Register is shared between both axis.

ADDRESS	NAME	FUNCTION AXIS 2	SIZE
$ 21	INPSR2	Input and Status Register	byte
$ 23	OUTCR2	Output Control Register	byte
$ 25	CNTDA2	Counter Data Register	byte
$ 27	CNTCS2	Counter Control and Status Register	byte
$ 28	DACDA2	DAC Data Register	word
$ 2B	ADCCS2	ADC Control and Status Register	byte
$ 2C	ADCDA2	ADC Data Register	word
$ 2F	CONCR2	Configuration Control Register	byte

Figure 4: TIP102-2x Additional Register Map

4.1. INPSR Input and Status Register

The input and status register INPSR1 (INPSR2) holds the actual status of all digital input lines and the status of the internal control logic.

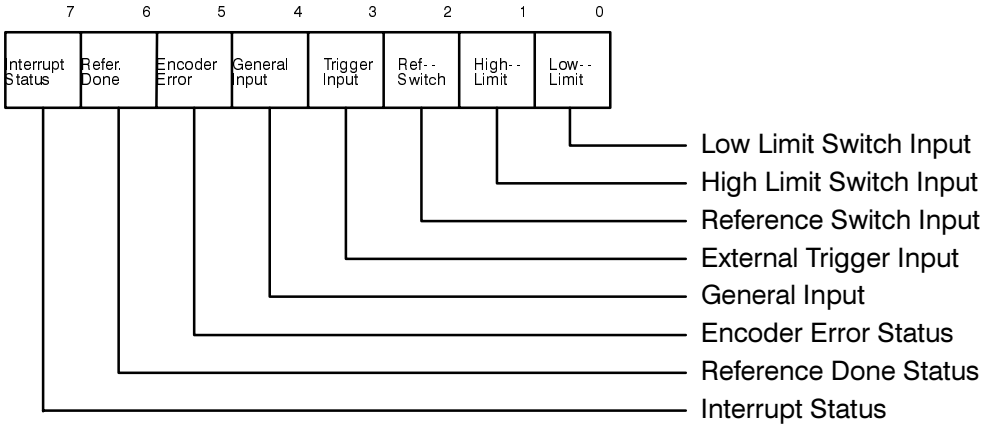


Figure 5: INPSR Input and Status Register

4.1.1. Low Limit Switch Input

Bit 0 in the INPSR1 (INPSR2) register is the actual read only status of the low limit switch input. A '1' indicates that the limit switch is activated, a '0' indicates not active.

4.1.2. High Limit Switch Input

Bit 1 in the INPSR1 (INPSR2) register is the actual read only status of the high limit switch input. A '1' indicates that the limit switch is activated, a '0' indicates not active.

4.1.3. Reference Switch Input

Bit 2 in the INPSR1 (INPSR2) register is the actual read only status of the reference switch input. A '1' indicates that the reference switch is activated, a '0' indicates not active.

4.1.4. External Trigger Input

Bit 3 in the INPSR1 (INPSR2) register is the actual read only status of the external trigger input $\overline{\text{TRIGGER INPUT}}$. A '1' indicates that the trigger input is activated, a '0' indicates not active.

4.1.5. General Input

Bit 4 in the INPSR1 (INPSR2) register is the actual read only status of the general input. A '1' indicates that the input is activated, a '0' indicates not active.

4.1.6. Encoder Error Status

Bit 5 in the INPSR1 (INPSR2) register is the latched encoder error status. A '1' indicates that an error in the timing of the encoder phase signals has occurred or the encoder itself has reported an error. The source of this flag is the error detection logic within the digital filter for the encoder phase signals or the input of the encoder signal $\overline{\text{ENC_ERROR}}$.

Because this is a latched status flag, it must be reset under software control. This is done by writing to the INPSR1 (INPSR2) register with bit 5 set to '1'.

This bit is automatically cleared with the $\overline{\text{IP_RESET}}$ signal.

4.1.7. Reference Done Status

Bit 6 in the INPSR1 (INPSR2) indicates the status of the reference logic, which is used to calibrate the counter to a reference position. A '1' indicates that the reference function, which was started with a corresponding command in the configuration control register CONCR1 (CONCR2), has completed successfully or the external trigger event has occurred. For more details see also 4.8.1., 5.1. and 5.2..

This flag will be cleared with each writing to the configuration control register CONCR1 (CONCR2).

This bit is automatically cleared with the $\overline{\text{IP_RESET}}$ signal.

4.1.8. Interrupt Status

Bit 7 in the INPSR1 (INPSR2) indicates that the corresponding axis has generated an interrupt request.

Because this is a latched status flag, it must be reset under software control. This is done by writing to the INPSR1 (INPSR2) register with bit 7 set to '1'.

This bit is also automatically cleared with the $\overline{\text{IP_RESET}}$ signal.

4.2. CNTDA Counter Data Register

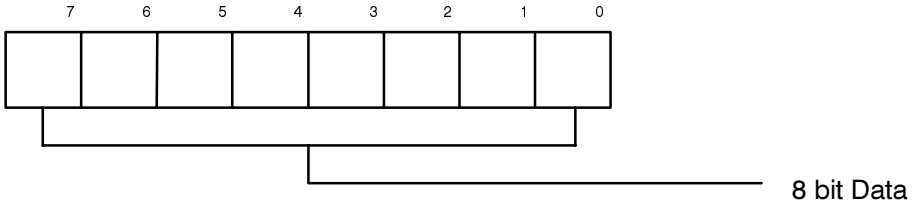


Figure 6: CNTDA Counter Data Register

The Counter Data Register CNTDA1 (CNTDA2) is the data I/O port to the LS7166 counter chip. It is used to the read counter position or to write a preset value. Because the LS7166 is a 24 bit counter, but the data register is only 8 bit wide, each data transfer needs three read or write cycles in sequence.

4.2.1. Reading Counter Data

The 24 bit data value of the counter can only be accessed through an 24 bit output latch (OL) internal the LS7166. The data is latched into the OL under software control by setting bit 1 in the counter MCR register to '1' (see 4.3.1.) or by an external hardware signal (see 5.2.). After that the data can be read through the CNTDA1 (CNTDA2) in three cycles in sequence. The transfer is least significant byte first, most significant byte last.

Note

The access to the three data byte within the output latch (OL) is controlled by an internal address pointer, which is automatically incremented with each read cycle. This pointer should be reset directly prior the three read cycles by setting bit 0 in the counter MCR register (see 4.3.1.).

4.2.2. Writing Counter Data

The 24 bit counter can be loaded from a 24 bit preset register (PR) internal the LS7166. The preset data have to be written to the PR through the CNTDA1 (CNTDA2) in three cycles in sequence. The transfer is least significant byte first, most significant byte last. The data is then transferred to the counter under software control by setting bit 3 in the counter MCR register to '1' (see 4.3.1.), by the reference logic (5.1.) or by an external hardware signal (see 5.2.).

Note

The access to the three data byte within the output latch (OL) is controlled by an internal address pointer, which is automatically incremented with each read cycle. This pointer should be reset directly prior the three read cycles by setting bit 0 in the counter MCR register (see 4.3.1.).

4.3. CNTCS Counter Control and Status Register

4.3.1. MCR Master Control Register

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '0' and bit 7 = '0' will be a write to the MCR Master Control Register of the LS7166 counter chip. Bit 0 to bit 5 have the following functionality:

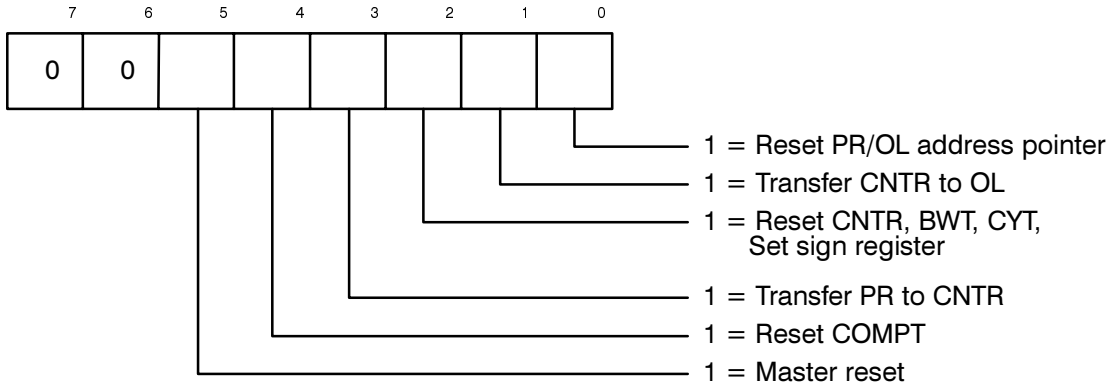


Figure 7: Counter MCR Master Control Register

4.3.1.1. Reset PR/OL address pointer

Writing bit 0 = '1' to the MCR will reset the internal PR/OL address pointer of the LS7166 counter chip, which is used during reads and writes to the CNTDA1 (CNTDA2) data register, to access the three bytes forming the 24 bit data word.

4.3.1.2. Transfer CNTR to OL

Writing bit 1 = '1' to the MCR will latch the current 24 bit value of the counter (CNTR) into the OL register of the LS7166 counter chip for subsequent readout. This bit can be combined with bit 0 to reset the OL address pointer at the same time.

4.3.1.3. Reset of CNTR, BWT, CYT, Set sign register

Writing bit 2 = '1' to the MCR will set the counter (CNTR) data value to zero, clear the borrow and carry toggle flag and set the sign bit.

4.3.1.4. Transfer PR to CNTR

Writing bit 3 = '1' to the MCR will transfer the previously loaded 24 bit data value into the counter (CNTR).

4.3.1.5. Reset COMPT

Writing bit 4 = '1' to the MCR will clear the compare toggle flag COMPT.

4.3.1.6. Master reset

Writing bit 5 = ’1’ to the MCR will perform a master reset on the LS7166 counter chip and put it into initial state.

4.3.2. ICR Input Control Register

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = ’1’ and bit 7 = ’0’ will be a write to the ICR Input Control Register of the LS7166 counter chip. Bit 0 to bit 5 have the following functionality:

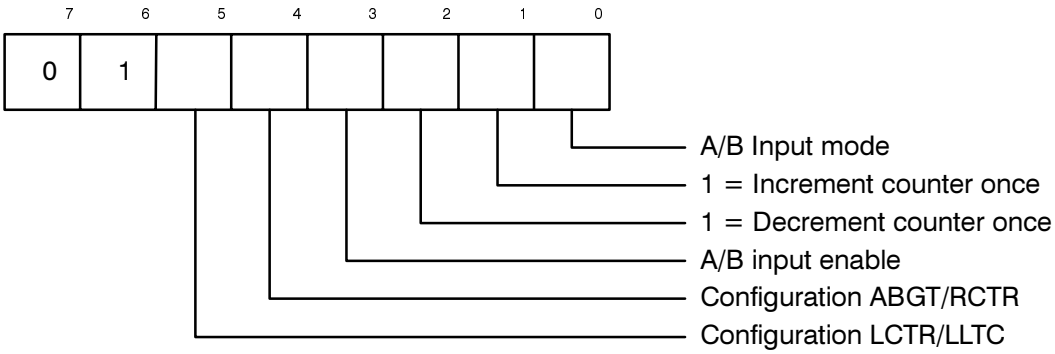


Figure 8: Counter ICR Input Control Register

4.3.2.1. A/B Input mode

Bit 0 of the ICR defines the functionality of the counter A and B clock inputs. Bit 0 = ’0’ will define A as up count input and B as down count input. Bit 0 =’1’ will define A as count input and B as count direction input with B = ’0’ for up and B = ’1’ for down.

Note

In a normal motion controller application the TIP102 will operate with an incremental encoder and the counter chip LS7166 programmed to quadrature mode by configure the QR register (see 4.3.4.). In this case the A/B input mode bit has no function.

4.3.2.2. Increment counter

Writing bit 1 = ’1’ to the ICR will increment the counter data value by one.

4.3.2.3. Decrement counter

Writing bit 2 = ’1’ to the ICR will decrement the counter data value by one.

4.3.2.4. A/B input enable

Bit 3 = ’1’ enables the A and B counter inputs. With bit 3 = ’0’ all counting function are disabled.

Note

For the normal motion controller application of the TIP102 the counter should always be enabled (bit 3 = ’1’).

4.3.2.5. Configuration ABGT/RCTR

Bit 4 of the ICR must always be set to ’0’ for the operation of the TIP102-xx IP.

4.3.2.6. Configuration LCTR/LLTC

Bit 5 of the ICR will configure the functionality of the LCTR/LLTC pin of the LS7166. On the TIP102 this pin is controlled by the reference and external trigger logic (see also 5.1. and 5.2.). With bit 5 = '0' an event (reference or external trigger) will load the counter with the contents of the PR register. With bit 5 = '1' the event will latch the actual counter data value into the OL register.

4.3.3. OCCR Output Control Register

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '0' and bit 7 = '1' will be a write to the OCCR Output Control Register of the LS7166 counter chip. Bit 0 to bit 5 have the following functionality:

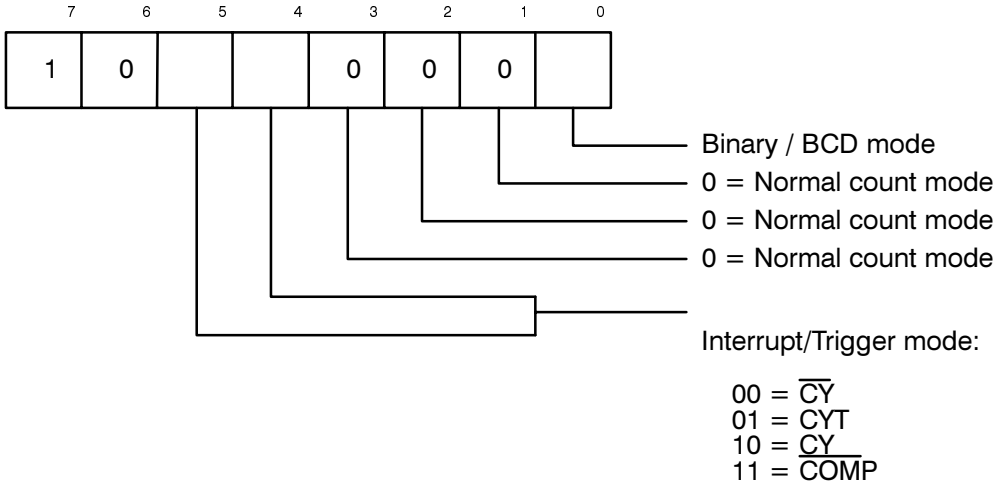


Figure 9: Counter OCCR Output Control Register

Note

For the normal motion controller application of the TIP102 the bits 1 to 3 of the OCCR must always be programmed as '0'.

4.3.3.1. Binary / BCD mode

Bit 0 of the OCCR will configure the counter to operate in binary or BCD counting mode. With bit 0 = '0' the counter is in binary mode, which should be the normal case.

4.3.3.2. Interrupt / Trigger mode

On the TIP102 the output Pin 16 of the LS7166 counter chip can be used for interrupt or output trigger impulse generation. However the internal source for this signal is selected by bit 4 and 5 of the OCCR.

00 - $\overline{CY}$

Pin 16 of the LS7166 follows the status of the inverted CY signal(carry).

01 - CYT

Pin 16 of the LS7166 follows the status of the CYT signal (carry toggle flip flop).

10 - CY

Pin 16 of the LS7166 follows the status of the CY signal (carry).

11 - $\overline{COMP}$

Pin 16 of the LS7166 follows the status of the inverted COMP signal (compare).

4.3.4. QR Quadrature Register

A write to the Counter Control and Status Register CNTCS1 (CNTCS2) with bit 6 = '1' and bit 7 = '1' will be a write to the QR Quadrature Register of the LS7166 counter chip. Bit 0 to bit 1 have the following functionality:

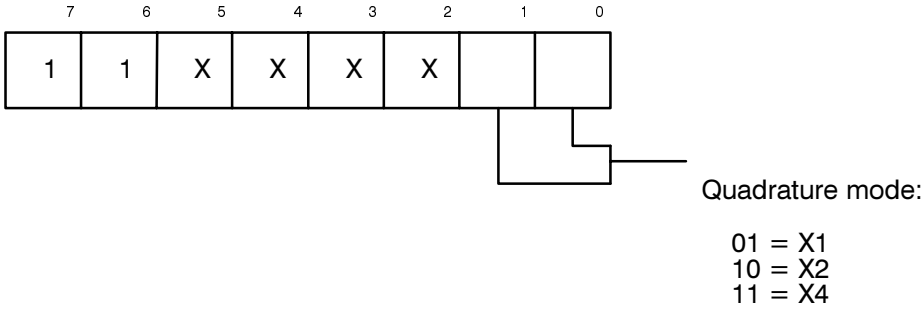


Figure 10: Counter QR Quadrature Register

4.3.4.1. Quadrature mode

Programming the bits 0 and 1 of the QR will put the LS7166 counter chip in quadrature counting mode. Depending on the mode X1, X2 or X4 the counter data values have one, two or four times the resolution of the encoder.

Note

Because the TIP102 was designed to decode quadrature signals of encoders, one of the modes X1, X2 or X4 must be selected for normal operation of the modul.

Bit 2 to bit 5 are don't cares.

4.4. DACDA DAC Data Register

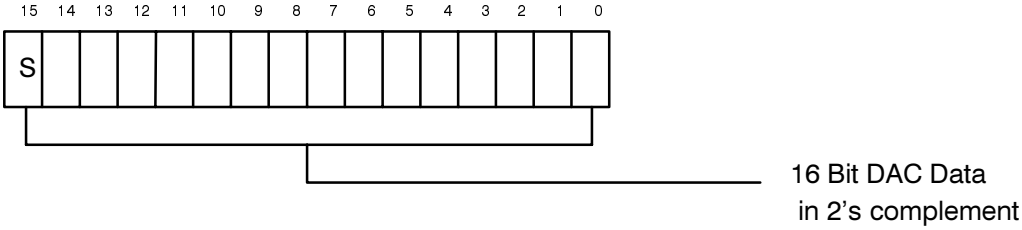


Figure 11: DACDA DAC Data Register

The DAC Data Register DACDA1 (DACDA2) is the write only data register for the ±10V controller output signal of the TIP102. The 2's complement value written into this register is converted to the corresponding output voltage with a range of ±10V.

Note

Only word access is supported for this register.

A read to this register will return a random bit pattern.

4.5. ADCCS ADC Control and Status Register

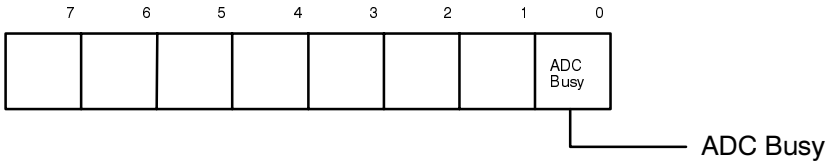


Figure 12: ADCCS ADC Control and Status Register

The ADC Control and Status Register ADCCS1 (ADCCS2) controls the function of the xxxx 12 bit ADC. A data conversion is started by a write cycle to the ADCCS1 (ADCCS2). However the data value of this write is a don't care.

As long as the ADC is busy converting the bit 0 of the ADCCS1 (ADCCS2) will read as '1'.

Note

The used bits 1 to 7 may be in an random state '0' or '1' when reading the ADC Control and Status Register ADCCS1 (ADCCS2).

4.6. ADCDA ADC Data Register

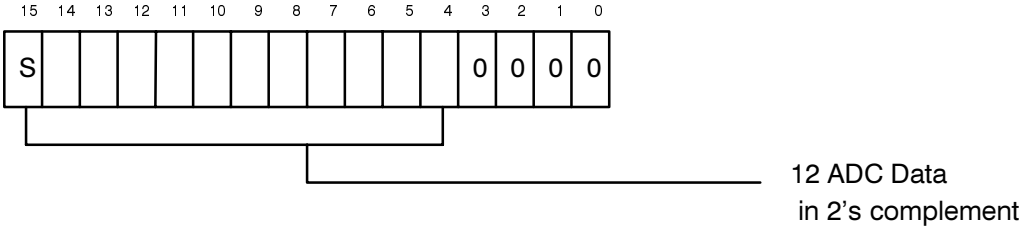


Figure 13: ADCDA ADC Data Register

The ADC Data Register ADCDA1 (ADCDA2) holds the conversion result of the 12 bit ADC xxxxx. It is left shifted by the hardware, that the software reads a 16 bit 2's complement value.

Note

Only word access is supported for this register.

4.7. OUTCR Output Control Register

The output control register OUTCR1 (OUTCR2) controls the status of some output signals.

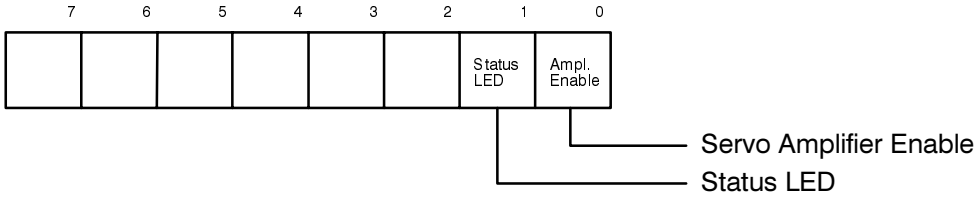


Figure 14: OUTCR Output Control Register

4.7.1. Servo Amplifier Enable

Bit 0 of the output control register OUTCR1 (OUTCR2) controls the status of a floating optical coupler output which is normally connected to the enable input of the servo amplifier of the motor drive system. It can be read and written by software.

This bit is automatically cleared with the $\overline{\text{IP_RESET}}$ signal.

4.7.2. Status LED

Bit 1 of the output control register OUTCR1 (OUTCR2) controls the status of a LED located on the transition modul. It can be read and written by software.

This bit is also automatically cleared with the $\overline{\text{IP_RESET}}$ signal.

4.8. CONCR Configuration Control Register

The configuration control register CONCR1 (CONCR2) controls the operation mode of the reference logic, the encoder configuration and interrupt generation.

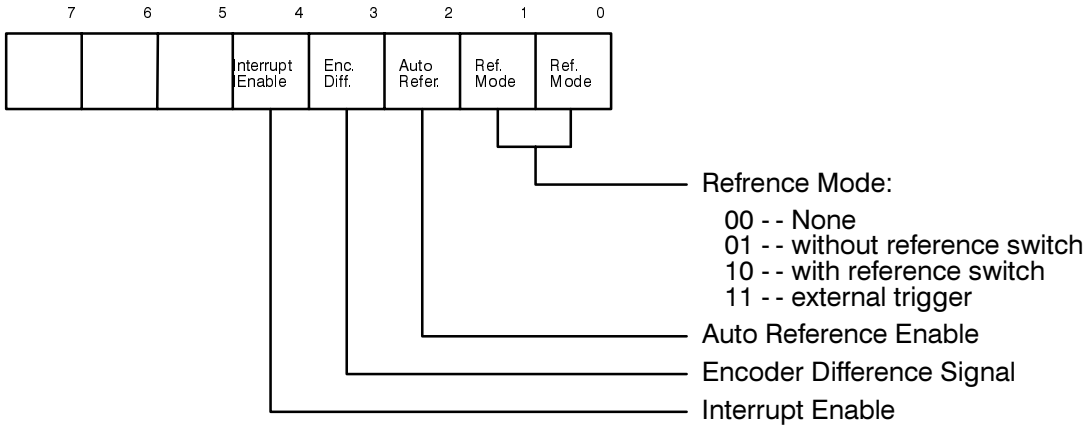


Figure 15: CONCR Configuration Control Register

Note

Writing to this register will clear the reference done flag (bit 6) in the input and status register INPSR1 (INPSR2).

The used bits 5 to 7 may be in an random state ’0’ or ’1’ when reading the Configuration Control Register CONCR1 (CONCR2).

4.8.1. Reference Mode

Bit 0 and bit 1 of the configuration control register CONCR1 (CONCR2) control the operation mode of the reference logic.

00 - None

In this mode the reference logic is disabled.

01 - Without reference switch

In this mode the zero signal of the encoder will trigger the load counter input of the LS7166 counter chip. For more details see 5.1. .

10 - With reference switch

In this mode the zero signal of the encoder is combined with the reference switch input to produce the load counter signal for the LS7166 counter chip. For more details see 5.1. .

11 - External trigger

In this mode the external trigger input signal will generate the load counter pulse to the LS7166 counter chip. For more details see 5.2. .

The reference mode bits will be cleared automatically, when the reference condition or external trigger occurs and the Auto Reference Enable bit (bit 2) is not set.

These bits are also automatically cleared with the $\overline{\text{IP_RESET}}$ signal.

4.8.2. Auto Reference Enable

Bit 2 of the Configuration and Control Register CONCR1 (CONCR2) enables the Auto Reference functionality when set to ’1’. This will automatically repeat the in bit 0 and bit 1 selected function of the reference logic and external trigger. For more details see 5.1. and 5.2..

This bit is automatically cleared with the IP_RESET signal.

4.8.3. Encoder Difference Signal

Bit 3 of the Configuration and Control Register CONCR1 (CONCR2) enables the analysis of the differential phase signals of a RS422 encoder in the digital filter. In this mode broken encoder wire will be detected and the Encoder Error Status will be set in the Input and Status Register INPSR1 (INPSR2) if such an error occurs.

Note

This function requires a transition modul with the isolated encoder input option.

This bit is automatically cleared with the IP_RESET signal.

4.8.4. Interrupt Enable

Bit 4 of the Configuration and Control Register CONCR1 (CONCR2) is the interrupt enable bit. When set, a transition on the CY output of the LS7166 counter chip will generate an interrupt. For more detail see the LS7166 data sheet which is part of the TIP102-EK engineering kit.

4.9. Interrupt Vector Register

The Interrupt Vector Register INTVEC is a byte wide read/write register. The Interrupt Vector Register is shared between both axis, but both axis will create an individual interrupt.

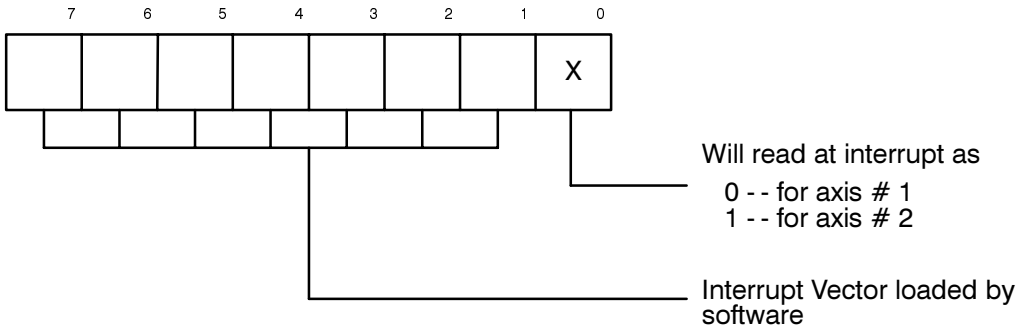


Figure 16: INTVEC Interrupt Vector Register

For an interrupt from axis # 1 bit 0 of the interrupt vector will read as '0', for an interrupt from axis #2 it will read as '1'. If the vector register is for example loaded with '$60', axis # 1 will create an interrupt at vector '$60' and axis # 2 will create an interrupt at vector '$61'.

Note

Axis #1 is using the INTREQ0 and axis #2 is using the INTREQ1 interrupt request line of the IP bus.

5. Functional Description

5.1. Reference Logic

Due to the nature of measurement systems with incremental encoders the absolute position of the axis are not now when the system is powered up. The system has to run through a reference procedure to calibrate the measurement system, in our case the counter, with the absolute positions.

The TIP102 IP has a reference logic, which allows several modes of operation for the reference procedure. The reference logic is generating a pulse to the Load Counter input of the LS7166 chip, when the reference condition occurs. This signal will either preset the counter with a value which was previously loaded into the Preset Register of the counter chip, or load the actual value of the counter to the Output Latch of the counter chip, depending on the configuration of the LCTR/LLTC bit of the ICR Input Control Register.

The desired operation mode of the reference logic is selected by programming the corresponding bits in the CONCR Configuration Control Register.

5.1.1. Reference Mode - without reference switch

In this mode the next occurrence of the zero (index) signal of the encoder is used as the source for the reference condition and therefor for the Load Counter signal. Because the incremental encoder will normally create a zero (index) pulse at each turn, this mode is only useful, if the absolute position of the next zero (index) pulse is known, or if there is only one such pulse in the operating range of the axis.

5.1.2. Reference Mode - with reference switch

This mode also make use of the zero (index) signal of the encoder to generate the reference condition. But it uses an additional Reference Switch (which is an input to the TIP102) to select a single zero (index) signal.

The reference condition in this mode is defined as the first zero (index) pulse of the encoder after a ’0’ to ’1’ transition of the reference switch, with the reference switch still in the ’1’ state.

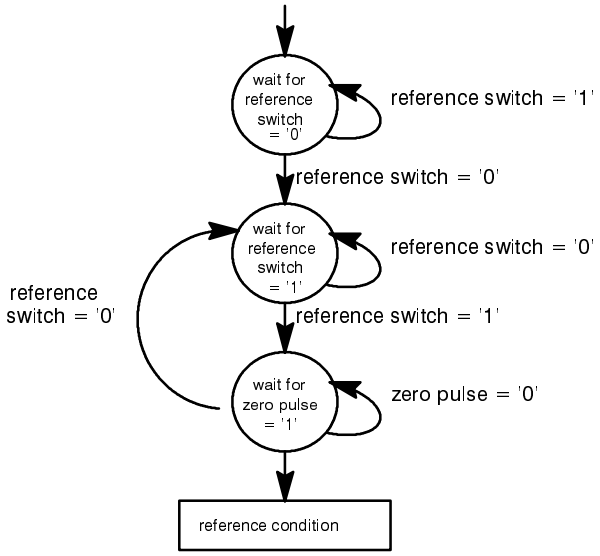


Figure 17: State diagram - Reference with reference switch

5.2. External Trigger Input

The TIP102 IP has a trigger input signal $\overline{\text{TRIGGER INPUT}}$ which can be used to latch the actual value of the counter or preload the counter at an external event. The Trigger Input is generating a pulse to the Load Counter input of the LS7166 chip, when the external trigger condition occurs. This signal will either preset the counter with a value which was previously loaded into the Preset Register of the counter chip, or load the actual value of the counter to the Output Latch of the counter chip, depending on the configuration of the LCTR/LLTC bit of the ICR Input Control Register.

The external trigger logic is activated by programming the corresponding bits in the CONCR Configuration Control Register (see also 4.8.1.).

Note

The external trigger and the reference logic can not be used at the same time.

Note

The transition module TIP102- -TM- -xx has only one set of isolated TRIGGER I/O signals, which are jumper configurable as Trigger Input or Trigger Output (see also 7.2.1.).

6. Programming Hints

6.1. LS7166 counter chip

6.1.1. Initialization

The LS7166 counter chip of the TIP102 requires some basic initialization, before it is able to decode the quadrature counting pulses of the incremental encoder. To do this the following data sequence has to be loaded into the CNTCS1 (CNTCS2) Counter Control and Status Register:

- write 0x20 to CNTCS1 (CNTCS2)
  select the counter MCR register, perform a master reset on the LS7166 counter chip
- write 0x68 to CNTCS1 (CNTCS2)
  select the counter ICR register, enable data inputs A/B, configure Pin3 as counter load input (required for the reference logic)
- write 0xB0 to CNTCS1 (CNTCS2)
  select the counter OCCR register, configure Pin 16 as compare result output (required for generation of interrupts at defined counter data values)
- write 0xC1, 0xC2 or 0xc3 to CNTCS1 (CNTCS2)
  select the counter QR register, enable quadrature decoding mode X1, X2 or X4

After this initialization the counter will begin decoding the encoders quadrature signals.

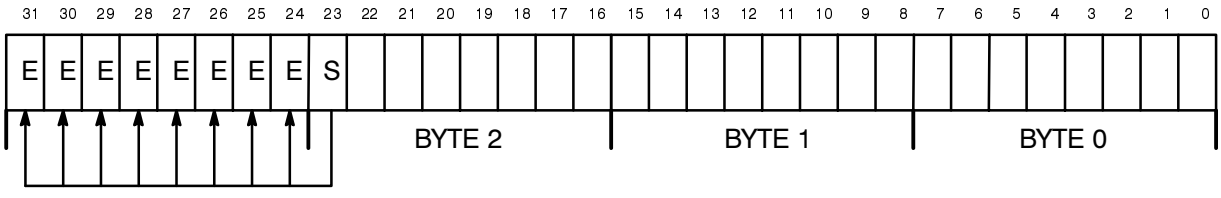
6.1.2. Reading actual counter data value

The LS7166 has a 24 bit up/down counter. However the data path to the LS7166 is only 8 bit wide. To read the 24 bit counter data value (8 bit at a time), you have to program the following sequence:

- write 0x03 to CNTCS1 (CNTCS2)
  select the counter MCR register, latch the actual counter data value into the output latch (OL), reset the OL address pointer
- read CNTDA1 (CNTDA2)
  read data byte 0 (LSB), increment OL address pointer
- read CNTDA1 (CNTDA2)
  read data byte 1, increment OL address pointer
- read CNTDA1 (CNTDA2)
  read data byte 2 (MSB), increment OL address pointer

Note

If you assemble the data bytes 0 to 2 into a 32 bit word for further processing, you have to extend the sign bit of the counter, which is bit 7 of data byte 2, into the upper 8 bits of your 32 bit word.



7. Jumper Configurations

7.1. TIP102-xx IP

Note

There are no jumpers to configure on the TIP102- -xx IP. Do never place any jumper on the 10 pin connector block at the TIP102- -xx IP. This block is used only for manufacturing and testing purpose.

7.2. TIP102-TM-xx Transition Module

7.2.1. Trigger I/O Jumper Configuration

The TRIGGER I/O signals at connector X2 (X202) of the transition module must be configured to input or output by the jumper J1 (J200) at the transition module.

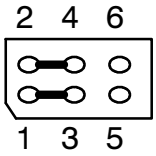


Figure 18: Jumper J1 (J200) configuration for trigger input

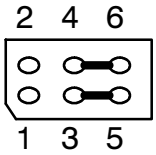


Figure 19: Jumper J1 (J200) configuration for trigger output

7.2.2. Encoder Input Jumper Configuration

The TIP102-TM-10 and TIP102-TM-20 transition modules have jumpers to enable or disable the $\overline{\text{PHASE_A}}$, $\overline{\text{PHASE_B}}$ and $\overline{\text{INDEX}}$ encoder inputs.

If the encoder provides the $\overline{\text{PHASE_A}}$, $\overline{\text{PHASE_B}}$ and $\overline{\text{INDEX}}$ signals the jumper J2, J3 and J4 (J201, J202 and J203) must be jumpered between pin 1 and 2.

If the encoder does **not** provide the $\overline{\text{PHASE_A}}$, $\overline{\text{PHASE_B}}$ and $\overline{\text{INDEX}}$ signals the jumper J2, J3 and J4 (J201, J202 and J203) must be jumpered between pin 2 and 3.

7.2.3. TIP102-TM-xx Jumper Layout

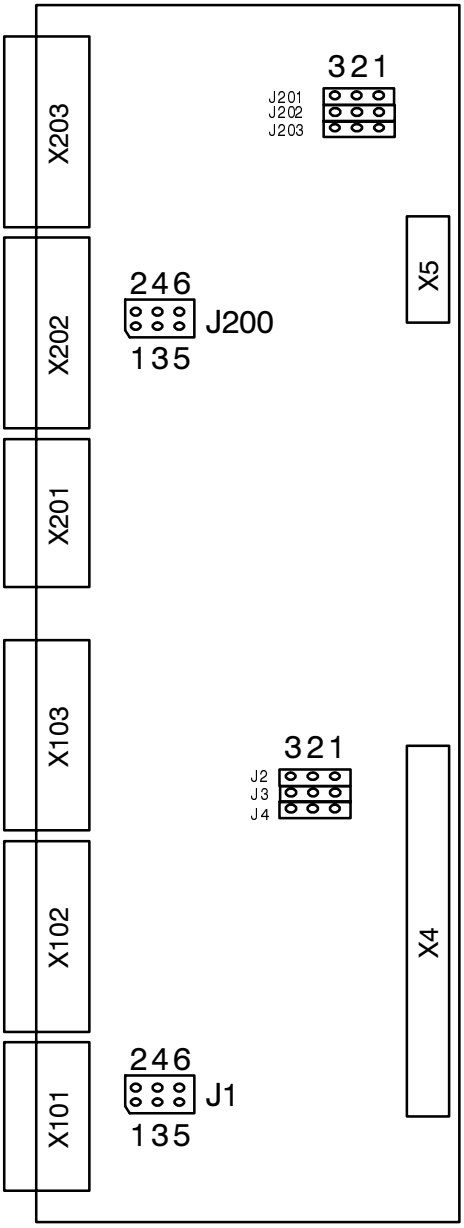


Figure 20: TIP102-TM-xx Jumper Layout

Note

The jumpers J2, J3 and J4 (J201, J202 and J203) are only present at the TIP102- -TM- -10 (TIP1020TM- -20) transition module.

8. IP I/O connector

8.1. 50 pin IP I/O connector

Pin-Number	Function
1	+5V VCC
2	+5V VCC
3	GND
4	GND
5	+12V
6	-12V
7	Status LED axis 1 (TTL output)
8	Servo Ampl. Enable axis 1 (TTL output)
9	GND
10	DAC Output axis 1 (±10V)
11	DAC GND axis 1
12	ADC Input axis 1 (±10V)
13	ADC GND
14	GND
15	Trigger Input axis 1 (TTL input)
16	Trigger Output axis 1 (TTL output)
17	General Input axis 1 (TTL input)
18	Reference Switch axis 1 (TTL input)
19	High Limit Switch axis 1 (TTL input)
20	Low Limit Switch axis 1 (TTL input)
21	Encoder Error axis 1 (TTL input)
22	NC
23	ENC INDEX axis 1 (TTL input)
24	ENC INDEX axis 1 (TTL input)
25	ENC PHASE B axis 1 (TTL input)
26	ENC PHASE B axis 1 (TTL input)
27	ENC PHASE A axis 1 (TTL input)
28	ENC PHASE A axis 1 (TTL input)
29	Status LED axis 2 (TTL ouput)
30	Servo Ampl. Enable axis 2 (TTL output)
31	GND
32	DAC Output axis 2 (±10V)
33	DAC GND axis 2
34	ADC Input axis 2 (±10V)
35	ADC GND
36	GND
37	Trigger Input axis 2 (TTL input)
38	Trigger Output axis 2 (TTL output)

Pin-Number	Function
39	General Input axis 2 (TTL input)
40	Reference Switch axis 2 (TTL input)
41	High Limit Switch axis 2 (TTL input)
42	Low Limit Switch axis 2 (TTL input)
43	Encoder Error axis 2 (TTL input)
44	NC
45	ENC INDEX axis 2 (TTL input)
46	ENC INDEX axis 2 (TTL input)
47	ENC PHASE B axis 2 (TTL input)
48	ENC PHASE B axis 2 (TTL input)
49	ENC PHASE A axis 2 (TTL input)
50	ENC PHASE A axis 2 (TTL input)

9. Transition Module

9.1. I/O Connection TIP102-TM

9.1.1. X1/X201 DB9 female Servo Amplifier Signals

Pin-Number	Function	Signal Level
1	Current_Limit_1 +	
2	Current_Limit_2 +	
3	Enable +	
4	Shield	
5	DAC_GND	
6	Current_Limit_1 -	
7	Current_Limit_2 -	
8	Enable -	
9	DAC Output	±10V

9.1.2. X2/X202 DB15 male Power and I/O Signals

Pin-Number	Function	Signal Level
1	ENC_VCC	
2	ENC_VCC Sense	
3	Shield	
4	LIMIT_SWITCH_2 Input	24V
5	General Purpose Input	24V
6	Trigger I/O +	
7	Shield	
8	ADC_GND	
9	ENC_GND	
10	ENC_GND Sense	
11	LIMIT_SWITCH_1 Input	24V
12	REFERENCE_SWITCH Input	24V
13	COMMON RETURN of Input Signals	24V common
14	Trigger I/O -	
15	ADC Input	±10V

9.1.3. X3/X203 DB15 female Encoder Signals

Pin-Number	Function	Signal Level
1	ENC_VCC	
2	ENC_GND	
3	ENC_VCC Sense	
4	NC	
5	INDEX	TTL or RS422 -
6	PHASE_B	TTL or RS422 -
7	PHASE_A	TTL or RS422 -
8	SHIELD	
9	ENC_VCC	
10	ENC_GND	
11	ENC_GND Sense	
12	ENC_ERROR	TTL
13	INDEX	TTL or RS422 +
14	PHASE_B	TTL or RS422 +
15	PHASE_A	TTL or RS422 +

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP