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TIP255

2 Mbytes SRAM Memory

with Battery Backup

Version 1.1 Revision A

User Manual

Issue 1.1.0

February 2018

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TIP255-10R

2 Mbytes SRAM memory with battery backup

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	February 2002
1.1	New Module Revision B	March 2002
1.2	New Module Revision C	October 2003
1.3	Added Security Warning (Lithium Battery)	August 2004
1.4	New Module Version TIP255-10-ET	April 2005
1.5	New address TEWS LLC	September 2006
1.0.6	New User Manual Issue Notation	September 2009
1.1.0	Typical data retention current changed. Chapter “Data Retention Time” added	February 2018

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1 Product Description

The TIP255 is an IndustryPack® compatible module that offers an easy and reliable way to implement 2 Mbytes of SRAM memory with battery backup.

The 2 Mbyte SRAM is organized in two banks, each bank is providing 512k x 16 bit memory. For all SRAM devices battery backup is provided by an on board lithium cell. During normal operation (standard 5V supply applied to the SRAM's) the capacity of the lithium cell is monitored every 24 hours by the battery monitor device. In addition an interrupt is generated if the battery voltage is too low. The battery monitor device switches the power supply of the SRAM's from the standard 5V to the battery if the 5V drop below the threshold level of the battery monitor device. At this point any active access to the SRAM's is executed correctly within 1.5 µs. After this time further accesses to the SRAM's are not possible.

Accesses to the TIP255 SRAM memory occur within the IP memory space. The IP I/O space holds the Interrupt Control Register, the Interrupt and Battery Status Register and the Interrupt Vector Register.

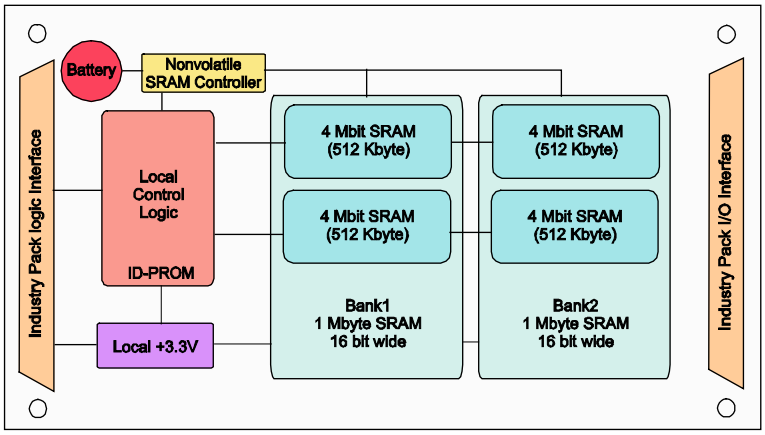


Figure 1-1 : Block Diagram

CAUTION! - This system contains a lithium battery. Lithium batteries may explode if mishandled.

Please refer to chapter "Security Warning (Lithium Battery)".

2 Technical Specification

IP Interface	Single Size IndustryPack® Logic Interface	
	ID PROM supports auto-configuration	
Module Specific Data		
Memory Size	2 Mbytes SRAM Memory	
Memory Organization	2 banks of 1 Mbyte	
Data Width	16 bit	
Wait States	No wait states	
Interrupts	IntReq0 on battery low	
SRAM		
CMOS SRAM Chip	4 x 512x8 low power SRAM	
Battery		
On Board Battery Type	CR2430 Lithium Cell (285mAh capacity)	
Battery Fault Voltage	2.6V typical	
Battery Lifetime (caused by self discharching effects)	@+25°C : approx. 8 years @+45°C : approx. 4 years	
Battery Current in Memory Backup Mode	10µA typical @ +25°C	
Min. Data Retention Voltage	2.0V	
5V Power Failure Threshold	4.37V typical	
I/O Interface	No connections to IP I/O connector	
Physical Data		
Power Requirements	65mA typical @ + 5V DC	
Temperature Range	Operating Storage	0 °C to +70 °C -55 °C to +125 °C
MTBF	550000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	

Table 2-1 : Technical Specification

3 ID PROM Contents

ADDRESS	FUNCTION	CONTENTS
0x01	ASCII ‘I’	49
0x03	ASCII ‘P’	50
0x05	ASCII ‘A’	41
0x07	ASCII ‘C’	43
0x09	Manufacturer ID	B3
0x0B	Model Number	31
0x0D	Revision	10
0x0F	RESERVED	00
0x11	Driver-ID Low – Byte	00
0x13	Driver-ID High – Byte	00
0x15	Number of bytes used	0C
0x17	Check Sum	9C

Table 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP255-10R is accessible in the I/O space of the IP.

Address	Symbol	Description	Size (Bit)	Access
0x01	CR	Interrupt Control Register	8	R/W
0x03	SR	Interrupt and Battery Status Register	8	R/W
0x05	INTVEC	Interrupt Vector Register	8	R/W

Table 4-1 : Register Set

4.1.1 SRAM Control Register (CR)

The CR is a read/write register to enable interrupt generation of the TIP255.

Bit	Symbol	Description	Access
7:1		N/A	
0	INT ENA	Interrupt Enable 1 = an interrupt is always initiated, whenever the battery voltage falls below the reference voltage of the nonvolatile SRAM controller (V_{ref}=2.6V typical).	R/W

Table 4-2 : SRAM Control Register (CR)

4.1.2 SRAM Status Register (SR)

The SR is a read/write register to observe battery and interrupt status of the TIP255.

Bit	Symbol	Description	Access
7:2		N/A	
1	IS	Interrupt Status 1 = if an interrupt is pending. This bit is reset to '0' by a write access to this register with any data.	R/W
0	BS	Battery Status 1 = the battery voltage has fallen below the reference voltage of V_{ref}=2.6V typical. In this case the battery will soon reach end-of-live. For reliable function of the battery backup, the battery should be replaced.	R/W

Table 4-3 : SRAM Status Register (SR)

4.1.3 Interrupt Vector Register (INTVEC)

The INTVEC is a read/write register. It must be loaded by software with the desired interrupt vector value, when interrupts shall be used.

A reset will set the INTVEC to the default value of 0x00.

4.2 Memory Addressing

Access to the TIP255 SRAM is simply done by reading or writing data to the address space where the TIP255 memory is mapped in the processors memory space. 8 bit and 16 bit accesses are supported.

5 Data Retention Time

The contents of the TIP255 SRAM will only be retained during system power-down while the battery is able to supply sufficient current to maintain the SRAM cell array.

TEWS uses a CR2430 lithium button cell battery with a capacity of 285mAh. It produces a nominal 2.9 V output with a flat discharge curve until the end of its effective live, and thus is suitable for providing battery backup to low-power SRAMs.

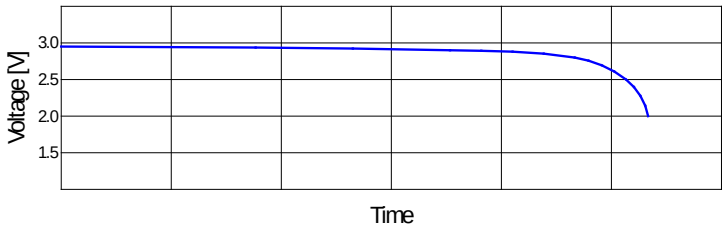


Figure 5-1 : Typical Lithium Battery Discharge Curve

The Battery will reach the end of its useful life, limiting the Data Retention Time, for one of two reasons:

- The effects of aging will have rendered the cell inoperative before the stored charge has been fully consumed by the SRAM. This is called Battery Lifetime.
- It becomes discharged by providing current to the SRAM in the battery backup mode. The time the battery can supply the SRAM is called Data Retention Time. It depends on Battery Capacity and SRAM Standby Current.

Whenever the TIP255 is powered up, the SRAMs are supplied by system-power and no current is drawn from the battery. Only when the TIP255 is powered down, the SRAM supply is switched from system-power to the on board battery.

During Battery Backup, the SRAMs consume current from the Battery. With a typical backup current of 10µA and a fresh 285mAh battery, the resulting Data Retention Time would be:

$$T_{DataRetention} = 285mAh / 10\mu A = 28500 \text{ hours (app. 3.3 years)}$$

The currently remaining Data Retention Time of a TIP255 is a function of battery age, already consumed Data Retention Time and SRAM backup current. As temperature has a non-linear influence on SRAM backup current and battery self-discharge rate, the remaining Data Retention Time is not calculable.

During normal operation, the TIP255 monitors the lithium cell capacity every 24 hours. If enabled, an interrupt is generated if the battery voltage is too low. Battery status can also be monitored by polling the SRAM Status Register (SR).

A battery low status is signaled when the battery voltage is below app. 2.6V. Since the SRAM data is preserved for battery voltages down to 2.0V, there is still some Battery Backup lifetime left and it is not necessary to exchange the battery immediately. But it should be replaced in the near future.

6 Module Installation

6.1 Security Warning (Lithium Battery)

CAUTION! - This system contains a lithium battery. Lithium batteries may explode if mishandled.

Please observe the following warnings strictly. If misused, the battery may explode or leak, causing injury or damage to the equipment.

- Keep batteries out of the reach of children. In case of ingestion of a cell or battery, the person involved should seek medical assistance promptly.
- The batteries must be inserted into the equipment with the correct polarity (+ and -).
- Do not use metallic or other conductive extraction tools to replace the batteries.
- Do not attempt to revive used batteries by heating, charging or other means.
- Do not dispose of batteries in fire. Do not dismantle batteries.
- Do not short circuit batteries.
- Do not expose batteries to high temperatures, moisture or direct sunlight.
- Do not place batteries on a conductive surface (anti-static work mat, packaging bag or form trays) as it can cause the battery to short.

CAUTION ! Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

6.2 Jumper Configuration

For the use of the battery backup support the enclosed battery must be unpacked and clipped into the battery holder. With the default jumper configuration the battery backup support of the TIP255 is now active.

If the battery support of the TIP255 is not used, jumper J1 must be switched to position 1-2.

6.2.1 Jumper Settings

J1: 1-2 Battery backup support disabled

2-3 Battery backup support enabled

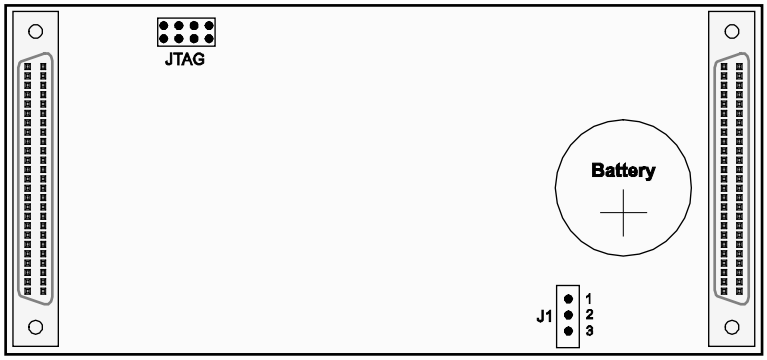


Figure 6-1 : Jumper Configuration

By factory configuration the battery backup support is enabled (J1: 2-3).

7 Pin Assignment

The table shows the complete IP J1 logic interface pin assignment. Some of these signals are not used by the TIP255-10R.

Pin	Signal
1	GND
2	CLK
3	Reset#
4	D0
5	D1
6	D2
7	D3
8	D4
9	D5
10	D6
11	D7
12	D8
13	D9
14	D10
15	D11
16	D12
17	D13
18	D14
19	D15
20	BS0#
21	BS1#
22	-12V
23	+12V
24	+5V
25	GND

Pin	Signal
26	GND
27	+5V
28	R/W#
29	IDSel#
30	DMAReq0#
31	MemSel#
32	DMAReq1#
33	IntSel#
34	DMAAck#
35	IOSel#
36	Reserved
37	A1
38	DMAEnd#
39	A2
40	Error#
41	A3
42	IntReq0#
43	A4
44	IntReq1#
45	A5
46	Strobe#
47	A6
48	ACK#
49	Reserved
50	GND

Table 7-1 : Pin Assignment J1

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