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TEWS TECHNOLOGIES

TIP605

16 Digital Inputs

Optically Isolated

Version 1.1

User Manual

Issue 1.1.4

September 2009

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TIP605

16 digital inputs optically isolated

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	May 1997
1.1	General Revision	April 2003
1.2	New address TEWS LLC	September 2006
1.3	Power consumption added to technical specification	June 2008
1.1.4	New hardware version of TIP605 and new notation of User Manual Issue	September 2009

Table of Contents

1 PRODUCT DESCRIPTION 6
2 TECHNICAL SPECIFICATION 7
3 ID PROM CONTENTS 8
4 IP ADDRESSING 9
4.1 I/O Addressing 9
4.2 Input Data Register 9
4.3 Global Interrupt Control Register 9
4.4 Interrupt Enable Register Rising Edge 10
4.5 Interrupt Enable Register Falling Edge 10
4.6 Interrupt Status Register Rising Edge 10
4.7 Interrupt Status Register Falling Edge 11
4.8 Interrupt Vector Register 11
4.9 Debounce Timer Register 11
5 INSTALLATION 12
5.1 Input Wiring 12
6 PIN ASSIGNMENT – I/O CONNECTOR 13
6.1 50 pin I/O flat cable 13
6.2 IP Connector Orientation 14

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM 6
FIGURE 5-1 : INPUT WIRING OPTIONS 12
FIGURE 6-1 : IP CONNECTOR ORIENTATION 14

List of Tables

TABLE 2-1 : TECHNICAL SPECIFICATION 7
TABLE 3-1 : ID PROM CONTENTS 8
TABLE 4-1 : REGISTER SET 9
TABLE 4-2 : INPUT DATA REGISTER 9
TABLE 4-3 : GLOBAL INTERRUPT CONTROL REGISTER 9
TABLE 4-4 : INTERRUPT ENABLE REGISTER RISING EDGE 10
TABLE 4-5 : INTERRUPT ENABLE REGISTER FALLING EDGE 10
TABLE 4-6 : INTERRUPT STATUS REGISTER RISING EDGE 10
TABLE 4-7 : INTERRUPT STATUS REGISTER FALLING EDGE 11
TABLE 4-8 : INTERRUPT VECTOR REGISTER 11
TABLE 4-9 : DEBOUNCE TIMER REGISTER 11
TABLE 6-1 : PIN ASSIGNMENT I/O CONNECTOR 13

1 Product Description

The TIP605 is an IndustryPack® compatible module with 16 digital inputs galvanically isolated by optocoupler. The individual inputs are potential free in relation to each other. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole.

All inputs have an electronic debounce circuit with a freely programmable debounce time. All inputs can generate an interrupt. The signal edge handling is programmable. For the TIP605 the operating temperature range is –40°C to +85°C.

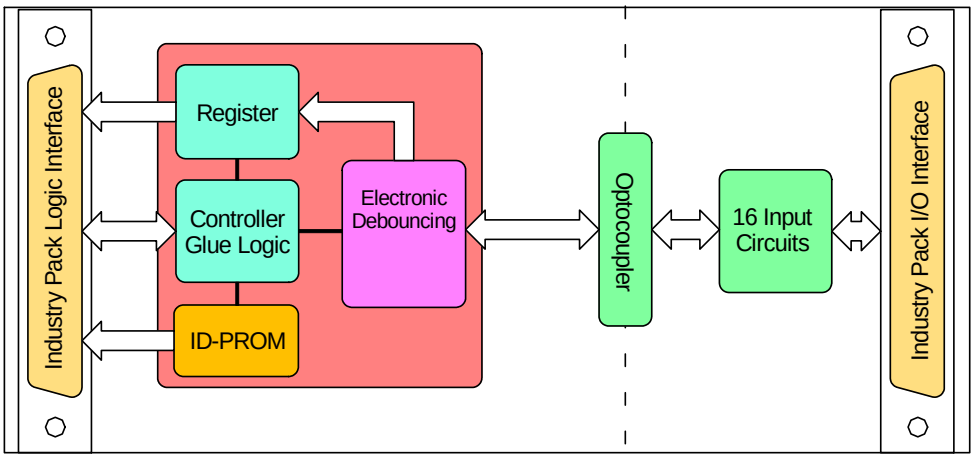


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used without wait states	
Memory Space	not used	
Interrupts	INTREQ0# is used for Input Interrupts INTREQ1# is not used by the TIP605	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
I/O Interface		
Inputs	16, each input can generate an interrupt at programmable signal transition	
Input Isolation	All channels completely independent from each other	
Input Voltage	24V DC	
Input Current	4.2mA typical @+24V input voltage	
Input Switching Level	12V typical (minimum 7.5, maximum 14V)	
Input Signal Debouncing	Electronic debouncing with programmable debounce time (8µs to 261ms in 1.024ms steps common for all inputs)	
Interface Connector	50-conductor flat cable	
Power Requirements	30mA typical @ +5V DC with 24V Input voltage +12V DC – not used -12V DC – not used	
Physical Data		
Temperature Range	Operating Storage	-40 °C to +85 °C -40°C to +125°C
MTBF	703000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	27 g	

Table 2-1 : Technical Specification

3 ID PROM Contents

Address	Function	Contents
0x01	ASCII ‘I’	**0x49**
0x03	ASCII ‘P’	**0x50**
0x05	ASCII ‘A’	**0x41**
0x07	ASCII ‘C’	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x1A**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0D**
0x17	CRC	**0x1F**
0x19	Version	**0x0A**

Table 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP605 is accessible in the I/O space of the IP.

Address rage: ip_io_base_address + (0x00 to 0x0F)

Address	Symbol	Description	Size (Bit)	Access
0x00	DATAREG	Input Data Register	word	R
0x03	INTCONT	Global Interrupt Control Register	byte	R/W
0x04	INTENALH	Interrupt Enable Rising Edge	word	R/W
0x06	INTENAHL	Interrupt Enable Falling Edge	word	R/W
0x08	INSTATLH	Interrupt Status Rising Edge	word	R/W
0x0A	INTSTATHL	Interrupt Status Falling Edge	word	R/W
0x0D	INTVEC	Interrupt Vector Register	byte	R/W
0x0F	DEBTIME	Debounce Time Register	byte	R/W

Table 4-1 : Register Set

All registers are set to '0' after reset.

4.2 Input Data Register

The Input Data Register is a read only register that reflects the actual states of inputs.

Bit	Symbol	Description	Access	Reset Value
15:0		16 bit input data	R	

Table 4-2 : Input Data Register

4.3 Global Interrupt Control Register

Bit	Symbol	Description	Access	Reset Value
7	Int Req	Global Interrupt Request flag Read as '1' = an interrupt request of at least one of the 16 input channels is pending.	R	
6:1		Not used and undefined during reads		
0	Int Enable	Global Interrupt Enable Bit 1 = globally enables interrupts for all 16 inputs on interrupt request line INTREQ0# of the IP bus	R/W	

Table 4-3 : Global Interrupt Control Register

4.4 Interrupt Enable Register Rising Edge

Bit	Symbol	Description	Access	Reset Value
15:0		Bit 0 enables the interrupt of input channel 1 for the rising edge, bit 15 enables interrupt of input channel 16. All other bits are equivalent. 1 = enabled 0 = disabled	R/W	

Table 4-4 : Interrupt Enable Register Rising Edge

An interrupt request on interrupt request line INTREQ0# of the IP bus is only generated if the global interrupt enable bit of the Global Interrupt Control Register is set to '1'.

4.5 Interrupt Enable Register Falling Edge

Bit	Symbol	Description	Access	Reset Value
15:0		Bit 0 enables the interrupt of input channel 1 for the falling edge, bit 15 enables interrupt of input channel 16. All other bits are equivalent. 1 = enabled 0 = disabled	R/W	

Table 4-5 : Interrupt Enable Register Falling Edge

An interrupt request on interrupt request line INTREQ0# of the IP bus is only generated if the global interrupt enable bit of the Global Interrupt Control Register is set to '1'.

4.6 Interrupt Status Register Rising Edge

Bit	Symbol	Description	Access	Reset Value
15:0		Bit 0 reflects the interrupt request state of input 1 for the rising edge, bit 15 reflects interrupt request of input 16. All other bits are equivalent. Read: 1 = interrupt request pending 0 = no interrupt request pending Write: 1 = clear pending interrupt request for a specific input	R/W	

Table 4-6 : Interrupt Status Register Rising Edge

4.7 Interrupt Status Register Falling Edge

Bit	Symbol	Description	Access	Reset Value
15:0		Bit 0 reflects the interrupt request state of input 1 for the falling edge, bit 15 reflects interrupt request of input 16. All other bits are equivalent. Read: 1 = interrupt request pending 0 = no interrupt request pending Write: 1 = clear pending interrupt request for a specific input	R/W	

Table 4-7 : Interrupt Status Register Falling Edge

4.8 Interrupt Vector Register

Bit	Symbol	Description	Access	Reset Value
7:0		8 bit interrupt vector is loaded by software	R/W	

Table 4-8 : Interrupt Vector Register

4.9 Debounce Timer Register

Bit	Symbol	Description	Access	Reset Value
7:0		Value 0 sets the debounce time to a minimum of 8µs (default after reset). The debounce time can be programmed in steps of 1.024ms in the range of 8µs to 261ms. The debounce time is common for all inputs. $preload\ \ value = \frac{debounce\ \ time\ (ms)}{1.024\ (ms)}$	R/W	

Table 4-9 : Debounce Timer Register

5 Installation

5.1 Input Wiring

Each input is optically isolated from the logic circuit. Each input is independent of the other inputs and can be wired different. Each input has two connections at the IP I/O connector, input x+ and input x-. All inputs are isolated by optocoupler and against each other. The input channels can be activated only in one polarity and have an external diode to prevent damage of the optocoupler by wiring the input in a wrong direction.

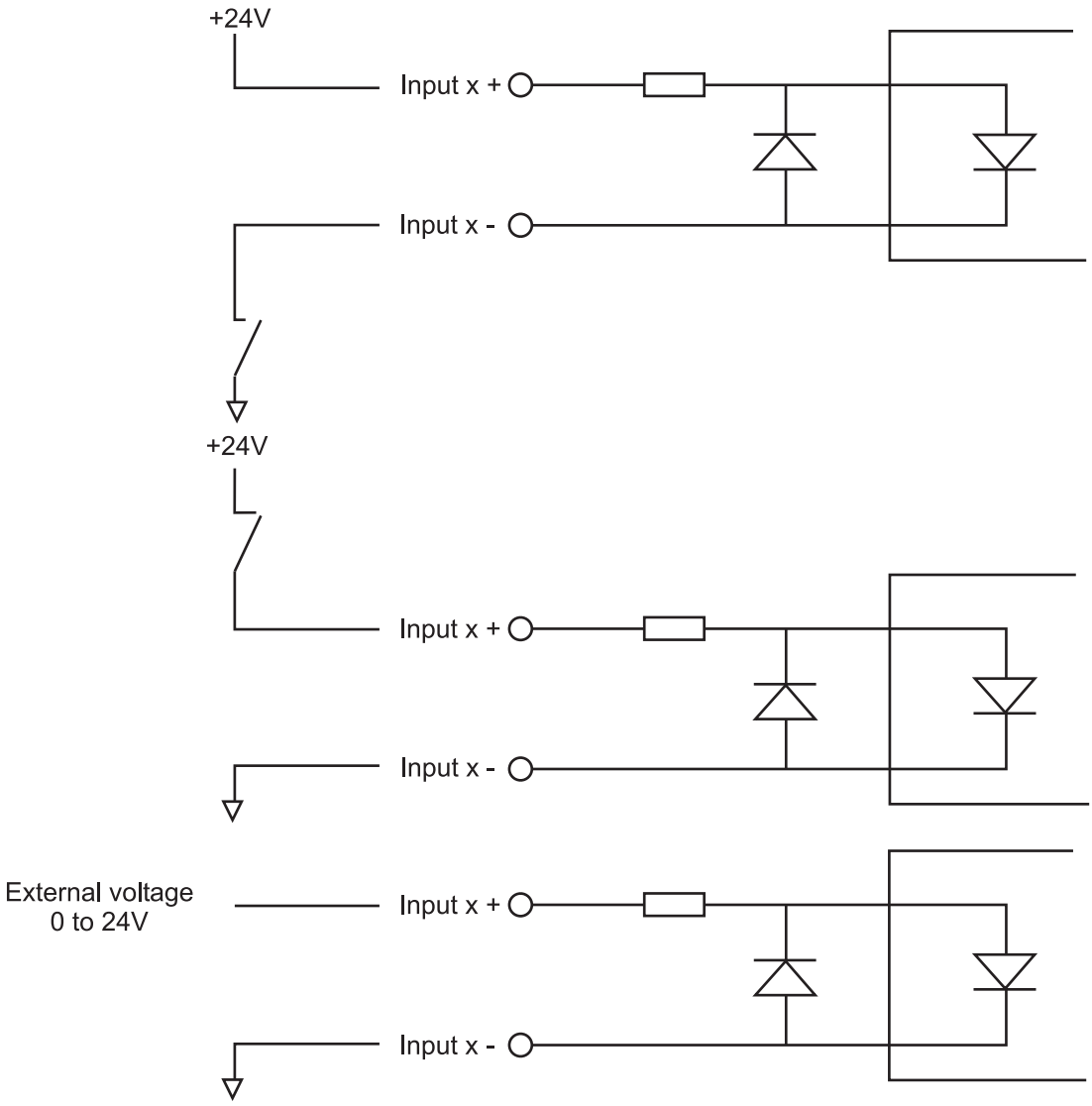


Figure 5-1 : Input Wiring Options

6 Pin Assignment – I/O Connector

6.1 50 pin I/O flat cable

Pin	Signal	Pin	Signal
1	Input 1 +	26	Input 13 -
2	Input 1 -	27	Input 14 +
3	Input 2 +	28	Input 14 -
4	Input 2 -	29	Input 15 +
5	Input 3 +	30	Input 15 -
6	Input 3 -	31	Input 16 +
7	Input 4 +	32	Input 16 -
8	Input 4 -	33	-
9	Input 5 +	34	-
10	Input 5 -	35	-
11	Input 6 +	36	-
12	Input 6 -	37	-
13	Input 7 +	38	-
14	Input 7 -	39	-
15	Input 8 +	40	-
16	Input 8 -	41	-
17	Input 9 +	42	-
18	Input 9 -	43	-
19	Input 10 +	44	-
20	Input 10 -	45	-
21	Input 11 +	46	-
22	Input 11 -	47	-
23	Input 12 +	48	-
24	Input 12 -	49	-
25	Input 13 +	50	-

Table 6-1 : Pin Assignment I/O Connector

6.2 IP Connector Orientation

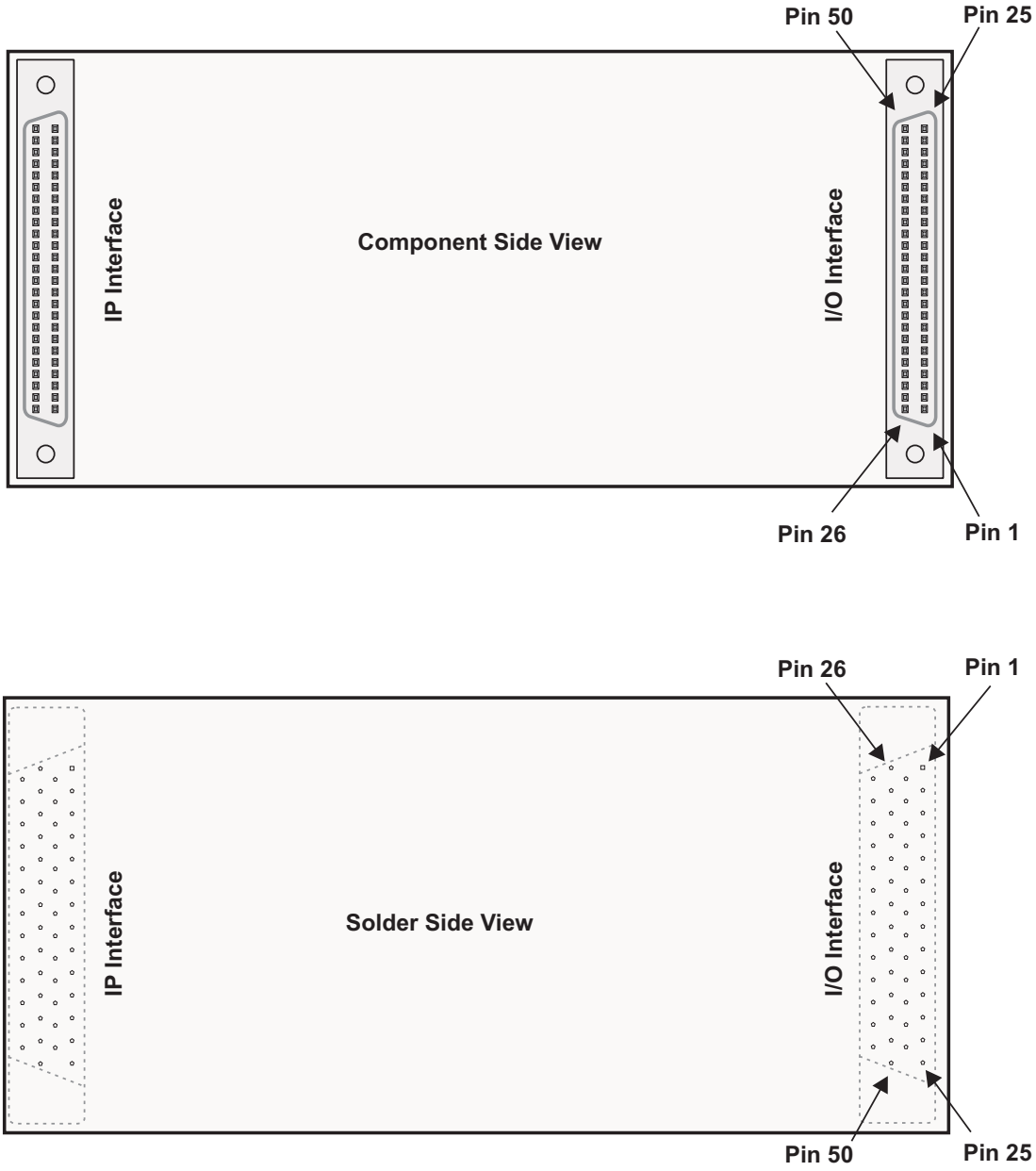


Figure 6-1 : IP Connector Orientation

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