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TEWS TECHNOLOGIES

TIP606

Digital Input Module for Avionic Applications

Version 1.1

User Manual

Issue 1.1.1

January 2016

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TIP606-10R

Digital Input Module for Avionic Applications

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	March 2000
1.1	General Revision	October 2003
1.2	Correction of figure “Input Circuit” in chapter “Functional Description”	January 2006
1.3	New address TEWS LLC	September 2006
1.1.0	New hardware version of TIP606 and new notation of User Manual Issue	September 2009
1.1.1	Correction of the drawing High Side and Low Side Switching	January 2016

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1 Product Description

The TIP606 is an IndustryPack® compatible module designed for avionic test environments. It provides 16 optically isolated differential inputs for high unipolar input voltage which may exceed the supply voltage of the module. The inputs can withstand input voltage up to 44V maximum between the two differential input pins.

Due to the differential inputs of the TIP606, it is even possible to use the module in noisy environments. The TIP606 provides a high differential input resistance of 112 kohms typically.

The interface circuit will detect a logic 1, if the differential voltage is typically greater than +14.0V and it will detect a logic 0, if the input voltage is typically lower than +3.5V. The inputs are isolated from the IP interface via optocouplers. Each input is capable of generating interrupts on rising or falling edges of the input signal. It is also possible to disable the generation of interrupts and poll the input register for new data.

All inputs have an electronic debounce circuit. The debounce time is programmable in a range from 900µs up to 230ms in 256 steps of 900µs. The debounce circuit can also be disabled.

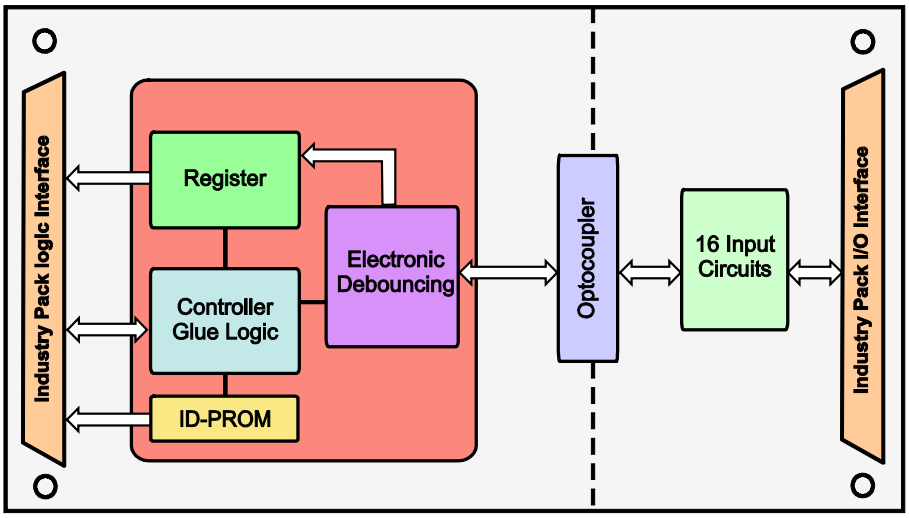


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used without wait states	
Memory Space	not used	
Interrupts	INTREQ0# used INTREQ1# not used	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
I/O Interface		
Number of Inputs	16 differential	
Maximum Input Voltage	44V between U_in+ and U_in-	
Input Isolation Voltage	500Vpp	
Input Switching Level	High level: >14.0V typical @+25°C (13.0V-16.0V) Low level: <3.5V typical @ +25°C (3.1V-4.6V)	
Input Impedance	112 kohms typical	
Debounce Timer	Time minimum: 900µs +/-15% Time maximum: 230.4ms +/-15% Step size: 900µs	
Interface Connector	50-conductor flat cable	
Power Requirements	260 mA typical @ +5V DC	
Interrupts	Interrupt generation for each input programmable on Low -> high transition, High -> low transition	
Physical Data		
Temperature Range	Operating Storage	-40 °C to +85 °C -55°C to +125°C
MTBF	673000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	29 g	

Table 2-1 : Technical Specification

3 ID PROM Contents

Address	Function	Contents
0x01	ASCII ‘I’	**0x49**
0x03	ASCII ‘P’	**0x50**
0x05	ASCII ‘A’	**0x41**
0x07	ASCII ‘C’	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x2E**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0C**
0x17	CRC	**0x0E**
0x19	Version	**0x0A**

Table 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP606 is accessible in the I/O space of the IP.

Address	Symbol	Description	Size (Bit)	Access
0x00	INPUT	Input Register	16	R
0x03	GLBCONT	Global Control Register	8	R/W
0x04	INTENALH	Interrupt Enable Register Rising Edge	16	R/W
0x06	INTENAHL	Interrupt Enable Register Falling Edge	16	R/W
0x08	INTSTATLH	Interrupt Status Register Rising Edge	16	R/W
0x0A	INSTATHL	Interrupt Status Register Falling Edge	16	R/W
0x0D	IVEC	Interrupt Vector Register	8	R/W
0x0F	DEBTIME	Debounce Time Register	8	R/W

Table 4-1 : Register Set

4.2 Input Register (INPUT)

Bit	Symbol	Description	Access	Reset Value
15:0		16 bit input data. Register reflects the actual state of the inputs.	R	

Table 4-2 : 16 bit ADC Data Register

4.3 Global Control Register (GLBCONT)

After power up or reset all bits of this register are reset to '0'.

Bit	Symbol	Description	Access	Reset Value
7		Global interrupt flag 1 = an interrupt request of at least one of the 16 input channels is pending. Bit will be cleared if the appropriate interrupt is acknowledged by writing '1' to one of the interrupt status registers.	R	
6:3		Not used, undefined during reads	R/W	
2		Debounce control bit 1 = enables debounce circuit for all 16 inputs 0 = disables debounce circuit	R/W	
1		Not used, undefined during reads	R/W	
0		Global interrupt enable bit 1 = enables all possible interrupts of the TIP606 on interrupt request line INTREQ0# of the IP bus 0 = disables all interrupts	R/W	

Table 4-3 : Global Control Register (GLBCONT)

4.4 Interrupt Enable Register Rising Edge (INTENALH)

Bit	Symbol	Description	Access	Reset Value
15 . . . 0		Interrupt enable bit of corresponding channel for the rising edge Bit 0 enables interrupts of input channel 1 and bit 15 enables interrupt of input channel 15 rising edge. 1 = interrupt enabled 0 = interrupt disabled	R/W	

Table 4-4 : Interrupt Enable Register Rising Edge (INTENALH)

An interrupt on interrupt request line INTREQ0# of the IP bus is only generated if the global interrupt enable bit of the Global Control Register is set to '1'. After power up or reset all bits of this register are reset to '0'.

4.5 Interrupt Enable Register Falling Edge (INTENAHL)

Bit	Symbol	Description	Access	Reset Value
15 . . . 0		Interrupt enable bit of corresponding channel for the falling edge. Bit 0 enables interrupts of input channel 1 and bit 15 enables interrupt of input channel 15 for the falling edge. 1 = interrupt enabled 0 = interrupt disabled	R/W	

Table 4-5 : Interrupt Enable Register Falling Edge (INTENAHL)

An interrupt on interrupt request line INTREQ0# of the IP bus is only generated if the global interrupt enable bit of the Global Control Register is set to '1'. After power up or reset all bits of this register are reset to '0'.

4.6 Interrupt Status Register Rising Edge (INTSTATLH)

Bit	Symbol	Description	Access	Reset Value
15 0		Interrupt status bit of corresponding input for the rising edge. Bit 0 reflects the interrupt request state of input 1 and bit 15 reflects the interrupt request state of input 16 for the rising edge. Read '0': no interrupt request pending Read '1': interrupt request pending Write '1': clear pending interrupt After power up or reset all bits of this register are reset to '0'.	R/W	

Table 4-6 : Interrupt Status Register Rising Edge (INTSTATLH)

4.7 Interrupt Status Register Falling Edge (INTSTATHL)

Bit	Symbol	Description	Access	Reset Value
15 0		Interrupt status bit of corresponding input for the falling edge. Bit 0 reflects the interrupt request state of input 1 and bit 15 reflects the interrupt request state of input 16 for the falling edge. Read '0': no interrupt request pending Read '1': interrupt request pending Write '1': clear pending interrupt After power up or reset all bits of this register are reset to '0'.	R/W	

Table 4-7 : Interrupt Status Register Falling Edge (INTSTATHL)

4.8 Interrupt Vector Register (IVEC)

Bit	Symbol	Description	Access	Reset Value
7:0		8 bit interrupt vector loaded by software. After power up or reset all bits of this register are reset to '0'.	R/W	

Table 4-8 : Interrupt Vector Register (IVEC)

4.9 Debounce Time Register (DEBTIME)

Bit	Symbol	Description	Access	Reset Value
7:0		8 bit debounce preload value The value 0 in this register sets the debounce time to a minimum of 900µs (default after reset), if the debouncer is enabled in the Global Control Register. A value of 255 sets the debounce time to a maximum of 230.4ms. The debounce time is common for all inputs. The programmable debounce time can be calculated as follows: Debounce time = (*x*+1) * 900µs *x*: 8 bit preload value in the range from 0 to 255.	R/W	

Table 4-9 : Debounce Time Register (DEBTIME)

The debounce time value can have a tolerance of up to +/-15% of the calculated value. The debouncer will be enabled by writing '1' to bit 2 of the Global Interrupt Control Register.

5 Functional Description

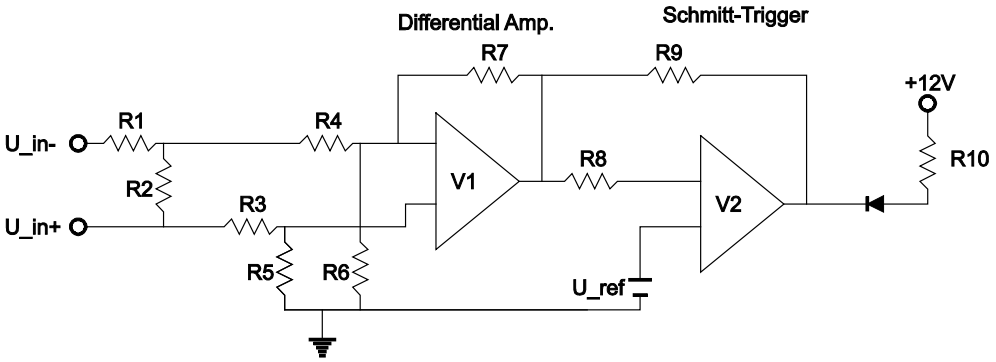


Figure 5-1 : Input Circuit

The input stage for each of the 16 inputs consists of a Differential Amplifier V1 followed by a Schmitt-Trigger V2. The Differential Amplifier provides a high impedance input for the input voltage. The input impedance between U_in+ and U_in- is typically 112 kOhm. The Differential Amplifier amplifies only the voltage difference across R2. The maximum frequency of the input signals should not exceed 10 kHz.

The thresholds of the TIP606 are determined by the resistor network around Opamp V2. At +25°C ambient temperature the TIP606 will detect a high level typically at input voltages greater than 14.0V and a low level at input voltages typically lower than 3.5V. These values can vary with the resistor deviation (max +/-1%) and the operating temperature of the module (see product specification for threshold bandwidth). The output voltage of each Schmitt-Trigger is fed to a separate optocoupler for each input. The outputs of the optocouplers are connected to the inputs of a FPGA which are doing the logic adaptation for the IP bus signaling.

To reduce power consumption of the TIP606 and avoid noise due to open inputs it is recommended to connect unused U_in+ inputs to a signal level of 28V and U_in- inputs to the respective ground signal.

The ground signal of the input signal source must be connected to the ground potential of the input stage (pin 49 and 50 on IP connector P2) to guarantee the specified switching threshold bandwidth.

The input stage of the TIP606 is designed to sense high side or low side switching.

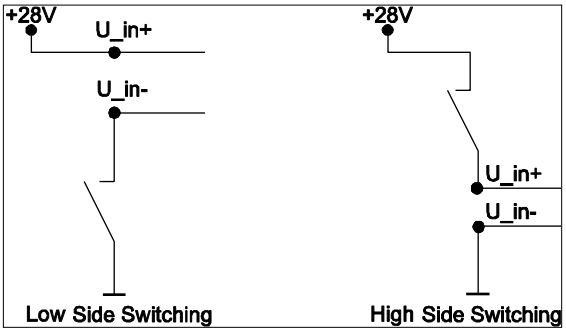


Figure 5-2 : High Side and Low Side Switching

6 Pin Assignment – I/O Connector

Pin	Signal
1	Input 1 +
2	Input 1 -
3	Input 2 +
4	Input 2 -
5	Input 3 +
6	Input 3 -
7	Input 4 +
8	Input 4 -
9	Input 5 +
10	Input 5 -
11	Input 6 +
12	Input 6 -
13	Input 7 +
14	Input 7 -
15	Input 8 +
16	Input 8 -
17	Input 9 +
18	Input 9 -
19	Input 10 +
20	Input 10 -
21	Input 11 +
22	Input 11 -
23	Input 12 +
24	Input 12 -
25	Input 13 +

Pin	Signal
26	Input 13 -
27	Input 14 +
28	Input 14 -
29	Input 15 +
30	Input 15 -
31	Input 16 +
32	Input 16 -
33	Not used
34	Not used
35	Not used
36	Not used
37	Not used
38	Not used
39	Not used
40	Not used
41	Not used
42	Not used
43	Not used
44	Not used
45	Not used
46	Not used
47	Not used
48	Not used
49	GND_I
50	GND_I

Table 6-1 : Pin Assignment I/O Connector

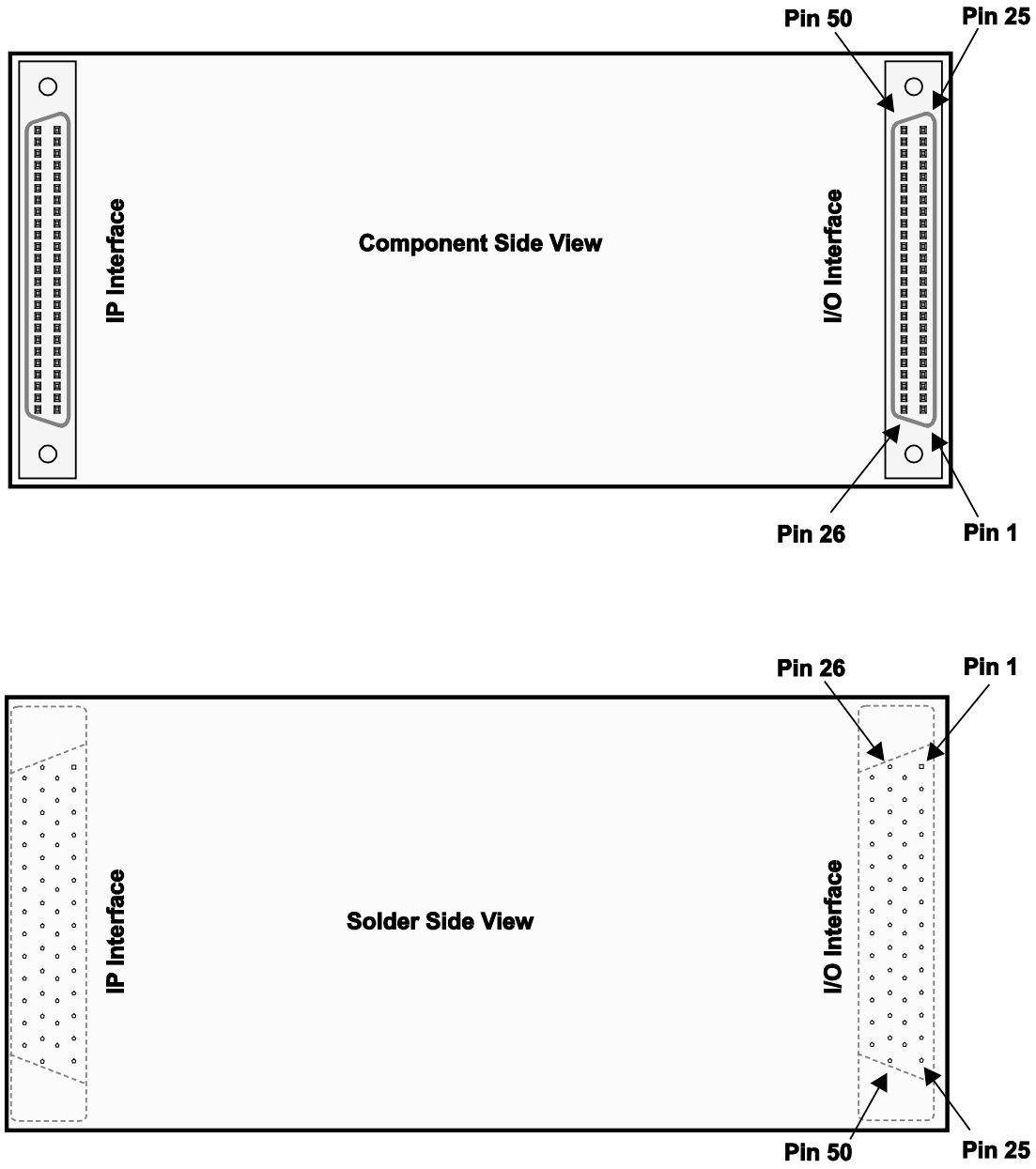


Figure 6-1 : IP Connector Orientation

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