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TEWS TECHNOLOGIES

TIP610

16/20 Channel TTL I/O

Version 1.0

User Manual

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TIP610-10R

16/20 Channel TTL I/O

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	December 1998
1.1	Addition chapter 5.2 “Hints”	January 1999
1.2	General Revision	May 2003
1.3	Output Current / IP Interrupt Line / General Revision	June 2004
1.4	New address TEWS LLC	September 2006
1.0.5	New notation of User Manual Issue	March 2009
1.0.6	General Revision	August 2014

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1 Product Description

The TIP610 is a single size IndustryPack® module with a TTL compatible I/O interface based on the Zilog Z8536 CIO (counter/timer and parallel I/O controller).

The TIP610 implements two independent, double-buffered, bidirectional 8 bit I/O ports, plus a 4 bit special-purpose I/O port.

Configuration jumper blocks permit to configure the 8 bit I/O port directions as permanent or programmable. The 4 bit port function is also configured by jumper configuration.

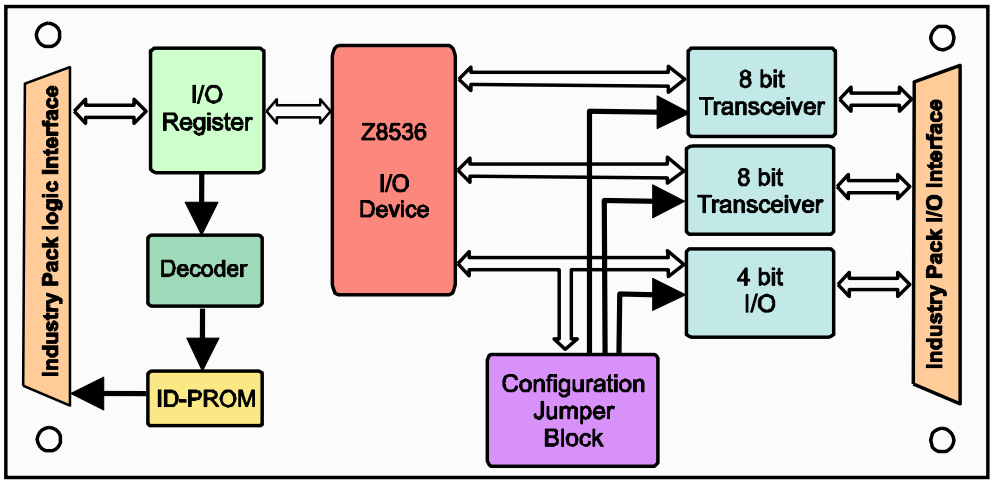


Figure 1-1 : Block Diagram

2 Technical Specification

Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
Counter/Timer Parallel I/O Controller (CIO)	Zilog Z8536 CIO	
Number of I/O Channels	16 TTL compatible I/O lines, arranged as two bi-directional 8 bit I/O ports plus a 4 bit TTL compatible control port (2x OUT, 1x IN, 1x I/O)	
Max. Output Current (per I/O line, if used as output)	Port A I/O signals : 24mA (source/sink) Port B I/O signals : 24mA (source/sink) Port C I/O signals : VOH min = 2.0V : 15mA (source) VOH min = 2.4V : 3mA (source) VOL max = 0.4V : 12mA (sink) VOL max = 0.5V : 24mA (sink)	
Wait States	ID Space : no wait states I/O Space (Z8536 CIO) : minimum 3 wait states	
Interrupts	The Z8536 interrupt pin is connected to the IP INTREQ0# line. The IP INTREQ1# line is not used.	
Interface Connector	50-conductor flat cable	
Power Requirements	240mA typical @ +5V DC	
Temperature Range	Operating Storage	0°C to +70°C -45°C to +125°C
MTBF	1279525 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	32 g	

Table 2-1 : Technical Specification

3 ID Prom Contents

Address	Function	Contents
0x01	ASCII ‘I’	**0x49**
0x03	ASCII ‘P’	**0x50**
0x05	ASCII ‘A’	**0x41**
0x07	ASCII ‘C’	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x2B**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0D**
0x17	CRC	**0x10**
0x19	Version -10R	**0x0A**
0x1B		**0x00**
…		**0x00**
0x3F		**0x00**

Table 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The TIP610 is accessed in the IP I/O space through the following set of direct accessible registers (implemented in the Z8536 CIO).

Address	Symbol	Description	Size (Bit)	Access
0x01	PORTC	CIO Port C Data Register	8	
0x03	PORTB	CIO Port B Data Register	8	
0x05	PORTA	CIO Port A Data Register	8	
0x07	CIOCSR	CIO Command and Status Register	8	

Table 4-1 : Register Set

The CIO Port A/B/C signals are mapped to the IP I/O connector pins by the use of extra on board I/O buffers.

The CIO Port C signals can be configured to be used as IP I/O signals and/or as enable and direction control signals for the Port A/B I/O buffers.

4.2 Indirect Addressable Registers

In addition to the direct accessible registers, the Z8536 CIO has 48 indirect addressable registers. These registers are used for port mode control and counter/timer functions.

Not all of the Indirect Addressable Registers are required for the operation of the TIP610.

Ind. Addr.	Name	Function	Size (bit)
0x00	MICR	Master Interrupt Control	8
0x01	MCCR	Master Configuration Control	8
0x02	PAIV	Port A Interrupt Vector	8
0x03	PBIV	Port B Interrupt Vector	8
0x04	CTIV	Counter / Timer Interrupt Vector	8
0x05	PCDP	Port C Data Path Polarity	8
0x06	PCDD	Port C Data Direction	8
0x07	PCSC	Port C Special I/O Control	8
0x08	PACS	Port A Control / Status	8
0x09	PBCS	Port B Control / Status	8
0x0A	C1CSR	Counter / Timer 1 Command and Status	8
0x0B	C2CSR	Counter / Timer 2 Command and Status	8
0x0C	C3CSR	Counter / Timer 3 Command and Status	8
0x0D	PADR	Port A Data Register	8
0x0E	PBDR	Port B Data Register	8
0x0F	PCDR	Port C Data Register	8
0x10	CT1CM	Counter / Timer 1 Current Count MSB	8
0x11	CT1CL	Counter / Timer 1 Current Count LSB	8
0x12	CT2CM	Counter / Timer 2 Current Count MSB	8
0x13	CT2CL	Counter / Timer 2 Current Count LSB	8
0x14	CT3CM	Counter / Timer 3 Current Count MSB	8
0x15	CT3CL	Counter / Timer 3 Current Count LSB	8
0x16	CT1PM	Counter / Timer 1 Preload MSB	8
0x17	CT1PL	Counter / Timer 1 Preload LSB	8
0x18	CT2PM	Counter / Timer 2 Preload MSB	8
0x19	CT2PL	Counter / Timer 2 Preload LSB	8
0x1A	CT3PM	Counter / Timer 3 Preload MSB	8
0x1B	CT3PL	Counter / Timer 3 Preload LSB	8
0x1C	CT1MO	Counter / Timer 1 Mode Specification	8
0x1D	CT2MO	Counter / Timer 2 Mode Specification	8
0x1E	CT3MO	Counter / Timer 3 Mode Specification	8
0x1F	CTCV	Counter / Timer Current Vector	8
0x20	PAMO	Port A Mode Specification	8
0x21	PAHS	Port A Handshake Specification	8

Ind. Addr.	Name	Function	Size (bit)
0x22	PADP	Port A Data Path Polarity	8
0x23	PADD	Port A Data Direction	8
0x24	PASC	Port A Special I/O Control	8
0x25	PAPP	Port A Pattern Polarity	8
0x26	PAPT	Port A Pattern Transition	8
0x27	PAPM	Port A Pattern Mask	8
0x28	PBMO	Port B Mode Specification	8
0x29	PBHS	Port B Handshake Specification	8
0x2A	PBDP	Port B Data Path Polarity	8
0x2B	PBDD	Port B Data Direction	8
0x2C	PBSC	Port B Special I/O Control	8
0x2D	PBPP	Port B Pattern Polarity	8
0x2E	PBPT	Port B Pattern Transition	8
0x2F	PBPM	Port B Pattern Mask	8

Table 4-2 : Z8536 CIO Indirect Addressable Registers

Access to the indirect addressable registers is controlled by a state machine and a hidden address pointer register (both implemented in the Z8536 CIO). The state machine has 3 different states: RESET state, state '0' and state '1'.

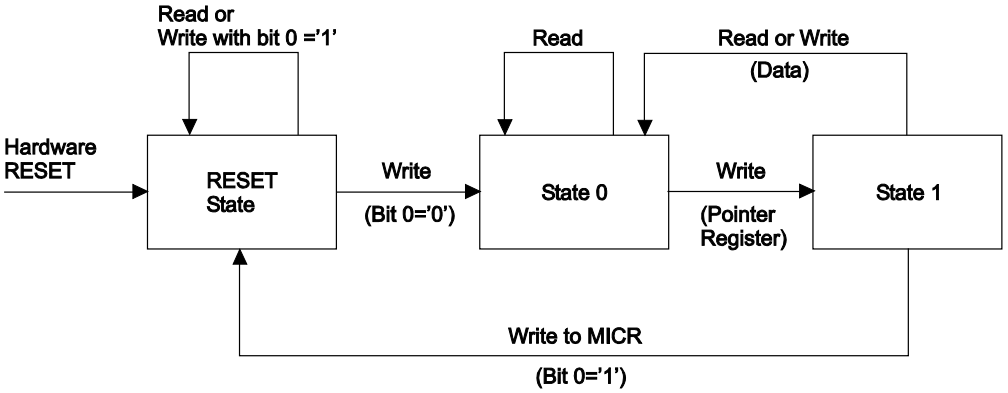


Figure 4-1 : CIO State Machine

An IP reset will set the state machine to the RESET state. In the RESET state it is only possible to access the RESET bit (bit 0) of the Master Interrupt Control Register (MICR).

When in RESET state, a CIOCSR register write access with bit 0 = '0' will set the state machine to state '0'.

When in state '0', a write to the CIOCSR register will set the internal register address pointer. This write access will also set the state machine to state '1'.

When in state '1', the first CIOCSR register access (read or write) will transfer data from or to the internal register that is actually selected by the internal address pointer. This access will also set the state machine back to state '0'.

Any CIOCSR register read in state '0' returns the contents of the actually selected register.

When not in the RESET state, any read of the CIOCSR register will set the state machine to state '0'. So a dummy read can be used to set the state machine to this known state.

If the state machine is in state '1', some of the internal operations of the CIO are disabled. So the state machine should never be left in state '1' longer as necessary.

Direct access to the PORTA, PORTB, and PORTC data registers has no effect on the state machine.

5 Programming

After power up or system reset the CIO Z8536 is in its initial state and the CIO ports A, B, C are disabled and configured to output direction. For normal operation of the TIP610, a minimum software initialization is required.

5.1 Required Software Initialization

The default jumper configuration supports programmable direction of I/O Port A and I/O Port B by the use of the CIO Port C signals.

Following example shows the minimum software initialization to set I/O Port A to output and I/O Port B to input. For other jumper configurations a different initialization is required.

- Write 0x00 to CIOCSR
- Write 0x01 to CIOCSR
- Write 0x00 to CIOCSR

  This sequence sets the Z8536 CIO to a known (reset) state
- Write 0x23 to CIOCSR

  This selects the CIO Port A Data Direction Register (PADD) for next operation.
- Write 0x00 to CIOCSR

  Sets all bits of CIO Port A as output.
- Write 0x2Bto CIOCSR

  This selects the CIO Port B Data Direction Register (PBDD) for next operation.
- Write 0xFF to CIOCSR

  Sets all bits of CIO Port B as input.
- Write 0x06 to CIOCSR

  This selects the CIO Port C Data Direction Register (PCDD) for next operation.
- Write 0x04 to CIOCSR

  Set direction for CIO Port C bits.
  (Bit 0 – Output, Bit 1 – Output, Bit 2 – Input, Bit 3 – Output)
- Write 0x01 to CIOCSR

  This selects Master Configuration Control Registers (MCCR) for next operation.
- Write 0x94 to CIOCSR

  Enables CIO Port A, Port B and Port C.
- Write 0x01 to PORTC

  Set Port A I/O buffer direction to Output, set Port B I/O buffer direction to Input, enable Port A I/O buffer, enable Port B I/O buffer.

5.2 Hints

The default jumper configuration requires programming of CIO Port C for enable and direction control of the on board Port A/B I/O buffers.

- Enable CIO Port C in the MCCR (Master Configuration Control Register)

  Bit 4 : 1 = enable 0 = disable

- Set direction of CIO Port C signals in the PCDD (Port C Data Direction)

  Bit 0: 0 = output (will be used for Port A direction control)

  Bit 1: 0 = output (will be used for Port B direction control)

  Bit 2: 1 = input

  Bit 3: 0 = output (will be used for Port A/B enable control)

- Set the CIO Port C signal outputs for proper enable and direction control of the on board I/O buffers in the PCDR (Port C Data Register)

  Bit 0: Port A I/O Buffer Direction 1 = output 0 = input

  Bit 1: Port B I/O Buffer Direction 1 = output 0 = input

  Bit 2: This bit is input only

  Bit 3: Port A/B I/O Buffer Enable 1 = disable 0 = enable

Other than the default jumper configuration may require a different CIO Port C programming.

CIO Port C Bit 0 function is board I/O and/or Port A/B I/O buffer direction control.
CIO Port C Bit 1 function is board I/O Output only and/or Port A/B I/O buffer direction control.
CIO Port C Bit 2 function is board I/O Input only.
CIO Port C Bit 3 function is board I/O Output only and/or Port A/B I/O buffer enable control.

CIO Port C Bit 2 direction must always be configured as Input before CIO Port C is enabled.

Before CIO Ports A/B/C are enabled, be sure that the CIO Port A/B/C bit direction programming matches the direction jumper configuration for the extra on board Port A/B/C I/O buffers.
E.g. if I/O Port B is configured as permanent Input by jumper, than the CIO Port B direction must also be programmed as Input BEFORE CIO Port B is enabled.

6 Installation

6.1 Jumper Installation

Default jumper settings:

Jumper	Settings
J1	1-2
J2	2-4
J3	3-4
J4	5-6
J5	1-2
J6	1-2

Table 6-1 : Default jumper settings

Use only the specified jumper combinations (see chapter "Jumper Configuration").

Use only one jumper for each of the jumper blocks J3, J4, J5 and J6.

Disregarding this note could damage the TIP610.

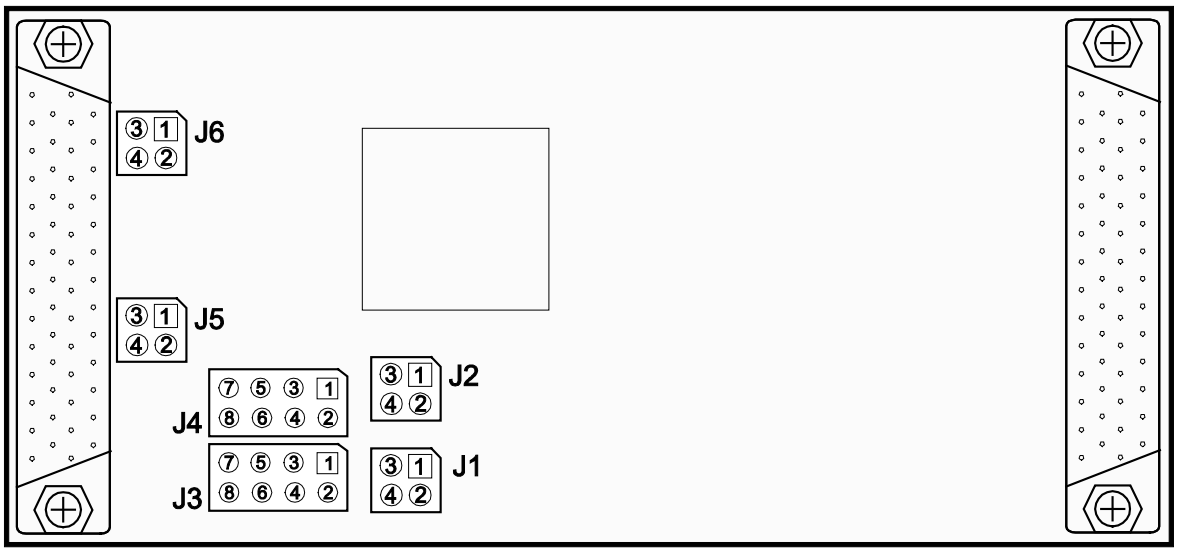


Figure 6-1 : Jumper Location

6.2 Jumper Configuration

Jumper J1/J2: Direction Control for Port C Bit 0 I/O Buffer

Position J1	Position J2	Function
1-2	**2-4**	Configures the Port C Bit 0 I/O Buffer as OUTPUT
3-4	1-2, 3-4	Configures the Port C Bit 0 I/O Buffer as INPUT

Jumper J3: Direction Control for Port B I/O Buffer

Position	Function
1-2	Port B I/O Buffer is set to OUTPUT
3-4	Port B I/O Buffer direction is set by CIO Port C Bit 1 0 = Input, 1 = Output
5-6	Port B I/O Buffer direction is set by CIO Port C Bit 0 0 = Input, 1 = Output
7-8	Port B I/O Buffer is set to INPUT

Jumper J4: Direction Control for Port A I/O Buffer

Position	Function
1-2	Port A I/O Buffer is set to OUTPUT
3-4	Port A I/O Buffer direction is set by CIO Port C Bit 1 0 = Input, 1 = Output
5-6	Port A I/O Buffer direction is set by CIO Port C Bit 0 0 = Input, 1 = Output
7-8	Port A I/O Buffer is set to INPUT

Jumper J5: Enable Control for Port A I/O Buffer

Position	Function
1-2	Port A I/O Buffer Enable is controlled by CIO Port C Bit 3 0 = Enable, 1 = Disable
3-4	Enables Port A I/O Buffer

Jumper J6: Enable Control for Port B I/O Buffer

Position	Function
1-2	Port B I/O Buffer Enable is controlled by CIO Port C Bit 3 0 = Enable, 1 = Disable
3-4	Enables Port B I/O Buffer

Table 6-2 : Jumper Configurations

7 Pin Assignment – I/O Connector

Pin	Assignment
1	I/O Port A Bit 0
2	I/O Port A Bit 1
3	I/O Port A Bit 2
4	I/O Port A Bit 3
5	I/O Port A Bit 4
6	I/O Port A Bit 5
7	I/O Port A Bit 6
8	I/O Port A Bit 7
9	AGND
10	I/O Port B Bit 0
11	I/O Port B Bit 1
12	I/O Port B Bit 2
13	I/O Port B Bit 3
14	I/O Port B Bit 4
15	I/O Port B Bit 5
16	I/O Port B Bit 6
17	I/O Port B Bit 7
18	AGND
19	I/O Port C Bit 3 (output only)
20	I/O Port C Bit 2 (input only)
21	I/O Port C Bit 1 (output only)
22	I/O Port C Bit 0
23	AGND
24 … 50	Not Used

Table 7-1 : Pin Assignment (I/O Connector)

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